Modeling in microelectronics at microwave/millimeter-wave frequencies and innovative circuit design

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**MODELING IN MICROELECTRONICS AT
MICROWAVE/MILLIMETER-WAVE FREQUENCIES AND
INNOVATIVE CIRCUIT DESIGN**

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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**Modeling in Microelectronics at Microwave/Millimeter-wave Frequencies and
Innovative Circuit Design**

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Summary

The advancement in microwave theories along with fabrication capabilities of modern foundries in terms of material processing and improved microelectronic devices have brought about unprecedented MMIC designs in terms of its size, power and frequency of operation. Through the discussion of active device modeling and innovative circuit design, this research work hopes to exploit the advancements in microelectronic devices and to achieve breakthrough in terms of circuit design methods and circuit performances.

In this thesis, the empirical modeling for an AlGaIn/GaN HEMT device capable of high power performance is described. The modeling for an AlGaIn/GaN HEMT was selected due to the material characteristics of the device but the modeling procedures and empirical formulations are not limited to GaN based devices. The research work covers the modeling process from data acquisition to the characterization of the device using empirical formulas and the implementation of the proposed model in circuit simulators.

From the bias independent small-signal linear model, the extrinsic parasitic parameters are extracted and subsequent modeling work is performed on the evaluated intrinsic device performance. Due to the large biasing voltages that can be applied on the HEMT device, emphasis was given to ensure that simulation will not result in errors and the characteristics are adequately modeled.

A charge modeling method applied on the model allows the charge model to model the symmetrical nature of the HEMT device. The active current which represents a major non-linearity of the HEMT is modeled with a proposed new current model to more accurately capture the characteristics at critical regions of the device

characterization. The forward diode current model is also described and a similar equation form is adopted for the breakdown current model.

The AlGaIn/GaN HEMT model implemented in circuit simulator is validated against measured performance of the device and good match is obtained between the large-signal measurements and modeled results. The small-signal performance of the HEMT model is also tested with good agreement to the measured results over a range of selected V_{GS} biasing which covers the pinch off, peak transconductance and gm compression regions.

A part of the thesis work will be dedicated to innovative active circuit design methods for the design of active circulators and a class E high efficiency power amplifier with the use of a coupled line load. The presented circuits serve to offer simplified design methodologies together with providing design equations to derive at the circuit parameters. Through the fabrication of the designed circuits, the importance of having an accurate device model is highlighted for the design of active circuits using CAD tools.

Chapter 1 Introduction

Monolithic microwave integrated circuits (MMICs) have become an important and integral part of our lives today. Modern day MMICs can be found in a wide range of applications ranging from commercial products such as the cellular communication systems to complex satellite systems and radar systems used in the defence industries. The advancement in the field of MMICs in terms of its performance and compactness in size is the result of the union between the understanding in microwave/millimeter-wave frequencies theories and microelectronics fabrication competencies.

The active device which is the key component for MMICs has seen tremendous progress over the past fifty years not solely in terms of the frequency of operation but also the achievable output power density [1]. For example, indium phosphide (InP) based double heterojunction bipolar transistors had demonstrated a $f_{\max}$ of greater than 800 GHz [2], silicon germanium (SiGe) and CMOS based RFICs working above 100 GHz [3], and AlGaIn/GaN based power amplifiers operating in the W-band frequency spectrum [4],[5]. A GaN power amplifier design capable of achieving pulsed output power of greater than 400W with PAE greater than 40% across the frequency range from 2.9 GHz to 3.5 GHz was demonstrated [6]. GaN power amplifier capable of achieving pulse output power of 750W was also demonstrated but has a narrow bandwidth performance at 2.14GHz [7].

As listed above, each material will have traits superior to others and selecting the appropriate material system to be used in circuit design will depend on the intended application. Certain materials such as InP and GaAs are more proficient in high frequency operation (beyond w-band operation) while material such as GaN display superiority when used in high power applications.

1.1 Modeling and circuit design

Alongside with the improvements to the device technology and fabrication techniques, having a device model which characterizes the performance of the active device is a critical portion for the success of the device technology. From the fabrication point of view, foundries can pick up critical information on the stability of the fabrication process from analyzing the various parameters of the device model and evaluate on the maturity of the fabrication process across time. From the commercial viewpoint, a device model is essential for the comprehensive release of fabricated devices to allow circuit designers to perform circuit design simulations prior to the fabrication of the integrated circuit design [8].

The use of CAD tools for rf circuit design is the most commonly practiced method given the convenience in terms of the time required to analyze and study the different circuit simulations for the implemented designs in addition to the precise performance prediction between simulated and fabricated performance with the modern day CAD tools. To fully exploit the benefits of the CAD tools and the potential of the device technology, an accurate device model is paramount to the success of an MMIC design. An accurate device model starts from the data acquisition process where obtaining the set of good quality experimental data is critical to the success of subsequent characterization process. The device model will only be accepted after verification with the measured data and is well suited for the design needs of the circuit to be designed.

In this work, the emphasis will be on the study of an active device model suitable for CAD implementation and active circuit design methods that complement the device model derived to achieve greater accuracy and efficiency when it comes to active device modeling and the designing of certain active circuitries.

1.2 Challenges with existing active device model and circuit design

In the recent years, much attention has been given to GaN based high electron mobility transistors (HEMTs) in the design of rf power amplifiers. The favorable properties of the GaN material such as high breakdown voltage and current density for GaN material [9] have enabled the designed MMICs to be biased at a higher voltage and give a much higher power density as compared to its GaAs counterpart. The increase in power density over materials such as GaAs meant that less power combining effort is required to achieve the required power output for the designed high power MMICs, which would in turn reduce any power loss in the combining stages and allow higher power efficiency to be achieved. That is one of the reasons why GaN based devices are highly sought after for the designing of power MMICs.

Very often, modifications and adaptations to the existing device model which has shown to be successful in characterizing a particular technology is applied when modeling devices for the latest technology with similar working principles. In the case of the GaN based active devices, many large-signal models were based on models previously used to characterize GaAs based devices and were shown to be successful in obtaining good device performance prediction [10]-[14]. However, the unique properties of the GaN based devices has presented modeling challenges previously not encountered with GaAs based devices. For instance, the high breakdown voltage for GaN based devices allows higher biasing voltages to be applied but this will lead to issues with circuit simulations if the current models derived for GaAs MESFET devices are directly applied with no modifications.

In the area of rf circuit design, circuit designers are constantly exploring ways to improve rf circuit design methodology with the aim of a more simplified design process, improved performance such as the broadband performing circuits and

even looking at ways to reduce the overall footprint of the overall designed circuit. An accurate device model will complement the conception of novel circuit with the use of CAD tools to assist in hypothetical testing of new design ideas or concepts.

1.3 Addressing the challenges in active device modeling and circuit design

In this thesis, the characterization of an active device will be presented via the modeling of an AlGaIn/GaN HEMT device. The proposed modeling procedures and empirical formulas will be able to model active devices not restricted to the GaN based HEMT demonstrated in this thesis. Alongside with the characterization of the active device, part of the thesis work will also be based on novel microwave circuit design to simplify the circuit design process and highlight the importance of an accurate device model in MMIC design work.

The breakdown of the content for this research work is as follows. Chapter 1 of the thesis highlights the emphasis on modeling work and circuit design. To fully exploit the benefits with the different material technology, the use of CAD tools for circuit design must be complemented with an accurate large-signal model for the active device.

An overview of the active device to be modeled will be covered in chapter 2 where the discussion will begin with the figure of merits for a selected group of material systems. A brief account will be provided for the AlGaIn/GaN HEMT device including the discussion on the heterostructure, which forms the basis for high electron mobility action in a transistor device. The chapter will conclude with the issues faced during device characterization and challenges to be addressed in this thesis work.

Chapter 3 of the report will focus on the characterization of an active device starting with the account of the modeling procedures adopted in this work. Next, the use of pulsed DC measurement for the characterization of the AlGaIn/GaN HEMT will be discussed. Dispersion effects due to gate lag and drain lag effects will be demonstrated. More details will be provided on the use of the pulsed DC measurement system to characterize the effects of quiescent biasing for pulsed measurements. The last part of chapter 3 will touch on the characterization of the parasitic for the active device which is not dependent on the applied bias and the subsequent intrinsic element extraction derived for device modeling.

The focus on chapter 4 will be on the modeling of the large-signal elements present in the model proposed. An empirical modeling approach with novel current formulation is proposed for the modeling of the IV profile for the experimentally obtained data. The empirical method aims to improve the overall modeling ability of the current profile with adaptations to improve the match before peak transconductance is achieved and also the linear region for the IV traces. The same empirical model will be applied to the modeling of the pulsed DC current profile and the association is made between the quiescent bias and the pulsed DC current profile. The issues with biasing at large voltages for the HEMT devices will also be looked at with proposed solution to better represent the device performance when simulating beyond the fitting data acquired. The large-signal model elements responsible for the modeling of diode current and representing the breakdown phenomenon will also be amended to be able to handle the large biasing voltages. A novel charge modeling approach will also be discussed which would make the modeling of charge sources more straightforward and not face convergence issues when performing simulations.

Chapter 5 of the report will be on the discussion of the large-signal model implemented for the modeling of the active device on electromagnetic CAD tools

followed by the verification of the modeled device with comparison to the measured data to ascertain the effectiveness of the proposed large-signal model.

In chapter 6, novel circuit designs in the form of an active circulator and a high efficiency class E power amplifier are introduced. The novel design method serves to simplify the complexity of the rf circuit design process with the analytical study on the various circuit elements. Having an accurate device model would greatly help in the design process of the circuits by saving on the time, effort and possibly fabrication cost should the designed circuit fail to meet its specifications.

Finally, in chapter 7, the conclusion and the future work that could be developed beyond this thesis work will be presented.

Chapter 2 Semiconductor devices

In the recent years, there is a growing interest in the use of GaN based devices for MMIC applications given its advantages such as high output power capability and high breakdown voltages compared to its GaAs counterparts and other competing technologies. Maturity in the processing and fabrication techniques over the years has greatly exploited the potential of the GaN technology. MMICs designed and fabricated with AlGaIn/GaN HEMTs such as the high efficiency power amplifier has displayed a power added efficiency of greater than 60% [15],[16] and amplifiers having a gain greater than 15 dB operating in W-band frequency spectrum optimized at 95 GHz [17] was also designed and fabricated.

The properties of GaN material introduced complications in the characterization of the GaN based devices where the empirical models must be adjusted accordingly to better suit the application demands of the GaN based devices. In the first part of this chapter, the focus will be on the discussion of different semiconductor materials used in the fabricated active devices and the associated device properties in relation to the material properties.

This is then followed by the discussion of HEMT device and heterostructures. HEMT devices which are capable of higher frequency operations coupled with GaN material has allowed higher power operations to be achieved at higher operating frequency. The chapter will conclude with the issues faced with the modeling of GaN HEMT devices which would be addressed in this thesis report. The modeling method proposed in this thesis work will be able to model active devices not limited to GaN based devices but also active devices from other material system such as GaAs and Si.

2.1 Semiconductor materials

A table of comparison between several semiconductor materials highlighting the various properties useful for high power and high frequency operation of transistors built on such materials is shown in Table 2.1 [9]. The various properties listed in Table 2.1 are also indicative measures of the different performance aspects of the active device. The electron mobility listed for GaAs and GaN in Table 2.1 is the typical 2-dimension electron gas (2DEG) mobility achievable for AlGaAs/InGaAs and AlGaN/GaN heterostructures.

Property	Si	GaAs	α -SiC (6H)	GaN
Energy Gap (eV)	1.12	1.42	2.9	3.4
Dielectric Constant	11.7	12.9	9.6	9.5
Electron mobility (cm^2/Vs)	1500	8500	330	1200
Hole mobility (cm^2/Vs)	500	400	60	<30
Saturation velocity (m/s)	10^5	1.2×10^5	$2\text{-}2.5 \times 10^5$	$2\text{-}2.5 \times 10^5$
Thermal conductivity ($\text{W}/\text{cm}^\circ\text{C}$)	1.31	0.46	4.9	1.5
Breakdown electric field (V/cm)	3×10^5	4×10^5	3.8×10^6	2×10^6

Table 2.1 A table of comparison between semiconductor materials

For the material properties listed in Table 2.1, the energy band gap and breakdown electric field will determine the biasing voltages that can be applied on the transistor device before breakdown of the material occurs. This property is also a measure of the rf power handling capability which is crucial for high power amplifier applications. The frequency of operation that the active device is capable of achieving will be largely determined by the electron mobility and the saturation velocity of the material property. The thermal conductivity property will dictate the degradation of the performance for the active device with the increase in the

channel temperature of the active area during rf operation, a property critical to the application of high power amplifiers.

In comparison, the GaN material has the highest energy bandgap and has higher breakdown electric field over GaAs which makes it the preferred material for high power applications. The lower dielectric constant of GaN also meant that it has lower capacitive loading effects as compared to other materials. Although the α -SiC has comparable properties to GaN based devices and well suited for high voltage and temperature operation, the lack of heterostructure results in the low electron mobility and limiting the high frequency operation for the fabricated device such as SiC MESFETs.

2.2 High electron mobility transistor (HEMT)

The principle behind the development of HEMT devices is the consequence on the work of heterostructures. Owing to the 2DEG present in the heterostructures, HEMT devices were able to operate at higher frequency up to the millimeter-wave range as compared to ordinary transistors topology. This section will give a brief description of the HEMT device followed by the discussion on HEMT fabricated with GaN material and the associated issues encountered with device modeling for GaN based device. The issues will be addressed in this thesis work in the aim of improving the modeling capability of the device model across different material systems.

2.2.1 Heterostructures

A heterojunction which forms the basis for a heterostructure is the interface that is formed between two materials typically semiconductor materials as a result of each

material having a different energy band gap value. When a material with a larger energy bandgap value such as AlGaAs is grown on GaAs which has a relatively smaller energy bandgap value, the alignment of the Fermi level will result in the diffusion of conduction carriers to the side of the material with lower energy bandgap. The conduction carriers will be located at the interface of the two materials and form a 2DEG and has a high sheet charge density. The band diagram of the heterojunction highlighting the 2DEG is shown in Figure 2.2.

By using undoped materials, the scattering mechanism of the charge flow due to the doping impurities will be eliminated allowing heterostructures such as AlGaAs/GaAs and AlGaN/GaN to have good low field electron mobility and concurrently achieve excellent high field electron saturation velocity.

Figure 2.2 Band diagram of AlGaAs/GaAs heterojunction depicting the 2 DEG at the interface of the two materials

2.2.2 GaN based HEMT

Due to the wide bandgap material properties of GaN, HEMTs fabricated with AlGaN/GaN materials are able to attain high breakdown voltage and able to sustain very high channel operating temperature with its good thermal conductivity property. AlGaN/GaN HEMT devices are also capable of operating at high ambient temperature with an individual tested AlGaN/GaN HEMT device fabricated on SiC substrate exhibiting device failure at 500°C [18]. The high sheet charge density as a result of the heterojunction between AlGaN/GaN also meant that AlGaN/GaN HEMTs are able to achieve high current densities. Such properties make AlGaN/GaN HEMTs desirable for high power applications and recording power densities up to 30W/mm on SiC substrate [19].

The schematic for the AlGaN/GaN heterostructure of the HEMT device to be modeled in this thesis work is shown in Figure 2.3. In addition to the heterojunction structure shown in Figure 2.2, an additional layer of capping GaN is grown between the devices' terminals and the undoped AlGaN barrier layer to protect the AlGaN/GaN layers beneath.

Figure 2.3 Schematic of the AlGaN/GaN structure for the modeled transistor device

For modeling and verification purposes, a commercially fabricated AlGaIn/GaN HEMT on SiC substrate will be measured and modeled. The results comparing the measured and modeled AlGaIn/GaN HEMT across a range of biasing voltages will be presented to evaluate the effectiveness of the proposed device model. The chosen device has a gate periphery of $2 \times 125 \mu\text{m}$, gate length of $0.25 \mu\text{m}$ and a gate to drain spacing of $4 \mu\text{m}$. A picture of the abovementioned AlGaIn/GaN HEMT device on SiC substrate is shown in Figure 2.4.

Figure 2.4 Picture of $0.25 \times 2 \times 125 \mu\text{m}$ AlGaIn/GaN HEMT on SiC substrate

2.2.3 Issues with modeling GaN based HEMT devices

The issues with regards to the modeling of GaN based devices such as AlGaIn/GaN HEMT can either be attributed to the inherent properties of the GaN based device or belonging to the case of immaturity in the fabrication technology. One of the technological related problems is the current collapse phenomenon experienced by GaN based devices as a result of the trap states at the surface and buffer layers. Many researchers have since focus on the problem of current

collapse and how the behavior can be modeled and characterized. As the process matures, more understanding was gained for the source of the current collapse mechanism and the magnitude of the current collapse issue has been alleviated with the recent studies on the electric field at the gate corner and in the active channel [20]-[22].

Issues that will be addressed in this work which is still prevalent in the device characteristics is the ‘kink’ behavior at the knee voltage of the IV characteristics which would be discussed in the modeling section in chapter 4. Non-technology related issues with modeling unique to GaN based devices is the large breakdown voltage property which enabled large biasing voltages to be applied to the device. Direct application of models previously used to fit the GaAs devices such as the active current model and the diode current model will face erroneous simulation results with the failure to consider high voltage biasing that could be applied to the large-signal model.

Another issue that would be addressed in this work would be the large-signal charge modeling process which will be reviewed and a more straightforward charge modeling method will be presented which will prevent any charge convergence issues with commercial circuit simulators.

In summary, the different types of material system were first discussed in this chapter highlighting the different figure of merits for the materials listed. The advantages of devices fabricated with GaN devices have also brought about challenges in the modeling and device model implementation. With the rising attention on the use GaN based devices, the chapter proceeded to discuss on HEMT devices with fabricated with GaN material. The chapter concluded with the issues with the empirical model to be addressed in this thesis work. The

proposed modeling techniques and empirical models should possess the versatility to model active devices from various materials system.

Chapter 3 Modeling and characterization techniques

The first and most important step for the modeling of an active device is the device characterization step where the accuracy of the data acquired will have a direct effect on the accuracy of the derived model especially when an empirical approach to the modeling of the device has been adopted in this thesis work. The type of measurements to perform for device characterization is usually dependent on the intended applications of the device and the data set collected should encompass information for the operating conditions of the modeled active device.

For the first part of the chapter, the modeling procedures for the characterization of an active device are described. The modeling procedures starting with data acquisition up to the acceptance of the device model will be discussed. The type of measurements usually performed for device characterization includes static, pulsed DC measurements, continuous wave s-parameters measurements with static DC and pulsed s-parameters measurements with static or pulsed DC. For the AlGaIn/GaN HEMT modeled in this research work, continuous wave s-parameters with static DC measurements will be performed.

The focus of the second part of the chapter will be on the pulsed measurement used in the characterization of the active device. Pulsed measurements in the form of pulsed IV plays a critical role in the modeling of active devices manifested with self-heating issues. Pulsed IV measurements are also employed for device characterization at biasing points beyond the safe operating area (SOA), particularly useful for devices capable of withstanding large biasing voltages. Different aspects of pulse measurements such as the charge trapping effects and the quiescent biasing that affects the pulsed IV profile will be discussed.

Finally, the chapter will end with the discussion on the parasitic element extraction which consists of the rf measurement contact pads, gate, drain and source metallization which are beyond the active region and independent of the biasing voltages applied. The extracted parasitic elements were used to evaluate the intrinsic characteristics of the active device and the discussions on the modeling of the bias dependent intrinsic elements would be covered in the subsequent chapter.

3.1 Modeling procedures

The modeling procedures for the characterization of an active device can be summarized into a flow chart shown in Figure 3.1. The first step of device characterization is the data acquisition step which is critical to the success of the modeled device. To model the active device, multi-bias measurements which capture the varying s-parameters profile with the applied external bias, together with the biasing conditions (instantaneous voltages and current) will be measured. Power measurements such as power sweep measurements and loadpull measurements should also be performed at this stage of data acquisition. Empirical model will be based on the data set collected and the accuracy of the obtained data set is of paramount importance.

The second step of the modeling procedures is an optional step as it involves the modeling of the breakdown characteristics and breakdown voltage value which will completely destroy the device under test or cause serious degradation of the device. For the case of GaN based devices, not every laboratory is equipped with the necessary equipment and setup to measure the high breakdown voltage which is typically greater than hundredth of volts. For the completeness of the modeled device, the breakdown voltage can either be obtained from the data sheet or estimated from literature working on the same device topology and configuration.

Figure 3.1 Flow chart for empirical modeling of active device

The next step of the modeling procedures is the parasitic elements extraction step which will characterize the parasitic due to the bond pad and metallization of the gate, drain and source terminals which are independent of the biasing voltages applied. This will allow us to extract the intrinsic parameter values which would be modeled accordingly with the empirical model.

Having ascertained all the required parameter values for the intrinsic elements, the comparison between the simulated and experimental data can be used to evaluate the fidelity of the extracted model. Comparisons can be made for the multi-bias s -parameters and also the large-signal power measurements performed. If discrepancies exist, the modeling step of parameters extraction should be revisited and the variables could be fine tuned to achieve an improved match between the simulation and experimental results. Only when the simulation data corresponds well to the measured data and well suited to the design needs of the circuit designer, the device characterization is considered to be complete and the device model can be accepted.

3.2 Pulsed DC measurement characterization

The notion for the use of pulsed DC measurements is to observe and study the response of the active device under the excitation of short pulsed stimuli and with a sufficiently short pulse width coupled with a low pulse duty cycle, the state of the trapped charges and the channel of the active device remains unchanged. The obtained current characteristic is also known as the isothermal current characteristics of the active device which is free of the self-heating effects inherent in GaN based devices under static DC measurement conditions.

Pulsed DC measurement is commonly used to effectively characterize the effects of charge trapping for GaN based transistors [23] and also study the gate and drain lag effects due to the different quiescent biasing applied [24]-[28]. Pulsed DC measurements also allows experimental data to be collected at biasing points outside of the safe operating area (SOA) extending the measurement biasing conditions towards higher voltages, attain higher current densities and prevent any breakdowns or serious degradation of the measured active device.

The challenge of the pulse measurement system is the ability to obtain a distinguished narrow pulse width with precise experimental data acquisition sampling points. Very often, how narrow a pulse width can be used for experimental measurement is dependent on the leading and trailing spikes of the applied pulse. The inevitable use of connecting cables to the bias tees of the measurement setup would introduce delays to the pulse and must be very carefully dealt with for both the gate and drain pulsing terminals. Typically, computer controlled software are used to manage and coordinate the excitation of the gate and drain pulse and to capture the measured data accordingly.

In this research work, the minimum measurement pulse width obtainable from the pulse measurement setup not impeded by the leading and trailing spikes with credible acquired data from the voltage and current pulses is $1\mu\text{s}$. To minimize any accumulated heating in the active channel, long pulse period of 5ms was employed resulting in a small duty cycle of 0.02%. Although it has been illustrated in some literature that the effects of self-heating can only be fully eradicated with sub-micron pulse widths [28]-[30], characterization for the charge trapping and dispersion effects can still be performed with the quasi-isothermal pulsed measurements obtained with the pulsing system available.

3.2.1 Characterization of charge trapping effects

The charge trap state within the semiconductor material layers can be described as a function of the quiescent and instantaneous biasing alongside the channel temperature [26] of the active region. With the meaningful selection of quiescent biasing points, the effects of drain and gate lag effects with relation to charge trapping can be studied accordingly [27],[28]. By maintaining the constant temperature of the test environment, the effects of gate and drain lag can be observed with quasi-isothermal current measurements.

To illustrate the drain and gate lag effects, a total of three pulsed measurements with isothermal or quasi-isothermal measurements is required [28]. The first set of measurements would require both the gate and drain to have a quiescent biasing of 0V which would create a quasi-isothermal measurement that avoids any trapping effects as a result of the applied biasing. During the pulsing measurement, the voltage at the gate terminal is pulsed down (depletion mode device) and the voltage at the drain terminal is pulsed up. In view of the fast filling phenomenon of the trap states in comparison to the pulse width, the trap states for gate and drain lag effects are filling during the pulse measurement process.

To illustrate the gate lag effects, a second set of pulsed IV measurements with quiescent biasing when the gate terminal is at pinched off biasing voltage level and the drain terminal at 0V is required. When pulsed IV is performed at these quiescent biasing voltages, both the voltages at the gate and drain terminal are pulsed up. When the voltage at the gate terminal is pulsed up, the trap states are emptying and the speed of the states emptying are slower than the pulsed duration and the state of gate traps can be said to be of the same level as the state before pulsed voltages is applied. The effects of the gate lag can be observed in Figure 3.2 (a) with the decrease in saturation current of the pulsed IV plots but maintaining the conductance value at the saturation region from the superposition of the two pulsed IV traces.

For the drain lag effects, a set of pulsed IV measurements with gate terminal quiescent biasing in the pinched off biasing voltage and the drain terminal biased with a quiescent voltage greater than 0V (typically 20V) is required. When performing pulsed measurement, the voltage at the drain terminal is pulsed down when the instantaneous voltage is less than 20V and pulsed up when the instantaneous biasing voltage is greater than 20V. When comparing to the set of pulsed IV measurements with quiescent biasing gate voltage at pinched off voltage and the quiescent drain voltage at 0V, more trap states are occupied for the case with applied drain biasing greater than 0V and the drain lag effects can be observed when superimposing the two pulsed IV plots as shown in Figure 3.2 (b). The pulsed IV recorded a higher saturation current when the instantaneous V_{DS} is lower than 20V which is expected as the charges are emptying much slower than the duration of the excitation pulse. The pulsed current gradually converge to the same value beyond the instantaneous biasing of 25V as the duration of trap states filling up is within the pulse excitation for both sets of pulsed data.

Figure 3.2 (a) Demonstration of gate lag effects: pulsed IV with quiescent biasing $V_{GS0} = 0V$ and $V_{DS0} = 0V$ (red trace, no markers) with pulsed IV with quiescent biasing $V_{GS0} = -5V$ and $V_{DS0} = 0V$ (blue trace with x markers) (b) Demonstration of drain lag effects: pulsed IV with quiescent biasing $V_{GS0} = -5V$ and $V_{DS0} = 0V$ (red trace, no markers) with pulsed IV with quiescent biasing $V_{GS0} = -5V$ and $V_{DS0} = 20V$ (blue trace with x markers)

3.2.1 Characterization of pulsed IV with quiescent biasing

Following the discussion on the charge trapping property for GaN based devices from the comparison between pulsed IV current plots with different quiescent biasing, it can be noted that the quiescent gate and drain biasing for the active device are factors of the pulsed IV profile. The dependence of the quiescent biasing must be highlighted in the empirical functions for pulsed current profile modeling in addition to the other dependent variables such as the instantaneous voltages. The pulsed current can then be expressed as the following

$$I_{DS} = f(V_{GS0}, V_{DS0}, V_{GSi}, V_{DSi}, T) \quad (3.1)$$

where T is the channel temperature of the active device. The channel temperature is influenced by the ambient temperature and the presence of self heating effects which is dependent on the dissipated power of the active device. If pulsed operation is required for the final designed circuit, it is critical to take into considerations the quiescent biasing during the data acquisition phase of the modeling process to ensure that the required data set is captured and modeled accordingly.

The studies have highlighted the importance of the quiescent biasing when characterizing the active current and in this thesis work, the dependence of quiescent biasing on the pulsed IV profile of the GaN based device will be characterized with the proposed current model. In this work, it was assumed that the pulse width of $1\mu\text{s}$ together with the long pulse period of 5ms (0.05% duty cycle) will not result in the increase in channel temperature significantly with the applied pulsing voltages.

3.3 Bias-independent parasitic values

S-parameters data collected from the measurement setup are accurate up to the DUT measurement plane and the DC current voltage characteristics data are based on the voltage and currents measured at the plane of the DC sources. Therefore, when modeling of the AlGaIn/GaN HEMT is concerned, it is necessary to de-embed the parasitic effects which are bias independent in order to perform device modeling based on the intrinsic parameters of the measured AlGaIn/GaN HEMT. The characterization of the extrinsic parameters that models the rf measurement contact pads, gate, drain and source metallization which are beyond the active region and independent of the biasing voltages will be discussed in this section of the report.

3.3.1 Equivalent circuit model

The first step of determining the intrinsic parameters of the measured AlGaIn/GaN HEMT is to determine the parasitic which are the lumped element values external to the intrinsic device shown in Figure 3.3. The cold FET method based on the work in [31] and [32] was used to extract the extrinsic lumped element values with the aid of several essential S-parameter measurements performed on the AlGaIn/GaN HEMT. It will be shown that the parasitic elements extracted together with the device circuit shown in Figure 3.3 are sufficient in describing the s-parameters performance at various biasing points including the s-parameters under pinched off condition and at the active biasing region.

Figure 3.3 Bias dependent small-signal equivalent circuit with lumped elements

By biasing the AlGaIn/GaN HEMT in deep pinch off condition, the conductivity of the channel will be fully suppressed. This is reflected in the s-parameters measured where both the S11 and S22 will depict the capacitive trend. At the

abovementioned deep pinch off condition, the conduction layer is depleted and a fringing capacitance term can be used to describe the depletion which extends at each side of the gate terminal. The imaginary portion of the Y-parameters for the device under deep pinch off condition will be reduced to the following [32]:

$$\text{Im}(Y_{11}) = j\omega(C_{pg} + 2 \cdot C_b) \quad (3.2)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -j\omega C_b \quad (3.3)$$

$$\text{Im}(Y_{22}) = j\omega(C_b + C_{pg}) \quad (3.4)$$

where C_{pg} and C_{pd} are the parasitic capacitance values at the gate and drain terminal respectively and C_b is the fringing capacitance value. The value of C_b can be evaluated from the linear profile of the imaginary portion for Y_{12} against frequency and the values for the parasitic gate and drain capacitance can be easily obtained by studying the imaginary portion of the Y-parameters.

To obtain the extrinsic parameter values for the resistances and inductances, several s-parameter measurements when the AlGaN/GaN HMET is in the forward conduction state with different gate current must be performed under the cold FET condition where zero drain bias voltage is applied. When obtaining the S-parameter measurements for the forward conduction state, it is crucial to ensure that the capacitive effect of the gate has been eliminated by observing the s-parameter measurements recorded. Under such biasing condition, the Z-parameters can be reduced to the following [32]:

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + j\omega(L_s + L_g) \quad (3.5)$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \quad (3.6)$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) \quad (3.7)$$

where R_c is the channel resistance under the gate. From either the imaginary part of Z_{12} or Z_{21} , the corresponding value of L_s can be determined and subsequently the parasitic element values for L_g and L_d can be evaluated. With the series of forward conduction S-parameter measurements of different I_g current, a linear relationship of the real portion of the measured Z_{11} with respect to the inverse of the gate current can be plotted. The intercept of the linear relationship will be the sum of R_s , R_g and $R_c/3$ and the values of R_g , R_d , and R_s can be easily evaluated from the other real portion of the Z-parameters knowing the channel technological parameter R_c .

For the AlGaIn/GaN HEMT device modeled, the parasitic element values are shown in Table 3.1. This same set of parasitic values will be used for the extraction of intrinsic parameters to illustrate the effectiveness of the small-signal model at different biasing conditions. Three different gate biasing voltages were selected to depict the capability of the selected small-signal model which include bias at pinched off condition ($V_{GS} = -5V$), near peak transconductance ($V_{GS} = -3V$) and the active region ($V_{GS} = -1V$) and the comparison between the measured and modeled s-parameters is shown in Figure 3.4 (a), (b) and (c) respectively. The drain voltage was selected to be 15V for all three biasing conditions.

Parasitic Elements	Cpg (F)	Cpd (F)	Lg (H)	Ld (H)	Ls (H)	Rg (Ω)	Rd (Ω)	Rs (Ω)
Values	1.29e-13	1.26e-13	6.32e-11	8.2e-11	4.61e-12	3.87	7.56	2.91

Table 3.1 Extracted parameter values for the extrinsic parasitic elements

(a)

(b)

(c)

Figure 3.4 (a) Comparison between measured (blue traces) and modeled (red traces) s-parameters (a) $V_{GS} = -5V$, $V_{DS} = 15V$, (b) $V_{GS} = -3V$, $V_{DS} = 15V$, (c) $V_{GS} = -1V$, $V_{DS} = 15V$.

Good match was obtained between the measured and modeled results across the selected biasing values after some fine tuning of the intrinsic elements obtained from the initial cold FET parameter extraction method. The extrinsic elements are bias independent unlike the intrinsic elements which are dependent on the biasing conditions. Thus, the accuracy of the extracted extrinsic elements can be verified by performing the parameter extraction process for devices at different biasing conditions. While other literatures have introduced enhancements to the small-signal model and the extraction methods [33]-[37], the existing parasitic extraction method has shown to be sufficient for the subsequent intrinsic elements extraction and modeling of the large-signal model.

3.3.2 Extracted intrinsic data

After determining the parasitic element values, the intrinsic parameters of the AlGaIn/GaN HEMT can be extracted. The first step of intrinsic parameter extraction is the evaluation of the intrinsic biasing voltages on the intrinsic device. The voltage drop across the resistance of the measurement setup and the parasitic resistances based on the current values measured must be subtracted to derive the voltage at the intrinsic plane of the device. However, direct application of de-embedding for the parasitic resistances to obtain the intrinsic voltages will generate non-discrete intrinsic gate and drain voltages as compared to the applied extrinsic voltages during the measurement process. With non-discrete intrinsic gate and drain voltages, the parameter extraction process such as the active current modeling will not be straightforward.

With the aid of the interpolation function of EM simulators such as ADS, the list of discrete intrinsic voltages with respect to the applied external biasing can be evaluated. The list of intrinsic voltages with respect to the applied extrinsic biasing will be stored in a separate data file which would be recalled by the simulator. Subsequent intrinsic parameters extraction process will be based on the discrete intrinsic voltages evaluated and the importance of the parasitic extraction process together with proficient quantifying of the resistance for the experimental setup is crucial for the accuracy of the subsequent intrinsic data evaluation.

With the intrinsic voltages listing, the extraction of the large-signal data such as the intrinsic IV and intrinsic forward current characteristics can be evaluated. The comparison between the extrinsic and intrinsic IV is shown in Figure 3.5. The plot shown in Figure 3.5 (b) is based on intrinsic voltages and the increase in current values is expected as a result of the potential drop at the extrinsic plane of the device.

Figure 3.5 (a) Measured drain current with respect to applied V_{DS} with different applied V_{GS} (b) Drain current with respect to simulated V_{DSi} and V_{GSi}

Similarly, the comparison between the measured diode current based on external applied bias and the computed diode current based on the intrinsic voltages is show in Figure 3.6.

Figure 3.6 (a) Measured diode current with respect to applied V_{GS} with V_{DS} kept at 0V (b) Diode current with respect to simulated V_{GSi} with V_{DSi} kept at 0V

The method of parasitic de-embedding was extended to the multi-bias s-parameters measurements as well. Negative elements were used in the EM simulators to

obtain the intrinsic parameter values to be used for subsequent charge modeling process. The comparison between the measured s-parameters and the extracted intrinsic s-parameters based on intrinsic voltages is shown in Figure 3.7.

Freq (50MHz to 10 GHz)

(e)

Freq (50MHz to 10 GHz)

(f)

Freq (50MHz to 10 GHz)

(g)

Freq (50MHz to 10 GHz)

(h)

Figure 3.7 (a) Measured S11 plots (b) S11* plots after de-embedding extrinsic parasitic values (c) Measured S12 plots (d) S12* plots after de-embedding extrinsic parasitic values (e) Measured S21 plots (f) S21* plots after de-embedding extrinsic parasitic values (g) Measured S22 plots (g) S22* plots after de-embedding extrinsic parasitic values (The intrinsic s-parameters plots are based on

intrinsic biasing voltages). The s-parameter plots are grouped according to the V_{GS} and V_{GSi} respectively which corresponds to the pinched off, peak transconductance and gm compression region.

In summary, the modeling procedures to characterize an active device deriving at an acceptable device model were presented in this chapter in the form of a flow chart. Different issues and challenges faced during the modeling process were highlighted in the first section of the chapter. The characterization of charge trapping effects and the applied quiescent biasing that shape the pulsed IV profile when performing pulsed IV measurements were also discussed, highlighting the considerations required if pulsed operations for the active device is required. Concluding the chapter was the discussion on the topic of parasitic elements extraction process. The parasitic elements independent of the applied biasing were extracted and subsequently used to evaluate the intrinsic elements values of the active device. The comparisons between the measured data value and the intrinsic elements values to be used for empirical formulation were also presented.

Chapter 4 Large-signal modeling

The large-signal modeling for an active device will model the bias-dependent nonlinear elements of the equivalent electrical circuit model. The main nonlinear elements for the equivalent circuit model discussed in this research work includes the various current and charge sources. The current sources include the gate to drain, gate to source and drain to source current sources likewise for the charge sources which include the gate to drain, gate to source and drain to source charge sources. The various nonlinear elements used to represent the active device characteristics can be shown in the large-signal schematic in Figure 4.1. The nonlinear elements are functions of the voltages applied on the device and the quiescent biasing will also be a factor of consideration for the nonlinear function of the pulsed current profile.

Figure 4.1 Nonlinear elements of the large-signal model

The accuracy of the active current model has been critical to the success of power MMIC design. The linear and pinched off region has been linked to the design success for circuits operating in the switched mode configuration where the load line was more accurately synthesized. So far, no work has worked on modeling the effects on the linear region due to impact ionization. The current values in the region prior to peak transconductance also have to be more adeptly represented in the design of high efficiency power amplifier and usually the accuracy in this region is compromised with existing empirical equations. The possibility of high voltage that could be applied must be taken care as well to prevent the generating of any erroneous current values.

The issue of charge conservation has always been the concern of large-signal capacitance modeling in order to maintain the simulation integrity of the charge model and not have any convergence issues during simulation. The conventional approach to charge modeling also has to address the issue of path dependent integration due to the equivalent large-signal charge model used. Regardless of the proposed charge modeling methods, the empirical formulation must be able to adequately describe the capacitance characteristics and the criteria of charge conservation must still be satisfied.

In this chapter, the active current modeling will first be presented. A detailed discussion will be on the modified current model and the derivation of its model parameters. The discussion will also touch on the pulsed characteristics of the active current and how the model is adapted to model large voltage biasing. Next the diode current modeling of the large-signal model will be discussed. Concluding the chapter will be the discussion on the derivation of the nonlinear charge model which reduces the complexity of empirically describing the multi-bias capacitance characteristics from the s-parameters measurement data and also the inclusion of switching functions to ensure no convergence issue would be encountered when performing circuit simulations with commercial simulators.

4.1 Active current modeling

The active current is the most important and prevailing source of nonlinearity in the modeling of the active device and many research works have been devoted to obtaining a good fit between measurement data and simulation model. Very often, established empirical current models used to model GaAs HEMTs and MESFETs such as the Chalmers model [38], Curtice model [39] or the EEHEMT model [40] were used to describe the active current (I_{DS}) characteristics for GaN HEMTs. In other cases, the I_{DS} forms of established models were modified to better describe the behavior of GaN HEMT devices [41]-[47]. In this thesis, the proposed modified I_{DS} formulation will provide a more straightforward extraction of the model parameters and provide better match between the experimental and simulated data and contribute more to the understanding of the AlGaN/GaN HEMT device.

4.1.1 Static DC current modeling

The basis of the active current models was established to model the major source of nonlinearity which is the bias dependent active current characteristics of III-V field effect transistors (FETs) and has been adapted to model different types of FET such as MESFET, MOSFET and HEMT devices.

Over the years, improvements were made to the Curtice model to enhance the modeling capability with the inclusion of additional parameters to better characterize the peak transconductance region [48]-[55]. Improvements were also made to enhance the modeling accuracy of the Angelov model to better characterize the transconductance and pinch off to on mode transition region [56]-[60]. To improve the differentiability of the EEHEMT1 model, other forms of

empirical formulations have been studied to replace the piecewise functions [61]-[67].

To better model the active current for GaN devices, the Angelov model has been modified notably of the inclusion of the V_{DS} dependence for the evaluation of V_{pk} parameter [41]-[43], [68]-[70]. Even with adaptations and modifications to the empirical formulated current models to better model AlGaIn/GaN transistor devices, the typical empirical formula used to describe the I_{DS} characteristics have the general form of $I_{DS} = f(V_{GS}) \cdot (1 + \lambda \cdot V_{DS}) \cdot (\tanh(\alpha \cdot V_{DS}))$. The constant and fixed λ term (parameter KAPA for EHEMT model) was used to model the channel length modulation effects for the transistor device but the product of the transfer function with the λ term is insufficient in describing the relationship between the conductance and the applied gate to source voltage in the saturation region of the active current profile. Discrepancies between modified current model and experimental data especially in the saturation region before the peak transconductance were still evident in the research works [41],[42],[71],[72].

To improve on the accuracy of modeling the device's active current, a new method was proposed to model the conductance as a separate entity. The proposed method not only serves to improve the modeling accuracy of the active current, it also simplifies the modeling parameter extraction process. Besides improving the modeling of the conductance for the active devices, the proposed model also seeks to address the issue of the 'kink' phenomenon at the linear region of the active IV. The phenomenon can be observed from the measured devices in many of the research work but was not adequately addressed [46], [73]. The modeling of the 'kink' behavior is achieved with the alpha function which is critical for the modeling of the device turn on resistance value and also the simulating of the device loadline for high efficiency power amplifier with zero voltage switching designs (e.g. Class-E, Class-F power amplifier).

To better model the asymmetrical profile of the transconductance characteristics for GaN HEMTs, modifications were made to the Chalmer's model which segments the transconductance profile based on the gate-to-source voltage (V_{GS}) in which peak transconductance occurs (V_{pk}) [74], [75]. The enhancements to improve the modeling capability presented in this thesis work will be based on abovementioned property of the modified Chalmer's model and the breakdown of the active current formulation to characterize the I_{DS} profile are described in equations 4.1 to 4.16

$$I_{ds} = [f(V_{GS}) + g(V_{GS}, V_{DS}) \cdot V_{DS}] \cdot \tanh(\alpha \cdot V_{DS}) \quad (4.1)$$

where

$$f(V_{GS}) = I_{pk1} \cdot (1 + \tanh(\varphi_1)) + I_{pk2} \cdot \tanh(\varphi_2) \quad (4.2)$$

$$g(V_{GS}, V_{DS}) = (\lambda_1 \cdot (1 + \tanh \beta_1)) + \lambda_2 \cdot \tanh(\beta_2)) \cdot h(V_{DS}) \quad (4.3)$$

$$h(V_{DS}) = 0.5 \cdot \left(1 + \tanh(-\text{grad} \cdot (V_{DS} - V_{\text{shift}}))\right) \quad (4.4)$$

$$\varphi_1 = P_1 \cdot V_{\text{eff}p1} \quad (4.5)$$

$$\varphi_2 = P_2 \cdot V_{\text{eff}p2} \quad (4.6)$$

$$\beta_1 = Q_1 \cdot V_{\text{eff}p1} \quad (4.7)$$

$$\beta_2 = Q_2 \cdot V_{\text{eff}p2} \quad (4.8)$$

$$V_{\text{eff}p1} = 0.5 \cdot (V_{gsp} - V_{gspa}) \quad (4.9)$$

$$V_{\text{eff}p2} = 0.5 \cdot (V_{gsp} + V_{gspa}) \quad (4.10)$$

$$V_{gspa} = \sqrt{V_{gsp}^2 + q^2} \quad (4.11)$$

$$V_{gsp} = V_{GS} - V_{pk} \quad (4.12)$$

$$\alpha = \alpha_{range} \cdot \left(1 - \tanh\left(\alpha_{grad} \cdot (V_{DS} - \alpha_{volt_shift})\right)\right) + \alpha_{min} \quad (4.13)$$

$$\alpha_{range} = (\alpha_1 \cdot V_{GS} + \alpha_2) \cdot \alpha_{limit} \quad (4.14)$$

$$\alpha_{limit} = \frac{\alpha_1}{(\alpha_1^2 + q^2)^{0.5}} \cdot 0.5 \cdot \tanh\left(10 \cdot \left(V_{GS} - \left(-\frac{\alpha_2}{\alpha_1}\right)\right)\right) + 0.5 \quad (4.15)$$

$$\alpha_{volt_shift} = \alpha_3 \cdot V_{GS} + \alpha_4 \quad (4.16)$$

The proposed formulation for the active current modeling can be grouped into three portions which models the transfer function (eqn. 4.2), the output conductance (eqn. 4.3) and the linear or triode region ($\tanh(\alpha \cdot V_{DS})$) of the I_{DS} plots for the transistor device. The alpha term which models the linear region of the I_{DS} plots is a function of a hyperbolic tangent function with the mid-point and the magnitude term of the hyperbolic tangent function having V_{GS} dependence. The alpha function employed in this work is capable of modeling the kink phenomenon [76]-[78] at the linear region and has a limiting function to prevent a negative range value.

To have a more physical current prediction for the modeled device operating at high biasing voltages, eqn. 4.4 was included as a product at the output conductance function. Eqn. 4.4 is a function of V_{DS} and the primary function is to control the conductance at high V_{DS} biasing which would be described in the subsequent subsection.

4.1.1.1 Modeling the current profile of the saturation region

Modeling of the active current would be separated into three main portions, mainly, the saturation region, the linear region and lastly the region for high V_{DS} operation.

To improve the output conductance modeling capability of the current function, the same methodology used for modeling the transfer function was adopted and equation 4.3 was established. Evaluating with the same V_{pk} value as the transfer function, the use of λ_1 , λ_2 , Q_1 and Q_2 gives more flexibility to control the rate of change and the trend of the output conductance with the changing V_{GS} in comparison to the other current models in literature. To ensure that the introduction of this variable gradient term will not generate erroneous transconductance values, the terms β_1 and β_2 in the current model are made to be a function of $(V_{GS} - V_{pk})$ which is identical to that used in the portion of the equation that is responsible for the computation of transconductance (g_m). This will ensure that the g_m evaluated with circuit simulators will not result in multiple g_m peaks due to the variable gradient term. Therefore, the V_{pk} term used in the active current formulation remains consistent with convention definition of the gate-to-source voltage in which the peak transconductance occurs.

The conventional method of parameters extraction for the active current is based on evaluating the transconductance of the active current characteristics. For the proposed method, the extraction of parameters is performed directly from the obtained measured active current plots. Considering the hyperbolic tangent function in equation 4.1, the value of the hyperbolic tangent function is at unity at the saturation region which means modeling function can be simplified to a family of straight line functions with gradient of $g(V_{GS}, V_{DS})$ and y-intercept of $f(V_{GS})$ with respect to the applied V_{DS} .

To extract the equation parameters for $g(V_{GS}, V_{DS})$, the gradients for the active current plots beyond a sufficiently large applied V_{DS} would be extracted. The sufficiently large applied V_{DS} must be selected such that current plots are operating in the saturation region and way beyond the linear region of the active current plots. In the case of the measured device, the gradients of the active current plots beyond the applied V_{DS} of 10V were extracted. With the gradients values evaluated, the

values for equation $f(V_{GS})$ can be evaluated for a particular applied V_{DS} in the saturation. The applied V_{DS} of 15V was selected to evaluate the values for $f(V_{GS})$. A plot of static active current with respect to the applied V_{DS} is shown in Figure 4.2(a). Based on the proposed methodology, the evaluated gradient and y-intercept of the static active current plot at the saturation region is shown in Figure 4.2(b) and Figure 4.2(c) respectively.

Figure 4.2 (a) Static active IV current profile (b) evaluated $g(V_{GS})$ function with respect to V_{GS} (c) evaluated $f(V_{GS})$ function with respect to V_{GS} . Values of $g(V_{GS})$ extracted from gradient in the saturation region and $f(V_{GS})$ extracted at an applied V_{DS} of 15V.

From the plot of $g(V_{GS})$ with respect to the applied V_{GS} , the parameters V_{pk} , λ_1 , λ_2 , Q_1 and Q_2 can be extracted. V_{pk} corresponds to the applied V_{GS} value where the peak occurs, λ_1 , and Q_1 controls the magnitude and the rate of increase for the for the $g(V_{GS})$ formulation before V_{pk} and λ_2 together with Q_2 parameter controls the magnitude and rate of increase for the $g(V_{GS})$ beyond the V_{pk} value. This proposed method gives better control for the overall active current function to model any output conductance profile not achievable with existing current models. In a similar manner, the equation parameters for $f(V_{GS})$ can be extracted from the plot of $f(V_{GS})$ with respect to V_{GS} . I_{pk1} and P_1 controls the magnitude and rate of increase for the $f(V_{GS})$ before V_{pk} value and both I_{pk2} together with P_2 parameter controls the $f(V_{GS})$ beyond the V_{pk} value.

Based on the abovementioned parameter extraction process, the parameters extracted for the $g(V_{GS})$ and $f(V_{GS})$ functions are shown in Table 4.1 and Table 4.2. The comparison between the evaluated and modeled plots for $f(V_{GS})$ and $g(V_{GS})$ is shown in Figure 4.3.

V_{pk}	$f(V_{GS})$				$g(V_{GS})$			
	P_1	P_2	I_{pk1}	I_{pk2}	Q_1	Q_2	λ_1	λ_2
-2.78	5	0.3	0.01	0.32	2.3	0.3	0.00082	-0.0045

Table 4.1 Extracted parameters for $f(V_{GS})$ and $g(V_{GS})$ of static current profile

α					
α_{grad}	α_1	α_2	α_3	α_4	α_{min}
0.46	2.2	5.4	-0.074	0.0665	0.23

Table 4.2 Extracted parameters for α of static current profile

Figure 4.3 (a) comparison between measured (red trace with no markers) and modeled (blue trace with x markers) $g(V_{GS})$ function with respect to V_{GS} (b) comparison between measured (red trace with no markers) and modeled (blue trace with x markers) $f(V_{GS})$ function with respect to V_{GS} . Values of $g(V_{GS})$ extracted from gradient in the saturation region and $f(V_{GS})$ extracted at an applied V_{DS} of 15V.

It can be observed from Figure 4.3(a) and 4.3(b) that the conductance and transfer function was well matched throughout the V_{GS} biasing with the proposed formulation. In addition to improving the modeling of conductance at low V_{GS} which is crucial to the design of high efficiency power amplifiers with reduced conduction angle (e.g. class C, D, E and F high power amplifier), the proposed method is able to capture the self-heating effects of the active current plots adequately. The self-heating effect is typically evident from non-pulsed measurement data which results in negative output conductance (R_{ds}) profile for the I_{DS} plots beyond certain V_{GS} biasing values. Ways to model this phenomenon previously would be to include a thermal sub-circuit and evaluate the decrease in current value as a result of the power dissipated [8], [79] or in the case of EEHEMT model, the inclusion of a power dissipation factor in the current equation to account for the decrease in current value [80].

In the proposed approach, the self-heating effects can be modeled in a more straightforward manner by directly considering the gradient of the I_{DS} plots for different V_{GS} . Apart from the direct parameters extraction approach for the proposed empirical equations, the extraction method does not require the availability of a pulsing system to extract parameter values for the current characteristics without the presence of self-heating effects. The characterization of the self-heating effects can be achieved with the modified output conductance function which is now independent of the transfer function.

4.1.1.2 Modeling the current profile of the linear region

The ‘kink’ phenomenon observable at the linear region of the active current plots can be attributed to the effects of impact ionization. The topic of impact ionization is not new and has been studied in detailed in previous work [81]–[83]. The kink effect is a result of the potential that was accumulated at the trap sites outside of the channel region with the effect of the accumulated potential amplified by the transconductance of the device resulting in additional current contribution. To characterize the effects due to impact ionization, the alpha function in equation 4.13 has to be modeled accordingly. The linear region of the active current profile is the product of the hyperbolic tangent function with the family of straight line curves of the saturation region. From an empirical approach, the alpha function can be extracted having already determined the parameters for $f(V_{GS})$ and $g(V_{GS}, V_{DS})$ by taking the inverse hyperbolic tangent function. This would give us the value of alpha that depicts the kinked profile to perform empirical parameter extraction for modeling. The dependence of the alpha value on the V_{GS} extracted from the measurement data can be shown in Figure 4.4.

Figure 4.4 Alpha extracted from measurement data depicting the dependence on applied V_{GS}

It was found that the V_{DS} applied have a weak effect on the impact ionization and is primarily affected by the V_{GS} applied on the device. This is in agreement to the study of impact ionization where the potential accumulated at the gate terminal affects the current behavior at the linear region. A similar form for the alpha equation was proposed for the modified Chalmer's equation [13] but it was not designed to model the effects due to impact ionization on the I_{DS} plots and does not highlight the V_{GS} dependence of the parameters α_{range} and α_{mid} . With the added V_{GS} dependence on the alpha function in equation 4.13, it is crucial that the evaluated alpha remains positive to prevent any erroneous negative current from being generated. In order to prevent a negative alpha value as a result of modeling the V_{GS} dependence, a limiting function has been put in place and it is capable of limiting the α_{range} function to a minimum value of 0 regardless of the polarity evaluated for parameters α_1 and α_2 . Four selected V_{GS} biasing depicting the simulated values for the alpha function used to describe the linear characteristics is shown in Figure 4.5.

Figure 4.5 Comparison between simulated and calculated alpha value for V_{GS} biasing (a) $V_{GS} = -1.5V$ (b) $V_{GS} = -1V$ (c) $V_{GS} = -0.5V$ and (d) $V_{GS} = 0V$

It is shown in Figure 4.4 that the alpha function introduced to model the effects due to impact ionization was able to match the alpha values calculated from the experimental data with a certain degree of accuracy across the various biasing values applied. In Figure 4.5a, the discrepancies between the calculated and modeled alpha at low V_{DS} for V_{GS} at $-1.5V$ will not affect the modeling outcome as the alpha value corresponds to the current profile for the active current close to the pinched off value. Near pinched off value, a small difference will result in the

large discrepancies shown between the calculated and modeled but will translate to a small difference in the active current plots.

The improved match with the implementation of the alpha model is illustrated in Figure 4.6. Figure 4.6a shows the comparison between the measured data and the current model with the proposed alpha function and Figure 4.6b shows the comparison the measured data and the current model without the alpha model. Although both Figure 4.6a and Figure 4.6b demonstrate a good match for the measured and simulated current values at the saturation region, the proposed alpha equation would give a more accurate representation for the turn on resistance and loadline analysis for large-signal circuit design.

(a)

Figure 4.6 Comparison between measured and modeled I_{DS} (a) with alpha model and (b) without alpha model

4.1.2 Pulse current modeling

As mentioned in Chapter 3, the quiescent biasing is a variable for the measured pulsed IV profile and the characterization will be discussed in this subsection. The same current equation and modeling techniques described in chapter 4.1.1 will be used to model the effects of the quiescent biasing on the pulsed IV profile.

The set of biasing voltages that has been selected to model the effects of quiescent biasing was based on the pulsed IV profile at the quiescent biasing of 0V for both the gate and drain terminal. At this quiescent biasing, the electric field within the device is negligible and the trap states are unoccupied. The measured pulsed IV with this quiescent biasing would represent the maximum potential for the measured device if thermal issues due to self-heating and the issues due to trap states are not present. Three quiescent gate biasing voltages have been selected for the measurements which includes the gate biasing at pinched off (-5V), biasing in

the vicinity of the peak transconductance (-3V) and biasing at the active region (-1V). As for the quiescent drain voltage, the range of biasing from 0V to 30V with a step voltage of 10V was selected.

The same extraction procedures of the empirical current parameters for the static IV current profile were adopted for the pulsed IV current profile parameters extraction. To reduce the number of modeling parameters to be included in this section, the parameters for the $h(V_{DS})$ function listed in equation 4.3 which is used to model the device current under large biasing conditions will not be presented. The function $h(V_{DS})$ will reduce the conductance of the current formulation at large V_{DS} biasing and will remain at unity at prior to the onset of conductance reduction. The extracted list of device parameters is shown in Table 4.3 and 4.4 with the q parameter kept at 0.01.

V_{GS0}	V_{DS0}	V_{pk}	$f(V_{GS})$				$g(V_{GS})$			
			P_1	P_2	I_{pk1}	I_{pk2}	Q_1	Q_2	λ_1	λ_2
-1	0	-2.55	2.4	0.16	0.04	0.558	1.8	0.01	0.0002	-0.053
-1	10	-2.55	2.4	0.16	0.028	0.512	1.8	0.01	0.00055	-0.048
-1	20	-2.55	2.4	0.16	0.016	0.466	1.8	0.01	0.0009	-0.043
-1	30	-2.55	2.4	0.16	0.004	0.42	1.8	0.01	0.00125	-0.038
-3	0	-2.45	2.4	0.16	0.04	0.504	1.8	0.01	0.0002	-0.029
-3	10	-2.45	2.4	0.16	0.028	0.5	1.8	0.01	0.00055	-0.024
-3	20	-2.45	2.4	0.16	0.016	0.496	1.8	0.01	0.0009	-0.019
-3	30	-2.45	2.4	0.16	0.004	0.492	1.8	0.01	0.00125	-0.014
-5	0	-2.35	2.4	0.16	0.04	0.45	1.8	0.01	0.0002	-0.005
-5	10	-2.35	2.4	0.16	0.028	0.44	1.8	0.01	0.00055	0
-5	20	-2.35	2.4	0.16	0.016	0.43	1.8	0.01	0.0009	0.005
-5	30	-2.35	2.4	0.16	0.004	0.42	1.8	0.01	0.00125	0.01

Table 4.3 Extracted parameters for $f(V_{GS})$ and $g(V_{GS})$ of pulsed current profile

V_{GS0}	V_{DS0}	alpha					
		α_{grad}	α_1	α_2	α_3	α_4	α_{min}
-1	0	0.25	3.333	6.833	-0.0727	0.0503	0.15
-1	10	0.25	3.333	6.833	-0.0727	0.0503	0.15
-1	20	0.25	3.333	6.833	-0.0727	0.0503	0.15
-1	30	0.25	3.333	6.833	-0.0727	0.0503	0.15
-3	0	0.3	3	6	-0.0893	0.0696	0.16
-3	10	0.3	3	6	-0.0893	0.0696	0.16
-3	20	0.3	3	6	-0.0893	0.0696	0.16
-3	30	0.3	3	6	-0.0893	0.0696	0.16
-5	0	0.35	2.667	5.167	-0.106	0.089	0.17
-5	10	0.35	2.667	5.167	-0.106	0.089	0.17
-5	20	0.35	2.667	5.167	-0.106	0.089	0.17
-5	30	0.35	2.667	5.167	-0.106	0.089	0.17

Table 4.4 Extracted parameters for alpha function of pulsed current profile

From the parameters extracted in Table 4.3, it can be observed that the effects on the pulsed current profile across various quiescent biasing can be systematically characterized with the varying parameters for the saturation region of the pulsed current profile ($f(V_{GS})$, $g(V_{GS})$). Parameters I_{pk1} and λ_1 display a weak dependence on the quiescent gate biasing and can be shown to be dependent on the applied quiescent drain voltage. A linear dependence on quiescent biasing can be drawn for the above mentioned parameters. On the other hand, parameters in the saturation region I_{pk2} and λ_2 beyond the V_{pk} value has shown to be dependent on both the gate and drain quiescent bias. The V_{pk} parameter has also shown to display a linear dependence with the quiescent gate biasing and can be modeled accordingly.

For the linear region, all the modeling parameters α_{grad} , α_{min} , α_1 , α_2 , α_3 and α_4 displayed linear dependence on the quiescent gate biasing with little to no dependence on the drain quiescent biasing. This is expected as the linear region

has shown dependence on the gate biasing voltage as mentioned in the previous section of this chapter and the outcome is exhibited in the pulsed current profile.

4.1.3 Biasing at high voltage

One important consideration for modeling the current voltage characteristics of AlGaIn/GaN HEMT devices is the high biasing voltages that can be applied on the device given the high breakdown voltage of GaN based material. Whether the simulation model used is a physical model representation of the device or an empirical model, it must be able to handle the high biasing voltages and give an accurate prediction for the device performance without resulting in any convergence issues or even erroneous results when running simulations such as harmonic balance simulations.

The second issue with existing modeling equations is the divergent of transconductance values with increasing applied drain to source voltage as a result of the product of $(1+\lambda V_{DS})$ channel length modulation term used in the empirical formulas. The general form for the transconductance equation for the Curtice, Chalmer, EEHEMT and most of the modified GaN based models are dependent on the product of the lambda (parameter KAPA for EEHEMT model) term and the applied V_{DS} .

The above mentioned issues will not be apparent when dealing with small biasing voltages for transistor devices fabricated on substrate such as GaAs. However, when dealing with devices like AlGaIn/GaN HEMTs where large biasing voltages could be applied, the effects will be more prominent and will result in an inaccurate prediction in the device performance. To illustrate the problem associated with applying large biasing voltages, Chalmer's model was used to

model a pulsed IV measurement measured up to a V_{DS} voltage of 30V. The model was used to simulate the current performance for V_{DS} up to 120V and the plots with the pulse measurement data alongside the simulated results of the applied Chalmer's model is shown in Figure 4.7. The effects of current divergence and over optimistic current prediction can be observed from the simulated data which can lead to inaccurate representation of the actual active device performance.

Figure 4.7 Comparison between measured data (blue trace with x markers) and simulated Chalmer's model (red trace) beyond modeled biasing data and up to 120V

In the proposed formulation, the issue with regards to the divergence of transconductance with large applied voltage biasing is managed by a separate output conductance term (eqn. 4.3) where the V_{DS} dependent output conductance is modulated by another V_{GS} function independent of the transfer function $f(V_{GS})$. This would reduce the effects of transconductance divergence as a result of the direct product between the transfer function and the V_{DS} applied on the device.

In addition, the $h(V_{DS})$ function (eqn. 4.4) embedded in the output conductance function limits the ever increasing transconductance with a hyperbolic tangent function reducing the output conductance when high V_{DS} biasing is applied. The function of the hyperbolic tangent curve is to provide a product of 1 at low V_{DS} and a product at 0 to the conductance function beyond the voltage shift parameter defined in the equation. The purpose of the imposed $h(V_{DS})$ function is to limit the output conductance by forcing the conductance to have a gradient of zero beyond certain defined V_{DS} which is a more physical representation of device performance instead of the ever rising transconductance with increasing V_{DS} biasing. At the same time, the high rate of decrease for the conductance is selected for the $h(V_{DS})$ function in order to not affect the extracted empirical current parameters which was performed at lower V_{DS} biasing. The rate and V_{DS} onset for the decrease in output conductance for the modeled device is controlled by the grad and shift term respectively.

To illustrate the effects of the overestimation for the drain conductance evaluation with increasing V_{DS} biasing, simulations of the modeled current were performed with and without conductance controlling function $h(V_{DS})$. The simulated plots are shown in Figure 4.8. The issue of divergence in transconductance is clearly illustrated if no control was enforced on the conductance of the extracted current model. With the conductance controlling function $h(V_{DS})$, a more physical current estimation and transconductance derived for small-signal simulations can be obtained with increasing applied V_{DS} biasing.

Figure 4.8 Comparison between two simulated plots up to a biasing drain voltage of 120V. Red trace (no markers) modulated with $h(V_{DS})$, blue trace (with x markers) without modulation function $h(V_{DS})$

4.2 Diode current modeling

The forward current model is used to model the diode currents that exist between the gate-source terminals and also the gate-drain terminals. As a symmetric device is modeled, the same current equation can be adopted to model the two diode current characteristics. The forward current model must be able to accurately model the forward current with respect to the applied voltage as shown in Figure 3.6 (b) from the previous section. With the possibility of applying large voltages to the AlGaIn/GaN HEMTs, there might be issues with simulations when applying conventional diode current formulations to represent the diode currents in AlGaIn/GaN HEMT models.

Typically, the Schottky junction diode equation would be used to model the diode currents with the metal-semiconductor junctions [84]. The conventional diode

equation which consists of the exponential term would not be appropriate to model the diode currents given rapidly increasing nature of the exponential function. Another forward current formulation that was experimented was a function of natural logarithm and hyperbolic cosine [75] which showed to have good differentiability. The function proved to provide a good match for the measured experimental data but showed to be not feasible as it would generate erroneous results from the circuit simulators when higher biasing voltage was applied to the AlGaIn/GaN HEMT model.

A simpler current model was adopted to model the forward current characteristics which eliminate the issue of erroneous outcomes from the simulators. The principle of the proposed current model is identical to the forward current equation used in [75] which emulates the absolute mathematical function with the use of the square-root function. Equation 4.17 is the final form adapted to model the forward current of the gate-to-source diode current equation with equation 4.18 having the similar form adapted to model the gate-to-drain diode current.

$$I_{gs} = \frac{cur_mag}{2} \cdot (\sqrt{(V_{Gsi} - shift)^2 + del_gs} + (V_{Gsi} - shift)) \quad (4.17)$$

$$I_{gd} = \frac{cur_mag}{2} \cdot (\sqrt{(V_{GDi} - shift)^2 + del_gd} + (V_{GDi} - shift)) \quad (4.18)$$

Empirical parameters in equations 4.17 and 4.18 can be extracted from the experimental plots where the *cur_mag* term was used to model the magnitude of the square root function to map to the experimental forward current value, a *shift* term which works like the turn on voltage for the diode current and the *del_gs/del_gd* term which is a generic term having a small value (typically 0.01) to prevent the square root function from running into a computational error and can be used to generate a smooth transition for the switching from turn on state of the diode to the off state.

4.3 Nonlinear charge modeling

Typically, large-signal parameters such as the charge element of the transistor can be obtained from the bias dependent small-signal linear circuit. Figure 4.9 (a) shows the general topology for the small-signal circuit typically used for charge modeling. Such an implementation is based on a total gate charge that is attributed between the gate-source and gate-drain branch where the terminal voltage V_{GD} must be evaluated. One issue with the conventional capacitance model used for large-signal HEMT modeling that can cause convergence issues with EM simulators is the failure to adhere to the charge conservation criteria [85], [86]. To ensure that the charges are conserved, the following criteria must be observed [87]:

$$\frac{\partial C_{gs}(V_{GS}, V_{GD})}{\partial V_{GD}} - \frac{\partial C_{gd}(V_{GS}, V_{GD})}{\partial V_{GS}} = 0 \quad (4.19)$$

In this work, a different approach to the conventional charge modeling will be adopted. The small-signal circuit implementation for the extraction of the large-signal charge model will be based on the works in [88]. The small-signal topology for the linear circuit modeling adopted in this work is shown in Figure 4.9 (b).

Figure 4.9 (a) Typical small-signal circuit used for charge modeling (b) small-signal circuit used in this work for charge modeling

From the schematic point of view, the differences between the small-signal circuit used in this work and the conventional small-signal circuit are the elimination of the C_{gd} capacitance and the inclusion of an additional transconductance element which has been given a label of dm in Figure 4.9 (b). From the circuit point of view, both of the small-signal circuit in Figure 4.9 can be used to describe the linear performance of a transistor adequately. The advantage of the topology used for this work is that only a single branch charge is considered for the small-signal circuit depending on whether a positive gate-source or positive gate-drain voltage is applied. Instead of considering two branch charges and the need to evaluate an internal V_{GD} terminal voltage which is not straightforward in extraction, the approach will eliminate the risk of charge convergence issues in the event where the charge conservation criteria is not satisfied or the simulator fails to converge at a defined capacitance value say for example when the applied drain to source voltage is at zero volts.

The first step to the empirical formulation of the charge source equation was to establish the relationship between the capacitance values of the small-signal performance and the applied biasing values. The capacitance values for each set of biasing voltages can then be extracted from the intrinsic Y-parameters of the

measured results from its imaginary part using the formulation listed in equations (4.20) to (4.23). The extracted intrinsic capacitance values in relation to the intrinsic biasing voltages are shown in Figure 4.10. The capacitance values were extracted from the data points with the frequency range from 100MHz to 5GHz.

$$\text{imag}(Y_{11}) = j\omega C_{11} = j2\pi f C_{11} \quad (4.20)$$

$$\text{imag}(Y_{12}) = j\omega C_{12} \quad (4.21)$$

$$\text{imag}(Y_{21}) = j\omega C_{21} \quad (4.22)$$

$$\text{imag}(Y_{22}) = j\omega C_{22} \quad (4.23)$$

(c)

(d)

Figure 4.10 (a) Extracted intrinsic C11 with respect to V_{GSi} (b) extracted C12 with respect to V_{DSi} (c) extracted C21 with respect to V_{GSi} (d) extracted C22 with respect to V_{DSi}

Having extracted the capacitance values and established the relationship between the various capacitance and biasing voltages, a more straightforward empirical equation for the charge source Q_{gs} and Q_{ds} can be derived based on the small-signal circuit in Figure 4.9 (b) with the following integrals:

$$Q_{gs} = \int C_{11} dV_{GS} + \int C_{12} dV_{DS} \quad (4.24)$$

$$Q_{ds} = \int C_{21} dV_{GS} + \int C_{22} dV_{DS} \quad (4.25)$$

To model the symmetrical nature of the device, the overall charge sources implementations for the AlGaIn/GaN HEMT model are shown in Figure 4.11. It consists of four charge sources Q_{gs} , Q_{gd} , Q_{ds} and Q_{sd} but not all the charge sources will be present during normal application of the transistor model. When a positive drain-source voltage is applied, only charge sources Q_{gs} and Q_{ds} will be present as shown in Figure 4.12 (a). Likewise, when the applied drain-source voltage is negative, only charge sources Q_{gd} and Q_{sd} will be present as shown in Figure 4.12 (b).

Figure 4.11 Charge sources implementation for the proposed AlGaIn/GaN HEMT

To implement the switching of the charge sources in the symbolic defined device (SDD) module, switching functions will be employed and the product of the switching functions with the charge sources will select the charge sources present in the SDD according to the V_{DS} applied. Besides the function of charge sources selection, the existence of the switching functions also ensure that the EM simulator does not run into any convergence issues when the polarity of the V_{DS} switches from positive to that of a negative value, especially when the value of V_{DS} equals zero.

Equations described in 4.26 to 4.29 are the four switching functions used in the SDD module to execute the switching behavior. The main form of the switching functions is a hyperbolic tangent formulation which is a function of the applied V_{DS} . The selection of the charge sources is accomplished as the hyperbolic tangent function is formulated to range from null to unity thus dictating which charge sources should be present from the applied V_{DS} . Equations 4.26 and 4.27 are used to control the transition of charge sources from Q_{gs} to Q_{gd} and equations 4.28 and 4.29 are used to control the switching of charge sources from Q_{ds} to Q_{sd} .

When $V_{DS} > 0$

When $V_{DS} < 0$

Figure 4.12 (a) Charge sources of the transistor model when positive V_{DS} is applied (b) Charge sources of the transistor when negative V_{DS} is applied

$$\text{Switching function 1} = \frac{1}{2} \cdot [1 + \tanh(m \cdot V_{DS})] \quad (4.26)$$

$$\text{Switching function 2} = \frac{1}{2} \cdot [1 + \tanh(m \cdot -V_{DS})] \quad (4.27)$$

$$\text{Switching function 3} = \frac{1}{2} \cdot [1 + \tanh(n \cdot V_{DS})] \quad (4.28)$$

$$\text{Switching function 4} = \frac{1}{2} \cdot [-1 + \tanh(n \cdot V_{DS})] \quad (4.29)$$

The use of the variables m and n in the switching functions serves to control the gradient of the hyperbolic tangent function which gives the flexibility to control the rate of which the charge values changes when the polarity of the applied V_{DS} switches. To illustrate the effects of the switching functions, the plots for equations 4.26 to 4.29 are shown in Figure 4.13 where the values of variable m and n are kept at one. The effect of polarity switching when the charge source Q_{ds} is switched to Q_{sd} is achieved with equation 4.29 as shown in Figure 4.13. The switching functions will also be able to model the uncharacteristic capacitance values when V_{DS} equals to 0V shown in Figure 4.10.

Figure 4.13 Plots for equations (4.26) to (4.29) illustrating the effects of the switching functions

From the capacitance plots in Figure 4.10, the empirical Qgs formula when positive drain-source voltage is applied can be evaluated using equation 4.24. A hyperbolic tangent function was selected to model the capacitance C11 with respect to the applied V_{GSi} and a linear function was selected to model capacitance C12 with respect to V_{DSi} . The hyperbolic tangent function used to model the capacitance C11 with respect to the applied V_{GSi} is shown in equation 4.30 and the linear equation used to model the capacitance C12 with respect to V_{DSi} is shown in equation 4.31. Based on the formulation Qgs formulation in equation 4.24, the derived empirical Qgs formulation is shown in equation 4.32.

$$C11 = \frac{mag_C11}{2} \cdot [1 + \tanh(grad \cdot (V_{GSi} - mid_point))] + (rate_of_change_pinchoff_C11 \cdot V_{DSi} + C11_0) \quad (4.30)$$

$$C12 = 2 \cdot grad_C12 \cdot V_{DSi} + C12_intercept \quad (4.31)$$

$$Qgs = \frac{mag_C11}{2} \cdot \left[V_{GSi} + \frac{1}{grad} \cdot \ln(\cosh(grad \cdot (V_{GSi} - mid_point))) \right] + pinchoff_C11 + grad_C12 \cdot V_{DSi}^2 + C12_intercept \cdot V_{DSi} \quad (4.32)$$

where

$$pinchoff_C11 = (rate_of_change_pinchoff_C11 \cdot V_{DSi} + C11_0) \cdot V_{GSi} \quad (4.33)$$

Modeling across a range of applied biasing, constant values such as mag_C11, grad and mid_point can be empirically extracted from the C11 capacitance plots where parameter mag_C11 controls the magnitude of the hyperbolic tangent

function, *grad* parameter controls the gradient of the hyperbolic tangent function and the *mid_point* parameter controls the shift of the hyperbolic tangent function from its zero origin respectively. A linear relationship was used to describe the change in *C11* capacitance with respect to changing V_{DSi} by the means of modeling the pinched off capacitance values. Parameter $C11_0$ denotes the *C11* capacitance values when V_{DSi} is at 0V and gradient term of the linear relationship can be obtained from the rate of change of pinched off *C11* capacitance values.

The same formulation method for the empirical equation of *Qgs* can be applied to the derivation of charge equation for *Qds*. An identical hyperbolic tangent function form was adopted to model the capacitance *C21* with respect to the applied V_{GSi} is shown in equation 4.34 and the linear function used to describe the capacitance *C22* with the applied V_{DSi} is shown in equation 4.35. The derived *Qds* equation based on equation 4.25 can be derived to be the equation form of equation 4.36. Similar to the empirical parameters extraction for the *Qgs* charge sources, empirical parameters such as *mag_C21*, *grad_2*, *mid_point_2*, *rate_of_change_pinchoff_C21* and $C21_0$ are now extracted from the capacitance plots of *C21* with respect to V_{GSi} . The parameters of the quadratic equation to model the linear relationship of capacitance for *C22* can be extracted from the plots of *C22* with respect to V_{DSi} .

$$C21 = \frac{mag_C21}{2} \cdot [1 + \tanh(grad_2 \cdot (V_{GSi} - mid_point_2))] + (rate_of_change_pinchoff_C21 \cdot V_{DSi} + C21_0) \quad (4.34)$$

$$C22 = 2 \cdot grad_C22 \cdot V_{DSi} + C22_intercept \quad (4.35)$$

$$Q_{ds} = \frac{mag_C21}{2} \cdot \left[V_{Gsi} + \frac{1}{grad_2} \cdot \ln \left(\cosh(grad_2 \cdot (V_{Gsi} - mid_point_2)) \right) \right] + pinchoff_C21 + grad_C22 \cdot V_{Dsi}^2 + C22_intercept \cdot V_{Dsi} \quad (4.36)$$

where

$$pinchoff_C21 = (rate_of_change_pinchoff_C21 \cdot V_{Dsi} + C21_0) \cdot V_{Gsi} \quad (4.37)$$

To model the symmetrical properties of the device, the same form for the empirical formulas are adopted for Qgd and Qsd. The same charge equation together with the extracted parameter values will be used for the empirical formulation of Qgd charge source and likewise the same charge equation together with the extracted parameter values for Qds will be used for the formulation of charge source Qsd. Having the same form and same extracted parameter values, the charge source Qgd is made a function of V_{GD_i} instead of V_{GS_i} in Qgs and Qsd is made a function of V_{SD_i} instead of V_{DS_i} in Qds.

4.4 Gate-drain and gate-source current breakdown model

For a more complete device model, the current breakdown model needs to be included in the large-signal model to emulate the situation when the device experience failure due to excessive biasing voltage applied to the GaN based HEMT device. However, the breakdown voltages of AlGaIn/GaN HEMTs are typically over hundredth of volts and the exact breakdown voltage and the characteristics for the HEMT device is not easily measurable given equipment

limitations in most of the laboratories. Therefore, an analytical approach has been implemented to the modeling of the breakdown current instead of the empirical modeling approach used for other elements of the large-signal model.

The same modeling principles applied for other large-signal elements was observed for the modeling of the breakdown current where the application of large voltage biasing values will not result in erroneous simulations outcome. Therefore, the same equation used to model the diode current was utilized to model the breakdown current characteristics. The modeling parameters were amended accordingly to represent the modeling of the breakdown current. The current breakdown formulation for the gate-to-source junction breakdown and the gate-to-drain junction breakdown are of the same form and is listed in equation 4.38 and 4.39.

$$g_{S_{breakdown}} = \frac{cur_mag_bd}{2} \cdot (\sqrt{(V_{GSi} - shift_bd)^2 + del_gs_bd} + (V_{GSi} - shift_bd)) \quad (4.38)$$

$$g_{D_{breakdown}} = \frac{cur_mag_bd}{2} \cdot (\sqrt{(V_{GDi} - shift_bd)^2 + del_ds_bd} + (V_{GDi} - shift_bd)) \quad (4.39)$$

The parameters used to model the breakdown current includes *cur_mag_bd* which models the rate of increase for the breakdown current, *shift_bd* term which is used to denote the breakdown voltage of the HEMT transistor and the *del_gs_bd* and *del_ds_bd* terms to prevent any mathematical computation error and controls the transition before and beyond the breakdown voltage similar to the workings in the forward current diode equations. The equations model the breakdown current with the use of the squareroot function which separates the current model before the breakdown voltage and beyond the breakdown voltage. Before the breakdown

voltage, the evaluated current from the breakdown current source is zero, beyond the breakdown voltage; the current can be modeled to rise rapidly with the magnitude controlling term.

As mentioned previously, the breakdown characteristics might not be experimentally obtainable but breakdown voltage information for the transistor device is usually provided by the fabrication foundries as the figure of merit under the specifications. Alternatively, references of the approximated breakdown voltage can be drawn from published literature with similar epitaxial and HEMT configuration [89]-[94].

Chapter 5 Large-signal equivalent circuit model

The notion of active device modeling is to have better knowledge of the various device characteristics and at the same time possess the ability to use circuit simulators to design circuits with the modeled device. The large-signal model of the active device is particularly important in the design and simulation of high power amplifier circuits to predict the performance of the active device under large-signal excitation at the input port. The proposed large-signal model was developed with the objectives of being able to model a symmetrical active device across a range of applied biasing voltage and be able to predict the performance of the modeled device when high biasing voltage is applied without the generating an error response from the simulator.

In the first part of the chapter, the large-signal equivalent circuit model will be described. The various components of the active device model discussed in the previous chapters will be used to construct the large-signal equivalent model. The implementation of the large-signal equivalent circuit for circuit simulators will also be discussed in the chapter. For a more accurate model, an additional rf dispersion element should also be included to bridge the discrepancies between the small-signal characteristics and the derived characteristics from the nonlinear elements in the large-signal model.

In the second part of the chapter, the different elements of the modeled device will be compared to the measured data to illustrate the effectiveness of the proposed empirical large-signal model. The modeled drain to source current which is the major source of non-linearity will be compared to the measured data. The modeled pulsed current with selected quiescent biasing will also be presented. Following is the comparison for another current source which is the diode current model before the comparison between the modeled and measured small-signal performances.

The comparison between the modeled and measured small-signal performances will be made across a selected range of biasing voltages to illustrate the competency of the empirical formulation used to model the small-signal performances. The chapter will conclude with the comparison between the modeled and measured single tone power sweep measurement and the corresponding evaluated power added efficiency values to illustrate the large-signal power prediction capability of the proposed large-signal model.

5.1 Model implementation

The proposed AlGaIn/GaN HEMT device model schematic is shown in Figure 5.1. A transistor device can be said to be a symmetrical device if the gate-to-source finger distance is the same as the gate-to-drain finger distance which means the drain and source terminals can be used interchangeably. To model the symmetrical nature of such a device, additional elements must be considered should the biasing terminals be switched. The model described in this thesis work will be based on symmetrical AlGaIn/GaN HEMT devices and in some cases, where a reduced gate-to-source finger distance is used to increase the channel current [95], additional characterization step in the reverse configuration is required.

Figure 5.1 Schematic of the proposed AlGaIn/GaN HEMT device model

Apart from the extrinsic parasitic components, nine elements will be used to describe the intrinsic performance of the AlGaIn/GaN HEMT for the proposed model. Three of the elements are charge elements which represent Q_{gs} , Q_{ds} and the third charge element which is a combination of Q_{sd} and Q_{gd} . Five of the elements are DC current elements which represent two diode current elements to model the forward current characteristics, two current elements to model the gate-to-source and gate-to-drain channel breakdown and one element to model the DC IV characteristics. The last current element will be used to model the rf current element which only would be present during rf operation of the device.

To enable simulations to be performed with the empirical AlGaIn/GaN HEMT model, the SDD module from Agilent's ADS can be employed to represent the various characteristics of the HEMT device. The SDD allows users to model a particular current or the charge value by using explicitly defined mathematical equations describing the port currents of the SDD. Potential difference across a

SDD port can also be tapped to be used in the formulation of the equation and is particularly useful when modeling is performed with the intrinsic voltages of the HEMT device. The screenshot of the implemented SDD model using Agilent's ADS is shown in Figure 5.2.

Figure 5.2 ADS schematic of the SDD for the proposed AlGaIn/GaN HEMT device model

Port 1 of the SDD will be used to model the Q_{gs} charge source of the proposed transistor model and the port voltage denotes the intrinsic gate-to-source voltage. Likewise, Port 2 of the SDD will be used to model the Q_{ds} and Q_{sd} charge sources and the port voltage denotes the intrinsic drain-to-source voltage. Port 3 of the SDD is used to model the Q_{gd} charge sources where the port voltage denotes the intrinsic gate-to-drain voltages. The toggling of the appropriate charge sources will be accomplished with switching functions and will be implemented as a product to the charge sources accordingly. Port 4 of the SDD models the active current and port 6 of the SDD models the rf component for the measured device. Port 5 and 7 of the SDD will be used to model the breakdown current for the gate-drain terminals and the gate-source terminals respectively should device failure

occurs. Port 8 and 9 will be used to model gate-drain and gate-source forward diode current respectively.

The connection between the different intrinsic elements together with the extrinsic parasitic elements is shown in Figure 5.2 and a DC blocking component is employed to isolate the rf current element which will only be reflected when rf simulation is performed on the device model. In addition to the device related elements, parasitic such as the DC resistance of the measurement setup were also added such that accurate device performance prediction can be obtained.

5.1.1 Rf dispersion

A rf current model is used to describe the rf dispersion characteristics of the modeled HEMT device at various DC biasing conditions. This method of dispersion characterization has been used to great effect with the EEHEMT model and also demonstrated in other literatures [40],[96],[97]. As shown in the transistor model in Figure 5.1, the rf current element is preceded by a DC blocking lumped component which ensures that the correct DC value is simulated when performing DC simulations with the HEMT model and the rf dispersion effects will only exist when performing rf simulations.

Empirical formulation for the rf current model used in this work can be derived using the low frequency intrinsic small-signal characteristics from the measured device and it can be used to describe the S-parameters dispersion effects such as the discrepancies of the forward gain for the measured AlGaIn/GaN HEMT device and the impedance values associated with the applied biasing voltages. With the intrinsic Y-parameters, the rf current can be extracted using equation 5.1 and the extracted intrinsic rf current plot is shown in Figure 5.3. The rf current plots are

extracted for the same biasing voltages with V_{GSi} of -5V to 0V in steps of 1V and corresponding V_{DSi} from V_{DSi} equals to 0V to 20V in steps of 1V.

$$intrinsic_rf_current = \int mean(low_freq_Y22) dV_{DSi} \quad (5.1)$$

The extracted plot of the rf current take on the same profile as the active current plots and the same modeling equation in 4.1 will be used for the modeling of the rf current. Having the same form current modeling form, the parameters extraction process is identical and will not be repeated in this section of the thesis report.

Figure 5.3 Extracted intrinsic rf current obtained from the intrinsic Y-parameters

5.2 Model verification

As mentioned in chapter 3, the verification of simulated data of the modeled device with actual measured data is the final modeling process before the simulation

model is accepted. Besides comparing with the data used for empirical modeling, the large-signal performance of the modeled device in the form of power sweep measurements and the corresponding evaluated power added efficiency values will also be tested. Power added efficiency provides us with the associated current values comparison between the simulated and measured device illustrating the fidelity of the implemented device model. This is critical for the design of power amplifiers especially in the case of high efficiency power amplifier where the current prediction under large-signal excitation can affect the efficiency calculation significantly.

The comparison with the data used for empirical modeling will begin with the static and pulsed IV data modeling where the effectiveness of the modeling for the current source under static and pulsed conditions is illustrated. The multi bias s-parameters will verify the effectiveness of the proposed charge source modeling technique with varying bias points across the measured frequency range. The chapter will conclude with the abovementioned power measurement comparison.

5.2.1 Static and pulsed IV

The simulated and measured active current plots with respect to the applied V_{DS} are shown in Figure 5.4. With the proposed current model with equation 4.1, the static DC characteristics of the AlGaIn/GaN HEMT device has been well modeled. The current characteristics in the saturation region of the transistor device has been well modeled with the proposed gradient control term capturing the characteristics of the turn off region and when large V_{GS} is applied on the device. The knee current characteristics at low V_{DS} were accurately captured with the equation which is critical for analyzing load line of the active devices operating in switched mode.

Figure 5.4 Comparison between modeled and measured data for the active current (I_{DS}) characteristics of the AlGaIn/GaN HEMT device. Modeled data are represented by the red traces (no markers) and measured data are represented by the blue traces with x markers

(a)

Figure 5.5 Comparison between modeled and measured data for the pulsed active current (I_{DS}) characteristics of the AlGaIn/GaN HEMT device for different quiescent gate biasing (a) $V_{GS0} = -5V$, $V_{DS0}=20V$ (b) $V_{GS0} = -3V$, $V_{DS0}=20V$ (c) $V_{GS0} = -1V$, $V_{DS0}=20V$. Modeled data are represented by the red traces (no markers) and measured data are represented by the blue traces with x markers

With the extracted pulsed parameter values discussed in chapter 4 of the report, the comparison between the measured and modeled pulsed parameters for the selected biasing is shown in Figure 5.5. The current formulation proposed has shown to be capable of modeling both the static and pulsed current profile proficiently at all regions of the current profile including the linear and saturation region.

5.2.2 Diode current

The simulated and measured forward current plots with respect to the applied V_{GS} are shown in Figure 5.6. The turn on characteristics of the diode has been well captured using the square root function with the del_gs empirical parameter in equation 4.17 and the subsequent on characteristics of the diode current are also well modeled.

Figure 5.6 Comparison between modeled and measured data for the forward current (I_{GS}) characteristics of the AlGaIn/GaN HEMT device. Modeled data are represented by the red trace (no markers) and the measured data are represented by the blue trace with x markers

5.2.3 Multi-bias s-parameters

Besides the modeling of the static DC current, the rf modeling capability of the proposed model will be evaluated. The comparison between the measured s-parameters and the simulated s-parameters characteristics from the model is shown in Figure 5.7. The s-parameters across different voltage biasing were well modeled with the S_{21} variation from pinch off to peak transconductance and the transconductance compression was quite adeptly represented. Characteristics such as the S_{11} parameters were also well captured by the model including the low impedance characteristics when the gate source diode is in forward biased with V_{GS} equals to 1V and V_{DS} at 0V. Likewise for the characterization of S_{22} , the characteristics of the s-parameters at V_{DS} equals to 0V and operating above the pinch off voltage is accurately modeled. The S_{12} performance of the measured transistor device was also well modeled by the proposed model.

Figure 5.7 Comparison between measured and modeled S-parameters (a) comparison of S11 characteristics (b) comparison of S12 characteristics (c) comparison of S21 characteristics (d) comparison of S22 characteristics. The measured traces are represented by blue traces and the modeled traces are represented by red traces

5.2.4 Power measurements

To verify the power performance characteristics of the modeled active device, a single tone power sweep was performed with a 50Ω power measurement system where the input and output of the measurement setup was kept at 50Ω throughout the power sweep. The active device was measured with no input and output matching network and the results to be presented from Figure 5.8 to Figure 5.10 will be based on a device biased at a gate to source voltage of -2V and the applied drain to source voltage of 28V. The frequency for the power sweep measurement was 10GHz.

The comparison between the measured and modeled output power plots is shown in Figure 5.8. The comparison between the calculated power added efficiency values for the measured and simulated data is shown in Figure 5.9. The power added efficiency was evaluated with the formulation: power added efficiency (PAE) % = $(P_{out} - P_{in})/P_{DC} \times 100\%$. The model was able to give a good prediction of the output power and the power added efficiency which is a good measure of the current value prediction of the modeled device. The comparison between the measured and modeled current values with different input power is shown in Figure 5.10. This is especially crucial when it comes to the design of high efficiency power amplifiers where the current prediction is a sensitive parameter to the PAE evaluation given that most of the time a large drain voltage is applied to the amplifier which will influence the P_{DC} calculation.

Figure 5.8 Comparison between the measured output power (blue trace with x markers) and the modeled output power (red trace with no markers)

Figure 5.9 Comparison between the measured power added efficiency (blue trace with x markers) and the modeled power added efficiency (red trace with no markers)

Figure 5.10 Comparison between the measured drain current (blue trace with x markers) and the modeled drain current (red trace with no markers)

As mentioned in chapter 3, the validity of the proposed model must be tested against the measured data to verify the fidelity of the proposed model and the extracted parameters used to describe the active device. From the various verification tests performed and presented, the proposed large-signal model in Figure 5.1 has successfully reproduced the performance of the measured AlGaIn/GaN HEMT device for the various current sources and including the small-signal performance simulated from the proposed model across a selected range of applied biasing.

The model was also able to give a good power prediction for the single tone power sweep measurement and the accuracy in the current prediction was illustrated with the good match obtained for the corresponding evaluation of the power added efficiency term.

Chapter 6 Innovative active circuit design methods

In chapter 1 to 5, the need for an accurate device model and the derivation of the large-signal model was presented, highlighting various important aspects of device characterization, from data acquisition to the device empirical modeling. The large-signal model proposed was validated with an AlGaIn/GaN HEMT device to illustrate the improved modeling capability of the model, the ability to handle large biasing voltages and the ability to characterize atypical behaviour of the GaN based device. However, the proposed modeling processes together with the empirical formulation are not technology limited and can be extended to other technology and material systems.

Due to the lack in opportunities for fabrication using the GaN on SiC material system, the active circuits to be discussed in chapter 6 will not be demonstrated using GaN on SiC system. Instead, the active circuit designs will be demonstrated using GaAs based system and hybrid circuitry with the use of LDMOS. The focus in this chapter will therefore be on the active circuit design methods with design equations to aid in reducing the complexity of a MMIC design procedures previously practiced, saving on time and design efforts. The significance of the modeling work presented in chapter 2 to 5 on the active circuits will be further elaborated in the respective subsections.

The first subsection of the chapter will discuss on an alternate design methodology for an active circulator circuit. The proposed design methodology serves to breakdown the design of a monolithic microwave integrated circuit (MMIC) to a modular form where the overall circuit can be constructed with identical modules. The method serves to reduce the complexity of the conventional MMIC design process and simplifies the design considerations of achieving broadband frequency operation for an active circulator. The modular approach to design an active

circulator will first be discussed with the derivation of the design equations followed by the circuit construction with the various modules. It would be shown that with the proposed method, the broadband performance of the overall active circulator circuit can be achieved with the use of broadband modules and the method is technology independent. The fabricated MMIC active circulator circuit on GaAs together with the measurement results will also be presented.

The second subsection of the chapter will discuss on a novel loading circuit for a class E power amplifier circuit. The novel class E load consists of a coupled line load which would provide the required loading conditions for a class E power amplifier circuit design. Conditions for class E power amplification are easily satisfied with the coupled line load and have added advantages such as the ability to achieve large impedance transformation ratio matching and inherent DC blocking capability. The design equations for the load equations of the class E power amplifier with the coupled line load will be derived and the circuit will be designed and fabricated with a commercially available LDMOS device. The accuracy of the large-signal device model is highlighted when performing harmonic balance simulations to study the current and voltage waveform when designing the high efficiency power amplifier. The fabricated high efficiency power amplifier together with the measured results will be presented in this chapter.

6.1 Active Circulator

In this subsection, a modular approach to design an active circulator is presented. The novel design methodology simplifies complicated circuit design steps by considering the cascading of modular components used in the active circulator circuitry. Using the above approach, it will be shown from the derived S-parameters that the frequency performance of the designed active circulator is dependent on the frequency performance of the modules used to construct the

active circulator. An advantage to the proposed methodology is when designing a broadband active circulator, the broadband performance of the overall active circulator circuit can be achieved by selecting modules with broadband performances.

A microwave circulator is a three port microwave device that only permits microwave signals to propagate in a specific direction e.g. clockwise direction, from one of the ports to the adjacent port and forbids the transmission of microwave signals in the opposite direction e.g. anti-clockwise direction. This directivity property of a circulator is represented in the s-parameters for an ideal circulator shown in Figure 6.1. Inferring from the s-parameters, an ideal circulator exhibits full transmission in a particular direction and complete isolation in the opposing direction [98].

$$[S] \text{ (ideal circulator)} = \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}$$

Figure 6.1 S-parameters for a matched ideal circulator

With its directivity property, a circulator is a critical microwave component and can be found in many microwave systems. A circulator can be found in reflection phase shifters and also in transmitting and receiving (T/R) modules to isolate the path between the transmitted and received signals. Before the conception of constructing a circulator using active components was proposed, circulators were constructed from magnetic ferrite materials. The magnetic properties of the ferrite materials provides for the properties of the circulators as a result of the interaction between the transmitting EM signals and the magnetic field.

An active circulator circuitry constructed based on the unilateral property of a transistor was proposed in 1965 [99]. The unilateral property of the transistor ensured that the microwave signals get amplified in the forward transmission path and the signals get highly attenuated in the reverse transmission path. The proposed active circulator meant that the bulky ferrite circulators could be replaced with the active circulator where integration with other MMIC circuitry was possible. The extension to the active circulator work also saw the development of other active circulator circuitries using CMOS, MESFET and GaAs FET[100]-[103] leading to more compact circuits.

Apart from full three way active circulators, quasi-circulators were also the subject of interest for many due to its practical use in phase shifters and T/R modules [104]-[112]. Different from the full three way circulators, quasi-circulators do not support the unidirectional microwave signal propagation for all the microwave ports. Two out of the three microwave ports will be completely isolated with no microwave signal propagation between them permitted.

Active circulator with broadband frequency performance was discussed in [111]. The active quasi-circulator circuit was designed to operate in the frequency range from 6 GHz to 18 GHz. The methodology to attain the broadband performance is the use a distributed topology of the narrowband active quasi-circulator design having multiple transconductance amplifier stage. Such a design process for the abovementioned active circulator is complex and the active circulator design could not be easily scaled to other frequencies.

6.1.1 Modular approach to design a three-way active circulator

The modular approach on the other hand reduces the complexity of the active circulator circuit designs by considering only properties of modular components

essential for the construction of the circuit. The modular blocks could then be cascaded in series to obtain the desired active circulator performance. To design a full three way active circulator circuit, three sets of identical modules would suffice. Each of such modules would contain two sub-modules consisting of a three port network having one of the ports functioning as one of the ports for the resultant active circulator circuit and a two port network which would contain the active circuitry. The schematic of the modular active circulator design approach is shown in Figure 6.2.

Figure 6.2 Schematic of the modular active circulator design approach

As shown in Figure 6.2, an active circulator circuit can be constructed from just two microwave modules. The three port network module used in the active circulator design not only functions to couple the microwave signals into and out of the circular topology of the active circulator device, it also must have good isolation to prevent the microwave signals from leaking to the adjacent active circulator port.

As for the two port networks in the modular active circulator design, it functions as the amplification circuitry components which not only provides the required gain

in the forward transmission path and also cater to the directivity of the active circuitry with the poor reverse transmission property.

The S-parameters of the active circulator design can be obtained by considering the S-parameters for the individual modules. The S-parameters for a matched three port network is shown in Figure 6.3 (a) where S₂₃ and S₃₂ represents the isolation and S₂₁ and S₃₁ represents the coupling of the three port networks. The S-parameters for a matched two port network is shown in Figure 6.3 (b) where S₄₅ represents the gain and S₅₄ represents the gain in the reverse transmission direction.

Figure 6.3 (a) S-parameters for a matched three port network (b) S-parameters for a matched two port network

The overall s-parameters of the full three-way circulator design can be obtained by cascading the s-parameters in the order of the schematic shown in Figure 6.2. Unique to the properties of the modules used, higher order S-parameter expression involving terms S₂₃, S₃₂ and S₄₅ were omitted as they are negligibly small. This

means that the overall full three-way active circulator s-parameters can be derived to be as follows:

Derived [S] (active circulator)

$$\begin{aligned}
 &= \begin{pmatrix} 0 & S^* & S_{13} \cdot S_{54} \cdot S_{21} \\ S_{13} \cdot S_{21} \cdot S_{54} & 0 & S^* \\ S^* & S_{13} \cdot S_{21} \cdot S_{54} & 0 \end{pmatrix} \\
 &= S^+ \cdot \begin{pmatrix} 0 & S^*/S^+ & 1 \\ 1 & 0 & S^*/S^+ \\ S^*/S^+ & 1 & 0 \end{pmatrix} \quad (6.1)
 \end{aligned}$$

where

$$S^+ = S_{13} \cdot S_{54} \cdot S_{21} \quad (6.2)$$

$$S^* = S_{12} \cdot S_{31} \cdot S_{45} + S_{13} \cdot S_{54}^2 \cdot S_{23} \cdot S_{21} \quad (6.3)$$

The expression has been simplified to the form which is similar to that of an ideal circulator for the illustration on how a modular approach can help in the design of an active circulator design. The evaluated s-parameters for the full three-way active circulator shows that all the transmission directional terms are identical, likewise for the terms evaluated for the isolation direction. The terms evaluated for the isolation direction S^*/S^+ comprises of two major components with one term due to the reverse transmission of the amplification circuitry and another component due to the forward transmission.

By comparing the evaluated s-parameters to the ideal s-parameters for a circulator, the modular active circulator design can be worked out to be the form of the ideal circulator if $|S^*/S^+| \approx 0$, i.e. $S_{45} \approx 0$ and $S_{23}, S_{32} \approx 0$. The above analysis can be

used to design existing active circulator circuits [103] and can be used to devise new active circulator circuits.

The advantage of such a modular active circulator design is the possibility of designing an active circulator with broadband performance by using modules with broadband performances. This simplifies the design procedures of having to design a broadband active circulator at an overall circuit level. The advantages of such a modular design must be complemented with accurate module components where the accuracy of the device model would play an important role.

6.1.2 Three-way MMIC active circulator design

A MMIC active circulator based on the proposed modular method was designed and fabricated. Two basic modules will be used for the MMIC circulator design comprising of a broadband feedback amplifier and broadband 180° hybrid stage. For the three-way circulator design, the 180° hybrid circuit is placed between the amplification stages and the schematic for the modular active circulator design is shown in Figure 6.4.

The 180° hybrid circuit stage was used and position between the active component stage due to the good isolation between the sum and delta port of the 180° hybrid circuit. The 180° hybrid circuit stage consists of an in phase power divider and a 180° balun circuitry [113]. Based on the work done in [113], it can be worked out that the input of the in phase power divider (sum port of the 180° hybrid circuit) is isolated from the input of the balun (delta port of the 180° hybrid circuit).

Figure 6.4 Schematic for the modular active circulator design with amplifier and 180° hybrid circuit modules

In addition, broadband performance for the 180° hybrid circuit can be simply obtained by selecting a broadband balun and in the case of this circuit design, a Marchand balun has been used for the design of the 180° hybrid circuit. With only three of the ports required, the fourth port of the 180° hybrid circuit was terminated with a 50 ohms termination. The schematic and the picture of the fabricated 180° hybrid test circuit is shown in Figure 6.5.

Figure 6.5 Schematic and picture of the fabricated 180° hybrid test circuit

As for the active device module, an amplification module of a conventional feedback amplifier circuit was selected. The feedback amplifier circuit was designed based on a $4 \times 100 \mu\text{m}$ device fabricated using $0.15 \mu\text{m}$ power pHEMT technology with 250Ω parallel feedback resistor to realize a flat gain profile in the frequency of interest. A picture of the fabricated feedback amplifier test circuit is shown in Figure 6.6.

Figure 6.6 Picture of the fabricated broadband feedback amplifier

Individual modules for the 180° hybrid circuit stage and the feedback amplifier circuit were fabricated and tested for its performance to verify the workings of the proposed circuit design methodology. With the established designs for the individual modules, a compact three way active circulator design can be obtained by cascading the two unique modules in alternating sequence. A picture of the fabricated three-way active circulator with the composite modules is shown in Figure 6.7. The size of the fabricated active circulator circuitry is $4.2\text{mm} \times 2\text{mm}$.

Figure 6.7 Picture of the fabricated three-way active circulator with the composite modules

The isolation of the 180° hybrid circuit is critical to the performance of the modular active circulator design. Placed between active devices, good isolation is required to prevent RF power leakage to the adjacent microwave port. It is also the basis of the assumption where the transmission coefficients between the sum and delta port of the 180° hybrid circuit can be approximated to a negligible value when evaluating the overall S-parameters for the modular three-way active circulator circuit.

6.1.3 Measurement results

The fabricated four-port 180° hybrid breakout circuit was measured for its performance. All the s-parameters measurements were performed with an input power of -10 dBm. Identical to the workings of the 180° hybrid circuit, the fourth port of the 180° hybrid circuit was terminated with 50 ohms termination and the resultant three-port network was measured. The measured results for the three-port

network are shown in Figure 6.8. The measured results show that the isolation of the 180° hybrid circuit between the sum and delta input ports to be better than 22 dB across the frequency range of 8 to 18 GHz. At the same time the coupling coefficients $|S_{12}|$, $|S_{21}|$ and $|S_{13}|$, $|S_{31}|$ for the hybrid circuit measured to be better than 5 dB and 4 dB, respectively.

Figure 6.8 Isolation and insertion loss of the measured 180° hybrid test circuit

Another important component which is the feedback amplifier which provides the amplification required and simultaneously provides the reverse transmission isolation which aids in the directivity property of the active circulator design. A single gate biasing voltage of -5V and drain biasing voltage of 5V was applied to the feedback amplifier test circuit. The measured gate and drain current was 10.1 mA and 119.5mA, respectively. At the applied biasing conditions, the measured result for the forward and reverse transmission performance is shown in Figure 6.9. The gain for the feedback amplifier across the measured frequency of 8 to 18 GHz is approximately 5 dB.

Figure 6.9 Isolation and insertion loss of the measured broadband feedback amplifier test circuit

After understanding the performances of the individual modules that constitute the modular active circulator design, the fabricated modular active circulator circuit was measured. The same biasing conditions for the feedback amplifier module were applied to the three feedback amplifier circuits in the active circulator circuit. The active circulator circuit was measured with a small signal power of -10dBm. With the applied gate voltage of -5V and drain voltage of 5V, the total gate current measured to be 28.6mA and the total drain current measured to be 342.2mA. The return loss measurements for the three input ports are shown in Figure 6.10. The three insertion loss together with the isolation measurements for the reverse transmission is shown in Figure 6.11.

Figure 6.10 Measured return loss for the fabricated three-way active circulator MMIC

Figure 6.11 Measured isolation and insertion loss for the fabricated three-way active circulator MMIC

The return losses for all the three input ports for the modular active circulator circuit measured to be better than 11.6dB across 8 to 18 GHz. The insertion loss for all the transmission path are measured to be better than 4 dB and the isolation

for all the reverse transmission paths measured to be better than 14.5 dB across the same frequency range.

The isolation between the sum and delta ports of the 180° hybrid circuit together with the poor reverse transmission coefficients for the feedback amplifier proved to be effective in the active circulator design. It provides the critical property of good isolation of a circulator circuitry by ensuring an isolation of 14.5dB for all the three isolation measurements. A benchmark between commercially available passive circulators operating in the same frequency range and the active circulator presented in this work is shown in Table 6.1.

	Passive Circulator			Active circulator
Source	Rf sky microwave	Fairview microwave	Pasternack	this work
Frequency (GHz)	8 to 18	8 to 18	8 to 18	8 to 18
Max insertion loss (dB)	0.8	1	0.8	4
Min isolation (dB)	16	14	16	14.5
Size	21mm x 15mm (packaged)	16mm x 12.7mm (packaged)	31.75mm x 9.91mm (packaged)	4.2mm x 2mm (without package)

Table 6.1 Comparison between commercial passive circulators and the active circulator design in this work

As shown in Table 6.1, it can be shown that the isolation of the presented active circulator is comparable to passive circulators operating in the same frequency band. Although the insertion loss for the active circulator circuit presented is on the high side as compared to the passive circulators, the issue can be overcome by having an amplifier circuit design with a higher gain. An advantage for the active circulator design is the small circuit size as compared to the passive circulators as

can be seen in Table 6.1. Another advantage is the capability of the active circuit to be integrated directly to other MMIC elements without the need for other forms of connecting interface as the SMA connector interface.

6.1.4 Discussion

The power handling capability aspect is one of the critical criteria for modern active circulator circuitry. The proposed modular design approach is technology independent and would allow many different types of active circulator to be designed quickly and easily. The methods shown to derive the final S-parameters form for the active circulator also meant that the design methodology can be scaled in frequencies (in terms of operating frequency and the bandwidth of operation) to design broadband active circulator circuits at the frequencies of interest to the circuit designers.

Tapping on the advantages of GaN on SiC material system, an active circulator capable of handling high rf power can be achieved. The method of active circuit design presented was accomplished with the analysis of the s-parameters of the associated components. Having a good device model would greatly aid in the performance prediction of the overall active circuit during the design phase and reduces the risk of having multiple fabrication runs to acquire the desired outcome from the fabricated device.

6.2 Class E amplifier with coupled line load

In this subsection, a novel class E amplifier circuit topology capable of achieving high power added efficiency which exploits the series-open property of the coupled line at second harmonic frequency will be discussed. The theory behind

achieving high efficiency with coupled load is first elaborated including the derivation of the design equations that could be used during design phase for quick evaluation of the design parameters. Class E operating condition can be easily achieved with the proposed load and the derived equations provides quick estimation to the design parameters required. To verify the workings of the load network, a power amplifier operating at 1.2 GHz was designed and fabricated with the use of a commercial transistor device and the corresponding simulation model.

From the conception of a novel circuit design to the fabricated end product, the accuracy of the active model is critical to the overall circuit design process. Demand for an accurate device model is further highlighted in the designing of a high efficiency power amplifier design where the large-signal model is tested for its reliability and ability to predict the output power of the active device under large-signal excitation and give a good approximation for the associated current value for the evaluation of the power added efficiency. The high power density of GaN on SiC material system has further emphasized the need for a reliable device model capable of achieving the design needs when designing high power circuits and devices.

6.2.1 Zero voltage switching high efficiency power amplifier

The proposed high efficiency circuit design is based on the principle of zero voltage switching high efficiency power amplification where high efficiency is achieved by shaping the time domain output voltage and current waveform such that the current across the transistor only starts to appear when the voltage across the transistor is zero. In theory, by manipulation of infinite number of harmonic impedances for an ideal transistor device operating in switched mode, a power efficiency of 100% can be achieved [114]. The methodology eliminates any overlaps between the voltage and current time domain waveforms at the transistor output to achieve 100% efficiency with no power dissipation in the device.

Power amplifier designs based on classical high efficiency theories have attained power efficiency as high as 96% for power amplifiers operating in the MHz region [115] with lumped elements most commonly used in the load network. For circuits in the millimeter and microwave frequency range, the use of distributed elements are preferred given the higher Q factor and better performance prediction especially when implementing the circuit using MMIC technologies [116] – [129].

In terms of high efficiency power amplification, load networks consisting of transmission lines have been reported with power added efficiency values greater than 80% [126] – [129]. All of these transmission line load networks are in essence a combination of series and shunt stubs. Studies on the use of coupled line as the load network has been explored previously, but did not venture into the domain of high efficiency power amplification. As illustrated in [130] and [131], the parallel coupled line implemented into the load network of amplifier design was used to achieve large impedance transformation ratio matching and has an added advantage of the inherent DC block property. Power amplifiers design with a load network consisting of a parallel couple line was demonstrated but was limited to the class-A/AB power amplifier design [131].

6.2.2 Novel coupled load

An ideal class-E power amplifier achieves zero voltage switching by presenting the appropriate load impedance at fundamental frequency and open circuit terminations at its harmonic frequencies. A circuit topology of an ideal class-E power amplifier is shown in Figure 6.12 (a). The proposed load network to achieve zero voltage switching high efficiency performance is shown in Figure 6.12 (b) where it comprises of a section of a parallel coupled line section and an open circuit stub. The parallel coupled line section is at quarter wavelength (i.e., $\theta = \pi/2$) of the fundamental frequency and the open circuit stub is at quarter wavelength of the third order harmonic frequency.

Figure 6.12 (a) Conventional class-E topology (b) proposed coupled line load network (c) equivalent circuit of proposed coupled line load network

Based on the works in [132], the exact equivalent circuit for the proposed load network of the high efficiency power amplifier design shown in Figure 6.12 (c). For the two port equivalent circuit of the coupled line, the connecting line has an impedance which is half of the difference between even (Z_{0e}) and odd (Z_{0o}) mode impedance and the series open circuit stubs have line impedances equivalent to Z_{0o} of the parallel coupled line. It can be observed that when the parallel coupled line section is a quarter wavelength long, a series-open circuit will be presented at even order harmonics and the connecting line operates like a quarter wavelength transformer.

For high efficiency operation, the open circuit stub will be transformed to a series-open circuit at the drain terminal for the third order harmonic frequency. Concurrently, the open circuit stub also serves to provide the required inductive load for the class-E fundamental load.

6.2.2.1 Design equations for proposed load network

To derive the equations for the proposed load network, the ideal load network equation to obtain a class-E operation for a power amplifier is considered and shown in equation (6.4) [133]. To obtain the design parameters for the coupled line load network, the impedance of the proposed network based on the quarter wavelength impedance transforming property of the parallel coupled line was first evaluated and shown in equation (6.6). By comparing the resistance and reactance component for equations (6.4) and (6.6), the difference between the even and odd mode impedance of the coupled line and the impedance of the third harmonics open circuit stub is shown in equations (6.7) and (6.8) respectively.

Impedance of class-E fundamental load:

$$Z_{\text{net}} = R_{\text{opt}} \cdot (1 + j \tan 49.0524^\circ) \quad (6.4)$$

Where

$$R_{\text{opt}} \approx \frac{0.1836}{2\pi f_s C_s} \quad (6.5)$$

Impedance of proposed coupled line load network:

$$Z_{\text{net}} = \left(\frac{Z_{0e} - Z_{0o}}{2} \right)^2 \cdot \left(\frac{1}{R_L} + j \frac{1}{Z_1} \tan 30^\circ \right) \quad (6.6)$$

Solving for design parameters of proposed load network:

$$Z_{0e} - Z_{0o} = 2 \cdot \sqrt{(R_{opt} \cdot R_L)} \quad (6.7)$$

$$Z_1 \approx 0.501 \cdot R_L \quad (6.8)$$

6.2.3 Class E amplifier with coupled line load design

To verify the validity of the proposed load network, a high efficiency power amplifier operating at 1.2GHz was designed, fabricated and tested. A commercially available LDMOS power transistor (BLF6G21-10G) was selected and Agilent's CAD simulator ADS was used to perform small-signal simulations as well as time domain analysis with the use of the harmonic balance simulator to design the high efficiency power amplifier. Time domain analysis is critical in the design of high efficiency power amplifiers to illustrate the workings of voltage and current waveform shaping as a result of the presented load network.

The circuit diagram for the high efficiency power amplifier design with the proposed load network is shown in Figure 6.13. The power amplifier was designed to operate at 1.2GHz with an input rf power of 30dBm. The bias applied for the gate and drain line of the transistor device was 2.5V and 28V respectively. Lumped elements such as capacitor and inductors were used as DC block in the input side and DC feed for the gate and drain biasing.

Figure 6.13 Circuit diagram of the high efficiency power amplifier

The transistor was stabilized with a resistor R1 at the gate terminal and a distributed input matching network consisting of TL1 and TL2 was designed to provide good input match to 50 ohms at 1.2GHz. With an output capacitance of 6.2 pF, the initial parameter values of the load network for an ideal class-E operation were derived from equations (6.6) and (6.7). Based on the work in [133], the designed amplifier is operating beyond the maximum class-E operating frequency for the selected transistor device and at the corresponding drain biasing. However, approximation to an ideal class-E operation can still be obtained but with reduced attainable efficiency which explains the lower than expected power added efficiency attained.

Based on the initial parameter values, harmonic balance simulations were performed to optimize the current waveforms to maximize the power added efficiency that could be achieved. The final optimized parameter values for the various elements of the designed power amplifier are shown in Table 6.2. The values in brackets of Table 6.2 refer to the initial design values evaluated from the derived designed formulas. The initial parameter values obtained from the

proposed design equations provided a good starting reference where the time domain current and voltage waveform plots would overlap in a high efficiency manner. The initial simulated power added efficiency for the high efficiency circuit design was around 40 percent and tuning it further increases it to the 62 percent presented in this work.

The simulated voltage and current time domain waveforms at the output of the transistor device for the designed high efficiency power amplifier circuit are shown in Figure 6.14. Characteristic of zero voltage switching is achieved with the output current waveform rising when the output voltage waveform is minimally flat. For the case of the designed power amplifier, zero voltage was not achieved due to the parasitic of the packaged transistor device.

C1	L1	R1	TL1		TL2		Z0e – Z0o	Z1
pF	nH	Ω	Char. imped. (Ω)	Phase, Φ (deg)	Char. imped. (Ω)	Phase, Φ (deg)	Impedance (Ω)	Char. imped. (Ω)
20	10	10	25	20	10	20	39 (28)	25(25)

* values in brackets are evaluated from eqns (6.6) and (6.8)

Table 6.2 Parameter values for the designed power amplifier

From the time domain analysis point of view, high efficiency operation was achieved with the reduced overlap of the output current and voltage transistor waveform. From the harmonics tuning power point of view, the proposed load network provided a negative reactance load at second and third order harmonics which is the characteristics for class-E power amplifiers [134]. Consequently, the power amplifier designed was fabricated on a Rogers RT6002 substrate with ϵ_r of 2.94 and a thickness of 20mils. A photograph of the fabricated test circuit with SMA connectors is shown in Figure 6.15.

Figure 6.14 Simulated time domain waveforms of voltage (blue trace) and current (red trace) at transistor output

Figure 6.15 Photograph of the fabricated high efficiency power amplifier

6.2.4 Measurement results

Before measuring the power performance of the fabricated circuit, the frequency response for the fabricated high efficiency power amplifier circuit was measured. The applied gate and drain biasing was 2.5V and 28V respectively. The small

signal input rf power for the measurement was -10dBm. The comparison between the measured and simulated results for both the return loss and insertion loss is shown in Figure 6.16 to Figure 6.18.

Figure 6.16 Frequency response comparisons between the measured (blue trace) and simulated (red trace) input return loss

Figure 6.17 Frequency response comparisons between the measured (blue trace) and simulated (red trace) insertion loss

Figure 6.18 Frequency response comparisons between the measured (blue trace) and simulated (red trace) output return loss

Good match between was generally observed between the measured and simulated small signal parameters for the insertion loss and the return loss of the output port. For the return loss of the input port, slight discrepancies were observed between the measured and simulated plots apart from the designed frequency of 1.2GHz but the general performance trend can be observed.

The measured performance for the output power, gain and the power added efficiency with comparison to the simulated values are shown in Figure 6.19 and Figure 6.20 respectively. The measurements were performed under pulsed DC condition with the pulse width set to 20 μ s having a duty cycle of 1%.

Figure 6.19 Measured and simulated rf output power and gain at different input rf power

Figure 6.20 Measured (blue trace with x markers) and simulated (red trace) power added efficiency at different input rf power

Good agreement was obtained between the simulated and measured performance for the designed high efficiency power circuit. At an input rf power of 30dBm, the

output power measured from the test circuit was 42 dBm with a gain of approximately 12 dB and power added efficiency of 67% was achieved. The device model was able to predict the performance of the fabricated circuit adequately allowing the circuit designers to save on design time and effort.

6.2.5 Discussion

The high efficiency power amplifier design using a pair of coupled line load was demonstrated using hybrid circuitry with LDMOS. With the active device model derived from the modeling procedures described in chapter 2 to 5, a MMIC version of the proposed high efficiency circuit can be realised. Improvements made to the active current modeling with respect to the overall conductance modeling will give a better prediction in terms of the fabricated device performance and other evaluated parameters such as the power added efficiency. The work on improving the empirical modeling of the linear region meant that the loadline for the high efficiency power amplifier design would be better represented in simulations.

Two innovative design methodologies in the form of active circulator and class E power amplifier with coupled line load were presented in this chapter for circuit designs involving active devices. The conception of the innovative design methods to the realization of fabricated circuits needs to be complemented with well modeled active device in the design phase of the circuits. The accuracy of the active model will continue to be an important and integral part of the MMIC process and the advantages of the technology can be fully harnessed with the understanding of the active device.

Chapter 7 Conclusion and future work

Modern day electromagnetic CAD tools have the capability to perform large-signal simulations such as harmonic balance simulations to aid in the design of high power amplifiers to be used in wireless communications applications. The prerequisite for a successful circuit design is having an accurate large-signal model to give a good prediction of the circuit performance and also allowing circuit designers to do meaningful fine tuning to achieve the desired outcomes. The merits of the GaN based devices have prompted much research work in the characterization, modeling and the understanding of the active devices. The unique properties of the GaN material such as high breakdown voltage and current density coupled with the appropriate substrate have made the devices favorable for power amplification applications.

In this thesis, through the characterization and modeling of an AlGaIn/GaN HEMT, the device modeling process was accounted in detail. The systematic step of deriving the large-signal model starting from the data acquisition step up to the derived model verification was presented. An empirical approach was adopted to model the measured device performance and the modeling accuracy issues previously not encountered with GaAs device were discussed. Simulations performed with the implemented large-signal model proved to be able to match well to the measured data. Following the characterization of the active device, novel circuit design was presented. The novel circuit design brought to focus was the modular approach to design an active circulator and the coupled line load capable of achieving class E high efficiency power amplification. The effectiveness of the presented novel circuit design is only as accurate as the device model used to simulate the circuit which highlights the importance of an accurate device model.

The key research results will be summarized in the following paragraphs followed by the possible future research work subsequent to the end of this thesis work.

7.1 Key research results

The motivation for the work in thesis was highlighted in chapter 1 with the focus on the need for an accurate large-signal model remaining a crucial part of the rf community today. The aim of this work is to generate an accurate large-signal model through the modeling of different elements and the novel circuit design simplifies circuit design methods previously practice at the same time highlights the importance of having a good device model. The merits of the different material system and the challenges faced when working with GaN based device was discussed in chapter 2 of the thesis work.

The modeling procedures to achieve the large-signal model were elaborated in the beginning of chapter 2. The pulsed DC measurement which is frequently used to model GaN based device was examined next. The pulse width required to obtain a true isothermal pulse characteristic was remarked to be narrower than what was expected for some of the research work. However, the use of the quasi-isothermal profile was able to illustrate the effects of current dispersion effects due to the gate and drain lag phenomenon which is attributed to the charge trapping effects. This brings to the attention of the quiescent dependence in the pulsed current profile which would be investigated subsequently. Part of chapter 3 is also dedicated to the extraction of the extrinsic parameter values that is not bias dependent and illustrate that the cold FET method is sufficient for parasitic extraction with good data acquisition and data processing.

The modeling of the large-signal elements was discussed next in chapter 4. The main source of non-linearity comes from the drain to source current element and substantial effort was attributed to improve the modeling capabilities of the empirical model. Amendments to existing current equations were aimed to improve the match between simulated and measured current data and in particular the portion of the current profile before reaching its peak transconductance biasing value. The abovementioned portion of the current profile is essential for reduced conduction high efficiency power amplifier analysis in which the power amplifier is usually biased at. The current value is especially critical for high efficiency power amplifier design as the power added efficiency is sensitive to the effects of the current drawn by the amplifier circuit. The accuracy of the linear region was also improved given the importance of the linear region used load line analysis for power amplifiers operating in the switch mode. The pulsed current profile was discussed next and a direct relationship was drawn between the quiescent biasing and the current parameters of the proposed current equations. This would greatly aid in the design of the circuit with pulsed operations and increase the understanding of the pulse performance of GaN based devices. The topic on large biasing was also elaborated on with proposed function affixed to the empirical current formulation to cope with the issue of erroneous current prediction with the large biasing voltage that could be applied on GaN based devices. The diode equations were amended accordingly with the issue of simulating large biasing voltages with the device model in mind.

A new method was proposed for the modeling of the charge sources by considering the equivalent circuit for conventional small-signal capacitance model. The proposed method reduces the complexity of capacitance extraction and offers a more straightforward charge source empirical formulation. The proposed method will eliminate any convergence issue due to the violation of charge conservation rule.

The various elements for the large-signal model have been presented in the previous chapter and an additional element was included to model the rf dispersion that exist between the DC and rf performance. Following which the verification of the large-signal model was presented. The model exhibited good match between the measured and simulated data for the static and pulsed IV traces, multi-bias s-parameters and single tone power sweep measurements.

Following the derivation for the large-signal model, innovative circuit design was presented. The modular approach to design active circulator made use of the unique property of circulators to derive a scalable circuit design method. The modular approach allows the quick design of even broadband active circulators by making use of the broadband modules. The second part of the chapter presented a coupled line load with simple design equations which is capable of attaining class E power amplification. The design exploited the inherent property of coupled line to achieve high efficiency power amplification. The success of the proposed innovative circuit design methods to save on design time and effort is dependent on the accuracy of the device model which further highlights the importance for a accurate large-signal model. A summary of the key contributions for this thesis work is listed in Table 7.1.

Current modeling approach and circuit design issues	Key contributions
Poor match for IV characteristics prior to peak transconductance	Proposed new modeling approach to model conductance and transfer function separately
Modeling of self heating effects on IV	
‘Kink’ phenomenon observed at triode region	Identify V_{GS} dependence in the triode region
High voltage application on simulation model	Introduced additional function to control the ever increasing

	transconductance value
Dependence of pulse IV profile on quiescent biasing	Derive the parameters and establish correlation between quiescent biasing and pulse IV profile
Charge model might result in convergence issues	Proposed new charge extraction method and switching function to ensure convergence
Capacitance values at applied VDS of 0V	
Broadband design for active circuits	Introduce modular approach to design active circulator scalable to other frequencies and broadband performance achieved with broadband modules
Complex design process for high efficiency power amplifier	Proposed coupled line load can satisfy class E operating conditions easily and derive formulas can provide quick design parameters estimation

Table 7.1 Table of summary for key contributions

7.2 Future work

Having achieved good modeling results for the data collected at ambient temperature, the next step of modeling would be the thermal modeling of the active device. The temperature dependence of the modeling parameters and the different methods to obtain the thermal time constant and thermal resistance of the device will be studied. The understanding of the thermal characteristics for the active device would allow better performance prediction when using the model to simulate real world applications at different ambient temperature.

The characterization of the device performance through empirical methods will continue to be the most practical approach to model the active devices in the future. The accuracy of the derived model to predict device performance would only be as accurate as the modeling data obtained from measurements which highlights the importance of a good data acquisition process.

Apart from reliable and accurate data acquisition process, the challenge for modeling work in the future would still be the derivation of appropriate empirical formulation to represent the various characteristics of the modeled device, having an accurate empirical parameters extraction process and the implementation of the derived empirical model in circuit simulators. Emerging device technologies will continue to see greater power handling capability and frequency of operation for the active device and adaptations to existing modeling work is essential to ensure good performance prediction can still be achieved.

Research on the subject of innovative circuit design shall continue with the aim to simplify the circuit design procedures and at the same time attain good frequency performance and make improvements to the size of the circuitry.

The proposed modular approach has laid the foundations for an alternative method to design an active circuit with the use of well known passive circuits. The approach can be extended to the development of other circuits and by exploiting the accurate performance prediction property of the modeled active device, the design of such active circuits can be accomplished more effectively using CAD tools.

Accurate active device representation and innovative circuit design methods will continue to be the interest for future researches to tap from both the advancements in the field of microelectronics and fabrication capabilities.

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List of Publications

1. H.Y. Lim, Z.C. Wei, Z. Li, G.I. Ng, and Y.C. Leong, "Design of a full band, compact waveguide-microstrip power splitter using multilayer PCB technology," *2009 IEEE Int. Symp. on Radio Frequency Integration Technology*, pp 273-275, 2009
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