Analysis and design of a highly efficient and versatile DC-DC converter

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**ANALYSIS AND DESIGN OF A HIGHLY
EFFICIENT AND VERSATILE DC-DC
CONVERTER**

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**A report submitted to the Nanyang Technological University in fulfillment of
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ABSTRACT

The thrive of battery-operated devices and connected devices with the vision of Internet-of-Things (IOT) calls for efficient and versatile Direct Current to Direct Current (DC-DC) converters to fulfil the ever-growing power demand.

Adaptive on-time (AOT) control of DC-DC converters has the advantages of simple structure, good light load efficiency and fast response to load step. The purpose of this research is to develop AOT control in two areas: digital control for its process scalability and flexibility, and ultra-low-power operation. Novel circuit blocks and techniques have been developed to improve the performance of AOT control, which are listed as follows.

For data conversion required by digital control, a flash analog-to-digital converter (ADC) using NOR gates as comparators has been proposed and verified by simulation and a prototype chip using 0.35 μm CMOS process. The advantages of the proposed ADC include low power, high speed and small silicon area.

Two methods have been proposed to achieve near optimum load transient response: level-based multi-loop control and body-brake. Level-based multi-loop control is able to achieve near minimum output voltage deviation during load transient using a simple algorithm. A new detection method is proposed for body-brake technique to further improve the unloading response.

A counter-based dead-time optimization method has been proposed to improve conversion efficiency under heavy load. Under specific simulation conditions, 2.3% efficiency improvement has been observed.

In the study of ultra-low-power operation, we further develop the existing method of duty-cycled operation that dynamically changes the system operation frequency with a low-power relaxation oscillator. The duty-cycled operation is

referring to the scheme that all active circuit blocks except the system clock are turned off when all the outputs are in regulation, hence the system quiescent current reduces to the system clock block current only. It has also demonstrated that making on-time adaptive to input voltage improves the peak efficiency by about 1% over the input range of 2.65 V to 3.3 V, by a prototype chip using CMOS 0.18 μm process.

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LIST OF SYMBOLS

Symbol	Nomenclature
ADC	Analog-to-Digital Converter
AOT	Adaptive On-Time
BOM	Bill of Material
C	Capacitor
CCM	Continuous Conduction Mode
COT	Constant On-Time
DAOT	Digital Adaptive On-Time
DC-DC	Direct Current to Direct Current
DCM	Discontinuous Conduction Mode
DITOB Converters	Dual-Input-Tri-Output Buck-Boost converter
DPWM	Digital Pulse-Width Modulator
DSP	Digital Signal Processor
DTC	Dead-Time Controllers
Du	Duty Cycle
DVS	Dynamic Voltage Scaling
EMI	Electromagnetic Interference
ES	Engineering Sample
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
IC	Capacitor current
I _{inductor}	Inductor current
I _{load}	Load current
IOT	Internet of Things
L	Inductor
LCO	Limit Cycle Oscillation

LIST OF SYMBOLS

Symbol	Nomenclature
LDO	Low-Drop-Out regulator
L_{es}	Capacitor equivalent inductance
LUT	Look Up Table
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
PFM	Pulse Frequency Modulation
PID	Proportional-Integral-Derivative
PV	photovoltaic
PVT	Process, Voltage, and Temperature
PWM	Pulse-Width-Modulation
R_{dc}	Inductor DC resistance
$R_{dson,hs}$	conduction resistance of PMOS
$R_{dson,ls}$	conduction resistance of NMOS
R_{es}	Capacitor equivalent resistance
RF	Radio Frequency
R_o	Load resistance
SR	Synchronous Rectification
TIQ	Threshold Inverter Quantization
V_d	Diode voltage drop when forward biased
V_{in}	Input voltage
V_{out}	Output voltage
VRM	Voltage Regulator Module
V_{th}	MOS threshold voltage
WSN	Wireless Sensor Network
ZOH	Zero Order Hold

Chapter 1 Introduction

1.1 Motivation

This work attempts to address the requirements of DC-DC converters in the following two areas: portable applications and energy harvesting applications.

1.1.1 Portable Applications

The recent development in the communication network and mobile broadband has made the connection between individuals and the outside world closer than ever before, which triggers huge demand for handheld communication equipment. In 2009, a total of 1.13 billion mobile phone units had been shipped worldwide and the converged mobile devices (smartphones) are expected to grow by 30% year on year [1].

Smartphone is a cellular telephone with built-in applications and internet access, which provides digital voice service as well as any combination of text messaging, e-mail, web browsing, still camera, video camera, MP3 player, video player, television and organizer [2]. All these functions are powered by a single compact Lithium Ion battery. To provide better user experience, mobile device needs to have a small form factor and long battery hours on each charge. The advancement of battery technology alone cannot keep up with this ever-growing demand for power. The size limitation also forbids the use of larger battery pack in smartphones. Hence smart power management to improve the overall system efficiency is essential to extend battery hours. The reduction in the wasted power also helps to conserve energy and reduce greenhouse gas emission.

In a mobile phone system, a number of voltage levels are required by

different functional blocks, e.g. 1.2 V for processor and 1.8 V for memory. To reduce the overall solution size, DC-DC converters are usually integrated with low-drop-out (LDO) regulators to form a specific power supply unit, or even integrated with other functional blocks [3, 4]. The power supply unit is required to meet the stringent static and dynamic voltage accuracy requirement [5] and yet be cost-effective since the target users are mainly price-sensitive consumers. The external component size and cost should also be minimized.

Most of the time, mobile phones are operating in the standby mode: all the functions are turned off except the chipset that receives signals from the base station. At standby mode, the load current drawn from the power supply unit is light. And when the user starts to make a call or activate other functions of the mobile phone, the load current will suddenly increase. DC-DC converter is required to regulate the output voltage within the required range in the shortest possible time. To extend battery hours, DC-DC converter is required to maintain high conversion efficiency across entire load range.

The above mentioned requirements by the battery operated devices call for highly efficient and versatile DC-DC converter that is able to operate in the optimized modes under different application scenarios to maximize the power conversion efficiency. The switching from one operation mode to another should be fast and well controlled.

Other requirements include design portability, compatible with the most advanced process and insensitive to the variation and ageing of external components. It is also preferable that the DC-DC converter can communicate with other parts of the system and can be configured and optimized on-the-fly to operate under different input voltages and load currents.

Meanwhile, due to continuous scaling in digital process following the Moore's Law, the cost of digital ICs has reduced over the years. Many circuit functions that are traditionally realized by analog means are being implemented in digital domain to take the advantage of CMOS scaling. To further reduce the footprint and cost, active research is being done to integrate the power management functions with the digital handset ICs [6].

In the power supply field, to fulfill the increased stringent cost and performance requirements, digital control has received increased attention from both academy and industry. Companies like Intersil [7], Texas Instruments [8], Maxim Integrated [9] and Silicon Lab [10] are releasing products with digital control features. The advantages of the digital control as compared to the analog control will be further discussed in Section 2.3.2.

The important performance parameters of the DC-DC converter in portable system include the following.

1) Efficiency. In battery-operated portable systems, the importance of the efficiency is paramount to extend the battery time and provide better user experience. Since the load current changes from a few μ As to a few hundred mAs, to maintain high conversion efficiency over the entire load range, multimode operation is often necessary.

2) Accuracy. As the power supply of the digital IC goes to lower voltage, the allowable voltage variation for the DC-DC converter output voltage is shrinking as well. DC-DC converter needs to maintain tight regulation under static and transient load/line conditions. The variation in the operating ambient temperature, diffusion process parameters and external component needs to be taken care of as well.

3) Noise. The switching nature of DC-DC converter system inevitably produces switching noise. The output ripple voltage is normally required to be in the range of 10 ~ 20 mV or less for digital loads. If DC-DC converter is used to power up sensitive RF load, for example, GSM power amplifier, there is requirement for the spectral noise level at multiples of switching frequency as well. Inside a mobile device, most of the functional modules are in close proximities of each other. Noise at the DC-DC converter switching frequency as well as the harmonics can easily extend to the frequency modulation (FM) frequency, which impairs the reception of FM radio signal. The electromagnetic interference (EMI) from DC-DC converter must be reduced to the level that other systems can operate correctly.

4) Protection. DC-DC converter needs to be able to protect itself when the load is demanding excessive current or when the load is short-circuited. Since DC-DC converter is a power device capable of supply a few hundred mAs to a few Amperes of current, an uncontrolled fault condition may cause damage to the overall system and may even cause fire under certain conditions. In the life time of DC-DC converter system, the external components inevitably experience parameter drifting due to aging. It is desired that the DC-DC converter system is able to diagnose and report the abnormality in the external component parameters before the drifting causes any potential malfunction of the whole system.

5) Size. Inside portable devices, the space is confined. It is desired that DC-DC converter, along with the necessary external components, occupies as little board space as possible. One way to achieve this is to increase the switching frequency, so that the external energy storage element, the capacitor and inductor, could reduce in component value and size. But higher switching frequency will

cause higher switching loss – more heat will be dissipated and the efficiency will reduce. Increasing switching frequency and reducing inductor value generally improves transient response, while reducing capacitor value degrades it. Hence, for DC-DC converter, contradicting requirements exist and the designer needs to carefully make trade-offs among those requirements.

From the above analysis, the system requirement for DC-DC converter used in the portable application is summarized in TABLE 1.1.1 below.

TABLE 1.1.1 Typical System Requirements in Portable Application

Operating temperature	-30 °C ~ 85 °C
Input range	2.8 ~ 5.5 V
Output voltage range	1.2 ~ 2.5 V
Output current range	10 μ A ~ 500 mA
Output voltage steady-state accuracy	< $\pm 1\%$
Output voltage at no load to full load transient	< $\pm 10\%$
Conversion efficiency	>90% (peak); >50% (full load range)
Quiescent current	<300 μ A

1.1.2 Energy Harvesting Applications

The emerging vision of IOT is pushing the connectivity to an unprecedented new level: to connect a wide variety of computing devices that are uniquely identifiable within the existing Internet infrastructure using standard communication protocols [11]. According to Gartner, there will be nearly 26 billion devices on the IOT by 2020 [12]. Wireless sensor network (WSN) is an

important part of IOT [13, 14]. WSN is preferred to be self-powered by harvesting energy from the environment to avoid costly battery replacement. In such system, DC-DC converters are widely used for energy harvesting, battery charging and output voltage regulation. Since the output power of WSN is usually very low, the quiescent current of the power management system should be as low as possible. Special techniques to fulfil the power requirements of the WSN system needs to be developed for practical implementations [11, 13-19].

1.2 Research Objective

The aim of this work is to research on new system structures and control methods of DC-DC converter to address the efficiency and versatility requirements of portable and energy harvesting applications. The research focuses on improvement of transient response and efficiency across load current ranges as shown in TABLE 1.1.1. Specifically, digital control techniques are investigated to further improve the performance of the existing DC-DC converter system.

Firstly, this work aims to design an area-efficient and low power ADC that is required to convert the analog signal to digital signal before it could be processed digitally to reap the benefits of digital control. The benefits of digital control are discussed in Section 2.3.2. There are specific requirements for ADCs used for digitally controlled DC-DC converters, which makes the general purpose low power ADC structures not suitable for this kind of application.

Secondly, this work aims to research on methods that improve the load transient response of DC-DC converters. Charge balance control in the literature, which aims to recover the output voltage in one switching cycle, is complex and limited by ADC conversion delay as well as external component values. This

research work aims to investigate alternative methods for fast load transient. Necessary circuit blocks have been designed.

Thirdly, this work aims to improve conversion efficiency of DC-DC converters over different load conditions. At heavy load, circuit technique to reduce dead-time loss is targeted. Dead-time is referring to the delay in the driver circuit to prevent simultaneously turning on both high side and low side power transistors. The optimum dead-time is affected by both process variation and operating conditions. It is one of the objectives of this research work to investigate method to minimize efficiency loss due to non-optimum dead-time. And for applications that output power is very small, the method to reduce the quiescent power of the DC-DC converter itself has been studied.

With the above research objectives, attention is also being paid to the power consumption and chip size of the new control methods, so as to generate a practical solution.

1.3 Organization of the Thesis

This thesis is organized as follows. Chapter 2 explains the background of this research. Specific topics that this research is addressing are presented in Chapter 3 to 6. For each specific topic, the requirements are analyzed, with detailed literature reviews on the existing solutions in its respective chapter. After that, the implementations of proposed solutions are discussed. Verification methodology and results of the proposed solutions are presented at the end of each chapter.

In the second chapter, the necessary background about DC-DC converter is given. The application area and classification of DC-DC converter is discussed. Various DC-DC control methods are reviewed. Comparison is done between the

traditional DC-DC converter using analog control method and digital control method. The major building blocks of the digitally controlled DC-DC converter system are reviewed to identify associated design challenges. Hysteretic control in general is reviewed and AOT control has been identified to address the issue listed previously. The limitations and areas of improvement for the existing AOT control method are discussed.

In chapter 3, the design of the only analog block in the digitally controlled DC-DC converter system – ADC is described. The specific requirements of ADC in DC-DC converter system are analyzed. A low-power flash ADC using NOR gates as comparators is proposed. The high speed and low power characteristics make the proposed ADC structure suitable for high frequency digitally controlled DC-DC converter applications. A 4-bit prototype chip has been built and its performance has been verified by simulation and measurement results.

The fourth chapter investigates load transient response of the buck DC-DC converter. A new load transient method based on peak and valley point detection has been proposed to improve the load transient response. A new body-brake algorithm has been developed to improve the unloading transient response.

Chapter 5 and 6 are addressing the efficiency optimization with different focuses. In chapter 5, various losses associated with DC-DC converter has been analyzed and a new counter-based dead-time optimization method is proposed, which mainly deals with heavy load condition. In chapter 6, the method to minimize quiescent power loss is investigated. The optimum on-time is derived. The on-time generating circuit is developed and experimentally verified.

Chapter 7 summarizes and concludes this thesis. Recommendations for further research is presented.

Chapter 2 Overview of DC-DC Converter Control Methods

2.1 Introduction to Voltage Regulator

Every electronic system needs a power supply with specified voltage range for it to operate properly. However, the unregulated power source may not be able to meet this requirement. For example, the voltage of a lithium ion battery may change from 4.2 V when fully charged to 3 V when it is depleted (Fig. 2.1.1). Hence the voltage of the power source needs to be regulated before it is supplied to the electronic system. The voltage regulation process is carried out by a voltage regulator.

Fig. 2.1.1 Lithium Ion Battery Voltage Vs. Capacity [20]

A voltage regulator is an electrical regulator designed to automatically maintain a constant voltage level. Depending on the way how the regulation is carried out, voltage regulators can be classified into two types: linear regulator and switching regulator.

Fig. 2.1.2 shows a typical linear regulator system [21-25]. The voltage across the power transistor is controlled to produce a constant 1.8 V voltage at the output when V_{DD} or load current is changing. The linear regulator is simple, low-cost and low-noise. One major limitation of the linear regulator is that the peak conversion efficiency is bounded by the ratio of output voltage to input voltage, which is low when output voltage is much less than the input voltage. When the linear regulator delivers output current to the load, same amount of current flows through the pass device, which is a PMOS in this particular example. The peak efficiency of the linear regulator is only 50% when V_{DD} is 3.6V. If I_{OUT} is 1 A, then the power loss in the PMOS pass transistor will be 1.8 W. The power loss will convert to heat and eventually this heat has to be removed from the regulator package to ensure reliable operation. Bulky heat sink cannot be used in space constrained applications, for example, smartphones.

Fig. 2.1.2 Linear Regulator Which Produces 1.8 V V_{OUT} from 3.6 V V_{DD}

On the other hand, switching regulator achieves the output voltage regulation through switching means [26-36]. The power transistor in a switching regulator is functioning as a switch: either cut off, or fully turn-on, as shown in Fig. 2.1.3. The loss associated with the power transistor is low since the voltage and current overlap time is short.

Fig. 2.1.3 Switching Regulator Block Diagram (Buck Converter)

Within the period T , when MP is on and MN is off, V_X voltage is pulled to V_{DD} ; whereas when MN is on and MP is off, V_X voltage is pulled to ground level. L and C function as a filter to convert the pulse train at V_X to a DC voltage, V_{OUT} , which is equal to $(V_{DD} \cdot D / T)$, where D is the duty cycle of V_X node voltage waveform and T is the period of switching cycle.

Switching regulator can achieve a much higher efficiency over most of the operation conditions, compared with the linear regulator. The drawbacks of the switching regulator include EMI by the switching action and the ripple voltage at the output. The control circuit is much more complicated which requires larger silicon area. The inductor in the output filter is expensive, which makes the switching regulator's cost higher compared with the linear regulator. TABLE 2.1.1

summarized the comparison between linear regulator and switching regulator.

DC-DC converter belongs to the switching regulator category and it is an important component in battery-operated electronic equipment. It efficiently converts the poorly regulated battery voltage to various well defined voltages to provide power supplies to other IC chips by switching means.

TABLE 2.1.1 Comparison between Linear Regulator and Switching Regulator

	Linear regulator	Switching regulator
Circuitry	simple	complex
Efficiency	low	high
Transient response	fast	slow
Heatsink Size	big	small
Output ripple	low	high
Output form	step down	step down, up and invert
EMI/RFI	small	big

As for linear regulator, due to its simple structure and excellent noise performance, it is still being widely used for noise sensitive applications for example, powering radio frequency (RF) ICs. The voltage difference between the input and output of the linear regulator is usually kept to as low as possible to limit the power loss.

There are mainly three types of DC-DC converters [37]: single-ended inductor circuits, diode-capacitor circuits (charge pump), and transformer-coupled circuits. Depending on the input and output voltage relations, DC-DC converters can be classified as step-up or boost (output voltage is higher than input voltage), step-down or buck (output voltage is lower than input voltage), buck-boost (output voltage can be higher or lower than input voltage), and inverting or inverting buck boost (absolute value of output voltage can be higher or lower than input voltage,

and is in opposite polarity).

Since buck converter using single-end inductor circuit is most widely used in the mobile phone application [6, 38-41], this research work will target this type of converter to explain and demonstrate the concepts.

2.2 Control Methods of DC-DC Converters

For DC-DC converter, as the name suggests, the output, or the control target is a DC voltage. Hence, there is always a voltage control loop in the system [42-46]. In some systems, the output current information is utilized to shape the dynamic response, which forms a current control loop [47-52]. For system with only voltage control loop, the control is called voltage mode control; for system with both the voltage control loop and current control loop, the control is called current mode control. The difference between these two is explained below with the example of a buck converter.

A typical voltage-mode buck converter is shown in Fig. 2.2.1. The error amp amplifies the difference between the feedback voltage and the reference voltage, V_{REF} , to produce the control signal, V_C , with frequency compensation. The control signal is then compared with saw-tooth ramp to produce pulse-width-modulation (PWM) signal to control the on-off of the power transistor. If the output voltage is lower than required value, the error amplifier will produce a larger control signal, which results in a larger duty cycle in the PWM signal; hence the high side power transistor will turn on for longer time and the output voltage will go up. The control-to-output transfer function is of second order, as shown in (2.2.1). To compensate the frequency response, type-2 or type-3 compensation is usually used.

Fig. 2.2.1 Block Diagram of a Typical Voltage-Mode Buck Converter

$$\frac{V_{OUT}}{V_C} = K_v \times \frac{1 + sC_oR_c}{1 + \frac{s}{\omega_o Q_p} + \frac{s^2}{\omega_o^2}}, \quad \text{where } \omega_o = \frac{1}{\sqrt{LC_o}} \quad (2.2.1)$$

In (2.2.1), K_v is a constant, R_c is the equivalent series resistance (ESR) of the output capacitor C_o , Q_p is the damping ratio, and ω_o is the resonant frequency of inductor L and C_o .

The voltage-mode control is simple and relatively easy to implement. But over current protection of the power transistor needs to be implemented separately using current sensing circuit. And due to the fact that it is a second order system, the compensation network is complicated and sensitive to component variations.

For current-mode control, as shown in Fig. 2.2.2, the control signal V_c is used to control the current in the inductor, hence the inductor effectively becomes a voltage controlled current source. The control-to-output transfer function of the current-mode buck converter is first order, as shown in (2.2.2). K_I is a constant and $F_h(s)$ is a second-order pair of poles at half the switching frequency due to sampling effect.

Fig. 2.2.2 Block Diagram of a Typical Current-Mode Buck Converter

$$\frac{V_{OUT}}{V_C} = K_I \times \frac{1 + sC_o R_C}{1 + sC_o R_o} \times F_h(s) \quad (2.2.2)$$

The current-mode control is robust in dynamic response because the control bandwidth can be extended with sufficient phase margin. The over current protection can be simply implemented by limiting the maximum value of the control signal. The disadvantage is that current sensing circuit needs to be accurate amid the switching noise.

2.3 Digitally Controlled DC-DC Converters

2.3.1 Introduction

In the industry, DC-DC converter IC has been traditionally implemented by analog control means due to low cost, robust design and familiar design flow for practicing design engineer. The DC-DC converter systems in Fig. 2.2.1 and Fig. 2.2.2 are both examples of analog control systems.

Digitally controlled DC-DC converters have received increased attention in recent years [53-62], not only from academia but also from industry. Indeed, many commercial products based on this converter topology are already available in the market. And it is estimated that global revenue for digital power devices to reach \$3.3 billion by the end of 2014 and \$11.8 billion in 2018 [63].

Source: IHS, February 2014

Fig. 2.3.1 Global Market Forecast for Digitally Controlled Power Supplies [63]

A typical digitally controlled DC-DC converter system is shown in Fig. 2.3.2. The example shown is a voltage mode buck converter. The output voltage error is sampled and determined by an ADC. A digital compensator computes a duty-cycle control signal based on the output of the ADC. Digital pulse-width modulator (DPWM) converts the duty-cycle control signal to PWM signal and drive the output power transistor on or off through a driver stage which in its simplest form is inverter trains with gradually increased size and driving capability.

2.3.2 Benefits of Digital Control

The main difference between the digitally controlled DC-DC converter and its analog counterpart is that the control loop is implemented in digital manner. This brings a number of benefits:

Fig. 2.3.2 Voltage Mode Buck Converter with Digital Control

- 1) Compatible and scalable with digital process. This makes it possible to integrate DC-DC converter with other digital ICs on the same monolithic substrate. In portable electronic devices, the limited space calls for higher level integration of components. By integrating DC-DC conversion function into the digital ICs, no individual DC-DC converter ICs are needed, hence more functions can be built into the portable devices with the same form factor. The digital blocks can also be scaled with the progress of the silicon processing technology advancement.
- 2) Easiness in porting the existing design to a new process. One issue with the traditional analog control is that once the process technology for analog ICs advances to the next technology node, the existing system will need re-design. Significant time will be spent on circuit design, simulation and manual mask layout. And most probably, the first engineering sample (ES) will need to be fine-tuned to get the required performance since the simulation result might not match well with the actual evaluation. This not only prolongs the lead time to market, but also incurs high initial design

cost. Whereas for digitally controlled DC-DC converters, the digital blocks can be ported to other processes easily, with the help of the readily available digital design, synthesis and auto place-and- route EDA tools. The system performance can be verified by Field Programmable Gate Array (FPGA) before the design goes to diffusion, which can help to capture the design mistakes in early stage and substantially reduce the initial design cost.

- 3) Low sensitivity to operating conditions. Since the control loop is not depending excessively on the linearity of the circuit elements like analog designs, the digitally controlled DC-DC converter is much less sensitive to the change of process parameters, voltage supply and ambient temperature (PVT). The performance of the digitally controlled DC-DC converter is also much less affected by external component variation and aging.
- 4) Able to communicate with other parts of the system. Since other parts in the mobile phone system are mainly digital ICs, it is easier for the digitally controlled DC-DC converter to communicate with other digital ICs on the system level. One example could be dynamic voltage scaling (DVS). Based on the application mode, the supply voltage to the digital IC is dynamically adjusted to lower voltage to conserve the battery power in standby mode or to higher voltage for faster computations when there are many tasks operating simultaneously.
- 5) Advanced control techniques which require extensive data processing can be easily implemented in digital control: for example, charge balance

control [64], auto tuning of the control parameters, self-diagnosis, efficiency optimization, on-line system identification and optimization, etc.

2.3.3 Limitations of Digital Control

Despite the benefits that digital control brings to power conversion, the adoption of it is rather slow in the industry, especially in cost-sensitive consumer product sector. Part of the reason is due to the fact that new skill sets are needed for the practicing designers to design this kind of converter, which has been dominantly designed in test-and-true analog approaches. Digital control itself also has many limitations.

First, to interact with the real analog world, the digital control system needs to first convert the analog signals to digital codes before they can be processed. This requires substantial analog design. A data converter is usually power hungry and occupies large silicon area. The design of data converter is complex. And the LSB accuracy decides the accuracy of the output voltage. Depending on the data converter structure, it is usually not straightforward to port the design to another process. Same portability challenge applies to DPWM as well.

Second, supporting software is usually needed to program the digitally controlled dc-dc converter, unlike its analog counterpart, which is usually self-contained. The initial software development cost is high and error prone, and usually takes long time [49].

Third, when handling complex task, the clocked digital signal usually takes long computation time when it is handled in serial manner. The added delay affects the dynamic response of the control loop.

One more disadvantage is that supporting analog ICs and discrete components

are usually needed if digital control is implemented by using standard digital signal processing (DSP) chip, which adds to the total cost of the system.

Lastly, it is challenging for digital control to match the accuracy and power consumption of the analog control. As explained in Section 2.3.5, high resolution and high switching frequency calls for innovative DPWM and ADC design to keep the area and quiescent current comparable to analog control.

2.3.4 Digital Power System Management

In view of the limitation of digital control, there is another type of implementation called digital power system management [65]. The DC-DC conversion in this kind of system is still done with analog control. A separate IC integrates the digital control functions, which sits between the host and the analog DC-DC converters and communicate to them using some standard protocols, like PMBus [66]. The block diagram of such a system is shown in Fig. 2.3.3.

PMBus defines a standard set of command language that communicates with power management units and system host. It is an open standard, and it can also implement proprietary commands to provide innovative value-added features. Through PMbus, the functions of power rail sequencing, system supervision, voltage margining, operating parameter reporting, fault diagnosis and logging can be achieved on the existing analog converters.

The benefit of this approach is that most of the digital control benefit can be achieved with the existing analog DC-DC converters. However, this approach cannot fully reap the benefit of process scaling and integration. Additional digital power management chips are needed, which increases the PCB size of the power management system.

Fig. 2.3.3 A Typical Digital Power Management System

2.3.5 Major Building Blocks of Digitally Controlled DC-DC Converter

The most common digital controller implementations can be grouped into three major types: programmable signal processor (typically a digital signal processor (DSP)), custom hardware, or some combination of both [10].

The major control blocks in the digitally controlled DC-DC converter system include ADC, digital compensator, DPWM and the driver [67-72].

A detailed discussion of the literatures and requirement of ADC is presented in Chapter 3. Here, the design of the other two building blocks, digital compensator and DPWM, are described.

A) Digital Compensator

The function of the digital compensator block is to ensure the stability of the feedback loop. It also determines the bandwidth of the feedback loop in the event of load transient.

For DC-DC converters with analog control, the compensator block is usually designed in frequency domain by using bode plot and pole-zero placement technique. The design method is intuitive and familiar to the power electronics engineers.

For DC-DC converters with digital control, the compensator block is designed in z-domain. There are mainly two approaches in compensator design: analog-to-digital redesign and direct digital design.

For analog-to-digital redesign approach, the compensator is first designed in frequency domain and then mapped to z-domain by one of the three mapping methods.

(1) Backward Euler

$$s = \frac{1 - z^{-1}}{T_{\text{samp}}} \quad (2.3.1)$$

(2) Bilinear

$$s = \frac{2}{T_{\text{samp}}} \times \frac{1 - z^{-1}}{1 + z^{-1}} \quad (2.3.2)$$

(3) Pole/zero matching

$$\begin{aligned} s + a &= 1 - z^{-1} \times e^{-a \times T_{\text{samp}}} \\ s \pm ja &= 1 - 2 \times z^{-1} \times e^{-a \times T_{\text{samp}}} \cos(b \times T_{\text{samp}}) + z^{-2} \times e^{-2a \times T_{\text{samp}}} \end{aligned} \quad (2.3.3)$$

The comparison of the three mapping methods is shown in TABLE 2.3.1. Among the three, bilinear transformation gives the best gain and phase response up to one tenth of the switching frequency f_{samp} . However all of them do not include the effect of delays due to acquisition, analog to digital conversion, computation and zero-order-hold (ZOH).

TABLE 2.3.1 Comparison of the three mapping methods

Mapping method	Resulting expression	Frequency response
Backward Euler	Simple	Does not preserve the impulse and frequency response of the analog controller
Bilinear	Complex	Accurate up to 10% of the sampling frequency
Pole/zero matching	Simple	Preserves the pole-zero location, but subject to aliasing

For direct digital design, the small signal discrete-time model of the digitally controlled DC-DC converter needs to be developed first [73]. The discrete poles, zeros and complex zero/pole pairs also need to be expressed in discrete-time domain [62]. After that, the discrete-time expressions are mapped to continue-time domain by using the relation in (2.3.4).

$$z^{-1} = e^{-s \times T_{\text{samp}}} = e^{-2j\pi f T_{\text{samp}}} \quad (2.3.4)$$

Since this mapping is exact, the continuous-time analysis is valid for all the frequencies. The continuous-time frequency tools like Bode plot can be used for intuitive controller design. The ability to design complex zeros in this method makes it possible to boost the phase by 180° at the double pole frequency due to the LC filter in the buck converter.

After the z-domain transfer function of the digital controller is obtained by either of the two above methods, a difference equation can be formulated for implementation.

To reduce the complexity of digital compensator design as well as reduce the power consumption, look-up-table (LUT) based compensator method has been proposed [59, 68]. In this method, the compensator output codes are pre-calculated based on the control law and controller parameters and stored in the LUTs. Since

during normal operation, the output of the DC-DC converter will vary around the center value with limited range, which results in limited error code. Based on the error code, the proper compensator output is selected.

In [74], an adaptive approach is proposed to vary the proportional constant and integral constant to improve the load transient response of the digital PID controller.

B) DPWM

In the control loop of a digital DC-DC converter, there are two quantizers, namely ADC and DPWM. Under certain condition, an undesired steady state oscillation of V_{out} and other system variables will happen at frequencies lower than the converter switching frequency. This steady state oscillation is referred to as limit cycle oscillation (LCO) [75]. LCO is usually undesired because it leads to large, unpredicted output voltage variations. Since it is difficult to predict the amplitude and frequency of the limit cycle, the resulting noise spectrum is impossible to be compensated or isolated to comply with the EMI requirement. Due to the increment of the ripple voltage, the efficiency of the system is also affected.

The resolution of the DPWM and ADC is defined as the output variation that is corresponding to 1 LSB change in DPWM input code or ADC output code.

Take the buck converter as an example. The input voltage V_{in} and the output voltage V_{out} are related as shown in (2.3.5), where D_u is the duty cycle of the power transistors in the output stage.

$$V_{out} = V_{in} \times D_u \quad (2.3.5)$$

Suppose DPWM has N_{DPWM} bits, the resolution of DPWM, R_{DPWM} , can be calculated as shown in (2.3.6).

$$R_{DPWM} = V_{in} \times \frac{1}{2^{N_{DPWM}}} \quad (2.3.6)$$

The resolution of the ADC, R_{ADC} , can be expressed as (2.3.7), where ΔV_q is the amount of output voltage change that will result in 1 LSB change in the ADC output.

$$R_{ADC} = \Delta V_q \quad (2.3.7)$$

Limit cycle will happen if the resolution of the DPWM is coarser than ADC, as shown in Fig. 2.3.4. The DC-DC control loop will always try to drive the output voltage to the zero error bit. However, there is no corresponding DPWM output at the zero error bit, hence, the duty cycle will change between two adjacent levels even in the steady state.

To ensure there is always a DPWM output that makes ADC output fall into the zero error bit of ADC, the resolution of DPWM needs to be finer than ADC. Besides that, there should an integral part in the digital compensator so that DPWM output can be stabilized at the required duty cycle [75].

Fig. 2.3.4 Limit Cycle Condition

In [76], the dynamic non-limit-cycle condition has been studied using describing function method. An amplitude and offset dependent dynamic system model is derived. It is shown that the loop gain of the dynamic system should be less than 1 at the frequency where the control loop has a phase of -180° to avoid limit cycle oscillation under dynamic conditions.

To have a finer resolution than ADC, DPWM is required to have higher number of bits. Normal counter-based DPWM is not practical since the clock needs to be in terms of Giga Hertz range to be able to meet the resolution requirement. This posed a design challenge for digitally controlled DC-DC converter operating at high frequency. It has been an active research topic to design high resolution and low power DPWM structure [77].

Hybrid delay-line / counter based DPWM architectures [68, 78] are effective in reducing the silicon area, with the challenge to match the delay of delay-line MSB of and counter LSB to ensure linearity. Adjustable delay line controlled by delay-locked-loop (DLL) [79] is able to mitigate this challenge with added design complexity.

A dithering method has been proposed in [75] to improve the resolution of DPWM by applying a specific pattern to successive duty cycles; hence the effective resolution of DPWM becomes finer. However, the design challenge is how to reduce the low frequency tones produced by dithering.

Multi-bit sigma-delta DPWM[80] has the benefits of fine resolution, low power and small size. It is effective in reduce the amplitude of the low frequency tone generated by dither method. A multi-bit sigma-delta based DPWM combining dithering has been proposed in [81] further reduces the low frequency tone across different duty cycles by adding a random signal before the quantizer.

In [4], it is suggested to avoid a zero at the ADC output by changing the ADC output from -1 to +1 directly at the output rising range. However, the loop gain is affected by this change and the stability issues need to be considered.

With the increase of the switching frequency of DC-DC converters, high resolution and low power DPWM architectures will continue to be a hot research area, especially for DC-DC converters requiring fixed switching frequency.

2.4 Hysteretic Control of DC-DC Converters

In the above discussed control methods, a dedicated PWM block is always present. By comparing the control signal with some ramp signal, a PWM signal with fix period and varying duty cycle is generated, which in turn is used to control the on/off of the power stage switches.

There is another type of DC-DC converter, which makes use of the output voltage ripple as PWM ramp signal [82-87]. This kind of DC-DC converter is usually referred to as ripple-based control [88] or hysteretic control. Fig. 2.4.1 shows the block diagram of a buck converter based on hysteretic control.

A major difference from other PWM converter is that the error amp is removed from control loop. Instead, a comparator (as shown in Fig. 2.4.1) compares the output feedback signal with the reference voltage. The output of the comparator, V_{cmp} , goes directly to PWM Signal Generator block to generate PWM signal.

The way the PWM signal is generated could be different depending on the system requirement. But there are some common features shared by DC-DC converter with ripple-based control:

Fig. 2.4.1 Block Diagram of DC-DC Converter with Ripple-Based Control

- 1) Simple structure as error amp (with associated compensation network) and ramp generator are eliminated;
- 2) Fast transient response. The delay due to compensation network is removed, hence correction to transient perturbations is instant, and usually finishes within one or two switching cycles;
- 3) Good light load efficiency. At discontinuous-conduction-mode (DCM), which refers to the state of operation that inductor current ramps down to zero before the start of next switching cycle, fixed on-time control and hysteretic control result in reduced switching frequency with load current. Since the switching loss is the mainly loss mechanism in light load, reduced frequency leads to reduced switching loss, which greatly improves the light load efficiency.

In this section, the output ripple of a buck converter is first studied. And then various ripple-based control methods are then introduced. The limitations of the

existing solutions are discussed and the target areas of improvement are then identified.

2.4.1 Buck Converter Output Ripple

The output of a buck converter is obtained by filtering the pulse train at the switching node. The duty ratio of the pulse train determines the DC value of the output voltage. Due to the non-ideality of the filter, there is always a small AC component rising on top of the DC voltage level, which is commonly referred to as output ripple voltage.

The frequency response of the LC filter is as shown in Fig. 2.4.2. After its double pole frequency, ω_o , the LC filter is able to attenuate the high frequency ac component. The attenuation increases with frequency at a rate of 40 dB per decade. At the switching frequency, the attenuation ratio is $40 \times \log(\omega_s/\omega_o)$.

Fig. 2.4.2 Frequency Response of LC Filter in Buck Converter

The equivalent series resistance of the output capacitor, R_{es} , also contributes to the over-all ripple voltage since it develops a ripple voltage component in response to the capacitor charging and discharging current. Unlike the ripple component due to output capacitor which is 90 degree lagging the switching node

voltage, the ripple component due to R_{es} is in phase with the switching node voltage under continuous conduction mode (CCM), which refers to the state of operation that inductor current stays above zero, as shown in Fig. 2.4.3.

The output ripple of the buck converter is a combination of the output capacitor ripple and R_{es} ripple. If the value of R_{es} is large, the output voltage ripple has the same shape as the inductor ripple current without phase delay. If the value of R_{es} is small, the output ripple has phase delay comparing with the switching node voltage, which may lead to sub-harmonic oscillations in some ripple based control scheme [85].

Fig. 2.4.3 Current Waveforms and Voltage Ripple of Buck Converter in CCM

2.4.2 Types of Ripple-Based Control

Based on control topologies, the ripple based control can be further classified to: hysteretic control, constant on/off time, constant frequency peak/valley control, etc. In this section, the operations of two basic topologies: hysteretic control and constant on-time control, are presented.

A) Hysteretic Control

In this type of control, comparator block is implemented with hysteresis band, V_H . Usually the hysteresis band is made to be centered at V_{REF} (as shown in Fig. 2.4.1). Hence the lower hysteresis band is $(V_{REF} - 1/2 \times V_H)$ and the upper hysteresis band is $(V_{REF} + 1/2 \times V_H)$. When the feedback signal is lower than the lower hysteresis band, PWM signal generator block turns on the high side MOSFET, M_P as shown in Fig. 2.4.1. The inductor current ramps up and the difference between the inductor current and load current charges the capacitor, which brings the output voltage up. When the feedback signal is higher than the upper hysteresis band, M_P is turned off and M_N is turned on (for synchronous control). M_P will stay off until the output voltage is low again and the cycle repeats.

Hysteresis control [89-93] is one of the simplest DC-DC control methods. The switching frequency under DCM is proportional to the load current, which brings the improved light load efficiency. Under CCM, the switching frequency is a strong function of output capacitor parameters [88]. The changing in switching frequency may not be acceptable in noise-sensitive applications. Another drawback is that the hysteresis band cannot be designed to be very small considering the accuracy requirement to the comparator and reference generation circuit, which makes the output ripple relatively large.

B) Constant On-Time (COT) Control / Adaptive On-Time (AOT) Control

For COT [54, 83, 85, 94, 95], only one threshold is needed for the comparator. When the feedback voltage is lower than the comparator threshold, the PWM signal generator block will turn on the high side MOSFET for a fixed amount of

time. After that, no matter whether the output voltage is high or not, the high side MOSFET will be turned off and the low side MOSFET will be turned on. Usually there is a minimum turn-on time of the low side MOSFET for stability reasons. After that, if the output voltage is higher than target, M_P will stay off, just like the case of hysteretic control. If the output voltage is still lower than target, another fixed on-time will be generated to turn on the high side MOSFET.

Unlike hysteretic control, COT regulator is prone to sub-harmonic oscillation if the below criteria is not met [88].

$$T_{on} < 2 \times R_{es} \times C_{out} \quad (2.4.1)$$

Under DCM, the switching frequency of COT regulator is proportional to load current, which produces excellent light load efficiency, just like the hysteretic control.

It can be derived that under CCM, the switching frequency of constant on-time regulator is:

$$F_{sw, cot(CCM)} = \frac{V_{out}}{V_{in} \times T_{on}} \quad (2.4.2)$$

From (2.4.2), if T_{on} is made proportional to (V_{out} / V_{in}) , the switching frequency is constant with first order approximation.

Here, the term of adaptive on-time (AOT) control is defined to be the type of constant on-time control which changes the on-time depending on the operating conditions, such as input voltage and output voltage, so as to improve the system performance. And this research focuses on AOT control.

2.4.3 Limitation of AOT Control

Digital control can be applied to AOT control to improve its performance and take the advantage of the benefits that are discussed in section 2.3.2. The digital implementation of AOT control involves changing the comparator block to ADC and changing the PWM signal generator block to digital On-time Generator block, as shown in Fig. 2.4.4. A similar implementation can be found in [83] for voltage regulator module (VRM) applications. This kind of control is referred as digital adaptive on-time (DAOT) control in this report.

Fig. 2.4.4 Digital Ripple Controller Block Diagram

In this implementation, a fast ADC is needed to reduce the loop delay. A comparator can be considered as a 1-bit ADC with limited information for adaptive control. It can be seen in the following chapter that, by knowing the output voltage profile, the transient response of the ripple controller can be further improved.

For both analog and digital implementation of AOT control, unloading

transient response is slow if it happens during on-time, since the high side MOSFET will stay on even if the output is already higher than target.

And it is desirable to further improve the efficiency of converter based on AOT control over the whole operating load range, both heavy load and light load. In this report, heavy load is referring to load current that is at or above DCM/CCM boundary, while light load is referring to load current that is well below DCM/CCM boundary and close to its quiescent current. Since different factors dominate the converter efficiency under heavy load and light load, different optimization methods are needed.

2.4.4 Proposed Solutions

In the following chapters, the solutions to the challenges discussed above are proposed, which are summarized in this section.

A NOR gate based flash ADC is discussed in chapter 3, which addresses the general analog-to-digital conversion requirement of digital control.

In chapter 4, transient response improvements are presented. A level-based load transient response improvement method is first presented to enhance the multi-loop control algorithm. To improve the unloading response, body brake and its related control timing is proposed. A LUT based reference tracking method is described in the Appendix A, which is very suitable for digital implementation.

Chapter 5 deals with the heavy load efficiency improvement by proposing a counter-based dead-time optimization algorithm.

At last, chapter 6 studies the ultra-low-quiescent-power operation of AOT in energy harvesting applications based on duty-cycling and optimum on-time operation.

Chapter 3 Threshold Inverter Quantization (TIQ) Based Flash ADC

DC-DC converter regulates its output to a target value by a voltage control loop. The input to the voltage control loop is the error voltage (the difference between the desired output voltage and the actual output voltage). In the digitally controlled DC-DC converter system, an ADC converts the error voltage to discrete form and sends the resulting digital code to compensator block to generate duty signals. The inputs to ADC include sampled DC-DC converter output voltage, reference voltage and often, a clock signal.

In this chapter, the required design parameters of ADC for digitally controlled DC-DC converter are first analyzed, followed by literature review of the reported structures. A new flash ADC using NOR gates as comparators is then proposed. The design details of the functional blocks are given. The performance of the proposed ADC is verified by simulation and measurement result of a test-chip.

3.1 ADC Design Parameters

The requirement of the ADC in a digitally controlled DC-DC converter is analyzed as following:

1) **Accuracy.** For a typical DC-DC converter, a DC accuracy of $\pm 1\%$ and a transient accuracy of $\pm 10\%$ are usually required. That is to say, the LSB of the ADC should be less than 2% of the required output voltage. And the ADC should be able to resolve 90%~110% of the required output voltage in order for the controller to properly compensate the transient response. In another word, a windowed ADC, which converts a certain range ("window") of the input voltage, rather than the entire range, is needed. The DPWM resolution needs to be finer

than ADC to avoid limit cycle oscillation, as explained in Section 2.3.5 (B).

The required number of bits for the ADC:

$$NOB = \log_2^{\frac{20\%}{2\%}} = 3.3 < 4 \quad (3.1.1)$$

A 4-bit ADC is sufficient for the required accuracy. Hence, a 4-bit ADC will be designed to demonstrate the concept.

2) **Conversion time.** For clocked ADC like SAR or pipelined ADCs, from the time the signal is available at the input to when the digital code is produced, a finite time is needed, which is called conversion time. The conversion time should be just a small fraction of the switching period for robust response in the event of sudden output change.

3) **Power consumption.** Low power operation is desired to improve the overall system efficiency.

4) **Digital process compatibility.** The ADC should not depend extensively on the matching of analog components; otherwise extensive re-design work is necessary when process node is changed.

3.2 Literature Review of ADC

In this section, ADC structures that have been used for the digitally controlled DC-DC converter in the literature are reviewed.

3.2.1 Delay-line ADC

Delay-line based ADC makes use of the nonlinear voltage-to-delay property of the digital building block to quantize the error voltage [68].

The propagation delay t_d of a logic gate is given as following:

$$t_d = K \frac{V_{DD}}{(V_{DD} - V_{th})^2} \approx K \frac{1}{V_{DD}} \quad \text{if } V_{DD} \gg V_{th} \quad (3.2.1)$$

In the above equation, V_{DD} is the power supply voltage, K is a process related constant and V_{th} is the threshold voltage of the MOS device. From this equation, it can be seen that the gate delay will reduce with the increase of V_{DD} . If V_{DD} is much higher than V_{th} , to the first order approximation, t_d is inversely proportional to the power supply voltage.

Fig. 3.2.1 shows an n-bit delay-line ADC configuration. The power supply node of the delay cell is used to sense the analog input voltage. Depending on the sensed voltage level, the propagation delay of each cell will change. At the beginning of conversion, a “test” signal goes from low to high and propagates through the delay cells. At the end of the conversion, a “sample” signal is used to capture the output of the delay cells. Depending on the cell delay, which is a strong function of input voltage, the signal will reach certain cell in the string upon the “sample” signal. Based on the state of the delay cell output, an encoder is used to generate the digital output.

Fig. 3.2.1 N-Bit Delay-Line ADC Configuration

Complete digital implementation and synthesis of the delay-line ADC is possible and the power consumption is low. The averaging effect of the multiple delay cells compensates partially the variation of delay element's voltage to delay relationship due to process.

However, this approach will need large silicon area when a tight output voltage regulation is required. And it needs to propagate the test pulse at the beginning of each conversion cycle, which causes conversion delay and phase shift of the control loop. Furthermore, the voltage-to-delay relationship applies for a short range of analog input only. When the analog input is required to change, which is often an important requirement of the DC-DC converter, a divider and a voltage buffer are necessary to bring the voltage to the range where the voltage-to-delay relationship applies.

To get a precise output voltage, the delay-line needs to be calibrated against process variation and temperature change. One calibration method is shown in Fig. 3.2.2 [68]. Two conversions are performed in one switching period. Firstly, the delay line is connected to the reference voltage. The conversion result is stored in a register. Then the delay line is connected to the sense voltage, the conversion result is then subtracted by the value stored in the register to get the calibrated error code. The calibration does not need to be done every cycle.

Fig. 3.2.2 N-Bit Delay-Line ADC with Calibration

The self-strobed delay-line ADC was proposed in [71]. As shown in Fig. 3.2.3, a reference delay line was added which consisted of one slow delay cell and N_r fast delay cells, while the input delay line consisted of one slow delay cell and (N_r+4) fast delay cells. The taps of the last nine fast delay cells were connected to the latch and encoder. At the beginning of the conversion, the “clk” signal simultaneously travels through both delay-lines. When the “clk” signal reached the end of the reference delay-line, it will take a snapshot of the state of the input delay-line. If the input voltage is higher than the reference voltage, the delay of each cell in the input delay-line is shorter than that in the reference delay-line; hence the “clk” signal will travel further in the input delay-line, vice versa. By using this method, a wider input range can be achieved with a small number of delay cells. One design challenge is that the two delay-lines need to be matched.

A differential sensing technique is applied to the self-strobed delay-line ADC in [96] to improve the sensitivity without increasing the element size and biasing current, as shown in Fig. 3.2.4. The source-degeneration transistors in the original design are replaced by the gm amplifier. The delay in the reference delay-line,

instead of being constant, changes with the sense voltage, which improves the sensitivity of the ADC.

Fig. 3.2.3 Self-Strobed Delay-Line ADC Configuration [71]

Fig. 3.2.4 Differential Sensing Self-Strobed Delay-Line ADC Configuration [96]

In [97], an asynchronous power saving controller turns off all the delay cells once the conversion is done after self sampling, which reduces the standby current consumption significantly.

3.2.2 Flash ADC

A “window” flash ADC was suggested in [56] based on the traditional flash ADC structure, aiming to reduce the latency of the ADC conversion in VRM applications where the transient response is of great importance. The comparator at both ends of the “window” can also be used as the indicator of out-of-window transient event, so that the fast recovery algorithm like duty cycle saturation can be implemented. For this structure, shown in Fig. 3.2.5, the matching between the comparators as well as the current consumption are the two major design challenges.

Fig. 3.2.5 “Window” Flash ADC Configuration

A 6-bit Threshold Inverter Quantization (TIQ) asynchronous ADC was suggested in [90], which is shown in Fig. 3.2.6. The comparators in the traditional flash ADC structure are replaced by inverters with different switching point. Advantages of using digital inverter as analog comparator include: eliminating the need of high gain differential input voltage comparator; eliminating the need of resistor ladder circuit to generate reference voltage if the output of DC-DC converter is a fixed value; and approximately ensuring an ADC LSB over the process parameter variation. Disadvantage is that the absolute characteristic of the ADC cannot be ensured. Hence, an ancillary circuit for the offset compensation is needed. And most of time, the DC-DC output voltage needs to vary, so voltage scaling circuit like resistor ladder is usually still needed.

Fig. 3.2.6 TIQ Based Flash ADC Configuration

3.2.3 $\Delta\Sigma$ ADC

A $\Sigma\Delta$ ADC followed by a decimator structure has been shown in Fig. 3.2.7 [98]. The ADC is first order with over sampling ratio of 32, which gives 5bit conversion. The input window is ± 20 mV. The common mode input voltage was rejected by switch capacitor network. A 32-cycle accumulate-and-dump is used as a decimator, which effectively functions as a comb filter to attenuate the noise at multiples of switching frequency. The $\Sigma\Delta$ ADC achieves small quantization level without using precisely matched analog component, yet can operate in low supply voltage. The drawback of this approach is that a high frequency clock rate is needed. In [98], a 100 MHz clock is used to get a sampling frequency of 3.125 MHz after decimation.

Fig. 3.2.7 $\Delta\Sigma$ ADC Configuration[98]

3.2.4 Frequency Domain ADC

An averaging windowed ring-ADC which is nearly entirely synthesizable has been reported in [72]. The ring-ADC is based on the principle that the switching

frequency of the CMOS ring oscillator is linearly related to the bias current when biased in sub-threshold region. The configuration of the ADC is as shown Fig. 3.2.8. The tail current of the differential pair is designed such that the two matched ring oscillator will be operating below threshold voltage. The differential pair is sized to operate in the saturation region at the maximum possible difference voltage between the input voltage and reference voltage. Depending on the voltage difference, the ring oscillator will have different frequency based the bias current received. The frequency information is then captured by a counter. The difference in frequency is then used to calculate the digitized error voltage D_e .

Comparing to the delay-line based ADC, the resolution of the developed ring-ADC is invariant under reference voltage changes because of the common mode rejection capability of the differential pair used. However, a faster clock is required to achieve better resolution.

Fig. 3.2.8 Ring Oscillator Based Frequency Domain ADC Configuration [72]

A frequency domain ADC structure based on first-order, 1-bit $\Sigma\Delta$ frequency discriminator without the need of analog integrator was presented in [53]. As shown in Fig. 3.2.9, the input voltage and reference voltage are both converted to frequency using ring-oscillator-based VCOs and modulated by single-bit $\Delta\Sigma$

discriminator. The resultant signals are subtracted and decimated using the 2-stage comb (CIC) filter before being applied to the compensator input. Similar to the ring-ADC, the design can be synthesized easily since almost all blocks are digital. However, the matching of the two oscillators to generate linearly voltage-dependent output oscillation frequency poses a great design challenge.

Fig. 3.2.9 1-Bit $\Sigma\Delta$ Frequency Domain ADC Configuration[53]

3.3 Proposed New Flash ADC Structure

The ADC conversion time (including sample and hold circuit delay time), digital compensator computation time and DPWM delay time limited the obtainable small signal bandwidth of the digitally controlled DC-DC converter, which in turn limits the response of the digital DC-DC converter in the event of a sharp voltage change due to load transient.

Due to the ability of the digital control in switching into different complex mathematical computation, it is therefore well suited for multimode system. For example, during the normal operation when the load current does not change much, the control is by a linear Proportional-Integral-Derivative (PID) controller. When there is load transient, the system changes to non-linear control in order to obtain the optimal response. One of such non-linear control method is the charge balance control (also known as time optimal control) [64].

For this kind of control method, it is important to determine the voltage

profile during the load transient in the shortest possible time. To address this issue, multi-sampling or sampling at higher frequency can be used with the penalty of higher switching loss. Another approach is to use asynchronous ADC to detect the output voltage change in continuous time. When the output voltage changes due to a sudden load current transient, and if the quantized output voltage error exceeds a certain preset threshold, the transient control loop will bypass the normal PID control loop and enter a certain non-linear control loop, which brings the output voltage back to the nominal value in the shortest possible time. To be able to do this, a low power asynchronous ADC is required[99].

The traditional types of ADC like SAR, two-step or those ADCs that require more than one clock cycle to compute, are not suitable to implement the fast load transient recovery algorithm because the conversion latency will cause the output to go out of the acceptable range before the controller can react and bring the output voltage back to regulation. Another drawback is that the input needs to be stable during conversion for these types of ADCs, which requires sample and hold circuit.

To achieve high conversion speed, flash-type ADC is preferred. But traditional flash ADCs need large number of matched comparators, which are not suitable for this application [56]. One solution to this problem is to use inverters as analog comparators in the flash ADC, as discussed in Section 3.2.2, which is referred to as Threshold Inverter Quantization (TIQ) method [90, 100]. Inverters are basic building blocks in the digital system. TIQ inverters are specially designed to mimic the operation of analog comparators. The relative sizes of NMOS and PMOS transistors in TIQ inverters are usually different from standard inverters in the digital library. The switching point of the inverter, V_{SP} , is defined as the point

on the inverter transfer characteristics curve where the input voltage is equal to the output voltage. V_{SP} is determined by the relative sizes of the PMOS and NMOS transistors, as shown in Eqn. (3.3.2), where μ_x , W_x , L_x and V_{thx} refer to mobility, channel width, channel length and threshold voltage of NMOS and PMOS respectively. If the sizes are chosen properly, the switching points of the inverters can be used to quantize the input voltage of the inverter.

$$V_{SP} = \frac{k \times V_{th,n} + (VDD - V_{th,p})}{k + 1}, \text{ where } k = \sqrt{\frac{\mu_n \times W_n \times L_p}{\mu_p \times W_p \times L_n}} \quad (3.3.2)$$

Figure 3.3.1(a) shows the voltage transfer characteristic of the inverter when the input voltage is swept from 0 V to the power supply voltage. It can be seen that the voltage transfer characteristic of the inverter closely resembles that of an analog comparator with the built-in threshold voltage at V_{SP} , as shown in Fig. 3.3.1(b).

Fig. 3.3.1 Inverter Is Equivalent to Comparator (a) Voltage Transfer Characteristic of Inverter; (b) Threshold of Inverter Used as Comparator Reference

As discussed in Section 3.2, TIQ ADC is low power and high speed. However, the drawback is that the threshold voltage changes with power supply voltage, temperature and process, and there is no correlation between the NMOS and PMOS threshold voltages. Using an accurately pre-regulated power supply for the inverters will improve the accuracy of the switching point. However, this approach will add significant complexity to the whole system. The variation of the switching point is not acceptable for DC-DC converter because the output of the DC-DC converter is required to be tightly regulated even with input voltage or temperature variations. The internal threshold of TIQ comparator cannot be easily trimmed because it involves the sizing adjustment of the MOS transistors. Yet another issue with TIQ comparator is that when input is close to the switching point, V_{SP} , there will be shoot through current in the inverter since both NMOS and PMOS are turned on at the same time.

In this section, the design of a new asynchronous ADC for the digitally controlled DC-DC converters by using logic gates and simple logic circuits is described. The new ADC structure is able to scale with the process advancement and it can function at low supply voltage. Dynamic referencing technique is

applied to reduce the shoot-through current. Simulation and experiment results confirms the functionality of the proposed ADC structure. It should be pointed out that the new structure still requires resistor divider string to operate, which is not required by conventional TIQ converter. One benefit of the added resistor divider is that now it is possible to trim the threshold of individual logic-gate comparator.

The new proposed flash ADC is as shown in Fig. 3.3.2. In the proposed structure, the power supply node of the NOR gate is used as one input of the comparator, which is connected to the output of DC-DC converter, while the scaled reference voltage is connected to one of the usual inputs of the NOR gate. V_{REF} is the reference voltage in the system, usually from band gap reference circuit. In this configuration, the NOR gate functions as a comparator to determine the error voltage between the reference voltage and the sensed DC-DC converter output. By feeding back the output of NOR gate with lower reference voltage, only one NOR gate will be potentially exposed to the shoot-through current (more details in next section).

The dynamic and static current consumption of the logic gates are drawn directly from the DC-DC converter output. This eliminates the need of a pre-regulated voltage buffer as in the TIQ case. Moreover, as the buck converter configuration is most widely used for portable applications, drawing current from the output of the DC-DC converter reduces the effective current consumption by the input to output ratio. For example, if the DC-DC converter is converting a 3.3V input voltage to 1.8V output, the effective current drawn by the logic gate comparators is reduced by about 1.83 times.

Similar to delay-line based ADC in Fig. 3.2.1, the proposed ADC will draw current from the analog input. In this context, analog input is the DC-DC converter

output. This indeed increases the DC-DC output load current slightly. For structure like Fig 3.2.8, which uses differential pair such that it does not load DC-DC output, the bias currents of the comparators are from VDD. From efficiency point of view, this is worse than drawing current from DC-DC output since VDD usually has higher voltage for buck configuration. To improve the efficiency at light load (μA) range, the technique discussed in Chapter 6 is effective.

Fig. 3.3.2 Proposed New Flash ADC Structure Using NOR Gate as Comparator.

3.4 Block Circuit Design of the New Flash ADC

In this section, the design of the functional blocks in the proposed ADC structure is described, namely comparator, boost stage, and encoder. The circuit is designed based on 0.35 μm CMOS process with two poly layers and three metal layers. The complete ADC circuit is as shown in Fig. 3.4.1.

(a)

Fig. 3.4.1 Cadence Schematic of the Proposed ADC: (a) over view, (b) zoom-in to show comparator, buffer and zero detector connections, and (c) Encoder zoom-in

A. Comparator

In the conventional TIQ ADC, the output of DC-DC varies within a narrow range, which is possible to operate a few adjacent logic gates at shoot-through condition since both PMOS and NMOS are on. To reduce the current consumption, NOR gates are used here instead of inverters. If the sensed voltage is lower than the voltage required to make the output of certain NOR gate to be high, it will be lower than the voltage required to make the output of all the NOR gates above this NOR gate to be high. Hence, the output voltages of all the NOR gates above this NOR gate are

set to be low.

Referring to Figure 3.3.2, if the output of NOR gate, NOR[0], is low, then $V_{REF}[0]$ is of logic high. Since $V_{REF}[1]$ to $V_{REF}[N-1]$ are all higher than $V_{REF}[0]$, they should be logic high as well. In the proposed structure, A[0] sets NOR[1] output to be low, and A[1] sets NOR[2] output to be low, and so on. In this way all NOR gates above NOR[0] have logic low output. Same operation applies to NOR[1] to NOR[N-2]. If the signal A[k-1] from the below NOR gate NOR[k-1] is high, then the output of NOR[k] is set to low. If A[k-1] is low, then the output of NOR[k] depends on the logic level of $V_{REF}[k]$.

The output of the NOR gate comparator depends on the output of the NOR gate comparator with a lower reference voltage, hence this method is called dynamic voltage referencing. By doing this, the static current consumption is reduced to one NOR comparator only. This method also effectively removes the bubble error.

1) Offset analysis:

Since the logic gates use the minimum length in the particular process, the tolerance of the switching point due to process variation needs to be considered. In this design, the switching point is fixed by the resistor ladder, so re-arranging (3.3.2) for the quantization levels:

$$V_{IN}[n] = (k+1) \times V_{SP}[n] - k \times V_{th,n} + V_{th,p},$$

$$\text{where } k = \sqrt{\frac{\mu_n \times W_n \times L_p}{\mu_p \times W_p \times L_n}} \quad (3.3.3)$$

The relative tolerance between the resistors is usually quite small and is ignored here. The offset is mainly attributed to the tolerance in the

threshold voltages of NMOS and PMOS, which are determined by the sizes of the transistors as well as the process parameters as shown in (3.3.4), where X_{VT} is process dependent parameter corresponding to 1 sigma (σ) variation for the threshold voltage.

$$\sigma_{vth} = \frac{X_{VT}}{\sqrt{w \times l}} \quad (3.3.4)$$

From (3.3.3) and (3.3.4), the 1σ variation of the quantization level is:

$$\sigma_{VDD} = k \cdot \sigma_{vth,n} + \sigma_{vth,p} \quad (3.3.5)$$

For the process we use in this design, the 1σ variation of the quantization level is 33.7 mV which is about 1.5 LSB. Simple digital calibration technique as in [101] can be utilized to trim the variation in the quantization level to be less than 1/3 LSB. In [101], the resistor corresponding to 1 LSB has been divided into 3 sections. Each section corresponds to 1/3 LSB and has its own tap. During calibration, the input to the comparator under calibration is set at target value, while its reference is switched within different taps in its calibration range. At the same time, the comparator output is monitored by a digital accumulator circuit. If the offset is zero, the digital accumulator circuit will have zero output. If the output of the digital accumulator is not zero, the reference will move to other taps accordingly to drive the accumulator output to be zero. In this way, the offset of the comparator after calibration will be bounded by [-1/3 LSB, 1/3 LSB].

The threshold of NOR gate comparator needs to be trimmed to guarantee the specified accuracy for mass production. The trimming range is

determined by process corners and Monte-Carlo model to cover process variations and achieve the targeted yield.

To illustrate the variations of the NOR gate comparator's threshold, it has been redesigned using standard 0.18 μm CMOS process. Monte-Carlo simulations (300 runs with process and mismatch) have been performed to find out the distribution of the threshold voltages, when the comparator is used at the top, middle, and bottom of the conversion range. The code transition voltages are defined as V_{top} (1.936V), V_{mid} (1.8V), and V_{bot} (1.618V) respectively. Monte-Carlo simulation results are presented as histogram diagrams, and shown in Fig. 3.4.2 (a), (b) and (c) respectively. Maximum standard deviation at V_{top} is 27.1785 mV, or about 1.2 LSB.

B. Boost Stage

The boost stage consists of two inverters. The main function is to make sharp transitions between the logic zero and the logic one level. One thing to take note is that the logic high level is the same as the sensed DC-DC output voltage level in this stage. The output of the boost stages are in the thermometer code format.

C. Encoder

The encoder converts the thermometer code to binary logic output. It mainly consists of zero/one detector and a ROM structure. The ROM structure also functions as a level shifter to convert the logic high level from the sensed DC-DC output voltage level to the power supply voltage of the compensator block for subsequent duty cycle calculation.

(a)

(b)

(c)

Fig. 3.4.2 Monte Carlo simulation showing the distribution of threshold voltages, with nominal threshold at (a) 1.936 V; (b) 1.8 V and (c) 1.618 V.

3.5 Simulation Result of the New Flash ADC

The above described system is designed and simulated in transistor level by using Cadence Spectre simulation tool. The simulation result is summarized as shown in TABLE 3.5.1.

TABLE 3.5.1 ADC Simulation Result Summary

Number of Bits	4
Technology	CMOS, 0.35 μm
Supply voltage	3.3 V
Output voltage	1.8 V
LSB voltage	22.5 mV
INL/DNL	0.49/0.29 LSB
“Window” range	1.618 V ~ 1.936 V
Static current from the power supply at zero error	63 μA
Static current consumption from the input at zero error	93 μA
Maximum conversion delay	12.55 ns

Fig. 3.5.1 shows the ADC output voltage when the input to the ADC is swept from 0V to 3.3V. It can be seen that when the input voltage is below the “window” range, all the out bits of the ADC are logic low, while when the input range is above the “window” range, all the bits are logic high. This is the desired operation for the windowed ADC.

Fig. 3.5.2 zooms into the range where the input voltage is within the conversion window, which shows the proper operation of the proposed ADC.

Fig. 3.5.1 Operation of the Proposed ADC with DC Sweep (Full Range)

Fig. 3.5.2 Operation of the Proposed ADC with DC Sweep (Window)

Fig. 3.5.3 shows the transient result when the input is swept from 1.6 V to 2 V in 80 ns. It can be seen that the ADC functions properly without missing code.

Fig. 3.5.3 Simulation Result of the 4-Bit ADC Operating at Transient Input

Fig. 3.5.4 shows the non-linearity result. The INL and DNL are both less than 0.5 LSB. A slight bowing effect due to the resistor divider is observed. This can be improved by impedance matching method [102]. For each comparator, the impedance looking into the resistor divider is different. Hence the input capacitance at each comparator results in different delay during the conversion. By inserting different value of resistor in-between the input of the comparator and resistor divider according to the tap point, it is possible to match the impedance that each comparator sees. As a result, all comparators have equal delay at the input, as shown in [102].

The above simulation result is obtained when the length of the NOR gate comparator is minimum at 0.35 μm . The length of the NOR gate is another important design parameter. By using smaller length, the response time of the logic gate is fast since the driving ability of the transistor increases while the parasitic

capacitance reduces. However, the static current consumption is also increased when the input voltage is near to the switching point.

(a)

(b)

Fig. 3.5.4 Non-Linearity Result (a) Code Transition Voltage Vs. Output Digital Code, (b) INL/DNL Result.

Fig. 3.5.5 shows the simulation result of the conversion time and static current consumption when the length of the NOR gate comparator varies. Compromise can be made between the conversion time and power consumption by changing the

length of the NOR gate, which provides another design degree of freedom.

Fig. 3.5.5 Effect of Gate Length to Conversion Time and Static Current Consumption

From Fig. 3.5.5, the conversion time increases almost linearly with transistor length, while the rate at which static current goes down become slower when transistor length becomes longer. The conversion time / static current pair can be selected depends on the system requirement. However, it does raise a concern that when the length becomes smaller, the conversion speed becomes faster at the expense of higher current consumption, which may prevent the structure taking the full advantage of the most advanced process. Hence, voltage scaling is necessary when this structure is used in order to put current consumption under control. Scaling V_{REF} and V_{IN} will reduce gate over-drive of the transistors in the NOR gate, which results in reduction in speed. Hence, when a new process is used, the proposed structure needs to be characterized to find the best trade-off between static current and conversion time.

3.6 Layout Design of the New Flash ADC

The layout of the ADC is as shown in Fig. 3.6.1. Cross-coupling has been done on resistor ladder to improve the relative matching of the resistors. The matching among the comparators affects the nonlinearities of the ADC. In this design, the comparators are just put side by side without special matching techniques. All other parts of the ADC are not sensitive to matching and are floor-planned to reduce interconnect length among blocks.

Fig. 3.6.1 Layout of the Proposed ADC

The total active area is measured to be 0.034mm^2 . The reference generator block, which consists of the poly resistor dividers to provide the reference for each comparator, takes about 0.009mm^2 . The comparator and boost stage takes about 0.012mm^2 . Zero detector blocks takes about 0.01mm^2 . The encoder block takes about 0.002mm^2 . The rest of the area is occupied by routings.

In the proposed structure, boost, 0 detector and encoder blocks are digital circuits, which are relatively insensitive to process variations. However, just like other digital circuits, the operating speed of the above circuits is affected by process corners as well as layout parasitic. A post-layout RC extraction has been done to derive the parasitic resistances and capacitances from the layout routings and coupling between different layers. Simulations have been run to check the

signal path delays from input to output, together with the extracted parasitic and process corner models, assuming the thresholds of the NOR gate comparators have been trimmed properly, as discussed in Section 3.4 (A). Table 3.6.1 below summarizes the results. From the result, the worst case delay of 28.37 ns happens at SS corner and Vbot crossing case.

TABLE 3.6.1 Signal path delay post-layout simulation results with process corners

Process corner	Vbot crossing delay, ns	Vmid crossing delay, ns	Vtop crossing delay, ns
Typ	12.89	8.741	6.88
FF	6.407	5.066	4.298
FS	11.99	8.148	6.489
SF	14.81	9.433	8.01
SS	28.37	18.07	13.55

3.7 Measurement Result

A test chip with the proposed flash ADC has been built by using TSMC 0.35 μm 2-Poly-3-Metal CMOS process to verify the operation. Fig. 3.7.1 shows the evaluation board for the test chip. The reference voltage during the evaluation is externally supplied and the value is 1.2V.

Fig. 3.7.1 Evaluation Board of ADC Test Chip

Fig. 3.7.2(a) shows the measured transition voltage corresponding to digital codes, which is close to simulated value in Fig. 3.5.4(a). The measured non-linearity result is shown in Fig. 3.7.2(b). DNL is between -0.73 LSB and 0.72 LSB, while INL is between -0.7 LSB and 0.64 LSB. Comparing with the simulation result in Fig. 3.5.4 (b), both DNL and INL become worse. The reason could be due to the random offset of transistors in NOR gates, which causing variations in switching point voltage. Since the test chip does not have trim

function, the switching point's variation is relatively large.

To measure the conversion time, a square wave with 1 MHz frequency is applied to the input of the ADC with voltage between 0.4V and 3V. The output of ADC is as shown in Fig. 3.7.3. The conversion time from lowest code to highest code is about 20 ns when the input is sweeping from low to high and 15 ns when the input sweeping from high to low. The difference in conversion time is due to the ROM type encoder has a stronger pull-down capability than pull-up. In a separate measurement, the delay of output buffer (to drive the pad capacitance) is about 5 ns.

Fig. 3.7.4 shows the ADC outputs when a ramp signal applied which crosses the conversion range in about 1.5 μ s. As seen from Fig. 3.7.4 (a) and (b), the output of ADC has no missing code. However, due to the random offset, the bit-widths are not equal, as discussed before. The zero error bit determines the accuracy of DC-DC output, hence it should be trimmed by fine-tuning the resistor ladder. For bits other than the zero error bit, they are used to determine the output during transient, hence the accuracy requirement is not so stringent. Nevertheless, there should be no missing code and the output should be monotonic for transient recovery algorithm to function properly.

(a)

(b)

Fig. 3.7.2 Measured DC Non-Linearity Result: (a) Code Transition Voltage vs. Output Digital Code, (b) INL/DNL Result.

(a)

(b)

(c)

Fig. 3.7.3 Measured ADC Output with Step Input (Ch1: Input; Ch2: D0; Ch3:D1;Ch4:D3):
 (a) Overall Result, (b) Zoom-in of Rising Edge, (c) Zoom-in of Falling Edge.

(a)

(b)

Fig. 3.7.4 Measured ADC Output with Ramp Input (Ch1: D0; Ch2: D1; Ch3:D2;Ch4:D3):
(a) Ramping Up; (b) Ramping Down

TABLE 3.7.1 compares the proposed flash ADC with the previously reported ADCs for digitally controlled DC-DC converter. Since the ADCs in this table are the structures used for digitally controlled DC-DC converter applications, many of them are windowed converters, which are different from normal full range ADCs.

Hence, they are compared by conversion time (affecting transient response), operating current (affecting system efficiency) and area (die cost). The current used for comparison is the total operating current, which includes V_{ref} current.

Generally speaking, flash type ADCs show much lower conversion time due to the fact that input voltage is digitized in parallel, which is essential for fast transient response. Major drawbacks of flash type ADCs include relatively higher current consumption and larger silicon area due to the parallel comparators.

From the table, it can be seen that the proposed flash ADC achieves fast conversion time with relatively low current and small chip area. Hence, the output voltage profile during the load transient can be detected to implement the fast load transient algorithm. Additionally, the proposed ADC is using standard logic gates only, which makes it very suitable for digitally controlled DC-DC converter. If a smaller geometry process is used, the total area of the proposed ADC can be scaled down accordingly.

3.8 Summary

In this chapter, one of the essential blocks for digitally controlled DC-DC converter, ADC, is investigated. The requirement of ADC has been analyzed in terms of accuracy, conversion time, power consumption and digital process compatibility. Literature review has been conducted on the reported ADC structures used for digital controlled DC-DC converter, with their advantages and disadvantages identified. A new flash ADC based on modified TIQ method is proposed. NOR gates replace comparators in the conventional flash ADC converter. Dynamic voltage referencing is used to reduce shoot-through current in the conventional TIQ ADCs.

The design details of all the functional blocks are described. The proposed ADC is designed and fabricated using available 0.35 μm CMOS process. Simulation result and experiment result demonstrate the performance of the proposed ADC, which is shown to be suitable for the target application.

During measurement, it has been found that the random offset of the NOR gates has profound impact on the code transition levels and non-linearity. To achieve required DC accuracy, the zero error bit needs to be trimmed. And the variation of other bits should be smaller than the targeted LSB to ensure monotonicity and no missing codes, such that load transient recovery algorithm can be applied.

TABLE 3.7.1 Comparison with Reported ADCs for Digitally Controlled DC-DC Converter

Author	Year	Topology	No. of Bit	LSB (mV)	Supply	Current	Conversion time	Process	Area (mm ²)
Patella [68]	2003	Delay line	3	40	2.7V	10 μ A	~1 μ S	0.5 μ m	0.2
Chan [96]	2008	Delay line	4	50	3V	-	250nS	0.35 μ m	0.28
Saggini [90]	2008	TIQ	6	3.7	3.3V	-	~50nS	0.35 μ m	0.3
Soenen [98]	2010	$\Delta\Sigma$	5	5	1.1V	360 μ A (with DAC)	320nS	40nm	0.05
Ahmad [53]	2010	Frequency domain	8	28	3.3V	220 μ A	62.5nS	0.18 μ m	0.08
Radic [103]	2010	Track and hold	5	4	1.8	240 μ A	15nS	0.18 μ m	0.023
Lan [70]	2010	Delay line	N.A.	10	3.3V	200 μ A	N.A	0.18 μ m	0.03
Kuttner [4]	2011	Flash	4	7.5	1.8V	40 μ A	83nS	28nm	N.A
Lan [97]	2013	Delay line	3	18	2.7	10 μ A@44K Hz	-	0.18 μ m	0.045
This work		Flash	4	22.5	3.3V	113μA	15nS	0.35μm	0.034

Chapter 4 Load Transient Response Improvement

In this chapter, the transient response of DC-DC converter is investigated. There are mainly three types of transient conditions that a DC-DC converter needs to respond to: load transient, reference tracking and line transient.

Load transient refers to the condition that the current drawn from the output of DC-DC converter changes in value in relatively fast speed. The current drawn by digital ICs connected to the output of DC-DC converter is very dynamic. The drawn current could increase in value, which usually results in a voltage undershoot due to the fact that the inductor current takes time to build up; or decrease in value, which usually results in a voltage overshoot due to the fact that the inductor current takes time to discharge. Since the power supply voltage to the digital ICs using advanced process node continues to drop, the tolerable voltage variation range in the power supply also becomes narrower [5, 104]. Undershoot and overshoot need to be small enough such that the digital ICs at the load can function properly. The load transient response is closely related to the rate of change in load current and external inductor/capacitor value. Faster load current change usually results in larger deviation from the nominal output voltage. Larger inductor value makes the current ramping slower, which causes more current excess/deficit during load transient. Smaller capacitor will show larger voltage deviation for the same amount of charge change. The load transient response of the DC-DC converter output voltage can generally be improved by using more filter capacitors at the output at the cost of larger PCB area and higher bill-of-material (BOM) cost, neither of which is welcomed in the portable equipment. Hence it is desirable to explore the circuit techniques and control methods to improve the load transient response of the DC-DC converter.

Reference tracking refers to the condition that the reference voltage to the DC-DC converter changes so as to change the output voltage to a value desired by the load [105-108]. This is important for systems employing DVS to optimize the overall efficiency. With DVS, power supply voltage to the digital block is dynamically changed based on operation mode required: high voltage for active mode and low voltage for standby or data retention mode. Power gating is also often used to shut off the unused block. During reference tracking, the optimum on-time and off-time which could bring the output to the new value within one switching cycle are derived in Appendix A. An implementation using LUT is also discussed.

Line transient refers to the condition that the power supply to the DC-DC converter changes value in short time. This could be induced by sudden increase in current drawn by other loads that share the same power supply with the DC-DC converter. Since the power supply usually has limited source impedance, the voltage appears on the DC-DC converter supply may see voltage level change in short time. Line transient is commonly dealt with by providing the input information into the voltage control loop. This is usually not a problem for AOT control, since when the switching cycle starts, the on-time changes with input voltage on the fly. For voltage mode control, line transient is handled by feed-forward method.

This chapter focuses on the improvement of load transient response. In this section, the optimum load transient recovery is derived first using the approach reported in [109]; which is followed by the literature review of the reported load transient reduction techniques. After that, a new level based load transient recovery algorithm is proposed to achieve fast voltage recovery. This technique can be used

to DC-DC converters with both PWM control and ripple-based control. Next, unloading transient response improvement to digital adaptive on-time (DAOT) control by using body brake is presented, together with the algorithm that makes sure that the body brake will not be applied during normal operation.

4.1 Optimum Load Transient Recovery

A general buck converter structure has been shown in Fig. 4.1.1, with all the parasitic of the output L/C filter shown. R_{dc} is the equivalent DC resistance of the inductor L . L_{es} and R_{es} are the equivalent inductance and resistance of the capacitor C , respectively.

Fig. 4.1.1 General Buck Converter Structure

Next, the load transient response of the buck converter is explained, as shown in Fig. 4.1.2. When the load current, I_{load} is constant, the current in the inductor $I_{inductor}$ is centered around I_{load} with current ripple, as shown between t_0 and t_1 in Fig. 4.1.2. When the load current is stepping up from I_1 to I_2 during the time interval of t_1

to t_2 , the control loop cannot respond immediately to increase the duty cycle, hence, the deficit of the current is supplied by the output capacitor. The increase of capacitor current through the equivalent inductance L_{es} causes an instant voltage drop of V_1 at t_1 , where

$$V_1 = L_{es} \times \frac{di}{dt} = L_{es} \times \frac{I_2 - I_1}{t_2 - t_1} \quad (4.1.1)$$

Fig. 4.1.2 Typical Load Transient Waveform

The down slope of the output voltage between t_1 and t_2 is determined by the output current slope and the equivalent resistance of the output capacitor, R_{es} .

$$\frac{dV_{1-2}}{dt} = R_{es} \times \frac{di}{dt} = R_{es} \times \frac{I_2 - I_1}{t_2 - t_1} \quad (4.1.2)$$

At t_2 , the load current settles at the new level of I_2 . Since the load current becomes constant, the current through the equivalent inductor L_{es} no longer increases. Hence, at t_2 , the output voltage goes up V_2 due to the effect of the

equivalent inductor, which is similar to V_1 in (4.1.1):

$$V_2 \approx V_1 = L_{es} \times \frac{di}{dt} = L_{es} \times \frac{I_2 - I_1}{t_2 - t_1} \quad (4.1.3)$$

Between t_2 and t_3 , the DC-DC control loop senses the drop in output voltage and starts to increase the duty cycle of the output stage. As a result, the inductor current starts to increase. Since during this interval, the inductor current is still less than the new load current, I_2 , the output capacitor continues to supply the difference between the inductor current and the load current. The output voltage continues to drop with the depletion of the output capacitor charge.

At t_3 , the inductor current is equal to the output current. The output capacitor stops discharging. At this point, the output voltage reaches the lowest value of the load transient process. Assuming the total charge that is depleted from the output capacitor is Q_c , the voltage drop can be calculated using the below equation:

$$V_3 = \frac{Q_c}{C} = \frac{\int_{t_1}^{t_3} (I_{load} - I_{inductor}) dt}{C} \quad (4.1.4)$$

The transient voltage deviation is largely determined by the output filters and the control loop robustness. To achieve minimum voltage deviation, the control loop should increase the duty cycle to 100% as soon as the load current starts to ramp up. Under this condition, the inductor current between t_1 and t_3 will become

$$I_{inductor, 1-3} = \frac{V_{in} - V_{out}}{L} \times (t - t_1) + I_1 \quad (4.1.5)$$

At t_3 , the inductor current is equal to the new load current I_2 . Hence

$$I_{inductor, 3} = \frac{V_{in} - V_{out}}{L} \times (t_3 - t_1) + I_1 = I_2 \quad (4.1.6)$$

$$(t_3 - t_1)_{min} = \frac{(I_2 - I_1) \times L}{V_{in} - V_{out}} \quad (4.1.7)$$

The minimum total charge that is depleted from the output capacitor between

t_1 and t_3 , $(Q_c)_{\min}$, can be calculated:

$$(Q_c)_{\min} = \frac{1}{2} \times (I_2 - I_1) \times (t_3 - t_1)_{\min} \quad (4.1.8)$$

By substituting (4.1.7) to (4.1.8),

$$(Q_c)_{\min} = \frac{1}{2} \times (I_2 - I_1) \times \frac{(I_2 - I_1) \times L}{V_{in} - V_{out}} = \frac{1}{2} \times \frac{(I_2 - I_1)^2 \times L}{V_{in} - V_{out}} \quad (4.1.9)$$

By substituting (4.1.9) to (4.1.4), the minimum achievable voltage deviation can be calculated.

$$(V_3)_{\min} = \frac{(Q_c)_{\min}}{C} = \frac{1}{2} \times \frac{(I_2 - I_1)^2}{(V_{in} - V_{out})} \times \frac{L}{C} \quad (4.1.10)$$

When the load current changes from heavy to light, the load transient process is similar. By performing the same analysis, the minimum achievable voltage overshoot can be calculated.

$$(V)_{\min,up} = \frac{1}{2} \times \frac{(I_2 - I_1)^2}{V_{out}} \times \frac{L}{C} \quad (4.1.11)$$

From the above analysis, it can be seen that the physical limit of the achievable smallest deviation is determined by the external inductor and capacitor. The inductor should have smallest possible inductance; hence, the current of the inductor can rise up with the fastest slope. And the capacitor should have largest possible value so that it can hold the output voltage when the inductor current is smaller than the load current. However, the inductor value cannot be reduced too much, otherwise the static output ripple voltage will increase as the inductor ripple current increases. And the capacitor value cannot increase too much either, since that will incur larger PCB area and BOM cost.

4.2 Reported Load Transient Recovery Method

One assumption that was made in the derivation of the minimum achievable voltage deviation is that the output stage reaches 100% duty as soon as the output current is ramping up. In actual situation, there are associated delays before the output stage can reach 100% duty. Linearly-controlled DC-DC converters usually ensures stability and robustness over wide operating ranges by using a PID controller based on small-signal models of the converter [110]. During step load transient, the output of the DC-DC converter is often out of the range where the small-signal assumption is valid. The response to such a large-signal event is limited by the system control bandwidth. For example, a closed-loop bandwidth of 10 kHz limits the system response to step load current to about 1 ms [98].

Recently, extensive researches have been conducted to improve the dynamic response of the DC-DC converters based on non-linear control methods. Non-linear control opens the possibility to overcome the bandwidth limitation of the conventional linear control and improve the dynamic response of the DC-DC converter.

The majority of the non-linear control methods are based on boundary control theory [111, 112]. In boundary control, the DC-DC system is modeled as a time-varying system that can operate in two distinct circuit topologies. The converter state-space equations are then used to derive the state-plane trajectories. Selection of the switching surface is essential to make the state trajectory converge to the regulation point after external disturbance [113]. In [114], boundary control has been implemented in voltage regulation modules (VRMs) to achieve fast transient response.

Charge balance control, also known as time optimal control, is a non-linear control method, aiming to drive a converter to steady state in the shortest time possible [9]. Charge balance control can be viewed as a special form of boundary control [113].

It is observed that when the load current changes, the inductor current cannot keep up with the load current change, hence the charge in the output capacitor will compensate for the difference between the two. As a result, DC-DC converter output voltage is changed. Charge balance control recovers the output capacitor charge by a single switching cycle starting at a precise moment [99, 115-118], as shown in Fig. 4.2.1. The value of t_{up} and t_{down} are derived based on the graphical method to make the net charge to the output capacitor to become zero, implying the recovery of the output voltage.

Fig. 4.2.1 Charge Balance Controller Response to Load Current Increase [64]

Due to the complex calculation involved, analog implementation of the charge balance control is difficult due to circuit complexity and power consumption. On the other hand, calculation in digital domain is much easier than

in analog domain; together with the use of LUT, the implementation in digital domain is more feasible.

In theory, the charge balance control is the optimum transient recovery method and quite a few experiment results have been reported[99, 115-118]. However, this method does not find very wide adoption in the industry because of its drawbacks. Charge balance control is usually sensitive to the variation of external component values, e.g. inductor value. For digital controller, it is difficult to detect the voltage change in short time without ADC sampling delay, which will affect the achievable performance of the optimal control. Another issue with this control method is that during the transient recovery, the switching frequency is changed; hence it will produce unexpected EMI if the load transient occurrence is frequent. Yet another issue is that this method assumes the inductor current can go up without limit, which is not the case in practical converter[113]. The mode transition between the normal PID control and charge balance control may cause instability when consecutive load steps happened [103].

To overcome load transient response limitation defined by (4.1.10) and (4.1.11), a few methods have been suggested. One method is to implement additional power switches to increase the voltage across the inductor during transients, thus increasing the inductor current slope [119, 120]. The improvement of transient response by using this method is limited by the converter's input and output voltages. And additional switch reduces the power efficiency at the steady state. Another reported method involves adding auxiliary phase at the output of the DC-DC converter, consisting of smaller switches and inductor [121, 122]. The auxiliary phase is only active during the load transient to speed up the recovery and is turned off during normal operation. Hence, the efficiency is not affected. The

drawback of the second method is that additional switches and inductor increase the total cost of the system. Yet another method is to connect additional push-pull switches directly at the output of DC-DC converter to provide additional current during transient [89], with the drawbacks of additional silicon area and challenge in controlling the precise turn on/off time of the additional switches such that the normal operation is not affected.

4.3 Proposed Level-Based Load Transient Recovery Method

A new transient recovery algorithm with much less complexity is proposed here to achieve fast transient response for DC-DC converter with multiple operating modes. Fig. 4.3.1 shows a multi-mode DC-DC converter with two control loops: DPWM and digital pulse-frequency-modulation (DPFM) control, while Fig. 4.3.2 shows a converter with DAOT control. The transient recovery algorithm developed in this section can be applied to both systems. The following description is based on DPWM / DPFM control, while it can be easily extend to the DAOT control.

Fig. 4.3.1 Multi-Mode DC-DC Converter with DPWM/DPFM Control

Fig. 4.3.2 Multi-Mode DC-DC Converter with DAOT Control

As shown in Fig. 4.3.1, when the load current is stable, the system operates in either DPWM mode or DPFM mode, depending on the load condition. To ensure accurate voltage regulation and control loop robustness, conventional linear control loop consists of ADC, discrete compensator, and DPWM/DPFM is used. When the output voltage change due to load current transient is detected, the transient recovery loop takes over the output stage control from linear loop and tries to recover the output voltage at the shortest possible time. At the same time, the discrete PID compensator and DPWM continue to operate and calculate the duty cycle based on linear control. However, the output of the DPWM is not passed to the driver stage. Since load transient recovery time is usually very short, the power loss due to the continuous operation of linear loop has negligible impact on the overall efficiency. Another method is to calculate and set DPWM output to optimum value after load transient, which requires extra circuits.

Based on the analysis in section 4.2, the transient recovery loop should turn the PMOS transistor fully on to achieve minimum voltage deviation when the load current steps up from low level to high level. The choice of the load transient detection point is important. If detection point is too near to the zero error bit, normal operation of PID control may be affected. The system may transit between

two operation modes unnecessarily. Another necessary consideration is about the equivalent inductance of the output capacitor, L_{ES} . The effect of L_{ES} on output voltage during load transient is that it causes V_1 and V_2 step in Fig. 4.1.2, of which the values are calculated in (4.1.3). The load transient detection point needs to be lower than the first valley voltage level at t_2 to avoid being mis-triggered. If the detection point is too far from the zero error bit, the delay in entering the transient recovery mode may cause the output deviation becomes large. To balance these two considerations, the second error bits (up and down) are chosen. Hence, when the error voltage falls between $[-2V_q, +2V_q]$, where V_q is the ADC LSB voltage, linear control is effective; when the error voltage is more than $+2V_q$ or less than $-2V_q$, the transient recovery loop is effective. The threshold can be made adjustable if all the error bits transition can be monitored, which is possible in flash type ADCs.

After the transient detection point is crossed, the system enters transient recovery mode. In the case when the load current is stepped up, the PMOS transistor is fully turned on. The current in the inductor will go up linearly with the slope of $(V_{in}-V_{out})/L$. When the current in the inductor reaches the new output current level, the minimum voltage deviation in the output capacitor is reached as shown at t_3 in Fig. 4.3.3.

Fig. 4.3.3 Excess Energy (Shaded Area) Causes Output Overshoot

After that, to compensate the loss of capacitor charges, the inductor current needs to continue to increase. However, if the inductor current increases till the output voltage is fully recovered to zero-error-bit, the excess energy in the inductor will cause the output voltage to overshoot, as shown in Fig. 4.3.3. Hence, the transient control loop should return the control to linear control loop after the voltage valley point is reached and before the output voltage goes back to the zero-error-bit, which is between t_3 and t_4 as shown in Fig. 4.3.3.

For charge balance control shown in Fig. 4.2.1, the inductor current may go to very high value at calculated switching point, causing reliability concern. Over current protection needs to be disabled here to make sure calculated t_{up} and t_{down} still correct. For the proposed approach, since output voltage level is detected to determine on/off timing, it is able to work with the over current protection circuit enabled. Since the new output current level should always be less than over current limit threshold, the inductor current can only reach over current limit threshold

after t_3 . Hence, the valley point is not affected. However, if over current limit is triggered between t_3 and t_4 , the recovery time to get back the normal output voltage will be longer.

The valley point during the load transient can be determined by monitoring the outputs of the comparators in ADC block. During load-step, V_{out} first drops and then recovers after reaching the valley point, as shown in Fig. 4.3.4. V_q is the error voltage bit width and $(V_{ref} - x \cdot V_q)$ is the reference voltage of x th comparator while $(Comp, -x)$ denotes its output. When V_{out} is higher than the comparator reference, the output of that comparator is high, and vice versa. It can be observed that the first comparator output that goes from low to high indicates that the valley point is between the reference voltage of this comparator and the one below it. In Fig. 4.3.4, the valley point is between $(V_{ref} - n \cdot V_q)$ and $(V_{ref} - (n+1) \cdot V_q)$. Similarly, during unloading, the peak point can be determined using the same method, by monitoring the first comparator whose output goes from high to low.

Fig. 4.3.4 Determination of Valley Point during Load Step

Next, the mode transition bit at which the mode should be returned to linear control is determined. The optimum transition point will depend on the system

parameters and bandwidth of the linear control loop. In the proposed method, the middle point between the valley error bit and zero error bit is used as the mode transition point. For example, if the valley error bit happens between $(V_{ref} - 7 \cdot V_q)$ and $(V_{ref} - 6 \cdot V_q)$, the mode transition point is chosen at $(V_{ref} - 3 \cdot V_q)$ which is at the center between the valley error bit and zero error bit.

To implement the proposed method, three important output voltage points are necessary: namely transient detection point, valley/peak point, and mode transition point. Out of these three points, transient detection point is the most important in term of detection delay, since the delay in making the system enter transient recovery mode will result in further depletion of the output capacitor. For DAOT control, since the switching cycle starts when the output voltage is lower than the zero error bit, it does not need to determine transient detection point. The valley point is relatively more tolerate to detection delay, since it is only an intermediate state to determine the mode transition point. Finally, delay in mode transition point detection will affect the system response when returning to the linear control loop.

In digitally controlled DC-DC converter, the error voltage between the output and the reference is sensed and converted to digital code by an ADC. To implement the above load transient recovery method, it is important to determine the output voltage profile in an asynchronous basis. The ADC that is described in Chapter 3 is suitable for the proposed system.

To verify the operation of the proposed load transient recovery algorithm, a system simulation circuit has been constructed. The block diagram of controller (as in Fig. 4.1.1) is shown in Fig. 4.3.5.

Fig. 4.3.5 Transient Recovery Controller Block Diagram

The ADC in the system is using the new flash ADC described in chapter 3. (Comp,+8) to (Comp,-8) are the outputs of the 16 comparators in the 4-bit ADC. Compensator and DPWM blocks are modeled by Verilog-A. The compensator is based on PID control. It is implemented using the following control law derived from Backward Euler transformation:

$$D[n] = D[n-1] + E[n] \times (K_p + K_i + K_D) + E[n-1] \times (-K_p - 2 \times K_D) + E[n-2] \times K_D \quad (4.3.1)$$

PID compensation is to stabilize the control loop when the output is close to regulation. During load transient, the bandwidth of PID compensation limits the response time of the control loop, which results in large output change. Widen the control bandwidth of PID compensation loop helps to make the response faster, at the risk of reduced phase margin. By using a separate transient recovery loop, it is possible to optimize load transient and steady-state stability margin separately.

As discussed in above, (Comp, +2) and (Comp,-2) are used to determine mode transition point. Specifically, when (Comp,+2) changes from low to high, which indicates the output is higher than the target value by two error bits, the

system enters unloading recovery mode; when (Comp,-2) changes from high to low, which indicates the output is lower than the target value by two error bits, the system enters load-step recovery mode.

Under unloading recovery mode, duty cycle reduces to zero till the unloading mode transition point (the error bit at the center of peak error point during unloading recovery and zero error point) is reached. On the other hand, under load-step recovery mode, duty cycle increases to 100% till the load-step mode transition point (the error bit at the center of valley error point during load-step recovery and zero error point) is reached. After the mode transition points, the control is returned to linear control loop, consists of compensator and DPWM.

Based on the above discussion, transient recovery block as shown in Fig. 4.3.5 has been designed using standard logic gates. Fig. 4.3.6 shows the schematic.

Fig. 4.3.6 (a) shows the generation of "Tran_en" and "Duty_tran" signals. In normal operation, "Comp, -1" and "Comp, +1" toggle between high and low, which reset "Undershoot_recover" and "Undershoot_recover" to low respectively, hence "Tran_en" is low, and the system operates under linear loop control. When load-step occurs, if the output voltage dips to a value such that "Comp, -2" becomes low, "Undershoot_recover" is set to high, which makes "Tran_en" to be high - the system enters transient recovery mode. At the same time, "Duty_tran" signal becomes high, which makes duty cycle of the power stage to be 100%. This continues until "Mode_tran_down" signal goes high, indicating the system will return to linear loop control. When unloading occurs, the operation is similar, except that "Duty_tran" becomes low to operate the power stage at 0% duty.

Fig. 4.3.6 (b) and (c) show the generation of mode transition signals: "Mode_tran_down" for undershoot recovery due to load-step, and "Mode_tran_up"

for overshoot recovery due to unloading. Both signals are implemented in positive logic: when they are high, it means the respective load transient recovery is effective. Let's use the same example that the valley error bit happens between $(V_{ref} - 7 \cdot V_q)$ and $(V_{ref} - 6 \cdot V_q)$, hence "Comp, -7" is the last one going from high to low before the valley point is reached. When the output voltage recovers, "Comp, -7" will be the first going from low to high and latches the D-flipflop it connects to. When the output voltage continues to increase and "Comp, -4" (middle point between Comp, -7 and zero error bit) becomes low to high, "Mode_tran_down" is set to low and the transient recover operation is finished.

(a)

(b)

(c)

Fig. 4.3.6 Schematic of transient recovery block: a) generation of "Tran_en" and "Duty_tran"; b) generation of "Mode_tran_down" for undershoot recovery; and c) generation of "Mode_tran_up" for overshoot recovery

The important system parameters are shown in TABLE 4.3.1 below.

TABLE 4.3.1 Important System Parameters of Load Transient Simulation

Supply voltage	3.3 V
Output voltage	1.8 V
Maximum load current	500 mA
Output capacitor	4.7 μ F (ESR = 30 m Ω)
Output inductor	2.2 μ H (DCR = 10 m Ω)
Load transition time	0 $\leftrightarrow$ 500mA in 1 μ s

Load transient response is simulated with and without the transient recovery block. The simulation result is shown in Fig. 4.3.7 for heavy load to light load transition and Fig. 4.3.8 for light load to heavy load transition. From Fig. 4.3.7 and Fig. 4.3.8, it can be seen that the proposed load transient recovery algorithm can improve the transient response significantly. For heavy load to light load transition, the overshoot voltage is reduced from 290 mV to 96.8 mV, or 66% improvement. For light load to heavy load transition, the undershoot voltage is reduced from 282 mV to 93 mV, or 67% improvement. The settling time that the system after load transient also reduces.

Based on equation (4.1.10) and (4.1.11), the minimum achievable voltage deviation is:

$$(V)_{\min,up} = \frac{1}{2} \times \frac{(I_2 - I_1)^2}{V_{out}} \times \frac{L}{C} = 32.5mV \quad (4.3.2)$$

$$(V)_{\min,down} = \frac{1}{2} \times \frac{(I_2 - I_1)^2}{(V_{in} - V_{out})} \times \frac{L}{C} = 39mV \quad (4.3.3)$$

(a) Heavy load to light load transient response, without transient recovery block: overshoot voltage is 290.3 mV.

(b) Heavy load to light load transient response, with transient recovery block: overshoot voltage 96.8 mV.

Fig. 4.3.7 Simulated Unloading Transient Response: (a) Without Transient Recovery Block; (b) With Transient Recovery Block

(a) Light load to heavy load transient response, without transient recovery block: undershoot voltage is 282mV.

(b) Light load to heavy load transient response, with transient recovery block: undershoot voltage is 93mV.

Fig. 4.3.8 Simulated Load-step Transient Response: (a) Without Transient Recovery Block; (b) With Transient Recovery Block

Since the proposed method using $2V_q$ as transient detection point, the minimum achievable voltage deviation is: $32.5\text{mV} + 2 \times 22.5\text{mV} = 75.5\text{mV}$ for heavy load to light load transient and $39\text{mV} + 2 \times 22.5\text{mV} = 84\text{mV}$ for light load to heavy load transient. The simulation result shows that the voltage deviation is near to the minimum achievable value.

However, it is also observed that the transition from transition recovery mode to linear control mode is not optimum. Some bumpiness can be observed when the system transiting from the transient recovery mode to linear control mode. For the case of light load to heavy load transition, the system entered transient recovery twice before finally settled down (Fig. 4.3.8(b)). Because the second dipping is less than the first dipping, near minimum achievable value is achieved.

The main reason of the non-optimum transition is due to the phase difference between the inductor current and capacitor voltage and delay in linear control mode. In the buck DC-DC converter, the inductor current is always leading the capacitor voltage. The proposed load transient recovery algorithm is based on voltage detection, which may over-charge the inductor current when recovering the capacitor voltage. For DC-DC converters with different inductor and capacitor combination, the optimum mode transition point can be different. The other reason is due to the delay in linear control mode. The load transient recovery algorithm is much faster than the linear control mode. Hence, when the load transient recovery algorithm returns the loop control to the linear control mode, the linear control mode tends to give delayed duty signal since it determines the duty cycle based on previous duty cycles.

With variation in temperature and component aging, the proposed approach is still able to minimize the voltage dip since the duty cycle is kept at 100% after the

valley point is achieved. However, the optimum mode transition point may change with the operating conditions. The choice of mode transition point does not affect the valley point, however, it does affect the transition from non-linear control to linear control. Since there are limited number of points to choose from, one possible solution to ensure stable transitions is to use look-up-table (LUT) method. Through simulation or measurement, the optimum transition point for given valley point is determined and programmed to LUT. During load transient, when certain valley point is reached, the corresponding mode transition point can be read from LUT and applied. And multiple LUTs can be used for different operating conditions, at the expense of increased silicon area.

For given DC-DC converter design, L/C nominal values are usually known. The variations over temperature and time are normally available from the manufacturer. If exact values of L/C are needed, real time component measurement techniques can be used, which is not being investigated in this research work.

4.4 Unloading Response Improvement by Using Body Brake

DAOT control is fast in response to load-step since a new switching cycle will be initiated the moment the output voltage drops below the target value. However, it's response to unloading condition is not always optimum. If unloading happens when the low side switch is on, since output is higher than target value, the off time will extend. If unloading happens when the high side switch is on, the high side switch can only be turned off after the set on-time, which will charge the inductor current to higher value and overshoot will increase.

This section focuses on the improvement of unloading response of DAOT controlled DC-DC converter. The proposed solution contains two parts. The first

part is to establish a criteria to turn off the high side switch within the set on-time, and the second part is to turn off the low side switch when inductor current is ramping down.

4.4.1 Criteria to Turn off the High Side Switch Within the Set On-Time

When DAOT controlled DC-DC converter operates with constant current, the high side switch turns on when the output voltage is lower than the target value, which will put a positive voltage across the inductor and ramp up its current. When the high side switch is turned off at the end of the set on-time, the output voltage will be higher than the target value by a specific amount depending on the operating condition, and it is normally smaller than the LSB of the ADC, hence the output will stay within the zero-error-bit.

If unloading happens during the on-time of high side switch, the difference between inductor current and output current will go to the capacitor and charge its output to be high.

Based on the above operation, during unloading, a simple criteria to turn off high side switch can be established: if the output voltage produces positive error bits higher than a set threshold (e.g. +2 bits) during the set on-time, the high side switch will be turned off.

To make the above operation effective, the conversion time of the ADC to generate the codes corresponding to the set threshold needs to be shorter than the set on-time.

4.4.2 Criteria to Turn off the Low Side Switch When Inductor Current is Ramping Down - Body Brake

For synchronous DC-DC converter, the low side switch will be turned on after the high side switch is turned off, which imposes a negative voltage across the inductor and makes the inductor current to discharge. If during this process, the low side switch is turned off, the inductor current will flow through the body diode and cause a negative voltage of $(-V_d)$ at the switching node, where V_d is the diode voltage drop when forward-biased. Hence the voltage across the inductor is $(-V_{out} - V_d)$. While when the low side switch is on, the voltage across the inductor is $(-V_{out} - I_L \cdot R_{ds,NMOS})$, which is approximately $(-V_{out})$ since $R_{ds,NMOS}$ is usually small. The method of turning off the low side switch when the inductor current is ramping down is referred to as body-brake since it utilizes the body diode of the low side switch to speed up the ramping down rate of the inductor current. For example, when the output voltage is 1 V and the diode voltage V_d is 0.7 V, the negative voltage across the inductor with the low side switch turned off is 70% higher, which will make the inductor ramps down with a faster rate and reduce the output overshoot.

The starting and ending timing of body-brake needs to be carefully designed. Body-brake should only be activated during unloading transient. In normal operation, turning off the low side NMOS transistor will greatly reduce the conversion efficiency. Several methods have been disclosed. One method is to directly monitor the output voltage: whenever it is crossing a threshold set higher than normal operating range, body-brake will start. In this type of implementation, there needs to be sufficient gap between the normal operating voltage range and body-brake threshold across all the process, power supply, and temperature variations. Since the output voltage has ripple and the ripple voltage changes with

external components and operating conditions, the variation in the ripple voltage also needs to be included when setting the body brake starting threshold. The resulting body-brake threshold needs to cover all the above variations, as shown in Fig. 4.4.1, which is usually too high for effective unloading transient improvement.

Fig. 4.4.1 Body-Brake Threshold for Direct Monitoring Method

Another method is to compare the error amp output with a set threshold. If the error amp output is higher than the threshold, body-brake is activated. The advantage is that the ripple effect is filtered out. However, error amp bandwidth limits the response time. And it is challenging to design a threshold voltage dynamically tracking the error amp output voltage under normal operating condition.

In a digitally controlled dc-dc converter, the output voltage is monitored by ADC. If the ADC used is of flash-type, such as the one proposed in Chapter 3, the information of the output voltage during unloading process can be obtained. Based on this, a new body-brake starting method is proposed: when the low side switch is on, if the output voltage continues to increase and produces error bits higher than a set threshold (e.g. +3 bits), unloading is confirmed and the low side switch is turned off by a latch. The latch is reset by the turn-on signal of the high side switch and the normal operation is resumed.

4.4.3 Proposed Unloading Recovery Algorithm

Based on the two proposed methods discussed in section 4.4.1 and 4.4.2, a new method for unloading recovery is proposed as following:

- 1) When the high side switch is on, if the ADC output is of certain code (programmable, e.g. +2 bits) higher than the zero-error-bit, the high side switch is turned off;
- 2) After high side MOS is turned off, if the ADC output continue to increase and becomes certain bits (programmable, e.g. +3 bits) higher than the zero-error-bit, the low side switch is turned off and body-brake starts;
- 3) When ADC output returns to zero-error-bit, body-brake stops and normal operation is resumed.

4.4.4 Simulation Verification

To verify the proposed algorithm, a DAOT converter with the parameters shown in Table 4.4.1 has been built and simulated.

TABLE 4.4.1 DAOT Converter Parameters for Unloading Simulation

Supply voltage	3.3 V
Output voltage	1 V
Ton (typical)	20 ns
Output capacitor	4.7 μ F (ESR = 30 m Ω)
Output inductor	2.2 μ H (DCR = 10 m Ω)
Unloading condition	550 mA to 50 mA in 0.1 μ s

Fig. 4.4.2 shows the simulation result. Unloading transient happens when the low side switch is on. Since inductor current, I_{inductor} , cannot change instantly, the excess current goes to the output capacitor and the output voltage goes up. When

output voltage is higher than the target value by 3 bits, the low side switch is turned off and the switching node voltage goes more negative. After the low side switch is turned off, I_{inductor} ramps down with fast slope.

Fig. 4.4.2 Simulation Result with Proposed Unloading Transient Recovery Method

Fig. 4.4.3 shows the comparison of unloading response with conventional control method. With the proposed method, overshoot reduces from 54.8 mV to 38.4 mV and the recovery time reduces from 5.9 μs to 4.0 μs.

Fig. 4.4.3 Simulated Unloading Response Comparison - Left: Conventional Control; Right: Proposed Control

To show the operation of the proposed algorithm when circuit non-ideality exists, firstly the parasitics of the power stage have been extracted and included in the simulation, and secondly the parasitics of the package and PCB have been included as 3 nH inductance and 10 mΩ resistance on power and ground connections, which are estimated from a standard DC-DC PCB board. Fig. 4.4.4 shows the simulation setup and results.

Fig. 4.4.4 Simulation with parasitic (a) simulation setup; (b) simulation waveform

As seen from Fig. 4.4.4 (b), the voltage of V_X exhibits ringing at its rising edge and falling edges due to the parasitics of power stage as well as power/ground pins. Comparing with Fig. 4.4.3 where no parasitic is added, the overshoot increased slightly by about 3.88 mV.

The above simulation has been repeated for different process corners with the added parasitics. And Table 4.1.3 summaries the simulation result with and without body-brake enabled. It can be seen from Fig. 4.4.4 and TABLE 4.4.2 that the proposed algorithm is able to reduce the unloading overshoot by over 30% by including the parasitics from power stage and external PCB connections across different process corners.

TABLE 4.4.2 Unloading simulation with parasitic and process corners

Process	Overshoot with body-brake disabled, mV	Overshoot with body-brake enabled, mV	Improvement, %
Typical	58.7	40.2	-31.5%
FF	60.5	41.3	-31.7%
FS	58.9	40.4	-31.5%
SF	55.2	38.1	-31.0%
SS	60.0	41.4	-31.0%

4.5 Summary

In this chapter, load transient response of the digitally controlled DC-DC converter is studied. A new level-based transient recovery method is proposed, to reduce the circuit complexity and achieve fast transient response. The proposed transient recovery method is simulated in system level by using the flash ADC designed in Chapter 3. It is shown that the proposed transient recovery method can improve the transient response significantly. The non-optimum mode transition point issue with the proposed transient recovery method is discussed.

To improve the unloading transient recovery of DAOT, a new algorithm has been proposed which establishes criteria to turn off the high side switch within the set on-time, and to turn off the low side switch when inductor current is ramping down. The algorithm has been verified by simulations which reduces the unloading overshoot by 30%.

Chapter 5 Dead-Time Optimization

5.1 Introduction

The operation principle of DAOT buck converter is as follows (Fig. 5.1.1). When the output voltage drops below the set threshold, an asynchronous ADC monitoring the output voltage will initiate the controller to turn on the high side switch for a predetermined period of time. After that the high side switch is turned off and the low side switch is turned on till the output voltage drops below the set threshold again. When steady state is reached, the DC-DC converter switches at the required duty cycle by adjusting the off time of the high side switch.

Fig. 5.1.1 Digital Constant On-Time Buck Converter Block Diagram with Proposed Dead-Time Optimization Block

As any power converter used in battery operated equipment, the conversion efficiency is of paramount importance for DAOT as well. In this section, a method that is able to minimize the loss due to dead-time in DAOT is proposed. Simple logic blocks are used in the implementation, which makes the design scalable and easy to port to other processes. In Section 5.2, the power losses in a DAOT system are first identified. Following that, in Section 5.3, a review of reported methods to minimize dead-time is presented. Section 5.4 describes the principle of the proposed dead-time optimization method. The implementation details using 0.18 μ m CMOS process and simulation results are discussed in Section 5.5. Section 5.6 concludes this chapter.

5.2 Power Losses in Digital Adaptive On-Time (DAOT) System

In this section, the power losses in a typical DAOT system is analyzed. Similar to other synchronously rectified DC-DC converters, the main losses include:

- 1) External components and PCB track loss;
- 2) Conduction loss of MOS switches;
- 3) Switching loss due to overlap of voltage and current across the terminals of the power switches;
- 4) Gate charging loss;
- 5) Dead-time loss;
- 6) Quiescent current loss.

5.2.1 Inductor Current RMS Value under CCM

Fig. 5.2.1 Inductor Current Waveform (CCM)

As shown in Fig. 5.2.1, under continuous-conduction-mode (CCM), the inductor current centers around the load current I_{load} , with a ripple component I_{ripple} . The valley point and the peak point of the inductor current are $(I_{load} - 0.5 \cdot I_{ripple})$ and $(I_{load} + 0.5 \cdot I_{ripple})$ respectively. The time that the inductor current rises from valley point to peak point is denoted as T_{on} , which is the on-time of the high side switch. The time that the inductor current falls from peak point to valley point is denoted as T_{off} , which is the off-time of the high side MOS switch. The low side MOS switch is a synchronous rectifier - it turns on when the high side MOS switch is off and turns off when the high side MOS switch is on. The switching period T is equal to the sum of T_{on} and T_{off} .

Since the power calculation involves root-mean-square (RMS) value, the RMS value of the inductor current is first derived.

During T_{on} , the inductor current can be expressed as

$$I_L(t) = I_{load} - 0.5 \times I_{ripple} + I_{ripple} \times \frac{t}{T_{on}} \quad (5.2.1)$$

Hence the rms value of the inductor current during T_{on} , $I_{L(rms),on}$, is given by

$$I_{L(rms),on} = \left[\frac{1}{T_{on}} \int_0^{T_{on}} I_L(t)^2 dt \right]^{1/2} \quad (5.2.2)$$

Substitute (5.2.1) to (5.2.2), and square both sides,

$$\begin{aligned}
 I_{L(rms),on}^2 &= \frac{1}{T} \int_0^{T_{on}} (I_{load} - 0.5 \times I_{ripple} + I_{ripple} \times \frac{t}{T_{on}})^2 dt \\
 &= \frac{1}{T} [(I_{load} - 0.5 \times I_{ripple})^2 \times t \Big|_0^{T_{on}} \\
 &\quad + (I_{load} - 0.5 \times I_{ripple}) \times I_{ripple} \times \frac{t^2}{T_{on}} \Big|_0^{T_{on}} \\
 &\quad + \frac{1}{3} (I_{ripple}^2 \times \frac{t^3}{T_{on}^2}) \Big|_0^{T_{on}}] \\
 &= \frac{T_{on}}{T} \times (I_{load}^2 + \frac{I_{ripple}^2}{12})
 \end{aligned} \tag{5.2.3}$$

Similar analysis can be done during T_{off} (as in Fig. 5.2.1), which yields the following expression.

$$I_{L(rms),off}^2 = \frac{T_{off}}{T} \times (I_{load}^2 + \frac{I_{ripple}^2}{12}) \tag{5.2.4}$$

In CCM, load current is always higher than half of the ripple current that is:

$$I_{load} \geq 0.5 \times I_{ripple} \tag{5.2.5}$$

Hence

$$I_{load}^2 \geq 0.25 \times I_{ripple}^2 \tag{5.2.6}$$

The effect of I_{ripple} on the rms current is less than 1/3 of load current. Hence when load current is reasonably high, the following equations can be assumed which simplifies the calculation without losing much accuracy.

$$I_{L(rms),on}^2 \approx \frac{T_{on}}{T} \times I_{load}^2 \tag{5.2.7}$$

$$I_{L(rms),off}^2 \approx \frac{T_{off}}{T} \times I_{load}^2 \tag{5.2.8}$$

5.2.2 External Components and PCB Track Loss

The loss of filter capacitor is mainly due to the equivalent series resistance, R_{es} , which can be calculated as:

$$P_{COUT} = I_{L(rms),ripple}^2 \times R_{es} = \frac{I_{ripple}^2 \times R_{es}}{12} \quad (5.2.9)$$

The loss of the PCB track is mainly due to the copper track resistance, R_{track} , in the high current path, which can be calculated as

$$P_{PCB} = I_{L(rms)}^2 \times R_{track} = (I_{load}^2 + \frac{I_{ripple}^2}{12}) \times R_{track} \quad (5.2.10)$$

The loss of inductor mainly comes from the dc resistance (R_{DCR}) and ac resistance (R_{ACR}) of the inductor coil, which can be calculated as

$$P_{L(DC)} = I_{L(rms)}^2 \times R_{DCR} = (I_{load}^2 + \frac{I_{ripple}^2}{12}) \times R_{DCR} \quad (5.2.11)$$

$$P_{L(AC)} = I_{L(rms),ripple}^2 \times R_{ACR} = \frac{I_{ripple}^2}{12} \times R_{ACR} \quad (5.2.12)$$

The losses of the external component and PCB track can be minimized by choosing components with lower resistances (R_{ESR} , R_{DCR} , or R_{ACR}) and laying out short and thick copper tracks for high current paths.

5.2.3 Conduction Loss of MOS Switches

When inductor current is charging up, during T_{on} in Fig. 5.2.1, the current goes through the high side MOS switch. When it ramps down, the current goes through the low side MOS switch. Hence inductor current can be used to calculate the conduction loss of the MOS switches.

Assume the conduction resistances of the high side and low side MOS switches are $R_{DS(on),HS}$ and $R_{DS(on),LS}$ respectively, the conduction loss can be calculated by the following equations:

$$P_{con}(HS) = I_{L(rms),on}^2 \times R_{DS(on),HS} \quad (5.2.13)$$

$$P_{con}(LS) = I_{L(rms),off}^2 \times R_{DS(on),LS} \quad (5.2.14)$$

To minimizing the conduction loss of the MOS switches, $R_{DS(on)}$ should be minimized, which can be achieved by using minimum gate length that could still fulfill reliability requirement, larger gate width (trade off with switching loss), proper layout that excites the switch cells evenly, and optimally sizing the high side and low side MOS switches based on the duty cycle.

5.2.4 Switching Loss Due to Voltage/Current Overlap

Switching loss results from the overlap of voltage across a MOSFET's drain and source terminal and the current through it when it is being turned on or off.

Fig. 5.2.2 shows the voltage and current waveforms during turn on of high side MOSFET.

At t_0 , the driver starts to charge the gate of MOSFET. Shortly before this, the low side MOSFET has been turned off and the inductor current is being fed by the current flowing from ground to the switching node via the low side MOSFET body diode.

At t_1 , the voltage across gate and source ($|V_{GS}|$) is higher than the threshold voltage (V_{TH}), the drain current ($|I_{DS}|$) starts to increase. At this time, the drain current is smaller than inductor current, and the drain voltage stays low since the low side MOSFET body diode needs to be forward biased to supply the deficit current. The gate voltage continues to increase, so does the drain current since there is more over-drive available.

At t_2 , the drain current is equal to inductor current, hence the drain voltage starts to go up. The gate voltage is maintained to be constant between t_2 and t_3 , since the driver current is charging the capacitance between gate and drain.

At t_3 , $|V_{DS}|$ becomes 0 and $|V_{GS}|$ starts to increase until it has reached the

maximum voltage swing of the driver at t_4 .

Fig. 5.2.2 Switching Loss Due to Overlap of V_{DS} and I_{DS} during Turn-On

In the above process, the time between t_1 and t_3 incurs the majority of losses for the high side MOSFET. From t_1 to t_2 , drain current increases from 0 to the lower boundary of inductor current when drain to source voltage is at maximum. While from t_2 to t_3 , the drain to source voltage starts to decrease from maximum value to minimum value. Before time t_1 or after time t_3 , either current is small or voltage is small, hence the loss is much smaller.

The power loss between t_1 and t_3 can be calculated as following by defining $t_{hs_on} = t_3 - t_1$:

$$P_{sw_hs_on} = f_{sw} \times \int |V_{DS}| \times |I_{DS}| dt \approx 0.5 \times f_{sw} \times V_{DR} \times I_{L,MIN} \times t_{hs_on} \quad (5.2.15)$$

Similarly, the following equations can be derived for other switching losses:

$$P_{sw_hs_off} \approx 0.5 \times f_{sw} \times V_{DR} \times I_{L,MAX} \times t_{hs_off} \quad (5.2.16)$$

$$P_{sw_ls_on} \approx 0.5 \times f_{sw} \times V_{DR} \times I_{L,MAX} \times t_{ls_on} \quad (5.2.17)$$

$$P_{sw_ls_off} \approx 0.5 \times f_{sw} \times V_{DR} \times I_{L,MIN} \times t_{ls_off} \quad (5.2.18)$$

It is worth noting that when low side MOSFET is turning on and off, the drain to source voltage change is the forward voltage drop of the body diode (V_D), which is much smaller than the high side MOSFET case (V_{DR}).

5.2.5 Gate Charging Loss

The loss associated with charging and discharging of the MOSFETs can be calculated as (5.2.19) by defining the gate charge of high side and low side MOSFET as $Q_{g,hs}$ and $Q_{g,ls}$ respectively.

$$P_{gate} = (Q_{g,hs} + Q_{g,ls}) \times f_{sw} \times V_{DR} \quad (5.2.19)$$

5.2.6 Dead-Time Loss

Synchronous rectification (SR) technique has been widely used in low output voltage high output current buck converters to achieve better conversion efficiency. When conducting the inductor current (I_L), the voltage across sync FET (M_N in Fig. 5.1.1) is equal to ($I_L \times R_{DS(on),LS}$), where $R_{DS(on),LS}$ is the on-resistance of M_N . Since ($I_L \times R_{on}$) is usually much less than the diode forward bias voltage, SR offers lower conduction loss comparing with a freewheeling diode. However, unlike the freewheeling diode that is self-driven, control signals that turn on/off SR need to be well controlled. Some amount of delay, which is called dead-time, is necessary to

make sure the control FET (M_P) and sync FET (M_N) will not turn on at the same time.

Sub-optimal dead-times, however, will result in additional power loss. In general, there are 3 types of losses that will happen when t_{DT1} is sub-optimal; (1) shoot-through current loss, (2) C_X switching loss and (3) body-diode conduction loss. The timing of the gate drive voltages (V_{PG} and V_{NG}) are responsible for the respective losses. The resultant response of the switching node (V_X) are as illustrated in Fig. 5.2.3.

A) Shoot-Through Current Loss

When $t_{DT} < 0$, M_N is switched ON before M_P goes OFF and a large shoot-through current flows through M_P and M_N due to the low ON resistance of the switches (Fig. 5.2.3a). This situation must be avoided as the shoot-through current not only introduces large power loss, but also could permanently damage the power converter. During the shoot-through condition, V_X can be approximated by the ratio of the ON resistances of M_P and M_N , and V_{IN} .

B) C_X Switching Loss

When M_P switches OFF and M_N is yet to be ON, charges stored in C_X , which is the capacitance associated with V_X , are transferred to the output by the inductor current (I_L). However, when t_{DT} is positive, but less than the optimal value (t_{DT-OPT}), i.e. $0 < t_{DT} < t_{DT-OPT}$, charge transfer is interrupted by M_N , which pulls V_X to ground (Fig. 5.2.3b). As a result, C_X switching loss is incurred as remaining charges are discharged to ground instead of being transferred to the output.

C) Body-Diode Conduction Loss

When $t_{DT} > t_{DT-OPT}$, V_X is pulled below ground by I_L and when $V_X \approx -0.7$ V, the body diode of M_N is switched ON and conducts I_L , thus contributing to body-diode conduction loss (Fig. 5.2.3c). Body-diode conduction is considered as highly inefficient, especially in low voltage DC-DC converters, as V_{DS} of M_N , when switched ON, is designed to be much lower than 0.7 V.

Fig. 5.2.3 Losses Due to Sub-Optimal Dead Time: (a) $T_{dt} < 0$, (b) $0 < T_{dt} < T_{dt-OPT}$, (c) $T_{dt} > T_{dt-OPT}$

5.2.7 Quiescent Current Loss

Quiescent current is the current consumed by the internal blocks. The associated loss can be calculated as:

$$P_q = V_{in} \times I_{cq} \quad (5.2.19)$$

5.3 Reported Dead-Time Optimization Methods

Among all the losses analyzed in section 5.2, external component loss depends on the availability and cost of the parts; conduction loss, switching loss, and gate charge loss are optimized by the power transistor structure and layout optimization; quiescent loss is related to the operating speed and noise rejection requirements of the internal blocks of the DC-DC converter and is especially important when the output power is light. In Chapter 6, a method that greatly reduces the quiescent loss of the DC-DC converter is developed for energy harvesting applications. In this section, the focus will be on the optimization of dead-time.

Traditionally, fixed dead-times were inserted to prevent shoot-through current under the entire range of operating conditions of the converter. This results in long periods of body-diode conduction under most operating conditions.

Adaptive Dead-Time Controllers (DTC) proposed in [123] [124] ensures that shoot-through events will never occur by cross-coupling the gate voltages of the PMOS and NMOS. Although the adaptive DTC proposed adjusts the dead-times according to variations in operating conditions, the delay of the comparators and the gate drivers are not compensated which could be quite significant.

To achieve smaller dead-time, various sensor-less dead-time tuning algorithms have been proposed, which optimize the dead-times using information easily

available from the converter's control loop [125, 126]. These methods adjust the dead-times such that either the input current [125] or the duty cycle [126] is minimized, which corresponds to maximizing the converter's conversion efficiency. However, these algorithms require the output current to be stable during optimization, thus making them unsuitable for applications with fast changing operating conditions.

In [127], the DC-DC converter is calibrated to operate with optimum dead-time under a set of predefined operating conditions and the dead-time is adjusted in accordance to load variations. The calibration can be done by finding the minimum duty cycle as stated above. However, an accurate on-chip load current sensor is required and the DTC could not optimize the dead-times when other operating conditions, such as the input voltage (V_{IN}) and temperature, are varied.

For rapid optimization of dead-times under varying operating conditions, the predictive DTC can be employed [128-131]. In general, the predictive DTC detects the occurrence of the body-diode conduction and adjusts the dead-times accordingly so that it is prevented in subsequent switching cycles. In [128], the prediction is performed by approximating the discharging of V_x with a linear relationship, but it could only achieve near-optimal dead-times. In [129], the delay generator is controlled by a counter, which could only perform step-wise delay variations that results in a slow transient and limited delay resolution. For [130], an analog delay-lock-loop (DLL) is used to speed up the optimization process, but it requires high-speed, power hungry comparators. In [131], a NOR gate replaces the comparators to detect the body-diode conduction and a "One-Step" method is used to obtain the optimized dead-times rapidly by quantizing the time error and subtracting it from the current delay. However, the time resolution is limited by the

quantizer for the time error. Furthermore, the NOR gate can only detect the occurrence of body-diode conduction, but not the more damaging shoot-through events. As such, unlike the analog DLL method that corrects both the shoot-through event and body-diode conduction, the "One-Step" method only increases the delay step-wise when the body-diode conduction is not detected.

5.4 Proposed Counter-Based Dead-Time Control (DTC) Method

In order to maximize the conversion efficiency of the buck converter, it is imperative that all 3 types of loss, discussed in Section 5.2.6, be minimized by constantly optimizing t_{DT1} such that it operates at $t_{DT1-OPT}$ under varying operating conditions. It is observed that when DAOT converter enters steady state under constant load, the off-time will be the longest when optimum dead time is applied, in other word, the switching frequency will be the lowest. The proposed dead time controller is based on "perturb then observe" algorithm. During the optimization process, the dead time is varied in steps to find the best setting that minimizes the switching frequency, which in turn will optimize the efficiency.

The relation of the optimum dead time and switching frequency for DAOT buck converter could be explained by referring to Fig. 5.2.3. The output voltage is the average of V_x . When dead time is shorter than optimum, as shown in Fig. 5.2.3(a), the shade area represents portion of V_x voltage that has been lost. To keep the output voltage constant, the off-time needs to be shorter, hence faster switching frequency. When dead time is longer than optimum, as shown in Fig. 5.2.3 (c), the body diode will conduct and cause V_x voltage to go to negative diode voltage, hence the average value of V_x will become smaller if the off time is the same. To

compensate the shaded area in Fig. 5.2.3 (c), the off-time needs to be shorter, hence a faster switching frequency as well.

The block diagram of a DAOT converter with the proposed DTC is shown in Fig. 5.1.1, the operation of which could be best understood by the flow chart shown in Fig. 5.4.1.

Before the optimization process starts, the dead time is determined by Adaptive Dead-Time Controllers (DTC) as proposed [123] [124] which is safe for all operating and process corners.

The switching frequency is measured by a counter within a set time period and the number of pulse is stored as Np_old . The optimization process only starts if Np_old stays the same for a number of consecutive measurement cycles, which indicates that the load current is constant.

When dead-time optimization starts, the dead time is reduced by one step, Δt , from the current value. Then the new switching frequency is again measured by the counter with the same time period. The number of pulses under the new dead time, Np , is compared with the previous stored value, Np_old . If the new frequency is slower than the previous value, which indicates that the efficiency is improved with the new dead time, the new dead time will be applied. The dead time is then reduced by another step and the process continues until it is detected that further reduction of dead time would cause the switching frequency to increase, which indicates the efficiency becomes lower. Then the dead time will change back to the value of the previous step and the optimization process is completed. The optimization is first performed on t_{DT1} , and then followed by t_{DT2} .

Fig.5.4.1 DAOT Dead Time Optimization Flow Chart under Steady Load Current

This method does not work well if the load current is changing within the measurement period. For that kind of the system, the same method might still be applicable if the load pattern is periodical and the counter period is long enough. For this section, we assume that the load current stays constant for the time period when the optimization is in progress.

5.5 Circuit Implementation Details and Simulation Results

In order to evaluate the performance of the proposed counter-based DTC, a synchronous buck converter is built and simulated, with the parameters shown in Table 5.5.1.

TABLE 5.5.1 DAOT Buck Converter Design Parameters

Input voltage	3.7V
Output voltage	1.5V
Capacitor	4.7 μ F (ESR = 30 m Ω)
Inductor	2.2 μ H (DCR = 10 m Ω)
On time	40.5 ns
Load current	300 mA

The waveform of ON, Pdrv, Ndrv, V_{PG} , V_{NG} and V_X are as shown in Fig. 5.5.1. When V_{OUT} is less than target value, ON signal changes from low to high. Pdrv signal rising edge is delayed by a fixed 4 ns delay, T_{dly} , from the rising edge of ON signal, while the falling edge of Pdrv is determined by the on-time generator. Ndrv signal rising edge follows the rising edge of ON signal with a programmable delay, DT1, and its falling edge follows the falling edge of Pdrv with another programmable delay, DT2. The delay time of DT1 and DT2 are controlled by 4-bit

signal with 0.5 ns step. Before optimization, DT1 is put at code 0 and DT2 is put at code 15, which generates 0 and maximum delay time respectively. The dead times between Pdrv and Ndrv are maximum. Note that the delay time can be determined by adaptive dead time method as well. The delay between rising edges is T_{dly} , while the delay between falling edges is maximum delay of DT2, which is 8 ns. These two values are designed such that they are safe across process and operating condition corners. During the optimization process, DT1 increases from 0 till the optimum value is found. Similarly, DT2 decreases from 15 till the optimum value is found.

Fig. 5.5.1 Gate Driving Signals

The counter period is set by a relaxation oscillator as shown in Fig 5.5.2. The absolute accuracy of the relaxation oscillator output frequency is not important since the same period will be used in consecutive optimization cycles. Hence the

relaxation oscillator is designed with the aim to reduce the current consumption. In this design, $I_b = 0.15 \mu\text{A}$, $C_t = 10 \text{ pF}$, the threshold voltage of the inverter connected to C_t , $V_{th,I1}$, is roughly 0.9 V , which makes T_{clk} to be $60 \mu\text{s}$. The value of C_t can be reduced if frequency divider is added to the output of the relaxation oscillator.

Fig. 5.5.2 Relaxation Oscillator Block Diagram

A 10-bit ripple counter, as shown in Fig. 5.5.3, is used to count the switching cycles within the measurement period. The number of bits of the counter is a trade-off between optimization speed and resolution. For longer measurement period, more counter bits are necessary and the optimization period become longer, but it can make the dead time closer to the optimum value.

Fig. 5.5.3 Block Diagram of 10-Bit Counter

Fig. 5.5.4 and Fig. 5.5.5 show the simulated switching frequency and efficiency versus different dead time setting, where the dead time is manually changed with 0.5 ns step. For Fig.5.5.4, DT2 is fixed at code 15 and there is a minimum switching frequency point when DT1 is at code 7, or 3.5 ns. For Fig. 5.5.5, DT1 is fixed at code 0 and there is a minimum switching frequency point when DT2 is at code 4, or 2 ns.

Fig. 5.5.4 and Fig. 5.5.5 also shows that the peak efficiency happens at the lowest switching frequency point. In this case, the optimization of dead time actually has two effects on the conversion efficiency. Firstly, by optimizing the dead time, the body conduction loss is reduced; secondly, the switching frequency is reduced which reduces the switching loss.

The factors influencing the efficiency in this simulation include: dead time loss, switching loss, and shoot-through loss if dead time is too small. The switching frequency, or equivalently, the on-time of the DAOT system, is determined by output ripple requirement as well as output filters. Once the on-time is fixed, optimizing the dead time does not affect the switching frequency so much. As shown in Fig. 5.5.4, the variation in switching frequency is about 2%, which is an acceptable number. The purpose of the proposed algorithm is to optimize the dead-time under the given on-time setting, while trying to avoid shoot-through.

Fig. 5.5.4 Switching Frequency and Efficiency versus DT1 with DT2=15

Fig. 5.5.5 Switching Frequency and Efficiency versus DT2 with DT1=0

Fig. 5.5.6 shows the control signals during optimization process in the simulation.

Fig. 5.5.6 Simulated Optimization Waveforms. From Top to Bottom: Opt_Start, DT1_Control, DT2_Control, DT1_Done, DT2_Done

Fig. 5.5.7 shows the waveform of driving signals, FET gate signals and switching node before and after optimization. It can be seen that the body diode conduction is almost completely eliminated by the proposed optimization algorithm.

Fig. 5.5.7 Simulated Optimization Waveforms: (a) Before Optimization, (b) After DT1 Optimization, (c) After both DT1 and DT2 Optimized

To check the robustness of the proposed algorithm in the presence of layout and PCB parasitics, the simulation is re-run by including extracted parasitics of the power stage and estimated PCB parasitics on power/ground pins, as shown in Fig. 4.4.4 (a). Switching frequencies and efficiencies versus dead-times have been shown in Fig. 5.5.8. Because of the added resistances at power/ground pins, the peak efficiency has significantly reduced comparing with Fig. 5.5.4 and Fig. 5.5.5, which is expected. And the optimum dead-time setting is now $DT1=10$ and $DT2=4$. It can be observed that the peak efficiency point still coincide with the minimum switching frequency point, hence the above proposed algorithm is effective in minimizing the deadtime and maximizing the efficiency. From these simulation results, it is apparent that optimized dead-time setting is affected by parasitics, hence fixed dead-time will result in sub-optimum efficiency under some conditions. To achieve optimum setting, programmable delay and maximum searching algorithm, as the one proposed by this chapter, are needed.

Fig. 5.5.9 shows the waveform of driving signals, FET gate signals and switching node before and after optimization, with parasitics included.

(a)

(b)

Fig. 5.5.8 Post layout simulation result: (a) switching frequency and efficiency versus DT1 with DT2=15; (b) switching frequency and efficiency versus DT2 with DT1=10

Fig. 5.5.9 Simulated optimization waveforms with parasitic: (a) before optimization, (b) after both DT1 and DT2 have been optimized

5.6 Summary

In this section, various losses in buck converter are analyzed. Methods of minimizing dead-time have been reviewed. A counter-based dead time optimization method is proposed for DAOT buck synchronous converter. The effectiveness of the proposed method is verified by simulation. This method utilizes some simple digital circuits and is well suited for digital control DAOT buck converts. The simulation result shows that the proposed method could improve the efficiency by 2.3%.

The efficiency improvement is a typical number at the given process parameters, which will change with process parameter and operating conditions. The significance of the proposed method is that it provides a method to minimize the dead time when output load is constantly high. The expense of achieving this improvement is added silicon area of relaxation oscillator (if the system does not have one), counters, registers to store the optimizing parameters and logic circuits to implement the flow chart. Except the relaxation oscillator, all other circuits are digital in nature and can be easily designed and synthesized. To apply this method commercially, it needs to be simulated using the corner models of the targeted process to determine there is enough sensitivity of switching frequency variation against dead time optimizing step.

Chapter 6 Ultra-Low-Power Operation for Energy Harvesting Applications

6.1 Introduction and Literature Review

A typical WSN consists of three parts: sensors, power management unit and RF unit which communicates with base stations. Sensors find wide applications nowadays in smart buildings, low power implantable health monitors, industrial automation, etc. In this section, the study is focused on the power management needs and solutions to one special type of WSN - indoor image sensor network.

Image sensing network, which is used indoor for motion detection and image capturing, is preferred to be self-powered, to avoid costly battery replacement [132, 133]. Harvesting energy from the environment where the sensor is located is a promising solution [134]. One of such energy source is indoor lighting [19, 135].

There have been active researches on reducing the power of image sensor so that it could be operating under relative low harvested energy [136, 137]. Low power image sensor consumes only 1.36 μW has been reported in [137]. For this power range, image sensor can operate by harvesting energy from indoor lighting through amorphous silicon photovoltaic (PV) cells.

To achieve maximum output power, the output voltage of the PV panel needs to be locked at the maximum power point (MPP) by a maximum power point tracker (MPPT), which is usually a DC-DC converter [138].

An energy storage device, such as battery, is needed to regulate the output power of the PV panel, which often fluctuates with the illumination level.

Image sensor commonly requires a high supply voltage, such as 1.8 V in [137], to achieve sufficient sensitivity. At the same time, the digital blocks in the sensing

network should operate at 1V power supply or lower to minimize power consumption. As a result, the remote sensor system would require at least two voltage rails to optimize its performance. Hence, there are three DC-DC conversions necessary in the sensor system, as shown in Fig. 6.1.1: MPPT tracking, sensor/analog core power supply regulation, and digital core power supply regulation.

Fig. 6.1.1 A Typical Energy Harvesting System For a Remote Sensor [139].

The power consumption of the remote sensor and the power conversion efficiency directly determine the power rating of the PV panel required, and hence the overall form-factor and cost of such a system. Most of the time, the remote sensor system is in standby mode and the load current is as light as a few μA . However, when the sensor is active, it consumes 3 to 4 orders higher current. To maintain good power conversion efficiency across such a large load range, especially during standby mode, the quiescent power of the energy harvesting and power conversion system has to be as low as possible.

There have been active researches on reducing the quiescent power of energy harvesting systems.

In [135], two PWM converters employing conventional proportional-integral

control method are used. The total power consumption is reported to be 135 μW .

In [140], a switch-capacitor power converter architecture with a power consumption of 2 μW has been reported. The switching frequency of the reported power converter, which is controlled by a relaxation oscillator, varies according to the power level. As such, when the harvested power is low, the switching frequency can be lowered to reduce the power consumption. The power supply of the relaxation oscillator is a linear voltage regulator, which consumes a significant amount of DC power regardless of the power level. Two reference voltages and two comparators are used in the relaxation oscillator block. Considerable amount of static power consumed by the reference voltage generators and comparators limits the further reduction in overall power consumption. Furthermore, the switch-capacitor architecture can only regulate the output voltage to discrete levels.

A voltage doubler and harvester has been reported in [141], which provides output voltages with programmable conversion ratios to the input, however, the output voltage is unregulated.

In [142], an inductive boost converter that is able to regulate the output voltage to a continuous range of values has been reported, with a static power consumption of 1.95 μW . The controller operates with pulse-skipping-modulation (PSM). When the power level is low, several switching cycles will be skipped to minimize switching losses. The number of switching cycles to be skipped depends on the power harvested from the PV cells and the required voltage level for maximum power point tracking of the PV cells. A nano-power reference circuit and a relaxation oscillator are included in the controller.

In [143], a boost converter with MPPT has been reported, which achieves 330

nA quiescent current by using sampled structure and clock/power gating.

In ultra-low power applications, like biomedical implantable electronic systems which requires less than 4 nW output power, inductive boost converter with sub 1 nW quiescent power has been reported [144].

In all designs discussed above, the power converter transfers the input power from the energy harvester, such as PV cells, to recharge the energy storage, such as a battery. As a result, an additional voltage converter is needed to convert the battery voltage to the voltage required by the load, which will inadvertently reduce the overall power efficiency of the system.

In [138], [145] and [146], power converters have been reported that is capable of transferring the harvested power to both the energy harvester and the load in one conversion step, thus improving the overall power efficiency. In [138], an inductor is time-shared by multiple conversion paths operating in DCM with a fixed system period. The system period needs to be short enough to support the worst case load, which results in extra switching under light load condition. Lead-lag compensation has been used in controllers reported in [145] and [146], which requires error amplifiers and comparators with significant amount of the static power consumption.

A low quiescent-power single-inductor dual-inputs-tri-outputs buck-boost converter (DITOB) is reported [147], which is able to transfer the input power to the load in one conversion step using fixed on-time control. A quiescent power of 400 nW has been achieved for the buck-boost converter designed using 0.18 μm CMOS process at typical input voltage. To fulfil output ripple requirement, on-time needs to be designed based on the maximum input voltage since on-time is fixed, which results in sub-optimum on-time for lower input voltages.

6.2 Control Architecture and Operation

In this section, adaptive on-time control to the previous DITOB[147] is proposed. By changing on-time according to the input voltage, power conversion efficiency could be improved over the useful input voltage range. First the operation principle of DITOB converter is explained, which is similar to the existing DITOB as reported in [147], except the adaptive on-time generator. A low-power ring oscillator has been designed and characterized by a test chip, which is used as the system clock. Following that the relationship between output ripple voltage and on-time is derived. The implementation of adaptive on-time generator is presented in Section 6.3. Simulation and experiment results are presented in section 6.4 and 6.5, respectively. Section 6.6 summarizes this chapter.

The architecture of the proposed DITOB converter is shown in Fig. 6.2.1, which consists of two major blocks: power stage and control circuit [147]. The power stage is a positive buck-boost configuration, which is capable of producing an output voltage that is either higher or lower than the input voltage. It is also capable of switching between two inputs and is able to regulate three output rails.

6.2.1 Controller Operation

As shown in Fig. 6.2.1, the control circuit of the DITOB comprises of SYS_CLK Generator, Bandgap Reference, Voltage Comparator, MPPT, INOUT Selector, Adaptive On-Time Generator, Dead-Time Controller (DTC), Zero Current Detector (ZCD) and Gate Drivers.

The operation of the control circuit is explained as follows. The rising edge of the SYS_CLK initiates a new switching cycle. Prior to that, all functional blocks, except the relaxation oscillator which generates SYS_CLK, are turned off. At the

beginning of the switching cycle, the Bandgap Reference is enabled to generate a reference voltage (VBG).

Fig. 6.2.1 Block Diagram of the Proposed DITOB.

The structure of the Bandgap Reference is similar to [148] with additional power gating switches at its input supply and output filter capacitor, as shown in Fig. 6.2.2. It consumes 1.8 μA current when enabled. The accuracy of VBG is important since it determines the status of harvested energy and the voltages of regulated output rails. In this design, 0.4% is targeted, which is trimmed manually after fabrication.

Fig. 6.2.2 Bandgap Block Diagram

The settling time of VBG is less than 800 ns under all conditions. At 2 μs after the Bandgap Reference is enabled, when VBG voltage is settled, a signal called VBG_RDY is generated, which triggers the voltage comparator block to compare the levels of all the input and output voltages of the DITOB one-by-one, to their respective reference voltages. The voltages of digital core, analog core, PV panel, and battery are represented by V_{10} , V_{18} , V_{PV} , and V_B respectively. Their reference voltages are represented by V_{REF-10} , V_{REF-18} , V_{REF-PV} , and V_{REF-B}

respectively, while the digital codes for the reference voltages (DREF) are represented by D_{REF-10} , D_{REF-18} , D_{REF-PV} , and D_{REF-B} respectively. An 8-bit Capacitive Digital-to-Analog Converter (CDAC) converts the digital codes to reference voltages. Out of the digital codes, D_{REF-10} , D_{REF-18} , and D_{REF-PV} can be stored in a memory device, such as an Electrically Erasable Programmable Read-Only Memory (EEPROM). In this design, all the above three reference voltages were hard-coded. As for the PV module, D_{REF-PV} is generated by the MPPT block to ensure MPP operation. Battery voltage V_B is monitored at both the source side to prevent over-discharging, and the load side to prevent over-charging; hence two reference voltages are required.

The results of the voltage comparison (CMP_{OUT}) is then sent to INOUT selector block to select one pair of input and output to be activated during the current switching cycle. When the harvested energy is excessive, indicated by PV panel charges its parallel capacitor (C_{PV} in Fig. 6.2.1) to a voltage higher than V_{REF-PV} , PV module is selected as the input. The harvested energy from the PV module is delivered through one power conversion step to either one of the two cores or to recharge the battery. On the other hand, when the harvested energy is low, the battery is selected as the input and the power required by the two supply rails will be supplied by the battery at their respective switching cycles. In this way, the output voltage of the PV panel is regulated at its maximum power point.

The selected input switch of proposed DITOB and M_3 in Fig. 6.2.1 are turned on for a period of time, called on-time, which is determined by the Adaptive On-Time Generator block, and are switched off when the on-time expires. After that, the selected output switch and M_2 are switched on to transfer the energy stored in the inductor to the selected load. When the inductor current ramps down

to zero, which is detected by the ZCD block, the input and output switches are switched off, while M_3 and M_2 are switched on (detail explanation in section 6.2.3). After that, all functional blocks of the control circuit, except the relaxation oscillator, are disabled to remove almost all static DC current consumptions and the control circuit enters sleep mode.

The control circuit will be awakened by the next rising edge of SYS_CLK , and begins the next switching cycle.

6.2.2 Oscillator Design and Test

In the proposed DITOB converter, the switching cycle initiating signal, SYS_CLK , is generated by the SYS_CLK generator block, as illustrated in Fig. 6.2.1. It consists of a relaxation oscillator to generate the main clock of the system (CLK), a frequency doubler ($2X_CLK$) to derive a signal with twice the CLK frequency and a 6-bit counter to derive the slower frequencies of CLK signal. The $FREQ_SEL$ block selects the corresponding SYS_CLK frequency based on the PFM algorithm described in [147].

Unlike other functional blocks, the SYS_CLK Generator block does not enter sleep mode after the switching activity is completed. Hence, it is imperative to minimize its power consumption, especially the relaxation oscillator since other blocks are digital in nature and only consume power during switching.

Relaxation oscillator has been widely used in low power system due to its simple structure and the fact that no off-chip component is needed [149, 150]. In a typical relaxation oscillator, as shown in Fig. 6.2.3, when Q is high, a capacitor is charged by a controlled current, I_b . When the voltage of the capacitor is higher than the reference voltage V_{REFH} , Q is reset to low and the capacitor starts to discharge.

When the capacitor voltage discharges to a lower second reference voltage V_{REFL} , Q is set to high and the capacitor starts to be charged again and the cycle repeats. Usually two comparators and two references are needed [151].

Fig. 6.2.3 Typical Relaxation Oscillator Structure

A current starved relaxation oscillator has been proposed in [134], and Fig. 6.2.4 shows the simplified diagram. The amplitude of CLK is mainly determined by the threshold of NMOS in the inverters, which reduces supply sensitivity. It is noted that when CLK signal transits from low to high, the charges in the two capacitor are pulled to ground, producing a short pulse. The advantage of the structure in [134] is that no reference generators or comparators are needed.

Fig. 6.2.4 Current Starved Relaxation Oscillator Structure.

A new relaxation oscillator which also requires neither comparators nor reference generators has been designed to minimize the power consumption of the SYS_CLK generator block. The structure is shown in Fig. 6.2.5a. Fig 6.2.5b shows the circuit that generates I_{BIAS} for the proposed relaxation oscillator [149]. The power supply (V_{DD}) of the relaxation oscillator is first connected to PV panel or battery during start-up. After V_{10} voltage stabilizes, V_{DD} is switched to V_{10} to have a stable power supply voltage at 1V. The power consumption of the oscillator also becomes lower with reduced voltage swing.

The operation of the proposed relaxation oscillator is now explained by referring to Fig. 6.2.6.

When CLK_EN is low, the oscillator circuit is put to off mode, and the output, CLK, is pulled low. The voltage of DLY1, which is across the first capacitor, is pulled to ground; while the voltage of DLY2, which is across the second capacitor, is pulled to V_{DD} . Notice that under this condition, there is no active current consumption except leakages.

(a)

(b)

Fig. 6.2.5 Proposed Relaxation Oscillator (a) Oscillator Structure; (b) Bias Current Generation Block [149]

At CLK_EN low to high transition edge, the relaxation oscillator starts to operate. The active devices before CLK goes high are highlighted in Fig. 6.2.6a. The voltage of node DLY1 is charged up by I_{BIAS} with the slope of (I_{BIAS} / C_1) . DLY1 is then connected to the inputs of two inverters. The first inverter, formed by transistor MP1 and MN1, is current starved by I_{BIAS} at both supply and ground. MP1 and MN1 are high threshold devices, which make them hardly conduct at the same time under 1V power supply. The second inverter, formed by transistor MP2 and MN2, is controlled by MP3 and MN3 with their gates connected to CLK. Since CLK is low at this time, MP3 is ON and MN3 is OFF. The switching point of the second inverter is $(V_{DD} - V_{th,p})$, where $V_{th,p}$ is the threshold voltage of low threshold PMOS. When DLY1 voltage crosses the threshold voltage of MN1, $V_{th,MN1}$, MN1 is ON. However, because MP3 and MP2 are both ON, DLY2 voltage stays high. When DLY1 voltage crosses the second inverter threshold, MP2 is turned off and DLY2 starts to be discharged by I_{BIAS} through MN1 with the slope of (I_{BIAS} / C_2) . It can be seen that when DLY1 is being charged up, DT_INV1 only consumes current when $V_{th,MN1} < DLY1 < (V_{DD} - V_{th,p})$, which is a small portion of the whole power supply range of the relaxation oscillator.

Similarly DLY2 is connected to two inverters formed by MP4/MN4 and MP5/MN5 respectively. The operation of DLY2 is similar to DLY1, except that the active devices become MP4 and MN5. The output of DT_INV2 is connected to a buffer block, BUF, to provide drivability at CLK output. The delay of BUF is negligible comparing with the total CLK period.

The active devices when CLK is high are highlighted in Fig. 6.2.6b. The operation is similar to when CLK is low. During this phase, DLY1 is discharged and DLY2 is charged, which make the high and low durations of CLK signal equal.

Fig. 6.2.6 Operation of the Proposed Oscillator (a) Active Devices When CLK is Low, (b) Active Devices When CLK is High, (c) Key Waveforms

From the waveforms shown in Fig. 6.2.6c, it can be seen that the time interval when CLK is low consists of t_{d1_r} and t_{d2_f} . Similarly the time interval when CLK is high consists of t_{d1_f} and t_{d2_r} .

In this design, $C_1=C_2=C$, hence t_{d1_f} , t_{d2_r} , t_{d2_f} , and t_{d1_r} can be calculated as (6.2.1) and (6.2.2):

$$t_{d1_r} = t_{d2_r} = \frac{C \times (V_{DD} - V_{th,p})}{I_{BIAS}} \quad (6.2.1)$$

$$t_{d1_f} = t_{d2_f} = \frac{C \times (V_{DD} - V_{th,n})}{I_{BIAS}} \quad (6.2.2)$$

The period of CLK, T , can be calculated as (6.2.3):

$$T = t_{d1_r} + t_{d2_f} + t_{d1_f} + t_{d2_r} = \frac{2 \times C \times (2 \times V_{DD} - V_{th,p} - V_{th,n})}{I_{BIAS}} \quad (6.2.3)$$

For this design, I_{BIAS} is 10 nA and $T = 100 \mu s$, which produces a 10 kHz clock signal.

From (6.2.3), it can be seen that T varies with the values of supply voltage, bias current, capacitor, MOS threshold voltages and temperature. By using V_{10} as the supply when it is in regulation, the supply variation can be suppressed since V_{10} is regulated with 1% accuracy. A post fabrication trim can in first order remove the process variation effect. Since MOS threshold voltages reduce with temperature, I_{BIAS} partially cancels the temperature variation due to that fact that it is proportional to absolute temperature. A more sophisticated bias current design will be needed to cancel the temperature effect totally. Since the system frequency is adaptive to the load current requirement, the absolute accuracy of the clock frequency is not required. However, a large variation in the clock frequency does

affect the load range that the proposed system is able to support.

Comparing with [134], the proposed relaxation oscillator can potentially generate a larger oscillation amplitude at the capacitors: $(V_{DD} - V_{th})$ vs. V_{th} , which reduces the capacitance needed to generate the same delay if charging currents are the same. Another advantage of the proposed oscillator is that by adding current starving at bottom side, the discharging of the capacitors are also used to generate delay, which improves the current utilization and reduces power consumption.

The highest frequency of SYS_CLK determines the maximum power that can be supplied by the DITOB. The rising edge of the SYS_CLK is used to initiate the switching cycle, hence the duty cycle of SYS_CLK is not so important. Since the duty cycle of CLK generated by the relaxation oscillator is 50%, 2X_CLK can be generated from CLK rising and falling edges. In this way, the output clock of the relaxation oscillator becomes half of the highest frequency required, hence consumes less power. To reduce power loss further, the 2X_CLK is only enabled when the converter needs to operate at 20 kHz. All the functional blocks of the SYS_CLK Generator, except the relaxation oscillator, are digital circuits that consume no static current.

A test chip using 0.18 μm CMOS process has been built to characterize the relaxation oscillator described above. Fig. 6.2.7 shows the uncompressed layout of the new relaxation oscillator and the area is $41 \mu\text{m} \times 26 \mu\text{m}$.

The die photo of the test chip is shown in Fig. 6.2.8. The package chosen is a 48-pin DIP ceramic package using wire-bond technology.

Since the quiescent current of the designed oscillator is expected to be several tens of nA, the test circuit for measuring the quiescent current is as shown in Fig. 6.2.9 (a), while Fig. 6.2.9 (b) shows the photo of the evaluation board. A low-pass

filter formed by 470 k Ω resistor and 10 μ F capacitor is inserted before the power supply of the oscillator block. The BUF block, which is used to drive the pad for measurement, is powered by another path, so that its current consumption will not be added to the oscillator block.

Fig. 6.2.7 Oscillator Block Layout

Fig. 6.2.8 Oscillator Test Chip Die Photo

Since the quiescent current of the designed oscillator is expected to be several tens of nA, the test circuit for measuring the quiescent current is as shown in Fig. 6.2.9 (a), while Fig. 6.2.9 (b) shows the photo of the evaluation board. A low-pass filter formed by 470 k Ω resistor and 10 μ F capacitor is inserted before the power supply of the oscillator block. The BUF block, which is used to drive the pad for measurement, is powered by another path, so that its current consumption will not be added to the oscillator block.

(a)

(b)

Fig. 6.2.9 (a) Test Setup; (b) Photo of Evaluation Board

The oscillator waveform when $V_{DD} = 1\text{ V}$ is as shown in Fig. 6.2.10. The switching frequency is about 10.64 kHz.

Fig. 6.2.10 Oscillator Output Waveform

The supply voltage has been swept from 0.9 V to 1.1 V and the switching frequency and input current are measured, as shown in Fig. 6.2.11 and Fig. 6.2.12.

Fig. 6.2.11 Input Current with Sweeping Supply Voltage

The input current is 25 nA when the supply voltage is at 1 V. The switching frequency changes about -10% ~ 10% with input voltage change. Since the

controller is adaptively changing the clock frequency, the variation of switching frequency is acceptable.

Fig. 6.2.12 Switching Frequency with Sweeping Supply Voltage

The jitter of the clock output is relatively big, when the oscilloscope is put to persist mode (Fig. 6.2.13), which makes the designed oscillator not suitable to timing critical applications. In the energy harvesting system, the clock is used to control the wake-up cycle of the internal blocks, hence jitter is not an issue.

Fig. 6.2.13 Oscillator Output Under Persist Mode

6.2.3 Power Stage Operation

The power stage is a buck-boost DC-DC converter stage with two inputs and three outputs, as shown in Fig. 6.2.1. During one switching cycle, only one pair of input and output are selected. The selection of battery or PV panel as the input is controlled by switches M_1 and M_7 . Switches M_4 , M_5 , and M_6 control which load will be selected: analog core, digital core or battery which stores the extra energy. The bodies of M_1 , M_5 , M_6 , and M_7 are always connected to the highest potential in the system; hence the body diodes are reverse-biased all the time. The power stage is always operating in DCM - the inductor current ramps down to zero before the next switching cycle starts. This is to avoid cross-conductions among output rails sharing the same inductor.

The simplified schematic of the power stage is shown in Fig. 6.2.14, when M_5 or M_6 is selected as output switch transistor. Since M_4 is a NMOS transistor, when it is selected as output switch transistor, the gate driving signal will be of opposite polarity. $V_{IN,i}$ and $M_{IN,i}$ represent the selected input and its corresponding switch transistor, while $V_{OUT,i}$ and $M_{OUT,i}$ represent the selected output and its corresponding switch transistor. The gate drive signals for the switch transistors are indicated by D_{ip} , D_{in} , D_{op} , and D_{on} respectively.

Fig. 6.2.14 Simplified Schematic of Power Stage.

Within one switching cycle, the operation of the power stage can be divided into three phases as shown in Fig. 6.2.15a, b, and c respectively. The typical waveforms of the power stage are shown in Fig. 6.2.15d.

Phase 1: D_{ip} and D_{in} are low, while D_{op} and D_{on} are high; hence $M_{IN,i}$ and M_3 are ON while M_2 and $M_{OUT,i}$ are OFF. $V_{IN,i}$ is applied across the inductor L and the current of L , i_L , increases linearly with the slope of $(V_{IN,i}/L)$. The load current, I_{LD} , is supplied by the output capacitor, C_O .

Phase 2: D_{ip} and D_{in} are high, while D_{op} and D_{on} are low; hence $M_{IN,i}$ and M_3 are OFF while M_2 and $M_{OUT,i}$ are ON. The input is disconnected from the inductor, hence the input current, i_{IN} , is 0. The voltage across L is $(-V_{OUT,i})$, hence i_L decreases with the slope of $(-V_{OUT,i}/L)$. As a result, the energy stored in the inductor is transferred to the output, thereby supplying I_{LD} and charging C_O . When inductor current decreases to zero, which is detected by ZCD block in control circuit, the operation will move to Phase 3.

Phase 3: D_{ip} , D_{in} , D_{op} , and D_{on} are all high; hence $M_{IN,i}$ and $M_{OUT,i}$ are OFF while M_2 and M_3 are ON. The two terminals of the inductor are both shorted to ground to reduce ringing around them. During this phase, the load current is supplied by the output capacitor.

(a)

(b)

(c)

(d)

Fig. 6.2.15 Operation of Power Stage: (a) Phase 1, (b) Phase 2, (c) Phase 3, (d) Waveforms of Drive Signals and Inductor Current

6.2.4 Optimum On-Time across Input Range

One important design parameter in the DITOB is on-time. In this section, the optimum on-time is derived that maximizes the conversion efficiency and yet fulfill the output ripple requirement.

In phase 1, as shown in Fig. 6.2.15 (a) and (d), the duration that $M_{IN,i}$ and M_3 are both turned on is defined as on-time, t_{on} . Ignore the voltage drop across the switches, the relationship between t_{on} and output ripple is derived as follows.

$$I_{pk} = \frac{V_{in}}{L} \times t_{on} \quad (6.2.4)$$

In phase 2, the duration that M_2 and $M_{OUT,i}$ are both turned on is defined as off-time, t_{off} .

$$t_{off} = \frac{I_{pk} \times L}{V_{out}} = \frac{\frac{V_{in}}{L} \times t_{on} \times L}{V_{out}} = \frac{V_{in} \times t_{on}}{V_{out}} \quad (6.2.5)$$

Total charge that is transferred to output during phase 2, Q_{out} , can be obtained by calculating the total area under i_L curve during phase 2.

$$\begin{aligned} Q_{out} &= 0.5 \times I_{pk} \times t_{off} \\ &= 0.5 \times \left(\frac{V_{in}}{L} \times t_{on} \right) \times \frac{V_{in} \times t_{on}}{V_{out}} = \frac{(V_{in} \times t_{on})^2}{2 \times L \times V_{out}} \end{aligned} \quad (6.2.6)$$

The ripple voltage can then be calculated as

$$V_{ripple} = \frac{Q_{out}}{C_{out}} = \frac{(V_{in} \times t_{on})^2}{2 \times L \times V_{out} \times C_{out}} \quad (6.2.7)$$

In [147], t_{on} is fixed across the input range, which makes the output ripple proportional to (V_{in}^2) with the inductor and capacitor selected. To fulfill the output

ripple requirement across the input range, t_{on} needs to be designed based on the maximum input voltage. When input voltage is low, output ripple is smaller with same t_{on} . However, the energy transferred within one cycle also becomes less, resulting in more frequent switching to supply the load current. As a result, the efficiency at low input voltage is not optimum.

From (6.2.7), it can be seen that to keep the same ripple voltage with different V_{in} values, t_{on} should be inversely proportional to V_{in} , or $(V_{in} \times t_{on})$ should be constant.

6.3 Optimum On-Time Circuit Design

In this section, the circuit block that realizes the required V_{in} and t_{on} relationship derived in previous section is explained. Simulation result of the designed on-time generator is presented.

Fig. 6.3.1 shows the simplified block diagram of the on-time generator. A charging current, I_{CH} , is used to charge capacitor C_0 . The voltage at C_0 is compared to a reference voltage, V_{REF} . When the on-time generator block is disabled, DIS signal is pulled high, which pulls V_C and the output of the on-time generator T_{ON_OUT} to be low. Under this condition, the output of the comparator stays high.

When the on-time generator is activated, DIS becomes low, since the comparator output is high, T_{ON_OUT} becomes high. I_{CH} starts to charge up C_0 . The voltage V_C increases with the slope (I_{CH} / C_0) . When V_C becomes higher than V_{REF} , the output of the comparator will become low, which will set T_{ON} to be low.

The time duration, t_{on} , that T_{ON_OUT} is high is determined by (6.3.1).

$$t_{on} = \frac{C_0 \times V_{REF}}{I_{CH}} \quad (6.3.1)$$

To make V_{in} inversely proportional to t_{on} , or $(V_{in} \times t_{on})$ constant,

$$V_{in} \times t_{on} = V_{in} \times \frac{C_0 \times V_{REF}}{I_{CH}} = \text{const} \quad (6.3.2)$$

In (6.3.2), since C_0 and V_{REF} are constant, to make $(V_{in} \times t_{on})$ constant, I_{CH} needs to be proportional to V_{in} . This is the characteristic of a voltage-to-current converter, or VI converter.

Fig. 6.3.1 Block Diagram of On-Time Generator

One way to implement VI converter is to by using op-amp, as shown in Fig.

6.3.2.

Fig. 6.3.2 Op-Amp Based VI Converter

By connecting the negative input of op-amp to its output through a source follower, the negative input terminal is forced to have the same voltage as V_{IN} due to feedback. Hence, the current through resistor R_0 is (V_{IN}/R_0) . After current mirror formed by MP_0 and MP_1 , the output current becomes (V_{IN}/R_0) . The problem with the op-amp based VI converter includes higher biasing current, stability concern, start-up delay and silicon area.

In [152], a simple VI converter structure by using two non-ideal converters has been proposed, which is shown in Fig. 6.3.3. The non-ideal VI converter is formed by cascading a PMOS source follower and a NMOS common source structure with source degeneration resistor. To enable a ground-compatible input range, V_{SG} of the PMOS source follower needs to be always larger than V_{GS} of the NMOS common source structure.

Fig. 6.3.3 VI Converter by Summing Two Non-Ideal VI Converter Outputs

From Fig. 6.3.3,

$$I_1 = \frac{V_{in} + V_{SG,MP3} - V_{GS,MN1}}{R_s} \quad (6.3.3)$$

$$I_2 = \frac{V_{SG,MP0} - V_{GS,MN0}}{R_s} \quad (6.3.4)$$

$$I_{OUT} = I_1 - I_2 = \frac{V_{in}}{R_s} + \frac{V_{SG,MP3} - V_{GS,MN1} - V_{SG,MP0} + V_{GS,MN0}}{R_s} \quad (6.3.5)$$

Since MP0 and MP3 have the same drain current, I_{bias} ,

$$V_{SG,MP0} \approx V_{SG,MP3} \quad (6.3.6)$$

Hence

$$I_{OUT} = I_1 - I_2 \approx \frac{V_{in}}{R_s} + \frac{-V_{GS,MN1} + V_{GS,MN0}}{R_s} \quad (6.3.7)$$

However, MN1 and MN0 have different drain current, hence there is always a small error term in the converter current output. Since I_1 is always larger than I_2 , $V_{GS,MN1}$ is larger than $V_{GS,MN0}$, hence the error is negative.

To mitigate the error term, a new VI structure has been proposed to converter the input voltage of DC-DC converter to current, which is shown in Fig. 6.3.4. Current flowing through $R0$ in Fig. 6.3.4 can be calculated as follows:

$$I_{R0} = \frac{V_{in} - V_{GS,MN3}}{R0} \quad (6.3.8)$$

I_{R0} is then mirrored to MN4 and MN2, respectively. Current flowing through $R1$ can be calculated as follows.

$$I_{R1} = \frac{V_{GS,MN0}}{R1} \quad (6.3.9)$$

Hence the output current of the proposed VI converter can be calculated as follows, assuming all the current mirror ratios are 1.

$$\begin{aligned}
 I_{out} &= I_{R1} + I_{R0} \\
 &= \frac{V_{GS,MN0}}{R1} + \frac{V_{in} - V_{GS,MN3}}{R0} = \frac{V_{in}}{R0} + \frac{V_{GS,MN0} - V_{GS,MN3}}{R0} \quad (6.3.10)
 \end{aligned}$$

Fig. 6.3.4 Proposed VI Converter

Since MN0 and MN3 have the same drain current,

$$V_{GS,MN0} \approx V_{GS,MN3} \quad (6.3.11)$$

$$I_{out} \approx \frac{V_{in}}{R0} \quad (6.3.12)$$

To mitigate the secondary effect, MN1 is using a native NMOS transistor, which is sized to have roughly 0 V across its gate to source, hence MN0 and MN3 have almost equal drain to source voltages as well, which effectively reduce the body effect.

Fig. 6.3.5 shows the cross-sections of NMOS, PMOS and native NMOS transistors in a typical CMOS process [153]. Unlike NMOS that is sitting on a relatively highly doped p-well, native NMOS sits directly on the lightly doped

substrate. As shown, there is no additional mask needed to construct native NMOS in a standard CMOS flow. Due to the fact that the P-substrate doping concentration is low, the channel in native NMOS is easier to be inverted, hence its threshold voltage is much lower than normal NMOS.

Fig. 6.3.5 Cross-Sections of NMOS, Native NMOS and PMOS in a Typical CMOS Process [153]

The minimum operating voltage for the proposed VI converter is that V_{in} needs to be higher than $V_{GS,MN3}$, which is normally the case in buck converters.

6.4 Simulation Result

The designed VI converter is designed and simulated using 0.18 μm CMOS process. Fig. 6.4.1 shows the current versus input voltage waveform by sweeping input voltage from 0V to 3.3V. It could be seen that when input voltage is more than 2 V, the output current shows good linearity with input voltage change. The minimum operational voltage of the proposed VI converter is the sum of V_{GS} of MN0 and V_{SG} of MP2, as shown in Fig. 6.3.4. The threshold voltage of this process is about 0.7 V, hence the proposed VI converter needs about 1.8V for it to operate properly. When input voltage is less than this required voltage range, the output current is still monotonic, however, the non-linearity is observed due to the fact that $V_{GS,MN3}$ term in (6.3.8) is not properly canceled out.

Fig. 6.4.1 V/I Converter Output Versus Input with Different Temperatures

Fig. 6.4.2 shows the on-time generator output, V_{out} , when input voltage, V_{dd} , is ramping from 2 V to 3.3 V in 33 μ s time, which clearly shows that the on-time is reversely proportional to input voltage.

Fig. 6.4.2 Transient Simulation Result with Vdd Ramping

6.5 Experiment Result

To verify the operation of adaptive on-time control with respect to input voltage, a test chip has been designed and fabricated. The majority of the functional blocks are re-used from the previous chip [147] except the Adaptive On-Time Generator block (as shown in Fig. 6.2.1) which has been redesigned to provide variable on-time according to the operation discussed in Section 6.3. The process used is 0.18 μm CMOS 6-metal dual-gate-oxide process. The total area including bond pads occupies an area of 2.15 mm $\times$ 2.15 mm. The photo-micrograph of the test chip is as shown in Fig. 6.5.1.

Fig. 6.5.1 Die Photo of Test Chip with Adaptive On-Time Control

The input range verified is from 2.65 V to 3.3 V. The on-time control circuit discussed in Section 6.3 is capable of operating with power supply as low as 2.0 V, however, the test chip has a built-in input voltage detection threshold of about 2.6 V, which prevents the measurement below 2.6 V input voltage. The 3.3 V upper limit is due to the process breakdown voltage.

Fig. 6.5.2(a) shows the waveforms of output voltage, V_X (switching node as shown in Fig. 6.5.1), and system clock respectively with 3.3 V input and 100 μ A load current. The pulse width of V_X is determined by the on-time, which is measured to be about 600 ns. Fig. 6.5.2 (b) shows a zoom-out image of the same setting. The frequency of V_X is 1.6 kHz and the output ripple is about 20 mV. For 3.3 V, the on-time is the same with or without adaptive on-time control enabled since it is the highest voltage and adaptive on-time uses it as the starting point to adaptively vary the on-time when input becomes lower.

The same test was done for 2.65 V input with and without adaptive on-time control enabled, which are shown in Fig. 6.5.3 and Fig. 6.5.4 respectively. It can be seen with fixed on-time of 600 ns, the ripple voltage is about 10 mV and V_X switching frequency is at about 2.6 kHz in average. With adaptive on-time control enabled, the on-time is extended to 750 ns. As a result, the ripple voltage increases to about 20 mV and switching frequency of V_X reduces to about 1.5 kHz.

(a)

(b)

Fig. 6.5.2 Output Waveforms with $V_{bat}=3.3V$ and $I_{load}=100\mu A$: Ch2: V_{I8} ; Ch3: System Clock; Ch4: V_x

(a)

(b)

Fig. 6.5.3 Output Waveforms with $V_{bat}=2.65V$ and $I_{load}=100\mu A$ using Fixed On-Time:
Ch2: V_{18} ; Ch3: System Clock; Ch4: V_x

(a)

(b)

Fig. 6.5.4 Output Waveforms with $V_{bat}=2.65V$ and $I_{load}=100\mu A$ using Adaptive On-Time: Ch2: V_{18} ; Ch3: System Clock; Ch4: V_x

The conversion efficiency result is shown in Fig. 6.5.5, with load current fixed at 100 μA and the input is swept from 2.65 V to 3.3 V. With adaptive on-time enabled, due to less switching at lower input voltage, the efficiency at 2.65 V is improved by about 1 %.

Fig. 6.5.5 Conversion Efficiency under Various Input Voltages with Fixed On-Time And Adaptive On-Time Control

After that, the response of a load change was evaluated. I_{18} was increased from 2 μA to 180 μA (Fig. 6.5.6a) and then decreased from 180 μA back to 2 μA (Fig. 6.5.6b). As shown in Fig. 6.5.6a, V_{18} initially dropped approximately 30 mV when I_{18} was increased as the converter could not supply enough power to V_{18} . In response to the drop in V_{18} , the converter increased its SYS_CLK frequency so as to increase its output power, which recovered V_{18} to its targeted voltage of 1.8 V. When I_{18} returned to 2 μA , large voltage transient was not seen at V_{18} because the converter started to skip pulses when V_{18} was above its threshold of 1.8 V. Fig. 6.5.6(a) and 6.5.6(b) clearly illustrated the progressive increase and decrease in SYS_CLK frequency respectively.

(a)

(b)

Fig. 6.5.6 V_{18} Rail Load Step Response: A) Light Load to Heavy Load; B) Heavy Load to Light Load

6.6 Summary

In this section, the use of adaptive on-time control in ultra-low power energy harvesting application is demonstrated on a DITOBB converter. The proposed DITOBB converter adjusts the wake-up timer frequency adaptively to the load requirement. To provide the required frequencies to the wake-up timer, a low-power relaxation oscillator is developed and characterized. A constant output voltage ripple across input range optimizes the efficiency since switching activity is minimized. The relationship between the optimum on-time and input voltage is derived. It is found that the optimum on-time should be reversely proportional to the input voltage. A circuit that realizes optimum on-time is designed based on a new VI converter structure which requires no op-amps and eliminates first order mismatches. A test chip has been developed and the measurement result shows about 1 % improvement in the conversion efficiency at $V_{IN} = 2.65$ V with the proposed adaptive on-time control.

The silicon area for the adaptive on-time generator is about 4800 μm^2 , which is about 0.48% of the total control circuit area. Hence 1% efficiency improvement with such a small area overhead is still significant.

Chapter 7 Conclusions and Recommendations for Future Work

7.1 Conclusions

The recent development in communication network and mobile broadband has made the connections between individuals and outside world closer than ever before, which triggers huge demands for battery-operated portable equipment, like smart phones and tablet PCs. Battery capacity is limited by its size and its output voltage reduces with usage time. To extend battery time, portable devices are often designed to have multiple operating modes depending on whether the device is active or in standby, which has brought great challenges to the built-in power management unit. The PMU needs to provide regulated supply voltages to internal functional blocks, which are often dynamically changed. At the meantime, the current demands of the internal functional blocks are also changing widely and quickly. So the PMU is required to not only maintain high efficiency over different input voltage and load current conditions to prolong battery life, but also to be versatile to deal with transients. The heart of PMU is usually voltage regulators that converts the varying battery voltage to well-regulated voltages.

Adaptive on-time (AOT) control is a powerful DC-DC control method due to its simple structure and good light load efficiency. The purpose of this research is to look into the development of AOT control in two areas: digital control and ultra-low-power operation, which would improve the performance of power management in battery-operated devices and low power sensor networks.

Digital control of DC-DC converter opens new possibilities to take the advantage of continued process scaling, which improves the performance of the transistor and reduces its cost. The existing analog control, however, shows good

output voltage accuracy and proven operation, and is still the dominating DC-DC control in the industry. To fully reap the benefit of the digital control, several improvements over the state of the art are necessary. First objective of this study is to look into control methods that could aid the transition from analog control to digital control. Digital adaptive on-time (DAOT) control is a very promising control method due to the fact that it does not need a high resolution DPWM or compensator, which are the two roadblocks to digital control. This research is focused on the implementation of DAOT control and the improvement of its performance by using digital techniques.

Energy harvesting is an important technique for improving the operational time of remote sensor network. The energy harvested from the environment is usually stored in a back-up battery and regulated to bias the functional blocks in the sensor system. The efficiency of energy harvesting, storing and management is of paramount importance, which requires new control methods to minimize the power management IC quiescent power. The other focus of this research is to look into the application of AOT control in ultra-low-power operations.

ADC converts the output of DC-DC converter to digital code for further digital processing. It is a crucial functional block in the digital control scheme. However, an overly power hungry or complex ADC could reduce or even eliminate all the benefits that the digital control may have. In Chapter 3, a new flash ADC structure based on Threshold Inverter Quantization (TIQ) has been developed. The basic principle is to use digital gate as comparator. One problem with this approach is that when the input is near to the threshold of the digital gate, there will be large shoot-through current in the logic gates since both the pull high and pull low transistors are active. A dynamic hysteresis scheme was introduced by using NOR

gate to reduce the current consumption.

AOT is inherently fast during load stepping. However, its response to load dumping is slow. The flash ADC provides the output profile during load transient, which could be used to optimize the load transient response. Two methods are proposed and verified in Chapter 4. Level based load transient recovery algorithm is able to achieve near minimum voltage overshoot/undershoot. Body-brake further improve the unloading transient response.

To improve the efficiency over the whole operating range, two methods have been developed to improve the efficiency during heavy load and light load, respectively.

For heavy load, to improve the dead-time control, a counter-based peak efficiency seeking method was proposed in Chapter 5. This method is based on the observation that during steady state, the switching frequency of the DAOT is lowest when the dead-time is minimized.

For extremely light load, in Chapter 6, we develop a method of duty-cycled operation that dynamically changes the system operation frequency with a low-power relaxation oscillator, which is suitable for energy harvesting applications. To further improve the system power efficiency, an adaptive on-time control has been developed, which regulates the on-time based on input voltage. For same ripple requirement, the proposed method improves the overall efficiency across different input voltages.

In conclusion, to address the efficiency and versatility requirements of portable applications and energy harvesting applications, AOT control has been developed in this research work for practical implementation in two areas: digital control and ultra-low-power operation.

7.2 Recommendations for Further Research

7.2.1 Optimize Encoder Design for TIQ ADC

A conventional ROM type encoder was used in the proposed TIQ ADC. The encoder delay in the proposed TIQ ADC limits the achievable conversion speed. Thus it is needed to research on efficient and fast encoder structure to further improve the conversion time.

7.2.2 Temperature Insensitive Relaxation Oscillator Design

The relaxation oscillator developed is sensitive to temperature. As indicated by (6.2.3), the temperature sensitivity of the oscillator is determined by the threshold voltage temperature variation, as well as the bias current temperature characteristics, which varies from process to process. To extend the design to other applications, the temperature characteristic of the propose relaxation oscillator need to be analyzed and improved. One possibility is to look into biasing current which can compensate the temperature variation of the proposed structure.

7.2.3 DAOT Control Stability Improvement

AOT control is sensitive to external component parasitic. Therefore, it is recommended to look into reducing sensitivity to external component by using digital techniques.

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Appendix A: Reference Tracking

DVS has been extensively used as an effective technique that dramatically reduces energy consumption in high performance digital systems [106] [154].

Battery operated system usually does not operate in full power mode all the time. Most of the time, it is idling and waiting for commands. To preserve the battery energy, when the system is in idling or standby mode, most of the functional blocks will be turned off. The supply voltage is also dropped to a level that is just enough for blocks that needs power even when other blocks are idling. One such block is memory, which needs voltage supply to keep the information it stores. Another benefit of dropping the voltage at standby is that the quiescent current and leakage current are reduced.

When the system receives command and needs to operate in high power mode, it will demand a higher operating voltage. As such, it will send a new voltage command to the DC-DC converter to raise its output voltage. DC-DC converter can do so by either increasing its reference voltage or increasing its resistor divider ratio, both of which are defined as reference tracking here. This situation is different from load transient. The new output voltage of the DC-DC converter could be much higher, which changes the operating point of the DC-DC converter. The small ripple approximation is not suitable in this case. The output of DC-DC converter will need to settle to the new value in short time so that the digital IC connected to it can enter high power mode to handle the tasks required.

On the other hand, when the system is changing from high power mode to standby, it will send a lower target value to the DC-DC converter. Since the output voltage is higher than target now, feedback loop will force the duty cycle to reduce to zero and stop switching. Under DAOT control, the off-time will extend. Usually

it is OK to let the output of DC-DC to ramp down to the low target value by the load since the charge has been stored in the capacitor already.

For DC-DC converters with analog control, End-point prediction (EPP) has been proposed to predict the position of control signal (usually is the output of the error amp) for a new reference voltage for V^2 control [154] and voltage mode PWM control [108], which shows improvement over linear control loop.

In this section, reference tracking response for the DAOT controlled DC-DC converter is investigated. The optimum on-time and off-time which could bring the output to the new value within one switching cycle are derived. An implementation using LUT has been proposed and discussed.

A.1.1 Optimum reference tracking

To analyze the reference tracking response, the output to reference voltage ratio is assumed to be N . This is realized by setting the feedback resistor divider ratio to be N . The load is assumed to be a constant current sink, I_{load} .

As shown in Fig. A.1.1, before time t_0 , the output is in steady state with the reference voltage being V_{REF0} and output voltage being V_{OUT0} . Here

$$V_{OUT0} = N \times V_{REF0} \quad (A.1.1)$$

Assume at time t_0 , a new reference voltage V_{REF1} is commanded. Hence the output voltage will need to rise from V_{OUT0} to V_{OUT1} , where

$$V_{OUT1} = V_{OUT0} + N \times (V_{REF1} - V_{REF0}) \quad (A.1.2)$$

The most optimum transition will be turning on high side switch fully from t_0 to t_1 , and then turning it off from t_1 to t_2 , such that at t_2 , the output voltage reaches the new voltage V_{OUT1} while the inductor current, $I_{inductor}$, goes back to I_{load} .

Fig. A.1.1 Optimum Reference Tracking Response

When the output voltage changes from V_{OUT0} to V_{OUT1} , the additional charges needed on the output capacitor is

$$\Delta Q = C_{OUT} \times \Delta V = C_{OUT} \times (V_{OUT1} - V_{OUT0}) \quad (A.1.3)$$

The additional charge on the output capacitor comes from the difference between inductor current and load current. As shown in Fig. A.1.1, the area of A, which is the integral of difference between inductor current and load current, is equal to the increase in output capacitor charge.

To simplify the derivation, the output voltage is assumed to be constant at V_{out} . Hence, the inductor current slope is constant during ramping up and ramping down,

as shown in Fig. A.1.2.

Fig. A.1.2 Optimum Reference Tracking Response with Approximated Linear Inductor Current Slope

With this approximation, between time t_0 to t_1 , the inductor current slope can be calculated as (A.1.4), where V_{in} and V_{out} are the input and output voltage respectively, and L is the inductance value.

$$\frac{d[I_{inductor}(t)]}{dt} = \frac{V_{in} - V_{out}}{L} \quad (A.1.4)$$

Between time t_1 to t_2 , the inductor current slope can be calculated as (A.1.5).

$$\frac{d[I_{inductor}(t)]}{dt} = \frac{-V_{out}}{L} \quad (A.1.5)$$

At time t_1 , the inductor current reaches peak value. The difference between

the peak inductor current and load current can be calculated in (A.1.6) by neglecting the inductor current ripple under steady state.

$$I_{inductor}(t_1) - IL = \frac{V_{in} - V_{out}}{L} \times (t_1 - t_0) = -\frac{V_{out}}{L} \times (t_2 - t_1) \quad (A.1.6)$$

$$\frac{t_1 - t_0}{t_2 - t_0} = \frac{V_{out}}{V_{in}} \quad (A.1.7)$$

The area of A in Fig. A.1.2 can be calculated by (A.1.8).

$$A = \frac{1}{2} \times (t_2 - t_0) \times (I_{inductor}(t_1) - IL) = \frac{1}{2} \times (t_2 - t_0) \times \frac{V_{in} - V_{out}}{L} \times (t_1 - t_0) \quad (A.1.8)$$

Since the area of A is equal to the additional charge on the output capacitor, from (A.1.3) and (A.1.8), the following can be obtained.

$$\frac{1}{2} \times (t_2 - t_0) \times \frac{V_{in} - V_{out}}{L} \times (t_1 - t_0) = C_{OUT} \times \Delta V \quad (A.1.9)$$

$$(t_2 - t_0) = \frac{2 \times L \times C_{OUT} \times \Delta V}{(V_{in} - V_{out}) \times (t_1 - t_0)} \quad (A.1.10)$$

Substitute (A.1.10) into (A.1.7) and re-arrange,

$$(t_1 - t_0) = \sqrt{\frac{2 \times L \times C_{OUT} \times \Delta V}{(V_{in} - V_{out}) \times \frac{V_{in}}{V_{out}}}} \quad (A.1.11)$$

$$(t_2 - t_1) = (t_2 - t_0) - (t_1 - t_0) \quad (A.1.12)$$

From the above derivation, the optimum switching on-time can be calculated from (A.1.11), and the optimum switching off-time can be calculated from (A.1.12). The following parameters are required in this calculation: inductor value (L), capacitor value (C_{OUT}), input voltage (V_{in}), output voltage (V_{out}) and voltage step (ΔV). V_{out} is assumed to be constant during the reference tracking process,

and the optimum value should be between the initial value (V_{OUT0}) and final value (V_{OUT1}).

To verify the derived result, the following simulation has been set up. The simulation result is as shown in Fig. A.1.3. It can be seen that with normal DAOT control (Fig. A.1.3 (a)), there is an overshoot of 66.1 mV during reference tracking. The reason of this overshoot is due to the fact when the control loop tries to bring the output voltage to the new target value, the inductor current is built up. After the output voltage reaches the new target value, the switching is stopped, but the inductor current discharges into the output capacitor and causes overshoot. Whereas with the calculated on/off time (Fig. A.1.3 (b)), the output voltage reaches the new target value while the inductor current goes back to the previous level, hence there is no overshoot.

TABLE A.1.1 DAOT Simulation Parameters for Reference Tracking

Supply voltage	3.3 V
Load current	300 mA
Ton (typical)	20 ns
Output capacitor	4.7 μ F (ESR = 30 m Ω)
Output inductor	2.2 μ H (DCR = 10 m Ω)
Output voltage	1 V to 1.1 V

A.1.2 Implementation of optimum reference tracking

Direct implementation of (A.1.10), (A.1.11) and (A.1.12) involves subtraction, multiplication, division and square-rooting, which may not be practical for systems without a digital signal processing unit. If the coefficients are all multiples of 2, or 1/2, multiplication can be done by logic shifters [155].

(a)

(b)

Fig. A.1.3 Simulated Reference Tracking Response: (a) Normal DAOT; (b) DAOT With Calculated On/Off Time

Another way to implement the optimum on/off time during reference tracking is by using LUT method. The use of the look-up tables occupies smaller silicon area when the number of entries is limited and is suitable for low-power, high frequency operations [59, 64, 68].

When LUT method is used, the on time and off time are calculated based on the formula derived and stored in registers. When an output voltage change request is received, based on the current output voltage and the new output voltage, proper on time and off time are read from the LUT and applied to the adaptive on-time DC-DC controller.