Development of high efficiency power electronics converter for medium voltage drive

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DEVELOPMENT OF HIGH EFFICIENCY POWER
ELECTRONICS CONVERTER FOR MEDIUM VOLTAGE
DRIVE**

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SCHOOL OF ELECTRONIC AND ELECTRICAL ENGINEERING

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Abstract

Use of Medium Voltage (MV) converters for high power motor drives application has gained a huge attention at present. Excellent speed control of the motor and the reduction of the energy loss in the system are the main attraction of these drives. These MV converters are widely used in industries for driving pumps, fans and propulsion system on ships. The advent of the higher voltage and high power application has made the study of multilevel converters for medium voltage drives application much more attractive. Multilevel Converters have far less harmonics than the 2 level converters for a given switching frequency and has very less distortions in the input current. In addition to this, the use of IGBTs in Multilevel converters helps in reducing the system loss thereby increasing the efficiency. Also the use of IGBT helps in increase system power density.

In this study MV converters from 3.3kV to 6.6kV have been considered. These converters would be feeding a 1MW squirrel cage induction motor.

The performance comparison has been done by computing and comparing the losses of different topologies with different current and voltage ratings of the IGBTs. In addition to the evaluation of losses, the impact on the power quality has also been analyzed for the multilevel converters and compared with the standard limits.

The purpose of this thesis is to compute the thermal losses of different topologies of MV multilevel converters and compare their efficiencies and to select the most efficient topologies for MV application. For this study, advanced topologies for MV drive application viz. Neutral Point Clamping and Cascaded H-Bridge Multilevel Converters topologies were reviewed and power loss model of each topology was established for different voltage levels. The converters are then simulated at different switching frequencies and are compared on the basis of the power losses and power quality.

The model of these topologies was built in Piece-wise Linear Electrical Circuit Simulation (PLECS) 3.6.3 software.

Keywords: Voltage Source Converters, Multilevel Converter, Thermal Losses, Efficiency.

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1. Introduction

1.1 Medium Voltage Drives

The advent of Gate Turn-off Thyristors (GTO) and high-power insulated gate bipolar transistors (IGBTs) has paved the way for the evolution of medium voltage drives and high-power converters. Because of the reduced switching losses, easiness in switching, snubberless operation and higher switching frequency, IGBT has been widely used in high power drives application. Generally the drives with the power ratings ranging from 1- to 4-MW with the voltage level in between 3.3 kV to 6.6 kV falls under the Medium Voltage Drives.

These MV drives have found their application in the fields of traction application in transportation sector, marine application, conveyor drive system in cement industries, petroleum and chemical industry and other fields.

Although, for the last few decades, the use of MV drives for the industrial application has been increasing, till date only 3% of the total MV motors use MV drives where as rest of the MV motors still use fixed speed system. This shows that there is a huge potential of MV drives for the coming days[1].

These drives systems not only help in speed regulation of the MV motors but also reduce the significant amount of energy loss. Reduction in energy loss leads to the savings on energy cost with a payback time of one to two years.

Figure 1-1 shows a general block diagram of a Medium Voltage drive system.

Figure 1-1 General Block Diagram of MV Drive

Application of the motor side filter and line side filter depends on the requirement of the system and the employed converter type. Multiple winding phase shifting transformer can be used to reduce the current harmonics.

This ac voltage can be converted to dc of fixed or adjustable value by using the rectifier. Diode rectifier or PWM rectifiers can be used depending on the requirements. To assure that a stiff dc voltage is fed into the inverter, a dc filter can be used. A capacitor can be used to provide this stiff dc voltage.

This dc voltage is now applied across a Voltage Source Inverter (VSI). The applied dc voltage can now be converted into the adjustable three phase ac voltage by the VSI. Depending upon the A variety of inverter topologies have been developed for the MV drive, depending upon the requirement.

1.2. Classification of Converters for High Power Drives:

Classification of converters used for high power drives application has been shown in figure 1-2. These high power drives can be divided into two parts viz. Direct and Indirect topologies[2]. Direct topology, as the name suggest directly connects the load to the source in one stage through power semiconductor devices. Cycloconverter is a very good example of the direct conversion converters. Indirect topologies on the other hand, deliver the power in two different stages viz. rectification and inversion. It is further classified into two groups, current source and voltage source converter topologies.

Figure 1-2 Classification of converters for high-power drives

Current Source Inverter (CSI) can be further divided into two topologies, the load commutated inverter (LCI) and the Pulse Width Modulation CSI.

But in this study we mainly focus on the high-power Voltage Source Inverters (VSI). These VSI fed drives occupy a very high market share in High power drives and hence attracts more research interest than other converter types. With the classical 2L-VSIs having their application limited to the low and medium power drives due to the voltage limits of the power semiconductor, concept of Multilevel Inverter has been developed. In these Multilevel Inverter Topologies, the switching devices are arranged in series such that the voltage stresses are distributed evenly in them. This allows the multilevel converters to be used in high power drives application. Another advantage is that the quality of output variables are much better in Multilevel Inverter than in 2L VSI.

Multilevel Converters and their types are further discussed in Chapter 2.

2. Multilevel Converters

2.1. Introduction to Multilevel Inverters

With the advent of higher power electrical apparatus, need of use of medium voltage converter has been a big necessity. But the use of conventional 2 Level converter topology where the entire voltage is subjected on only one power semiconductor switch is very difficult. So, Multilevel converters are used when there is a need of high power and medium voltage application[3].

These inverters comparatively contain more number of power semiconductor switches and capacitors than the 2 Level converters. Likewise the output voltages obtained from the multilevel inverters are of more than 2 Levels which increase their resemblance to the sine waveform. A [4] schematic diagram of one phase-leg of inverter with different level-numbers has been shown in Figure 2-1. Converter shown in Figure 2-1 (a) produces two voltage levels ($+V_a$ and 0). Similarly the 3 Level converter shown in Figure 2-1 (b) can generate 3 Level of output voltages waveforms ($-V_a$, 0 and $+V_a$) and so on. So, multilevel converter can produce several number of output voltages. Additionally, these converters can produce higher output voltages without overstressing the power semiconductor switches.

Figure 2-1 One phase leg of an inverter: (a) Two levels, (b) Three levels, and (c) n levels

2.2. Advantages and Disadvantages of Multilevel Converters:

Following are the advantages of Multilevel Converters:

- 1) ML converters can generate the output voltages with considerably low distortion and lower order harmonics.
- 2) ML converters draw input current with a very low distortion.
- 3) ML Converter switches can operate with the less switching frequency. Hence lower switching losses.
- 4) Secondly, the dv/dt of switches is low since the switches endure reduced voltage.

- 5) By using the advanced methods, common-mode voltages problem can be eliminated in ML converters.

Because of their attractive features over the 2 Level converters, multilevel inverters are being used in wide domain ranging from [5]MV drives application to the FACTS devices applications such as in UPFC, SVC, STATCOM etc.

The main disadvantage of multilevel converters is that they need more number of power semiconductor switches than the two level converters. Each of these switches needs to be operated with a separate gate drive circuit. So it increases the complexity and overall cost of the system.

2.3. Classification of Multilevel Converters:

In this research, we only focus on the multilevel inverter part of the drives. And particularly, for this study, 3 Level Neutral Point Clamping and Cascaded H-Bridge Multilevel Converter (2 cells and 4 cells) topologies were considered as they are the most established and commercialized multilevel inverter types[6].

2.3.1. Neutral Point Clamping Converter:

A 3 Level Neutral Point Clamped inverter is shown in Figure 2-2. The bulk capacitors C_1 and C_2 split the dc-bus voltage into 3 levels[7]. n , the middle point of two capacitors, is considered to be the neutral point. For the applied dc bus voltage of $2E$, capacitors C_1 and C_2 share the dc bus voltage equally so that the voltage across each capacitor is E .

Figure 2-2 Neutral Point Clamped multilevel inverter circuit topology

The main difference between NPC 3Level converter and conventional 2 Level inverter is the presence of diodes D_1 and D_2 [4]. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When S_1 and S_2 switches are turn on, the voltage across port a and o is same as the dc bus voltage i.e., $v_{ao} = 2E$. This dc voltage is imposed on lower switches $S_{1'}$ and $S_{2'}$. The sharing of the voltage between the lower two switches $S_{1'}$ and $S_{2'}$ is balanced out by diode $D_{1'}$.

This makes the switch S_1 , only needing to block the voltage across C_1 . Similarly, the switch S_2 , sharing the voltage stress across capacitor C_2 . So because of these two clamping diodes, each device is only subjected to share the voltage stress of E rather than the entire bus voltage.

It can be seen that the output leg voltage v_{an} will have three levels viz. $-E$, 0 and E .

Switching states of the NPC 3 Level Converter to achieve three different voltage levels have been shown in Table 2-1.

Switches ON	Switches OFF	Output Voltage
S_1, S_2	S_3, S_4	$+E$
S_2, S_3	S_1, S_4	0
S_3, S_4	S_1, S_2	$-E$

Table 2-1 Switching States of NPC 3 Level Converter

2.3.1.1. Modulation Technique Used in NPC Converter:

Widely used modulation techniques in industries are carrier based sine triangle modulation which is based on the arrangements of multiple carrier waves in vertical shifts. For this NPC converter topology, modulation technique called “Phase-Disposition Pulse Width Modulation (PD PWM)” has been used since it has been known that this technique gives the lowest harmonic distortion among all the carrier-based sine-triangle modulation technique[8].

In general, for an n level NPC converter, $n-1$ phase matched triangular carrier waves are arranged in a vertical manner. Arrangements of carrier waves are in such a way that they fully occupy contiguous bands inside the normalized range between $+1$ and -1 . Then a single-reference sine wave for each phase is compared with these carrier waves which decide the switching of each of the phase legs.

Figure 5 illustrates the Phase-Disposition Pulse Width Modulation (PD PWM) technique for 3 Level NPC converter and the output voltage waveform.

Figure 2-3 Phase-Disposition Pulse Width Modulation (PD PWM) technique for Three Level NPC Converter

2.3.1.2. Advantages and Disadvantages of NPC Topology

Following are the advantages of Neutral Point Clamping Converter:

- 1) The same DC bus is shared by the three phases of the converter. This significantly reduces the capacitive requirement of the converter. So the use of back to back topology is very much feasible in this case.
- 2) Since less IGBT switches are involved, the so total losses across the switching components are also less.

Following are the disadvantages of Neutral Point Clamping Converter:

- 1) The number of clamping diodes will increase if the number of voltage levels is to be increase. This makes the converter topology quite complex for the higher level.
- 2) Since the DC link provides path for the flow of active power, the fluctuation of this intermediate DC level by frequent overcharging and discharging causes difficulties in the flow of real power.

2.3.2. Cascaded H- Bridge Converters:

Two Cells Cascaded H-Bridge (CHB) Converter is shown in figure. 6.

Figure 2-4 Cascaded H-Bridge Multilevel Inverter Circuit Topology

In the CHB multilevel converter topology, in every phase legs, the H-bridge units are cascaded upon one another. The arrangements and the connection of the two H-Bridges (HB1 and HB2) in the five-level CHB topology has been shown in Figure 2-4. It can be seen that each H-Bridge with their own source have been connected in series in a modular structure[9].

Each HB is contains 4 IGBTs (referred as S1, S2, S3 and S4) and supplied by a separate dc source. Three output levels, +Vdc, 0 and –Vdc can be obtained from each of the HB. The switching states and the corresponding output voltages for each of the HB are shown in below:

Switches ON	Switches OFF	Output Voltage
S ₁ , S ₂	S ₃ , S ₄	+E
-, -	S ₁ , S ₂ , S ₃ , S ₄	0
S ₃ , S ₄	S ₁ , S ₂	-E

Table 2-2 Switching States of Single H Bridge

The phase-voltage can be obtained by adding the output voltage of each H-Bridges. If the dc link voltages of H-Bridges are same on each cell, the multilevel inverter is called the cascaded multilevel inverter. More the number of H-bridges per phase, more would be the resemblance of the output voltage to sinusoidal waveform.

It can be verified that for n -level topology, the number of identical H- Bridges, b , that are needed in each phase can be calculated by:

$$b = \frac{(n-1)}{2} \quad (2.1)$$

This gives the number of possible voltage levels of output voltage obtained from the b number of H-Bridges:

$$n = 2b + 1 \quad (2.2)$$

It can be seen from the above expression that the number of levels of output voltage obtained from the CHB Converter is always in odd number.

But unlike Neutral Point Clamping Converter, in Cascaded H-Bridge Converter, a separate DC source is needed for each of the individual H-Bridge.

2.3.2.1. Modulation Techniques Used in CHB Converters:

For both 2Cells (5 Level) and 4 Cells (9Level) CHB use Phase-shifted PWM (PS-PWM). This is because of the modular nature of CHB topology. It is possible to independently modulate each cell in a phase using unipolar PWM with the same sinusoidal reference signal[1]. It is necessary to introduce phase shift across all the carrier signals of each cell in order to produce the stepped multilevel waveform. It has been found that when the phase shift between carriers is kept at $\frac{180}{b}$, the distortion produced in the output voltage waveform would be the lowest. Where b = number of cells in each leg of CHB.

Figure 2-5 shows the working principle of seven level CHB converters[1]. It has been found that the inverter-output voltage has b times the fundamental component of each cell. It can be seen that the frequency of the switching pattern of output voltage of the inverter is b times the switching frequency of the cell, as the multiplicative effect has been caused by the phase shift. This fact plays a very important role in analyzing that, because the device switching frequency (hence, the switching losses) is lower by b times the apparent frequency perceived by the load. So, for the same output switching frequency, the switching losses produced by the phase-shifted PWM are b times less as compared to level-shifted PWM. But since the carrier waves are in phase for level-shifted PWM, the distortion in line voltage would be lesser than that with this one.

The total power delivered to the load would be shared equally by the each H-bridge cells, because of the reason that all the cells are controlled with the same reference and the same carrier frequency. This helps in significantly reducing the input current harmonics.

Figure 2-5 Three Cell (Seven Level) Phase Shift PWM waveform generation

2.3.2.2. Advantages and Disadvantages of CHB Topology:

The advantages as well as the disadvantages for using CHB converters are as follows:

Advantages of Cascaded H-Bridge Converters:

- 1) The possible output voltage level is more than twice the number of DC sources employed.
- 2) Because of the fact that each H-bridges are connected in series in each phase, so each H-bridge cells can make for a modularized layout. This in turn reduces the production cost as well as the production time for these converters.

- 3) Each HB can generate three levels of output voltage: $+E$, 0 , and $-E$. So, when two H-Bridges are connected in series, their output voltage can vary as $+2E$, $+E$, 0 , $-E$ and $-2E$. The benefit of this topology over the other is that the number of cells can be stacked up as desired to get the higher output voltage by using much lower dc source voltage.

Disadvantage of Cascaded H-Bridge Converters is that separate DC sources are needed for each cell.

3. Application of PLECS Software for Simulation of the Converter Circuits

PLECS 3.6.3 software is used for simulation of circuits of 3 Level NPC converter and CHB Converters (2 Cells and 4 Cells). The Schematics of both the converter circuits are given in the later part of this section.

The conceptual diagram of the converter topologies varies from the schematic configuration designed for the simulation in software.

3.1. Schematics of Cascaded H-Bridge Converters Using PLECS

As discussed in previous chapter, CHB converter consists of a several units of single phase H-bridge power cells. Each H-bridge is supplied by separate dc voltage sources of same magnitude. The output terminals of the individual H-bridges are connected in series so that the medium voltage operation can be achieved with a low harmonic distortion.

3.1.1. Schematics of 2 Cells Cascaded H-Bridge Converters Using PLECS

Figure 3-1 shows a typical cascaded multilevel inverter where the dc link voltages of each of H-bridge power cells are identical.

i.e. $V_{dc}=V_{dc1}=E$

where E is unit voltage. Each H-Bridge generates three voltages at the output: $+E$, 0 , and $-E$. The resulting output from ac voltage from each legs swings from $-2E$ to $2E$ with five levels. Circuitry for the implementation of Symmetrical PWM has also been shown in the figure.

Similarly if 4 H-Bridge cells used, maximum possible output voltage in each phase ranges from $-4E$ to $+4E$ with 9 levels.

Generally, the required output voltage and the cost of manufacturing determine the number of power cells in a CHB inverter. For example, to develop a CHB inverter with an output voltage (L-L) of 3.3kV with 9 levels of output voltage waveform, total number of H-bridge power cells required is 12. Hence both the output voltage as well as the cost of the inverter depends upon the number of H-bridges employed[5].

A typical waveform diagram for 3.3kV CHB Converter (2 Cells) for the output voltage (Line-neutral), output voltage (Line to Line), current waveform, harmonics of output voltage and harmonics of output current feeding the induction motor load are given in figures 3-1, 3-2, 3-3, 3-4, 3-5, 3-6 respectively.

Figure 3-1 Schematic Diagram of Cascaded H-Bridge Converter (2 Cells)

Figure 3-2 Output Voltage Waveform (L-N) for Cascaded H-Bridge (2 Cells) MLI

Figure 3-3 Output Voltage Waveform (L-L) for Cascaded H-Bridge (2 Cells) MLI

Figure 3-4 Output Current Waveform for Cascaded H-Bridge (2 Cells) MLI

Figure 3 Harmonics of Output Voltage for Cascaded H-Bridge (2 Cells) MLI

Figure 3-6 Harmonics of Output Current for Cascaded H-Bridge (2 Cells) MLI

3.1.2. Schematics of 4 Cells Cascaded H-Bridge Converters Using PLECS

The schematics for the 4 Cell CHB Converter is shown in Figure 3-7 below.

Figure 3-7 Schematic Diagram of Cascaded H-Bridge Converter (4 Cells)

Figure 3-8 Output Voltage Waveform (L-N) for Cascaded H-Bridge (4 Cells) MLI

Figure 3-9 Output Voltage Waveform (L-L) for Cascaded H-Bridge MLI (4 Cells)

Figure 3-10 Output Current Waveform for Cascaded H-Bridge MLI (4 Cells)

Figure 3-11 Harmonics of Output Voltage for Cascaded H-Bridge MLI (4Cells)

Figure 3-12 Harmonics of Output Current for Cascaded H-Bridge MLI (4Cells)

3.2. Schematics of Neutral Point Clamping Converters Using PLECS

Since PLECS software uses ideal components for voltage sources and capacitors, we cannot connect capacitors in parallel to voltage sources during simulation. Instead, voltage source itself has been divided into two equal parts V_{dc} and V_{dc1} as shown in Figure 9. The middle point of these two voltage sources is the neutral point. As described earlier, the output voltage V_{out} has three states E , 0 and $-E$. The diodes connected to the neutral point, $Da5$ and $Da6$, are the clamping diodes.

Switching pattern has already been described for this converter in the earlier chapter.

Since there are three possible output voltages for each phase ($+E$, 0 and $-E$), hence name 3 Level NPC. The line current, line-to-ground as well as the line-to-line voltages can be found by connecting a three phase meter at the output terminals of the converter.

Circuitry for the implementation of Symmetrical PWM has also been shown in the figure.

The PLECS implementation for PD-PWM technique along with the schematic for the modulation of 3 Level NPC converter has been shown in Figure 3-12.

The typical waveform diagram for 3.3kV NPC converter for the output voltage (Line to neutral), output voltage (Line to Line), output current waveform, harmonics of output voltage and harmonics of output current for the induction motor load are given in figures 3-13, 3-14, 3-15, 3-16, 3-17 respectively.

Figure 3-13 Schematic Diagram of Neutral Point Clamping Converter (3 Level)

Figure 3-14 Output Voltage Waveform for Neutral Point Clamping Converter (L-N)

Figure 3-15 Output Voltage Waveform for Neutral Point Clamping Converter (L-L)

Figure 3-16 Output Current Waveform for Neutral Point Clamping Converter

Figure 3-17 Harmonics of Output Voltage for Neutral Point Clamping Converter

Figure 3-18 Harmonics of Output Current for Neutral Point Clamping Converter

4. Application of IGBT in Converter

IGBT has been very popular in power electronic application because of its high power rating, robustness and ease of control. Because of these features of IGBTs, it has been widely implemented to develop the high power MV drives beyond 1 MW rating.

But before the implementation of IGBT, it is very important to study about its electrical and thermal parameters to ensure its safe, effective and efficient application in MV drives. The aim of this study is to determine the best possible rated IGBT for a specific topology and application with regards to these two aspects.

In this study, IGBTs and diodes manufactured by ABB has been studied.

4.1. Selection of Voltage Ratings of IGBT

Choosing the optimum voltage rating of the semiconductors to be used in the power electronic equipment is the most fundamental part of designing the equipment. For example, if the voltage rating of the semiconductor is chosen near to the operating voltage range, then the risk of failure would be very high. This negatively affects the overall reliability of the equipment. On the other hand, if the safety margin is taken too high (i.e much higher voltage rated semiconductor is used) then the overall performance and the efficiency of the equipment is significantly decreased. This is because thicker silicon is required for the higher rated devices which ultimately produce higher losses[10].

Because of 3L connection, the voltage stress on each switch will be half of the DC supplied voltage. So, DC voltage per device:

$$V_{dc} = \frac{V_{nom\ rms} \times \sqrt{2} \times \left(1 + \frac{x}{100}\right)}{2} \quad (4.1)$$

Where $V_{nom\ rms}$ is the nominal line voltage V_{dc}

x is an over-voltage factor which depends on the application and line tolerances.

x ranges typically from 15% (for industrial network) to 20% (for traction network)

The required repetitive voltage rating for the device selection is given by:

$$VDR = V_{dc} \times \left(1 + \frac{y}{100}\right) \quad (4.2)$$

where y is taken as a safety factor which depends on the switching conditions and stray-inductances. Typically, $y=60\%$.

The preferred device rating is then normally selected as the next highest available standard device voltage rating.

For example, to determine the voltage rating the IGBT used in 3 Level converter,

$$V_{nom\ rms}=3300V.$$

$$\text{So, } V_{dc}=2683.5V$$

$$\text{And, } V_{DR}= 4293.55V$$

Hence the rating of the IGBT required is 4500V.

Another method for the selection of device voltage rating is by using PLECS. The peak voltage across device is measured using voltmeter probe. This value is then multiplied by the safety factor. Then device rating is selected as the next highest available standard device voltage rating.

4.2. Current Ratings of IGBTs

While selecting the current rating of the IGBT, it should be noted that the selected IGBT is able to carry the current with its junction temperature not exceeding the limit. The operating junction temperature depends on the thermal impedance, ambient temperature and the semiconductor losses [11]. Also, the current rating of IGBT hugely determines the losses on the IGBT. For example, if the current rating is chosen higher than needed, then the selected IGBT would have higher Silicon area, which implies that there would be a higher value of parasitic capacitance and which leads to the higher switching losses. During this study the IGBT current rating has been selected in such a way that the operating junction temperature doesn't go beyond 85°C.

4.3. Device Current and Voltage Rating Selection for CHB (2 Cells), CHB (4 Cells) and NPC Converters for 3.3kV, 4.5kV and 6.6kV output voltages:

Following table contains the best possible device selection for the different topologies of converters for different output voltages. As mentioned earlier **semiconductors are selected from pool of ABB Hipak series IGBTs and Diode Modules**:

IGBT Voltage rating selection for CHB (2 Cell):

$V_{nom\ rms}$ (V)	Source Voltage V_s (V)	IGBT Voltage Rating Required (V)	IGBT Current Rating (A)
3300	1305.5	3300	500
4500	1780.2	3300	500
6600	2611	4500	650

Table 4-1 IGBT Voltage rating selection for CHB (2 Cell)

IGBT Voltage rating selection for CHB (4 Cell):

$V_{nom\ rms}$ (V)	Source Voltage V_s (V)	IGBT Voltage Rating Required (V)	IGBT Current Rating (A)
3300	668.6	1700	800
4500	912	1700	800
6600	1337.2	3300	500

Table 4.2 IGBT Voltage rating selection for CHB (4 Cell)

IGBT Voltage rating selection for 3L NPC:

V_{nom} $_{rms}$ (V)	Source Voltage V_s (V)	IGBT Voltage Rating Required (V)	IGBT Current Rating (A)	Diode Voltage Rating (V)	Diode Current Rating (A)
3300	2537	4500	650	4500	650
4500	3460	6500	400	6500	400

Table 4-3 IGBT Voltage rating selection for 3L NPC

4.4. Power Losses calculations

Power losses in IGBTs and Diodes use for converter application can be separated into three parts

1. Conduction losses
2. Switching losses
3. Leakage losses (normally neglected)

4.4.1. Calculation of Conduction losses

The conduction losses can be computed in a as the product of the device current and the device voltage. These losses, as the name suggest, occurred during conduction time within the IGBT and the anti-parallel diode. So they need to be calculated for both the IGBT switch and the anti-parallel diode[12].

Conduction loss for an IGBT switch:

$$P_{ci} = u_{CEO} \cdot I_{Iav} + r_c \cdot I_{Irms}^2 \quad (4.3)$$

Similarly, conduction loss for an anti-parallel diode:

$$P_{cd} = u_{DO} \cdot I_{Dav} + r_D \cdot I_{Drms}^2 \quad (4.4)$$

Where,

u_{ce0} : on-state collector emitter voltage

I_{Iav} : IGBT current (average)

r_c : on state resistance between collector-emitter

I_{Irms} : IGBT current (RMS)

u_{DO} : on state voltage drop for diode

I_{Dav} : diode current (average)

r_D : on state resistance for diode

I_{Drms} : diode current (RMS)

4.4.2. Calculation of Switching losses

The switching of the IGBT from ON state to OFF state and vice versa doesn't occur instantaneously. The switching on mechanism is similar to the switching off mechanism but the switching off mechanism of the IGBT is very slow because of the current tailing. This incurs a

significant amount of energy loss during the switching off period. Figure 4.1 shows the Current and Voltage waveform during the IGBT switching. It can be clearly seen that the switching off time is longer than the switching on time.

Figure 4-1 IGBT Switching Waveform

These losses occur because of the non zero values of the current and voltage across the switches. For diode, switching loss occur only during turn off period. This occurs because of the reverse recovery characteristics of the diode. When a forward biased diode is to turn off, it takes time to extinguish free carriers across the p-n junction. The time period is taken into consideration when the current goes to negative, reaches its peak value and decays up to 25% of the maximum value. This is called the reverse recovery time. The energy loss during this period is calculated by computing the area of the power loss vs time graph.

The current and voltage waveforms as well as the power loss during diode switching have been shown in Figure 4-2.

Figure 4-2 Reverse Recovery Characteristics of Diode

Switching losses occur in the IGBT switch and in the anti parallel diodes during switching (ON/OFF) operation. These losses also need to be separately calculated for the IGBT as well as for the anti-parallel Diode[12].

Switching loss for IGBT:

$$P_{swI} = (E_{onI} + E_{offI}) \cdot f_{sw} \quad (4.5)$$

Similarly, switching loss for Diode:

$$P_{swD} = (E_{onD} + E_{offD}) \cdot f_{sw} \quad (4.6)$$

where

E_{onI} : IGBT turn-on energy losses

E_{offI} : IGBT turn-off energy losses

E_{onD} : diode turn-on energy losses

E_{offD} : diode turn-off energy losses (normally neglected)

f_{sw} : switching frequency (Hz)

E_{onI} , E_{offI} , E_{onD} can be obtained from the datasheet of each IGBT.

4.4.3. Calculation of Total losses

To obtain the total losses in an IGBT (P_{TII}) and a diode (P_{TID}), their corresponding switching losses and conduction loss are added[12].

So, total losses for an IGBT:

$$P_{TII} = P_{swI} + P_{ci} \quad (4.7)$$

Total losses for a diode:

$$P_{TID} = P_{swD} + P_{cd} \quad (4.8)$$

4.4.4. Power Loss Calculations using PLECS software:

The thermal loss (Conduction and switching loss) data for the particular IGBT or diode for a certain range are obtained from the datasheet of that switch or diode. These data are now filled up in PLECS's Thermal Description parameters. Actual losses (both switching and conduction) are calculated by using the linear interpolation technique, provided that the values fall within the pre specified index range. But if the values fall beyond the specified index range, then, extrapolation technique is used[13].

To create a new thermal data, view an already created thermal data and to edit the thermal data, Thermal Editor is used. Thermal parameters of a semiconductor can be entered in Thermal Description. The thermal data regarding the switching-losses, conduction-losses and the thermal equivalent circuit of a semiconductor can be entered from the semiconductor datasheet.

Following is the typical example of thermal description for the IGBT:

IGBT selected: **ABB 5SNA 0800N330100**

Switching Losses for IGBT

Figures showing the turn on and turn off losses of the aforementioned IGBT have been shown in Fig. 4.3 and Fig 4.4 respectively.

IGBT Turn-on loss:

Figure 4-3 IGBT Turn-on losses

It can be seen that the turn on loss of the IGBT increases with the increase in current and the voltage. The turn on loss data corresponding to voltage and current has been tabulated below.

$T=25^{\circ}$

	0A	400A	800A	1200A
0V	0J	0J	0J	0J
1800V	0J	0.4068J	1.001J	1.822J

$T=125^{\circ}$

	0A	400A	800A	1200A
0V	0J	0J	0J	0J
1800V	0J	0.6317J	1.38J	1.784J

Table 4-4 IGBT Turn On Losses

IGBT Turn-off loss:

Figure 4-4 IGBT Turn-off losses

It can be seen that the turn off loss of the IGBT increases with the increase in current and the voltage. The turn off loss data corresponding to voltage and current has been tabulated below.

T=25°

	0A	400A	800A	1200A
0V	0J	0J	0J	0J
1800V	0J	0.6J	0.88J	1.177J

T=125°

	0A	400A	800A	1200A
0V	0J	0J	0J	0J
1800V	0J	0.9094J	1.25J	1.784J

Table 4-5 IGBT Turn Off Losses

IGBT Conduction loss:

Figure 4-5 IGBT Conduction Loss

The ON state voltage and the current data for the above figure has been tabulated below. It can be observed that the conduction losses will be higher for the higher values of the currents and the on state voltage.

	0A	100A	200A	400A	600A	700A	800A	900A	1000A	1200A	1400A	1600A
25°	0V	1.5V	1.8V	2.3V	2.69V	2.9V	3.1V	3.25V	3.41V	3.73V	4V	4.31V
125°	0V	1.63V	2.09V	2.77V	3.37V	3.63V	3.8V	4.11V	4.37V	4.81V	5.29V	5.7V

Table 4-6 IGBT Conduction Losses

Switching Losses for Diode

As discussed in section 4.4.2 switching losses in diode only occurs during turn off period. The loss during the turn off is due to the reverse recovery characteristic of the diode. This has been further illustrated in the figures and the data tabulated below.

Diode Turn-on loss:

Figure 4-6 Diode Turn-on losses

T = 25 °	
	0 A
0 V	0 J

T = 125 °	
	0 A
0 V	0 J

Table 4-7 Diode Turn On Losses

Diode Turn-off loss:

Figure 4-7 Diode Turn-off losses

T=25°

	0A	400A	800A	1200A
-1800V V	0J	0.413 J	0.6201 J	0.7856 J
0V	0J	0J	0J	0J

T=125°

	0A	400A	800A	1200A
-1800V V	0J	0.828 J	1.18 J	1.342 J
0V	0J	0J	0J	0J

Table 4-8 Diode Turn Off Losses

Diode Conduction loss:

Figure 4-8 Diode Conduction Loss

	0A	100A	200A	400A	600A	700A	800A	900A	1000A	1200A	1400A	1600A
25°	0V	1.34 V	1.54 V	1.84 V	2.14 V	2.24V	2.3 V	2.44 V	2.51 V	2.66 V	2.81 V	2.95 V
125°	0V	1.05 V	1.34 V	1.75 V	2.1 V	2.1 V	2.35 V	2.48 V	2.6 V	2.81 V	3.04 V	3.24 V

Table 4-9 Diode Conduction Losses

The average switching losses of power semiconductors are calculated by using Periodic Impulse Average Block.

Figure 4-9 Periodic Average Impulse Block

As the name suggests, this block periodically averages an impulse input signal u for an averaging period of time T . At the end of time T , the output y returns a new value. The mathematical formulation of the periodic average impulse block is given below:

$$y(t) = \frac{1}{T} \int_{t-T}^t u(\tau) d\tau \cdot \text{rect} \left[t - \frac{n + \frac{1}{2}}{T} \right] \quad (4.8)$$

The average conduction loss of power semiconductors are calculated by using Periodic Average Block.

As the name suggests, this block periodically averages a continuous input signal u for an averaging period of time T . At the end of time T the output y returns a new value. The mathematical formulation of the periodic average block is given below:

$$y(t) = \frac{1}{T} \int_{t-T}^t u(\tau) d\tau \cdot \text{rect} \left[t - \frac{n + 1/2}{T} \right] \quad (4.9)$$

Figure 4-10 Periodic Average Block

Thermal impedance (Foster):

	1	2	3	4
R	0.00878 K/W	0.00206 K/W	0.000961 K/W	0.000948 K/W
τ	0.2074 s	0.0301 s	0.00755 s	0.00157 s

Table 4-10 IGBT Thermal Impedance

Average Switching loss of these semiconductors is obtained by using Periodic Impulse Average blocks.

Switching losses in the entire converter circuit is obtained by addition of each of average switching losses values.

On the other hand, average conduction losses of these semiconductors are obtained by using the Periodic Average block. Conduction losses of the semiconductor of the entire converter circuit are obtained by addition of each average conduction losses values.

5. Power Quality Analysis

We can observe that the output voltage waveform obtained from the inverter is not perfectly sinusoidal in shape. This means that the output current also won't be perfectly sinusoidal either. A distorted or non-sinusoidal waveform comprises of a multitude of harmonics in along with the fundamental component. This harmonics is the periodic sinusoidal having frequency which is a whole multiple of the fundamental frequency.

The presence of harmonics can be quantified by using the harmonic index known as the Total Harmonic distortion (THD).

The RMS value of the harmonic content expressed as a percentage of the fundamental is given by:

$$THD (\%) = \frac{\sqrt{\text{Sum of squares of all harmonic amplitudes}}}{\text{Amplitude of the fundamental}} \times 100\% \quad (5.1)$$

These harmonics present in the inverter output will have the effects such as

- i. Increase in resistive and magnetic losses due to additional flow of currents and flux at harmonic frequencies.
- ii. Increase in the dielectric loss at the capacitor banks.
- iii. Deterioration of insulation system of the system which results in shortening the useful life of the system.
- iv. Malfunctioning of the system components.
- v. Possibility of amplification of the harmonic levels due to resonance.

Because of these issues, the production of the harmonics at the converter output should be minimized as much as possible.

While selecting the topology of the converter one need to confirm that the selected topology complies with the standardized harmonic guidelines. In this study, the harmonic standard delineated by the **IEEE Standard 519-1992** has been taken as a reference[14].

This use of this standard in this study stipulates the maximum allowable harmonic distortion allowed in the current waveforms

To analyze the current harmonics according to the **IEEE Standard 519-1992**, short circuit ratio for each case are needed.

$$\text{Short Circuit Ratio (SCR)} = I_{SC}/I_L$$

Where, I_{SC} = Maximum current that a source is able to deliver.

I_L = maximum demand load current (fundamental frequency component)

In this case the magnitude of I_{SC} can be taken as twice the normal load current.
So SCR, in this case is, 2.

Below is the IEEE Standard 519-1992 for Harmonic Current Limits:

Maximum harmonic current distortion in percent of I_L (system 120V-69kV)						
I_{SC}/I_L	<11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	THD
<20	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above						

Table 5-1 Harmonic Current Limit Standard

In chapter 6, while considering the most suitable topology, the above mentioned IEEE Standard 519 would be taken as a reference to analyze whether the particular topology complies with the standard of the harmonic current limits.

6. Simulation Results and Loss Calculation

6.1. Simulation Scope:

Two different topologies, NPC and CHB, are simulated and their percentage losses for the given load are then compared. Both the topologies of inverters are feeding to the same 1MW squirrel cage induction motor. Different voltage levels of 3.3kV, 4.5kV and 6.6kV are considered.

A non-saturable squirrel cage induction-machine has been used for PLECS simulation.

Stationary reference frame has been used for the machine modeling. This machine model helps in the connection of external components such as inductors in series with the stator winding.

Because of the stationary reference frame model the machine parameters are viewed from the stator side. Below are the details of the induction motor used during simulation:

Induction Machine (Squirrel Cage) (mask) (link)

Three-phase induction machine with short-circuited rotor windings. All parameters and electrical quantities are referred to the stator side.

Parameters
Assertions

Stator resistance R_s :	Friction coefficient F :
<input type="text" value="0.45"/>	<input type="text" value="0.001"/>
Stator leakage inductance L_{ls} :	Number of pole pairs p :
<input type="text" value="2.1e-3"/>	<input type="text" value="4"/>
Rotor resistance R_r' :	Initial rotor speed ω_{m0} :
<input type="text" value="0.8"/>	<input type="text" value="0"/>
Rotor leakage inductance L_{lr}' :	Initial rotor position θ_{m0} :
<input type="text" value="2e-3"/>	<input type="text" value="0"/>
Magnetizing inductance L_m :	Initial stator currents [i_{sa0} i_{sb0}]:
<input type="text" value="70e-3"/>	<input type="text" value="[0 0]"/>
Inertia J :	Initial stator flux [ψ_{sisd0} ψ_{sisq0}]:
<input type="text" value="0.3"/>	<input type="text" value="[0 0]"/>

Figure 6-1 Induction Machine Ratings

Current and the voltage rating selection of IGBTs used in different topologies for different voltage can be referred according to section 4.3.

Switching losses and Conduction losses are calculated for each switching frequency of 500Hz, 1000Hz, 1500Hz and 2000Hz.

Motor starting state or any transient state is beyond the scope of this study, hence only steady state motor operation is considered.

6.2. Performance evaluation Criteria for CHB and NPC Converters

The performances of Cascaded H-Bridge Converter (CHB) and Neutral Point Clamping (NPC) converters are analyzed over a wide range of parameters such as switching frequency, output harmonics, switching and conduction losses.

For CHB converters, two types of converters are considered:

- 1) CHB with 6 H-Bridge Modules (2 H-Bridge Modules in each leg).
- 2) CHB with 12 H-Bridge Modules (4 H-Bridge Modules in each leg).

It should be noted that the objective of this study is to find the most efficient inverter topology with agreeably lower harmonic currents.

While calculating the % individual harmonics as well as the % THD, higher order current harmonics (beyond 20th order) can be neglected. The load we are using in this study is in an induction motor load. This motor load has high value of inductance parameter. This inductance offers higher impedance for higher harmonics. Hence the magnitudes of higher order current harmonics are very small and can be neglected.

The modulation for the CHB and the NPC converters using PWM has already been discussed in earlier chapter.

In the coming sections performance of these three converts are analyzed on the basis of the efficiency and quality of power.

First of all the performance measuring parameters such as %Losses and the % THD of the current waveforms are calculated and listed for each topology for the switching frequencies of 500Hz, 1000Hz, 1500Hz and 2000Hz. These listed parameters are then compared to decide the best possible inverter topology[15].

The installed cost of IGBTs and Diodes in a particular topology for a particular output voltage is also taken into account. This parameter is expressed in terms of installed KVA of IGBT. This installed KVA reflects the cost of that particular topology. Although this is a very much deciding factor for selecting the best topology, in this study the topology selection based on this factor has not been done.

6.3. Simulation Observation

6.3.1. Simulation Observations for 3.3kV Inverters

6.3.1.1. Simulation Observations for 3.3kV Cascaded H-Bridge Converter (2 Cells)

Semiconductor Details	
IGBT used	5SND 0500N330300
Manufacturer	ABB
V _{ce}	3300V
I _c	500A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV CHB (2 Cells) inverter:

Device switching frequency (Hz)	500		1000		1500		2000	
Source (Each DC Source) (Vdc) (V)	1305.5		1305.5		1305.5		1305.5	
Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	1910.59		1911.45		1912.09		1912.02	
Output Voltage (RMS) (L-L) (V)	3300.03		3300.24		3300.47		3300.32	
Output Current (RMS)	206.634		206.52		206.5		206.492	
Total power delivered by sources (W)	1005888		1005714		1005687		1005678	
Losses in all three phases (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	3951.84	0.393	3961.5	0.394	3990.51	0.397	4012.86	0.399
Switching Loss	3048.6	0.303	6452.43	0.642	9957.87	0.990	13545.12	1.35
Total Loss	6983.07	0.696	10411.44	1.06	13921.56	1.39	17519.07	1.75

Installed KVA of IGBT: 39600

Table 6-1 Simulation Result for 3.3kV CHB (2Cells) Converter

Figure 6-2 Percentage Loss vs. Device Switching Frequency for 3.3kV CHB (2 Cells)

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV CHB (2 Cells) inverter:

	% Harmonics at Device switching frequency (Hz)			
Harmonics Order	500	1000	1500	2000
0	6.0E-09	6.9E-08	8.8E-08	5.9E-08
1	100	100	100	100
2	2.1E-09	5.5E-08	6.1E-08	5.1E-08
3	3.7E-06	2.0E-06	2.5E-06	1.5E-06
4	8.5E-10	1.5E-08	1.7E-08	1.3E-08
5	1.6E-05	1.9E-05	1.9E-05	1.3E-05
6	6.4E-10	8.2E-09	9.3E-09	6.9E-09
7	1.4E-05	1.1E-06	7.0E-06	5.6E-06
8	4.1E-10	5.8E-09	6.7E-09	4.7E-09
9	4.2E-06	3.4E-06	2.4E-06	4.1E-07
10	1.7E-10	4.6E-09	5.1E-09	3.5E-09
11	1.6E-05	2.4E-05	2.0E-05	1.7E-05
12	2.7E-11	3.7E-09	4.3E-09	2.8E-09
13	2.0E-05	1.9E-05	1.7E-05	1.5E-05
14	1.6E-10	3.2E-09	3.6E-09	2.5E-09
15	1.2E-05	2.0E-06	2.6E-06	4.9E-07
16	1.1E-10	2.8E-09	3.2E-09	2.1E-09
17	1.6E-05	9.6E-07	2.6E-06	1.3E-06
18	1.3E-10	2.4E-09	2.8E-09	1.9E-09
19	7.5E-06	3.5E-06	1.9E-07	1.2E-06

20	1.1E-10	2.2E-09	2.4E-09	1.7E-09
% THD	4.0E-05	3.6E-05	3.3E-05	2.7E-05

Table 6-2 % Harmonics and % THD of Output Current Waveform for 3.3kV CHB (2 Cells)

It can be observed that for 3.3kV CHB (2 Cells) inverter all individual current harmonics as well as the THD complies with the Harmonic Current Limits standard (Table 6-1) for the entire range of switching frequency.

6.3.1.2. Simulation Observations for 3.3kV Cascaded H-Bridge Converter (4 Cells)

Semiconductor Details	
IGBT used	5SND 0800M170100
Manufacturer	ABB
V _{ce}	1700V
I _c	800A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV CHB (4 Cells) inverter:

Device switching frequency (Hz)	500		1000		1500		2000	
Source (Each DC Source) (Vdc) (V)	668.6		668.6		668.6		668.6	
Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	1908.76		1908.93		1908.84		1908.91	
Output Voltage (RMS) (L-L) (V)	3300.12		3300.09		3300.01		3300.08	
Output Current (RMS)	202.56		202.554		202.553		202.552	
Total power delivered by sources (W)	1003536.6		1003522.8		1003519.2		1003521.6	
Losses (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	6013.32	0.599	6013.86	0.599	6041.88	0.602	6020.55	0.600
Switching Loss	548.544	0.055	1146.219	0.114	1752.186	0.175	2356.554	0.235
Total Loss	6565.44	0.654	7163.85	0.713	7782.12	0.777	8383.11	0.835

Installed KVA of IGBT: 65280

Table 6-3 Simulation Result for 3.3kV CHB (4 Cells) Converter

Figure 6-3 Percentage Loss vs. Device Switching Frequency for 3.3kV CHB (4 Cells)

It can be observed here that the percentage losses doesn't increase considerably with switching freq (0.654% to 0.835%), unlike other topologies where losses increases considerably with switching frequency.

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV CHB (4 Cells) inverter:

	% Harmonics at Device switching frequency (Hz)			
Harmonics Order	500	1000	1500	2000
0	6.9E-09	1.7E-08	3.1E-08	1.4E-08
1	100	100	100	100
2	9.5E-09	1.2E-08	1.3E-08	9.6E-09
3	4.7E-06	1.8E-06	1.3E-06	2.3E-07
4	2.6E-09	4.0E-09	3.1E-09	3.2E-09
5	2.6E-05	2.8E-05	1.6E-05	1.1E-05
6	1.5E-09	2.6E-09	1.7E-09	1.6E-09
7	2.7E-05	2.7E-05	1.6E-05	1.1E-05
8	7.4E-10	2.0E-09	1.3E-09	1.1E-09
9	5.1E-06	2.7E-06	1.0E-06	4.0E-07
10	5.4E-10	1.6E-09	9.2E-10	7.5E-10
11	1.4E-05	2.0E-05	1.2E-05	8.0E-06
12	3.5E-10	1.2E-09	8.3E-10	4.0E-10
13	1.8E-05	1.9E-05	1.2E-05	8.0E-06
14	3.4E-10	1.1E-09	7.2E-10	4.2E-10
15	1.2E-05	4.7E-06	2.6E-06	5.2E-07
16	2.0E-10	9.4E-10	6.1E-10	3.1E-10
17	9.5E-06	6.7E-06	3.6E-06	4.1E-06

18	2.3E-10	8.5E-10	5.5E-10	3.4E-10
19	4.9E-06	7.0E-06	4.8E-06	4.2E-06
20	1.6E-10	7.5E-10	4.5E-10	2.4E-10
% THD	4.69E-05	4.21E-05	2.92E-05	2.01E-05

Table 6-4 % Harmonics and % THD of Output Current Waveform for 3.3kV CHB (4 Cells)

It can be observed that for 3.3kV CHB (4 Cells) inverter all individual current harmonics as well as the THD complies with the IEEE Std 519-1992 Harmonic Current Limits (Table 5-1) for the entire range of switching frequency.

6.3.1.3. Simulation Observations for 3.3kV Neutral Point Clamping Converter (3 Levels):

Semiconductor Details 5SNA 0650J450300			
IGBT used		Clamping Diode Used	
Manufacturer	ABB	Manufacturer	ABB
V _{ce}	4500V	Repetitive peak reverse voltage (V _{rrm})	4500V
I _c	650A	I _f	650A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV NPC (3L) inverter:

Device switching frequency (Hz)	500		1000		1500		2000	
Source (Each DC Source) (Vdc) (V)	2537V		2537V		2537V		2537V	
Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	2015.88		2022.15		2023.31		2023.71	
Output Voltage (RMS) (L-L) (V)	3302.71		3296.9		3293.57		3305.25	
Output Current (RMS)	214.667		211.27		210.779		210.606	
Total power delivered by sources (W)	1007815		1003267		1002637		1002432	
*Losses in Phase A (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
*Conduction Loss	2270.805	0.225	2243.631	0.224	2244.348	0.224	2249.535	0.224
*Switching Loss	2147.511	0.213	4274.04	0.426	6522.12	0.650	8891.61	0.887

*Total Loss	4420.05	0.439	6517.29	0.650	8765.91	0.874	11140.23	1.11
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*Includes the losses due to the clamping diodes

Installed KVA of IGBT: 31500

Table 6-5 Simulation Result for 3.3kV NPC (3 Level) Converter

Figure 6-4 Percentage Loss vs. Device Switching Frequency for 3.3kV NPC (3L)

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 3.3kV 3L NPC inverter:

	% Current Harmonics for different Device switching frequency (Hz)			
Harmonics Order	500	1000	1500	2000
0	1.8E-04	4.0E-04	2.6E-04	-1.1E-04
1	100	100	100	100
2	3.4E-01	4.7E-02	1.5E-01	7.7E-03
3	1.2E-02	9.7E-04	1.5E-03	1.8E-04
4	1.1E+00	2.9E-01	9.1E-02	2.3E-02
5	2.1E+00	5.4E-01	2.4E-01	1.4E-01
6	1.1E+01	4.8E-01	5.5E-04	4.7E-02
7	5.7E-01	1.8E-01	8.0E-02	4.4E-02
8	8.4E+00	1.4E-01	1.4E-01	3.9E-02
9	2.2E-01	3.2E-03	1.1E-03	3.0E-04
10	6.4E-01	6.7E-01	1.6E-01	2.2E-02
11	2.3E-01	7.6E-02	3.7E-02	2.0E-02

12	5.9E+00	1.1E+00	5.8E-04	5.7E-02
13	1.2E+00	5.3E-02	2.5E-02	1.3E-02
14	6.4E+00	1.0E-01	2.0E-01	5.5E-02
15	4.2E+00	6.0E-03	2.1E-03	2.3E-04
16	3.1E-01	4.1E+00	2.5E-01	1.7E-02
17	1.9E-02	1.9E-02	1.5E-02	9.3E-03
18	1.0E+00	3.4E+00	8.8E-04	7.7E-02
19	4.2E+00	2.0E-02	9.3E-03	6.6E-03
20	2.0E-01	7.8E-02	4.3E-01	8.4E-02
% THD	17.4	5.52	0.652	0.213

Table 6-6 % Harmonics and % THD of Output Current Waveform for 3.3kV NPC (3L)

Comparing these observations with the IEEE Standard 519-1992 Harmonic Current Limits (Table 6-1), it can be noticed that for 3.3kV NPC (3L) inverter, at SCR <20:

- For 500Hz switching frequency, even harmonics of the orders 8th, 12th, 14th, 18th, the odd harmonics 15th and 19th along with the THD violates the standard harmonic current limits.
- For 1000Hz switching frequency, even harmonics of the orders 12th, 16th, 18th along with the THD violates the harmonic current limits.
- For 1500Hz and 2000Hz switching frequencies, all the harmonic components along with the THD comply with the IEEE Std 519-1992 Harmonic Current Limits.

6.3.1.4. Consolidation of Losses Data and the % THD of current waveform for Topology selection for 3.3kV Inverter

Switching Frequency= 500Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.393	0.599	0.225
% Switching Loss	0.303	0.055	0.213
% Total Loss	0.696	0.654	0.438
% THD of current waveform	3.98E-05	4.69E-05	17.4
Installed KVA of IGBT	39600	65280	52650

Switching Frequency= 1000Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.394	0.599	0.224
% Switching Loss	0.641	0.114	0.426
% Total Loss	1.035	0.713	0.650
% THD of current waveform	3.63E-05	4.21E-05	5.52
Installed KVA of IGBT	39600	65280	52650

Switching Frequency= 1500Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.396	0.602	0.224

% Switching Loss	0.990	0.175	0.650
% Total Loss	1.39	0.775	0.874
% THD of current waveform	3.34E-05	2.92E-05	0.652
Installed KVA of IGBT	39600	65280	52650

Switching Frequency= 2000Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.399	0.600	0.224
% Switching Loss	1.346864503	0.235	0.887
% Total Loss	1.745884866	0.835	1.11
% THD of current waveform	2.68E-05	2.01E-05	0.213
Installed KVA of IGBT	39600	65280	52650

The % Total losses for all three circuits has been summarized below for entire switching frequency range to illustrate the variation of the % total losses with respect to switching frequency.

Figure 6-5 Comparison of %Total Losses for Different Topologies of MLI with respect to Switching Frequency for 3.3kV Converters

The THD for the current waveforms for all three circuits has been summarized below for entire switching range to illustrate the variation of the THD with respect to switching frequency.

Figure 6-6 Comparison of THD for current waveform for Different Topologies of MLI with respect to Switching Frequency for 3.3kV Converters

6.3.1.5. Selection of Topology for 3.3kV converter for different switching frequencies:

As discussed before, the fundamental requirement for the topology selection is that the selected topology should have the minimum losses and also must have lower harmonic current. From the data tabulated above and the corresponding figure for comparing the % total loss and switching frequency as well as THD with switching frequency, it has been found that:

- 1) For 500Hz switching frequency, total losses for the NPC converter is much lesser than that of CHB (2 Cells) and CHB (4 Cells) converters. However, its THD is significantly higher and beyond the standard limit (5% THD).
So, NPC topology cannot be considered in this case. To choose in between the CHB (2 Cells) and CHB (4 Cells) converters, it can be seen that the losses in CHB (4 Cells) is lesser by about 0.05%
Hence, for the 3.3 kV converter with a switching frequency of 500Hz, CHB (4 Cell) converter is the preferable over the others.
- 2) For 1000Hz switching frequency, again, the %total losses for NPC (3L) converter is lower than that of the CHB (2 Cells) and CHB (4 Cells) converters. However, its THD is slightly more than the standard current harmonic limit.
Comparison between the CHB (2 Cell) and CHB (4 Cell) converter shows that both have minimum current harmonic contents within the limit. But CHB (4 Cell) converter has much lower % total losses than the CHB (2 Cells) converter.
Hence, for the 3.3 kV converter with a switching frequency of 1000Hz, CHB (4 Cell) converter is the preferable over the others.

- 3) For 1500Hz switching frequency, the %total losses and the THD for current waveform are higher for the NPC (3L) and CHB (2 Cell) converters than the CHB (4 Cells) converters.

Hence, for the 3.3 kV converter with a switching frequency of 1500Hz, CHB (4 Cell) converter is the preferable over the others.

- 4) For 2000Hz switching frequency, the %total losses and the THD for current waveform are higher for the NPC (3L) and CHB (2 Cell) converters than the CHB (4 Cells) converters.

Hence, for the 3.3 kV converter with a switching frequency of 2000Hz, CHB (4 Cell) converter is the more preferable over the others.

6.3.2. Simulation Observations 4.5kV Inverters

6.3.2.1. Simulation Observations for 4.5kV Cascaded H-Bridge Converter (2 Cells)

Semiconductor Details	
IGBT used	5SND 0500N330300
Manufacturer	ABB
Vce	3300V
Ic	500A

The maximum value of current through each IGBT is lies in the range of 250 A to 273.3A. The current rating of each IGBT is taken as 500A.

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV CHB (2 Cells) inverter:

Device switching frequency (Hz)	500	1000	1500	2000
Source (Each DC Source) (Vdc) (V)	1780.2	1780.2	1780.2	1780.2
Simulation Time (s)	5	5	5	5
Output Voltage (RMS) (L-N) (V)	2605.31	2605.82	2607.36	2607.26
Output Voltage (RMS) (L-L) (V)	4499.97	4500.25	4500.57	4500.37
Output Current (RMS)	174.6	174.346	174.301	174.286
Total power delivered by sources (W)	989787	989472	989412	989394

Losses Types (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	3105.12	0.314	3117.57	0.315	3131.43	0.316	3148.62	0.318
Switching Loss	3617.16	0.365	7708.2	0.779	11914.68	1.20	16248.42	1.64
Total Loss	6723.6	0.679	10823.88	1.09	15049.59	1.52	19398.63	1.96

Installed KVA of IGBT: 39600

Table 6-7 Simulation Result for 4.5kV CHB (2Cells) Converter

Figure 6-7 Percentage Loss vs. Device Switching Frequency for 4.5kV CHB (2 Cells)

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV CHB (2 Cells) inverter:

	% Harmonics at Device switching frequency (Hz)			
Harmonics Order	500	1000	1500	2000
0	-7.9E-09	2.3E-09	-1.4E-07	4.7E-08
1	100	100	100	100
2	1.9E-08	1.7E-08	1.4E-08	6.7E-09
3	8.2E-06	1.1E-06	1.5E-06	2.4E-06
4	1.0E-08	8.5E-09	3.0E-09	2.6E-09
5	1.9E-05	2.2E-05	2.4E-05	1.9E-05
6	5.8E-09	6.7E-09	1.4E-09	1.2E-09
7	3.0E-05	7.2E-06	1.1E-05	9.8E-06
8	4.5E-09	4.5E-09	1.0E-09	7.1E-10
9	1.0E-05	4.2E-06	4.2E-06	2.3E-07
10	3.4E-09	3.7E-09	1.0E-09	4.6E-10

11	4.1E-05	4.8E-05	3.9E-05	2.9E-05
12	3.2E-09	3.1E-09	5.0E-10	2.4E-10
13	4.6E-05	4.2E-05	3.5E-05	2.7E-05
14	2.7E-09	2.7E-09	3.6E-10	2.6E-10
15	1.6E-05	1.8E-06	4.5E-06	1.3E-06
16	2.2E-09	2.3E-09	9.6E-11	2.8E-10
17	9.3E-06	6.8E-06	1.9E-06	3.4E-06
18	1.9E-09	2.1E-09	4.1E-10	1.3E-10
19	4.0E-06	4.3E-06	7.3E-06	3.7E-06
20	1.8E-09	1.9E-09	2.3E-10	1.8E-10
% THD	7.51E-05	6.84E-05	5.98E-05	4.51E-05

Table 6-8 % Harmonics and % THD of Output Current Waveform for 4.5kV CHB (2 Cells)

It can be observed that for 4.5kV CHB (2 Cells) inverter all individual current harmonics as well as the THD complies with the IEEE Std 519-1992 Harmonic Current Limits (Ref. Table 6-1) for the entire range of switching frequency.

6.3.2.2. Simulation Observations for 4.5kV Cascaded H-Bridge Converter (4 Cells)

Semiconductor Details	
IGBT used	5SND 0800M170100
Manufacturer	ABB
Vce	1700V
Ic	800A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV CHB (4 Cells) inverter:

Device switching frequency (Hz)	500	1000	1500	2000
Source (Each DC Source) (Vdc) (V)	912	912	912	912
Simulation Time (s)	5	5	5	5
Output Voltage (RMS) (L-N) (V)	2603.9	2603.86	2603.74	2603.81
Output Voltage (RMS) (L-L) (V)	4501.49	4501.47	4501.36	4501.46
Output Current (RMS)	173.381	173.365	173.363	180.568

Total power delivered by sources (W)	988981.8		988963.2		988962		988958.4	
Losses (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	4855.35	0.491	4860.33	0.491	4858.2	0.491	4856.8	0.491
Switching Loss	655.97	0.066	1371.31	0.139	2090.5	0.211	2817.6	0.285
Total Loss	5515.47	0.558	6236.67	0.630	6950.28	0.703	7677.63	0.776

Installed KVA of IGBT: 65280

Table 6-9 Simulation Result for 4.5kV CHB (4Cells) Converter

Figure 6-8 Percentage Loss vs. Device Switching Frequency for 4.5kV CHB (4 Cells)

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV CHB (4 Cells) inverter:

	% Harmonics at Device switching frequency (Hz)			
Harmonics Order	500	1000	1500	2000
0	-5.1E-09	1.6E-08	4.5E-05	4.5E-05
1	100	100	100	100
2	1.6E-09	2.7E-09	3.3E-05	3.3E-05
3	1.0E-05	3.6E-06	1.2E-05	1.3E-05

4	8.1E-10	9.3E-10	7.7E-06	7.7E-06
5	4.7E-05	4.5E-05	2.4E-05	1.5E-05
6	6.0E-10	5.1E-10	4.0E-06	4.0E-06
7	4.9E-05	4.2E-05	2.6E-05	1.6E-05
8	5.1E-10	4.4E-10	2.7E-06	2.7E-06
9	6.1E-06	4.4E-06	3.3E-06	2.4E-06
10	5.2E-10	3.1E-10	2.0E-06	2.0E-06
11	3.1E-05	3.4E-05	2.3E-05	1.4E-05
12	4.1E-10	4.6E-10	1.6E-06	1.6E-06
13	3.8E-05	3.3E-05	2.2E-05	1.4E-05
14	3.8E-10	2.5E-10	1.4E-06	1.4E-06
15	1.9E-05	7.0E-06	4.3E-06	1.4E-06
16	3.4E-10	2.0E-10	1.2E-06	1.2E-06
17	8.2E-06	1.1E-05	8.1E-06	6.8E-06
18	2.8E-10	2.2E-10	1.0E-06	1.0E-06
19	7.1E-06	1.3E-05	1.0E-05	7.2E-06
20	2.7E-10	1.9E-10	9.2E-07	9.2E-07
% THD	8.68E-05	8.02E-05	7.64E-05	6.61E-05

Table 6-10 % Harmonics and % THD of Output Current Waveform 4.5kV CHB (4 Cells)

It can be observed that for 4.5kV CHB (4 Cells) inverter all individual current harmonics as well as the THD complies with the IEEE Std 519-1992 Harmonic Current Limits (Ref. Table 6-1) for the entire range of switching frequency.

6.3.2.3. Simulation Observations for 4.5kV Neutral Point Clamping Converter (3Levels)

Semiconductor Details			
IGBT used	5SNA 0400J650100	Clamping Diode Used	5SLD 600J650100
Manufacturer	ABB	Manufacturer	ABB
V _{ce}	6500V	Repetitive peak reverse voltage (V _{rrm})	6500V
I _c	400A	I _f	600A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV NPC (3L) inverter:

Device switching frequency (Hz)	500	1000	1500	2000
Source (Each DC Source) (V _{dc}) (V)	3460V	3460V	3460V	3460V

Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	2749.23V		2758V		2759.23V		2759.97V	
Output Voltage (RMS) (L-L) (V)	4500.21		4502.1		4500.86		4500.3	
Output Current (RMS)	186.83		176.689A		175.669		175.342A	
Total power delivered by sources (W)	998816		985695		984526		984152	
*Losses Types (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
*Conduction Loss	2992.698	0.299	2845.368	0.289	2850.702	0.289	2868.012	0.291
*Switching Loss	3435.39	0.344	6697.77	0.679	10233.75	1.04	13829.07	1.40
*Total Loss	6431.85	0.644	9543.51	0.968	13088.43	1.33	16692.93	1.70

*Includes the losses due to the clamping diodes

Installed KVA of IGBT: 31200

Table 6-11 Simulation Result for 4.5kV NPC (3 Level) Converter

Figure 6-9 Percentage Loss vs. Device Switching Frequency for 4.5kV NPC (3Level) Converter

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 4.5kV NPC (3L) inverter:

Harmonics Order	% Harmonics at Device switching frequency (Hz)			
	500	1000	1500	2000
0	1.03E-03	5.7E-04	5.4E-04	-3.2E-04
1	1.00E+02	100	100	100
2	6.23E-01	7.9E-02	2.0E-01	1.3E-02
3	1.04E-02	1.4E-03	2.1E-03	5.8E-04
4	2.22	5.1E-01	1.9E-01	4.2E-02
5	4.13	1.1	4.8E-01	2.7E-01
6	22.6	8.6E-01	7.9E-04	7.2E-02
7	3.27E-01	1.2E-01	5.4E-02	2.9E-02
8	19.2	2.2E-01	2.3E-01	6.6E-02
9	3.66E-01	4.5E-03	1.9E-03	6.4E-04
10	1.05	1.1E+00	2.6E-01	3.5E-02
11	3.93E-01	1.2E-01	6.0E-02	3.2E-02
12	10.3	1.8E+00	9.9E-04	9.3E-02
13	1.87	8.3E-02	3.9E-02	2.0E-02
14	11.1	1.7E-01	3.3E-01	9.0E-02
15	6.94	9.8E-03	3.5E-03	1.3E-04
16	5.08E-01	6.9E+00	4.1E-01	2.9E-02
17	3.19E-02	3.0E-02	2.5E-02	1.6E-02
18	1.69	5.8E+00	1.4E-03	1.3E-01
19	7.06	3.2E-02	1.7E-02	1.2E-02
20	2.92E-01	1.3E-01	6.9E-01	1.4E-01
% THD	35.18288	9.400314	1.091703	0.374124

Table 6-12 % Harmonics and % THD of Output Current Waveform for 4.5kV NPC (3L)

Comparing these observations with the IEEE Std 519-1992 Harmonic Current Limits (Table 6-1), it can be noticed that for 3.3kV NPC (3L) inverter, at SCR <20:

- For 500Hz switching frequency, even harmonics of the orders 4th, 6th, 8th, 10th, 12th, 14th, 18th, the odd harmonics 5th, 15th and 19th along with the THD violates the standard harmonic current limits. Hence
- For 1000Hz switching frequency, even harmonics of the orders 16th, 18th along with the THD violates the harmonic current limits.
- For 1500Hz switching frequency, even harmonic of the order 20th violates the harmonic current limits.
- For 2000Hz switching frequency, all the harmonic components along with the THD comply with the IEEE Std 519-1992 Harmonic Current Limits.

6.3.2.4. Consolidation of Losses Data and the % THD of current waveform for Topology selection for 4.5kV Inverter

Switching Frequency= 500Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.314	0.491	0.299
% Switching Loss	0.365	0.066	0.344
% Total Loss	0.679	0.558	0.644
% THD	7.51E-05	8.68E-05	35.18
Installed KVA of IGBT	39600	65280	54600

Switching Frequency= 1000Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.315	0.491	0.289
% Switching Loss	0.779	0.139	0.679
% Total Loss	1.09	0.630	0.968
THD (for Current)	6.84E-05	8.02E-05	9.400314
Installed KVA of IGBT	39600	65280	54600

Switching Frequency= 1500Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.316	0.491	0.289
% Switching Loss	1.20	0.211	1.04
% Total Loss	1.52	0.703	1.33
THD (for Current)	5.98E-05	7.64E-05	1.09
Installed KVA of IGBT	39600	65280	54600

Switching Frequency= 2000Hz	CHB (2 Cells)	CHB (4Cells)	NPC
% Conduction Loss	0.318	0.491	0.291
% Switching Loss	1.64	0.285	1.405
% Total Loss	1.96	0.776	1.69
THD (for Current)	4.51E-05	6.61E-05	0.374
Installed KVA of IGBT	39600	65280	54600

The % Total losses for all three circuits have been summarized below for entire switching range to illustrate the variation of the % total losses with respect to switching frequency.

Figure 6-10 Comparison of %Total Losses for Different Topologies of MLI with respect to Switching Frequency for 4.5kV Converters

The THD for all three circuits has been summarized below for entire switching range to illustrate the variation of the THD with respect to switching frequency.

Figure 6-11 Comparison of % THD for Current Waveform for Different Topologies of MLI with respect to Switching Frequency for 4.5kV Converters

6.3.2.5. Topology Selection for 4.5 kV Converters for Different Switching Frequency:

From the data tabulated above and the corresponding figure for comparing the % total loss and switching frequency as well as THD with switching frequency, it has been found that:

- 1) For 500Hz switching frequency, the THD for the NPC (3 Level) converter is beyond the standard limit. For CHB (2 Cells) and CHB(4 Cells) converters, both comply with the harmonics limit. Also the losses for the CHB (4 Cells) converter is the least among the three converter topologies. Hence, for the 4.5 kV converter with a switching frequency of 500Hz, CHB (4 Cell) converter is the preferable over the others.
- 2) For 1000Hz switching frequency, the THD for the NPC (3 Level) converter is beyond the standard limit. For CHB (2 Cells) and CHB (4 Cells) converters, both comply with the harmonics limit. Also the losses for the CHB (4 Cells) converter is the least among the three converter topologies. Hence, for the 4.5 kV converter with a switching frequency of 1000Hz, CHB (4 Cell) converter is the preferable over the others.
- 3) For 1500Hz switching frequency, the % total losses and the THD for current waveform are higher for the NPC (3L) and CHB (2 Cell) converters than the CHB (4 Cells) converter.
Hence, for the 4.5kV converter with a switching frequency of 1500Hz, CHB (4 Cells) converter is preferred over the others.
- 4) For 2000Hz switching frequency, the % total losses and the THD for current waveform are higher for the NPC (3L) and CHB (2 Cell) converters than the CHB (4 Cells) converter.
Hence, for the 4.5kV converter with a switching frequency of 1500Hz, CHB (4 Cells) converter is preferred over the others.

6.3.3. Simulation Observations for 6.6kV Inverters

6.3.3.1. Simulation Observations for 6.6kV Cascaded H-Bridge Converter (2 Cells):

Semiconductor Details	
IGBT used	5SNA 0650J450300
Manufacturer	ABB
Vce	4500V
Ic	650A

The maximum value of IGBT current goes from 267A up to 288.2 A, so the next higher current rating for the 4500V rated IGBT available is 650A

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 6.6kV CHB (2 Cells) inverter:

Device switching frequency (Hz)	500		1000		1500		2000	
Source (Each DC Source) (Vdc) (V)	2611		2611		2611		2611	
Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	3821.18		3823.46		3824.19		3824.03	
Output Voltage (RMS) (L-L) (V)	6600.05		6600.47		6600.93		6600.64	
Output Current (RMS)	186.319		185. 629		185.539		185.508	
Total power delivered by sources (W)	995859		995178		995055		953433	
Losses (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	3946.56	0.396	3947.04	0.397	3962.85	0.398	3979.89	0.4
Switching Loss	7495.68	0.753	15625.05	1.57	24049.59	2.42	32985.9	3.31
Total Loss	11443.41	1.149	19581.6	1.97	28017.84	2.81	36972.3	3.71

Installed KVA of IGBT: 70200

Table 6-13 Simulation Result for 6.6kV CHB (2Cells) Converter

Figure 6-12 Percentage Loss vs. Device Switching Frequency for 6.6kV CHB (2 Cells)

Harmonic Analysis for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 6.6kV CHB (2 Cells) inverter:

Harmonics Order	% Harmonics at Device switching frequency (Hz)			
	500	1000	1500	2000
0	4.8E-09	1.1E-08	-1.1E-08	6.7E-09
1	100	100	100	100
2	1.6E-08	2.2E-09	4.6E-09	5.7E-09
3	2.4E-06	4.3E-06	4.3E-06	1.7E-06
4	5.6E-09	4.1E-10	6.4E-10	2.0E-09
5	6.0E-05	4.4E-05	3.6E-05	2.0E-05
6	4.5E-09	3.7E-10	7.3E-10	1.5E-09
7	5.7E-05	2.0E-05	1.7E-06	4.8E-06
8	3.5E-09	4.7E-10	6.0E-10	1.3E-09
9	1.5E-05	8.5E-06	4.8E-06	3.1E-06
10	2.6E-09	7.4E-11	2.9E-10	9.6E-10
11	2.7E-05	5.2E-05	4.0E-05	2.6E-05
12	2.3E-09	1.4E-10	3.6E-10	8.9E-10
13	3.8E-05	4.1E-05	3.3E-05	3.0E-05
14	1.8E-09	2.8E-10	3.5E-10	6.4E-10
15	1.8E-05	5.6E-06	6.4E-06	1.9E-06
16	1.5E-09	1.4E-10	2.1E-10	5.6E-10
17	1.5E-05	1.1E-05	5.0E-06	1.4E-05
18	1.5E-09	1.2E-10	2.1E-10	5.4E-10
19	5.5E-06	1.2E-05	1.4E-05	1.1E-05
20	1.3E-09	1.0E-10	2.0E-10	4.8E-10
% THD	9.94E-05	8.45E-05	6.63E-05	4.85E-05

Table 6-14 % Harmonics and % THD of Output Current Waveform for 6.6kV CHB (2Cells) Converter

It can be observed that for 6.6kV CHB (2 Cells) inverter all individual current harmonics as well as the THD complies with the IEEE Std 519-1992 Harmonic Current Limits (Ref. Table 6-1) for the entire range of switching frequency.

6.3.3.2. Simulation Observations for 6.6kV Cascaded H-Bridge Converter (4 Cells)

Semiconductor Details	
IGBT used	5SND 0500N330300
Manufacturer	ABB
Vce	3300V
Ic	500A

Peak value of current flowing through IGBT is 274.5A. So, IGBT of current rating of 500A is selected because of unavailability of IGBT of current rating lower than that which can hold the peak current of 274.5 A.

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 6.6kV CHB (4 Cells) inverter:

Device switching frequency (Hz)	500		1000		1500		2000	
Source (Each DC Source) (Vdc) (V)	1337.2		1337.2		1337.2		1337.2	
Simulation Time (s)	5		5		5		5	
Output Voltage (RMS) (L-N) (V)	3817.56		3817.63		3817.68		3817.78	
Output Voltage (RMS) (L-L) (V)	6600.21		6600.18		6600.02		6600.17	
Output Current (RMS)	187.928		187.89		187.892		187.89	
Total power delivered by sources (W)	996238.5		996198		996191.1		996188.4	
Losses (W)	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses	Losses (W)	% Losses
Conduction Loss	6787.98	0.695	6928.53	0.695	6928.23	0.695	6937.95	0.696
Switching Loss	2972.013	0.259	5318.85	0.534	8110.56	0.814	10957.8	1.10
Total Loss	9765.57	0.955	12251.37	1.23	15057.87	1.51	17906.34	1.80

Installed KVA of IGBT: 79200

Table 6-15 Simulation Result for 6.6kV CHB (4 Cells) Converter

Figure 6-13 Percentage Loss vs. Device Switching Frequency for 6.6kV CHB (4 Cells)

Simulation Results for Switching Frequencies 500Hz, 1000Hz, 1500Hz and 2000Hz for 6.6kV CHB (4 Cells) inverter:

Harmonics Order	% Harmonics at Device switching frequency (Hz)			
	500	1000	1500	2000
0	1.2E-08	8.8E-09	-5.4E-09	1.2E-08
1	100	100	100	100
2	7.1E-09	2.6E-09	2.8E-09	3.2E-09
3	1.1E-05	2.9E-06	1.4E-06	7.4E-07
4	3.0E-09	4.8E-10	1.7E-09	6.7E-10
5	6.8E-05	6.2E-05	3.9E-05	2.4E-05
6	1.6E-09	6.0E-10	1.2E-09	2.3E-10
7	7.3E-05	6.0E-05	3.9E-05	2.5E-05
8	1.2E-09	4.2E-10	9.0E-10	2.0E-10
9	1.3E-05	5.2E-06	9.7E-07	6.9E-07
10	1.1E-09	1.3E-10	5.5E-10	7.2E-11
11	3.3E-05	4.2E-05	2.8E-05	1.7E-05
12	7.6E-10	2.5E-10	6.0E-10	1.5E-10
13	4.1E-05	4.2E-05	2.8E-05	1.8E-05
14	7.4E-10	2.7E-10	4.7E-10	1.8E-10
15	2.2E-05	9.9E-06	5.1E-06	9.4E-07
16	6.8E-10	1.6E-10	4.6E-10	5.7E-11
17	1.2E-05	1.5E-05	1.1E-05	9.5E-06
18	5.4E-10	2.1E-10	3.0E-10	6.0E-11
19	1.2E-05	1.7E-05	1.4E-05	9.9E-06
20	5.4E-10	1.4E-10	3.1E-10	8.3E-11
% THD	0.000117	0.000108	7.01E-05	4.51E-05

Table 6-16 % Harmonics and % THD of Output Current Waveform for 6.6kV CHB (4 Cells) Converter

It can be observed that for 6.6kV CHB (4 Cells) inverter all individual current harmonics as well as the THD complies with the IEEE Std 519-1992 Harmonic Current Limits (Ref. Table 6-1) for the entire range of switching frequency.

6.3.3.3. Consolidation of Losses Data and the % THD of current waveform for Topology selection for 6.6kV Inverter

Switching Frequency= 500Hz	CHB (2 Cells)	CHB (4Cells)
% Conduction Loss	0.396	0.695
% Switching Loss	0.753	0.259
% Total Loss	1.15	0.954
%THD (for Current)	9.94E-05	0.000117
Installed KVA of IGBT	70200	126720

Switching Frequency= 1000Hz	CHB (2 Cells)	CHB (4Cells)
% Conduction Loss	0.397	0.695
% Switching Loss	1.57	0.534
% Total Loss	1.97	1.23
% THD (for Current)	8.45E-05	0.000108
Installed KVA of IGBT	70200	126720

Switching Frequency= 1500Hz	CHB (2 Cells)	CHB (4Cells)
% Conduction Loss	0.398	0.695
% Switching Loss	2.42	0.814
% Total Loss	2.81	1.51
% THD (for Current)	6.63E-05	7.01E-05
Installed KVA of IGBT	70200	126720

Switching Frequency= 2000Hz	CHB (2 Cells)	CHB (4Cells)
% Conduction Loss	0.400	0.696
% Switching Loss	3.31	1.10
% Total Loss	3.71	1.80
THD (for Current)	4.85E-05	4.51E-05
Installed KVA of IGBT	70200	126720

The % Total losses for all three circuits has been summarized below for entire switching range to illustrate the variation of the % total losses with respect to switching frequency.

Figure 6-14 Comparison of %Total Losses for Different Topologies of MLI with respect to Switching Frequency for 6.6kV Converters

The THD for all three circuits has been summarized below for entire switching range to illustrate the variation of the THD with respect to switching frequency.

Figure 6-15 Comparison of %THD for Current waveform for Different Topologies of MLI with respect to Switching Frequency for 6.6kV Converters

6.3.3.4. Topology Selection for 6.6kV Converter for Different Switching Frequencies

From the data tabulated above and the corresponding figure for comparing the % total loss and switching frequency as well as THD with switching frequency, it has been found that:

- 1) For 500Hz switching frequency, the current harmonics for both the CHB (2 Cells) and CHB(4 Cells) converters are within the compliance of standard harmonic limit. But the losses for the CHB (4 Cells) converter is the least among the two converters. Hence, for the 6.6 kV converter with a switching frequency of 500Hz, CHB (4 Cell) converter is the preferable over the CHB (2 Cells).
- 2) For 1000Hz switching frequency, for CHB (2 Cells) and CHB(4 Cells) converters, both comply with the harmonics limit. But the losses for the CHB (4 Cells) converter is the least among the three converter topologies. Hence, for the 6.6 kV converter with a switching frequency of 1000Hz, CHB (4 Cell) converter is the preferable over the CHB (2 Cells).
- 3) For 1500Hz switching frequency, for CHB (2 Cells) and CHB(4 Cells) converters, both comply with the harmonics limit. But the losses for the CHB (4 Cells) converter is the least among the three converter topologies. Hence, for the 6.6 kV converter with a

switching frequency of 1000Hz, CHB (4 Cell) converter is the preferable over the CHB (2 Cells).

- 4) For 2000Hz switching frequency, for CHB (2 Cells) and CHB(4 Cells) converters, both comply with the harmonics limit. But the losses for the CHB (4 Cells) converter is the least among the three converter topologies. Hence, for the 6.6 kV converter with a switching frequency of 1000Hz, CHB (4 Cell) converter is the preferable over the CHB (2 Cells).

7. Conclusion and Further Studies

7.1. Conclusion:

Since the converter topology with the minimal losses is hugely desired, its selection from the pool of topologies also requires a detailed analysis of the total losses and the corresponding THD level for the output currents. For example the converter with the very low percentage loss with a very high presence of low order harmonic content is of no use. So the quality of power delivered by the inverter is also important criteria of selection of a converter topology along with the efficiency of the inverter. But in the case of power quality, the THD can be minimized by the use of the filters in the load side. Also the use of inductive loads will effectively filter out the high order harmonics. So although both efficiency and the THD criteria will play their part in topology selection, selection of the converter with the least amount of losses should be the priority.

Although in Simulation Results of Chapter 6, we've found that the CHB (4 Cells) converter is suitable from both the efficiency as well as the power quality point of view but in general there is certainly not a single topology which is the most efficient one in all the cases. The most optimum topology of the converter used in the MV application depends on the switching frequency employed, and also on the required output voltage.

It can also be seen that the harmonic content in the output current of the inverter depends on the switching frequency. This has been illustrated by the data obtained from simulation, for a given converter topology, the THD for the output current of the inverters decreases with the increase in the switching frequency.

So while selecting the most efficient topology, the data related to the percentage total losses is referred. While selecting the best possible topology the harmonic content of the output current also needs to be considered along with the percentage total losses. The one with the least percentage losses and the least THD value would be considered as the best topology for that particular switching frequency and for that particular output voltage.

7.2. Future Studies:

The cost factor of an inverter is also a deciding factor while selecting the best inverter topology. The cost of the converter increases with the increase in number and the current and voltage ratings of the switching components. This is because higher the kVA rating, more is the silicon requirement and hence more is the cost.

Hence this factor compares the different IGBT topologies from the economic vantage point based on the cost of the silicon expressed in terms of kVA. Further study can be done in this

front. The comparison inclusive of all three factors viz. losses, THD and the cost factors would decide the best possible topologies with the lesser losses, lesser current harmonics and lesser cost.

In this study, only the losses on each topology for different switching frequencies, for different operating voltages have been studied. Along with this, comparison based on the harmonic analysis has also been touched briefly.

The amplitude modulation index has been fixed throughout the entire study. But, both the power quality and losses will be varied significantly with this index. Further study needs to be done on the changes in efficiency and the power quality based on the changes in the modulation index of each topology.

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