Time mode analog-to-digital converter

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**NANYANG
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CONVERTER**

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TIME MODE ANALOG-TO-DIGITAL CONVERTER

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ABSTRACT

Fully digital Analog-to-Digital Converter (ADC) and digitally assisted ADC has gained popularity in recent research works. The continuous scaling in CMOS technology has prompted designers to look for ADC architecture that is highly digital intensive with minimal analog circuitry. Time Mode ADC appears as an attractive solution due to its more digital intensive topology. As transistor's gate delay reduces along with scaling in CMOS technology, the resolution and speed of Time Mode ADC also improve along with the advancement in modern CMOS technology.

There are two popular types of Time Mode ADC, namely the Voltage-Controlled-Oscillator (VCO) based ADC and the Integrating ADC. The VCO-based ADC works by first converting analog input voltage to frequency/time information by a VCO, where the frequency/time information is subsequently converted to digital code using a time-to-digital converter. Although high speed high resolution time-to-digital converters are currently available, the inherent nonlinear property of VCO however has become the bottleneck for Time Mode VCO- based ADC.

In the first part of this research work, a new concept named K-locked-loop is proposed to solve the nonlinearity issue of VCO within a time mode ADC. The main idea of K-locked-loop is to use local feedback in the voltage-time domain for VCO nonlinearity suppression. To the best of the author's knowledge, this is the first ever proposed feedback system in the voltage-time domain. A 10-bit, 2MS/s K-locked-loop VCO ADC has been modeled using SIMULINK tool in Matlab as a proof of concept. In addition, an AMS model is constructed to further verify the concept of K-locked-loop at the transistor level. Through analysis, the non-ideal effect will be discussed in this thesis.

The second part of this research work will focus on the Integrating ADC. A new architecture of the All-Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL) for Time Mode integrating ADC is proposed. The proposed ADMMDLL further interpolate the clock to enhance the Integrating ADC resolution. It exploits the advantages of digital design – faster design cycle, more robust, and better scalability in modern CMOS technology. Measurement result is finally presented to verify the working principle of this architecture.

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Chapter 1 Introduction

1.1 Motivation

Contemporary Integrated Circuits (ICs) are mixed signal systems consisting of a large digital core such as Central Processing Unit (CPU), Digital Signal Processor (DSP) and memory, and surrounded by several analog interface blocks such as I/O, ADC, RF front ends, and more [1]. The rapid advancement in the integrated circuit technology have made it possible to construct highly sophisticated digital systems capable of performing complex digital signal processing tasks, which are usually less expensive, more reliable and flexible compared to the analog counterpart [2]. While most of the signal processing tasks that were conventionally performed by the analog means are realized today in the digital domain, an ADC is always needed as the interface circuit due to the fact that our real world signals such as speech, biological signals, radar signals, video signals, sonar signal, and etc are analog in nature.

A conventional analog data processing system is illustrated in Fig. 1.1, which consists of an anti-aliasing filter, an ADC, a Digital Signal Processor (DSP), a Digital-to-analog converter (DAC), and a reconstruction filter.

The performance of the ADC will determine the digital system's basic performance, such as data rate, sensitivity, signal dynamic range, bit error rate, and power consumption. Expectations on the performance of ADCs have been continuously increasing along with the advancement in digital system performance [3]. Various kinds of ADC have been employed for a variety of applications. Examples include data acquisition systems, communication systems, sensor networks, test and measurement apparatus, and consumer electronics. Each

application requires different performance specification of ADC in term of resolution and speed. For example, high speed data acquisition system need ADC with high speed and low resolution requirement, and flash ADC or subranging ADC are best fit for those applications. On the other hand, energy monitoring system with high resolution and low speed requirement can best be met using integrating type ADC or sigma-delta ADC.

Figure 1.1 A conventional analog processing system

The evolution in CMOS technology is motivated by the decreasing price-per-performance for digital circuitry. As such, CMOS processes are typically optimized for improved digital switching speeds and reduced transistor geometries for higher packing density. As the CMOS technologies reduce transistors feature size dimensions, the gate oxide thickness is reduced, forcing the system supply voltage to decrease. Lower supply voltage is expected to cause serious roadblocks for analog circuits, because the signal headroom becomes too small to design circuits with sufficient signal integrity at a reasonable power consumption level [1]. The signal-to-noise ratio (SNR) also suffers as the signal amplitude is continuously scaled down but noise does not scale accordingly. Furthermore, scaling in technology makes the Early Voltage of the MOS transistor to decrease, causing a reduction in the

amplifier's gain. All these challenges spur strong research interest for new ADC architectures in use for the new generation of CMOS technologies [3].

A potential candidate to replace conventional voltage mode ADC such as flash ADC, pipeline ADC, successive approximation ADC, etc is the time mode ADC. The circuits involved in time mode ADC comprise mainly of digital circuits such as counter and latch. Time mode ADC can benefit from the digital CMOS technology due to its highly digital intensive topology. Therefore, it is expected that the time mode ADC can operate at higher speed, consume lower power and have higher packing density. The general topology of the time mode ADC is illustrated in Fig. 1.2.

The operation of the time mode ADC starts by first converting the analog input voltage $V_{in}(t)$ to time domain signal using a voltage-to-time converter (VTC), where the signal is further processed by time domain processing circuitry. Finally a time-to-digital converter (TDC) is used to transform the time information into the final digital output code [4]. While the time domain processing circuitry and the TDC comprise purely of digital circuits, the VTC block is the only remaining mixed signal circuit, e.g., a Voltage Control Oscillator (VCO). The nonlinearity of the VCO has significant impact on the performance of the time mode ADC, limiting the input ranges since the VCO is only linear around a limited input region. As such a great research potential remain for new techniques to suppress the VCO nonlinearity.

Figure 1.2 Time mode ADC

1.2 Objectives

The first objective of this thesis is to propose a novel approach in order to solve nonlinearity issue of the VCO for the Time Mode ADC application. The novel approach is named as K-locked-loop. The philosophy behind this idea is to look into the nonlinearity of the VCO from a new perspective. The feasibility of this approach, its mathematical model, as well as simulation result is then presented. Recommendation and future works are proposed for researchers who are researching about the feasibility of this approach.

The second objective of this thesis is to propose a new architecture of the All Digital Multiphase Multiplying Delay-locked Loop for the time mode ADC application. The idea is to push the processing jobs to the digital domain and make the circuit as digital as possible. It makes use of the advantages of the digital design – faster design cycle, smaller area and the ease of portability to another CMOS process.

1.3 Thesis Organization

The thesis has five main chapters. Chapter 2 reviews on the state-of-the art of the Time Mode ADC architecture. The working principle of the proposed K-locked-loop is analyzed in chapter 3, including the modeling and simulation result. Chapter 4 reveals the proposed ADPLL for the Time Mode ADC application. Finally, a conclusion and future works is discussed in chapter 5.

1.4 Thesis Contribution

The first contribution of this thesis is to propose a new concept named K-locked-loop to solve the nonlinearity issue of VCO within a time mode ADC. The main idea of the K-locked-loop is to use local feedback in the voltage-time domain for VCO nonlinearity suppression. To the best of the author's knowledge, this is the first ever proposed feedback system in the voltage-time domain. The main architecture of K-locked-loop, its main building blocks as well as a thorough mathematical analysis will be presented in this thesis.

The second contribution of this research work is to propose a new architecture of the All-Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL) for Time Mode integrating ADC. The proposed ADMMDLL further interpolate the clock to enhance the Integrating ADC resolution. It exploits the advantages of digital design – faster design cycle, more robust, and better scalability in modern CMOS technology. Measurement result is finally presented to verify the working principle of this architecture.

Chapter 2. Review on Time Mode ADC architectures

The Time Mode ADC can be broadly categorized into the VCO based Time Mode ADC and the integrating type Time Mode ADC. The VCO based ADCs have emerged as an attractive solution due to its highly digital intensive circuit architecture, inherent noise shaping characteristic, as well as its anti-aliasing property. However, the nonlinear behavior of VCO's voltage-to-frequency characteristic has severe limitation on the performance of the VCO based ADC. Different techniques have been proposed to solve the VCO nonlinearity issue, which can be sub-divided into two main architectures: the Open loop architecture and the Closed loop architecture. The state of the art of the Open Loop VCO based ADC architectures will be reviewed in Section 2.1, while the VCO based Closed Loop ADC architectures will be discussed in section 2.2.

Section 2.3 will review on another type of Time Mode ADC, namely the integrating type ADC. Different techniques for improving the time resolution of integrating type ADC will be summarized, including the use of delay line for time interpolation.

2.1 Open Loop VCO based ADC Architectures

Several techniques have been proposed to solve the nonlinearity issue of Open Loop VCO based ADC. Among the recent popular approaches including the use of enhanced linear delay element [6]-[7], digital calibration technique [9]-[12],

Pulse Width Modulation (PWM) approach [21]-[23], as well as the two stages VCO based ADC [24]. Each of these techniques will be reviewed in this section.

2.1.1 Enhanced linear delay element Open Loop VCO based ADC

Figure2.1 Enhanced Linear delay element Open Loop VCO based ADC topology

The operation of an enhanced linear delay element Open Loop VCO based ADC can be best described by Fig.2.1. The VCO first converts the continuous time analog input voltage, $V_{in}(t)$ into a time/frequency information, in which the frequency is proportional to the average analog input voltage $V_{in}(t)$, as shown in Fig.2.2(a). A phase quantizer (e.g. a digital counter) will then convert the frequency information into a digital code by quantizing the frequency/time information, before being encoded by a digital encoder. Ideally, the resolution of the VCO based ADC is improved with continuous scaling in CMOS technology, since the time resolution of the digital gates improves with smaller CMOS technology dimension.

However, the actual voltage-to-frequency characteristic of a VCO as shown in Fig.2.2(b), where the linear range of VCO is limited, thereby limiting the resolution of ADC to be less than 10 bits without any digital calibration [5]. Several

techniques have been proposed to linearize the VCO, including the use of cross-coupled current starved delay element [6]-[7] and single-ended enhanced linearity delay element [8]. The block diagram of the cross-coupled current starved delay element is shown in Fig. 2.3, it consists of two pull down NMOS transistors which determine the delay, and NMOS latch for high positive feedback gain and two PMOS input transistors. The block diagram of the single-ended enhanced linearity delay element is shown in Fig.2.4. The single-ended delay element consists of two inverters in parallel. The sizing of transistors Q3 and Q4 should be much larger than Q5 such that the on resistance of Q5 much larger than Q3 and Q4. In this way, the delay would become mainly a function of the current passing through Q5, and consequently as a function of V_{in} . However, both reported techniques are not able to achieve more than 10 bits resolution, as the VCO nonlinearity limits the performance of the ADC.

Figure.2.2(a) Ideal voltage-to-frequency characteristic of VCO

Figure.2.2 (b) Actual voltage-to-frequency characteristic of VCO

Figure.2.3 Cross-coupled differential delay element

Figure.2.4. Single-ended enhanced linearity current starved

2.1.2 Open Loop VCO based ADC with Digital calibration

The limitation of the enhanced linear delay element method has led to other linearization technique. Another popular open loop technique is using digital calibration technique. The architecture of an Open Loop VCO based ADC with digital foreground calibration is shown in Fig. 2.5(a). The architecture is similar to the Open Loop VCO based ADC with Enhanced linear delay element, except that a Look-up Table (LUT) is employed for the VCO nonlinearity correction. The VCO characteristic is pre-stored in a LUT, the LUT then maps the digital code according to the pre-characterized VCO behavior. The LUT is in fact the inverse transfer

function of the VCO tuning Curve [9-12]. Fig.2.5(b) illustrate the concept of digital calibration using the Look Up Table approach.

The resolution of the ADC can be further improved by using the interleaving ADCs in parallel [13-15] or by using the Time Interpolation approach to achieve sub-gate delay resolution [16, 17] .While all of these architectures are all-digital in nature, the characteristic of the VCO drifts with the change in temperature, thus requiring the VCO to be recalibrated by interrupting the normal ADC operation.

Recently reported VCO based ADC with digital background calibration can avoid interrupting the ADC, at the cost of requiring a high performance V-I Converter and complex digital calibration engine [18-20]. The Look Up Table data is updated periodically by the Calibration Unit without interrupting the normal ADC operation. The dynamic range is also improved by automatically retuning the VCO center frequency by the Digital Bias Control. The circuit architecture of Open Loop VCO based ADC with digital background calibration is best summarized in Fig.2.6. The main drawback of this digital background calibration method, however, is the matching between the replica and the main VCO needed for good cancellation of the nonlinearity which is difficult to ensure in deep-submicron CMOS processes. Furthermore, the calibration algorithm is complex and takes very long to converge. Another main drawback is since the open loop architecture is limited to 1st order noise shaping, the sampling clock is required to operate at multi-GHz range to get high SNR.

Figure.2.5 (a) Open Loop VCO based ADC with Digital foreground calibration

Figure.2.5 (b) Lookup Table based Calibration method

Figure.2.6 Open Loop VCO based ADC with Digital background calibration

2.1.3. PWM Modulation VCO based ADC

Figure.2.7(a) . Open Loop VCO based ADC architecture with PWM Modulation

Figure.2.7(b). Corresponding output spectrum of PWM VCO based ADC

To avoid the complex digital background calibration, another recently popularized technique using Pulse Width Modulation (PWM) has been proposed. The Pulse Width Modulation (PWM) technique as shown in Fig.2.7 does not require calibration engine for VCO nonlinearity correction [21-23]. Instead, it operates the VCO at only two output frequencies. The PWM output drives the VCO at either F_{HIGH} (correspond to V_{HIGH}) or F_{LOW} (correspond to V_{LOW}). The output is a scaled version of its input, thus the Voltage-to-Frequency conversion is perfectly linear. The

disadvantage of this approach, however, is the requirement of the two active RC integrator and voltage comparator in the PWM unit, which are getting harder to design in modern CMOS technology.

Ideally, naturally sampled PWM does not produce any distortion tones within the signal band. However, as shown in the representative output spectrum in Fig. 2.7(b), many tones around the PWM carrier frequency is created [23]. Increasing the carrier frequency to push these tones to higher frequencies will increase power dissipation in the PWM generation circuitry. Furthermore, the quantization error suppression is also limited by first-order noise shaping.

2.1.4. Two stage ADC with VCO based second stage

Figure.2.8. Two stage ADC with VCO based second stage

The first attempt to employ VCO-based ADC into the traditional two-step ADC has been reported in [24] and the architecture is shown in Fig.2.8. The architecture consists of a traditional voltage-domain first stage, followed by a time-domain second stage. The first stage does the coarse quantization, which is 5-bit as reported in reference [24], and the residue is quantized by the second stage VCO-based ADC. The linearity requirement on the VCO is reduced by the number of bits obtained from the first stage. To reduce the Op-Amp gain requirement, the reference to the second stage is scaled by a factor of eight. The feedback factor is also increased to reduce its output swing. This is not very practical in traditional two-step designs because the reduced voltage range makes the design of the flash converter in the second stage very difficult. However, with a VCO-based second stage, it actually helps to linearize the VCO by reducing the input voltage range.

While the proposed VCO-based two-stage ADC can alleviate the linearity requirement on VCO, the proposed architecture achievable maximum SNR is around 73dB, limited by Op-Amp noise. The first stage is still very analog in nature and does not scale well with technology.

2.2 Closed Loop VCO based ADC

2.2.1 Closed Loop VCO based sigma Delta ADC

Figure.2.9 Closed Loop VCO based Sigma Delta ADC

The very first concept of VCO based sigma delta ADC utilize VCO as a multi-bit quantizer is shown in Fig.2.9. By placing the VCO within an analog feedback path, the nonlinearity of VCO is suppressed due to the presence of high gain before the VCO input. The inherent noise shaping property of the VCO quantizer also adds one order of noise shaping to the sigma delta ADC, without significantly impacting the sigma delta loop dynamics[25, 26].

However, since the VCO quantizer will span the whole input range, the entire nonlinear VCO tuning curve will be exercised, this in turn results with the need of a very high gain loop filter to suppress the VCO nonlinearity. Since the VCO based quantizer can only be used as the last stage, high performance analog circuitry is still required at the front stage, which is getting harder to design in modern CMOS

technology. To further improve SFDR performance, higher order loop filter is needed. But higher order loop filter will degrade the loop stability and increase the power dissipation [27-29].

In [30, 31], a variation of the Sigma-Delta VCO-based ADC named residue cancellation technique is recently proposed, as introduced in the next section. The advantage of the residue cancelling technique is that the VCO input could only span a very small input range, thus avoiding the VCO linearity issue in conventional VCO based Sigma Delta ADC.

2.2.2 Closed Loop Residue Canceling VCO based Sigma Delta ADC

The architecture of the Residue Cancelling VCO based Sigma Delta ADC is similar to the conventional closed loop Sigma-delta VCO ADC, except that the output of the loop filter is not directly fed to the input of the VCO quantizer. Instead it is coarsely quantized by the 1st ADC and only the residue, V_{res} is fed to VCO quantizer, as shown in Fig.2.10. The impact of VCO nonlinearity on the ADC performance can be suppressed by not exercising the nonlinear region of the VCO's V-to-F transfer curve.

While in principle this residue cancellation technique is effective in suppressing the distortion due to VCO nonlinearity, the nonlinearity of 1st ADC and 1st DAC circuitries however limit their performance in practice. Furthermore, the loop filter in the front stage is also implemented using high performance analog circuitry, similar to the conventional VCO-based Sigma Delta ADC.

Figure.2.10 Closed Loop Residue Canceling VCO based Sigma Delta ADC

2.2.3 Closed Loop multi-rate MASH VCO based ADC

As discussed previously in section 2.2.1, high SNR can be achieved by increasing the order of the modulator but it is accompanied by potential instability and high power consumption. An alternative solution is to use a multistage noise shaping structure (MASH) [32-37], where a chain of lower orders Sigma Delta ADCs are cascaded.

Multi-rate MASH ADC can mitigate the power penalty by having a lower frequency sampling clock in the first stage, followed by a higher frequency sampling clock in the second stage, as shown in Fig.2.11. VCO based ADC is used in the second stage to exploit the advantage of its faster speed and higher resolution in the deep sub-micron CMOS technology. To further suppress the nonlinearity of the VCO, the second stage VCO processes only the quantization error from the first

stage. The small amplitude and signal independent nature of the quantization noise error significantly reduces the sensitivity of the overall ADC performance to the VCO nonlinearity [38, 39].

Figure.2.11 Closed Loop multi-rate MASH VCO based ADC

2.2.4 Closed Loop K-locked-loop VCO based ADC

The concept of K-locked-loop is first reported in [40, 41]. Unlike the VCO based sigma delta ADC, the K-locked-loop is a nyquist rate ADC, with feedback in voltage-time (V.S) domain to solve the VCO nonlinearity issue. The architecture of K-locked-loop is shown in Fig.2.12.

A thorough analysis of the K-locked-loop, including the mathematical model, advantages as well as disadvantages is the main focus of this thesis, and will be explored in chapter 3.

Figure.2.12 K-locked-loop VCO based ADC

To summarize the performance of different VCO-based ADC (Open Loop and Closed Loop), a summary table listing the performance comparison of each topology is shown in Table 2.1.

Table 2.1: Summary table of VCO-based ADC

	Open Loop VCO based ADC			Closed Loop VCO based ADC		
Architecture	Enhanced linear delay element [6]	Digital calibration [19]	PWM Modulation [22]	VCO based sigma Delta ADC [27]	Residue Cancelling VCO based Sigma Delta ADC [30]	Multi-rate MASH VCO based ADC [39]
Technology (nm)	350	65	90	130	90	130
Area (mm ²)	-	0.07	0.1	0.45	0.36	0.7
Signal BW (MHz)	1 E-5	9	8	20	10	4
OSR	-	64	40	22.5	30	150
SNDR (dB)	60	73	59.1	78.1	78.3	77
Power (mW)	0.09	17	4.3	87	16	13.8
FoM (fJ/Conv-step)	-	258	366	331	120	298

From the summary table, it can be seen that generally Open Loop VCO based ADC has limitation in achieving higher SNDR, this is especially true for Enhanced Linear Delay Element method and PWM Modulation Method. Digital calibration method can achieve higher SNDR compared to other Open Loop Method with higher Over Sampling Ratio (OSR), at the expense of higher power consumption.

Closed Loop VCO based Sigma Delta ADC can achieve higher SNDR (>77dB). Among all the Closed Loop architecture, Residue-cancelling VCO based Sigma Delta ADC can achieve the best FoM (fJ/conv-step). In view of the advantage of Closed Loop architecture, this research work focus on exploring new architecture in Closed Loop architecture with feedback in voltage-time domain named K-locked-loop. Chapter 3 shows the detail analysis and design of this newly proposed concept.

2.3 Integrating type of Time Mode ADC

In this section, a general topology of integrating time mode ADC will first be reviewed in section 2.3.1. Recent techniques to improve the resolution of integrating ADC including the use of Time-to-Digital converter and Delay-locked-Loop will be introduced in section 2.3.2.

2.3.1. Integrating ADC topology

Integrating type time mode ADC is a classical means of implementing an ADC taking advantage of having a very simple implementation with minimal analog circuitry. The key operating principle of the integrating time mode ADC is to translate an input voltage to a ramp signal in time domain, and the time duration it takes for the ramp to pass a given threshold voltage is then measured. Typically, the time measurement is performed with a digital counter, whose time resolution corresponds to the counter clock period [42, 43].

Fig.2.13 (a) shows the general topology of an integrating time mode ADC, where the analog input voltage is fed into the analog RC integrator. The output voltage of the Op-Amp, which is a ramp signal, is then fed into an analog comparator. Once the ramp signal crosses the comparator's reference voltage (V_{ref}), the output of the comparator will go high, which reset the counting cycle.

Recently, Time-to-Digital converter (typically embedded inside a Delay-locked-loop) has been adopted to enhance the resolution of the conventional integrating ADC [44-48]. Different Time-to-Digital converter architectures will be reviewed in the following section.

(a)

(b)

Figure.2.13 (a) Integrating ADC circuit topology (b) Timing diagram of an integrating ADC

2.3.2 Time-to-Digital Circuitry (TDC)

To further improve the resolution of the integrating ADC, the counter resolution can be further improved using various techniques. Time-to-Digital Converter has been adopted to improve the time resolution of Time Mode ADC. Time-to-digital converter (TDC) is a system that performs a time interval measurement and converts the result into digital code. High resolution TDCs can be found in a variety of measurement systems, such as time-of-flight measurement, jitter measurement, laser range finders, logic analyzer, etc [49-51]. Among the popular TDC techniques include simple delay line method, vernier-delay line method, pulse shrinking method, time amplification method, gated ring oscillator method, as well as passive time interpolation method. Each of these methods will be briefly reviewed in this section.

2.3.2.1 Simple Delay Line and Vernier Delay Line TDC

The simple delay line TDC, which consists of a delay line, a latch and an encoder is perhaps the simplest type of TDC, as shown in Fig. 2.14(a). The operation principle of the simple delay line TDC is straightforward: a start signal first propagates along the delay line; the state of the delay line is sampled on the rising edge of the stop signal. The total number of passes through the delay element represents the digital value of the time difference between the start and the stop signal [52, 53]. The advantages of this delay line TDC lie in its simplicity in the circuit construction. However, the resolution is limited by the smallest delay of the delay element, which is two inverters delay.

(a)

Figure.2.14 (a) Simple delay line TDC. (b) Vernier delay line TDC

In order to improve the resolution of TDC to achieve sub-gate delay, Vernier delay line TDC can be used, as shown in Fig. 2.14(b). In this approach, both the start and the stop signals are delayed independently in two delay lines. The delay elements for the stop signal ($t_d - \alpha$) are designed to be slightly faster than those of the start signal (t_d). Therefore, the stop signal will eventually catch up with the start signal

due to its smaller delay. Early-late detector such as the flip-flops will detect the position of the delay element in which the stop signal outrun the start signal, thus providing the digital code for the time difference between the start and the stop signal.[54, 55].

While high resolution can be achieved using Vernier delay line TDC, where the resolution is given by the time difference between both delay lines (which is α in this case), the conversion time increase linearly with the time interval. Thus, for large time interval between the start and the stop signal, or for small α value, the TDC will be very slow and expensive in silicon area.

To overcome the large area issue, two-level conversions have been applied successfully to achieve wide input range and high resolution at the same time. In this method, time interval is converted using a simple delay line in the first conversion, where the time is digitized to the nearest multiple of a constant element delay. The sub-gate delay is then carried out using Vernier delay line in the second conversion. By employing the two level conversions technique, the number of second level Vernier delay line sampler can be reduced significantly, thus solving the large area issue by using Vernier delay line TDC alone.

2.3.2.2 Pulse Shrinking Method

The working principle of a Pulse-shrinking TDC is similar to Vernier principle. The area penalty for using two separate delay lines is mitigated by employing different rise time delay t_r and fall time delay t_f in a single delay line, resulting in a Pulse-shrinking delay line [56, 57]. An example of Pulse-shrinking TDC is shown in Fig.2.15.

Figure 2.15 Pulse-shrinking TDC

A digital front-end circuit is used to convert the time interval of the start signal and the stop signal into a pulse width of the same duration. The Pulse-shrinking delay element is composed of two unequal sizing inverters. For unequally sized inverters, the pulse width is changed by:

$$T_{\text{LSB}} = t_{r1} + t_{f2} - t_{r2} - t_{f1} \quad (2.1)$$

where t_{r1} is the rise time of the first inverter, t_{r2} is the rise time of the second inverter, t_{f1} is the fall time of the first inverter, and t_{f2} is the fall time of the second inverter. A pulse extinction detector such as an R-S flip-flop can be used to detect when the propagating pulse has been shrunk to a duration below the R-S flip-flop set time. The end of the propagation position is then decoded to a digital value through a thermometer logic circuit, producing the final digital output. The disadvantage of this method as compared to Vernier delay line is the calibration

method involved is usually more complicated. Calibration is need in all TDCs to ensure the invariance of TDCs against process, temperature, and supply voltage fluctuation.

2.3.2.3 Time Amplification Method

All the TDCs discussed up to now are in close analogy to FLASH conversion in ADC. The time amplification TDC reviewed here is based on the concept of two-step ADC – improves the resolution by amplifying the residue between the input and the closest coarse level [58-60]. A coarse-fine (two-step) TDC become feasible only if the time amplifier (TA) can be realized. A possible implementation of the TA is shown in Fig. 2.16(a), with the associated timing diagram shown in Fig. 2.16(b)

The very first TA was reported in [58]. The invention of the TA and the improvement of its performance over the years have made time-amplification TDC feasible nowadays. An example of time-amplification TDC is shown in Fig. 2.17. Since the input time cannot be stored, every possible time residue must be created and amplified separately. Each amplified residue then goes to a multiplexer (MUX). The coarse code will indicate which residue to be selected for conversion in the fine TDC. In this circuit, an arbiter (A) is used as the latching comparator because it has equal delay from its two inputs, from the start and the stop signals to the output. Note that the TA gain variation and offset can be compensated using digital calibration technique, and the linearity of the converter can be improved using an INL look up table.

(a)

(b)

Figure 2.16 (a) Time amplifier schematic (b) example timing diagram for time amplifier

Figure 2.17 Time amplification TDC

2.3.2.4 Gated Ring Oscillator Method

Gated-ring-oscillator (GRO) TDC performs an operation analogous to sigma-delta ADCs by noise shaping the quantization noise of the TDC, thereby improving the effective resolution of the TDC. Fig. 2.18 shows the GRO TDC and the associated gated inverter. The gated inverter operates as a normal inverter when it is enabled, and disconnect from the power supply to hold the charge on the parasitic output capacitance when it is disabled. The GRO only allows the oscillator to have transitions (gate enabled) during a given measurement interval, and freeze the ring oscillator (gate disabled) between measurements [61, 62].

The benefit of gating the inverter to enable or disable the oscillation is that the residue occurring at the end of a given measurement interval, $T_{\text{stop}}[k-1]$ can be transferred to the next measurement interval, $T_{\text{start}}[k]$. This property can achieve first-

order noise shaping on the quantization noise. To see how this can happen, consider the timing diagram shown in Fig. 2.19. We first note that

$$T_{\text{start}}[k] = T_{\text{stop}}[k-1] \quad (2.2)$$

The overall quantization error for a given measurement interval, T_{error} , is then given by:

$$T_{\text{error}}[k] = T_{\text{stop}}[k] - T_{\text{start}}[k] = T_{\text{stop}}[k] - T_{\text{stop}}[k-1] \quad (2.3)$$

The discrete-time first-order difference operation is equivalent to the first-order noise shaping in frequency domain. So this confirms the first order noise shaping property of the GRO TDC. As such, there is no need to perform calibration for the TDC, even in the presence of large mismatch.

Figure 2.18 Gated-ring-oscillator TDC

Figure 2.19 Timing diagram to illustrate the concept of Gated-ring-oscillator TDC

2.3.2.5 Passive Time Interpolation Method

The idea of passive time interpolation method is dividing the delay of inverter to achieve sub-gate delay resolution. This can be done by connecting the resistors across inverters as shown in Fig.2.20 [63]. Since the interpolated signal is linearly dependent on the signals generated by inverter, the interpolated signals are thus monotonic in nature. As shown in Fig.2.20 (b), the interpolated signal is exactly parallel to signal V_A and V_B in the middle of the transition region, and this is sufficient for comparator to detect the transition. Due to this inherent monotonic nature and relatively simpler circuit construction, the time interpolation method can

be employed in Integrating Time Mode ADC application to improve ADC resolution, as proposed in Chapter 4.

(a)

(b)

Figure.2.20 (a) Passive local time interpolation TDC (b) Timing diagram of interpolated signal

Since the quantization noise of TDC is dependent on the width of the Least Significant Bit (LSB). Variation of delay in the delay element due to process

mismatch and layout limit the accuracy of the TDC. To overcome this problem, two popular methods are currently used, namely digital post-processing method, or the use of DLL/PLL to do calibration. By embedding the TDC within a DLL / PLL, the overall delay is equal to an external time reference independent of the process variations or environmental conditions.

In this thesis, a novel all digital multiphase multiplying Delay-locked-loop will be introduced in chapter 4 for the Time Mode ADC application. To the best of the author knowledge, there is no prior publication on the all digital multiplying multiphase Delay-locked-loop in integrating ADC application. A detailed analysis and design of the proposed *All Digital Multiphase Multiplying Delay locked Loop* will be explored in chapter 4.

Chapter 3 K-Locked Loop and its application in Time Mode ADC

This chapter will propose a novel Time Mode ADC architecture, namely K-locked-loop which based on the concept of feedback in voltage-time domain. In contrast to a conventional feedback amplifier or Phase-locked-loop, whereby feedback is done in the voltage or time domain respectively, K-locked-loop explore the concept of feedback in voltage-time domain, with a physical unit of V.S.

The equation of a VCO can be described by the following equation:

$$f_{KVC0} = K_{VC0} \cdot V_{in} \quad (3.1)$$

Alternatively, if we define T_{VCO} to be the period of the VCO oscillation, we can rewrite the equation of VCO to be:

$$T_{VCO} = \frac{K}{V_{in}} \quad (3.2)$$

Where $T_{VCO} = 1/f_{kvco}$ and $K = 1/K_{VCO}$

If the value of K is constant for the input range of interest, we can therefore prove that the digital output $D_j(V_{in})$ and input voltage V_{in} relationship is linear and given by:

$$D_j(V_{in}) = \int_{(j-1)T_s}^{jT_s} \frac{1}{T_{VCO}} dt = \frac{V_{in}}{K} T_s \quad (3.3)$$

In other words, the digital output $D_j(V_{in})$ of a time-mode ADC is linearly proportional to the analog input voltage V_{in} if and only if equation (3.2) holds, where K is constant for all the input value. In fact, most current-starved delay elements or other type of linearized delay elements obey (3.2) for small input range. However, for larger input range, the K value varies with input voltage change, as shown in Fig. 3.1.

Figure 3.1 Variation of K value across V_{in}

Therefore, we can surmise that the nonlinearity of a time-mode ADC originate from the nonlinearity of K value of VCO across the input range of interest. From Fig.3.1, we can see that the K value is lower than K_{ref} for V_{in} less than V_{ref} , and larger than K_{ref} for V_{in} larger than V_{ref} . The K parameter of a typical VCO is

dependent on the number of inverter stages, supply voltage, loading capacitor, etc. A detailed derivation of the K parameter will be elaborated in section 3.1 (Dual controlled Ring Oscillator).

Let's take a look at an example as shown in Fig.3.2

Figure 3.2 Variation of K value across Vin

Assuming the analog input voltage V_{in} pass through an ideal VCO that fulfill the equation of $T_{VCO} = K_{ref} / V_{in}$, which correspond to case 1 in Fig.3.2, The digital output $D_j(V_{in})$ and input voltage V_{in} relationship is linear and is given by

$$D_j(V_{in}) = \int_{(j-1)T_s}^{jT_s} \frac{1}{T_{VCO}} dt = \frac{V_{in}}{K_{ref}} T_s \quad (3.4)$$

On the other hand, the second case in Fig.3.2 referring to a non-ideal VCO, where the K value of the VCO is lower than the desired K_{ref} value ($K_1 < K_{ref}$). Assuming the K value can be varied and it is changed to K_2 at time t_2 , and

subsequently varied to K_3 at time instant t_3 and K_4 at time instant t_4 , such that the average value of K is equal to K_{ref} as shown below:

$$\frac{(K_1 + K_2 + K_3 + K_4)}{4} = K_{ref} \quad (3.5)$$

Effectively it is equivalent to converting the analog input voltage into time information by a linear equation of $T_{VCO} = K_{ref} / V_{in}$. This can be further illustrated in the timing diagram in Fig.3.3.

Figure 3.3 (a) Timing diagram of ideal VCO (b) Non-ideal VCO timing diagram

Equation 3.5 can be generalized to include variation of K value at n -th instances such that the average K value is equal to K_{ref} :

$$\frac{(K_1 + K_2 + .. + K_n)}{n} = \frac{1}{n} \sum_{i=1}^n K_i = K_{ref} \quad (3.6a)$$

If equation 3.6a holds, it can be shown that a non-ideal VCO with a varying K value such that the average K value is equal to K_{ref} will have a linear relationship between digital output $D_j(V_{in})$ and V_{in} , as shown in equation 3.6b below:

$$D_j(V_{in}) = \int_{(j-1)T_s}^{jT_s} \frac{1}{T_{VCO}} dt = \frac{V_{in}}{\frac{1}{n} \sum_{i=1}^n K_i} T_s = \frac{V_{in}}{K_{ref}} T_s \quad (3.6b)$$

The core working principle of K-locked-loop is varying the K value of a non-ideal VCO such that equation 3.6b is valid, and thus a linear relationship between digital output $D_j(V_{in})$ and V_{in} . The underlying assumptions made are:

1. The K value of a VCO can be tuned / varied
2. There exist a circuitry to compare the average K value against a desired K_{ref}
3. The time taken for average K value to be equal to K_{ref} must happen before each sampling clock T_s arrive for all input range of interest.

Each of these assumptions will be addressed in details in the following sections.

Recall from previous section the definition of $K = T_{VCO} \times V_{in}$, to tune the K value of VCO, the frequency of VCO must be controllable by at least two independent variables. An example of the VCO that serve the purpose is a Dual-Controlled Ring Oscillator circuitry. Fig.3.4 shows the architecture of the Dual-Controlled ring oscillator adopted in K-locked-loop. The frequency of the Dual-Controlled ring oscillator depends not only on the analog input voltage; it can also be tuned by adjusting the value of the load capacitance.

Figure 3.4 Dual-Controlled Ring Oscillator circuitry adopted in K-locked-loop

Fig.3.5 further illustrates the relationship between K and analog input voltage V_{in} as well as load capacitance C_L . As can be seen from Fig.3.5, K value increases with increasing input voltage, or larger C_L . If the input voltage is less than V_{ref} and thus has smaller K value than desired K_{ref} , the K value can be increased by increasing the load capacitance C_L ; similarly, for input voltage larger than V_{ref} , the K value can be brought to K_{ref} by reducing the load capacitance value.

Figure 3.5 Graph depicting nonlinear relationship between K and V_{in}

While we know that the K value of a non-ideal VCO can be tuned by adjusting the load capacitor value, it is the average K value that we are interested in, as shown previously in equation 3.6a. K -comparator is the circuitry in K -locked-loop that compares the average K value of VCO to the reference K_{ref} . Similar to the working principle of a voltage comparator, the K -comparator will output a zero if the average K value is smaller than K_{ref} , and vice versa. The circuit architecture and mathematical equations of K -comparator will be disclosed further in the next section.

Besides a Dual-controlled Ring Oscillator to enable the tuning of K value of the VCO, and the K -comparator to compare the average K value against the reference K_{ref} , there must exist a feedback loop to continuously adjusting the K value of VCO such that the average K value is as close as possible to K_{ref} . The decision to adjust the K value comes from a simple digital controller inside the feedback loop. This lead to the proposed architecture of K -locked-loop, as shown in Fig.3.6, the output of the K -locked-loop can then be quantized by a Time-to-Digital Converter

circuit, and the digital output $D_j(V_{in}, T_s)$ is proven linearly proportional to analog input voltage V_{in} .

Section 3.1 will discuss Dual-controlled Ring Oscillator, one of the main building blocks in K-locked-loop. Section 3.2 will reveal on the mathematic equation and circuitry of K-comparator, while the digital controller will be revealed at section 3.3. Non-idealities and limitations of K-locked-loop will be discussed in section 3.4. Section 3.5 will show the SIMULINK model and simulation result of K-locked-loop. Finally a discussion is drawn at section 3.6.

Figure 3.6 Architecture of K-locked-loop circuitry, together with Time-to-digital circuit to form a Time Mode ADC

3.1 Dual Controlled Ring Oscillator

The main function of the Dual-Controlled Ring Oscillator is to enable the tuning of the K parameter of the VCO, such that the average K value is locked to K_{ref} . The circuit architecture of the Dual-Controlled Ring Oscillator is shown in Fig.3.7. It consists of a Voltage-to-Current Converter (V-I Converter) at the front stage, and the output current of the V-I is fed to the Dual-Controlled Ring Oscillator.

As a first order approximation, the input voltage V_{in} can be related to I_1 by $I_1 = G_m * V_{in}$. The value of G_m can also be approximated as $1/R_s$. Therefore, we can relate V_{in} and I_1 in equation 3.7a below:

$$V_{in} = I_1 \times R_s \quad (3.7a)$$

The output current I_1 is then combined with I_{bias} before being fed to the Dual-Controlled Ring Oscillator. Since $M7 = M8$, the output current I_8 is equal to $I_1 + I_{bias}$. The value of I_{bias} is chosen to be 300uA.

In addition to analog voltage control V_{in} , the frequency of the ring oscillator can be tuned by adjusting the load capacitance C_L of the delay element. If V_{in} is kept constant, the frequency of the Ring Oscillator is minimum when $C_L = C_{max}$, and the frequency is maximum when $C_L = C_{min}$. In this design, each output node is connected to 16 MSB MOS capacitors (5-bit wide) and 32 LSB MOS capacitors (6-bit wide). The dimension for the Most Significant Bit (MSB) MOS capacitor is $(W/L)_{MSB} = 8u/1u$, while the dimension for the Least Significant Bit (LSB) MOS capacitor is $(W/L)_{LSB} = 1u/0.2u$. The equivalent capacitance value for the MSB MOS capacitor is about 27fF and the equivalent capacitance value for the LSB MOS capacitor is about 1.5fF.

To derive the parameter K, we can start from the VCO frequency equation. Equation 3.7b shows the fundamental equation that relate current and capacitor:

$$I = C \frac{\Delta V}{\Delta T} \quad (3.7b)$$

For an N-stage Ring Oscillator, the oscillation frequency can then be expressed as equation 3.7c:

$$f = \frac{1}{N(t_{rise} + t_{fall})} = \frac{I}{N \times C_L \times V_{DD}} \quad (3.7c)$$

Where N = number of stages of ring oscillator, C_L = loading capacitor of each stage of ring oscillator, and V_{DD} = supply voltage of ring oscillator, which is 1.8V in this design. From equation 3.7a, we can now relate frequency of ring oscillator, f to the analog input voltage V_{in} as shown in equation 3.7d:

$$f = \frac{V_{in}}{N \times C_L \times V_{DD} \times R_s} \quad (3.7d)$$

By rewriting the period for the ring oscillator, $T = 1/f$, equation 3.7d can be rewritten as equation 3.7e:

$$T = \frac{N \times C_L \times V_{DD} \times R_s}{V_{in}} = \frac{K}{V_{in}} \quad (3.7e)$$

Therefore, we can relate equation 3.7e to equation 3.2 shown in previous section. The parameter K can be approximated as $K = N \times C_L \times V_{DD} \times R_S$.

As discussed in the previous section, the nonlinearity of VCO based ADC can be attributed to the variation of K value across the whole input range V_{in} . This can be understood from the assumptions made during the derivation of equation 3.7e.

1. The V-I converter equation, $V_{in} = I \times R_S$ is generally valid only for a small input range.
2. The ring oscillator frequency equation of 3.7c is only a first order approximation of the charging and discharging of the load capacitor. The frequency is linearly proportional to the current I only for a small range.

Therefore, the K parameter is generally not a constant value. The function of the Dual-Controlled Ring Oscillator is to enable the tuning of K value by changing the value of the load capacitor C_L in addition to the analog input voltage V_{in} .

The value of K_{ref} is chosen to be $1.6e^{-10}$. Ideally, the K_{ref} value is the K value at typical corner when C_L is in the middle range, and V_{in} at mid input range, as shown in Fig.3.5 previously. Since the K value is given by $K = N \times C_L \times V_{DD} \times R_S$, we can approximately calculate the ideal K_{ref} value to be $K = 16 \times 216fF \times 1.8V \times 200 \text{ ohms} = 1.2e^{-9} \text{ VS}$. Since there is a constant $I_{bias}=300uA$ added at the V-I converter to speed up the Ring Oscillator, and the K parameter derivation is only accurate to the first order approximation, therefore the K value is slightly deviate from the ideal equation derived in 3.7e.

The system must be ensured locked across PVT (Process, Voltage and Temperature) variation. Let's denote K_A as the K value at minimum V_{in} and maximum C_L , and K_B as the K value at maximum V_{in} and minimum C_L . The inequality to be fulfilled is $K_A < K_{ref} < K_B$. This can be illustrated in graphical form

as shown in Fig. 3.8. Once the inequality is obeyed, the system is ensured to be locked under any temperature and process variation, as the load capacitance can be adjusted to compensate for the deviation from the ideal K value, K_{ref} . The tuning of the load capacitance is achieved by a digital control algorithm, which will be explained in the next section.

Table 3.1 parameters for the devices used in the Dual-Controlled Ring Oscillator in Fig.3.7

Device	Value
M1	10u / 2u
M2, M3	8u / 2u
M4, M5	8u / 2u
M6, M6a, M6b, M6c, M6x	8u / 2u
M7, M8	4u / 2u
Mp	2u / 200n
Mn	1u / 200n
Rs	200 ohms
Ibias	300uA

Figure 3.7 (a) Dual-Controlled Ring Oscillator Circuit Topology (b) Digital Controlled Array of Dual-Controlled Ring Oscillator circuit

Figure 3.8 Graph depicting K variation and condition of locking

3.2 K-Comparator Circuit

The function of the K-Comparator circuit is to compare average K value with reference K_{ref} . The output of the K-comparator is equal to '0' if average K value is less than K_{ref} , otherwise it will output a '1'. The output of the K-comparator is then fed to Digital Controller inside the K-locked-loop circuit.

Fig.3.9 shows one possible circuit implementation of the K-comparator circuit. Other possible implementation with more digital circuit implementation will be one of the future research directions of this work. The current circuit implementation consists of an analog integrator with a time constant of gm/C , a DAC with y -bit resolution, a sampling switch, and a voltage comparator.

To understand the circuit operation of this K-comparator circuit, recall from section 3.1 on the Dual-Controlled Ring Oscillator circuit. Let's denote t_i as the time instant the rising edge of the time pulse of ring oscillator appear at the last stage of the ring oscillator. Assuming that V_{in} is a sampled data and held constant throughout the sample window. At each t_i instant, the voltage comparator positive input voltage is given by:

$$\frac{g_m}{C} \int_0^{t_i} V_{in} dt = \frac{g_m}{C} V_{in} t_i = \frac{g_m}{C} V_{in} \sum_{w=1}^i \Delta t_w = \frac{g_m}{C} N \sum_{w=1}^i K_w \quad (3.8)$$

While the voltage comparator negative input voltage is:

$$i \times \frac{V_{ref}}{2^y - 1} \quad (3.9)$$

In this design, y represents the DAC resolution. By setting the value of g_m/C to be

$$\frac{g_m}{C} = \frac{V_{ref}}{2^y - 1} \frac{1}{K_{ref}} \frac{1}{N} \quad (3.10)$$

The K-comparator then effectively compares at each t_i instant the average value of K with K_{ref} .

Figure 3.9 K-Comparator Circuit

3.3 Digital Controller

Digital controller is the last building block of K-locked-loop. From previous section, it has been shown that Dual-controlled Ring Oscillator can be adopted to tune the K value of the Ring Oscillator, while the K-Comparator will compare the average K value of the Dual-Controlled Ring Oscillator at each t_i instant. To complete the function of the K-locked-loop, an algorithm is needed to adjust the K value at each t_i instant. Furthermore, the average K value must be tuned to as close as possible to K_{ref} at the t_i instant before the sampling clock arrives. The function of the digital controller is to implement the above mentioned K-locking algorithm. The allowed error between average K value and K_{ref} will be discussed in the next section.

Figure 3.10 An example to illustrate the working principle of Digital Controller of K-locked-loop

To illustrate the working principle of K-locking algorithm, consider the example shown in Fig.3.10. The initial K-value of the system might deviate from the reference K value. In order to bring the K value closer to the reference value, the number of load capacitance changes between two consecutive sign change at the output of the K-comparator is stored. The digital controller then changes the load capacitance to half the stored value in the opposite direction, bringing the average K value closer to K_{ref} .

In the example shown in Fig. 3.10, the initial K value is below K_{ref} , the digital controller then increase the load capacitance by turning on a MSB switch at each t_i instance. In this example, $6\Delta C_{MSB}$ has been added to the output load, and hence an increment of $6\Delta K_{MSB}$ before the K-comparator changes its sign. The system then change the load capacitance to half of its previous incremental value, which is $3\Delta C_{MSB}$ (equivalent to $3\Delta K_{MSB}$). The first phase MSB tuning is then completed and

the second phase LSB tuning starts with the same algorithm as first phase but with smaller incremental step.

During the second phase tuning, one step increment in the load capacitance ΔC_{LSB} is equivalent to ΔK_{LSB} increment in K value. In the steady state, the K value will toggle near K_{ref} . Recall from equation 3.6a on the definition of average K value, it can be easily seen that as t_i increase, the average K value is brought closer to K_{ref} .

The algorithm is best summarized by the the flow chart in Fig. 3.11.

Figure 3.11 Algorithm of K-locked-loop

3.4 Nonidealities of K-locked-loop

3.4.1 Nonideal average K value derivation

In the previous analysis, some assumptions have been made and the equations are oversimplified. The average K value derived in (3.6) assumes decision making time for K-comparator, the computational time for digital controller, and the switching time of the digitally controlled varactor cells in the dual-controlled ring oscillator all to be equal to zero, an unrealistic assumptions.

If the effect of the above mentioned delay time is taken into consideration, the average K value will be different as the K value is updated only after a certain time delay. Let's define $t_x = (\text{decision making time for K-comparator}) + (\text{the computational time for digital controller}) + (\text{the switching time of the digitally controlled varactor cells in the dual-controlled ring oscillator})$. Fig.3.12 shows the deviation of t_i from the ideal value, which ultimately change the average K value at each t_i instant. Let's denote $K_{\text{avg},i}$ as the average K value at each t_i instant. Let's define $t_{di} = (t_i - t_{i-1})/N$ ($N = \text{no of delay element in the dual-controlled ring oscillator}$, which is 16 in this design). We further define $\Delta t_i = t_i - t_{i-1}$, we can then derive the average K value at each t_i instant by taking those nonidealities into consideration:

$$K_{\text{avg},1} = \frac{V_{\text{in}}}{N} \Delta t_1 = V_{\text{in}} t_{d1} \quad (3.11)$$

Taking the effect of t_x into consideration, the value of $K_{\text{avg},2}$ become:

$$\begin{aligned}
K_{\text{avg},2} &= \frac{1}{2} \frac{V_{\text{in}}}{N} \left(\Delta t_1 + t_x + \left(N - \frac{t_x}{t_{\text{d1}}} \right) t_{\text{d2}} \right) \\
&= \frac{1}{2} \frac{V_{\text{in}}}{N} \left((\Delta t_1 + N t_{\text{d2}}) + t_x - \frac{t_x}{t_{\text{d1}}} t_{\text{d2}} \right)
\end{aligned} \tag{3.12}$$

If we substitute the equation of $K_i = V_{\text{in}} t_{\text{di}}$, $K_{\text{avg},2}$ can be expressed as :

$$K_{\text{avg},2} = \frac{1}{2} \left(K_1 + K_2 + \frac{V_{\text{in}}}{N} t_x \left(1 - \frac{t_{\text{d2}}}{t_{\text{d1}}} \right) \right) \tag{3.13}$$

By carrying the similar analysis, the value of $K_{\text{avg},3}$ can then be obtained as:

$$\begin{aligned}
K_{\text{avg},3} &= \frac{1}{3} \frac{V_{\text{in}}}{N} \left(\Delta t_1 + t_x + \left(N - \frac{t_x}{t_{\text{d1}}} \right) t_{\text{d2}} + t_x + \left(N - \frac{t_x}{t_{\text{d2}}} \right) t_{\text{d3}} \right) \\
&= \frac{1}{3} \left(K_1 + K_2 + K_3 + \frac{V_{\text{in}}}{N} t_x \left(2 - \frac{t_{\text{d2}}}{t_{\text{d1}}} - \frac{t_{\text{d3}}}{t_{\text{d2}}} \right) \right)
\end{aligned} \tag{3.14}$$

By induction, the general term for $K_{\text{avg},n}$ at the n-th instant can be obtained:

$$\begin{aligned}
K_{\text{avg},n} &= \frac{1}{n} \sum_{i=1}^n K_i + \frac{V_{\text{in}}}{nN} t_x \left(n - 1 - \sum_{i=2}^n \frac{t_{\text{d},i}}{t_{\text{d},i-1}} \right) \\
&= K_{\text{avg},n} = \frac{1}{n} \sum_{i=1}^n K_i + \frac{V_{\text{in}}}{nN} t_x \left(n - 1 - \sum_{i=2}^n \frac{K_i}{K_{i-1}} \right)
\end{aligned} \tag{3.15}$$

If $t_x = 0$, equation (3.15) is reduced to the ideal equation derived from (3.6).

As long as the effective K value as shown in (3.15) is locked to K_{ref} , with $|K_{\text{avg},n} - K_{\text{ref}}| < \sigma K$, where the value of σK is the largest allowable deviation of K_{avg} from K_{ref} , the

system will remain K-locked, and linearity of time-mode ADC is assured. The value of σK is discussed next.

3.4.2 Deviation of effective K value from K_{ref} in the steady state

To achieve x -bit resolution, the frequency difference between the ideal and practical VCO should be smaller than 1 LSB. Mathematically, it can be expressed as:

$$f_k' - f_k < \frac{f_{max} - f_{min}}{2^x} \quad (3.16)$$

where f_k' is the frequency of a practical VCO while f_k is the frequency of an ideal VCO, f_{max} is the maximum frequency, f_{min} is the minimum frequency and x = number of bit of the ADC. The concept can be extended easily to K-locked-loop. Expressing the equation in terms of time delay of delay elements, we can obtain:

$$\frac{1}{t_k'} - \frac{1}{t_k} < \frac{\frac{1}{t_{d\_min}} - \frac{1}{t_{d\_max}}}{2^x} \quad (3.17)$$

By expressing the equation in terms of K, (3.17) becomes:

$$\frac{V_{in}}{K_{eff, i}} - \frac{V_{in}}{K_{ref}} < \frac{V_{in\_max} - V_{in\_min}}{K_{ref} 2^x} \quad (3.18)$$

If we define the input voltage range $V_{in\_range} = V_{in\_max} - V_{in\_min}$, (3.18) can be simplified to

$$\left(\frac{\sigma K}{K_{\text{ref}} - \sigma K} \right) < \frac{V_{\text{in\_range}}}{V_{\text{in}} 2^x} \quad (3.19)$$

Since $K_{\text{ref}} \gg \sigma K$, we can arrive at the final equation for σK

$$\sigma K < \frac{V_{\text{in\_range}}}{V_{\text{in}} 2^x} K_{\text{ref}} \quad (3.20)$$

Even under the steady state, the value of effective K will deviate from K_{ref} by a small amount. In order to ensure the time-mode ADC achieves the desired resolution, (3.20) must be fulfilled. The K -comparator must be able to resolve the value of σK . In other words, the smallest resolvable K value in K -comparator must be smaller than σK to ensure the desired resolution of the time-mode ADC can be achieved.

3.4.3 Jitter in the reference clock

For an x -bit time-mode ADC with sampling clock period of T_s , the jitter (σ_{T_s}) should be less than half LSB so that the DNL is less than one LSB. Mathematically, it can be expressed as:

$$\sigma_{T_s} < \frac{1}{2} \frac{T_s}{2^x} \quad (3.21)$$

In this design, the jitter requirement = $\frac{1}{2} (3.072e^{-7} / 2^{10}) \approx 1.5e^{-10}$ s, which can be met quite easily in today's technology.

The number of time of K comparison is input dependant, the larger the input, the smaller the delay time, and thus the more time the K is compared and averaged.

3.5 SIMULINK Modeling

SIMULINK has gained popularity among system designer as a commercial modeling tool. In this design, the K-locked-loop is modeled in SIMULINK environment as a proof of concept. There are 5 main blocks in K-locked-loop based time-mode ADC, namely dual-controlled ring oscillator, digital controller, K-comparator, time to digital converter and clock generator. Each of these components and its SIMULINK models are shown in Fig. 3.12, except for the Clock generator, which is shown separately in Fig. 3.13. Each of these SIMULINK models will be described further below.

Figure 3.12 SIMULINK model of K-locked-loop

3.5.1 SIMULINK model for Dual-Controlled Ring Oscillator

Remember from Fig.3.1 that K is a nonlinear function of V_{in} and load capacitance. To model the dependency of K vary in a function of input voltage, the dual controlled ring oscillator circuit needs to be characterized first in Cadence environment. The simulation data is then curve fitted to obtain the nonlinear equation between K and V_{in} . In this design, $K = (8.8e^{-11}) V_{in} + 6.3e^{-11}$. The equation holds when the load capacitance is set at midpoint value, and is modeled by *fcn1* function in the SIMULINK model.

Similarly, to obtain the relationship between K value and the load capacitance, the dual controlled ring oscillator circuit was simulated in Cadence environment to obtain a relationship between K_{LSB} and the digital control code. To improve the modeling accuracy, the variation of K_{LSB} as a function of input voltage

is also taken into consideration. The relationship between K_{LSB} and V_{in} can be described by the equation $K_{LSB} = 9e^{-13} + (5.6e^{-13})V_{in}$. The equation is embedded in the digital controller model.

A subtractor is then used to combine the K value as a function of input voltage and digital control code. The K value is finally inputted into *fcn2* function in the SIMULINK model. Equation $t_d = K/V_{in}$ is embedded in the function in the SIMULINK model, *fcn2*. The t_d signal is then used to control the propagation delay of ‘variable time delay’ block, which is used to model a delay element. The delay element will be described further in the SIMULINK model of the Time-to-Digital Converter section.

Figure 3.13 SIMULINK model of K-locked-loop clock generator and timing diagram

3.5.2 SIMULINK model for clock generator

The start signal PA and sampling clock signal PB are generated from a clock generator. The SIMULINK model of the clock generator is shown in Fig. 3.13. At the rising edge of signal PA, the system will reset the counter, enable the ring

oscillator and reset the DAC. At the rising edge of the sampling clock PB, the system will latch the output of the counter and reset the analog integrator. The process will repeat itself for all the subsequent clock cycles.

3.5.3 SIMULINK model for Digital Controller

The algorithm of the digital controller was described in the state chart in Fig. 3.11 in previous section. The algorithm is modeled using stateflow®, a SIMULINK tool box. The digital controller is clocked by t_i signal generated from the Time-to-Digital Converter (In2). Other inputs to the digital controller include PA signal from clock generator (In1), V_{in} (In4) and K-comparator output (In3). Note that while stateflow® and SIMULINK models are used in this behavioral modeling, the digital controller can be described using HDL languages as well, giving the flexibility to the designer to choose different modeling technique.

3.5.4 SIMULINK model for Time-to-Digital Converter

The time-to-digital converter operates by first resetting the counter and initiates the pulse to propagate around the ring oscillator at the rising edge of the signal PA (from clock generator). The number of edges appears at the ‘variable time delay’ block is counted by a dual-edge triggered counter. It might appear that a ring oscillator with 16 delay units needs to be modeled by 16 ‘variable time delay’ blocks. However, the behavioral model for the ring oscillator can be simplified by one delay unit, and the counter value is used directly as the digital output. This behavioral equivalent model can save the simulation time by having fewer components in eliminating the behavioral model for the latch and the encoder block.

To model the instant of time when the pulse appears at the end of ring oscillator circuit which consists of $N=16$ delay units, a 'mod' function is used. $M = \text{mod}(\text{counter output}, 16)$. The instant of time when $M = 0$ is t_i . The t_i signal is used as the sampling signal to sample the integrator and the DAC within the K-comparator, as shown previously in Fig. 3.9. The digital output, which is the counter value, is sampled at the rising edge of the signal PB from clock generator at sampling rate of T_s .

3.5.5. SIMULINK model for K-comparator

K-comparator consists of a triggered DAC, a sampled integrator and a voltage comparator. The t_i signal generated from the TDC is used to sample the output of the integrator and the DAC, and those signals are fed to a voltage comparator, which is modeled using an embedded Matlab function *fcn0* in Fig.3.12. If $u_1 > u_2$, the output y of the comparator will be a '1', else it will output a '0'. In this model, the latency of the K-comparator is modeled using a fixed transportation delay block.

The analog integrator and DAC are reset at the rising edge of signal PB and PA signals from clock generator respectively. The DC gain of the integrator is set according to equation (3.10), where $K_{\text{ref}} = 1.6e^{-10}$ vs in this design, yielding $g_m/C = 5.536e^6 \text{ s}^{-1}$. For the DAC, the self-incremental counter will increase its value at every rising edge of t_i , the DAC gain is thus set to be $V_{\text{ref}} / (2^y - 1)$, where y is the number of bits of the DAC, which is 7-bit in this design. V_{ref} is chosen to be 1.8V. The summary of all the design parameters is given in table 3.1.

Table 3.2 Summary of design parameters in the design of K-locked-loop based time-mode ADC

Parameter @V _{DD} = 1.8V	value
ADC resolution	10-bit
Speed	2MS/s
Input range	0.6V–1.2V (600mV)
Digitally controlled varactor resolution	10-bit
DAC resolution (K-comparator)	7-bit
K _{ref} (refer to Fig. 3.8)	1.6 e ⁻¹⁰ Vs
K _{A,Max} (refer to Fig. 3.8)	2.324 e ⁻¹⁰ Vs
K _{B,Min} (refer to Fig. 3.8)	1.061 e ⁻⁹ Vs

3.5.6 SIMULINK Simulation Result

Code density test is used to test the integral nonlinearity (INL) and differential nonlinearity (DNL) of this time-mode ADC, with an average of 8 codes per level. The DNL plot and INL plot are shown in Fig.3. 14. As can be seen from the figures, the DNL is bound to ± 0.125 LSB, while the INL is found to be within ± 0.1875 LSB. This confirms the monotonic behavior of the K-locked-loop based time-mode ADC, which is linear up to 10-bits without any missing codes.

To summarize, the concept of K-locked-loop has been proven to be a feasible idea through simulation result. The mostly digital nature of K-locked-loop is attractive in modern CMOS technology as it scales well with technology. Future research work should therefore focus on digital implementation of K-comparator, thereby achieving all-digital-K-locked-loop.

Figure 3.14 DNL and INL result of K-locked-loop SIMULINK simulation result

Chapter 4 All Digital Multiphase Multiplying Delay-Locked Loop and its application in Time Mode ADC

Besides VCO-based ADC, integrating ADC is another form of Time Mode ADC that has been around for many years, before the topology of VCO-based ADC emerged. The operation of integrating ADC can be easily understood from Fig.4.1. The analog input voltage is fed into the analog RC integrator, the output voltage of the Op-Amp, which is a ramp signal, is then fed into an analog comparator. Once ramp signal cross the comparator reference voltage (V_{ref}), the output of the comparator will go high, which reset the counting cycle. The counter output represents the digital output of integrating ADC.

Traditional analog Delay Locked Loop has been adopted to improve the resolution of integrating ADC. However, charge pump and Voltage Controlled Delay Line are required in traditional analog Delay Locked Loop. These analog circuitries are getting more difficult to design in modern CMOS technology. With continuing scaling in CMOS technology and the trend to digitize analog circuitry continue, there is a trend to digitize the analog Delay Locked Loop. In recent years, All-Digital Delay Locked Loop has gained popularity. In this thesis, a new topology of All Digital Multiphase Multiplying Delay-Locked Loop (ADMMDLL) has been proposed; the ADMMDLL is well suited for integrating ADC application due to its all digital nature, and scale well with modern CMOS technology.

(a)

(b)

Figure.4.1 (a) Integrating ADC circuit topology (b) Timing diagram of an integrating ADC

Section 4.1 will give a brief introduction to Delay Locked Loop operation. Section 4.2 then reveal the architecture of the proposed ADMMDLL. Section 4.3 will discuss the layout, chip photo and measurement result. Lastly, a summary will be drawn at section 4.3.

4.1 Delay Locked Loop

The general architecture of a Delay Locked Loop (DLL) can be well described by Fig.4.2. Very similar to a conventional Phase Locked Loop (PLL), it consists of Phase detector circuit, a charge pump, and a loop filter. However, the main difference is that a DLL consists of a delay line, rather than an oscillator in a typical PLL. The advantage of DLLs over PLL is delay line is generally less sensitive to noise than oscillator as corrupted zero crossings of waveform disappear at the end of the delay line, while it is re-circulated in an oscillator.

Besides no jitter accumulation, DLL is mostly a single-pole system, thus its stability and settling issues are more relaxed compared to PLL. It does not rely on a high loop bandwidth for jitter correction. However, one main drawback of DLL is unable to provide programmable clock multiplication ratio.

Figure.4.2 Delay Locked Loop (DLL) circuit architecture.

The multiplying Delay Locked Loop (MDLL) architecture, as shown in Fig.4.3(a) can provide programmable clock multiplication, without the jitter accumulation problem faced by PLL. The MDLL can perform the clock multiplication by having a multiplexer in front of the delay line. The multiplexer can select the clock signal from either reference clock or last stage of delay line. When the multiplexer connected to the last stage of delay line, it forms a ring oscillator. After a certain number of circulation (controlled by the divider circuit output), the multiplexer input will be connected to the jitter-free reference clock, and the recycling begins again.

The timing diagram shown in Fig.4.3(b) illustrate an example of frequency multiplication by 4. Once the sel signal goes high (controlled by divider output, which is a divide-by-4 circuit in this example), the multiplexer will select the reference clock into delay line. When the sel signal is low, the delay line is configured in a feedback loop, functioning as a ring oscillator. This MDLL configuration effectively performs the clock multiplication function, without the jitter accumulation problem of a typical PLL.

The focus of this chapter is to introduce the proposed novel All Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL) for Time Mode ADC application. The all digital nature of the proposed architecture makes it attractive in modern CMOS technology. Most of the blocks can be synthesized using the standard digital flow, making the design cycle faster and easier portability to other process nodes. The circuit topology and building blocks of proposed ADMMDLL is explained next.

Figure 4.3(a) Multiplying Delay Locked Loop (MDLL) circuit architecture.
 (b) Timing diagram of MDLL for a multiplication factor of 4

4.2 All Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL)

The main motivation for the ADMMDLL is for Time Mode ADC application, more specifically, the integrating ADC. As the trend to digitize analog circuitry continues due to better scalability in modern CMOS technology, as well as automation in standard digital design, more analog circuitries has been replaced by digital counterpart. To the best of the author knowledge, there is no corresponding digital counterpart for the Multiplying Delay Locked Loop (MDLL) shown in Fig. 4.3. A novel ADMMDLL architecture is thus proposed, and the architecture is well suited for integrating ADC to improve the clock resolution.

The main architecture of ADMMDLL is shown in Fig.4.4. It consists of Digitally Controlled Delay Line, a phase detector, a SAR state machine, a multiplexer, a select logic and a Divider circuit. When the select logic is low, the Multiplexer will select signal from the last stage of Digitally Controlled Delay Line, and thus the Digitally Controlled Delay Line is configured as an oscillator. After $M-1$ cycle (where M is the divider ratio), the select logic will goes high, in which the multiplexer will select signal from clean reference. Effectively, this has performed the function of clock multiplication by a factor of M .

Figure.4.4 All Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL) architecture

Similar to conventional analog Delay Locked Loop, a circuitry to detect the phase difference between reference and feedback clock is always required, and the lead / lag information is then used as a indicator to adjust the delay time of delay line such that the reference clock and feedback clock remain locked. Therefore a phase detector block is required in ADMMDLL as well. However, unlike conventional Delay Locked Loop, there is no charge pump circuit; instead, the digital block that perform SAR algorithm engine is in place to perform the delay adjustment according to the lead / lag information from phase detector. The functionality of each block will be explained in detail in following sections.

4.2.1 Digitally Controlled Delay Line

The Digitally Controlled Delay Line consists of a multiplexer and three differential delay elements. To ensure matched delay among all the delay stage, the multiplexer and the delay elements are actually built from the same circuitry, with only minor changes in the input connection. To illustrate, Fig.4.5 shows the simplified schematic of the multiplexer circuit.

Figure.4.5 Simplified Multiplexer Circuit inside Digitally Controlled Delay

When the Sel signal is '1', the first input stage (In1+ and In1-) is enabled, while the second input stage (In2+ and In2-) is disconnected. On the other hand, when the Sel signal is '0', the second input stage is connected while first input stage is disabled. To ensure equal matching, the other three delay elements are actually same as the multiplexer circuit shown in Fig.4.5. The only difference is the Sel signal

is always tied to '1', implying the second input stage is permanently disabled, and just functions as a dummy block to equalize delay as the first multiplexer stage.

The differential circuit configuration of the multiplexer and delay elements also implies better noise immunity, as the common mode noise, e.g. supply and ground noise will be rejected. The delay time is also half of the single ended counterpart, implying higher time resolution. A positive latch is added at the output to enable faster transition time.

While Fig.4.5 shows the simplified architecture of the multiplexer and delay element, it does not reveal how the delay can be tuned digitally. The function of the Digitally Controlled Delay Line is to tune the delay according to digital code, such that the reference clock and feedback clock remain locked. Fig.4.6 shows the complete schematic of the multiplexer delay element circuit that was adopted in this design to enable digital programmability.

Figure.4.6 Detailed multiplexer circuit made of array of 16 inverting stages

As can be seen from Fig.4.6, there are a total of 16 inverting stages connected to the output nodes Out+ and Out-. By digitally control the number of inverting stages connected to the output nodes, the delay time can be altered. The delay time is inversely proportional to the number of connected stages, e.g. smallest delay when all the inverting stages are connected together.

To ensure delay time decreases monotonically with number of delay stages turned on (connected to output nodes), the transistors sizing has been chosen based on simulation results. The transistor parameters of multiplexer circuits shown in Fig.4.6 is summarized in Table 4.1. The stage one ($n=1$) has the largest transistor size, and the sizing is smallest at last stage ($n=16$).

Table 4.1 Summary of the design parameters in the multiplexer circuit making use of an array of 16 inverting stages

	n = 1	n = 2	n = 3	n = 4	n = 5	n = 6	n = 7	n = 8
M1, M1a, M1b, M1c	36u / 120n	18u / 120n	12u / 120n	6u / 120n	4.8u / 120n	4.2u / 120n	3.6u / 120n	3u / 120n
M2, M2a, M2b, M2c	6u / 120n	6u / 120n	6u / 120n	6u / 120n	6u / 120n	6u / 120n	6u / 120n	6u / 120n
M3, M3a, M3b, M3c	2u / 120n	2u / 120n	2u / 120n	2u / 120n	2u / 120n	2u / 120n	2u / 120n	2u / 120n
M4, M4a, M4b, M4c	12u / 120n	6u / 120n	4u / 120n	2u / 120n	1.6u / 120n	1.4u / 120n	1.2u / 120n	1u / 120n

	n = 9	n = 10	n = 11	n = 12	n = 13	n = 14	n = 15	n = 16
M1, M1a, M1b, M1c	3.6u / 120n	2.4u / 120n	1.8u / 120n	1.8u / 120n	2.4u / 120n	1.8u / 120n	1.5u / 120n	1.5u / 120n
M2, M2a, M2b, M2c	3u / 120n	3u / 120n	3u / 120n	3u / 120n	1.5u / 120n	1.5u / 120n	1.5u / 120n	1.5u / 120n
M3, M3a, M3b, M3c	1u / 120n	1u / 120n	1u / 120n	1u / 120n	0.5u / 120n	0.5u / 120n	0.5u / 120n	0.5u / 120n
M4, M4a, M4b, M4c	1.2u / 120n	0.8u / 120n	0.6u / 120n	0.6u / 120n	0.8u / 120n	0.6u / 120n	0.5u / 120n	0.5u / 120n

4.2.2 Select Logic

The function of the select logic block is to control the multiplexer input clock signal. When the Sel signal is ‘1’, the multiplexer input will select Reference clock. On the other hand, the feedback clock will be selected when the Sel signal is ‘0’. The timing of the select logic is critical as it will affect the jitter performance, since the clock edge might experience distortion if the logic does not completely switch before the next clock edge arrives. Therefore, the select logic has to be implemented using dynamic CMOS logic topology.

Figure 4.7(a) select logic circuit (b) select logic timing diagram

Fig.4.7(a) shows the select logic circuit, and the corresponding timing diagram is shown in Fig. 4.7(b). As can be seen from the timing diagram, the Sel signal is asserted immediately after the falling edge of the feedback clock and

deasserted immediately after the rising transition of the reference clock. The Sel signal is deasserted when both the reference clock and feedback clock go high.

4.2.3. Phase Detector

The main function of the phase detector is to detect whether the reference clock is leading or lagging the feedback clock, and thus sending the lead / lag signal to the SAR algorithm engine. The inputs to the phase detectors are the reference clock and feedback clock. The circuit topology of phase detector circuit is shown in Fig.4.8.

Figure 4.8 Phase Detector schematic

If the In1 (feedback clock) signal is leading In2 (reference clock) signal, the output (Q) is equal to '1', otherwise, it will output a '0'. The output of the phase

detector is sent to SAR algorithm engine to decide on the delay adjustment. The SAR algorithm is discussed next.

Table 4.2 shows the transistor sizing of the phase detector circuit

Table 4.2 Summary of the design parameters of the phase detector circuit

Device	Value
M1, M2	6u / 120n
M3	2u / 120n
M4	4u / 120n
M5, M8	8u / 120n
M6, M7, M9, M10	3u / 120n
INV (PMOS)	6u / 120n
INV (NMOS)	2u / 120n

4.2.4. SAR state machine

The SAR state machine implements the Binary search algorithm, as shown in Fig.4.9. The number inside each circle represents the number of enabled delay stages, as explained in section 4.2.1. If the Phase detector output is 0, which represent the feedback clock is lagging the reference clock, the delay time of delay line will be shortened, and this can be done by enabling more delay stages. Similarly, if the phase detector output is 1, which represent the feedback clock is leading the reference clock; the delay time will be lengthened. This can be achieved by reducing the number of delay stages.

Since there is a total of 16 delay stages inside each delay element, the Binary Search algorithm will start at midpoint, which is 8 in this design. If the phase

detector output is 0, the next state is 12; if the phase detector output is 1, the next state is 4. And the binary search will continue. After the 3 cycles of binary search, the sequential search will take places. For example, if after 3 cycles of binary search, and the state is 15, the next state will be 14 if phase detector output is 1, otherwise it will enters state 16.

Figure 4.9 Binary Search algorithm

The whole SAR state machine can be synthesized using the conventional digital flow, from HDL code entry, to logic synthesis, and physical synthesis. This will fasten the whole design cycle, and easier portability to other CMOS process. Since some of the customized blocks like Digitally Controlled Delay line, and select logic still follow through analog flow, the whole ADMMDLL actually goes through the whole mixed signal flow, as shown in Fig.4.10

Figure 4.10 Mixed Signal flow adopted in ADMMDLL design

4.2.5. Divider Circuit

The divider circuit is a standard divide-by-4 logic, and thus can be synthesized using the same digital flow as SAR state machine. The divide-by-4 logic also can be changed to modulus divider in the future project for programmable dividing ratio, and thus programmable clock multiplication factor. Since the clock multiplication factor is equal to the divider ratio.

4.3 ADMMDLL layout and measurement result

The ADMMDLL is implemented in IBM 0.13 μ m CMOS process. The chip micro-photograph is shown in Fig. 4.11. There are a total of 18 pads surrounding the active area, with two VDD supply pads, and two GND ground pads. One pad is reserved for input reference clock, and one for reset signal (Rst). There are a total of 12 pads connected to the 12 output buffers respectively. The output pads are named as out1 to out12. The corresponding output out1 to out12 correspond to the nodes in the schematic shown in Fig.4.12.

Figure.4.11 ADMMDLL Chip micro-photograph

Figure.4.12 ADMMDLL block schematic

A more detail breakdown of the chip area occupied by different blocks are shown in Fig.4.13. As can be seen from Fig.4.13, the whole active area is less than 220um by 210um, while more than 70% of the total area is occupied by the Digitally Controlled Delay Line, while the SAR state machine and other logic blocks only occupy less than 20% of the total area. The layout of the Digitally Controlled Delay Line and buffers are drawn manually, following the conventional analog flow, while the layout of the SAR state machine and other logic blocks are placed and routed using standard digital flow.

Figure.4.13 ADMMDLL chip area by blocks

Fig.4.14 shows the measured Reference clock and Output clock, with a clock multiplication factor of 4. The output clock frequency is 170MHz. The input reference clock of 42.5MHz is inputted at the Ref pad shown in Fig.4.11. The maximum frequency of the current ADMMDLL is 170MHz. Further research work on the new topology of Digitally Controlled Delay Line can further improve the speed of the ADMMDLL.

The measured peak-to-peak jitter is 21.74ps measured using an oscilloscope, under the supply voltage VDD of 1.5V. Fig. 4.14(a) shows the output waveforms

plotted at nodes out3 and out11. The pk-to-pk jitter histogram is shown in Fig.4.14

(b). The total power consumption of the whole chip is 4.6mW.

(a)

(b)

Figure .4.14 Measured reference and output clock, clock multiplication
factor of 4

Table 4.3 ADMMDLL Performance Summary and Comparison

	[64]	[65]	[66]	[67]	This Work
process	0.18um	0.35um	0.13um	55nm	0.13um
Category	All Digital Delay Locked Loop	All Digital Delay Locked Loop	All Digital Delay Locked Loop	All Digital Delay Locked Loop	All Digital Multiphase Multiplying Delay Locked Loop
Supply Voltage (V)	1.8	3.3	1.5	0.65	1.5
Active area (mm ²)	0.88	0.075	0.03	0.007	0.046
f _{max} (MHz)	700	260	2500	300	170
Lock Time(cycles)	32	10	24	2 ~ 6	4
pk-pk Jitter (ps)	17.6	24.2	14	9	21.74
Power @ f _{max} (mW)	23	9.9	30	0.16	4.6
Power in uW/MHz	32.86	39.6	12	0.53	27.06

The Figure-of-Merit (FoM) is defined in the unit of $\mu\text{W}/\text{MHz}$. The FoM of this ADMMDLL is $27\mu\text{W}/\text{MHz}$, and it is comparable to other state-of-the-art of “All Digital Delay-Locked Loop” as shown in table 4.3. Since this is the very first “All-Digital Multiphase Multiplying Delay-Locked Loop (ADMMDLL)” proposed, and its performance is on-par with other existing All Digital Delay-Locked Loop techniques from reference [64] to [67], thus this technique can be researched further to improve its speed performance.

One major drawback of this ADMMDLL is its speed limitation with f_{max} of only about 170MHz. The speed is limited by the architecture of the *Digitally*

Controlled Delay Line. As the *Digitally Controlled Delay Line* consists of 16 inverting stages connected in parallel, it will increase the load capacitor considerably. More innovative idea on the *Digitally Controlled Delay Line* architecture shall be explored to make the idea of ADMMDLL more attractive.

To conclude, the ADMMDLL is suitable for time mode ADC application due to its highly digital nature, and most of the circuit can be synthesized using standard digital flow, making it very easy to port to other process. Since most of the circuit consists of digital circuit, it scales well with CMOS technology node, occupy less area, and enjoying higher speed with more advanced CMOS node. However, future research work should focus on improving the architecture of *Digitally Controlled Delay Line* to enhance the speed of ADMMDLL, so that it can suit high speed application.

Chapter 5 Conclusion

This thesis introduced the concept of K-locked-loop and its application in Time Mode ADC. SIMULINK modeling, together with circuit level simulation has been used to prove the feasibility of K-locked-loop. To the best of the author knowledge, there is no similar concept been proposed before, which explore the concept of feedback in voltage-time domain. In contrast to a conventional feedback amplifier or Phase-locked-loop, whereby feedback is done in the voltage or time domain respectively, K-locked-loop explores the concept of feedback in voltage-time domain, with a physical unit of $V.S$.

The basics operating principle of the K-locked-loop concept has been explained in chapter 3. Start with the identification of the nonlinear relationship between VCO frequency and V_{in} , the equation has been rewritten as a function of K , which can be related to circuit parameter as shown in equation 3.7e. The K-locked-loop architecture, which consists of a *Dual Controlled Ring Oscillator*, a *K-comparator*, and a *Digital Controller* has been shown to be able to overcome the nonlinearity of VCO by using the idea of feedback in the voltage-time domain, namely the K-locked-loop Principle. Under steady state, the average K value is shown to be locked to K_{ref} , and a linear relationship between VCO frequency and V_{in} is thus established.

A detailed mathematical derivation on the main concept of K-locked-loop has been discussed in Chapter 3. The non-ideality effect and its impact to K-locked-loop has been discussed as well. Furthermore, a 10-bit, 2MS/s time mode ADC with K-locked-loop has been modeled and simulated using SIMULINK as a proof of concept.

There are two major limitations of the K-locked-loop topology and require further research work for performance improvement. The first limitation is due to the k-comparator circuit architecture. The current implementation rely on analog circuitry such as analog comparator and DAC for the K value comparison. Since analog circuit does not scale well with CMOS technology, future work on K-locked-loop shall focus on the all-digital implementation of K-comparator, which still built from analog circuit in the current thesis.

The second limitation lies on the *Dual Controlled Ring Oscillator* circuit topology. The speed of the current K-locked-loop based ADC is only 2MS/s, limited by the speed of the *Ring Oscillator*. Since current *Dual Controlled Ring Oscillator* rely on switching of the Capacitor Bank for tuning of the K value, this inevitably slow down the *Ring Oscillator*. Other topology of *Dual-controlled Ring Oscillator* should also be explored to further enhance the speed of the *Time Mode ADC*.

The second main contribution of this thesis is the introduction of the *All Digital Multiphase Multiplying Delay Locked Loop (ADMMDLL)* for integrating ADC application. The mostly digital nature of ADMMDLL is very attractive in modern CMOS technology, as most of the circuit can be synthesized using standard digital flow, which greatly speed up the whole design cycle and easier portability to other CMOS node. The chip only occupy an active area of 220 μ m by 210 μ m, and has peak-to-peak jitter of around 22ps.

Future work on ADMMDLL will focus on other implementation of the *Digitally Controlled Delay Line* to further increase the speed of the ADMMDLL. The divider circuit also can be made programmable to enable programmable clock multiplication ratio. Future work can also embbed ADMMDLL into the integrating ADC to improve the time resolution of integrating ADC.

To summarize, two novel circuit topologies, namely K-locked-loop and ADMMDLL has been introduced in this thesis. Since VCO-based ADC has gained popularity recently due to its highly digital implementation, the introduction of K-locked-loop provides another useful insight into the alternative way of implementation of the VCO-based ADC. Similarly, the ADMMDLL can be embedded inside the integrating ADC to further improve the resolution. As Time Mode ADC will be the next generation ADC, K-locked-loop and ADMMDLL should be researched further, owing to their highly digital implementation. The trend to continuously digitize analog circuitry will prevail, especially in the area of ADC circuit.

Author's Contribution

[1]H. Hon Cheong and L. Siek, "K-locked-loop and its application in time mode ADC," in *Integrated Circuits, ISIC '09. Proceedings of the 2009 12th International Symposium on*, 2009, pp. 101-104.

[2]H. Hon Cheong and L. Siek, "Review on VCO based ADC in modern deep submicron CMOS technology," in *Radio-Frequency Integration Technology (RFIT), 2012 IEEE International Symposium on*, 2012, pp. 86-88.

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