ZrO₂ as high-K gate dielectric for GaN-based transistors

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**ZRO₂ AS HIGH-K GATE DIELECTRIC FOR GAN-
BASED TRANSISTORS**

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School of Electrical & Electronic Engineering

2016

ZRO₂ AS HIGH-K GATE DIELECTRIC FOR GAN-BASED TRANSISTORS

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School of Electrical & Electronic Engineering

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

Date

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Abstract

GaN-based high electron mobility transistors (HEMTs) have shown their excellent performance in high power, high frequency and low noise applications. One of the critical issues that further limits the performance and reliability of GaN HEMTs is the high gate leakage current. The high gate leakage current will reduce the power added efficiency and breakdown voltage and increase the minimum noise figure ($NF_{\min}$) for GaN-based HEMTs. To mitigate above issues, GaN Metal-Insulator-Semiconductor HEMTs (MISHEMTs) using high- k materials as gate insulator and passivation layer are investigated.

Owing to its large band gap (~ 5.6 eV) and high dielectric constant (~ 25), ZrO_2 is a promising candidate to be utilized as the gate dielectric for GaN MISHEMTs. In order to effectively suppress gate leakage and passivate surface traps, understanding of band alignments and interfacial properties between ZrO_2 and GaN-based semiconductor substrates is important.

In this thesis, the studies on the band alignment between ZrO_2 and GaN were carried out. The effect of device processing on interfacial properties between ZrO_2 on (Al)GaN was investigated. The application of ALD- ZrO_2 as high- k gate dielectric for GaN-based HEMTs was also explored.

The major contributions of this thesis are summarized below:

(1) The band alignment between atomic layer deposited (ALD) ZrO_2 and GaN was experimentally evaluated by utilizing angle-resolved X-ray photoelectron spectroscopy (XPS) combined with numerical calculations by taking into account of GaN surface band bending and gradient potential in ZrO_2 layer. Valence band discontinuity ΔE_V of 1 eV and conduction band discontinuity ΔE_C of 1.2 eV at ZrO_2/GaN interface were determined.

(2) The interface states related to the interfacial sub-oxide layer between ALD- ZrO_2 and (Al)GaN were affected by various fabrication processing treatments. The effect of surface pre-treatment before ALD deposition and post-deposition annealing on interfacial chemical bonding states for ALD- ZrO_2 on (Al)GaN were analyzed by X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HR-TEM).

(3) AlGaN/GaN MISHEMTs on high-resistivity Si substrate using 10 nm thick ALD- ZrO_2 as gate dielectric were demonstrated. Due to the application of ALD- ZrO_2 , the reverse gate leakage current was effectively suppressed and forward gate input bias was extended to a high value. The interface trap state density was also evaluated by AC conductance and “Hi-Lo frequency” methods. Reduction of interface trap state density D_{it} value from $4 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ and $3 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ at energy of -0.29 eV to $7 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ and $1 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ at energy of -0.38 eV was observed by AC conductance method and “Hi-Lo” frequency method, respectively.

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Chapter 1

Introduction

1.1 GaN Compound Semiconductor Technology

In the past few years, III-nitride compound semiconductors and their alloys such as GaN, AlN, AlGaN and InAlN have attracted much attention due to several advantages over Silicon (Si) such as large band gap energy, high critical electric field and high saturation drift velocity. The fundamental properties of the III-nitride compound semiconductor materials are generally attributed to the smaller bond length between constituent atoms along with their wide band gap energy [1]. Smaller bond length will lead to strong bond energy between constituent atoms, which brings in high chemical stability. Furthermore, large bond energy and smaller atom mass will also cause large phonon energy, which makes lattice scattering even more difficult to occur. This will then result in high thermal conductivity and high electron saturation drift velocity for III-nitride compound semiconductor materials. In addition, due to large band gap energy, breakdown voltage will be high and the intrinsic carrier generation rate will also be low even at high temperature [2], and thus allows for device operation at high temperature without excessive leakage current. Overall, the above-mentioned characteristics make III-nitride compound semiconductors extremely suitable for high frequency [3], high power [4], high voltage [5] and high temperature applications [6].

Among III-nitride compound semiconductors, GaN is the most investigated. Thus, in this chapter, we will concentrate on the introduction of properties of GaN. The material properties of GaN compared to other semiconductors of interest are listed in Table 1.1 [7].

Table 1.1 Key material properties of GaN compared with other semiconductor materials of interest.

Material properties	Si	6H-SiC	4H-SiC	GaN	GaAs
$E_g(\text{eV})$	1.1	3.0	3.26	3.4	1.4
$E_c(\text{MV/cm})$	0.3	2.4	2.0	3.3	0.4
ϵ_r	11.8	9.7	10	9.0	12.8
$\mu_n(\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1})$	1350	370	720	900	8500
$v_{\text{sat}}(10^7 \text{ cm/s})$	1.0	2.0	2.0	2.5	2.0
$\kappa(\text{W} \cdot \text{cm}^{-1} \cdot \text{K}^{-1})$	1.5	4.5	4.5	1.3	0.5

E_g : band gap energy, E_c : breakdown electric field, ϵ_r : relative dielectric constant, μ_n : electron mobility, v_{sat} : saturated drift velocity of electron, κ : thermal conductivity.

As shown in Table 1.1, large band gap energy leads to high breakdown electric field. Compared with Si and GaAs, both GaN and SiC have almost ten times higher breakdown electric field. In addition, intrinsic carrier generation rate is generally low for wide band gap energy materials, making GaN and SiC

suitable for high voltage operations while keeping low current leakage [2].

Fig.1.1 shows the relation between electric field and electron drift velocity for Si, GaAs, 6H-SiC, 4H-SiC, GaN and AlGaN/GaN heterostructure [8]. AlGaN/GaN heterostructure, which is the key component for GaN high electron mobility transistors (HEMTs) to provide a large density of electrons and high electron mobility, will be introduced in Chapter 1.2. At low electric field, the carrier velocity shows linear relation with the applied electric field. The low field mobility is defined as the slope of carrier velocity versus the electric field. In general, the mobility defines the resistivity of the material and is an important parameter for high frequency operations. As indicated in Table 1.1 and Fig. 1.1, GaAs has a high mobility, which makes it rather successful in high frequency applications. However, after a certain value of electric field, the carrier velocity gradually reaches a maximum and the carrier velocity becomes independent of the electric field. It is generally desirable that a high carrier velocity can be maintained under a high electric field. This permits high voltage and RF current to be obtained at the same time, which can result in high RF power. As indicated in Fig.1.1, SiC and GaN show higher electron saturation velocity as compared to Si and GaAs. In addition, for AlGaN/GaN heterostructure, a even higher electron saturation velocity is found. On the other hand, as wide bandgap semiconductors, SiC and GaN can work under high electric field, which make them ideal candidates for high power and high frequency transistors.

Fig.1.1 Relation between electric field and electron drift velocity for GaAs, 6H-SiC, 4H-SiC, Si, GaN and AlGaIn/GaN heterostructure.

The figure of merit (FOM) is an index which combines some relevant material properties into a value to roughly estimate the relative strength of a certain material with respect to some specific device applications. Four typical FOMs of GaN compared with Si, 6H-SiC and GaAs are listed in Table 1.2 [7]. JM represents the product of frequency and power performance for high output power high frequency devices [9]. KM is a suitable index for the high temperature operation of devices [10]. BM expresses a low loss feature at low frequency [11]. While for BHM, it indicates a switching loss of a power FET at high frequency [12]. It is obvious that semiconductor materials with wide band gap energy (e.g. GaN and SiC) exhibit larger indices, which indicate that superior performance can be obtained when they are used for high power high

frequency devices.

Table 1.2 Four typical figures of merit (FOM) of GaN compared with other semiconductor materials of interest. All FOM values are normalized to Si.

FOM	Si	6H-SiC	4H-SiC	GaN	GaAs
JM	1	260	180	760	7.1
KM	1	4.68	4.61	1.6	0.45
BM	1	110	130	650	15.6
BHM	1	16.9	22.9	77.8	10.8

JM: Johnson's figure of merit= $(E_c \cdot v_{sat}/\pi)^2$, KM: Keyes's figure of merit= $\kappa(v_{sat}/\epsilon)^{1/2}$, BM: Baliga's figure of merit= $\epsilon \cdot \mu_n \cdot E_c^3$, BHM: Baliga's high frequency figure of merit= $\mu_n \cdot E_c^2$.

1.2 Characteristics of GaN HEMTs

The High Electron Mobility Transistors (HEMTs), which is also known as Heterostructure Field-Effect Transistors (HFETs), was first reported in 1980 [13]. The unique feature of HEMTs is their heterostructures. By growing a semiconductor material with wider band gap energy on top of another un-doped semiconductor material with narrower band gap energy, an electron potential is formed at the heterointerface due to the conduction band offset ΔE_c of the two materials. A two-dimensional electron gas (2DEG) channel is then generated with the confinement of the electrons in the potential well. For conventional III-

V based HEMTs, the modulation-doped barrier layer (semiconductor with wider band gap energy) is the main source to provide carriers for 2DEG channel. Owing to the potential barrier at the heterointerface, the electrons are separated from the ionized donors and highly confined in the 2DEG channel, which lead to the reduction of the scattering effect between the remaining ionized donors and the electrons. Thus, a high mobility and carrier density can be obtained from this feature, which facilitate the utilization of HEMTs for high power and high frequency applications [13].

In the early 1990s, promising progress in growing III-nitride epitaxial layers with high quality was achieved by utilizing metal organic chemical vapor deposition (MOCVD) method [14,15]. The AlGa_N/Ga_N heterojunction was first reported in 1991 [16]. Since the first demonstration of AlGa_N/Ga_N HEMTs in 1993 by Khan *et al.* [17], comprehensive investigations have been explored on Ga_N-based HEMTs in the last two decades. Ga_N-based HEMTs are now attracting great attention for amplifier operating at high power levels, high temperature and high frequency, which are ascribed to the excellent properties of AlGa_N/Ga_N heterostructures. A wide range of application areas have been explored for Ga_N-based HEMTs, including high frequency Monolithic Microwave Integrated Circuits (MMICs) [18], high power amplifiers for wireless base station [19], and high voltage electronic devices for power transmission lines [20], etc.

The fundamentals of Ga_N-based HEMTs are different to that of conventional

III-V based HEMTs like GaAs, GaN-based HEMTs have a distinct origin of 2DEG, namely spontaneous and piezoelectric polarization induced 2DEG [21]. Owing to the strong spontaneous and piezoelectric polarization effect, a conductive channel with a high-density of sheet carriers can be obtained even without intentional doping in the barrier layer (semiconductor material layer with wider band gap energy) for GaN-based HEMTs [22].

As mentioned above, GaN-based semiconductor materials have a unique property compared to conventional III-V semiconductors like GaAs—a rather strong polarization field inside the crystal, which is more than five times of that of GaAs [23]. Prominent influences on the electronic characteristics of GaN-based HEMTs will be introduced by the polarization field. The polarization for the GaN-based HEMTs can be divided into two types, namely the spontaneous polarization and the piezoelectric polarization. In general, spontaneous polarization refers to the polarization at heterointerface without any strain, which are mainly determined by the net charge at the crystal growth front. On the other hand, piezoelectric polarization results from the difference between lattice constants of III-N semiconductors of the heterostructures. Generally, piezoelectric polarization increases as the strain at the interface raises [23].

For spontaneous polarization, the direction of the polarization field in nitride-based materials relies on the polarity of the crystal [24]. Along the common growth direction (c-axis) for hexagonal wurtzite structure of nitride-based materials, the atoms are arranged in bi-layers. These bi-layers contains two

closely spaced hexagonal layers, one generated by Ga atoms and the other generated by N atoms. If the surface has $[0001]$ polarity, the top position of the $\{0001\}$ crystal plane are Ga atoms and it is referred as Ga-face (Fig.1.2.(a)). In contrast, $[000\bar{1}]$ polarity has only N atoms at the surface and is referred as N-face (Fig.1.2.(b)). Ga-face and N-face surfaces of GaN are not equivalent and have different chemical and physical properties [23]. N-face crystals are chemically active and make wet chemical etching of the material possible, but suffer serious rough surface morphology and high background carrier concentration issues. In contrast, Ga-face crystals have much smoother surface morphology and lower background carrier concentration, which are advantageous for buffer resistivity and thus beneficial for electrical device isolation. However, it can only be etched away by using plasma etching method [25]. Anyway, despite of etch issue, Ga-face crystals have superior electron transport properties and thus are preferred for device operation [26]. Therefore, for nitride-based semiconductor HEMTs, we generally discuss about Ga-face devices unless specifically mentioned.

For piezoelectric polarization, when a thin AlGaN barrier is deposited on the GaN channel layer to form AlGaN/GaN heterostructure, strain will be induced due to the lattice mismatch between these two layers and this strain will yield a piezoelectric polarization. In general, as compared to other traditional III-V semiconductor materials like GaAs, the piezoelectric polarization for nitride-based materials is significantly larger [27]. Increasing the Al-content in the strained AlGaN will lead to a further increase in piezoelectric polarization.

Fig.1.2 Wurtzite crystal structure for (a) Ga-faced and (b) N-faced.

Fig.1.3 AlGaN/GaN heterostructure and its band diagram.

The typical energy band profile for AlGaN/GaN heterostructure is indicated in Fig.1.3 [7]. Obviously, piezoelectric and spontaneous polarization difference

between the AlGaN barrier and GaN channel layer will yield positive charges at the interface. The positive charges will attract electrons and lead to the accumulation of electrons at the interface to generate a 2DEG channel. A typical sheet carrier density of $\sim 10^{13} \text{ cm}^{-2}$ for a 2EDG channel was reported for the AlGaN/GaN heterostructure [26].

1.3. Basic Device Characteristics of GaN HEMTs

The basic DC behavior of GaN HEMTs are generally characterized by two important parameters: the saturation current I_{DS} and the transconductance g_m .

A typical DC I - V output curves of the GaN HEMT devices are shown in Fig.1.4 (a). The dotted parabola in Fig.1.4 (a) indicates saturation voltage. It is the drain to source voltage at which the drain current saturates under a given V_{GS} . This parabola separates the output curve into linear and saturation regions.

Transconductance g_m is one of the most important indicators for device microwave applications. It has strong relations with device gain and high frequency properties. The transconductance is defined as [28]:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS} = \text{constant}} \quad (1.1)$$

The transconductance g_m as a function of V_{GS} is shown in Fig. 1.4 (b).

Fig.1.4 DC I - V characteristics of GaN HEMTs: (a) output curve; (b) transfer curve.

For GaN HEMT high power applications, the output density (P_{out}) and the power added efficiency (PAE) are two important parameters. Fig.1.5 shows the typical I - V curves for GaN HEMTs operated in class A mode. In class A operation, the maximum output power delivered from GaN HEMTs is given by [29]:

$$P_{out} = \frac{I_{dmax}(V_{BR} - V_{knee})}{8} \quad (1.2)$$

where I_{dmax} means the maximum drain current, V_{BR} means the breakdown voltage and V_{knee} is the knee voltage. It is clear from equation 1.2 that to achieve high power the values of V_{BR} and I_{dmax} should be as large as possible.

For class A operation, the PAE of the device can be written in terms of the power gain as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{p_{out}(1 - 1/G_a)}{P_{DC}} = \frac{1}{2} \left(1 - \frac{1}{G_a}\right) \quad (1.3)$$

where G_a is the power gain of device. It is obvious from equation 1.3 that the maximum value (50%) of PAE for class A operation can be obtained with the infinity power gain G_a .

Fig.1.5 Schematic I - V characteristics for GaN HEMTs operated in class A mode.

1.4 High- k Gate Dielectric for GaN-based Transistors

Although GaN-based HEMTs have shown their great potential for high frequency high power applications, one critical issue that further limits the performance and reliability of GaN-based HEMTs is the high gate leakage current. In general, high gate leakage current will reduce the power added efficiency [30] and breakdown voltage [31] and increase minimum noise figure

($NF_{\min}$) of GaN-based HEMTs [32]. To overcome the above problems, GaN Metal-Insulator-Semiconductor HEMTs (MISHEMTs) are employed. As illustrated in Fig.1.6, through the insertion of the dielectric layer between gate and underlying GaN-based substrates, significantly larger potential barrier between the gate metal and conductive channel will be provided and this will effectively suppress the gate leakage current and keep a reasonably larger gate voltage swing. In addition, the gate dielectric can also acts as a surface passivation to reduce current collapse and surface leakage for GaN HEMTs. As current collapse and surface leakage are two important device operational issues related to GaN MISHEMTs, detailed introduction will be conducted in Chapter 2.

Fig.1.6 A typical band diagram for AlGaN/GaN MISHEMTs.

In the early stage, GaN-based MISHEMTs with SiO_2 and Si_3N_4 as the gate dielectric have been proven to be a good method to suppress the aforementioned gate leakage issue [33-35]. However, as indicated in Fig.1.7, a

prominent reduction in transconductance g_m and a severe shift of threshold voltage V_{th} were observed for MISHEMTs utilizing Si_3N_4 and SiO_2 as gate dielectric [34]. However, the usage of high- k dielectric is helpful to overcome these issues. Due to the larger dielectric constant, more efficient gate modulation can be obtained for GaN-based MISHEMTs with high- k dielectric, which will bring in a slighter reduction in g_m along with a moderate shift of V_{th} [36].

Fig.1.7 The saturation-current (a) and transconductance (b) in the saturation region for GaN MOSHFETs with SiO_2 as gate dielectric and baseline HFET devices. Drain to source voltage is 10 V.

1.5 Motivations and Objectives

Major characteristics, merits and drawbacks of the potential high- k candidates are summarized in Table.1.3 [37,38]. It is obvious from Table. 1.3 that there is

no perfect high- k materials in terms of all material properties. For example, Al_2O_3 has a large bandgap and good thermal stability, but exhibits a medium dielectric constant. While, on the other hand, Ti_2O_5 shows a high dielectric constant, but its bandgap is too small.

However, due to its high dielectric constant (~ 25) [39,40] and large band gap energy (~ 5.6 eV) [41,42], ZrO_2 is a good option among the listed high- k candidates in terms of overall material properties. Compared with ZrO_2 prepared by other techniques [43-46], atomic layer deposition (ALD) technique has the advantages of high uniformity, precise thickness control down to atomic scale, good coverage and low trap defect density and so on [47,48]. However to-date, comprehensive study was not carried out in AlGaIn/GaN MISHEMTs on Si with ALD- ZrO_2 as the gate dielectric. On the other hand, the interfacial properties between GaN-based substrates and ALD- ZrO_2 play a significant role in determining the device performance. In general, the process conditions during device fabrication have great influence on interfacial properties. Unfortunately, so far, only a few studies have been carried out on the analysis of interfacial properties between ALD- ZrO_2 and GaN-based semiconductors on the influence of fabrication processes. In this thesis, detailed investigations of high- k ZrO_2 gate dielectric deposited by ALD on GaN-based semiconductors will be carried out.

Table 1.3 Major characteristics and problems associated with the major high- k candidates.

Dielectric	Dielectric Constant (k)	Bandgap (eV)	Merits	Drawbacks
Al_2O_3	9-10	8.8	Large E_g Amorphous Good thermal stability	Medium Q_{ox} Medium k
Ta_2O_5	25	4.4	High k	Small E_g
La_2O_3	27	5.8	High k Better thermal stability	Moisture absorption High Q_{ox}
Y_2O_3	15	6	Large E_g	Low crystalline temperature
HfO_2	25	5.6	Most suitable compared with other candidates	Crystallization
ZrO_2	25	5.6	Most suitable compared with other candidates	Crystallization

1.6 Overview of This Thesis

This thesis mainly focuses on the application of ALD-ZrO₂ as high- k gate dielectric for GaN-based transistors.

In chapter 2, a review of the influence of surface traps on devices performance such as current collapse and surface leakage is introduced to better understand the importance of the insertion of high- k dielectric materials as gate insulator and passivation layer for AlGaIn/GaN HEMTs. Two major challenges presented for AlGaIn/GaN MISHEMTs, which are band alignment and interfacial properties between ALD-ZrO₂ and GaN-based semiconductors, will also be discussed.

In chapter 3, basic information related to the deposition and analytical methods, which are atomic layer deposition (ALD) and X-ray photoelectron spectroscopy (XPS), is introduced in the first part. In the following part, angle-resolved XPS measurements combined with mathematical calculations utilized to determine the band alignment between ALD-ZrO₂ and GaN substrate are introduced.

In chapter 4, a comprehensive study on the influence of device fabrication processes on the interfacial properties between ALD-ZrO₂ and GaN-based semiconductors are conducted. X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscope (HR-TEM) are utilized to analyze the interfacial chemical bonding states and observe the interfacial layers, respectively. The interfacial trap states induced by the sub-oxide layers

formed at the interface are highly relied on the surface pre-treatment method before ALD deposition and post-deposition annealing (PDA) temperatures.

In chapter 5, AlGaIn/GaN MISHEMTs on Si with 10 nm thick ALD-ZrO₂ as gate dielectric are demonstrated. The analysis of interface trapping effects is also conducted. For AlGaIn/GaN MISHEMTs, owing to the use of ALD-ZrO₂, the reverse gate leakage current is effectively suppressed and forward gate input bias is extended to a higher value. In addition, low interface trap state density is also confirmed by “Hi-Lo frequency” and AC conductance methods.

In chapter 6, the most inspiring results of this thesis are summarized and recommendations for the future work based on current studies are also proposed.

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Chapter 2

Application of Gate Dielectric for AlGaN/GaN MISHEMTs

2.1 Introduction

AlGaN/GaN HEMTs have demonstrated their excellent performance in high frequency [1], high power [2], and low noise applications [3]. Currently, the two main factors that further limit the reliability and performance of AlGaN/GaN HEMTs are their large gate leakage current [4] and severe current collapse [5]. The surface traps may be the main contribution to the above-mentioned issues. By the insertion of high- k dielectrics as gate insulator and passivation layer for AlGaN/GaN MISHEMTs, gate leakage and current collapse problem can be significantly mitigated. In this chapter, mechanisms for current collapse and surface leakage caused by surface states will be illustrated. In addition, the benefits and major challenges for AlGaN/GaN MISHEMTs will also be discussed.

2.2 Impact of Surface States on AlGaN/GaN HEMTs

Traps are generally referred as the energy states located in the bandgap of a semiconductor or an insulator. The origins of traps could be attributed to a

combined result of many different factors, such as dislocations, defects in crystal or the incorporation of the impurities. There are mainly two types of trap states, namely acceptor-like and donor-like traps [6,7]. For acceptor-like traps, they will get negatively charged when occupied by electrons and keep neutral when empty. On the other hand, for the donor-like traps, they become neutral once occupied by electrons and get positively charged when empty [6,7]. The traps at the surface of the semiconductors have great impact on the device operation and performance. For GaN-based HEMTs, the surface traps will cause severe issues including current collapse [8-10] and surface leakage [11].

2.2.1 Current Collapse

The current collapse is defined as the discrepancy between the DC and pulse measurement of I - V curves. As indicated in Fig.2.1 (a), pulse I - V measurements are realized by applying a pulse signal which drives the device from a defined quiescent point Q (generally a high off state below breakdown) to points of the I - V curves in order to show the I - V characteristics. When GaN HEMTs are biased under a high V_{DS} off-state condition, a high electric field will exist at the side of the Schottky gate close to the drain. Such high electric field will lead to an injection of electrons from the gate metal to the surface traps [12,13]. As a consequence, the channel below is depleted by the trapped electrons (Fig.2.1 (b)). When GaN HEMTs are turned on, the trapped electrons could emit from the traps and increase the current in the channel (Fig.2.1 (c)). However, if the

Fig.2.1 (a) Schematic comparison of DC I - V characteristics and pulse I - V characteristics when the GaN HEMTs show current collapse issues. (b) Traps behavior in GaN HEMTs when it is under off condition. Large amount of electrons trapped at the surface will deplete the electrons in the channel. (c) Traps behavior in GaN HEMTs when it is under on condition. The emission of trapped electrons at the surface will increase the carrier density in the channel. (d) A schematic diagram to show series connection of the virtual gate induced by surface traps and transistor metal gate.

traps are deep in the bandgap, the emission process is considerably slow. As a consequence, the slow recovery of the current during pulse on-state transient in the channel will lead to higher on-resistance (R_{ON}) and low saturated channel

current I_{dmax} as depicted in Fig.2.1 (a). The region over which the 2DEG depletion spread can be referred as “virtual gate” V_G , which is firstly proposed by Vetury [14]. As indicated in Fig.2.1 (d), the virtual gate forms a series connection with the metal gate and this connection can control the current flow in the channel under pulse on-state transient [14,15].

The maximum output power delivered from GaN HEMTs is given by [16]:

$$P_{out} = \frac{I_{dmax} (V_{BD} - V_{knee})}{8} \quad (2.1)$$

where I_{dmax} means the maximum drain current, V_{BD} means the breakdown voltage and V_{knee} is the knee voltage. As can be seen from Fig.2.1 (a), with the presence of surface traps in GaN HEMTs, the V_{knee} moves towards a higher V_{DS} value and I_{dmax} drops to a lower I_{DS} value, which will lead to a reduction of overall output power during switching (pulse characteristics). On the other hand, due to the increase in the R_{ON} , dynamic conduction losses during switching will also occur. Overall, due to current collapse, the high frequency characteristics of GaN HEMTs are not able to match those predicted by DC performance.

2.2.2 Surface Leakage

For GaN HEMTs, except the vertical gate leakage through one-dimensional transport at Schottky interface, surface leakage by lateral injection of electrons

to the AlGaN surface through the edge of the gate will also cause instability in device operation [17,18]. J. Kotani [17] and Z. H. Liu [18] reported that two-dimensional variable-range hopping (2D-VRH) assisted by a high-density of electronic states at the AlGaN surface could be the possible mechanism for surface leakage current. Fig.2.2 demonstrates a simple model for the generation of surface leakage current in the vicinity of the Schottky gates assisted by surface states [17]. As indicated in Fig.2.2, high electric field at the gate metal edge will bring in lateral injection of electrons to AlGaN surface electronic states through the tunneling. With the assistance of 2D-VRH conduction through the high-density AlGaN surface electronic states, these laterally injected electrons could propagate towards drain electrode and then generate the surface leakage current.

Fig.2.2 A simple model describing the two-dimensional variable-range hopping (2D-VRH) assisted by AlGaN surface electron states. I_V is the vertical gate leakage, while I_S is the surface gate leakage.

2.3 Advantages of AlGaN/GaN MISHEMTs with High- k Dielectrics as Gate Insulator and Passivation Layer

By incorporation of dielectrics as gate insulator for AlGaN/GaN MISHEMTs, device performance is effectively improved owing to the reduction of gate leakage current. In addition to be utilized as a gate insulator, gate dielectric can also serve as a passivation layer to passivate surface traps for AlGaN/GaN HEMTs. Through the passivation, device reliability issues caused by surface traps such as current collapse and surface leakage can also be effectively mitigated.

To date, a number of dielectrics have been considered as surface passivation layer and gate insulator for AlGaN/GaN HEMTs. In the early stage, Si_3N_4 [19,20] and SiO_2 [21] were the extensively researched gate dielectric for AlGaN/GaN MISHEMTs. This is largely related to their widespread usage in Si-based CMOS technologies. However, due to their low dielectric constant, a significant unexpected decrease in transconductance g_m [22] and an obviously large threshold voltage V_{th} shift to negative side [22] were observed, which is rather detrimental for high frequency operation for AlGaN/GaN MISHEMTs. To solve these problems, high permittivity (high- k) dielectric are utilized. Owing to the high dielectric constant, more efficient gate modulation over the 2DEG channel is achieved. It only causes a slight reduction in g_m [23] and a moderate shift of the V_{th} [23]. During the last few years, prominent progress has been achieved on AlGaN/GaN MISHEMTs using high- k materials including

Sc₂O₃ [24], MgO [24], Al₂O₃ [25], HfO₂ [26,27], ZrO₂ [27] and their related gate stacks [28] as the gate insulator and passivation layer.

2.4 Major Challenges for AlGaN/GaN MISHEMTs

In addition to high dielectric constant property, the criteria to choose high- k material as gate insulator and passivation layer include their band gap energy, critical breakdown electric field, chemical properties, thermal properties etc. However, in order to effectively reduce gate leakage current and passivate surface traps, two most important considerations are band alignment and interfacial properties between high- k dielectric and GaN-based semiconductor substrate.

2.4.1 Band Alignment between Gate Dielectric and GaN Substrate

Ideally, a high- k gate insulator should have a large band gap and a reasonably high dielectric constant. However, the two properties are often inversely related for high- k materials [29]. Thus, the band alignment between gate dielectric and GaN substrate is a critical issue to inhibit gate leakage. As depicted in Fig.2.3, two major quantities used to evaluate the band alignment between high- k dielectrics and GaN substrates are conduction band offset (CBO) and valence band offset (VBO). The CBO is the difference between the minimum in the

conduction band of two materials; while VBO is difference between the maximum in the valence band of two materials. In order to use high- k materials as gate insulator in GaN-based transistors, it should have sufficiently high (> 1.0 eV) tunneling barrier to both holes (VBO) and electrons (CBO) to suppress gate leakage [30].

Fig.2.3 Band alignment between high- k dielectrics and GaN substrates. χ , which is the energy difference between the vacuum level and the conduction band minimum, is referred as the electron affinity. E_g is the band gap. ΔE_V and ΔE_C are valence band offset (VBO) and conduction band offset (CBO) between dielectric and GaN, respectively.

2.4.2 Interfacial Properties between High- k Dielectrics and GaN Substrates

For a simple dielectric-semiconductor system, four types of charges are generally identified. As indicated in Fig.2.4, they are mobile oxide charge,

Fig.2.4 Four different types of charges and their location for dielectric layers on semiconductors.

Fig.2.5 A simple model to describe the dependence of charge or discharge of interface traps on surface potentials.

oxide trapped charge, fixed oxide charge and interface trapped charge [31]. Among these charges, the interface trapped charges, which can electrically communicate with the underlying semiconductor have prominent impacts on device performance. In general, the interface trapped charges are mainly caused by structural defects, oxidation-induced defects, metal impurities or other defects introduced by bond breaking processes (such as radiation or hot electrons), and they are located at the interface between dielectric layers and semiconductors [31]. It is shown in Fig.2.5 that the charge or discharge of

interface traps is highly depending on the surface potential [31]. Since the presence of the interface trapped charges can be ascribed to the dangling bonds at the interface between the insulator and semiconductor, high quality interfacial properties between gate dielectric and GaN is a key factor to realize GaN-based devices with excellent performance.

For AlGaIn/GaN MISHEMTs, unintentional and uncontrolled surface oxidation of GaN-based semiconductors during the fabrication was reported to result in side effects on device performance such as high gate leakage [32-34], low breakdown [35], threshold voltage shift [36] and severe current collapse [33,34,37]. The interface disorder caused by such oxidation will introduce a high density of interface states at GaN-based semiconductor surface [38-42]. Removal or passivation of such oxygen-induced surface traps can mitigate the above issues. In recent years, surface treatment before dielectric deposition was reported to be an effective method to reduce trap density associated with sub-oxide layers at the surface [32,33].

Summary

Surface traps of AlGaIn/GaN HEMTs result in severe current collapse and large surface leakage. The use of high- k dielectrics as gate insulator and passivation layer is an effective method to alleviate these issues. However, in order to effectively reduce the gate leakage current, reasonably large VBO and CBO are

required for high- k materials. On the other hand, interfacial properties between high- k dielectrics and GaN-based semiconductors could deteriorate due to the unintentional and uncontrolled surface oxidation during AlGaIn/GaN MISHEMTs fabrication. The sub-oxide layer, which results in high density of interfacial traps should be removed or passivated to improve device performance.

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Chapter 3

Band Alignment between GaN and ZrO₂ Formed by Atomic Layer Deposition

3.1 Introduction

Excellent electrical characteristics of GaN-based MISHEMTs with the utilization of ultrathin high- k ZrO₂ dielectric as gate insulator and passivation layer have been investigated recently [1-6]. One of the main parameters, which has great impact on the properties of GaN-based MIS structures, is the band alignment between gate dielectric layer and GaN substrate. In order to maintain low gate leakage current and smaller effective oxide thickness, a large conduction band discontinuity ΔE_C (> 1 eV) between ZrO₂ oxide layer and GaN is required [7]. However, so far, ΔE_C at the ZrO₂/GaN interface has not been experimentally investigated. In this chapter, band alignment between atomic layer deposited (ALD) ZrO₂ and GaN is evaluated by using angle resolved XPS measurements combined with numerical calculations.

3.2 Deposition and Analytical Methods

3.2.1 Atomic Layer Deposition (ALD)

Atomic Layer Deposition (ALD) technique is capable of depositing ultrathin

films and now it is widely applied in semiconductor, optical, photovoltaic, and medical devices [8]. ALD has the ability to control the deposited film thickness down to atomic scale with a high precision and thus can generate pinhole free coatings with excellent thickness uniformity, even deep inside trenches with high aspect ratio [9].

Fig.3.1 Typical ALD growth cycles.

The main advantage for ALD technique is that the ALD process isolates the chemical vapor deposition (CVD) process into two parts and keeps the precursors separated during the reaction. As illustrated in Fig.3.1, a single ALD cycle generally contains four steps [10]: 1) Pulse of the first precursor into the chamber, 2) Purge the chamber to remove the non-reacted precursors and by-product gases, 3) Pulse of the second precursor, 4) Purge the reaction chamber again. After one cycle with four steps, a monolayer of film is then formed. In general, two major fundamental mechanisms are involved during ALD process, which are chemisorption saturation process and the sequential chemical

Fig.3.2 ALD growth procedure of Al_2O_3 .

reaction process. Since exactly one monolayer of film can be generated by one growth cycle, the number of the growing cycles can be utilized to precisely control the thickness of the deposited film. However, to optimize the ALD process, the precursor dose and purge time should be well-controlled [11]. Insufficient dose time will lead to unsaturated chemisorption at surface and thus bring in uniformity issue. On the other hand, insufficient purge can leave gas-phase residues, which will cause CVD-type reactions when the next precursor is introduced. The unexpected CVD-type reactions will degrade film qualities by introduction of a high density of defects.

An example of depositing Al_2O_3 using Trimethylaluminum (TMA) and H_2O as precursors in ALD system is illustrated in Fig.3.2 [8]. Precursors TMA and H_2O are alternatively pulsed into the chamber to deposit the Al_2O_3 film.

3.2.2 X-ray Photoelectron Spectroscopy (XPS)

As illustrated in Fig.3.3, the basic working principle of XPS is the photoelectric effect. In this process, with the absorption of an incident photon ($h\nu$), a core-level electron of the atom will be emitted with a characteristics kinetic energy (KE). The binding energy (BE) of the electron can thus be calculated as follows:

$$BE = h\nu - KE - \phi_{spec}, \quad (3.1)$$

where ϕ_{spec} is the spectrometer workfunction. This parameter accounts for the energy loss of the emitted electron during its passing through the apparatus until

the final detection and needs to be properly calibrated to ensure an accurate determination of peak positions. During the calculation of the *BEs*, fermi-level is commonly used as the reference. The XPS spectral lines are identified by the shell where the electrons are ejected (like *1s*, *2s*, *2p*, etc.).

Fig.3.3 A schematic illustration of the x-ray photoelectron spectroscopy (XPS) system and the description of electron excitations in XPS.

The energy of the emitted photoelectrons from a sample gives a spectrum containing a series of peaks and the binding energy of the peaks is the characteristics of each element in the sample. In general, the binding energy for a core-level electron from an atom is the competitive result between the

coulomb interactions with other electrons and attractive force from the nucleus. Through the screening effect, reduction of the attraction from the nucleus for a core-level electron could occur with the interactions with its surrounding electrons. If the atom is bound to another atom with a larger electronegativity, some outer-shell electrons of this atom could be transferred to its neighbor atoms owing to the chemical reactions, which will result in a reduction of coulomb interaction between the remaining electrons, and cause the effective increment of the binding energy. For example, an increase in oxidation state of one element in sample will cause the binding energy to increase due to the decrease in the screening of other bound electrons from the ion core. The above phenomenon makes XPS a powerful analytical technique utilized not only for estimating the elemental composition but also chemical states of the elements in sample [12]. Due to the limited sampling depth of XPS (<10 nm), XPS is thus a powerful tool to determine the interfacial chemical bonding environment between dielectrics and semiconductors.

As presented in Fig.3.3, X-ray source and analysis system are the two key components for a XPS spectrometer. The characteristic X-rays will be generated with the acceleration of electrons emitted from a hot filament through a high voltage onto a metal anode. Al and Mg are the two most commonly used anodes and their corresponding photon energies are 1486.7 eV and 1253.6 eV, respectively. In order to provide a higher resolution, a monochromator is used for X-ray sources. The function of the X-ray monochromator is designed to generate a narrow X-ray line through Bragg's diffraction in a crystal lattice.

With the utilization of the analysis system, which mainly consists of analyzers and detectors, kinetic energy of the photonelectrons can be obtained.

3.3 Band Alignment Measurement by XPS

As discussed in Chapter 2, the two major quantities used to describe the band alignment between gate insulator and semiconductor substrate are the conduction band discontinuity ΔE_C (or conduction band offset CBO) and valence band discontinuity ΔE_V (or valence band offset VBO). In order to use high- k materials as the gate insulator for AlGaIn/GaN MISHEMTs, the ΔE_C and ΔE_V between the potential gate dielectric and GaN substrate should be large enough (> 1 eV) to effectively suppress both electron and hole gate leakage.

Among the different methods of determining band alignment, the XPS measurement method, which was first reported by Kraut [13] on the estimation of ΔE_V of Ge/GaAs heterojunctions, is believed to provide a high accuracy. Through the XPS measurement of the energy difference between core-level position and the valence band maximum (VBM) for each bulk material and the energy of the core-level positions at the interface, the calculations of ΔE_V and ΔE_C between semiconductor X and insulator Y shown in Fig.3.4 are given by the following expressions [13]:

$$\Delta E_V = [E_{CL}^X(b) - E_V^X(b)] - [E_{CL}^Y(b) - E_V^Y(b)] - \Delta E_{CL}, \quad (3.2)$$

$$\Delta E_{CL} = [E_{CL}^X(i) - E_{CL}^Y(i)], \quad (3.3)$$

$$\Delta E_C = E_g^Y - E_g^X - \Delta E_V, \quad (3.4)$$

where $E_{CL}^X(b) - E_V^X(b)$ and $E_{CL}^Y(b) - E_V^Y(b)$ are the differences between core-level energy and VBM for bulk material of semiconductor X and insulator Y, respectively. $\Delta E_{CL} = E_{CL}^X(i) - E_{CL}^Y(i)$ is the energy difference between core-level positions of semiconductor X and insulator Y at the interface.

Fig.3.4 Determination of band alignment between an insulator Y and a semiconductor X by XPS measurement method.

3.4 Band Alignment between GaN and ALD-ZrO₂ by Angle-resolved XPS Measurement

For a polar semiconductor like GaN or AlN, large polarization combined with

Fig.3.5 The schematic band diagram describing the impact of upward band bending at GaN surface on the evaluation of valence band discontinuity ΔE_V at ZrO₂/GaN interface by using angle-resolved XPS measurements. The potential gradient in ZrO₂ layer will bring in similar effect on the evaluation of ΔE_V . $q\Delta V_{ZrO_2}$ is the potential drop in ZrO₂ oxide layer.

possible surface Fermi-level pinning caused by surface defects will bring in sharp surface band bending in GaN-based semiconductors [14-19]. On the other hand, potential gradient could also exist in high- k dielectric, which could be attributed to the possible fixed/trapped charges presented in the oxide layers [20-23]. In such case, ΔE_V at the ZrO₂/GaN interface measured by commonly used XPS method with a fixed take-off angle θ could be erroneous. As indicated in Fig.3.5, if strong band bending occurred at GaN surface, the ΔE_V value

evaluated by XPS method with a fixed take-off angle θ , especially when measured under a large take-off angle θ , could deviate a lot from the theoretical result. To overcome this problem, angle-resolved XPS measurements combined with numerical calculations could be the possible method to ensure a better prediction of ΔE_V at ZrO_2/GaN interface [24-27].

In order to measure the ΔE_V at ZrO_2/GaN interface by XPS method, ZrO_2 with different thicknesses were deposited on un-doped GaN-on-sapphire substrates with ALD. The wafers were grown by MOCVD utilizing a commercial reactor. A GaN-on-sapphire substrate and a 30 nm thick ZrO_2 layer on GaN were used to obtain GaN and ZrO_2 bulk material properties, respectively. For the investigation of ZrO_2/GaN interface, sample with ~ 2 nm thick ZrO_2 on GaN surface was used. To deposit the ZrO_2 on GaN, the GaN-on-sapphire wafers were initially degreased in acetone and subsequently in isopropyl alcohol (IPA) for 10 min. Before loading into the ALD chamber, samples were treated by buffered oxide etchant (BOE) solution to clean the surface native oxide and then rinsed by the flowing de-ionized (DI) water. ZrO_2 dielectric layer was deposited by a Cambridge Nanotech Savannah ALD system. The tetrakis-(dimethylamido)-zirconium and H_2O were used as the precursors. Chamber pressure and substrate temperature were set at 0.6 Torr and 250 °C, respectively. During the deposition, sequential 400 ms and 40 ms pulse of H_2O and Zr sources were introduced into the chamber separately. After each pulse of gas, the chamber was purged with N_2 for 6 seconds to remove excess precursors and by-product gases. The XPS measurements were carried out using a

monochromatic Al K α X-ray source of energy 1486.7 eV. The spectra are curve-fitted by a combination of Gaussian and Lorentzian line shapes utilizing a Shirley-type background subtraction. With the consideration of the variations in the peak core-level positions due to binding energy (BE) shift caused by surface charging, all XPS peaks were aligned to the C 1s peak at energy of 284.6 eV.

Fig.3.6 A schematic cross-sectional diagram for GaN-on-Sapphire with 2 nm thick ALD-ZrO₂ dielectric layer. The definition of take-off angle θ is also shown.

The schematic structure of the sample used for investigating the ZrO₂/GaN interface is shown in Fig.3.6, where the photoelectron take-off angle is defined as θ . In order to change the photoelectron escape depth (λ), the measurements were conducted under three different take-off angles (15°, 45°, and 75°). The λ can thus be defined as,

$$\lambda = \lambda_0 \sin \theta, \quad (3.5)$$

where λ_0 is the inelastic mean free path of photoelectrons.

Fig.3.7 The measured (open circles) and fitted (lines) XPS Ga 3d (a) core-level spectra and Zr 3d (b) core-level spectra for 2 nm thick ZrO₂ on GaN obtained at different take-off angles θ .

Fig.3.7 shows the Ga 3d and Zr 3d spectra obtained at different take-off angles for 2 nm ZrO₂ on GaN sample. Two components, which are Ga-N and Ga-O bonds, were observed for Ga 3d spectrum in Fig.3.7 (a); while, as shown in Fig.3.7 (b), Zr 3d spectrum could be deconvolved into two spin orbit split components, namely Zr 3d_{5/2} and Zr 3d_{3/2}. It can be seen that the Ga 3d spectrum showed a trend to shift to lower binding energies with the decrease in θ , which indicates that there is strong upward band bending occurred at GaN

surface. Similar to Ga 3*d*, a shift of spectrum to lower binding energies with the decrease of θ was also observed for Zr 3*d*. This implies the existence of potential gradient in ZrO₂ oxide layer. Using the energy difference between Ga-N bond component and Zr 3*d*_{5/2} spectra at a fixed take-off angle θ shown in Fig.3.6, the commonly used XPS method for the evaluation of valence band discontinuity (ΔE_V) between ZrO₂ and GaN is summarized as below:

$$\Delta E_V = [E_{CL}^{GaN}(b) - E_V^{GaN}(b)] - [E_{CL}^{ZrO_2}(b) - E_V^{ZrO_2}(b)] - \Delta E_{CL} \quad (3.6)$$

$$\Delta E_{CL} = [E_{CL}^{GaN}(i) - E_{CL}^{ZrO_2}(i)], \quad (3.7)$$

where the subscript CL and V denotes the BEs for the core-level position and valence band maximum (VBM). The bulk and interface binding energies are indicated by the notation (b) and (i), respectively. ΔE_{CL} is the BE difference between core-levels from each side of the interface at a fixed take-off angle XPS measurement as shown in Fig.3.6.

Predicted by Poisson's equation, the amount of band bending, which is caused by the spatially varying electrostatic potential, is only depending on the distance from the surface. Therefore, the quantities ($E_{CL} - E_V$) for bulk GaN and ZrO₂ should be independent of band bending [17]. The differences of binding energy between core-level position and VBM of bulk GaN and ZrO₂ are shown in Fig.3.8. The VBM of each sample is determined by extrapolating the leading edge of the valence band spectrum to the base line (the cross-over points in Fig.3.8) [28]. Using binding energies of Ga-N bond and Zr 3*d*_{5/2} spectra as the

Fig.3.8 (a) Ga 3d core-level position and valence band spectra (VB) for bulk GaN. The difference between Ga 3d core-level (Ga-N bond) and VBM is 17.34 eV. (b) Zr 3d core-level position and valence band spectra (VB) for thick ALD-ZrO₂ layer. The difference between Zr 3d core-level (Zr 3d_{5/2}) and VBM is 179.43 eV. The VBM is extrapolated from the intersection point between the leading edge of the valence band spectrum and the base line.

core-levels for bulk GaN and ZrO₂ respectively, the corresponding BE

difference between the core-level position and VBM are thus determined to be 17.34 eV and 179.43 eV.

As indicated in Fig.3.5, the accurate evaluation of ΔE_{CL} at ZrO_2/GaN interface could be influenced by surface band bending of GaN and potential gradient existing in ZrO_2 layer. The estimated ΔE_{CL} between ZrO_2 and GaN is highly relied on take-off angles and this will lead to uncertainties during the evaluation of ΔE_V . If large band bending at GaN surface and potential gradient exist in ZrO_2 layer that affects the XPS measurement results, correction is necessary for ΔE_{CL} . In brief, for a layer of thickness d , the intensity $I(E)$ of a core-level spectrum as a function of the binding energy E can be described by [24,25,27]:

$$I(E) = \int_0^d I_0(E, z) \exp\left(-\frac{z}{\lambda}\right) dz, \quad (3.8)$$

where z , λ and $I_0(E, z)$ are the depth from the surface, the escape depth of the photoelectrons and the spectrum generated at each depth point, respectively. For example, $I_0(E, z)$ for a single spin orbital can be given by the Pseudo-Voigt function in the following form [25]:

$$V(E, z) = I_{00} \left[\alpha \exp \left\{ -\ln 2 \frac{(E - E_0)^2}{(F/2)^2} \right\} + (1 - \alpha) \frac{1}{1 + \left\{ -\frac{(E - E_0)^2}{(F/2)^2} \right\}} \right], \quad (3.9)$$

where I_{00} , α , E_0 and F are the intensity, the ratio of the Gaussian function, the

binding energy of the core-level, and the actual full width at half maximum (FWHM), respectively. If surface band bending cannot be ignored on the scale of the escape depth of photoelectrons, E_0 should be treated as a function of depth z .

Fig.3.9 A schematic diagram describing the change in the spectral shape of the core-levels due to surface band bending.

As schematically outlined in Fig.3.9, the observed spectrum is obtained by integrating the true spectrum from each depth point along the bended core-levels through equation 3.8. Therefore, surface upward band bending in GaN results in the increase of E_{CL} with the incensement of θ to extend the probing depth λ . The above analysis is also applicable to the case when potential gradient exists in the ZrO_2 layer. For the correction of the measured ΔE_{CL} , in order to obtain the dependence of apparent binding energy values E_{CL} on take-off angles, numerical calculations considering the effect of surface band bending in GaN and potential gradient in ZrO_2 on the core-level spectra are

conducted.

Fig.3.10 Dependence of measured (open squares) and simulated (solid lines) BEs on take-off angles for (a) Ga-N bond from the GaN substrate layer and (b) Zr 3d_{5/2} from 2 nm thick ZrO₂ dielectric layer.

Assuming that the internal electric field in ZrO₂ dielectric and GaN substrate layer is uniform, the internal electric field can be obtained by fitting the apparent binding energy and FWHM. More details of the principle and calculation can be found in [25,27]. The dependence of measured and simulated

BEs on take-off angles for Ga-N bond from the GaN layer and Zr $3d_{5/2}$ spectra from a 2 nm thick ZrO₂ on GaN are shown in Fig.3.10. The internal potential drop of -400 meV for ZrO₂ layer, which provides a best fit between the measured and simulated binding energies, is obtained. The negative sign of the potential drop indicates that potential goes down in the ZrO₂ layer as the depth increases. To obtain a more accurate ΔE_{CL} at ZrO₂/GaN interface, binding energies E_{CL} for both Ga-N bond and Zr $3d_{5/2}$ spectra at $\theta=0^\circ$ obtained from simulated binding energy curves as well as potential drop in ZrO₂ layer are considered. The equation (3.7) can be written as:

$$\Delta E_{CL} = [E_{CL}^{GaN}(i) - E_{CL}^{ZrO_2}(i)]_{\theta=0^\circ} + q\Delta V_{ZrO_2}, \quad (3.10)$$

where q is the elementary charge, and $q\Delta V_{ZrO_2}$ is the potential drop in ZrO₂ layer. Combining equations 3.6 and 3.10, a ΔE_V of 1 eV and ΔE_C of 1.2 eV at ZrO₂/GaN interface are thus estimated with a total error of ± 0.2 eV [13]. A summary of the band alignment between GaN and ZrO₂ is given in Table 3.1.

Table 3.1 Summary of parameters for band alignment between ALD-ZrO₂ and Ga-face GaN.

GaN ($E_{CL}-E_V$) _{bulk} (eV)	ZrO ₂ ($E_{CL}-E_V$) _{bulk} (eV)	$E_{CL}^{GaN}(i)$ at $\theta=0^\circ$ (eV)	$E_{CL}^{ZrO_2}(i)$ at $\theta=0^\circ$ (eV)	$q\Delta V_{ZrO_2}$ (eV)	GaN E_g (eV)	ZrO ₂ E_g (eV)	ΔE_V (eV)	ΔE_C (eV)
17.34	179.43	19.19	181.87	-0.4	3.4	5.6 ^a	1.0	1.2

^aReferences [29] and [30]

Summary

The band alignment between ALD-ZrO₂ and Ga-face GaN was experimentally evaluated by utilizing XPS measurements. The core-level energy E_{CL} of the Ga 3d and Zr 3d decreased with the decrease of take-off angles θ , which suggests strong band bending occurred at GaN surface as well as the existence of potential gradient in ZrO₂ layer. ΔE_V of 1 eV and ΔE_C of 1.2 eV at ZrO₂/GaN interface were determined by taking into account of GaN surface band bending and gradient potential in ZrO₂ layer using angle-resolved XPS measurements combined with numerical calculations. The results suggest that ZrO₂ could serve as an excellent high- k insulator for both p and n-type carriers in GaN-based devices.

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Chapter 4

Influence of Fabrication Process on Interfacial Chemical Bonding States between (Al)GaN and ALD-ZrO₂

4.1 Introduction

Low quality interfaces induced by unintentional and uncontrolled oxidation during fabrication process is one of the major challenges presented for GaN-based transistors with MIS structures [1-6]. In order to have a comprehensive understanding of the chemical configuration of the interface between (Al)GaN substrates and atomic layer deposited (ALD) ZrO₂ dielectric layer as well as the impact of surface pre-treatment before ALD and post-deposition annealing, the primary focus of this chapter will be on the analysis of ZrO₂/(Al)GaN interface by using X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HR-TEM).

4.2 Effect of Surface Pre-treatment on Interfacial Chemical Bonding States of ALD-ZrO₂ on AlGaN

In order to improve the interfacial properties of dielectric on GaN-based

devices, pre-deposition surface cleaning is suggested to be a critical procedure to remove native oxide prior to ALD high- k dielectric. Surface cleaning of III-N materials with hydrofluoric acid (HF) solution is widely utilized as a surface pre-treatment process [7-9]. However, even though AlGa_{0.5}N has been extensively utilized in GaN HEMTs, only a few studies concerning the impact of pre-treatment on interfacial chemical bonding states for ZrO₂/AlGa_{0.5}N interfaces during ALD have been conducted. In the following text, the interfacial properties of ALD-ZrO₂/Al_{0.5}Ga_{0.5}N with and without buffered oxide etchant (BOE) treatment is analyzed by angle-resolved XPS and HR-TEM. The effectiveness of BOE pretreatment on the formation of interfacial oxide between the ALD-ZrO₂ and AlGa_{0.5}N are evaluated.

Commercially obtained unintentionally doped Al_{0.5}Ga_{0.5}N-on-sapphire substrates grown by MOCVD were utilized in this work. An Al to Ga ratio of 1:1 in the AlGa_{0.5}N layer was intentionally used to facilitate the comparison of the roles of Al and Ga upon different pre-treatments. The substrate wafers were initially degreased in acetone and subsequently rinsed by isopropyl alcohol (IPA) for 10 minutes. Samples with HF pre-treatment were dipped into BOE solution to clean surface native oxide and then rinsed by the flowing de-ionized (DI) water prior to ALD deposition. The ALD process was carried out at a pressure of 0.6 Torr and a substrate temperature of 250 °C with tetrakis-(dimethylamido)-zirconium as the metal precursor and H₂O as the oxidant. During the deposition, 400 ms and 40 ms pulse of H₂O and Zr sources were introduced sequentially into the chamber. After each pulse, the chamber was

purged with N₂ for 6 s to remove excess precursors and by-product gases. Samples with 2 nm thick ZrO₂ were utilized for XPS characterizations. The XPS measurements were carried out as described in Chapter 3. The schematic structure of the sample used for investigating the ZrO₂/AlGa_{0.5}N interface by XPS measurements is shown in Fig.4.1, where the photoelectron take-off angle is defined as θ . The take-off angle θ was changed to vary the photoelectron escape depth λ according to

$$\lambda = \lambda_0 \sin \theta, \quad (4.1)$$

where λ_0 is the inelastic mean free path of photoelectrons. By decreasing of θ to shorten the probing depth, more sensitive analysis of chemical binding states near the interface between ZrO₂ layer and Al_{0.5}Ga_{0.5}N substrate can be obtained.

Fig.4.1 A schematic cross-sectional diagram for Al_{0.5}Ga_{0.5}N with 2 nm ALD-ZrO₂ dielectric layer for XPS measurements. The definition of take-off angle θ is also shown.

Fig.4.2 The measured (open circles) and fitted (lines) XPS Ga 3d core-level spectra for 2 nm ALD-ZrO₂ on (a) untreated AlGaIn with native oxide and (b) BOE treated AlGaIn at three different take-off angles θ of 15°, 45°, and 75°.

The Ga 3d and Al 2p spectra obtained at three different take-off angles θ of 15°, 45° and 75° for ZrO₂ on the untreated sample with native oxide (S1) and BOE treated sample (S2) are illustrated in Figs.4.2 and 4.3, respectively. Ga 3d spectrum in Fig.4.2 could be deconvoluted into two components, corresponding to Ga-N and Ga-O bonds, while Al-N and Al-O bond components are observed for Al 2p spectrum as shown in Fig.4.3. The existence of the oxygen-related

Fig.4.3 The measured (open circles) and fitted (lines) XPS Al 2p core-level spectra for 2 nm ALD-ZrO₂ on (a) untreated AlGaN with native oxide and (b) BOE treated AlGaN at three different take-off angles θ of 15°, 45°, and 75°.

chemical bonding states of Ga 3d and Al 2p spectra for BOE treated sample could be attributed to the parasitic oxidation of AlGaN surface during ALD deposition process after cleaning [10-13]. By comparison of Ga-O and Al-O bonding states between S1 and S2 as shown in Figs.4.2 and 4.3, significantly different oxidation characteristics between Ga and Al atoms are observed for ZrO₂/AlGaN samples. This implies that the impact of Ga and Al on the

Fig.4.4 The measured (open circles) and fitted (lines) XPS Ga 3d core-level spectra for 2 nm ALD-ZrO₂ on (a) untreated GaN with native oxide and (b) BOE treated GaN at three different take-off angles θ of 15°, 45°, and 75°.

formation of the interfacial oxide layer at ZrO₂/AlGa_{0.5}N interface could be different. On the other hand, it can be seen from Figs.4.2 and 4.3 that the shift of binding energy (BE) of Al-N and Ga-N bonds to lower values with the decrease of take-off angle θ , which indicates an upward band bending at AlGa_{0.5}N surface, are also highly relied on the Al-O/Al 2p and Ga-O/Ga 3d ratios. Such upward band bending could be ascribed to the surface Fermi-level pinning

caused by interfacial oxide related defects.

In order to distinguish the difference on the roles between Ga and Al atoms during parasitic oxidation and facilitate the analysis, samples with ALD-ZrO₂ on GaN using same pre-treatment and ALD process conditions are also tested to serve as the references. The Ga 3*d* spectra for ZrO₂ on untreated GaN (with native oxide) R1 and BOE treated samples R2 are given in Fig.4.4. As evidenced by the Ga-O bonding states, parasitic oxidation is also observed for BOE treated GaN during ALD deposition. However, no significant differences are observed between the untreated GaN and the one undergone BOE pre-ALD treatment.

To further analyze the interfacial chemical bonding states for ZrO₂ on AlGaN and referenced GaN, the dependence of Ga-O/Ga 3*d* and Al-O/Al 2*p* XPS peak area ratios on take-off angles θ are plotted in Fig.4.5. It can be seen from Fig.4.5 that both of the Ga-O/Ga 3*d* and Al-O/Al 2*p* area ratios increase with the decrease of θ , which suggests that the formation of the sub-oxide layer is mainly occurred within a narrow depth near the substrate surface for all samples. Furthermore, by comparison of the Ga 3*d* spectra, similar Ga-O/Ga 3*d* ratio between untreated (with native oxide) and BOE treated surfaces are observed for both AlGaN and GaN samples. Different from the Ga-O/Ga 3*d* ratio shown in Fig.4.5 (b), a drastic increase in Al-O/Al 2*p* with the decrease of take-off angles is observed for BOE treated AlGaN sample (S2) [Fig.4.5 (c)]. The large increase in Al-O/Al 2*p* ratio suggests that a prominent growth of

Fig.4.5 (a) Ga-O/Ga 3d ratio for ALD-ZrO₂ on untreated (R1) and BOE treated (R2) GaN surface as a function of take-off angles θ . (b) Ga-O/Ga 3d ratio for ALD-ZrO₂ on un-treated (S1) and BOE treated (S2) AlGaN surface as a function of take-off angles θ . (c) Al-O/Al 2p ratio for ALD-ZrO₂ on untreated (S1) and BOE treated (S2) AlGaN surface as a function of take-off angles θ .

interfacial oxide layer on BOE treated AlGaN surface is occurred during ALD deposition. This could be attributed to that Al atoms are easier to be oxidized than Ga atoms at AlGaN surface during ALD deposition process owing to the high reactivity of Al atoms [14-17]. In fact, the formation of the interfacial oxide layer for BOE treated AlGaN during the ALD can also be further confirmed by high-resolution transmission electron microscope (HR-TEM) indicated in Fig.4.6. Compared with the untreated AlGaN and referenced GaN

samples, the BOE treated AlGaN has obviously thicker interfacial oxide layer.

Fig.4.6 Cross-sectional TEM images of ALD-ZrO₂ on (a) untreated GaN with native oxide and (b) BOE treated GaN, (c) untreated AlGaN with native oxide and (d) BOE treated AlGaN. The interfacial layer is indicated as IL.

The XPS and TEM results clearly suggest that, compared to Ga, Al atoms on AlGaN surface may play a more important role in terms of parasitic oxidation during ALD deposition process. For either GaN or AlGaN buffer layer on Si, only slight difference of Ga-O/Ga 3d ratio between untreated samples with native oxide and BOE treated samples is observed. Thus, we believe that, for

Ga atoms, saturated oxidation of Ga atoms on both GaN and AlGaN surface could occur either under atmosphere condition or during ALD deposition process, which is very similar to the saturated thermal growth of silicon oxide on Si substrate [18]. However, on the contrary, because of the higher reactivity of Al atoms, the generation of a thicker interfacial oxide layer on BOE treated AlGaN surface as compared to its untreated counterpart covered with native oxide is evidenced by Al-O/Al 2*p* ratio and HR-TEM. For the untreated AlGaN, the native oxide on the AlGaN surface may serve as a protecting layer to inhibit the further parasitic oxidization during ALD deposition process, which gives a weak dependence of Al-O/Al 2*p* ratio on the take-off angles and a thin interfacial oxide layer.

The results suggest that the widely used BOE surface pre-treatment process prior to ALD may not be favorable for ZrO₂/AlGaN interface.

4.3 Impact of Post-Deposition Annealing on Interfacial Chemical Bonding States between ALD-ZrO₂ and GaN Substrate

As for device fabrication, post-deposition annealing (PDA) has been found to be an effective way to improve interfacial properties between high-*k* dielectric layer and semiconductor substrate for GaN-based devices [19-21]. Therefore, it is essential to analyze the thermal stability of the interface between ZrO₂ and

GaN substrate, which is critical for the application of ZrO₂ as high- k gate dielectric for GaN-based transistors. In order to investigate the impact of post-deposition annealing on the interfacial properties related to the formation/annihilation of interfacial GaO_x sub-oxide layer of ALD-ZrO₂ on GaN, XPS and HR-TEM characterizations are carried out.

ZrO₂ dielectric layers were deposited on GaN-on-sapphire substrates by using the ALD process described in Chapter 4.2. After dielectric layer deposition, different post-deposition anneals (PDAs) using rapid thermal annealing (RTA) in N₂ atmosphere for 30 s were performed in different temperatures ranging from 300 °C to 700 °C. Samples with ~2 nm thick ALD-ZrO₂ were used for XPS characterization. The take-off angle θ was set at 15°, which enabled sensitivity analysis of chemical states at the interface between ZrO₂ layer and GaN substrate.

Ga 3*d* core-level XPS spectra obtained for samples under different post-deposition annealing temperatures are depicted in Fig.4.7. Two components, namely the Ga-N and Ga-O bonds, can be observed for Ga 3*d* spectrum in Fig.4.7. The existence of the Ga-O spectrum for the as-deposited sample (indicated by N.A in Fig.4.7) could be attributed to the parasitic oxidation of the GaN surface after cleaning during ALD deposition process [10-13]. Apparently, the Ga-N bonds show an obvious increase in binding energies (BEs) with the increment of annealing temperatures while the annealing temperatures are lower than 500 °C. Further increment in annealing temperature shows a reduction of

Fig.4.7 The measured (open circles) and fitted (lines) XPS Ga 3d core-level spectra for ALD-ZrO₂ on GaN samples measured at take-off angle θ of 15° under different post-deposition annealing (PDA) temperatures. The as-deposited sample is indicated as N.A.

the BEs. As a polar semiconductor, GaN surface is sensitive to fabrication process. Sharp upward band bending at GaN surface owing to large polarization combined with possible surface Fermi-level pinning caused by surface defects may occur [22-27]. Meanwhile, as obtained from Fig.4.7, the integrated XPS intensity of Ga-O bond to Ga 3d ratio also shows variation related to annealing

temperatures.

For clarity, the dependence of Ga-N binding energy and ratio of the Ga-O to Ga 3*d* XPS peak area on the annealing temperature are plotted in Fig.4.8. It can be seen that the Ga-N binding energy has strong correlations with the ratio of Ga-O to Ga 3*d* peak area. In general, the decrease in the ratio of Ga-O to Ga 3*d* peak area leads to the increase of Ga-N bond binding energy. This indicates that the Fermi-level position at GaN surface is affected by surface-related defect states associated with GaO_x layer [28-32]. The surface states contribute to upward band bending at GaN surface. A higher defect density at ZrO₂/GaN interface could cause stronger upward band bending and hence lower Ga-N bond binding energy. The annihilation or formation of the gallium sub-oxide layer at the interface is highly related to annealing temperature. Under the annealing temperature of 500 °C, the Ga-N bond binding energy shows the highest value along with the smallest Ga-O to Ga 3*d* peak area ratio. The decrease in Ga-O bond concentration may suggest a “clean up” effect, which is most likely attributed to the formation of Ga-O-Zr configurations to passivate Ga-O bond. “Clean up” effect, which is also known as “self-cleaning” effect, refers to the reaction process (passivation effect) to remove interfacial native oxide during ALD deposition of dielectrics on III-V substrates [33-40]. It is firstly observed on GaAs and recently reported for GaN.

Fig.4.8 Change of Ga-N bond binding energy (BE) and integrated XPS intensity ratio of Ga-O bond to Ga 3d for ZrO₂/GaN samples under different post-deposition annealing (PDA) temperatures. The as-deposited sample is indicated as N.A and the dashed lines are for guidance to illustrate the trend.

HR-TEM is used to further characterize the interfacial properties between ALD-ZrO₂ and GaN. The cross sectional TEM micrographs of as-deposited sample (N.A) and samples annealed under 500 °C and 700 °C are shown in Fig.4.9. It is obvious from Fig.4.9, compared with the as-deposited sample, ZrO₂ thin films get further crystallized with the increasing of the annealing temperatures, which is consistent with the reports in the literature [41,42]. For the as-deposited film shown in Fig.4.9 (a), an interfacial layer could be found. An abrupt interface without any interfacial layers is observed for sample annealed under 500 °C. This may further indicate the “clean up” effect for ALD-ZrO₂ on GaN at

Fig.4.9 Cross-sectional TEM images of the ZrO_2 dielectric layers on GaN: (a) as-deposited (N.A) and (b) with a 500 °C post-deposition annealing in N_2 for 30 s and (c) with a 700 °C post-deposition annealing in N_2 for 30 s. The interfacial layer is indicated as IL.

annealing temperature of 500 °C. For the sample annealed at 700 °C in Fig.4.9 (c), re-formation of interfacial layer was observed. This could be attributed to the oxidation at the ZrO_2/GaN interface due to oxygen segregation at higher annealing temperatures [43,44]. The observation of the regrowth of interfacial layer at higher annealing temperatures is in consistence with the reduction of Ga-N binding energy. The annihilation or formation of the gallium sub-oxide GaO_x interfacial layer at the interface between ZrO_2 and GaN during the post-deposition annealing is dependent on annealing temperatures. The decrease in Ga-O to Ga 3d peak area ratio in the samples annealed at the temperatures below 500 °C can be attributed to the reduction of Ga-O bonds due to the

passivation of Ga-O bond through the “clean up” effect. While, oxidation at the ZrO_2/GaN interface due to oxygen segregation at higher annealing temperatures may lead to the increase of Ga-O to Ga $3d$ peak area ratio.

4.4 Impact of Post-deposition Annealing on Interfacial Chemical Bonding States between ALD- ZrO_2 and AlGa N Substrate

Although AlGa N has been extensively utilized in AlGa N /Ga N HEMTs, only a few studies have been explored on the interfacial structure and chemical bonding states at the interface between ZrO_2 and AlGa N subjected to post-deposition annealing. In this study, a detailed investigation of the impact of post deposition annealing on interfacial chemical bonding states between ALD- ZrO_2 and $\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}$ is carried out by using angle-resolved XPS and HR-TEM.

ZrO_2 dielectric layers were deposited on $\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}$ -on-sapphire substrates utilizing the ALD process recipe described in Chapter 4.2. The substrate wafers were grown by MOCVD utilizing a commercial reactor. An Al to Ga ratio of 1:1 in the AlGa N layer was intentionally used to facilitate the comparison of the roles of Al and Ga at the interface upon annealing. After ALD deposition, different post-deposition anneals using rapid thermal annealing (RTA) in N_2 atmospheres for 30 s were performed in the temperature range of 300 to 700 °C.

Fig.4.10 The measured (open circles) and fitted (lines) XPS Al 2*p* (a) core-level spectra and Ga 3*d* (b) core-level spectra for 2 nm ALD-ZrO₂ on Al_{0.5}Ga_{0.5}N samples at take-off angle θ of 90° under different PDA temperatures. The as-deposited sample is indicated as N.A.

The Al 2*p* and Ga 3*d* core-level spectra obtained at two take-off angles θ of 90° and 15° for 2 nm thick ZrO₂ on AlGa_{0.5}N samples under different PDA temperatures are shown in Figs.4.10 and 4.11, respectively. Al 2*p* spectrum in Figs.4.10 (a) and 4.11 (a) could be deconvoluted into two components, namely

Fig.4.11 The measured (open circles) and fitted (lines) XPS Al 2p (a) core-level spectra and Ga 3d (b) core-level spectra for 2 nm ALD-ZrO₂ on Al_{0.5}Ga_{0.5}N samples at take-off angle θ of 15° under different PDA temperatures. The as-deposited sample is indicated as N.A.

the Al-N and Al-O bonds; while Ga-N and Ga-O bond components are observed for Ga 3d spectrum as shown in Figs.4.10 (b) and 4.11 (b). The existence of the Al-O and Ga-O spectrum for the as-deposited sample (indicated by N.A in Figs.4.10 and 4.11) could be attributed to the parasitic oxidation of the AlGa_{0.5}N

surface after cleaning during ALD deposition process [10-13]. Obviously, the interfacial chemical bonding states for ALD-ZrO₂ on AlGa_{0.5}N are highly depending on the annealing temperatures.

Fig.4.12 Change of integrated XPS intensity ratios of Al-O bond to Al 2p and Ga-O bond to Ga 3d for ZrO₂/Al_{0.5}Ga_{0.5}N samples measured at take-off angles θ of 15° and 90° of different PDA temperatures. The as deposited sample is indicated as N.A and the dashed lines are for guidance to illustrate the trend.

Fig.4.12 plots the dependence of Al-O to Al 2p and Ga-O to Ga 3d XPS peak area ratio as a function of the annealing temperature at take-off angles of 15° and 90°. For both take-off angles, the Al-O/Al 2p and Ga-O/Ga 3d area ratios decrease with the increment in annealing temperature while the RTA

temperature is lower than 500 °C. This could be ascribed to the passivation of sub-oxide interfacial states through the “clean up” effect that is widely reported for ALD deposited high- k dielectric on III-V semiconductor substrates [33-40]. However, with the further increment in annealing temperature, re-growth of the sub-oxide interfacial layer is evidenced by the increase in Al-O/Al 2 p and Ga-O/Ga 3 d area ratios for both take-off angles.

Fig.4.13 Cross-sectional TEM images of the ZrO₂ dielectric layers on Al_{0.5}Ga_{0.5}N: (a) as-deposited (N.A), (b) annealed at 500 °C in N₂ for 30 s, and (c) annealed at 700 °C in N₂ for 30 s. The interfacial layer is indicated as IL.

In fact, the annihilation or formation of the interfacial layer can be further confirmed by HR-TEM. Cross-sectional TEM micrographs for as-deposited sample (N.A) and samples annealed at 500 °C and 700 °C are shown in Fig.4.13. An interfacial layer is observed for the as-deposited sample (Fig.4.13 (a)). An abrupt interface without any interfacial layer is observed by HR-TEM

for the sample annealed under 500 °C. With the further increase in annealing temperatures to 700 °C, re-formation of the interfacial layer is observed as shown in Fig.4.13 (c). This phenomenon is rather similar to the case of ALD-ZrO₂ on GaN, and hence may share the same mechanisms of annihilation/formation of the interfacial layer for ALD-ZrO₂ on GaN. On the other hand, it can be seen from Figs.4.10 and 4.11 that shift of binding energy of Al-N and Ga-N bonds is highly related to Al-O/Al 2*p* and Ga-O/Ga 3*d* ratios. This could be due to surface Fermi-level pinning caused by interfacial oxide related defects, which is also consistent with the observations for ALD-ZrO₂ on GaN.

As a ternary III-nitride semiconductor, interfacial chemical bonding states between ZrO₂ and AlGa_{1-x}N_x could be more complicated compared to ZrO₂/GaN. This is evidenced by the decrease or increase rate of area ratio upon annealing temperatures in Fig.4.12. The influence of annealing temperatures on both of the Al-O/Al 2*p* and Ga-O/Ga 3*d* area ratios at a smaller θ are more pronounced, which suggests the annihilation/formation of the interfacial layer is mainly occurred within a narrow depth near the AlGa_{1-x}N_x surface. More importantly, compared to Ga spectra, the Al-O/Al 2*p* area ratio shows more obvious variations with respect to the PDA temperatures at θ of 15°. This implies that, at annealing temperatures lower than 500 °C, the passivation of Al-O bonds at ZrO₂/AlGa_{1-x}N_x interface could be more effective compared with Ga-O bonds through the “clean up” effect. On the other hand, when the annealing temperature is further increased, Al atoms at the ZrO₂/AlGa_{1-x}N_x interface are

more likely to get oxidized than Ga atoms owing to the higher reactivity of Al atoms [14-17].

Summary

The interface states associated to the interfacial sub-oxide layer between ALD-ZrO₂ and GaN-based semiconductor layers are highly affected by the various device fabrication processes, such as surface pre-treatment before ALD deposition and post-deposition annealing.

The effectiveness of BOE pre-treatment on the formation of interfacial sub-oxide between the ALD-ZrO₂ and AlGa_{0.5}N are evaluated. Due to the high reactivity of Al atoms, parasitic oxidation during ALD deposition is largely enhanced on BOE treated AlGa_{0.5}N surface. For AlGa_{0.5}N, the presence of the native oxide at the surface may serve as a protecting layer to inhibit the surface from being further oxidized during the deposition and thus results in a much thinner interfacial oxide layer with better interface quality. Therefore, the widely accepted BOE surface pre-treatment may not be favorable for ALD-ZrO₂ on AlGa_{0.5}N.

The effect of post-deposition annealing in N₂ on interfacial chemical bonding states for ALD-ZrO₂ on GaN and Al_{0.5}Ga_{0.5}N is analyzed by XPS and TEM. The formation/annihilation of interfacial oxide layer is highly relied on the annealing temperatures. With the increase of temperatures to 500 °C, interfacial

quality is improved with the annihilation of the interfacial oxide layer, which could be ascribed to the “clean up” effect of ALD-ZrO₂ on GaN-based semiconductors. However, for AlGaN, higher effectiveness of the passivation of Al-O bond than Ga-O bond through the “clean up” effect near the interface is found. On the other hand, deterioration of the interface quality attributed to the re-growth of interfacial layer at higher annealing temperatures is observed. Due to higher reactivity of Al atoms, Al atoms are much easier to be oxidized compared to Ga atoms.

Overall, this study provide an important process guideline for the usage of ALD-ZrO₂ as high-*k* gate insulator and passivation layer for AlGaN/GaN HEMTs.

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Chapter 5

AlGaN/GaN MISHEMTs on Silicon with ALD-ZrO₂ as Gate Dielectric

5.1 Introduction

In this chapter, AlGaN/GaN MISHEMTs utilizing 10 nm thick ALD-ZrO₂ as gate insulator and passivation layer are fabricated and characterized. The whole fabrication process of MISHEMTs includes mainly five steps, namely mesa isolation, ohmic contact formation, gate dielectric deposition, gate formation and pad and interconnection metallization. For device characterization, commonly used C - V characterization technique was utilized to evaluate the interfacial properties. DC I - V characterization was applied to analyze the electrical characteristics like gate leakage current, transconductance g_m , breakdown voltage, etc.

5.2 Device Structure for AlGaN/GaN MISHEMTs on Si with ALD-ZrO₂ as Gate Dielectric

The device structure of AlGaN/GaN MISHEMTs utilizing ALD-ZrO₂ as the gate dielectric is shown in Fig.5.1. The AlGaN/GaN HEMT structures on high-

resistivity Si (111) are grown by MOCVD. The typical epitaxial structure consists of the following layers (from bottom to top):

Fig.5.1 Cross-sectional diagram of the AlGaN/GaN MISHEMT utilizing ALD-ZrO₂ as the gate dielectric layer.

Substrate: Because of the lack of native substrate, GaN epitaxy layers are generally deposited on a non-native substrate. Currently, there are mainly three types of substrates for the epitaxy growth of GaN HEMTs, namely SiC [1], sapphire [2] and Si [3]. The comparison of some key material properties between the three substrates and GaN is listed in Table 5.1 [4]. SiC, with the highest thermal conductivity and lowest lattice mismatch to GaN, is obviously the most suitable substrate. GaN HEMTs grown on SiC substrate always show the best power and noise performance. However, SiC substrate has the highest cost. Compared with SiC, sapphire substrate is more cost-effective and the lattice mismatch between GaN and sapphire is moderate among the three. But, unfortunately, the thermal conductivity of sapphire is the poorest among the

three materials, which limits the maximum output power density to be reached for the GaN HEMTs grown on it. Therefore, in general, output power density and noise performance of GaN HEMTs on sapphire are much worse compared to those grown on SiC.

Table 5.1 Physical properties of substrates used for GaN material growth.

Substrate	Lattice constant (Å)	Thermal conductivity (W·cm ⁻¹ ·K ⁻¹)	Thermal expansion coefficient	Lattice mismatch (%)
GaN	3.189	1.3	5.59	0
6H-SiC	3.080	4.9	4.2	3.4
Sapphire	2.747	0.5	7.5	13.9
Si	5.430	1.5	3.59	-70.3

Among the three substrates, Si substrate is the most cost effective. Furthermore, from Table 5.1, Si has a higher thermal conductivity than sapphire. In addition, Si substrates have the advantages to provide the ability to integrate the GaN HEMTs fabrication process with Si CMOS mature industrial process technologies. However, for conductive silicon substrate, it will cause a noticeable parallel conduction and large parasitic pad capacitance, which lead to extra signal loss and time delay, and thus are not suitable for RF and microwave circuit applications. In such cases, high-resistivity Si substrate is typically used to overcome these shortcomings [5]. Thus, silicon (111) substrates with high-resistivity (>6000 Ω·cm) were used for MISHEMT structures in this work.

Transition and nucleation layer: Currently, due to the large lattice mismatch between GaN and Si, one of the main challenges presented for GaN HEMTs on Si is the growth of crack-free high-quality GaN epilayers. However, with the utilization of a system of transition and nucleation layers [6-10], high quality and crack-free structures can be obtained, and thus making GaN HEMTs on Si attractive. This interlayer can reduce the lattice mismatch and stress between GaN epitaxial layers and the non-native substrates. Therefore, the design and growth of this layer is the key process to get high quality GaN epitaxial layer.

Buffer Layer: Part of this layer adjacent to the barrier layer is served as the channel layer. This layer has narrower band gap compared to the barrier layer and the 2DEG channel is formed close to the heterojunction in this layer. Hall measurement showed a two-dimension-electron-gas (2DEG) sheet carrier density of $1.3 \times 10^{13} \text{ cm}^{-2}$ and electron mobility of $1223 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K for HEMT structures used in this work. For buffer layers, a high resistivity or semi-insulating (SI) GaN layer is sometimes necessary to ensure complete channel pinch-off, low loss at high frequency, proper drain-source current saturation, and little cross-talk between adjacent devices [11,12]. Intentional dopants such as Iron (Fe) [13,14] and Carbon (C) [15,16] have been used to compensate the background unintentional dopants in this layer to reduce the buffer leakage. However, such intentional doping will bring in more carrier traps, which will give rise to serious side effect on HEMT device performance like current collapse [17,18]. Therefore, optimization of the buffer layer growth is still widely under research. In this work, unintentionally doped (UID) GaN buffer

layer is utilized.

Barrier layer: Barrier layer needs to have larger band gap energy than the buffer/channel layer and $\text{Al}_{0.27}\text{Ga}_{0.73}\text{N}$ is used in this work as the barrier layer. This layer is the most critical layer in HEMT structures and is typically un-doped. Generally, high Al composition is needed to provide a high conduction band offset ΔE_C , which can induce more carriers into the 2DEG channel and block the hot electrons spilling over into the barrier [19,20]. However, due to the crystal strain arising from the lattice mismatch between the buffer/channel layer and the barrier with the increasing composition of Al in the AlGa_N barrier, the maximum composition of Al in AlGa_N barrier is typically smaller than 30%.

Cap layer: To avoid oxidation of the epitaxial surface and to realize low resistance ohmic contact for the heterostructures, a thin cap layer is generally deposited on the top of the barrier layer [21]. This cap layer could be either un-doped or n^+ doped. For un-doped GaN cap, the gate can be directly formed on this layer without the need to remove this layer since the Schottky barrier height (larger than 1 eV) is sufficiently high enough. Since Schottky Barrier (SB-) HEMTs are utilized as reference in this work, un-doped GaN cap is thus used.

Dielectric layer: Compared with conventional GaN SB-HEMTs, an extra ALD- ZrO_2 dielectric layer with 10 nm thickness is inserted between the metal gate and the III-nitride semiconductor surface as the gate insulator and passivation layer in this work.

5.3 Fabrication Process of AlGaIn/GaN MISHEMTs on Si with ALD-ZrO₂ as Gate Dielectric

The fabrication process for the AlGaIn/GaN HEMTs utilizing ALD-ZrO₂ as gate dielectric is illustrated in Fig.5.2. The fabrication process for AlGaIn/GaN MISHEMTs contains mainly five steps: mesa isolation, ohmic contact formation, gate dielectric deposition, gate formation and pad and interconnection metallization.

1) Mesa Isolation

Each individual device and pad must be isolated from each other to avoid short-circuit. In this work, the isolation was realized by Inductively-Coupled-Plasma (ICP) etching. ICP dry etch system has the advantage of high plasma density, low ion and electron energy and fast etching speed. Thus, for ICP etching process, the plasma damage can be reduced while maintaining an acceptable etch rate. Photoresist AZ 1518 was used to open windows for mesa isolation through standard photolithography process. Cl₂/BCl₃ gases were used as the etchants for AlGaIn/GaN bulk materials. The etch depth was around 150 to 200 nm, which is deep enough to cut off 2DEG channel.

2) Ohmic Contact Formation

Low ohmic contact resistance is crucial to obtain high drain current, high frequency and low noise operations. The metal selection and stack structure, device material, surface pretreatment, barrier/cap doping, and post-deposition

annealing will all have influences on the ohmic contact resistance.

Fig.5.2 Fabrication process flow for AlGaIn/GaN MISHEMTs with 10 nm ALD- ZrO_2 as gate dielectric.

Photoresist AZ 5214 was used to define ohmic contact pattern through photolithography process. Before metal deposition, surface pretreatment is necessary to remove the surface oxide and contamination. BOE solution treatment was used as the pre-treatment on our samples.

Ti/Al/Ni/Au is currently the most commonly used metal stack for contacting with GaN bulk materials to form a low resistance ohmic contact for GaN HEMTs. Generally, Ti/Al is used to create N-vacancies in III-nitride semiconductor materials after annealing and these vacancies will contribute to the high concentration of n-type doping in the barrier layer [22]. Ti and Al can react with N to form AlN and TiN during the annealing. The formed TiN and AlN is rather thin and electrons can easily tunnel through this thin layer under the ohmic electrode [23,24]. Ni is used to prevent the interdiffusion of the Au and Ti/Al [24], and Au is used to avoid oxidation of the metal stack [25]. By optimization, the thickness of each metal layer in Ti/Al/Ni/Au scheme is 25/200/40/50 nm, respectively. After metal deposition and lift-off process, samples were annealed in nitrogen ambient at 825°C for 30 s in a rapid thermal annealing (RTA) system to form low ohmic contact.

Generally, the ohmic contact resistance can be estimated by using the transmission line method (TLM) technique. A linear TLM pattern with only two ohmic metal pads fabricated on an isolation mesa of AlGaN/GaN heterostructure is shown in Fig. 5.3 (a). The total resistance R_{total} between two pads can be calculated as [26]:

$$R_{total} = 2R_C' + R_{sh} \frac{L}{W} \quad (5.1)$$

where R_C' is the non-normalized ohmic contact resistance (Ω), R_{sh} is the sheet resistance ($\Omega/\square$) of the AlGaN/GaN heterostructure between the two ohmic

metal pads and L/W is the gap length/width.

Fig.5.3 (a) Schematic of the cross-sectional diagram of a linear TLM pattern and its equivalent circuit. (b) A typical layout of TLM patterns with different gap lengths.

The R_C' can be standardized by $R_C' = R_C / W$ and the equation 5.1 can thus be expressed as:

$$R_{total} = 2 \frac{R_C}{W} + R_{sh} \frac{L}{W} \quad (5.2)$$

Since R_{total} is directly proportional to gap length L , the value of R_C and R_{sh} can be obtained by using a group of TLM patterns with different gap lengths as shown in Fig. 5.3. (b). Therefore, the measured R_{total} as a function of L can be plotted and R_C and R_{sh} can be extracted:

$$R_C = \frac{\text{intercept}}{2} \times W \quad (5.3)$$

$$R_{sh} = \text{slope} \times W \quad (5.4)$$

The specific contact resistivity ρ_c can be calculated as

$$\rho_c = \frac{R_C^2}{R_{sh}} \quad (5.5)$$

The evaluation of contact resistance and sheet resistance is shown in Fig. 5.4.

The ohmic contact resistance for our devices in this work was measured to be $\sim 0.3 \, \Omega \cdot \text{mm}$ from the TLM pattern.

Fig.5.4 Evaluation of contact and sheet resistance from TLM structure.

3) Gate Dielectric Deposition

The ZrO_2 gate dielectric layer was deposited by a Cambridge Nanotech Savannah ALD system using tetrakis-(dimethylamido)-zirconium and H_2O as precursors. Before gate dielectric deposition, samples were treated by BOE solution to remove the surface native oxide. The chamber pressure and substrate temperature were 0.6 Torr and 250 °C, respectively. During the deposition,

sequential 400 ms and 40 ms pulses of H₂O and Zr sources were introduced into the chamber separately. After each pulse of gas, the chamber was purged with N₂ for 6 s to remove excess precursors and by-products from the reactor and substrate surface.

The dielectric constant k of the ALD-ZrO₂ was characterized by using a metal-insulator-metal (MIM) structure on the wafer. After determination of the dielectric thickness by ellipsometry, the dielectric constant k values were estimated to be in a range from 17 to 19 for ALD-ZrO₂, which is consistent with the values reported in literatures [27-29].

4) Gate Formation

The high work function gate metal (Ni/Au) was used to obtain high barrier height and hence to suppress the gate leakage current. After ALD growth of ZrO₂ gate dielectric layer, the contact mask aligner was used to pattern the gate and then Ni/Au with thickness of 50/400 nm was deposited with electron beam evaporation (E-beam) technique. The devices used for characterizations are with a gate length of $L_g=1.9\ \mu\text{m}$, a gate-to-source distance $L_{gs}\sim 0.9\ \mu\text{m}$, a gate-to-drain distance $L_{gd}\sim 1.5\ \mu\text{m}$, and a gate width of $W_g=2\times 100\ \mu\text{m}$.

5) Interconnect and Pad Formation

The interconnect is used for connecting and the pad is designed for characterization usage. The interconnect and pad were deposited using Ti/Au (50/300 nm).

5.4 C - V Characterization Technique for Gate Dielectric

The quality of interface between gate insulator and the semiconductor wafer is crucial for the AlGaIn/GaN MISHEMTs to achieve excellent and reliable performance. Many characterization techniques have been developed to evaluate the interfacial quality, including optical metrologies, such as SEM, TEM etc.; electrical metrologies, such as current-voltage (I - V), capacitance-voltage (C - V); temperature accelerated test and so on. Among these techniques, C - V measurement is the most commonly used due to its simplicity and reliability to evaluate the interfacial quality both qualitatively and quantitatively.

5.4.1 Basic MOS Capacitor C - V Behaviour

The MOS capacitor is the key for MOSFET transistors. Its C - V behavior, which is very similar to that of the GaN MISHEMTs introduced in this thesis, is briefly summarized here for better understanding of the operational mechanisms of GaN MISHEMTs. The MOS capacitor is a structure with the insertion of an oxide layer as the gate dielectric between a metal gate and a semiconductor substrate. The metal gate and semiconductor are the two plates of the capacitor.

Fig.5.5 Low frequency and high frequency capacitance-voltage (C - V) response of a typical n-type Si substrate MOS capacitor.

One of the most important characteristics of the MOS capacitor is its capacitance response with an applied DC voltage. Generally, the C - V response is obtained by the application of DC bias voltages on the capacitor while making the measurements with an AC signal. The DC voltage sweep can drive the MOS capacitor into three mainly regions: accumulation, depletion and inversion. A typical C - V curve of an n-type Si substrate MOS capacitor is shown in Fig.5.5. The blue curve marked as C_{HF} is the C - V response measured under high frequency while the red curve named as C_{QS} indicates the measurement conducted in quasistatic condition (low frequency). The quasistatic measurement is always taken under a very low frequency which is almost DC. More details of these three operational modes of MOS capacitor are summarized below.

Accumulation: As indicated in Fig.5.6. (a), when a positive voltage ($V_G > 0$) is applied at the gate, the majority carriers (electrons for n-type substrate) will be attracted to the oxide-semiconductor interface. Under this gate bias, the energy band is downward bended near the interface and the conduction band edge is very close to the Fermi-level. A high concentration of electrons are located near the oxide-semiconductor interface and this is called as the accumulation. The oxide capacitance is generally measured in the strong accumulation region.

Depletion: As shown in Fig.5.6 (b), when the gate voltage is swept from the positive value to a small negative voltage ($V_G < 0$), the energy band at the interface is gradually upward bended and the majority carriers (electrons) are depleted. For the depleted area, it can no longer conduct charges. The total measured capacitance in depletion region is the series of the gate oxide capacitance and the depletion layer capacitance. As a more negative gate voltage applied, the depletion region width will increase, which will lead to the decrease of gate capacitance as illustrated in Fig.5.5.

Inversion: As illustrated in Fig.5.6 (c), when a more negative voltage ($V_G \ll 0$) is applied, the upward bending of the energy band becomes more obvious. When the intrinsic level at the surface crosses over the Fermi-level, the number of minority carrier (holes) will exceed that of majority carrier (electrons) and the MOS capacitor is then working in the inversion region. Initially, the hole concentration is small and only a weak inversion is formed. However, with the further upward bending of the band, the onset of strong inversion will occur

when the hole concentration near the interface become equal to the substrate electron doping level.

Fig.5.6 The energy band diagram of a typical n-type semiconductor capacitance at three different regions: (a) accumulation, (b) depletion and (c) inversion. E_C is the conduction band, E_F is the Fermi level, E_i is the intrinsic energy level and E_V is the valence band.

An important point needed to emphasis here is that the behavior of the MOS capacitor is different under high frequency and low frequency measurements. For the n-type substrate MOS structure, the minority carriers (holes) are generated by thermal excitation and thus a period of time is needed to form the inversion layer. As shown in Fig.5.5, for a high frequency signal, there is no sufficient time for the generation of inversion layer to occur and the measured capacitance is equal to the minimum of the depletion region capacitance (C_{min}). However, when the measurement frequency is low enough, the minority generation rate in the surface depletion region is faster than the voltage variation, then the inversion formation can follow the AC signal. As a result, the capacitance in strong inversion is that of oxide layer capacitance as shown in

Fig.5.5.

Fig.5.7 A typical C - V curve for n-type GaN-based MOS capacitors. The inversion layer cannot form even the C - V measurement is conducted under low frequency.

However, for GaN-based MOS capacitors, the C - V response is slightly different with that of Si. As indicated in Fig.5.7, when the gate bias on n-type GaN MOS capacitors sweep from high to low, the inversion layer cannot form even the measurement is conducted under low frequency. This behavior is mainly due to the very low generation rate of minority carriers for wide bandgap semiconductors [30,31].

5.4.2 Basic Theory of GaN-based MIS Heterostructure

Capacitance

Fig.5.8 The schematic and equivalent circuit of a MIS diode: (a) the top view of the layout for a typical circular MIS diode; (b) the cross section and equivalent circuit element distribution; (c) the equivalent circuit topology.

The schematic and the equivalent circuit of a MIS diode with AlGaN/GaN heterostructure are indicated in Fig.5.8. Fig.5.8 shows (a) the top view of the layout for a typical circular MIS diode, (b) its cross section and equivalent circuit element distribution and (c) its equivalent circuit topology. Only the traps located at the interface between gate insulator and III-nitride

semiconductor will be discussed. The resistance R_s stands for the series resistance from the ohmic contact to the channel below gate through the access region between the source and gate electrodes. The resistance R_t shows the effect of the gate leakage current through the gate to the channel. C_{IN} represents the capacitance of the gate insulator. C_b accounts for the capacitance of the barrier layer (here the term “barrier” may also include the possible cap layer). C_d represents the capacitance of the channel depletion region. The C_{it} and R_{it} in series describe the capacitance effect of the traps located at the interface between the gate insulator and III-nitride semiconductor materials. With the change of gate bias, the number of trapped electrons at the interface states varies, thus an effective capacitor C_{it} is formed. The R_{it} together with C_{it} can describe the time delay (τ) required for the electrons trapped at the interface to reach equilibrium with those in the channel, and C_{it} which is related to the trap density (D_{it}) can be expressed as [32]:

$$\begin{cases} \tau = R_{it} C_{it} \\ D_{it} = \frac{C_{it}}{qA} \end{cases} \quad (5.6)$$

where A is the area of the gate.

5.4.3 Thickness/Permittivity Measurement of the Gate Insulator by C-V Technique

If the diode gate leakage current is negligible, the value of R_t will be extremely large. On the other hand, when the gate bias is oscillating at a very high

frequency that the emission and capture of the electrons in the interface traps cannot catch up with the change of the gate bias, then the effect of C_{it} and R_{it} can be ignored. Furthermore, when the device is working in the accumulation region, C_d is not plausible anymore. Based on these assumptions, the circuit shown in Fig.5.8 (c) can be simplified into Fig.5.9 (a). Similarly, the equivalent circuit for the corresponding conventional Schottky diode can also be simplified into Fig. 5.8 (b). The equivalent measured circuit through C - V measurement is assumed to be that showed in Fig.5.9 (c).

Fig.5.9 (a) Simplified circuit of Fig. 5.7 (c); (b) Simplified circuit of the conventional Schottky diode and (c) Measured circuit by C - V measurements.

The C_m and G_m shown in Fig.5.9 (c) are the values of capacitance and conductance directly measured by the C - V equipment. The series resistance R_s can be determined by biasing the diode into accumulation region according to:

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad (5.7)$$

The effect of R_s on the measured capacitance and conductance can thus be excluded by:

$$\begin{cases} C_m' = \frac{C_m}{(1 - G_m R_s)^2 + (\omega C_m R_s)^2} \\ G_m' = \frac{\omega^2 R_s C_m C_m' - G_m}{R_s G_m - 1} \end{cases} \quad (5.8)$$

For conventional Schottky (SB) diode ($C_m' = C_{HEMT}$):

$$C_{HEMT} = C_b \quad (5.9)$$

For MIS diode ($C_m' = C_{MISHEMT}$):

$$\frac{1}{C_{MISHEMT}} = \frac{1}{C_{IN}} + \frac{1}{C_b} \quad (5.10)$$

C_{IN} can thus be calculated from the measured overall capacitance for the corresponding MIS diode ($C_{MISHEMT}$) and conventional Schottky diode (C_{HEMT}):

$$C_{IN} = \frac{1}{\left(\frac{1}{C_{MISHEMT}} - \frac{1}{C_{HEMT}}\right)} \quad (5.11)$$

In general, C_{IN} is related to dielectric constant k and thickness of the gate dielectric layer d by the following expression:

$$C_{IN} = \frac{Ak}{d} \quad (5.12)$$

where A is the area of the diode gate.

Fig.5.10 High frequency (at 1 MHz) C - V characteristics of SB and ALD-ZrO₂ AlGaIn/GaN MIS diodes after R_s is subtracted.

Therefore, if one of the values between k and d is determined, the left one can be calculated by using equation 5.12. Through the capacitance measurement of MIM structures as described in Chapter 5.3, the k value of 18 is estimated. In order to have a comparison between MIS and SB diodes, GaN HEMTs with Schottky barrier were also fabricated for reference. Capacitance-Voltage (C - V) characteristics of SB and ZrO₂ MIS diodes measured at 1 MHz are plotted in Fig.5.10. At zero gate voltage bias (accumulation region), $C_{\text{MISHEMT}}=3.38 \times 10^{-7}$ F/cm² and $C_{\text{HEMT}}=4.28 \times 10^{-7}$ F/cm². Taking k as 18, the thickness of insulator

layer is calculated as 9.9 nm, which is in good agreement with the designed thickness (10 nm).

5.4.4 Evaluation of Interface Quality of AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as Gate Dielectric by C - V Technique

If a large amount of electronic states existed at the interface between ZrO₂ and AlGaIn/GaN HEMT substrates, the transition region of the measured C - V will be broadened when the gate voltage sweeps from the accumulation region to the depletion region, which is rather similar to the case of Si MOS diodes. For a trap-free AlGaIn/GaN MIS diode, when the gate voltage is ramped down from a high gate bias to a point lower than the threshold voltage V_{th} , the channel will be turned off and $C_{MISHEMT}$ will sharply decrease to a small value nearly close to zero. However, when a large amount of interface traps exist at the interface between the gate dielectric layer and the III-nitride semiconductor, the traps will capture or emit electrons when gate bias changes. These trap charge variations will cause the change of threshold voltage V_{th} . When reflected on the C - V curves, the trapped charge will lead to a broader transition from the depletion to the accumulation region. Thus, the degree of the sharpness for this transition in the C - V curve can be used to roughly judge the interfacial quality of the gate insulators on III-nitride semiconductors. As can be seen from Fig.5.10, the transition region from depletion to accumulation of the C - V curve is rather

sharp for AlGaIn/GaN MIS diode with ALD-ZrO₂ as the gate dielectric, which indicates good interfacial quality for ALD-ZrO₂ on AlGaIn/GaN HEMT substrates (with small amounts of traps inside the oxide and/or at the interface).

Fig.5.11 C - V curves of AlGaIn/GaN MIS structures on Si with ALD-ZrO₂ as gate dielectric measured at high frequency (1 MHz) and low frequency (10 kHz).

Another simple technique to directly evaluate the quality of the thin dielectric films on III-nitride semiconductors is the comparison between high and low frequency C - V measurements. At a rather low frequency, the electrons at the interface states have sufficient time to reach equilibrium through electron exchange with electrons at the conduction band in the channel, and hence C_{it} will be added to the measured overall capacitance C_m . As a result, the measured overall capacitance at low frequency will be larger than the one measured at

high frequency, and the differences varies with the electrical potential at the interface, which relies on the gate bias. Fig 5.11 plots the $C-V$ curves for AlGaIn/GaN MIS structure with ALD-ZrO₂ as gate dielectric measured at high frequency (1 MHz) and low frequency (10 kHz). As can be seen from Fig.5.11, the difference between these two curves at high and low frequencies is rather small. This may further indicate good quality of ALD-ZrO₂ on III-nitride semiconductors.

Fig.5.12 Simplified equivalent circuit of a MIS diode for interface trap density calculation by “Hi-Lo frequency” method.

Above-mentioned two techniques can be only employed for qualitative evaluation of the quality of the deposited ZrO₂ thin films on III-nitride semiconductors. However, “Hi-Lo frequency” method [33,34] and AC conductance method [35] are the two commonly used simple methods to

quantitatively determine the interface trap density (D_{it}). Although these two methods can only estimate interfacial trap density within limited energy range, they are still widely utilized for interfacial trap density calculation for GaN MISHEMTs due to its simplicity and easy availability for laboratory measurements. Thus, these two methods are utilized in this work for the determination of interfacial trap density D_{it} of ZrO_2 GaN MISHEMTs.

As discussed, information of trap effects can be extracted from the difference between the measured overall capacitance at high and low frequencies. The simplified equivalent circuit of a MIS diode for the calculation of interface state density by “Hi-Lo frequency” method is shown in Fig.5.12. The interface state density can be calculated as [34]:

$$D_{it} = \frac{C_{LF} - C_{HF}}{q(1 - \frac{C_{LF}}{C_{IN}})(1 - \frac{C_{HF}}{C_{IN}})} \quad (5.13)$$

where C_{LF} and C_{HF} are capacitance values at low (10 kHz) and high frequencies (1 MHz) after R_s subtraction from the measured capacitance values (C_m') of AlGaIn/GaN MIS diodes with ALD- ZrO_2 as gate dielectric.

The conductance, which represents the loss mechanism due to the capture and emission of carriers at the interface traps, is a good method to measure the interface trap density. AC conductance method is based on analyzing the loss which is caused by the change in the trap level charge state and thus is a sensitive method to determine trap density [35]. To further simplify the

analysis, the C_{IN} in the circuit of Fig.5.13 (a) can be subtracted and the part inside the dashed frame can be de-embedded. The C_b and C_d in series can be combined as one element C_d' . After Thevenin transformation, the circuit of Fig.5.13 (b) can be transferred into the one described in Fig.5.13 (c). With the measurement of the equivalent parallel conductance G_p of the MIS diode, which is a function of the bias voltage and frequency, the trap density can be estimated.

Fig.5.13 Simplified equivalent circuit of a MIS diode for interface trap density calculation by AC conductance method.

Assuming a continuum of trap energy levels, the equivalent parallel conductance G_p as a function of radial frequency can be described as:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad (5.14)$$

where τ_{it} is the trap state time constant and $\omega=2\pi f$ (f is measurement frequency) is the radial frequency. In equation 5.14, G_p/ω has a maximum at $\omega \approx 2/\tau_{it}$. Hence, D_{it} can be determined by the maximum G_p/ω and τ_{it} . Here, τ_{it} can be evaluated from ω at the peak conductance location on the ω -axis. Both the interface trap density D_{it} and trap level energy position E_T can be estimated as follows:

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{\max} \quad (5.15)$$

$$E_T = E - E_C = -kT \ln(\tau_{it} \sigma_T N_C v_t) \quad (5.16)$$

where k is the Boltzmann constant, T is the temperature and here $T=300$ K, σ_T is the capture cross section of the trap densities, N_C is the density of states in the conduction band, v_t is the average thermal velocity of the carriers.

However, the G_p determined by equation 5.14 is based on the parallel C_p - G_p equivalent circuit shown in Fig.5.13 (c), which ignores the effect of the gate insulator capacitance C_{IN} . A circuit comparison of Fig.5.12 (b) and Fig.5.13 (c) gives G_p/ω with respect to the measured capacitance C_m' (after R_s subtraction), the measured conductance G_m' (after R_s subtraction) and the insulator layer capacitance C_{IN} as

$$\frac{G_p}{\omega} = \frac{\omega G_m' C_{IN}^2}{G_m'^2 + \omega^2 (C_{IN} - C_m')^2} \quad (5.17)$$

Under different gate biases, the parallel conductance (G_p/ω) versus radial

frequency (ω) curves obtained from AlGaIn/GaN MIS diodes with ALD-ZrO₂ as gate dielectric are plotted in Fig.5.14. The solid lines are fitting curves for experimental $G_p(\omega)$ data and D_{it} and τ_{it} can be extracted from these fitting curves.

Fig.5.14 G_p/ω versus ω for AlGaIn/GaN MIS diodes with ALD-ZrO₂ as gate dielectric at different gate biases. The solid lines are fitting curves.

The extracted interface state density (D_{it}) as a function of their energy (E_T) for ZrO₂ MIS diodes determined by both “Hi-Lo frequency” and AC conductance methods are plotted in Fig.5.15. The trap level energy position E_T under different gate biases was evaluated by assuming $\sigma_T=3.4\times 10^{-15}$ cm²,

Fig.5.15 Extracted D_{it} as a function of energy obtained by “Hi-Lo frequency” method and AC conductance method conducted at room temperature from 10 kHz to 1 MHz for AlGaIn/GaN MIS diodes with ALD-ZrO₂ as gate dielectric.

$N_C = 4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$, and $v_t = 2.6 \times 10^7 \text{ cm/s}$ [36]. However, due to the limitation of given frequency range (10 kHz to 1 MHz) and with the measurements only conducted at room temperature, the range of E_T is limited from -0.29 eV to -0.36 eV. The reduction of the D_{it} value from $\sim 4 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ at energy of -0.29 eV to $\sim 7 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ at E_T of -0.38 eV was observed by AC conductance method as shown in Fig.5.15. Similar to the results extracted by AC conductance method, D_{it} decreased from $\sim 3 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ to $\sim 1 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ in the same energy range was determined by “Hi-Lo frequency”

method. When compared with interface state density determined by AC conductance measurements for AlGaN/GaN MIS structures with 10 nm thick ALD-Al₂O₃ as gate dielectric reported by Gregušová [37], our result is slightly lower in the similar energy range. This may indicate good interfacial property of the ALD-ZrO₂ on nitride-based semiconductor surfaces.

5.5 DC Characteristics of AlGaN/GaN MISHEMTs on Si with ALD-ZrO₂ as Gate Dielectric

Fig.5.16 (a) shows I_{DS} - V_{DS} curves of AlGaN/GaN MISHEMTs on Si with ZrO₂ as gate dielectric and Fig.5.16 (b) compares the DC transfer characteristics of ZrO₂ GaN MISHEMTs and referenced Schottky Barrier (SB) HEMTs. The drop in drain current for higher drain and gate bias can be attributed to self-thermal effect. It is evident that MISHEMTs with 10 nm thick ZrO₂ insulator can work at a high positive gate voltage of +5 V while still maintaining a low gate leakage current. The ZrO₂ MISHEMTs exhibited higher maximum drain current densities (I_{dmax}) of 790 mA/mm as compared to the referenced SB-HEMTs (I_{dmax} =638 mA/mm). As expected, the ZrO₂ MISHEMTs showed a shift of threshold voltage (V_{TMIS} = -3.9 V) with a slight reduction of the maximum extrinsic transconductance (g_{mmax} =138 mS/mm) as compared with those for SB-HEMTs (V_{TSB} = -3.0 V and g_{mmax} =146 mS/mm). The gate-to-channel modulation ability was slightly reduced due to the insertion of the high- k ZrO₂ insulator, which results in the shift of threshold voltage and smaller g_{mmax} [28].

If the change of the flat band voltage and the pinning of the Fermi-level at the interface can be ignored, the change of threshold voltage ΔV_{th} due to the insertion of high- k dielectric can be written as [29]:

Fig.5.16 (a) I_{DS} - V_{DS} characteristics for AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric. (b) Comparison of transfer curves between AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric and referenced AlGaIn/GaN SB-HEMTs.

$$\Delta V_{th} = \frac{V_{TSB} \times d_{ox} \times \epsilon_B}{d_B \times \epsilon_{ox}}, \quad (5.18)$$

where V_{TSB} is the threshold voltage for the AlGaIn/GaN SB-HEMTs without

using high- k dielectric, d_B , d_{ox} , ϵ_B and ϵ_{ox} are thickness and dielectric constant for the barrier layer (here term “barrier layer” may also include possible cap layer) and dielectric layer, respectively. Taking d_B , ϵ_B and ϵ_{ox} as 20.5 nm, 9 and 18 respectively, a ΔV_{th} of ~ 0.8 V was roughly estimated, which is very close to the value we obtained. This may further confirm good interface quality between the ALD-ZrO₂ insulating layer and the surface of nitride-based semiconductors. Fig.5.17 shows the transfer characteristics of AlGaIn/GaN MISHEMT with ALD-ZrO₂ as gate dielectric at $V_{DS}=8$ V and $V_{DS}=1$ V in semi-log scale. I_{ON}/I_{OFF} ratio $\sim 10^6$ at $V_{DS}=8$ V were obtained.

Fig.5.17 Transfer characteristics of AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric at $V_{DS}=8$ V and $V_{DS}=1$ V plotted in semi-log scale.

Gate I - V characteristics for ZrO₂ MISHEMTs and referenced SB-HEMTs are shown in Fig.5.18. Large reduction in the reverse gate leakage currents at $V_g=-$

Fig.5.18 Gate I - V characteristics of AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric and referenced SB-HEMTs.

10 V of MISHEMTs with 10 nm thick ZrO₂ as gate dielectric ($\sim 10^{-5}$ mA/mm) by four orders of magnitude as comparison to the referenced SB-HEMTs ($\sim 10^{-1}$ mA/mm) were observed. More importantly, a forward gate bias voltage as high as 7.4 V can be reached if we define the limit of the gate leakage current at 1 mA/mm. This gives the oxide electrical strength of ~ 7.4 MV/cm, which is the highest value achieved for ZrO₂ on GaN-based HEMTs so far. The high forward gate bias voltage allows for higher input voltage swing to be applied at the gate. Table 5.2 compares the key parameters of GaN-based MISHEMTs using ZrO₂ as the gate dielectric in literature with those measured results from our devices. It can be seen that the usage of 10 nm thick ALD-ZrO₂ insulating layer has the advantage to both reduction of gate leakage current and increment of forward

input gate voltage to 7.4 V while still maintaining a reasonable g_{mmax} value.

Table 5.2 Comparison of key parameters of GaN-based MISHEMTs with ZrO_2 as gate dielectric.

T_{ox} (nm)	Deposition method	L_g (μm)	g_{mmax} (mS/mm)	Magnitude of reduction for $I_{\text{g-leakage}}$ ($V_g = -10$ V)	Forward V_g at $I_g = 1$ mA/mm (V)	E_{ox} (MV/cm)	
10	E-beam	1	96.74	1 order	3	N.A	[28]
10.5 -11	ALD	2	N.A	3 orders	≥ 2	N.A	[39]
10	ALD	1	140	N.A	~ 6	N.A	[40]
10	MOCVD	2	110	4 orders	4	4	[29]
30	E-beam	2	140	4 orders	N.A	7.15	[38]
10	ALD	1.9	138	4 orders	7.4	7.4	this work

Summary

AlGaIn/GaN MISHEMTs on high-resistivity Si substrate using 10 nm thick ALD- ZrO_2 as gate dielectric were demonstrated in this chapter. The devices with $L_g = 1.9 \mu\text{m}$ showed g_{mmax} of 138 mS/mm and I_{dmax} of 790 mA/mm at $V_g = +5$ V. Compared with conventional AlGaIn/GaN SB-HEMTs, AlGaIn/GaN MISHEMTs with ALD- ZrO_2 as gate dielectric showed a reduction of reverse gate leakage current by four orders of magnitude with significant improvement of gate forward bias voltage (> 7.4 V). Low interface trap density (D_{it}) in the range of $7 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ to $4 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ obtained by using AC conductance and “Hi-Lo frequency” methods suggests good interface quality

between ALD-ZrO₂ and nitride-based semiconductors interface.

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Chapter 6

Conclusions and Recommendations for Future Work

6.1 Conclusions

In this thesis, the use of ALD-ZrO₂ as gate insulator and passivation layer for GaN MISHEMTs is studied. Two key areas for the implementation of ZrO₂ in GaN MISHEMTs as gate dielectric, namely band alignment and interfacial properties between ZrO₂ and GaN, are investigated. The main contributions of this thesis are summarized below.

The band alignment between ZrO₂ and GaN was experimentally investigated. Using angle-resolved XPS measurements combined with numerical calculations, valence band discontinuity ΔE_V of 1 eV and conduction band discontinuity ΔE_C of 1.2 eV at ZrO₂/GaN interface were determined by taking into account of GaN surface band bending and gradient potential in ZrO₂ layer. The results suggest that ZrO₂ is a good high- k insulator with sufficient energy barrier for both p and n-type carriers in GaN-based devices.

The device fabrication process, such as surface pre-treatment before ALD deposition and post-deposition annealing, has great influences on the interfacial chemical bonding states between ALD-ZrO₂ and GaN-based semiconductors.

The effectiveness of BOE pre-treatment on the formation of interfacial oxide layer between the ALD-ZrO₂ and AlGa_{0.5}N were evaluated. Owing to high reactivity of Al atoms, more prominent oxidation of Al atoms is observed, which results in thicker interfacial layer formed on BOE treated surface. Furthermore, for AlGa_{0.5}N, the presence of the native oxide at the surface may serve as a protecting layer to inhibit the surface from further parasitic oxidization during ALD deposition process, which results in a much thinner interfacial oxide layer with better interface quality. The widely used BOE surface pre-treatment process prior to ALD may not be favorable for ZrO₂/AlGa_{0.5}N interface.

The effect of post-deposition annealing in N₂ on interfacial chemical bonding states for ALD-ZrO₂ on GaN and Al_{0.5}Ga_{0.5}N was analyzed by XPS and HR-TEM. The formation/annihilation of the interfacial oxide layer is highly relied on the annealing temperatures. With the increment of temperatures to 500 °C, interfacial quality is improved with the annihilation of the interfacial oxide layer, which could be ascribed to the “clean up” effect of ALD-ZrO₂ on GaN-based semiconductors. However, for AlGa_{0.5}N, higher effectiveness of the passivation of Al-O bond than Ga-O bond through the “clean up” effect near the interface is observed. On the other hand, deterioration of the interface quality owing to the re-growth of interfacial layer at higher annealing temperatures is also found. Due to higher reactivity of Al atoms, Al atoms are easier to be oxidized when compared to Ga atoms.

The results in this work provide important process guidelines for the utilization of ALD-ZrO₂ as high- k gate insulator and passivation layer for AlGaIn/GaN HEMTs.

Finally, AlGaIn/GaN MISHEMTs on high-resistivity Si substrate using 10 nm thick ALD-ZrO₂ as gate insulator and passivation layer were demonstrated. The devices with $L_g=1.9\ \mu\text{m}$ showed g_{mmax} of 138 mS/mm and I_{dmax} of 790 mA/mm at $V_g=+5\ \text{V}$. Compared with conventional AlGaIn/GaN SB-HEMTs, AlGaIn/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric showed a reduction of reverse gate leakage current by four orders of magnitude with significant improvement of gate forward bias voltage ($>7.4\ \text{V}$). Low interface trap density (D_{it}) in the range of $7\times 10^{10}\ \text{cm}^{-2}\cdot\text{eV}^{-1}$ to $4\times 10^{11}\ \text{cm}^{-2}\cdot\text{eV}^{-1}$ obtained by using AC conductance and “Hi-Lo frequency” methods suggests high interface quality between ALD-ZrO₂ and GaN-based semiconductor interface.

6.2 Recommendations for Future Work

(1) Although the excellent electrical performance has been achieved for AlGaIn/GaN MISHEMTs utilizing a thin layer of ALD-ZrO₂ as gate insulator and passivation layer in this thesis, there is still much room for the further improvements. More optimizations can be applied to further improve the quality of the ALD-ZrO₂ gate dielectric, such as lower fixed charge density, higher interface stability, higher crystallization temperature and larger dielectric

constant. On the other hand, additional surface pre-treatments, including utilization of plasma pre-treatment [1-4] and sulfur passivation [5] to remove or passivate the unintentional and uncontrollable native oxide layer, can also be utilized to further improve the interface quality.

(2) Although ALD-ZrO₂ has been demonstrated as an excellent high-*k* material for AlGaIn/GaN MISHEMTs, there are still some problems needed to be solved before the widely usage of GaN MISHEMTs with ZrO₂ as gate dielectric for power amplifier and RF circuit. Among these problems, device reliability like stress issue and surface roughness is a rather important consideration. Reliability measurements, such as thermal stress, DC and RF stress and high-temperature characterizations can be applied to further understand the device reliability mechanisms behind. In addition, advanced device structure can also be utilized to further improve device performance and reliability.

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List of Publications

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1. G. Ye, H. Wang and R. Ji, "Band alignment between 4H-SiC and atomic-layer-deposited ZrO₂ determined by X-ray photoelectron spectroscopy," *Applied Physics Express*, Vol. 8, pp. 091302-1-091302-3, Sep. 2015.
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1. Y. Li, G. I. Ng, S. Arulkumaran, C. M. Manoj Kumar, K. S. Ang, H. Wang, G. Ye, R. Hofstetter, M. J. Anand, “Investigations of CMOS-Compatible Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contact for AlGa_N/Ga_N HEMT on Si with Low Contact Resistance”, *International Conference on Nitride Semiconductors*

(ICNS) 25-30 August 2013, U. S. A.

2. G. Ye, H. Wang, S. Arulkumaran, G. I. Ng, R. Hofstetter, Y. Li, M. J. Anand, K. S. Ang, Y. K. T. Maung, S. C. Foo, "AlGaIn/GaN MISHEMTs on Silicon Using Atomic Layer Deposited ZrO₂ as Gate Dielectric," *71st Device Research Conference (DRC)* 23-26 June 2013, U. S. A.

Appendix A

A Generic Process Flow for AlGaN/GaN

MISHEMTs with ALD-ZrO₂ as Gate

Dielectric

This appendix shows a generic process flow for AlGaN/GaN MISHEMTs with ALD-ZrO₂ as gate dielectric. The whole fabrication process for MISHEMTs includes mainly five steps: mesa isolation, ohmic contact formation, gate dielectric deposition, gate formation and pad and interconnection metallization.

1. Mesa Isolation

Organic Cleaning

- (1) Clean by Acetone (10 minutes)
- (2) Clean by IPA (10 minutes)
- (3) Rinse by DI Water
- (4) Dry blow with Nitrogen
- (5) Dehydration baking on hot plate (105 °C, 5 minutes)

AZ 1518 Photoresist Coating

- (1) Wafer cooling down after dehydration baking (5 minutes)
- (2) Place wafer on spinner chuck (vacuum on)
- (3) AZ 1518 photoresist coating

(4) Spin (4000 rpm, 30 seconds)

(5) Soft baking on hot plate (105 °C, 45 seconds)

Exposure & Development

(1) Exposure by a UV-light (320 nm) contact mask aligner (hard contact mode, 28 seconds)

(2) Develop in CD-26 (45 seconds)

(3) Rinse by DI water

(4) Inspection (microscopy)

Plasma Descum

(1) Chamber pressure (200 mTorr)

(2) O₂ flow rate (20 sccm)

(3) RF power (30 W)

(4) Process time (90 seconds)

Mesa Etching by ICP

(1) BCl₃ flow rate (20 sccm)

(2) Cl₂ flow rate (10 sccm)

(3) RF power (50 W)

(4) ICP power (100 W)

(5) Chamber pressure (10 mTorr)

(6) Etch rate: ~13 nm/min

Removal of Residue Photoresist by Organic Cleaning

(1) Clean by Acetone (10 minutes)

(2) Clean by IPA (10 minutes)

(3) Rinse by DI water

(4) Dry blow with Nitrogen

2. Ohmic Contact Formation

Organic Cleaning

(1) Clean by Acetone (10 minutes)

(2) Clean by IPA (10 minutes)

(3) Rinse by DI Water

(4) Dry blow with Nitrogen

(5) Dehydration baking on hot plate (105 °C, 5 minutes)

AZ 5214 Photoresist Coating

(1) Wafer cooling down after dehydration baking (5 minutes)

(2) Place wafer on spinner chuck (vacuum on)

(3) AZ 5214 photoresist coating

(4) Spin (4000 rpm, 30 seconds)

(5) Soft baking on hot plate (105 °C, 1 minute)

Exposure & Development

(1) Exposure by a UV-light (320 nm) contact mask aligner (hard contact mode, 1.2 seconds)

(2) Post-exposure baking on hot plate (115 °C, 1 minute)

(3) Flood exposure by a UV-light (320 nm) contact mask aligner (28 seconds)

(4) Develop in CD-26 (45 seconds)

(5) Rinse by DI water

(6) Inspection (microscopy)

Plasma Descum

(1) Chamber pressure (200 mTorr)

(2) O₂ flow rate (20 sccm)

(3) RF power (30 W)

(4) Process time (90 seconds)

Surface Preparation

(1) Clean by BOE (30 seconds)

(2) Rinse by DI water

(3) Dry blow with Nitrogen

Metal Evaporation by E-beam

(1) Load wafer

(2) Chamber pressure ($< 10^{-6}$ Torr)

(3) Metal deposition

Metal layer	Thickness (nm)	Deposition Rate (Å/sec)
Ti	25	1
Al	200	1
Ni	40	1
Au	50	1

Liftoff

(1) Soak wafer into Acetone until metal peels off from the surface

(2) Rinse by IPA

- (3) Rinse by DI water
- (4) Dry blow with Nitrogen
- (5) Inspection (microscopy)

Annealing by RTP

- (1) Load wafer
- (2) Keep the flow of nitrogen into the chamber (10 minutes)
- (3) Ramp the temperature up to 825 °C in 1 minute
- (4) Anneal in Nitrogen atmosphere (825 °C, 30 seconds)
- (5) Chamber cooling down
- (6) Unload wafer
- (7) Ohmic contacts inspection (TLM pattern)

3. ZrO₂ Gate Dielectric Deposited by ALD

Organic Cleaning

- (1) Clean by Acetone (10 minutes)
- (2) Clean by IPA (10 minutes)
- (3) Rinse by DI Water
- (4) Dry blow with Nitrogen

Surface Preparation

- (1) Clean by BOE (30 seconds)
- (2) Rinse by DI water
- (3) Dry blow with Nitrogen

ZrO₂ Deposition

- (1) Load wafer
- (2) Chamber temperature (250 °C)
- (3) Chamber pressure (0.6 Torr)
- (4) Pulse of H₂O (400 milliseconds)
- (5) Purge with Nitrogen (6 seconds)
- (6) Pulse of Metalorganic source (40 milliseconds)
- (7) Purge with Nitrogen (6 seconds)
- (8) Repeat from (4) to (7) for 120 cycles
- (9) Unload wafer

4. Gate Deposition

Organic Cleaning

- (1) Clean by Acetone (10 minutes)
- (2) Clean by IPA (10 minutes)
- (3) Rinse by DI Water
- (4) Dry blow with Nitrogen
- (5) Dehydration baking on hot plate (105 °C, 5 minutes)

AZ 5214 Photoresist Coating

- (1) Wafer cooling down after dehydration baking (5 minutes)
- (2) Place wafer on spinner chuck (vacuum on)
- (3) AZ 5214 photoresist coating
- (4) Spin (4000 rpm, 30 seconds)
- (5) Soft baking on hot plate (105 °C, 1 minute)

Exposure & Development

- (1) Exposure by a UV-light (320 nm) contact mask aligner (hard contact mode, 1.2 seconds)
- (2) Post-exposure baking on hot plate (115 °C, 1minute)
- (3) Flood exposure by a UV-light (320 nm) contact mask aligner (28 seconds)
- (4) Develop in CD-26 (45 seconds)
- (5) Rinse by DI water
- (6) Inspection (microscopy)

Plasma Descum

- (1) Chamber pressure (200 mTorr)
- (2) O₂ flow rate (20 sccm)
- (3) RF power (30 W)
- (4) Process time (90 seconds)

Metal Evaporation by E-beam

- (1) Load wafer
- (2) Chamber pressure ($<10^{-6}$ Torr)
- (3) Metal Deposition

Metal layer	Thickness (nm)	Deposition Rate (Å/sec)
Ni	50	1
Au	400	1

Liftoff

- (1) Soak wafer into Acetone until metal peels off from the surface
- (2) Rinse by IPA

- (3) Rinse by DI water
- (4) Dry blow with Nitrogen
- (5) Inspection (microscopy)

5. Pad and Interconnection Metallization

5.1 ZrO₂ RIE Etching to Open Window for Pad and Interconnect

Organic Cleaning

- (1) Clean by Acetone (10 minutes)
- (2) Clean by IPA (10 minutes)
- (3) Rinse by DI Water
- (4) Dry blow with Nitrogen
- (5) Dehydration baking on hot plate (105 °C, 5 minutes)

AZ 5214 Photoresist Coating

- (1) Wafer cooling down after dehydration baking (5 minutes)
- (2) Put wafer on spinner chuck (vacuum on)
- (3) AZ 5214 photoresist coating
- (4) Spin (4000 rpm, 30 seconds)
- (5) Soft baking on hot plate (105 °C, 1 minute)

Exposure & Development

- (1) Exposure by a UV-light (320 nm) contact mask aligner (hard contact mode, 1.2 seconds)
- (2) Post-exposure baking on hot plate (115 °C, 1 minute)
- (3) Flood exposure by a UV-light (320 nm) contact mask aligner (28 seconds)

(4) Develop in CD-26 (45 seconds)

(5) Rinse by DI water

(6) Inspection (microscopy)

Plasma Descum

(1) Chamber pressure (200 mTorr)

(2) O₂ flow rate (20 sccm)

(3) RF power (30 W)

(4) Process time (90 seconds)

ZrO₂ RIE Etching

(1) BCl₃ flow rate (20 sccm)

(2) Cl₂ flow rate (10 sccm)

(3) RF power (50 W)

(4) Chamber pressure (10 mTorr)

(5) Etch rate: ~5 nm/min

Removal of Residue Photoresist by Organic Cleaning

(1) Clean by Acetone (10 minutes)

(2) Clean by IPA (10 minutes)

(3) Rinse by DI water

(4) Dry blow with Nitrogen

5.2 Pad and Interconnection Deposition

Organic Cleaning

(1) Clean by Acetone (10 minutes)

(2) Clean by IPA (10 minutes)

(3) Rinse by DI Water

(4) Dry blow with Nitrogen

(5) Dehydration baking on hot plate (105 °C, 5 minutes)

AZ 5214 Photoresist Coating

(1) Wafer cooling down after dehydration baking (5 minutes)

(2) Put wafer on spinner chuck (vacuum on)

(3) AZ 5214 photoresist coating

(4) Spin (4000 rpm, 30 seconds)

(5) Soft baking on hot plate (105 °C, 1 minute)

Exposure & Development

(1) Exposure by a UV-light (320 nm) contact mask aligner (hard contact mode, 1.2 seconds)

(2) Post-exposure baking on hot plate (115 °C, 1 minute)

(3) Flood exposure by a UV-light (320 nm) contact mask aligner (28 seconds)

(4) Develop in CD-26 (45 seconds)

(5) Rinse by DI water

(6) Inspection (microscopy)

Plasma Descum

(1) Chamber pressure (200 mTorr)

(2) O₂ flow rate (20 sccm)

(3) RF power (30 W)

(4) Process time (90 seconds)

Metal Evaporation by E-beam

- (1) Load wafer
- (2) Chamber pressure ($<10^{-6}$ Torr)
- (3) Metal deposition

Metal layer	Thickness (nm)	Deposition Rate ($\text{\AA}/\text{sec}$)
Ti	50	1
Au	300	1

Liftoff

- (1) Soak wafer into Acetone until metal peels off from the surface
- (2) Rinse by IPA
- (3) Rinse by DI water
- (4) Dry blow with Nitrogen
- (5) Inspection (microscopy)