Design, analysis and development of tank-less, non-resonant and low-loss zero current switching inverter

Moreddy, Abhinava Chaitanya

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NANYANG
TECHNOLOGICAL
UNIVERSITY

**DESIGN, ANALYSIS AND DEVELOPMENT OF
TANK-LESS, NON-RESONANT AND LOW-
LOSS ZERO CURRENT SWITCHING INVERTER**

ABHINAVA CHAITANYA MOREDDY

**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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Design, Analysis and Development of Tank-Less, Non-Resonant and Low-Loss Zero Current Switching Inverter

Abhinava Chaitanya Moreddy

School of Electrical and Electronic Engineering

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Dedication

To my Father and Mother,

Janardhan Reddy and Amaravathi Moreddy,

To my Brother

Kranthi Ranadheer Moreddy,

And

All of my friends & family,

For their constant love and support

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List of Acronyms

AC	Alternating Current
ATC	Advanced Technology Centre
BOS	Balance of System
CPP	Controlled Pitch Propellers
DC	Direct Current
DC	Direct Current
DP	Drill Pipe
EMF	Electro Magnetic Force
EMI	Electro Magnetic Interference
EV	Electric Vehicle
FOC	Field Oriented Control
HEV	Hybrid Electric Vehicle
HFAC	High Frequency Alternating Current
HVAC	Heating Ventilation and Air Conditioning
IGBT	Insulated Gate Bi-Polar Transistors
IGCT	Integrated Gate Commutating Thyristors
LRC	Load-Resonant Converters
MILHDBK217F	Military Handbook for Electrical Installations
MPA	Maritime Port Authority of Singapore
MRC	Multi Resonant Converters
MTO	MOS Turn-off Thyristors
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
NEA	National Environmental Agency
NPC	Neutral Point Clamp
PRC	Parallel Resonant Converters
PV	Photo Voltaic

PWM	Pulse Width Modulation
QRC	Quasi Resonant Converters
QSC	Quasi Square Wave
RC	Resonant Converter
RDCLC	Resonant-DC-Link Converters
RMS	Root Mean Square
RR	Rolls-Royce PVT Ltd
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
ZCS	Zero Current Switching
ZCS- PWM	Zero Current Switching – Pulse Width Modulation
ZCSS	Zero-Current Switching Signal
ZVS	Zero Voltage Switching
ZVS-PWM	Zero Voltage Switching – Pulse Width Modulation
ZVT	Zero Voltage Transition

List of Symbols

λ_b'	Basic failure rate
π_E	Environmental factor
π_A	Circuit factor
π_S	Voltage stress factor
π_{SW}	Soft switching factor
π_C	Construction factor
π_T	Temperature factor
π_Q	Quality factor
μ_r	Repair rate
a_{00}, b_{mn}, a_{mn}	Fourier harmonic coefficients
a_{01}, a_{n1}, b_{n1}	Fourier Coefficients of I_{DC1}
a_{02}, a_{n2}, b_{n2}	Fourier Coefficients of I_{DC2}
a_{0n}, b_{0n}	Harmonic coefficients in $i_{pwm}(t)$
A_{11} - A_{12}	Inverter switches
A_{1PWM}	Gate signal to A_{11}
A_{21} - A_{22}	Partitioning cell switches
A_{2PWM}	Gate signal to A_{12}
$A_{PWM-1ph}$	Availability of 1-phase PWM Inverter
$A_{ZCS-1ph}$	Availability of 1-phase ZCS Inverter
$A_{ZCS-3ph}$	Availability of 3-phase ZCS Inverter
C_1	Input Filter Capacitor-1
C_2	Input Filter Capacitor-2
C_{DC1}, C_{DC2}	DC-Link Capacitors
C_f	Filter Capacitance
C_{gE}	Gate-emitter capacitance
C_p	Parasitic capacitance

C_r	Resonant Capacitance
C_{rp}	Parallel Capacitance
C_{rs}	Series Capacitance
C_s	Stray Capacitance
D_1	Diode-1
D_1, D_2, D_n	Diode Rectifier Units (Figure 3.1)
$D_{11}, D_{12}, D_{13}, D_{14}$	Diode Bridge rectifier of Inverter Cell-1 (INV1)
D_2	Diode-2
D_2	Diode-2
$D_{21}, D_{22}, D_{23}, D_{24}$	Diode Bridge rectifier of Inverter Cell-2 (INV2)
di/dt	Rate of change of Current Across the Inverter Switch
dV/dt	Rate of change of Voltage across the inverter switch
E_{CgE}	Energy stored in gate to emitter capacitance
E_{fall}	Energy loss incurred in fall time period during turn-off transition
E_{off}	Energy loss incurred during turn-off transition
E_{ON}	Device energy loss during ON-state
E_{sw}	Device energy loss during OFF-state
f_c	Carrier frequency/ Switching frequency
f_c	Carrier frequency
f_s	Fundamental frequency
f_{sw}	Switching frequency
f_t	Switching frequency of inverter cell switches
HS	Hard switching
i, j	Number of states
I_0	Initial load current
$I_0(\omega)$	Initial load current in frequency domain
I_A	Output line current of phase-A

I_d	D-axis current
I_{DC}	Rectified DC current (Figure 3.4)
I_{DC0}	Average current supplied by DC source
I_{DC1}	Input DC current to INV1 in Topology-2
I_{DC2}	Input DC current to INV2 in Topology-2
I_{dem}	Current pulse to the inverter switch
I_{IN}	Input inverter current
$I_L(t)$	Instantaneous load current
INV1	Inverter cell-1
INV2	Inverter cell-2
I_q	Q-axis current
I_{rr}	Reverse recovery current
I_{SW12}	Current Through the inverter cell switch T_{12}
I_T	Turn-off current
I_{T0}	Current through the device at t_0
I_{tl}	Tail current
k	Time Constant
k	curve fitting constant
K	Proportional Constant
L-A	Leg-A
L-B	Leg-B
L-C	Leg-C
L-D	Leg-D
L_E, R_E	Emitter Inductance and Resistance respectively
L_f	Filter Inductance
L_g, R_g	Gate Inductance and Resistance respectively
L_i	Input Line Inductance
L_r	Resonant Inductance

L_s, R_s	Source Inductance and Resistance respectively
L_{stray}	Stray Inductance (Integral Half Cycle Converters)
M	Induction Motor Load
m	Modulation Index
m_1, m_2	Modulation Indices of Inverter Cells INV1 and INV1 respectively
m_a	Amplitude Modulation Index
m_f	Frequency Modulation Index
$MTBF_{ZCS-3ph}$	Mean time between failures in 3-phase ZCS Inverter
N_m	Speed
p	Duty-Cycle Ratio of Current Through Inverter Switches
$P_{ij}^*(t)$	First derivative of probability of the state (i, j)
P_0	Probability in State 1
P_1	Probability in State 0
P_{cond}	Device conduction loss
$P_D(t)$	Probability of a degraded state
P_{fall}	Power loss incurred during fall time
PI	Proportional Integral
$P_{ij}(t)$	Failure rate probability of a particular state (i, j)
$P_j(t)$	Probability of a system in j^{th} state
P_{loss1}	Switching power loss in PWM inverter
P_{loss2}	Switching power loss in ZCS inverter
P_{off}	Power loss during turn-off time
$P_{\text{SW-Device}}$	Device switching power loss
Q_1	Semiconductor Switch/ MOSFET -1 (QRC)
Q_1, Q_2, Q_3	Gate signals to the inverter switches
Q_2	Semiconductor Switch/ MOSFET -2 (MRC)
Q_s	Switching State Matrix

$R(t)$	Total reliability
$R'_T()$	Reliability of conventional system
R_{Load}	Resistive Load
R_{N+X}	System reliability function for a parallel configuration
S_1	Gating Signal/Switching Function to Partitioning Cell Switch-1
$S_1(\omega)$	Gating signal to partitioning cell switch in frequency domain
S_2	Gating Signal to Partitioning Cell Switch-2
S_A	Switching Function of Switches in LEG-A
S_{A1}	Switching function of inverter switch A_{11}
$S_{A1}(\omega)$	Switching function of inverter switch A_{11} in frequency domain
S_B	Switching Function of Switches in LEG-B
S_C	Switching Function of Switches in LEG-C
S_D	Switching Function of Switches in LEG-D
s_i	Switching Functions of Partitioning Cell Switches 3-Phase Topology-2
s_{ij}	Switching Functions of Inverter Switches in 3-Phase Topology-2
SS	Soft switching
SW_1	Partitioning Cell Switch-1
SW_1	Partitioning Cell Switch corresponding to INV1
SW_1	Partitioning Cell Switch corresponding to INV2
$SW_1, SW_2, \dots SW_n$	Partitioning Cell Switches
SW_2	Partitioning Cell Switch-2
$S_x(t)$	Generalized harmonic function by SPWMs
T_0	Initial time
t_0, t_1, t_2, t_3	Time instants during turn-off transtition
T_1	Semiconductor Switch -1

$T_1, T_2, \dots, T_n$	Inverter Switches
$T_{11}, T_{12}, T_{13}, T_{14}$	Inverter Cell Switches in Single Phase Topology-1 and Topology-2 (INV1)
$T_{11}, T_{12}, T_{13}, T_{15}, T_{14}, T_{16}$	Inverter Cell Switches in 3-Phase Topology-2 (INV1)
T_2	Semiconductor Switch -2
$T_{21}, T_{22}, T_{23}, T_{24}$	Inverter Cell Switches in Single Phase Topology-1 and Topology-2 INV2
$T_{21}, T_{22}, T_{23}, T_{24}, T_{25}, T_{26}$	Inverter Cell Switches in 3-Phase Topology-2 (INV2)
T_3	Semiconductor Switch -3
T_4	Semiconductor Switch -4
T_5	Semiconductor Switch -5
T_6	Semiconductor Switch -6
T_c	Time Period of Partitioning Cell Switches
T_d	Duty ratio of Inverter cell Switches
T_d	Duty ratio
T_{ij}	Switches in 3-Phase Topology-2
$T_{on, PWM}$	Turn-On period of PWM signal
T_p	Time period
V_{1N}	Voltage Across Inverter Cell INV1 in 3-Phase Topology-2
V_{2N}	Voltage Across Inverter Cell INV2 in 3-Phase Topology-2
$V_{A1O}, V_{B1O}, V_{C1O}$	Output Phase Voltages of INV1
$V_{A2O}, V_{B2O}, V_{C2O}$	Output Phase Voltages of INV2
V_{AN}	Output Phase Voltage of Phase-A
V_{AN}	Output Line-Line Voltage of Phases A&B
V_{GE}	Gate to emitter voltage
V_{GG}	Gate signal

V_{GS}	Voltage across gate and source
V_{in}	Input Voltage
V_{LL}	Output Line to Line Voltage in Topology-2
V_{LL1}	Output Line to Line Voltage of INV1 in Topology-2
V_{LL1}	Load Line- Line RMS Voltage
V_{LL2}	Output Line to Line Voltage of INV2 in Topology-2
V_{ON}	Instantaneous Input side ON-State Voltage of ZCS Inverter
V_{ON}	ON-State voltage drop across the switching device
V_{PWM}	Voltage corresponding to On state of PWM signal
V_{si}	Voltage Matrix
V_{SW12}	Voltage Across the Inverter Cell Switch T_{12}
V_{TH}	Threshold voltage
δ_{ij}	Failure rate of partitioning cell switches (i, j)
θ_{cx}	Carrier phase angle
λ_i	Failure of i_{th} entity
λ_{ij}	Failure of inverter cells
λ_{ph}	Failure rate with hard switching
λ_{ps}	Failure rate with soft switching
$\lambda_{PWM-3ph}$	Failure rate of 3-phase PWM inverter
$\lambda_{ZCS-3ph}$	Failure rate of 3-phase ZCS inverter
τ	Decay constant
τ_g	Gate time constant
ω_{0n}	Angular frequency of n^{th} harmonic
ω_p	Angular frequency

Chapter 1 Introduction

This chapter, the fundamental aspects of the research work presented in this thesis are discussed. The motivation to pursue the research opportunities in the field of power electronics and the research objectives are highlighted. The chapter as well summarizes the organization of this thesis.

1.1 Background and Motivation

Due to the steep increase in oil prices, marine system designers are exploring energy efficient solutions through technological and operational advancements. From a customer perspective there is an increase in demand for modern amenities. With new demand devices being incorporated into ship system and on board space being limited, ship designers are faced with a tremendous challenge to find compact, efficient and cost effective solution bearing reliability in mind.

The move towards full electric and hybrid electric propulsion systems in the marine industry is attracting considerable interest due to the perceived advantages of reduced fuel consumption and emissions. Rolls Royce (RR), a global leader in the design and manufacturing of marine propulsion systems offers a range of individual items of equipment such as propellers, azimuth thrusters and engines, to complete integrated ship systems including configuration of electric and hybrid electric systems.

The electrical propulsion system architectures can be composed of several generators and motors systems, to transform mechanical to electrical power and vice versa. Here, variable speed drive systems are required to facilitate the transformation of power between the prime mover and the propulsion system.

Traditionally, marine industries employ thyristor based DC drive systems. Today, fuel cost and emission regulations are fiercely demanding the design and use of efficient electric power systems. One solution is the variable speed drive topology, which offers an improved system efficiency through improvement in the design of power factor (pf). Secondly, the

Figure 1.1 Proposed variable speed drive

input line filters that are employed on such variable speed drive can be large and bulky and therefore, may impact the system volume and weight constraints. This proposal investigates the design of the front-end rectifier to reduce the size and therefore weight of the passive components used by the input line filter. This is achievable by actively controlling the conduction angle of the three bi-directional power switches as depicted in Figure 1.1.

This research will explore the design and development of a novel inverter system. Note that a rear-end inverter is used for the switching characteristics for appropriate voltage frequency control. An advanced control strategy to be developed through this research program will drive the bi-directional switches which will reduce or even eliminate the requirement of the large input inductance (L_a , L_b , L_c in Figure 1.1), reduction in rear-end inverter power losses and improving reliability and availability by fault ride through with energy storage will result in significant cost savings. The major motivating factor of this project is the research on diversified and broader aspects of power electronic converters.

1.2 Research Objectives

The significance of the project will address three main issues through which new knowledge will be created:

a) Reducing the size of the input filter for front-end rectifier

One of the key problems in front-end rectifier of a variable speed drive is the requirement of large input filters to suppress the harmonics. Previous research activities by the NTU PI have demonstrated the proposed solution by actively controlling the conduction angle of the three bi-directional switches to reduce the harmonics and therefore the size of input line inductances. Note, to date, this concept has not been commercially demonstrated.

In this research, parallel structures will be considered, where multiple front-end converters will be connected in parallel configuration and cascaded in modular form. Interleaved modulation techniques will be studied herein for modulating the parallel front-end firing angle control unit. Interleaving technology has gained wide acceptance in DC/DC converter to reduce the size of inductors. However, it has not been demonstrated in a front-end converter application. Appropriate control methods will be developed to achieve the optimum performance from modular structures designed to reduce the input line inductor size.

b) Novel inverter configuration

The power electronic community has been relentlessly working on improving the efficiency of converter systems. But the true energy savings are realized by system level efficiency and redundancy. In many cases, the power electronic converter systems are more efficient than the system itself. This research focuses on introducing a new breed of inverter configurations suitable for transportation and drive applications where efficiency and reliability are of prime importance. Conventional inverter systems operating with PWM strategy have a significant utilization in drive systems. However, limitations in operational frequencies, harmonic influence, device power losses and EMI have provoked research for more optimized power conversion methods.

The research work presented herein will propose a novel inverter configuration with reduced power loss, improved reliability and higher cost savings.

c) Ride through of faults

Marine electric propulsion systems operate under steady state and dynamic conditions. A significant variation on the DC-link voltage can occur during transients resulting in system instability. Failure to ride through fault conditions may impact the performance of motor and introduce voltage sags and swells onto the utility network which can in turn affect other equipment's connected to network.

This research will address ride-through problems by introducing hybrid storage in the form of battery and super capacitor bank. The focus here will be given to modeling and control solutions for optimal sizing.

1.3 Research Collaboration

NTU and RR have an excellent research relationship and both parties are already involved in numerous collaborative research programmes. The Advanced Technology Centre (ATC) of RR Singapore is already engaged in marine R&T activities. This programme will assist to develop and demonstrate advanced technology for marine vessels, by bringing together the industrial and technical expertise of RR and the academic strength of NTU. The research goals are aligned and relevant to MPA and other industries.

1.4 Thesis Organization

In Chapter-1, an overview of power electronics from Singapore's perspective is explained. A general introduction to inverter markets in Singapore and around the world is presented. The forecasts suggest that as demand and need for more clean power increases, the inverter market would penetrate into deeper utility applications. The current inverter applications are limited to drives and solar converters. As the inverters are made more efficient, the cost of benefit ratio decreases, enabling many small scale and house hold consumers to install an inverter system for local renewable power generation setup. The current research work focuses on design and development of novel inverter configurations for marine and other drive applications.

In Chapter-2, a review of various soft switching converters is presented. Power electronic converters have made tremendous advancements over the past few decades. But the power

loss incurred by semi-conductor devices has been a major limitation in increasing the power level and frequency. Soft switching converters are well known for their zero current and zero voltage switching strategies. The advantages and drawbacks of various soft switching converters are highlighted. Limited load power range, passive elements, bulkiness, resonant frequency dependency, complexity, poor efficiency at lighter loads and circulating currents are few of the major limitations in soft switched converters. In order to address the above limitations while achieving the prime objectives of a soft switching converter, a novel inverter configuration with desired features such as zero current switching, reliable, no resonant tank and wide load range has to be designed and developed.

Chapter-3 introduces novel zero current switching, tank-less, non-resonant, modular and highly efficient inverter configurations. The various operational features and design considerations have been explained. The zero current switching feature of the inverter is well explained. One of the two proposed configurations is chosen for further research for its simplicity and ease of retrofit ability. The proposed ZCS inverter achieves zero current switching without the use of any resonant technique. It combines the advantages of PWM and soft switching strategies. The other advantages of the proposed ZCS inverter such as simplicity in architecture and control strategy, modularity and zero voltage switching are highlighted. The feasibility of the concept is demonstrated by experimental results.

Chapter-4 presents a comparative cost and power loss analysis between the proposed ZCS inverter and PWM inverter. Efficiency has always been the key factor for determining the inverter applicability. The proposed ZCS inverter incurs minimal switching loss due to its zero current switching features. The total power loss incurred in ZCS inverter is about 40% of that incurred in hard switched PWM at a similar operational frequency. The conduction losses tend to be higher in ZCS inverter due to the incorporation of more number of switches. But this increase is only in partitioning cells. The average conduction loss per switch in the ZCS inverter is much lower compared to PWM inverter. This reduces the amount of cooling requirements for the overall system. The cost comparative analysis shows that ZCS inverter is beneficial over long run. Though the initial capital costs are high, the ZCS inverter compensates and gains at operational costs due to lower device power losses. Around 35-40% reduction in overall costs is achieved. This is a significant reduction

considering basic costs. The ZCS inverter with its redundant architecture would result in greater economic savings when reliability aspects are evaluated for an economic case.

In Chapter-5, the reliability analysis for ZCS inverter is carried out with respect to conventional PWM inverter. Reliability is a corner stone for many modern day applications. With the increase in onboard utilities and complex systems, a highly reliable system with great redundancy is preferred for better operational and cost effectiveness. In power inverter the reliability as well depends on the configuration and characteristic operation of the inverter. Markov analysis considering system failure states is used to determine the reliability of ZCS inverter. The reliability analysis considering the parallel path conversion system is as well carried. The analysis has as well considered a basic practical system and their failure rates. The reliability analysis resulted in a lower failure rate of ZCS inverter. The failure rate of ZCS inverter is 35% of that of PWM inverter system. The soft switching nature and modular configuration of ZCS inverter are prime factors contributing to the improvement of reliability in ZCS inverter over conventional PWM inverters.

In Chapter-6, the effects of DC-link switching and dead-time in ZCS inverter are explained. DC-link switching analysis is carried out to investigate the effect of partitioning cells on DC-link. This analysis is important as the concept of partitioning cells is relatively novel and the key idea behind ZCS inverter's efficient operation. It is seen that the harmonic peak of DC-link capacitor input current is dependent the duty ratio of the partitioning cell switches. This interesting feature actually results in a reduction of input current harmonics by 20% compared to conventional PWM inverter input current harmonics. Moreover, the inherent delay in ZCS inverter which enables zero current switching operation as well contributed to reduction in peak harmonics. This is due to the non-availability of any load current and conduction paths during the rise and fall time transitions of the inverter switches.

Influence of dead-time has been one of the major draw backs of PWM inverter. A number of methods have been proposed to compensate for the effect of dead-time. The ZCS inverter has an inherent operational delay during switching transitions. This feature eliminates the need of an additional induced dead-time or delays to prevent shoot-through. ZCS inverter completely eliminates the need of dead-time circuit and the inherent delay does not cause any distortion in the load current waveform. The effect of dead-time is studied under the

operation of well-known control strategies such as FOC (Field Oriented Control) and Sensor less FOC. In either case, the ZCS inverter produces load current waveforms of lower THD and better quality.

In Chapter-7, the conclusions are drawn for the research work presented in this Ph.D. thesis. The future scope and research opportunities that lay beyond are well described.

The research work has unified various aspects of power electronics that are considered in the design and development of a novel power electronic converter. The original research work presented here in shows great potential to be applicable in inverter market for major transportation and renewable energy applications. The ZCS inverter addresses all major drawbacks of soft switching and PWM inverters by a unique novel yet a simple circuit configuration.

Chapter 2 Literature Review

A brief analysis about the trends and growth in the field of power electronics and drives is presented. Statistical results and global inverter market sales are as well presented. The role of power electronic converters in future ship systems is highlighted. Advantages and limitations of current marine power converters are listed. Research opportunities in future marine systems are explained and a review on most suitable power electronic converters for marine systems is presented.

2.1 Trends in Energy Consumption

The need for energy is ever increasing in 21st due to massive industrialization as more countries are economically empowered. Globally about 87% of the energy is generated by fossil fuels, about 6% from nuclear plants and 7% from renewable energy power systems. Due to rapid increase in production costs and fuel costs, energy efficiency has become a keynote index for any industrial operation. The oil prices have reached \$100 for the first time ever. An annual energy consumption recorded an increase of 2.5% [1]. The evident climate changes are forcing technology towards pursuing more sustainable solutions.

Advent of renewable energy has been tremendously increasing. The share of renewable energy production was up from 7.8% in 2012 to 8.2% in 2013. This is due to improved cost competitiveness, especially in PV and Wind [2]. A total of 39 GW of solar PV were installed in 2013. The steep fall in cost per kilowatt allows newer markets to compete without any subsidies. In Figure 2.1, the trends in renewable energy consumption are shown. As shown in Figure 2.1.b, the transportation sector is the highest consumer of fossil fuel energy.

The statistics and reports indicate that renewable energy market has surpassed all its expectations and major barriers in the past decade. However, the percentage of CO₂ has been constantly increasing (Figure 2.1.d). The two major factors affecting more renewable energy market penetration are policy/investment fluctuations and higher cost of supporting technologies. The utilization of highly efficient power electronics plays a major role in the

near future for reducing power generation from conventional fossil fuels and maximizing the conversion efficiency of renewable energy power systems.

Figure 2.1 Global Energy Consumption Trends [3]: (a) World energy consumption by end fuel type 1990-2035 (b) Energy Consumption by industry sector (c) Renewable energy generation (d) Global CO₂ emissions 1990-2035

2.2 Energy Consumption in Singapore

Figure 2.2 Energy Consumption Index in Singapore [3]: (a) Energy consumption by utility sectors in Singapore (b) Energy Consumption by household appliances (c) Power level of various industrial Loads

In Figure 2.2, annual energy consumption trends in Singapore are presented [4]. The industrial sector consumes more than any other sector. Propulsion Systems, Drives, Conveyor belts, Cargo cranes and many utilities incorporate motor drives. Amongst the consumer utilities, Air conditioners consume more power than any other utilities. Various performance indices and standards are set by National Environmental Agency (NEA) to improve the overall efficiency and reduce harsh effects on environment. The demand for PV inverter would increase as population becomes aware of increasing costs. Singapore belongs to “Sunbelt” region; hence, adequate amount of solar energy can be tapped. Even a slight improvement in efficiency in the above-mentioned systems would result in significant

amount of savings. An efficient inverter system with low loss and wide power range operation would be highly advantageous.

2.3 Power Electronics- Key Technology

“Sustainable development meets the need of present without compromising the ability of future generations to meet their needs [5]”. Energy efficiency as part of concept of sustainable earth is being urged on every sector to realize a sustainable society. The future electrical infrastructure would be a non-carbon based system. Power Electronics technology plays a key role in creating a sustainable system. Lately, due to the incorporation of renewable energy sources there has been a drastic turnaround in the design of power system infrastructure. Aerospace, Marine and EV power systems are heading towards a modular structure in order to increase reliability and decrease operational costs. Realizing the importance of clean energy many governments and public themselves are keen on installing a low power domestic power generation unit to cut down incurring costs. All these factors

Figure 2.3 Applications of Power Electronics [5]

vibrantly pronounce the need of having a highly efficient power electronic conversion system. Therefore, power electronics engineers are continuously challenged to understand the requirements beyond the fundamental theory. Power electronics suiting renewable energy stage are at a rapid advancement stage as shown in Figure 2.3 [5]. In case of renewable energy, like solar, wind and tidal the process of power generation and the process

of delivering power vary widely. For example, large numbers of inverters are utilized to deliver the power generated at a wind farm to the grid. This fundamental shift in generation and transmission poses a new challenge to design power electronic converters. In such case power electronic devices play a key role in overall reliability, stability and the power quality of the system.

High fossil fuel prices and stringent emission laws caused the transportation sector to switch from conventional vehicular systems to hybrid and electric vehicle systems (HEVs, EVs) rapidly. Various transportation sectors are increasingly being electrified in order to achieve high efficiency and low overall system cost. A highly efficient inverter system, as well as a battery system is one possible way to realize optimum and smart utilization of renewable and primary energy resources in transportation, industrial and other consumer applications.

2.4 Current Ship Propulsion Technologies and Trends

Electric propulsion with gas turbine and diesel engine has been implemented in numerous ships with large variety in configuration and type. At present electric propulsion is used in Cruise vessels, ferries, DP drilling vessels, thruster assisted moored floating production facilities, shuttle tankers, cable layers, pipe layers, icebreakers and other ice going vessels, supply vessels, and war ships [6, 7]. The on board energy demand is ever increasing. The current improvements to the system are resulting only in fractional benefits while the power demand is increasing at a rate of 10x and 100x. An *All Electric Ship* is envisaged as a solution to address the above limitations. The current ship technology is heading towards an integrated technology which brings the beneficial factors of conventional drive and electric propulsion system. An integrated power system combines propulsion and electric service into one highly coupled, dynamic, non-linear and discontinuous (switching) system.

As discussed earlier, the incorporation of VSIs would lead to significant energy savings. The major drawback of using power electronic converters is the need for filter. But replacement of conventional transformers with power electronic converters is highly advantageous as the problem of impedance matching and power conversion is solved. Usually the line filters take up 15-20% of the total volume occupied by the converter. To achieve filter size reduction, operating at higher frequency is one possible approach. But

this approach has limitations due to increased power loss, switching stress and higher EMI. In Figure 2.4 [8], trends in electrical architecture of ship are listed. The trend suggests a shift from ac to dc-power architecture. The incorporation of renewable energy, elimination of line filters, transformers, lower cost and copper per kW are prime reasons for such a magnanimous shift.

Figure 2.4 Trends in ship electrical architecture [8]

2.5 Global Inverter Technologies and Market

Current research focuses on building a highly efficient inverter system for marine applications and extends its application to various other renewable energy powered systems. In this context it is quite important to analyze the current inverter market and trending technologies with respect to power level and application.

As inverters are a part of a BOS (Balance of System) in any modern day drive or power generation setup, the need to have a highly efficient inverter is more than ever. As the discussions on energy related issues have become more and more important – electric mobility, renewable energy systems, transportation and electrification, as a direct result the demand for power electronic components has increased. The demand for inverters for various drive applications is increasing at a steady pace while the demand for renewable

Figure 2.5 Global inverter market [7]

inverters is increasing at an exponential rate. As population and more number of governments become aware about the harsh environmental effects of carbon emissions, the demand for renewable inverters is expected to increase even more. The global trends in all kinds of utility inverters is shown in Figure 2.5.

2.6 Marine Propulsion

There has been an exponential increase as shown in Figure 2.6 in growth of electric propulsion since 1995 [9]. The major reasons for such exponential increase are:

(a) Development of power electronics

The mass production of semi-conductor and high power components made way for high power AC/AC converters and thus eliminating the need of controlled pitch propellers (CPP).

(b) Electric podded propulsion

Maneuverability and greater zero speed torque (ice breaking capacity) made electric propulsion more favorable option especially in cruise liners and ice breakers.

(c) Offshore exploration

With the increase in offshore oil exploration opportunities, the demand for vessels that have significant advantages with electric propulsions and distribution as well increased.

(d) Oil Price

High oil prices and increasing operational costs have led ship designers to seek energy efficient and reliable solutions.

2.7 Power Electronics in Marine Systems

The rapid development of electric propulsion and auxiliary power systems has created more demand for on board power electronic equipment. The recent advances in construction of power electronic devices and converters have been the prime movers of advancements in marine electrical power systems.

2.7.1 Marine Power Converters

Early marine electrical propulsions systems were based on AC/AC converters (as in cycloconverters) with thyristors as switching devices. High efficiency is obtained as these devices commuted naturally by voltages obtained from either the supply side or back EMF. However, the thyristors are not space efficient and are limited by operational frequency, waveform quality and ease of control. And hence, current source converters and AC/AC converters are now being fast replaced by voltage source converters and IGBT's as switching devices.

Figure 2.6 Growth of electric propulsion over 1970- 2014 [8]

The major advantages of voltage converters are:

a) PWM operation

PWM switching strategies provide easy of control and high quality sinusoidal voltage to the load.

b) Switching devices

Insulated Gate Bi-Polar Transistors (IGBT) Devices, Integrated Gate Commutating Thyristors (IGCT) and MOS Turn-off Thyristors (MTO) are replacing traditional thyristors due to higher ratings, faster switching transition times and lower device power losses.

c) High power converter topologies

As the ratings of switching devices such as IGBT's is higher, the need to connect devices in series has been limited to a few very applications. Topologies such as Neutral Point Clamp (NPC) make 30MVA operation achievable. A major advantage of such topologies is the reduced voltage fluctuation at the voltage resulting in a near to sine voltage waveform. Such high power voltage clamped configurations eliminate the need to reduce the DC-link voltage (clamping voltage). This allows an extensive capacitor network forming many intermediate voltage levels. Sequential linking of these voltage levels by switching devices to loads results in a near to sine wave voltage waveform. However, the device switching losses and DC-link switching losses increase as number of operating voltage levels increase.

2.7.2 Limitations in Marine Power Converters

Though modern day power electronic converters bring in significant advantages to marine propulsion when compared to traditional thyristor based converters, their optimal utilization is limited by various factors briefly explained below:

a) Total Harmonic Distortion (THD)

The power conversion process in any power electronic converter happens through a definitive switching process. Switching by nature is discontinuous. This results in drawing discontinuous current from supply and thus creating voltage fluctuations at the load end. The drastic the voltage fluctuations are the more non-sinusoidal load voltages are. The DC side distortion, for example, is one of most common forms of distortion. Many harmonic

mitigation methods and harmonic filtration methods have been proposed [3, 10-13]. Conventional method of adding line inductors to connect propulsion system to power lines does mitigate distortion but occupies 60% of propulsion system space and adds more weight [14].

b) dV/dt

With higher power ratings and shorter switching transition times. The rate of change of voltage is immensely high. This voltage stress results in degradation of insulation in motors, or a potential failure. This as well limits the DC-link voltage. Output filters are usually used to reduce the rate of voltage change. Unlike the sinusoidal filters, the output filters are small and cost less.

c) Motor regeneration

Larger marine systems gain a lot of kinetic energy as they move. Hence in order maneuver, they need to expel the stored kinetic energy. One way to reduce the speed of propeller is to reduce its speed to less than synchronous speed. This allows the motor to now operate in generator mode. In order to allow the upstream flow of power, the power converter must be able to operate in bi-directional mode and regulate the power flow.

d) Device switching losses

Higher the switching frequency, better the quality of current and voltage waveform. The size of filters is greatly reduced with higher switching frequency. Although switching losses increase resulting in more heat dissipation and requiring larger cooling equipment. Hence the designer has a tradeoff between switching frequency and device power losses.

2.7.3 Future of Marine Power Converters

As the electric propulsion fleet increases, major shipping companies are bound to develop new solutions for safer, reliable and efficient operation of propulsions systems. The future of propulsion systems gives an immense scope for power electronics primarily in power distribution and conversion. Few major enabling technologies are briefly explained below:

a) DC distribution

DC distribution popularly branded as “DC Grid”, takes the advantage of the fact that installed capacity is usually higher than utilization capacity. Other major advantage is ease of incorporating renewable energy systems. DC grid systems as well eliminate the need to synchronize generators during parallel operation. The biggest challenge in full-fledged implementation of DC systems is the development of standardized protection equipment as there is no natural zero to DC current. However some maritime companies already are operating DC electric propulsion, Figure 2.7 shows an example of such application [15].

Figure 2.7 “Dina Star” Equipped with DC electric propulsion [15]

b) Hybrid energy storage

With hybrid energy combination of batteries and super capacitors, fuel savings are achieved by reducing peak demand (peak shaving) and improving redundancy by increasing spinning reserve. Batteries are suitable for short and medium time applications while super capacitors are more suitable for very short abrupt power demand intervals. An example [16], of a marine system retrofitted with batteries as main power source is shown in Figure 2.8.

Figure 2.8 M/V Deutschland recently retrofitted with batteries as main source [16]

c) Power electronic converters

The role of power electronics in the advancement of marine converters lie in converter size reduction, high voltage applications, lower device power losses and modularity. Innovative form of Multi-level converters such as SPCo, Matrix Converters and modular multi-level converters could be considered for high voltage applications in marine systems. Due to high operational costs and stringent safety and regulatory issues reliability has become a prime corner stone in the design of any ship system. Modular converters offer reliable and redundant features that suit rough marine environment conditions. Higher power quality, adaptability, easy restoration and replacement of modular units, faster customization, unit

and demand basis operation are some of the advantageous features that would make modular converters an attractive option for marine electrical systems.

From an operational perspective the size of a power electronic converter depends on switching frequency. Higher the operational frequency, lower the passive element's size, but also higher switching losses. Resonant converters(RC) incur minimal switching losses and can operate at very high frequencies. However, RC's have innate limitations such as poor efficiency at low loads, low life span due to the presence of resonant tank, circulating currents and associated losses and control complexity. New topologies (such as one proposed in this research work) which can incorporate the advantages of RC's and PWM operation is feasible solution for size reduction. Hence, resonant converters have been considered for initial review in order to propose a novel converter topology which combine's the advantages of RC's and PWM converters and suitable for marine environment with reduced operational cost and improved efficiency.

2.8 Review on Existing ZVS and ZCS Converter Topologies

Classification of existing Zero-Current and Zero-Voltage switching converters:

- a) Resonant-Switch Converters
- b) Load-Resonant Converters
- c) Resonant-DC-Link Converters
- d) High –Frequency-Link Integral-Half-Cycle Converters

2.8.1 Resonant Switch Converters

Extensive work has been done on resonant switch converters over the past few decades[17-19]. The resonant switch converters are broadly classified into following four categories based on control pulse generation and applicability.

- I. Fixed Frequency Resonant Converters.
 - a) Series Resonant Converters (SRC)
 - b) Parallel Resonant Converters (PRC)
- II. PWM Resonant Converters

- a) Quasi Resonant Converters (QRC)
- b) Multi Resonant Converters (MRC)
- c) Zero Voltage Transition (ZVT)
- d) Quasi Square Wave (QSC)
- e) ZCS-PWM
- f) ZVS-PWM

III. Load Resonant Converters

IV. Resonant Converter for Inverter Applications

- a) Resonant DC-Link with Inverter System
- b) High Frequency Link Integral Half Cycle Converters

2.8.2 Fixed Frequency Resonant Converters

The most common feature of all the resonant switch converters is the existence of resonant tank, which is used to shape the current and voltage to achieve zero-current turn-off or zero-voltage turn-on. Series-Resonant Converter (SRC) as shown in Figure 2.9.a and Parallel-Resonant Converter (PRC) as shown in Figure 2.9.b are conventional resonant converters [20-32]. In SRC the load is connected in series with resonant tank, while in PRC, the load is connected across the resonant tank. Zero-current turn-off is achieved when the operating frequency is below the resonant frequency and zero-current turn-on is achieved when the operating frequency is above the resonant frequency. This is a major drawback with regards to eliminating switching losses. Significant amount of energy is circulated instead of being transferred to load. This increases peak stress on converter components and has high detrimental effects on efficiency. In general, variable frequency method is used for SRCs and PRCs; this requires a complex and robust control system so as to avoid erratic behavior of the converter due to resonance mismatch.

2.8.3 PWM Resonant Converters

In many known applications, variable switching frequency is considered a huge drawback, especially in the applications where a number of parallel converters are to be used like in distributed power systems. Since converters operating at varying frequencies cannot be

synchronized, the level of harmonic current content rises and results in significant power loss. In Quasi-Resonant Converters (QRC) as shown in Figure 2.10.a, resonant tank is employed across a PWM switch by which the current and voltage are shaped in such a way so as to avoid high current or voltage stress on the semiconductor switch [33-41]. But in most of the converters high current stress is avoided and voltage stress is limited to acceptable limits by using specially designed voltage clamping circuits. Depending on how the switch is connected either turn-on or turn-off losses are eliminated.

Figure 2.9 Fixed frequency resonant converters: (a) Series resonant converter (b) Parallel resonant converter

Figure 2.10 Quasi resonant converters: (a) ZCS Quasi Resonant Converter (b) ZVS MRC Resonant Converter

Multi-Resonant Converters (MRC) as shown in Figure 2.10.b operate at high frequencies by absorbing all the major parasitic impedances. MRCs require constant turn-off time and variable frequency operation. Voltage stress on the switch is reduced at the cost of increase in current stress. Similar is the case Quasi-Square Wave-Converters (QSC), current stress is traded off with voltage stress. By the use of inductors, which can saturate, the above-mentioned converters can retain their ZVS and ZCS property for wide load and input voltages. But lose their basic features when operating at light loads. In ZVT converters shown in Figure 2.11, an auxiliary switch is operated to achieve controlled resonance. These

converters can operate with wide input and load ranges but the power loss due to the presence of auxiliary switch becomes dominant as the power level increases.

(a)

(b)

Figure 2.11 PWM resonant converters: (a) ZVT-PWM Resonant Converter (b) ZVS-PWM Resonant Inverter

The performance of all the above-mentioned converters is very much application dependent. For variable voltage sources and constant load current applications, the increase in input voltage increases voltage stress and conduction losses. The rate of increase of power loss in the converters depends on operating resonant frequency. If the converter is operating at a frequency less than the resonant frequency the increased conduction, losses partially offset frequency-dependent losses (switching, gating losses). If the operating frequency is above the resonant frequency with the increase in input voltage results in faster rate of efficiency

decrement. The conclusion applies to family of resonant converters discussed above. PRC family of converters is suitable only for high current, low voltage and narrow input voltage range. In QRC converters, operating frequency is limited due to capacitive turn-on feature. At higher frequencies the discharge rate of the capacitor increases resulting in significant power loss. Though the discontinuity in resonant current reduces the circulating current, it decreases the input side efficiency drastically in QRCs. The effect of circulating energy loss is significant in all the resonant family converters especially when operating with wide load range. In single-ended ZVS-PWM, the switch suffers from a very high voltage stress, which is proportional to load range which ZVS condition is achieved. One major drawback corresponding to ZVS-PWM converters is that the rectifier diode is not operated with suitable switching condition in regards to achieve ZVS. All the converters achieving ZVS do not utilize the transformer leakage reactance effectively and hence require additional inductance to achieve resonance. This increases size, weight and complexity of the converter. In order to achieve zero voltage switching the device off-time must be kept constant at the value determined by the resonant elements.

2.8.4 Load Resonant Converters

In Load Resonant Converters (LRCs) shown in Figure 2.12, load actually forms a part of a resonant circuit. The hybrid Series-Parallel LRC is the most commonly used converter of this family [42-51]. The output voltage is produced by rectifying and smoothing the sinusoidal voltage across C_{rp} . Regulation of the output voltage is achieved by small

Figure 2.12 Parallel Load Resonant Converter

adjustments to the switching frequency. ZCS is achieved while operating below the resonant frequency and ZVS is achieved while operating above the resonant frequency. The disadvantages of this circuit are high peak currents and excess power loss due to high circulating energy. To sustain with higher peak currents, the devices should be of higher rating which in turn increases the conduction losses and limits the frequency range. The peak current and voltage levels are comparable with hard switched circuits. In LRCs it is very difficult to obtain effective power control while achieving ZCS.

2.8.5 Resonant DC-Link Inverters

Resonant DC-link inverter shown in Figure 2.13, is commonly used in inverter applications [52-62]. Many topologies have been designed to achieve ZCS and ZVS by using resonant DC-link. The operation of this circuit is similar to any other resonant converter. By careful control of inverter switches, the resonating voltage is forced to zero. During this period inverter switches are operated (ON/OFF) and thus keeping switching losses to minimum. Apart from giving us the advantage of low-loss topology resonating DC-link gives rise to many major setbacks. Resonant DC-link has many disadvantages when compared to hard-switching topologies. The peak off-state voltage impressed across the devices is typically increases to 2.5-3.0 times input voltage. Furthermore, since the device commutations are constrained to occur at the zero voltage instants, the usual PWM control strategies cannot be employed since they require continuous variation in the times between the switching

Figure 2.13 Resonant DC-Link Inverter

instants. Instead, a discrete pulse modulation technique must be utilized. However, the resultant output voltage frequency spectrum is severely degraded compared with a well-established PWM technique.

As high voltage stress is one of the major drawbacks with the use of resonant DC-link, many actively clamped circuits have been designed to limit the voltage rise to 1.5 times the input voltage. But this requires specially designed voltage clamp circuits and more components. By adding protection circuits for the devices; power loss as well increases. A part from this a complex control system has to be designed. As it known that the voltage stress on the switches would be high, the devices and components have to be rated for higher voltage. Use of devices with higher rating increases on-state voltage drop and thus increasing conduction loss. Devices with higher current and voltage rating are not suitable for high frequency operation.

2.8.6 High Frequency-Link Integral Half Cycle Converters

Figure 2.14 High Frequency-Link Integral Half Cycle Converters

If the input to a single-phase or three-phase inverter is a high-frequency sinusoidal ac, then by using bidirectional switches it is possible to synthesize a low-frequency ac of adjustable magnitude and frequency or an adjustable-magnitude DC, where the switches are turned-on and turned-off at zero crossings of the input voltage. The high-frequency-link converters shown in Figure 2.14 [63-65], are a form of cyclo-converters, whereby the power is

transferred between two ac systems operating at two different operating frequencies without an intermediate DC link. Drawbacks similar to resonant-DC link are realized here as well. The voltage stress on the inverter switches is 1.5 times the nominal input voltage. For inverter switch to operate at ZCS/ZVS careful and precise switching sequence is necessary and hence a very complex control system is required. High-frequency-link converters are usually preferred for very high power and narrow input voltage range

2.9 Summary

Limitations of the above discussed Resonant/ ZCS/ZVS inverter configurations are summarized as follows:

1. Increased circuit complexity.
2. Increased device voltage or current ratings and large circulating energy.
3. Restrictions on device switching times and conduction times. Hence resulting in inefficient utilization of switch and requiring variable switching frequency especially in DC power supply applications.
4. Converters are highly sensitive to resonant component values; hence components have to be precisely fabricated; which is difficult. The impedance of magnetic components does change with operating environment parameters like temperature and EMI.
5. Depending on circuit design either turn-on or turn-off losses are mitigated; not both.
6. Highly sensitive to circuit parasitic features.
7. Wide load range operation is not possible.
8. Presence of inductors and capacitors increases the volume and weight of the converter system.
9. Resonant converters are highly dependent on source and load operating conditions which is major draw when it is required that the converter has to suit for multi-purpose operation.
10. Complex structure and control is required for multi-level operation.
11. Achieving high levels of power density is difficult.

12. Resonance can occur between grid connected capacitors and transformers (especially in the case of DC-link and AC-link resonant converters connected to grid). Hence resulting in current and voltage magnifications

2.9.1 Desired Features in an Efficient Inverter

Based on the understanding of above limitations and various complications associated with high frequency power conversion, we can conclude by listing out the desired or ideal features required for an inverter to be highly efficient.

1. ZCS/ZVS condition should be achieved.
2. Neither resonant tank nor any sort of magnetic components should be utilized in achieving ZCS/ZVS operation.
3. Wide Load Range operation should be possible (no load to full load)
4. Losses occurring should be limited to minimal (by at least 20%)
5. Very high frequency operation should be feasible for further size reductions as technology enhances. (> 30 kHz for medium voltage)
6. Reduced or eliminate the need to any inductance required at the input (5kW/dm^3)

The research work presented here primarily focuses on efficiency, cost effectiveness and reliability on the inverter side. The front end converter research work (prior research conducted by Prof. Iftekar. Ali Maswood's team [66-73]) aims at reducing the size of the input line inductance. Collectively a lightweight and efficient power inverter system for marine applications is expected to be designed and developed.

The development in marine converters has been rapid in the past two decades. This advancement is due to developments in power electronic device and converter construction and operational technologies. Hence, the implications of power electronics have been revolutionary. As mentioned earlier, due to rising oil prices and stringent environmental policies, the demand for large multi-purpose ships is increasing. The ship builders are confronted with new challenges of finding design solutions which can withstand rough marine environment while conserving space and weight to accommodate numerous utilities.

A compact medium voltage solution is one way to achieve to an efficient and light weight propulsion system. Resonant converter characteristics have been found to be quite suitable for marine drive systems due to advantageous features such as minimal switching losses, high frequency operation, and compact retrofit able configurations. These parameters are the foundational layers for this research. The research work presented here in focuses on achieving the high efficiency, lower switching losses, higher reliability, improved redundancy and lower cost (i.e., the advantageous features of resonant converters) by eliminating the major drawbacks and associated limitations of resonant converters and further more proposing novel inverter configurations which enable to meet the success parameters.

Chapter 3 A Novel Highly Efficient Tank-Less Zero-Current Switching Inverter

3.1 Overview of the Proposed Inverter Configuration

Addressing the limitations of soft-switching and existing inverters, a novel inverter configuration is proposed. The proposed inverter aims to achieve high frequency operation by a unique soft-switching technique without the utilization of any kind of resonance phenomenon. The proposed inverter configurations retain the advantages of PWM control as well. Detailed description, analysis and operational features of proposed inverter are presented in this chapter.

In spite of considerable research, resonant techniques have yet to be incorporated into commercial PWM inverter systems. The increased equipment complexity and the limitations of the useable modulation techniques with some systems outweigh the advantages. The novel topologies presented will address the limitations of these resonant converters. Zero current lossless switching, low voltage stress, wide load operation are few important limitations, which are very well addressed by the topologies. The topologies stand out from existing zero current/voltage switching converters as they do not use any resonant technique or resonant tank what so ever to achieve zero current switching. The inverter switches are turned-on and off at zero current. This unique feature to eliminate switching losses presents one with a possibility to operate at very high frequency (medium high voltage, $> 20\text{kHz}$).

The overview of the topology is shown in Figure 3.1. In practice, switching frequency is increased by decreasing the turn-on period to keep the conduction losses in check, but switching losses turn out to be dominant as the frequency is increased. The topologies achieve zero-current switching and hence minimizing switching losses to an insignificant level. The optimum operating frequency and size of the input line inductance (not shown here) has to be determined based on the relation between rated power and supply frequency.

In Figure 3.1, the overview of the proposed concept is presented. Multilevel rectifier is required for very high power applications; usually a single rectifier unit is sufficient for small, medium and high power applications. The bi-directional switch control unit is incorporated with the front-end rectifier [66-73] to achieve Unity Power Factor operation. The DC-link capacitor bank is used to maintain a constant DC-output voltage at the output side of the rectifier. The above-mentioned operational blocks constitute a front-end converter unit, which is well known and extensively studied. *The novel topology designed is the back-end converter comprising of partitioning cell and multi-input inverter.* The idea of novel back-end converter is presented along with a front-end converter to demonstrate immediate applicability in AC-AC drive systems. The back-end converter performs two operations; partitioning cell performs a multiplexing operation while the inverter performs the inversion operation. Both the partitioning cell and inverter combine to result in a low-loss operation.

Figure 3.1 Overview of the proposed Inverter topology

3.2 Proposed Topologies and Principle of operation

Two novel topologies are designed to address the limitations of the existing zero-current/zero-voltage switching inverter while having the added advantages of PWM control. The positioning of partitioning cell gives rise to two inverter topologies. The basic structures of the two topologies are presented in Figure 3.2 and Figure 3.3, and their operation is explained in the following sections explained. The topologies have similar operational features but differ largely in applicability, complexity and structural features.

3.2.1 Proposed Topology-1

In Figure 3.2, the basic structure of Topology-1 is presented. The partitioning cell is placed in front of the front-end rectifier. The current/power is directed into various rectifier units, according to the switching functions of the switches in partitioning cell. This presents a parallel path power conversion and is closely inferred as more suitable for high power application.

Figure 3.2 Proposed Topology-1

The output of an individual rectifier is in the form of DC pulses. The inverter switches operate just beyond the boundary limits of these DC pulses from the rectifier. This ensures that the switch is operated (ON/OFF) at zero current condition. Hence, the switch can be operated at very high frequency.

3.2.2 Proposed Topology-2

In Figure 3.3, the basic structure of topology-2 is presented. The partitioning cell is placed in between the front-end rectifier and the inverter. This topology is more suitable for Medium and Low power applications. The partitioning cell segregates the current after rectification. Current entering the Inverter is in the form of DC pulses and as the inverter switches are operated beyond the limit of DC pulse, zero current switching operation is ensured. Simplicity of topology-2 over topology-1 and its feature to readily integrate with existing converter systems encourages one to perform an in-depth analysis for utility-based applications.

Figure 3.3 Proposed Topology-2

3.2.3 Principle of Operation

The principle of operation for both the topologies is similar. Although the analysis is presented bearing topology-2 in mind. Assuming an ideal sinusoidal source, the input current I_{IN} and voltage V_{IN} . The supply frequency is f_s . In describing the operation of partitioning cell switches consider two flying switches connected in parallel as shown in Figure 3.4.a. The switching frequency of both the switches is f_t . If the duty ratio of one switch is T_d , then the other switch is $1 - T_d$. Hence, when one switch is ON the other is OFF and vice versa. The switches S_1 , S_2 constitute the partitioning cell and their switching sequence is shown in the Figure 3.4.a.

Due to such complimentary operation as shown in ref. Figure 3.4 Principle of operation of proposed inverter topologies. b of partitioning cell switches (S_1 , S_2), the current entering into the inverter (INV 1, INV 2) is in the form of DC pulses. INV- 1 and INV 2 denote inverter cells. The duty ratio of inverter switches must be a fraction greater than that of partitioning cells throughout the operation in order to achieve zero current switching. The inverter switches are gated just beyond the limits or the boundary of the current pulse (indicated by dotted line as shown in Figure 3.4 Principle of operation of proposed inverter topologies) and hence switching (ON/OFF) at zero current.

The inverter switching signals as explained in Figure 3.4.c (INV 1, INV 2) operate just beyond the limits or boundary of the current pulse (indicated by dotted line in Figure 3.4.c) and hence switching ON/OFF at zero current. The voltage stress across the switch during these short intervals is very low. The importance on voltage stress and exact losses incurring are discussed in detail in loss modeling chapter. As we can observe, zero-current switching is achieved without using any resonant technique or resonant tank, no circulating energy is lost. The incorporation of partitioning cell presents us with numerous advantages and addresses almost all the limitations of resonant converters and high frequency converters. The inverter switches are now operated (ON/OFF) at zero-current and low voltage, both turn-on and turn-off losses are practically zero. As the switching now causes no switching losses, reduced di/dt and dv/dt losses, it is feasible to operate inverter switches at a very high frequency.

Figure 3.4 Principle of operation of proposed inverter topologies: (a) Switching operation of partitioning cells (b) Switching sequence of S_1 and S_2 (c) Zero current switching operation of proposed inverter

3.3 Open Loop Operation

3.3.1 Topology-1

In Figure 3.5, the schematic up for open loop operation of Topology-1 is shown for a single-phase application. Table 3-1 presents the correspondence between switches and inverter design blocks. No DC-link is utilized as of now. DC-link is incorporated when discussing the utility-based applications of the topologies. The control signals for all the switches in both the topologies are similar. Simple SPWM pulse generator along with a Zero-Current switching signal (ZCSS) is designed as a gate pulse to the inverter.

Figure 3.5 Topology-1 – Open loop operation with ‘R’ load with simple logic trigger circuit

Table 3-1

Operational switches in Topology-1

Switches	Inverter block
S_1, S_2	Partitioning Cell
$(T_{11}, T_{12}, T_{13}, T_{14})$	Inverter 1 (INV 1)
(T_{11}, T_{14})	LEG-A (L-A)
(T_{12}, T_{13})	LEG-B (L-B)
$(T_{21}, T_{22}, T_{23}, T_{24})$	Inverter 2 (INV 2)
(T_{21}, T_{24})	LEG-C (L-C)
(T_{22}, T_{23})	LEG-D (L-D)

3.3.2 Results: Topology-1 with R-load

The switching sequence of partitioning cell switches and inverter switches is shown in Figure 3.6. For a resistive load, a simple logical pulse-generating unit is sufficient. However, for RL load and motor load sinusoidal PWM technique is used. Zero-current switching is achieved in both the cases. The partitioning cell switches and inverter switches operate at 20 kHz. Delay units are used to avoid any chance of overlap which can occur with a highly inductive load. An AC wave in the pulse circuit is used as a reference wave so that the load current is of desired frequency. A 400v DC- line is used as an input source supplying a resistive load of 40.5 Ω . The load current and load voltage are presented in Figure 3.7.a. The current and gating pulse of the inverter switch is shown in Figure 3.7.b. It is inferred that zero switching operation is ensured and the switch operates beyond the rising and falling edges of the current pulses. The switch is turned-on before the current rises to its maximum value at particular switching cycle.

Figure 3.6 Switching sequence for partitioning cell and inverter Switches

(a)

(b)

Figure 3.7 Output waveforms of Topology-1 shown in Figure 3.5 : (a) Load Voltage and Load Current of Topology-1 with R-load (b) Current through an inverter switch

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3.3.3 Topology-2

In Figure 3.8, the schematic for open loop operation of Topology-2 is presented. Output waveforms are shown in Figure 3.9. Topology-2 with RL load and SPWM control pulse generator with a logical combination of ZCS control pulse is presented. The inverter switches operate just beyond the boundary of operation of S_1, S_2 as these switches enable the inverter switches to operate at zero current.

As the switches are switched at zero current and beyond the limits of rising and falling edges of the current pulse, the switch endures a very low voltage/current stress. The source current waveform is considered as reference assuming the required load current frequency is same as source current frequency. If the load current is required to have a different frequency, then a waveform of a frequency equal to required load frequency is taken as a reference and similar operation can be achieved.

Figure 3.8 Topology-2 schematic

In Figure 3.9, the simulation results of Topology-2 with RL load are presented. In Figure 3.9.b, it is shown that the inverter cell switch is turned ON and OFF beyond the edge of the current pulse. It is inferred that the load current waveform is continuous and zero-current switching operation is as well ensured.

Figure 3.9 Simulation results of Topology-2 shown in Figure 3.8 with RL-Load : (a) Load current and Load voltage (b) Zero current switching (c) Input current of Topology-2

3.4 Three-Phase Analysis

3.4.1 Topology-1: Three-Phase Inverter Analysis

In this section, three-phase operation of the proposed topologies is explained. Three-phase schematic of Topology-1 is presented in Figure 3.10. Construction of Topology-1 is simple as three single-phase circuits are connected in parallel with output shifted by 0° , -120° and -240° . The output from all the parallel circuits is cascaded at the load end. Each parallel power conversion path operates similar to single-phase operation of Topology-1 but with a phase difference of 120° . The phase voltage at the load end is sinusoidal just as observed in single-phase operation of Topology-1. This due to the fact that there is no DC-link or filter present after rectification. Topology-1 has similar operational features of matrix converters.

The load voltage (phase and line-line) is sinusoidal as the two modulating sinusoidal waveforms are 180° apart unlike in commonly SPWM three-phase inverter where the load voltage is a stepped waveform. A 440 volt, 50 Hz, 4-phase supply is used as a power source.

Figure 3.10 Topology-1- Three-phase schematic with RL load

In Figure 3.10, a parallel path power conversion architecture of Topology-1 is presented. This feature of Topology-1 is suitable for very high power application and where a wide load range operation is required. Depending upon the required load power, number of parallel paths required for supplying that particular load are varied. This improves converter efficiency at lighter/ frequently varying loads.

When operating at a rated power condition, all the parallel paths are operated at their rated conditions. Though the number of switches increases, losses are limited to minimum. The only switches, which incur amount able loss, are partitioning cell switches. However, total losses incurred are less than that incurred by conventional PWM 3-phase inverter. Another advantage over conventional three-phase inverter is having good operational performance at high power and high frequency operation. The drawback as visible in the case of Topology-1 is the use of more semiconductor devices and this effects reliability of overall system. This limitation is addressed by Topology-2 by using minimum number of switches and providing more advantages than Topology-1. Hence, Topology-2 is extensively studied over Topology-1 and its simplicity in design encourages us to validate its effectiveness when incorporated into various existing systems.

In Figure 3.11, the simulation results of output waveforms of Topology-1 have been presented. The waveforms obtained are similar to that of conventional three phase inverter without sinusoidal modulation. The complexity in operation, construction and higher number of semi-conductor switches of Topology-1 outweigh the benefits of zero current switching. The construction of Topology-2 can be easily deduced as two parallel PWM inverter operating with corresponding DC link enabling switch. Topology-2 as well incorporates a parallel path power conversion process yet utilizing lower number of switches. Hence, Topology-2 will be of a greater interest due to its retrofit table, easy construction and operational features.

Figure 3.12 Source current and input DC current to inversion stage in Topology-1

Figure 3.11 Three phase Topology-1 output waveforms shown in Figure 3.10: (a) Phase voltage (b) Line current (c) Line-line voltage

3.4.2 Topology-2: Three Phase Inverter Analysis

The 3-phase schematic of Topology-2 is presented in Figure 3.13. Operational principle of Topology-2 is similar to Topology-1. Both the topologies achieve ZCS irrespective of load and source conditions. The control pulses generated by a logical combination of ZCS signal generator unit and PWM signal generator. In conventional PWM inverter, the modulation index is varied for certain applications depending on the load condition. Hence, the inverter cannot operate at peak efficiency at all times. The proposed ZCS inverter incorporates a partitioning cell, which can as well regulate the power flow to the inverter cells. This allows the inverter to operate at constant modulation where peak efficiency is achieved.

Figure 3.13 Three-phase schematic of Topology 2

Figure 3.14 Simulation results of analysis of three phase Topology-2 shown in Figure 3.13: (a) Load voltage and current waveforms (b) Gate pulse to inverter switch T_{12} (c) Current through and voltage across inverter switch T_{12}

3.4.3 Simulation Results of Topology-2: Three-Phase Inverter Analysis

In Figure 3.14, the simulation results of Topology-2 are presented. The output waveforms are similar to that of a conventional PWM inverter. The performance of the proposed ZCS inverter topology-2 is deemed equal to existing 3-phase PWM inverter. In Figure 3.14.b, the cumulative gating pulse consisting of ZCS and PWM inverter is shown. The envelope of gating pulse is similar to PWM pulse as explained in Figure 3.14.b to the left. The current and voltage waveforms presented in Figure 3.14.c prove the feasibility of the concept. The inverter input side waveforms presented in Figure 3.15 are similar to that of the PWM inverter drive system with a front end converter. Topology-2 has a great ease of construction and realization. Many comparative conclusions are drawn between ZCS inverter and PWM inverter in the following chapters. The major advantages of ZCS inverter is reduction of switching loss, redundant architecture and elimination of passive components to achieve zero current switching.

Figure 3.15 Simulation results of 3 phase Topology-2 shown in Figure 3.13: (a) Source current (b) Rectified DC current (c) Output phase current (I_A)

3.5 Experimental Results

The design specifications for the 1kW lab prototype are: DC link Voltage of 500V; Max current of 2A, DC-link capacitance used being 1000 μ F, 500V(DC); 5kHz switching frequency and IRG450CKBPf IGBT's are utilized as an inverter switches. Most of the conventional three phase inverter systems operate at switching frequencies less than 10kHz. Though the proposed ZCS inverter can operate at higher frequencies, 5kHz switching frequency is chosen in order to draw comparisons and evident gains of the proposed inverter configuration. Experimental results are illustrated in Figure 3.16 and Figure 3.17. The current and voltage waveform pertaining to partitioning cell switches of topology-2 are presented in Figure 3.16. Only two, partitioning cell switches S1 and S2 are hard switched. In Figure 3.17.b and Figure 3.17.c, zero current turn off and zero current turn on pertaining to an inverter switch are shown respectively. It is noted that the current is nearly zero during both turn on and turn off periods. The switching losses occurring during these intervals are minimal. This allows the inverter switches to operate at higher frequency. In addition, the resulting turn-on, turn-off switching transients due to di/dt and dv/dt are reduced drastically. This aids in high reduction of EMI. In Figure 3.17.d, Figure 3.17.e and Figure 3.17.f Phase voltage of the load, line-line load voltage and load current are presented respectively. In Figure 3.17, the experimental setup of ZCS inverter is shown with various components and their placement.

Figure 3.16 Voltage and current waveforms of partitioning cell switches: (a) SW₁ (b) SW₂

Figure 3.18 Experimental setup of ZCS Inverter

Figure 3.17 Experimental results of 3-phase Topology-2: (a) Current and gate signal of inverter switch T_{12} (b) Zero Current Turn-OFF (c) Zero Current Turn-ON (d) Phase Voltage V_{AN} (e) Line-Line Voltage V_{AB} (f) Load Current-ZCS Inverter

3.6 Comparison of Topology-1 and Topology-2

In Table 3-2, a Topology-1 and topology-2 are compared based on feasibility and retrofit ability aspects. A simple trade analysis is presented in order to justify the choice of topology-1 for further research.

Table 3-2
Comparison of Topology-1 and Topology-2

Aspect	Topology-1	Topology-2	PWM inverter
Ease of construction	4	3	5
PWM Operation	4	4	4
Power losses	5	4	3
Number of hard switching devices	5	3	3
Number of soft switching devices	5	3	-
Ease of operation	4	3	5
Partitioning cell's operation	3.5	4	-
Effect on DC-Link	3	4	5
Size and weight	4	2	3.5
Overall	4.1	3.3	3.5

5- being the best, 1- being the poor

The scores have been given with respect to conventional PWM inverter

Topology-1 with soft switching capabilities, parallel path power conversion and relative ease of operation makes it a more favorable choice for further investigation. A comparative study on various other prime aspects such as cost effectiveness, reliability, redundancy, harmonics between Topology-1 and conventional PWM is presented in the following sections. Topology-1 will be presented as the proposed zero current switching inverter in this document. Topology-2 will no longer be considered for further analysis.

3.7 Mathematical Analysis of the Proposed ZCS Inverter: Topology-2

3.7.1 Analysis of Single-Phase Topology-2

Mathematical analysis for both the topologies is similar. Topology-2 due to its simplicity and its readiness to be incorporated into existing systems with minimum retrofitting, attracts greater interest. Hence, the mathematical analysis presented here is with respect to Topology-2.

The switching functions of each switch in Topology-2, shown in Figure 3.3 are listed in Table 3-3.

Table 3-3
Switching functions in Topology-2

Switching function	Inverter block
S_1	SW_1
S_A	LEG-A (T_{11}, T_{14})
S_C	LEG-C (T_{21}, T_{24})
S_2	SW_2
S_B	LEG-B (T_{21}, T_{13})
S_D	LEG-D (T_{22}, T_{23})

The average current supplied by the DC source is I_{DC0} . The instantaneous current through SW_1 is $I_{dc1}(t)$. The instantaneous current through SW_2 is $I_{dc2}(t)$. The instantaneous load current $I_L(t)$ as function of DC input current entering into the inverter and switching states of SW_1 and SW_2 is expressed in Eq. (3.1).

$$I_L(t) = S_A S_1 I_{dc1}(t) + S_C S_2 I_{dc2}(t) + S_B S_1 I_{dc1}(t) + S_D S_2 I_{dc2}(t) \quad (3.1)$$

The Eq. (3.1) is rewritten as shown in Eq. (3.2),

$$I_L(t) = (S_A S_1 + S_B S_1) I_{dc1}(t) + (S_C S_2 + S_D S_2) I_{dc2}(t) \quad (3.2)$$

The partitioning cell switches SW_1 and SW_2 operate at a frequency at a frequency of f_c , T_c being the time period and the duty ratio is 'p'. I_{dc0} is the value of the current pulse input to the inverter from the DC supply. The currents through the partitioning cells are expressed in Fourier domain as shown by Eq. (3.3) and Eq. (3.4).

$$I_{dc1}(t) = a_{01} + \sum_{n=1}^{\infty} \left(a_{n1} \cos \frac{2n\pi}{T_c} t + b_{n1} \sin \frac{2n\pi}{T_c} t \right) \quad (3.3)$$

$$I_{dc2}(t) = a_{02} + \sum_{n=1}^{\infty} \left(a_{n2} \cos \frac{2n\pi}{T_c} t + b_{n2} \sin \frac{2n\pi}{T_c} t \right) \quad (3.4)$$

By substituting the Fourier coefficients in Eq. (3.3) and Eq. (3.4), the input DC current expressions for INV1 and INV2 are given by Eq. (3.5) and Eq. (3.6).

$$I_{dc1}(t) = p \cdot I_{dc0} + \frac{2I_{dc0}}{kT} \sum_{i=1}^n \left(\sin(pkT_c) \cos(kt) \right) + \left(1 - \cos(pkT_c) \sin(kt) \right) \quad (3.5)$$

$$I_{dc2}(t) = (1-p)I_{dc0} + \frac{2I_{dc0}}{kT} \sum_{i=1}^n \left[\cos(pkT_c - 1) \sin(kt) - \cos(pkT_c) \sin(kt) \right] \quad (3.6)$$

Where, $k = 2n\pi/T_c$ and 'p' is the duty cycle ratio of the current passing through the switching devices in the DC-bus.

Substituting Eq. (3.5) and Eq. (3.6) in Eq. (3.2) we get an expression for the instantaneous load current shown in Eq. (3.7). On observing the Eq. (3.5) and Eq. (3.6) we can infer that the harmonic coefficients are opposite in sign to each other. The coefficients contain the duty cycle term 'p'. Selective harmonic reduction techniques can be applied easily by adjusting the values 'p', 'k' especially when the proposed concept is applied for multilevel inverters.

$$I_L(t) = (S_A S_1 + S_B S_1) \left[\frac{p \cdot I_{dc0}}{kT} \sum_{i=1}^n \left[\frac{\sin(pkT_c) \cos(kt)}{kT} + (1 - \cos(pkT_c) \sin(kt)) \right] \right] +$$

$$(S_C S_2 + S_D S_2) \left[\frac{(1-p) I_{dc0}}{kT} \sum_{i=1}^n \left[\frac{\cos(pkT_c - 1) \sin(kt)}{kT} - \cos(kt) \sin(pkT_c) \right] \right]$$

(3.7)

3.7.2 Analysis of Three-Phase Topology-2

A conventional 3-phase PWM inverter with six switches has nine possible switching states as represented by matrix Q_s . The corresponding line-line output voltages at the operation of respective switching states from Q_s are represented by voltage matrix V_{si} . In order to satisfy KVL and KCL both the switches in the same leg are not turned-on at the same instant. The proposed ZCS inverter as explained in Figure 3.13, consists of two PWM inverter cells and two partitioning cell switches. The switching function for each switch (T_{ij}) of the proposed ZCS inverter Topology is represented by s_{ij} and s_i for partitioning cells switches, where $i = \{1, 2\}$ represents n^{th} inverter cell and corresponding switch in portioning cell while $j = \{1, \dots, 6\}$ represents the n^{th} switch in any particular inverter cell. When a partitioning cell switch is ON ($s_i=1$), the corresponding inverter cells switches in the same leg are complementary in nature. The switching functions for INV1 and INV2 abide by the relations as listed in Table 3-4.

Table 3-4
Switching function relations

INV 1	INV2	Partitioning cell
$s_1(s_{11} + s_{14}) = 1$	$s_2(s_{21} + s_{24}) = 1$	$(s_1 + s_2) = 1$
$s_1(s_{13} + s_{15}) = 1$	$s_2(s_{23} + s_{25}) = 1$	$s_1 = \bar{s}_2$
$s_1(s_{12} + s_{16}) = 1$	$s_2(s_{22} + s_{26}) = 1$	

The switching states of the SPWM inverter cell switches and corresponding line-line voltages are represented by matrices Q_s and V_{si} respectively.

$$Q_{si} = \begin{bmatrix} S_{i1} & S_{i3} & S_{i2} \\ 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \quad V_{si} = \begin{bmatrix} V_{ab_i} & V_{bc_i} & V_{ca_i} \\ 0 & 0 & 0 \\ 0 & -V_{DC} & V_{DC} \\ -V_{DC} & V_{DC} & 0 \\ -V_{DC} & 0 & -V_{DC} \\ V_{DC} & 0 & -V_{DC} \\ V_{DC} & -V_{DC} & 0 \\ 0 & V_{DC} & -V_{DC} \\ 0 & 0 & 0 \end{bmatrix} \quad (3.8)$$

Ensuring only eight possible valid states from the matrices Q_s and V_{si} we obtain the following relations for instantaneous voltages in INV1 and INV2 as listed in Table 3-5. V_{ON} is determined by adding the equations from either of the columns in Table 3-6. Thus, obtained an expression for V_{ON} is given by Eq. (3.9).

$$V_{ON} = \frac{V_{DC}}{12} [s_1(2s_{11} + 2s_{13} + 2s_{12} - 3) + s_2(2s_{21} + 2s_{23} + 2s_{22} - 3)] \quad (3.9)$$

By substituting Eq. (3.9) in all the equations listed in Table 3-5 and assuming balanced condition ($V_{AO} + V_{BO} + V_{CO} = 0$), output phase voltages can be determined. The output phase

Table 3-5
Instantaneous voltages of INV1 and INV2

INV1	INV2
$\frac{V_{DC}}{2} s_1(s_{11} - s_{14}) = V_{A_1O} + V_{ON}$	$\frac{V_{DC}}{2} s_2(s_{21} - s_{24}) = V_{A_2O} + V_{ON}$
$\frac{V_{DC}}{2} s_1(s_{13} - s_{15}) = V_{B_1O} + V_{ON}$	$\frac{V_{DC}}{2} s_2(s_{23} - s_{25}) = V_{B_2O} + V_{ON}$
$\frac{V_{DC}}{2} s_1(s_{12} - s_{16}) = V_{C_1O} + V_{ON}$	$\frac{V_{DC}}{2} s_2(s_{22} - s_{26}) = V_{C_2O} + V_{ON}$

voltages (V_{A1O} , V_{B1O} , V_{C1O}) and (V_{A2O} , V_{B2O} , V_{C2O}) obtained are listed in Table 3-6. The incorporation of partitioning cells provides an additional degree of freedom in controlling the power flow. This unique feature allows the inverter to operate at a fixed modulation index while maintaining good performance and high efficiency. The frequency modulation index is m_f and m_a being the amplitude modulation index

Table 3-6
Output phase voltages of proposed ZCS inverter

Phase	Phase voltage expression
V_{A1O}	$\frac{V_{DC}}{6} [s_1(5s_{11} - s_{13} - s_{12} - 1.5) + s_2(s_{21} + s_{23} + s_{22} - 1.5)]$
V_{B1O}	$\frac{V_{DC}}{6} [s_1(5s_{13} - s_{11} - s_{12} - 1.5) + s_2(s_{21} + s_{23} + s_{22} - 1.5)]$
V_{C1O}	$\frac{V_{DC}}{6} [s_1(5s_{12} - s_{11} - s_{13} - 1.5) + s_2(s_{21} + s_{23} + s_{22} - 1.5)]$
V_{A2O}	$\frac{V_{DC}}{6} [s_2(5s_{21} - s_{23} - s_{22} - 1.5) + s_1(s_{11} + s_{13} + s_{12} - 1.5)]$
V_{B2O}	$\frac{V_{DC}}{6} [s_2(5s_{23} - s_{22} - s_{21} - 1.5) + s_1(s_{11} + s_{13} + s_{12} - 1.5)]$
V_{C2O}	$\frac{V_{DC}}{6} [s_2(5s_{22} - s_{21} - s_{23} - 1.5) + s_1(s_{11} + s_{13} + s_{12} - 1.5)]$

Excluding blanking time, the line-line RMS voltage at fundamental frequency f_s is given by Eq (3.10)

$$V_{LL1} = \sqrt{\frac{3}{2}} \left(\hat{V}_{A1N} \right) \quad (3.10)$$

The peak value of the fundamental frequency component in each leg of the inverter is given by Eq. (3.11). Refer Figure 3.13 for nodal voltages- v_{IN} .

$$\left(\hat{V}_{A_1N} \right) = m_a \frac{V_{1N}}{2} \quad (3.11)$$

Where, $V_{1N} = T_d V_{DC}$. By using Eq. (3.10) and Eq. (3.11) the line –line RMS voltage for inverter cell INV1 (V_{LL1}) can be expressed as shown in Eq. (3.12).

$$V_{LL1} = \sqrt{\frac{3}{2}} m_a T_d V_{DC} / 2 = 0.612 m_a T_d V_{DC} \quad (3.12)$$

Similarly, the line-line RMS voltage for inverter cell INV 2 (V_{LL2}) can be expressed as shown in Eq. (3.13).

$$V_{LL2} = \sqrt{\frac{3}{2}} m_a (1 - T_d) V_{DC} / 2 = 0.612 m_a (1 - T_d) V_{DC} \quad (3.13)$$

The total line-line RMS load voltage of the proposed ZCS inverter is shown in Eq. (3.14)

$$V_{LL} = 0.612 m_a V_{DC} \quad (3.14)$$

If each inverter cell is required to supply an individual load of varied power level with different modulation indices m_1 and m_2 , the total line-line RMS load voltage at the ZCS inverter terminal is given by Eq (3.15).

$$V_{LL} = 0.612 V_{DC} \sqrt{(m_2^2 + T_d^2 (m_1^2 - m_2^2))} \quad (3.15)$$

Equations (3.14) and (3.15) suggest that the peak amplitude of V_{LLrms} for a ZCS inverter is equal to that of a conventional PWM inverter. The presence of partitioning cell duty ratio ‘ T_d ’ parameter in the equations (3.14) and (3.15) enables better control of average of power delivered to the load when it is required to maintain constant PWM modulation (m_a) index.

3.8 Summary

Two novel topologies of different structural design with similar operational characteristics have been introduced and analyzed in detail. The comparison between the two topologies has been made and conclusions have been made to aid when choosing a design to implement. Topology-2 has been chosen for an extensive study to prove an application case while competing with conventional 3-phase PWM inverter. The hardware of Topology-2 proves the feasibility of the proposed concept. Mathematical analysis of proposed ZCS inverter (Topology-2) is as well presented. The experimental results prove the feasibility of the novel concepts. A further analysis on various inverter aspects are carried to inspect the competitiveness of ZCS inverter with respect to conventional PWM inverter

Chapter 4 Analysis on Power loss, Cost Effectiveness and Reliability Analysis of ZCS Inverter

In this chapter a detailed comparative power loss analysis between ZCS inverter and conventional PWM inverter is presented. Economic feasibility and cost effective operation are major challenges hindering many power converter technologies. Hence a brief cost analysis considering capital and operational costs for 1MW propulsion inverter is presented.

4.1 Power Loss in Semiconductors

Semiconductor technology has made rapid advancements in the past few decades. IGBTs and MOSFETs are an integral part of modern day power electronic equipment. Lately IGBTs have captured interests of power electronic engineers. This is mainly because IGBT's have higher voltage, current ratings and can be operated at a few tens of kilohertz frequency. Another major reason being, conduction losses in MOSFETs are higher when compared to IGBT's. Due to relatively high tail-current in IGBTs, it is not highly beneficial when operating at very high frequency. But with soft-switching IGBTs are a good choice for high power and high voltage applications. ZCS is more effective in reducing IGBT switching losses compared to ZVS [74-77] . Such features make IGBT highly attractive to the proposed inverter topologies.

This section presents a brief insight on ZCS and ZVS techniques. A comparative analysis between conventional PWM and proposed Topology-2 is done. Mathematical analysis alongside with simulation results is presented. Various factors such as frequency, load current and switching times are considered. The comparison demonstrates the effectiveness of the proposed technique in mitigating device losses generally incurred.

Over the years, IGBT has been extensively studied and utilized in various power electronic applications. Knowledge on methods to estimate total device losses, IGBT loss modeling, switching loss model, losses incurred with various switching techniques, Turn-On loss models, Turn-Off loss models and thermal stress analysis is readily available [77-87].

4.1.1 Evaluation of device losses with hard and soft switching

The two kinds of losses, which are usually of interest in the inverter, are:

- Switching losses
- Conduction losses

Switching losses in an IGBT comprise of Turn-Off and Turn-On and diode losses.

4.1.2 TURN-OFF Losses

The hard switching turn-off and turn-on models of IGBT are well known and discussed in [77, 88-93] and [77-79]. Using the model equations are formulated to show the possible reduction in losses resulting in proposed inverter topologies.

Figure 4.1 IGBT Turn-Off losses: (a) Turn-Off loss model (b) Turn-Off characteristics [72], [84] and [75]

The current through the device I_T during the turn-off is usually an exponential decay, expressed as

$$I_T = I_0 e^{\frac{-t}{T}} \quad (4.1)$$

Where, T is the decay constant, and I_{T0} is the current through the device at t_0 which is equal to the load current I_0 . But for simplicity in analysis we consider a linear relation as shown in Eq. (4.2).

For $t < t_0$,

$$I_T = I_0.$$

For $t > t_0$,

$$I_T = I_0 - (\text{Rate of change of current through IGBT} * \text{Time lapse})$$

$$I_T = I_0 - \left[\left(\frac{I_0 - I_{tl}}{t_f} \right) (t - t_1) \right] \quad (4.2)$$

t_f is the total fall time $t_f = t_3 - t_0$

If C_p is the parasitic capacitance of the device, the voltage V_T across the device during the interval t_0 and t_1 be can written as shown in Eq. (4.3)

$$\begin{aligned} V_T &= \frac{\Delta Q}{2C_p} \\ &= \frac{di \cdot dt}{2C_p} = \left(\frac{I_0 - I_{tl}}{2C_p t_f} \right) (t - t_1)^2 \end{aligned} \quad (4.3)$$

The power loss P_{fall} during the interval t_1 to t_2 is given by Eq. (4.4)

$$\begin{aligned} P_{fall} &= \int_{t_1}^{t_2} V_T dI_T \\ &= \left[I_0 - \left(\frac{I_0 - I_{tl}}{t_f} \right) (t - t_1) \right] \left[\left(\frac{I_0 - I_{tl}}{2C_p t_f} \right) (t - t_1)^2 \right] \end{aligned} \quad (4.4)$$

The energy lost during this interval, E_{fall} is calculated by Eq. (4.5)

$$\begin{aligned} E_{fall} &= \int_{t_1}^{t_2} P_{off} \cdot dt \\ &= \frac{t_f^2 (I_0 - I_{tl})(I_0 + 3I_{tl})}{24C_p} \end{aligned} \quad (4.5)$$

The time interval $t_2 < t < t_3$ is the tail time, the losses during interval constitute for higher percentage of turn-off losses.

The power during the tail time P_{tl} is given by Eq. (4.6)

$$\begin{aligned} P_{tl} &= I_T V_s \\ &= I_T V_s \left(1 - \frac{t-t_2}{t_{tl}}\right) \end{aligned} \quad (4.6)$$

The energy loss during the tail time E_{tl} is calculated by Eq. (4.7)

$$\begin{aligned} E_{tl} &= \int_0^{t_{tl}} P_{tl} dt \\ &= \frac{1}{2} I_{tl} V_s t_{tl} \end{aligned} \quad (4.7)$$

The total energy loss is given by the summation of energy loss during fall time and during tail period. By adding Eq. (4.5) and Eq. (4.7) we get Eq. (4.8) representing the instantaneous total energy loss E_{off} .

$$\begin{aligned} E_{off} &= E_{fall} + E_{tl} \\ E_{off} &= \frac{t_f^2 (I_0 - I_{tl})(I_0 + 3I_{tl})}{24C_p} + \frac{1}{2} I_{tl} V_s t_{tl} \end{aligned} \quad (4.8)$$

The losses occurring during the tail time are predominant and constitute up to 65% of the total turn-off losses occurring. The tail time even prolongs the turn-off time, hence becomes an important factor during the design of drive circuit. When the switch is operated at zero current condition as shown there is no tail current.

$$I_{tl} = 0$$

The energy loss E_{Total} will now have only the first term in Eq. (4.8) with $I_{tl}=0$, as shown in Eq. (4.9).

$$E_{off} = \frac{I_0^2 t_f^2}{24C_p} \quad (\text{usually around } 2\text{mJ}) \quad (4.9)$$

The fall time in case is less than that compared to hard switching. Hence the energy loss is even more reduced. Usually the fall time is around $0.1\mu\text{s}$ and tail time around $3\mu\text{s}$.

4.1.3 TURN-ON Losses

For $V_T < V_{TH}$,

When the gate pulse is applied, V_{gE} rises exponentially because of the presence of gate-emitter capacitance C_{gE} . The power during this period occurs in the form of stored charge in the capacitor. In Figure 4.2 the IGBT turn on model and characteristics are presented. The gate to emitter voltage variation as a function of time is given in Eq. (4.10)

$$V_{gE} = V_{gg}(1 - e^{\frac{-t}{\tau_g}}), \quad \tau_g = R_g C_g \quad (4.10)$$

The energy loss is the energy stored in the capacitor $E_{C_{gE}}$ is given by Eq. (4.11)

$$E_{C_{gE}} = \frac{1}{2} C_{gE} V_{gg}^2 \quad (4.11)$$

The initial off-state is assumed to zero. Hence V_{gg} is the max voltage across gate and emitter.

For $V_T > V_{TH}$,

As the gate voltage reaches the threshold value (V_{TH}) the collector voltage starts decreasing at a rate $\frac{-dv_c}{dt}$ and the load starts to increase at a rate $\frac{di_c}{dt}$. The collector current I_c increases as the diode reverse recovery current also flows into the circuit. The max current through the switch is $I_c + I_{rr}$. The change in current during this interval is major cause for high Turn-On losses.

The rate of increase of collector current can be assumed to be linear through the inductor L_s as shown in Eq. (4.12).

$$\frac{dI_c}{dt} = \frac{V_{CC} - V_{CE}}{L_s} \quad (4.12)$$

(a)

(b)

Figure 4.2 Turn –On Characteristics of IGBT: (a) IGBT Turn-On characteristics (b) IGBT Turn-On Loss Model [69], [70] and [72]

The energy loss during turn-on period is given by Eq. (4.13)

$$E_{ON} = \int_{t=0.1 I_{cc}}^{t=0.1 V_{cc}} I_c(t) V_{cE}(t) dt \quad (4.13)$$

During zero-switching conditions the losses can be minimized to a great extent as there would be no collector current and the only current present would be the diode reverse recovery current I_{rr} as shown in Figure 4.3.

$$E_{ON} = \int_0^{t_{ON}} I_c(t) V_{cE}(t) dt \quad (4.14)$$

The losses reduction can mainly be attributed to very low I_{rr} when compared to $(I_c + I_{rr})$ and lower value of V_{CE} . The energy lost during the voltage rise in C_{gE} is device phenomenon and comparatively small. The turn-on time decreases as there is no negative voltage being applied to the diode as in the case of hard switching. Hence, the recovery time decreases increasing the speed to operation of IGBT without additional losses.

The total switching losses constitute the turn-on losses and turn-off energy losses. The expression for total energy losses can be obtained by using Eq. (4.9), Eq. (4.14) in Eq. (4.15)

$$E_{sw} = E_{on} + E_{off} \quad (4.15)$$

If T_d is the duty ratio and f_c being the switching frequency of the switch, then the switching power loss for that particular switch can be written as

$$P_{off} = E_{sw} \cdot T_d \cdot f_c \quad (4.16)$$

Figure 4.3 IGBT turn-On transitions in ZCS inverter

4.1.4 Conduction Losses

The conduction losses arise due to the ON-state voltage drop of the device and are calculated by using Eq. (4.17).

where, V_{ON} – ON-State voltage drop, $I_L(t)$ - Instantaneous Load Current

$1/T_c$ – Fundamental switching frequency

$$P_{cond} = \frac{1}{T_c} \int_0^{T_c} V_{ON}(t) I_L(t) dt \quad (4.17)$$

$$V_{ON}(t) = V_{bias} + r_{ON} \cdot i_L(t)$$

Hence, the conduction losses can be expressed as

$$P_{cond} = \frac{1}{T_c} \int_0^{T_c} (V_{ON} + r_{ON} \cdot I_L(t)) I_L^k(t) dt \quad (4.18)$$

‘ k ’ is the curve fitting constant.

By the use of zero current switching technique, converter could be optimized by selecting IGBTs of much lower threshold value and hence much lower forward voltage drop and on-

Figure 4.4 Comparison of instantaneous device losses incurred: (a) Instantaneous device losses in proposed ZCS inverter device losses (W) (b) Instantaneous device losses in conventional PWM inverter

state resistance. Therefore, a considerable amount of loss reduction is possible. The reduction in ON-state losses directly influence the size of heat sink required. In Figure 4.4, the instantaneous device losses in conventional and PWM inverter are presented. The average loss in a given time interval is lower in ZCS inverter compared to PWM inverter. Conduction losses constitute a major portion of total losses in the proposed ZCS inverter.

Fuji Electric-2MBI100TA-060 IGBT is used for analyzing the losses resulting due to hard switching and soft switching of the topologies explained above. This motivates us to explore various other features the topologies have to offer.

4.1.5 Zero Voltage Switching in ZCS Inverter

The above discussion provides an insight on switching loss reduction possible with the proposed topologies and zero-current switching concept. This provokes one to operate at higher frequencies and obtain equally good performance and quality power. In this section we now examine the possibility of losses actually occurring and draw interesting conclusions regarding the relation between switching frequency and switching losses.

Figure 4.5 Gate Pulse to an inverter switch

Consider Figure 4., the gating pulse, voltage and current waveforms pertaining to one inverter switch are shown. 'AND'ing zero-current switching signal (ZCSS) and Sinusoidal Pulse Width modulated signal (SPWM) as shown in Figure 4., generates the switching sequence for any particular inverter switch (Topology-1 and Topology-2).

Figure 4.6 Zero Voltage Switching in Proposed ZCS inverter

As shown in Figure 4.6, the switching scheme of the any particular inverter switch in the proposed ZCS inverter topology is classified into two recurring time intervals L_1 and L_2 . In the time interval, L_1 - current through the inverter switch is discontinuous and follows the switching scheme. In conventional PWM inverter topology, when the current is decaying

through the inverter switch the voltage rises. However, in the proposed ZCS inverter topology in the region L_1 the voltage is zero irrespective of current being discontinuous. During this time interval, no voltage rise is seen and thus achieving a Zero voltage switching as well. Hence, no switching losses are incurred during the time interval L_1 . During the time interval L_2 - the current through the inverter switch decays to zero and voltage rises. However, switching losses are incurring during the transition of recurring time intervals L_1 and L_2 . The switching losses during time interval L_2 are minimal compared to the switching loss in conventional PWM inverter.

On observing Figure 4.5 and Figure 4.6 we can infer that the envelope/contour of switching sequence of the inverter switch is determined by SPWM signal while operating states (ON/OFF) are determined by the ZCS signal. This can be easily observed by magnifying on time scale as shown Figure 4.6. A particular section of the waveform is presented in Figure 4.7. Observing voltage waveforms in Figure 4.7, we can note that voltage (DC-link voltage) is impressed upon the switch only when the SPWM signal is LOW and not actually every time when the switch is OFF (open). When SPWM signal is HIGH, there is no voltage impressed upon the switch (refer Figure 3.10 for switching Sequence of the Inverter Switch and Voltage across the switch waveforms). Examine the following two cases:

- (i) When SPWM signal and ZCS signal are HIGH, the inverter switch operates beyond the limits of current pulse entering the inverter and zero-current switching operation is achieved. As the inverter switch is ON there no voltage impressed upon it.
- (ii) When SPWM signal is HIGH and ZCS signal is LOW, the inverter switch is off and dc-link voltage is impressed across the inverter switch. During this particular interval the partitioning cell switch (SW_1/SW_2) is open which implies that during this interval the inverter is not actually part of power circuit and hence no voltage is impressed upon the switch. Therefore, ZVS operation is achieved.

Hence, inverter switches are operating (ON/OFF) at zero-current and zero-voltage. This is a unique feature of the proposed topologies. The switch operates under complete loss-less condition when SPWM signal is HIGH. When SPWM signal is low the inverter switch is

OFF and DC-link voltage is impressed upon the switch according to the operation of partitioning cell switch as shown in Figure 4.5.

Figure 4.5 Zero voltage switching: (a) Voltage across the inverter switch (b) Gating pulse to the inverter switch

In Figure 4.8, we can observe that the possibility of power loss incurring is at the rising and falling edge of the SPWM signal. Turn-on losses can incur at the turn-on of SPWM and Turn-off losses can incur at the turn-off of SPWM. Therefore, it is inferred that the switching losses are no longer dependent on switching frequency of the inverter (high) switch but dependent only on carrier frequency of SPWM (low). This is an interesting conclusion as the switching losses are independent of switching frequency then the switches can be operated at a comparatively high frequency.

For a general 3-phase SPWM inverter, the power loss due to switching is given by

$$P_{loss\ 1} = E_{sw} \cdot T_d \cdot f_{sw} \quad (4.19)$$

Figure 4.6 Occurrence of Turn-ON and Turn-OFF Losses

E_{sw} is the energy lost due to switching losses and f_{sw} is the switching frequency. T_d is the duty ratio of the inverter switch. The carrier wave frequency is equal to inverter switch frequency in the case of conventional PWM inverter ($f_{sw} = f_c$).

From the Eq. (4.19), power loss is proportional to the square of the switching frequency as shown in Eq. (4.20)

$$P_{loss\ 1} \propto f_{sw}^2 \quad (4.20)$$

For the proposed inverter $f_c = 1.5$ kHz and $f_{sw} = 20$ kHz.

The switching power loss occurring in the proposed topology is independent of switching frequency of the switch but depends on carrier frequency.

$$P_{loss\ 2} \propto f_c^2 \quad (4.21)$$

The switching power loss scale occurring in proposed topology can expressed in terms of switching power loss occurring in general inverter topology as

$$\frac{P_{loss\ 2}}{P_{loss\ 1}} = \frac{f_c^2}{f_{sw}^2} \quad (f_{sw} = 33.33 f_c)$$

$$P_{loss\ 2} \approx 5.625 * 10^{-3} \cdot P_{loss\ 1}$$

The switching losses are reduced by an order of 3. Since the switching losses of the inverter no longer depend on inverter switching frequency the inverter can now operate at very high frequency.

Figure 4.7 Turn-ON and Turn-OFF Loss estimation: (a) No Turn-OFF Loss occurs when both partitioning cell switch and inverter turn-off at the same instant (b) Turn-OFF Loss occurs when both partitioning cell switch and inverter turn-off at the different instant (c) No Turn-ON Loss occurs when both partitioning cell switch and inverter turn-on at the same instant (d) Turn-ON Loss occurs when both partitioning cell switch and inverter turn-on at the different instant

As explained earlier the possibility of incurring switching losses is only at rising and falling edge of SPWM as briefed in Figure 4.6 and Figure 4.9. But this does not happen in every cycle. Though the switch is operating at zero-current condition due to the presence of SPWM, the pulse width of gate pulse to the inverter varies at the rising and falling edge of

the SPWM. Due to this zero current condition may not occur and turn-on and turn-off losses are incurred. But as the rise time and fall time are very small these losses are usually of insignificant amounts.

As an approximation we can conclude that switching losses occur only when

$$\frac{T_{on, PWM}}{T_{sw}} = n \neq Integer$$

Hence, the average switching power loss can be expressed as

$$P_{SW_Device} = 0.612 \times m_a \times (E_{on} + E_{off}) \times f_c \quad (4.22)$$

The following figures illustrate and explain the cause and occurrence of switching loss due to SPWM.

4.1.6 Loss Analysis Results-Three-phase inverter

A comparative analysis between a conventional PWM inverter and proposed ZCS inverter is presented in Figure 4.8. IRG4PC50KBPF is modeled in PSim for loss analysis. The rated power of the inverters modeled is 5kW. In Figure 4.8.a, comparison is made in terms of total losses, switching losses and conduction losses at various load conditions and frequencies are made. It has to be noted that the total power losses of the ZCS inverter also include the losses incurred in partitioning cell. Therefore, total losses of ZCS inverter are the sum of total power losses incurred in the partitioning and inversion stages. As shown in Figure 4.8.b, approximately 40-50% total loss reduction is achieved throughout the load range. This aids in reducing the size of the heat sink required, especially for transportation systems with fuel cells as a power source. Referring to Figure 4.8.c, it is noted that the switching losses in ZCS inverter are almost constant and relatively low when compared to that of conventional PWM inverter. There is a marginal increase in conduction losses in the ZCS inverter. This is due to the incorporation additional two partitioning cell switches. The increase in conduction losses is minimal compared to the gain achieved by switching loss reduction. The switching loss incurred in inverter cells is insignificant due to zero current switching. A considerable amount of switching loss is associated with partitioning switches

due to their hard switching nature. However, this switching loss is quite less when compared to that of hard switched PWM inverter as shown in Figure 4.8.d.

PWM_Loss: Total loss in conventional PWM inverter at a given frequency
ZCS_Loss: Total Loss in ZCS inverter at a given frequency

(a)

SW_ZCS: Switching loss in ZCS inverter, SW_PWM: Switching loss in conventional PWM inverter, COND_ZCS: Conduction loss in ZCS inverter, COND_PWM: Conduction loss in conventional PWM inverter

(b)

(c)

(d)

Figure 4.8 A comparative loss analysis between conventional inverter and proposed ZCS inverter: (a) Comparison of total losses (b) Comparison of switching and conduction losses for various frequencies (c) Comparison of switching and conduction losses with respect to load current (d) Summary of losses occurring at various switching frequencies in conventional PWM inverter and proposed ZCS inverter

4.1.7 Cost Comparative Analysis

In order to realize the potential of any modern day power converter, it is imperative to analyze its economic feasibility. Prominent methods for reliability prediction and cost optimization are presented in [94-98]. This section highlights the comparative study carried out to evaluate the competitiveness of the proposed ZCS converter in terms cost compared to the conventional PWM inverter. The proposed inverter has 14 switches in total while the conventional inverter has six switches. The switch utilization factor is lower in proposed ZCS inverter.

A minor cost comparative analysis is presented based on the assumption that the proposed ZCS inverter is retrofitted for a 1MW drive suiting marine propulsion system. The study considers major fundamental parameters such as typical operational device power loss, capital costs and additional fuel charges incurred due to power losses. The cost comparative study is presented in Table 4-1.

Table 4-1
Comparative cost analysis of ZCS and conventional PWM inverter

	Differential parameters		Costs incurred	
	PWM Inverter	ZCS Inverter	PWM Inverter	ZCS Inverter
Number of Switching Devices	6	14	\$11,229.36	\$26,201.84
Total Avg. Device Loss occurring At Load power of 1MW	7720 W	6280 W	\$11.92	\$5.34
Initial Capital Costs			\$13,711.08	\$27,115.48
Additional Annual Costs Incurred due to device power losses*			\$103013.5	\$46100.62
Effective Comparison of Costs incurred in1 Year			\$116724.58	\$73216.1
Effective costs incurred in 10 years			\$1,924,602	\$757,800

Note: All the calculations are made at a rated condition of 1MW

The analysis shows that despite the capital costs of ZCS being relatively higher, the effective expenditure over a year for PWM inverter is higher. The cost analysis shows that the proposed converter offers high potential in operational cost reduction despite the capital cost being higher. The proposed ZCS inverter would result in greater cost savings when cooling costs, reliability, redundancy, fault clearance costs, person-hour costs and component replacement costs are considered.

In addition, the proposed ZCS inverter is redundant, more reliable, higher durability due to lower average current and voltage stress on inverter cell switches due to zero current switching capability.

From the above the analysis it can be inferred that there is a drastic reduction in total losses incurring. The total losses occurring are reduced by 30-40%. Switching losses are reduced to minimum. There is a fractional increase in conduction losses. But this increase does not affect the critical gain obtained in reduction of total losses.

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4.2 Reliability Analysis of ZCS Inverter System

Reliability has been one of most important factors to consider for modern day power converters. The fact that most modern converters are innately complex makes reliability assessment ever so important. In this section various reliability parameters such as MTBF, failure rate, availability of ZCS inverter are compared to conventional PWM inverter. Markov analysis, MIL HDBK217F is considered for simple reliability prediction. Most reliability assessment techniques do not consider the structural configuration of the converter. Effort has been made to consider the parallel power path configuration of ZCS inverter and deduce figurative advantages over conventional PWM inverter

4.2.1 Reliability in Power Electronic Converters

Most power electronic converters are developed considering efficiency, performance and volume as paramount parameters. This approach lacks relevance to reliability and durability of the converter. The life span of any power system is reduced by the conversion system at the power stage [99]. Most of converter components such as semiconductor switches do not possess any innate detrimental mechanism. However, it has been known that electrolytic capacitors/batteries are the least redundant and short lived components [94, 100, 101]. For the development of any new power electronic converter system reliability assessment is deemed necessary earlier on to prevent any significant changes in converter configuration. In this section the reliability of ZCS inverter is predicted and compared with conventional 3-phase inverter. Wind-Chill Solutions software, MIL HDBK217, Markov analysis and parallel inverter reliability are the methods and tools used in this analysis.

4.2.2 Markov Analysis

Markov modeling is considered to be an effective reliability assessment tool, particularly during the design phase of the power electronic converter system. For any given system, a Markov model considers the number of possible states, transitions between each state and its respective failure rate [102]. The symbol ' λ ' denotes the failure rate parameter of the transition from State 0 to State 1 as shown in Figure 4.9. $P_j(t)$ the probability of the system being in a particular state ' j '. The probability of State 0 decreases at the constant rate λ , which means that if the system is in State 0 at any given time, the probability of making the

Figure 4.9 Markov model state diagram

transition to State 1 during the next increment of time dt is λdt . This shows that the probability of the next transition state is reduced by a factor of λ . The total probability of two states must be equal to 1. Hence it is inferred that the probability of state 1 increases at the same rate as the probability of state 0 decreases. The equations for a simple model are given as shown.

$$\frac{dP_0}{dt} = -\lambda P_0 \quad \frac{dP_1}{dt} = \lambda P_0 \quad P_0 + P_1 = 1 \quad (4.23)$$

The solutions for the above equation, with initial conditions $P_0(0) = 1$ and $P_1(0) = 0$ is as shown in Eq. (4.24)

$$\begin{aligned} P_0(t) &= e^{-\lambda t} \\ P_1(t) &= 1 - e^{-\lambda t} \end{aligned} \quad (4.24)$$

4.2.3 ZCS Inverter Reliability - Markov Analysis

The proposed ZCS inverter is a modular configuration consisting of both discrete semiconductor modules and whole converter units. Hence it is a prerequisite to consider the topological features and functionalities when evaluating the reliability of the proposed ZCS inverter.

This analysis is carried out by method presented in [94, 101, 103]. It is widely known that modular structures provide greater availability of power, more flexible, higher redundancy and reliable converter system over conventional single unit converter systems. In this analysis, by using Markov model, a comparative insight is presented in terms reliability and

availability of conventional PWM inverter and proposed ZCS Inverter system. Figure 4.11 shows the inverter systems considered for analogy.

Figure 4.10 Inverter module representation considered for Markov Analysis: (a) Inverter module representation (b) Inverter module representation considered for Markov analysis

The following assumptions are made throughout the analysis:

- a) The failure rate if each module and component is constant.
- b) The failure rate for discrete IGBT modules and whole of the inverter module are equal.
This assumption is made to consider for ease in numerical calculations and as well for fronting the worst case [101]
- c) When a modules/ components are damaged, the system is said to be working in degraded mode. When all the modules are operating, the system is running at rated condition.
- d) If the number of operating modules falls below two (<2), the system fails.

The failure rate of Inverter Module is given by δ_{ij} and the failure rate of IGBT module constituting the partitioning cell is given by λ_{ij} .

In Figure 4.10, the failure rate model considered for Markov analysis is shown. In Figure 4.10, a Markov state transition model is shown. The failure rates for possible degraded state are as well shown. Failure of inverter cells or partitioning cells causes the ZCS inverter to perform at a degraded state. Hence the factors responsible for failure are considered as the axis and a state transition model is determined. In Figure 4.10, the state (2, 2) represents the state when ZCS inverter is healthy and addressing the load without any power curtailment. The state (0, 0) occurs when both the partitioning cells and the inverter cells fail to operate. In this state there is no load power is supplied by the ZCS inverter. From the above figure, the state matrix for estimating the probability of each state is determined. The state space matrix is developed as shown in Eq. (4.27) to represent the operational behavior of the proposed system.

The failure rate probability of a particular state is given by Eq. (4.23)

$$\overline{P}_{i,j} = \frac{dP_{i,j}}{dt} = \sum_{i,j=1}^2 \pm \lambda_{i,j} P_{i,j} \quad (4.25)$$

Figure 4.11 Markov State Transition Model

For example, the probability of state (2,2), $P_{2,2}(t)$; will be the summation of degraded state probabilities of state (1,2) and (2,1) multiplied with respective failure rates as shown in Eq. (4.26). Similarly, the failure rate probability states are determined for every possible state, 6 states in this case as shown in Eq. (4.27).

$$\overline{P_{2,2}} = \frac{dP_{2,2}}{dt} = -2\lambda_{2,2}P_{2,2} - 2\delta_{2,2}P_{2,2} = -2(\lambda_{2,2} + \delta_{2,2})P_{2,2} \quad (4.26)$$

$$\begin{bmatrix} P_{2,2}^*(t) \\ P_{1,2}^*(t) \\ P_{0,2}^*(t) \\ P_{2,1}^*(t) \\ P_{1,1}^*(t) \\ P_{0,1}^*(t) \\ P_{2,0}^*(t) \end{bmatrix} = \begin{pmatrix} -2(\lambda_{2,2} + \delta_{2,2}) & 0 & 0 & 0 & 0 & 0 & 0 \\ 2\delta_{2,2} & -(\delta_{1,2} + 2\lambda_{1,2}) & 0 & 0 & 0 & 0 & 0 \\ \lambda_{2,2} & 0 & -(2\delta_{2,1} + \lambda_{2,1}) & 0 & 0 & 0 & 0 \\ 0 & 2\lambda_{2,2} & 2\delta_{2,1} & -(\delta_{1,1} + \lambda_{1,1}) & 0 & 0 & 0 \\ 0 & \delta_{1,2} & 0 & 0 & -2\delta_{0,2} & 0 & 0 \\ 0 & 0 & \lambda_{2,1} & 0 & 0 & -2\lambda_{0,2} & 0 \end{pmatrix} \begin{bmatrix} P_{2,2} \\ P_{1,2} \\ P_{0,2} \\ P_{2,1} \\ P_{1,1} \\ P_{0,1} \\ P_{2,0} \end{bmatrix} \quad (4.27)$$

where, $P_{i,j}$ is the probability of the system to be in stage (i, j) and $P_{i,j}^*(t)$ is the first derivative of the probability of the state (i, j) .

The reliability of the system to be operated without any degraded performance is given by Eq. (4.28). During faultless operation, there is only one existing state which is $P_{2,2}(t)$.

$$R(t) = e^{-2(\lambda_{2,2} + \delta_{2,2})t} \quad (4.28)$$

The probability of the system to operate at a degraded mode is given by the Eq. (4.29). The degraded mode considers only the states where the system is partially functional and still able to address partial load and hence the possible states are $P_{1,2}(t)$, $P_{2,1}(t)$, $P_{1,1}(t)$.

$$P_D(t) = P_{1,2}(t) + P_{2,1}(t) + P_{1,1}(t) \quad (4.29)$$

The total reliability of the system to operate in a degraded mode is now the summation of probability at no fault and probabilities of all degraded states as shown in Eq. (4.30)

$$R_T(t) = R(t) + P_D(t) \quad (4.30)$$

As the conventional PWM inverter consists of only one PWM inverter module, the reliability of the conventional system is given by Eq. (4.31)

$$R'_T(t) = e^{-(\lambda_{0,1})t} \quad (4.31)$$

From Eq. (4.31), the degraded mode probabilities can be calculated. Table 4-2 lists the failure rate parameters. A comparative analysis of system reliability performance of ZCS inverter and conventional PWM inverter is presented in Table 4-3. It is concluded that the due to the presence of modular configuration of the proposed system, it is more reliable. Availability of power during partial degraded state is a prominent factor that contributes to high reliability of the proposed system.

Table 4-2

ZCS inverter state probabilities

IGBT failure rate	Inverter module
$\lambda_{2,2} = 2.3 \text{ e-06}$	$\delta_{2,2}=2.3 \text{ e-06}$
$\lambda_{2,1} = 1.3 \text{ e-06}$	$\delta_{2,1}=1.3 \text{ e-06}$
$\lambda_{2,0} = 1.0 \text{ e-06}$	$\delta_{2,0}=1.0 \text{ e-06}$
$\lambda_{1,2} = 1.3 \text{ e-06}$	$\delta_{1,2}=1.3 \text{ e-06}$
$\lambda_{1,1} = 2.3 \text{ e-06}$	$\delta_{1,1}=2.3 \text{ e-06}$
$\lambda_{1,0} = 1.0 \text{ e-06}$	$\delta_{1,0}=1.0 \text{ e-06}$

Table 4-3

Comparison of ZCS and PWM inverter reliability

Time in years	Proposed inverter system			Conventional PWM inverter reliability %
	System Reliability R(T)%	Degraded state Probability %	Total reliability %	
5	67.77	25.26	93.03	90.72
10	45.16	42.34	87.5	81.97
15	38.35	35.35	76.7	74.224
20	30.39	31.03	61.42	59.203
25	13.07	27.03	40.1	39.25

4.2.4 ZCS Inverter - Parallel Inverter Reliability

As the demand for power increases, the role of power electronic converters in distributed generation systems increases. Thus in order to improve the overall system reliability it is important to improve the reliability of power conversion units. The proposed ZCS inverter has higher number of semiconductor switches operating in a parallel configuration at lower average current stress. Hence it is deemed appropriate to compare reliability of the proposed ZCS converter to conventional hard switched PWM inverters. Failure rate determination methods explained in MIL HDBK 217F are referred for reliability assessment of the ZCS inverter. The failure rate is assumed constant within a predetermined operating range of the converter. Similar procedure is carried out in IEEE standard 1240 [95, 101].

Using Military handbook, the failure rate of IGBT is calculated as shown in Eq. (4.32).

$$\lambda_p = \lambda'_b \left(\pi_E \cdot \pi_Q \cdot \pi_A \cdot \pi_S \cdot \pi_R \cdot \pi_C \cdot \pi_T \right) \quad (4.32)$$

Table 4-2
Failure rate of circuit components

Parameter	Factor	Failure rate
λ'_b	Basic Failure Rate	0.0022
π_E	Environmental Factor	3.0
π_Q	Quality Factor	2.4
π_A	Circuit Factor	NA
π_S	Voltage Stress Factor	0.82
π_{SW}	Soft Switching Factor	0.26
π_R	Rating Factor	3.9
π_C	Construction Factor	NA
π_T	Temperature Factor	21

By substituting the values in Table 4-4 in Eq. (4.32), the failure rate obtained for IGBT for soft-switching condition ' λ_{ps} ' is

$$\lambda_{ps} = 0.245 FITS$$

And the failure rate for hard switching ' λ_{ph} '

$$\lambda_{ph} = 0.895 FITS$$

A generalized inverter circuit shown in Figure 4.14 is considered for reliability analysis. The peripheral circuit components are considered in order to have a realistic evaluation. The failure rate for a three phase hard switched PWM inverter λ_{PWM_3Ph} is calculated as shown in Eq. (4.33).

Figure 4.12 Generalized inverter circuit

Table 4-3

Failure rates of components in generalized inverter circuit

Parameter	Component	Failure rate
λ_{ph}	IGBT	0.895
λ_1	DC-Link Capacitor	3.03
λ_2	IGBT diode	0.8
λ_3	Snubber	0.001
λ_4	Passive Filter Inductance	0.038
λ_5	Passive Filter Capacitance	0.87
λ_6	Voltage sensor	0.56
λ_7	Current Sensor	0.5
λ_8	Circuit Breaker	3.3
λ_9	Cooling System	1.36
λ_{10}	Gate Drive	1.0

*failure rate = number of failures per million hours

The failure rates for all the circuit components presented in Table 4-5 are substituted in Eq. (4.33).

$$\begin{aligned}
 \lambda_{PWM_3Ph} &= \lambda_1 + 6(\lambda_{Ph} + \lambda_2 + \lambda_3 + \lambda_{10}) \\
 &+ 2\lambda_4 + \sum_{i=5}^9 \lambda_i \\
 &= 25.87 \text{ failure} / 10^6 \text{ hours} = 0.2266 / \text{ year}
 \end{aligned} \tag{4.33}$$

The reliability index for ZCS inverter cannot be calculated by Eq. (4.33) as the proposed ZCS inverter incorporates a parallel inverter structure. Only one partitioning cell and one inverter cell operate at any particular instant. Hence, the second partitioning cell and inverter are considered as redundant blocks. The reliability analysis for parallel inverter configuration is explained in [97, 98].

The failure rate for the proposed ZCS inverter ‘ $\lambda_{ZCS'}$ ’ at any instant, considering only one parallel is in operation is calculated as shown in Eq. (4.34). The failure rate parameters listed in Table 4-5 are substituted in Eq. (4.34).

$$\begin{aligned}
 \lambda_{ZCS'} &= \lambda_1 + \underbrace{(\lambda_{Ph} + \lambda_2 + \lambda_3 + \lambda_{10})}_{\text{PartitioningCell}} \\
 &+ \underbrace{6(\lambda_{Ps} + \lambda_2 + \lambda_3 + \lambda_{10})}_{\text{InverterCell}} + 2\lambda_4 + \sum_{i=5}^9 \lambda_i \\
 &= 23.66 \text{ failure} / 10^6 \text{ hours} = 0.2072 / \text{ year}
 \end{aligned} \tag{4.34}$$

The obtained failure rate $\lambda_{ZCS'}$ represents the number of probable failures occurring if only one partitioning cell and one inverter cell were operated throughout. The failure rate of ZCS inverter considering parallel architecture of ZCS inverter is explained as follows. In parallel power conversion architecture, a total of $N+X$ converter, the system delivers required performance when N converters operate and X number of converters is considered

redundant. In case of proposed ZCS inverter $N=X=1$ at any instant as only two inverter cells are considered.

The system reliability function for a parallel configuration ' R_{N+X} ' is written as shown in Eq. (4.31), where ' R ' is the reliability of the single inverter system in this case.

$$R_{N+X} = \sum_{i=N}^{N+X} \binom{N+X}{X} R^i (1-R)^{N+X-i} \quad (4.35)$$

The failure rate of a parallel inverter system is written as shown in Eq. (4.36).

$$\lambda_{N+X} = \frac{1}{\frac{1}{\lambda_{ZCS}} \sum_{i=N}^{N+X} \left(\frac{1}{i} \right)} \quad (4.36)$$

For $N=X=1$, the failure rate λ_{ZCS} for the proposed three phase ZCS inverter is given by Eq. (4.37).

$$\begin{aligned} \lambda_{1+1} &= \frac{1}{\frac{1}{0.2072} \left(1 + \frac{1}{2} \right)} = 0.1381 \\ \lambda_{ZCS_3Ph} &= 0.1381 / \text{year} \end{aligned} \quad (4.37)$$

The mean time between failures for the two three phase inverters are given by Eq. (4.38).

$$\begin{aligned} MTBT_{ZCS_3Ph} &= \frac{1}{\lambda_{ZCS_3Ph}} = 7.25 \text{ years} \\ MTBF_{PWM_3Ph} &= \frac{1}{\lambda_{PWM_3Ph}} = 4.816 \text{ years} \end{aligned} \quad (4.38)$$

The repair rate of the inverter system is assumed to be 30 days; the expression for repair rate is given by Eq. (4.39).

$$\mu_r = 365/30 = 12.16 / \text{year} \quad (4.39)$$

The availability for the 3-phase PWM inverter system can be calculated using Eq. (4.40) and Eq. (4.39).

$$A_{PWM_3ph} = \frac{\mu_r}{\mu_r + \lambda_{PWM_3ph}} = 0.9832 \quad (4.40)$$

The overall availability of three phase ZCS inverter system is given by Eq. (4.41).

$$A_{ZCS_1Ph_{N+X}} = \sum_{i=N}^{N+X} \binom{N+X}{N} A^i (1-A)^{N+X-i} \quad (4.41)$$

For N=X=1, the calculated probability of availability for ZCS inverter system is given by the Eq. (4.42).

$$A_{ZCS_3Ph} = 0.9887 \quad (4.42)$$

Comparing Eq. (4.34) and Eq. (4.37), it is seen that failure rate of ZCS inverter is about 40% lower with respect to PWM inverter.

From Eq. (4.42) and Eq. (4.40) it is noticed that the probability of ZCS inverter system being available to address the load is higher than conventional PWM inverter. Under the similar operating conditions, the mean time between failures is about 34% lower in ZCS inverter when compared to PWM inverter as shown in Eq. (4.38). This in turn improves the mean time between failures in ZCS inverter. This feature reaps great economic benefits when translated into repair time costs.

4.3 Summary

The analysis here focusses on qualitative advantages of ZCS inverter over PWM inverter. ZCS inverter achieves a loss reduction of 40% compared to PWM inverter. These results in a lower overall heat generated due to power losses. The size of heat sink determines the overall converter size. In ZCS inverter, only the partitioning cell switches are hard switched and require liquid cooling system. The costs incurred in design and deployment of cooling system is greatly reduced. The other major advantages being the reduction in fuel costs incurred due to power losses. The operational costs are reduced by 35%. This compensates for the additional capital costs due to added switches. The capital gains would be more pronounced in the future as the fuel charges rise while semiconductors costs decrease.

The reliability analysis presents a comparative study of ZCS inverter and PWM inverter under various parameters and methods. It is inferred that ZCS inverter with its parallel power configuration is about 40% (Eq. (4.34) and Eq. (4.37)) more reliable than PWM inverter. The soft switching capability of ZCS inverter reduces the stress on inverter switches and improves their lifecycle.

Chapter 5 DC-Link Switching Analysis and Harmonic Peak Mitigation

The proposed ZCS inverter incorporates a unique set of partitioning cells. The partitioning cells play a key role in achieving zero current switching. The partitioning cell switches chop the input DC- current to the inverter. In this chapter the effects of switching of partitioning cells on DC-link is studied and compared to conventional inverter switching. Apart from that, the effect of inherent delay in the proposed ZCS inverter on switching harmonics is as well analyzed.

5.1 DC-Link Stability

Many inverter systems are constantly fed by uncontrolled rectifiers or by lines with lower power quality. The DC-link capacitors are usually used to:

- a) Compensate the difference in power levels
- b) Supply the input inverter current with pulse frequency
- c) Reduce the spread of harmonics
- d) Discharge during transient power peaks

The instability at the DC-link occurs as the inverter is seen as a negative resistance with respect to DC-link [104, 105]. Instabilities in DC-link are quite rare as the electrolytic film capacitors are oversized for a particular application. This increases the cost and size of the system, but aids in supplying transient power during ride through. But with larger capacitors, the recharging currents are large enough to damage the rectifier diodes. Many methods have been developed to address the instability of DC-link during voltage sag conditions [106-109].

The proposed ZCS inverter is promises a viable solution for high frequency operation of drive systems. The ZCS inverter incorporates a set of unique partitioning cells which

segregate the input DC link current allowing inverter cells to operate at zero current switching conditions. However, the partitioning cell switches are hard switched. This might cause a voltage ripple at the DC-link. Hence it is prerequisite that the voltage ripple at the DC-link due to the hard switching of partitioning be predicted.

5.2 Effect of Partitioning Cells on Input DC-Current

This section focuses on the effect of switching of partitioning cell switches and the dependence of harmonics generated on the switching parameters. The switching phenomenon of partitioning cells is examined with respect to hard switching in conventional PWM inverter and similarities of analysis carried out are highlighted. The mathematical expression of input DC current to the inverters is obtained. Both the PWM and ZCS inverters are modelled in PSim and prove the mathematical conclusions inferred. The proposed ZCS inverter does not necessarily inject any transients, but it is quite imperative to prove this through harmonic analysis of input DC current and compare with conventional PWM inverter.

The DC-link voltage (V_{dc}) fluctuation primarily depends on the switching strategy of inverter switches and the switching frequency. In order to investigate the voltage fluctuation, the input DC-link current to the inverter has to be determined. The expression for DC-link current gives a better insight on the RMS values and harmonic components existing. The expression for input DC-link current for ZCS inverter ($I_{dc} = I_{dc1} + I_{dc2}$) is obtained by multiplication of load current of a particular phase current with its respective switching function. The load current being $I_0(t)$, and the average load current being I_0 for both the inverters. For the ease of analysis, we consider only a single phase. The switching function S_{A1} represents the switching state of switch A_{1pwm} in conventional PWM inverter as shown in Figure 5.1.

The input DC-link current can be expressed as shown in Eq. (5.1).

$$I_{PWM}(t) = S_{A1} * I_0(t) \quad (5.1)$$

Figure 5.1 Single leg/phase of a 3-phase PWM inverter

In Figure 5.2, a single phase of ZCS inverter with two parallel paths is presented. S_1 , S_2 are the partitioning cells and (A_{11}, A_{12}) and $(A_{21}-A_{22})$ are inverter cells switches of INV1 and INV2 respectively. The switches A_{11} and A_{21} operate with similar PWM signal formulation as A_{1pwm} . However, the operation is as well defined by switching strategy of corresponding partitioning cell switches.

The input DC-link current expression for ZCS inverter is expressed as shown in Eq. (5.2)

$$I_{dc}(t) = I_{dc1}(t) + I_{dc2}(t) \quad (5.2)$$

Where, I_{dc1} , I_{dc2} are given by Eq. (5.3) and Eq. (5.4)

$$I_{dc1}(t) = S_1 * S_{A1} * I_0(t) \quad (5.3)$$

$$I_{dc2}(t) = S_2 * S_{A1} * I_0(t) \quad (5.4)$$

Figure 5.2 A single phase of ZCS inverter

The above Eq. (5.2), Eq. (5.3) and Eq. (5.4) it can be inferred that the total DC-link current to the ZCS inverter can be expressed as a simple superposition of three phase legs signals generated by products of two time varying functions. The product of time varying functions in time domain is equivalent to convolution in frequency domain. The convolution operation determines the spectrum of the time varying functions.

As per theoretical understanding, the switching analysis of ZCS inverter and PWM inverter would be quite similar. In Figure 5.2, it is seen that when DC-link is supplying the load, current would take the path through the nodes (1-2-3-4). In this case, the number of hard switching switches is one. In Figure 5.2, the partitioning cell switches are rearranged to observe them as a part of inverter. The load current would take the path through the nodes (5-6-8-9-11) or (5-6-7-10-11). The switching operations of S_1 and S_2 are complementary in nature. The switches A_{11} , A_{21} are soft switched. In either case, the number of hard switching switches in ZCS inverter is as well one. Hence, the switching analysis of ZCS inverter is quite similar to that of PWM inverter except for the change in frequency and switching strategy.

A lot of research work has been published over the years concerning the spectral analysis of PWM switching signals [110-113]. The general form of PWM signals with harmonic components is shown in Eq. (5.5).

$$s(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} \left[A_{0n} \cos(n\omega_0 t) + B_{0n} \sin(n\omega_0 t) \right] + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left[A_{mn} \cos(m\omega_c t + n\omega_0 t) + B_{mn} \sin(m\omega_c t + n\omega_0 t) \right] \quad (5.5)$$

The spectral coefficients are obtained by double Fourier integral evaluated for particular switching strategy and converter topology.

The convolution process for ZCS inverter in frequency domain takes the form as shown in Eq. (5.6).

$$I_{dc1}(\omega) = \underbrace{S_1(\omega)}_{ZCS_part} \otimes \underbrace{(S_{A1}(\omega) \otimes I_0(\omega))}_{PWM_part} \quad (5.6)$$

Figure 5.3 Switching Signals to S1 and S2

The switching pulses to S1 are shown in Figure 5.3. The Fourier transform of $S_1(t)$ is given by Eq. (5.7)

$$s_{1/2}(\omega) = d_p + \frac{1}{\pi} \sum_{n=1}^{\infty} \left[\frac{1}{n} \left(\cos(d_p n \omega_p) * \sin(n \omega_p t) \right) + \frac{1}{n} \left((1 - \cos(n \omega_p d_p)) * \sin(n \omega_p t) \right) \right] \quad (5.7)$$

The generalized expression of harmonics generated by SPWM signals is given in [114] is shown in Eq. (5.8).

$$S_x(t) = \frac{1}{2} + \frac{M}{2} \cos(\omega_0 t + \theta_{0x}) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left[\frac{2}{m\pi} \sin \left[(m+n) \frac{\pi}{2} \right] J_n \left(m \frac{\pi}{2} M \right) \times \cos \left(m [\omega_c t + \theta_{cy}] + n [\omega_0 t + \theta_{ox}] \right) \right] \quad (5.8)$$

where, M is the amplitude modulation index, ω_0 is the frequency of the sine wave (modulating signal), ω_c is the carrier frequency. The Fourier form of phase leg switched current of PWM inverter is expressed as shown in Eq. (5.9).

$$i_{pwm}(t) = \frac{a_{00}}{2} + \sum_{n=1}^{\infty} \left[a_{0n} \cos(n \omega_0 t) + b_{0n} \sin(n \omega_0 t) \right] + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left[a_{mn} \cos(m \omega_c t + n \omega_0 t) + b_{mn} \sin(m \omega_c t + n \omega_0 t) \right] \quad (5.9)$$

The harmonic coefficients are defined as shown in Eq (5.10),

$$\begin{aligned} a_{00} &= \frac{I_0}{2} [A_{01} \cos \phi + B_{01} \sin \phi] \\ a_{mn} &= \frac{I_0}{2} [(A_{m,n-1} + A_{m,n+1}) \cos \phi + (B_{m,n-1} + B_{m,n+1}) \sin \phi] \\ b_{mn} &= \frac{I_0}{2} [(B_{m,n-1} + B_{m,n+1}) \cos \phi - (A_{m,n-1} - A_{m,n+1}) \sin \phi] \end{aligned} \quad (5.10)$$

The carrier phase angle Θ_{cx} is typically set to zero for two level converters. The phase angle of the three phases would be 0, $-2\pi/3$ and $+2\pi/3$ respectively. For a conventional PWM inverter the DC-link current harmonics are obtained by convoluting PWM part in Eq. (5.6). The harmonic coefficients obtained after adding all the three phases are given in Eq. (5.11).

The resultant I_{pwm} has to be convoluted with $S_I(t)$ to obtain the current harmonics of the input DC-link current for ZCS inverter. Eq. (5.12), Eq. (5.13) and Eq. (5.14) represent the harmonic components present in the input DC link current $I_{dc1}(t)$ of ZCS inverter. Similarly, one can obtain the expression for current harmonics in $I_{dc2}(t)$. The superimposing $I_{dc1}(t)$ and $I_{dc2}(t)$, the harmonic spectrum of $I_{dc}(t)$ is obtained.

$$\begin{aligned}
 a_{00_{pwm}} &= \frac{3M}{4} I_0 \cos \phi \\
 a_{mn_{pwm}} &= \frac{I_0}{m\pi} \left[\cos \phi \left([m+n] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \cos \phi \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix} \\
 b_{mn_{pwm}} &= \frac{I_0}{m\pi} \left[\cos \phi \left([m+n] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \sin \phi \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix}
 \end{aligned} \tag{5.11}$$

It is interesting to notice the presence of the term d_p in harmonic coefficients of $I_{DC}(t)$. The fundamental component of $I_{DC}(t)$ does not contain the duty ratio term of partitioning cell. Hence, the magnitude of fundamental component is equal to that obtain in the PWM spectrum of conventional inverter. However, the n^{th} order harmonics of $I_{DC}(t)$ do retain the duty ratio term. It can be safely concluded that magnitude of harmonic components is a function of duty ratio of the partitioning cell switches. As the fundamental component does not vary, the peak output load line-line voltage does not suffer amplitude reduction. While the rest of the harmonic spectrum, would achieve amplitude reduction.

$$\begin{aligned}
 a_{00_{ZCS}} &= \underbrace{\frac{3M}{4} d_p I_0 \cos \phi}_{I_{dc1}} + \underbrace{\frac{3M}{4} (1-d_p) I_0 \cos \phi}_{I_{dc2}} = \frac{3M}{4} I_0 \cos \phi \\
 a_{0n_{ZCS}} &= \frac{1}{n\pi} \left(\cos(d_p n \omega_p) * \sin(n \omega_p t) \right) \frac{3M}{4} I_0 \cos \phi + \frac{1}{n\pi} \left(\cos(d_p n \omega_p) * \sin(n \omega_p t - \delta) \right) \frac{3M}{4} I_0 \cos \phi
 \end{aligned} \tag{5.12}$$

$$\begin{aligned}
 a_{mn_{ZCS}} &= \underbrace{d_p \frac{I_0}{m\pi} \left[\cos \phi \left(\left[m+n \right] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \cos \phi \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix}}_{I_{dc1}} + \\
 &\underbrace{d_p \frac{I_0}{m\pi} \left[\cos \phi \left(\left[m+n \right] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \cos \phi \cos \delta \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix}}_{I_{dc2}}
 \end{aligned} \tag{5.13}$$

$$\begin{aligned}
 b_{mn_{ZCS}} &= \underbrace{d_p \frac{I_0}{m\pi} \left[\cos \phi \left(\left[m+n \right] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \sin \phi \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix}}_{I_{dc1}} + \\
 &\underbrace{d_p \frac{I_0}{m\pi} \left[\cos \phi \left(\left[m+n \right] \frac{\pi}{2} \right) \right] \left[1 + 2 \cos \left(n \frac{2\pi}{3} \right) \right] \sin \phi \cos \delta \times \begin{bmatrix} J_{n+1} \left(m \frac{\pi}{2} M \right) \\ - \left[J_{n-1} \left(m \frac{\pi}{2} M \right) \right] \end{bmatrix}}_{I_{dc2}}
 \end{aligned} \tag{5.14}$$

This aids in great reduction of RMS value of the capacitor current. The higher the amplitude of the harmonics components, more would be the heat generated the capacitor terminals. To justify the mathematical analysis, both ZCS inverter and PWM inverter are modelled in PSim and investigated. The duty ratio of S_1 is d_p and the duty ratio of S_2 is $(1 - d_p)$ which is as well be written as ' $d_p \cos \delta$ '. The simulation results are presented below and justify the mathematical analysis.

Figure 5.4 Input DC current and its harmonic spectrum in ZCS and PWM inverter: (a) Input DC-link current comparison (b) Frequency spectrum of input DC-current (c) DC-Link capacitor current spectrum comparison (d) DC-link capacitor current comparison

In Figure 5.4, the harmonic spectrum of total dc-link input current and capacitor current is presented. The duty ratio of S_1 is 0.7. It can be easily inferred that the fundamental component of both ZCS and PWM inverter input current is same. However, the harmonic components and harmonic side bands tend to have higher amplitude peaks in the case of a PWM inverter. The reduction in harmonic peaks in ZCS inverter is due to the presence of partitioning cell switches and soft switching capability. The momentary delay infused in order to achieve soft switches avoids the current and voltage transients to peak. The delay cumulatively could be as well seen as a change in rise times and fall times of partitioning cell and inverter switches. The magnitude of any particular transient depends on the magnitude of change in parameter (current/voltage) and duration of this change to incur. The proposed converter achieves zero current and voltage switching. So, in a practical scenario, during a soft switching condition, the transients are caused due to switching with residual current or voltage. Such transients are usually very low in amplitude and are usually neglected. The by prolonging the rise and fall times, the slope of transient build up is low as well. This results in lower amplitude harmonics. The simulation results for other duty ratios of partitioning cell are presented.

Figure 5.5 DC-link switching analysis with partitioning cell switch duty ratio $D_p=0.7$: (a) DC-link capacitor current of ZCS and PWM inverter (b) DC-link current spectrum of ZCS and PWM inverter

In Figure 5.5, the DC-link switching analysis for a partitioning cell switch duty ratio of $D_p=0.6$ is presented. It is seen that the peak of the input DC current is lower in ZCS inverter. The peak of the input DC-link current is dependent on the duty ratio the partitioning cell switches. The peak current through the DC-link capacitors as well is dependent on the duty ratio of the partitioning cell switches as shown in Figure 5.6.

Figure 5.6 DC-link switching analysis with partitioning cell switch duty ratio $d_p=0.6$

5.3 Output Voltage Harmonic Reduction Due to Change in Device Switching Periods

This section investigates the feasibility of extending the application of zero current switching concepts so far dealt to multilevel inverters. Multilevel inverters have not yet captured a chunk of inverter market share, but they would steadily in the near future. Multilevel inverters are preferred in an environment where there are stringent restrictions on THD and EMI limits. As discussed earlier the proposed topologies achieve ZCS/ZVS by operating beyond the boundary limits of incoming current pulse. This implies that there exists a small lag and lead time for the switching pulse with respect to current pulse. From

Figure 5.7 A simple stepped waveform

the basic theory of selective harmonic elimination, we know that by changing the triggering angle ($\cos\theta_n$) the chosen harmonic is either reduced or eliminated. On similar front, we analyze the magnitude of various harmonics by changing the switching periods, which infuse a change in triggering angle of the inverter switches.

5.3.1 Simple Fourier Analysis

Consider a simple stepped waveform as shown in Figure 5.7. Fourier expansion for the waveform shown is

$$V(t) = \sum_{n=1}^{\infty} a_n \cos n\omega t + b_n \sin n\omega t \quad (5.15)$$

where, ' a_n ' and ' b_n ' are the Fourier coefficients given as,

$$a_n = 0$$

$$b_n = \frac{4}{T_s} \int_0^{T_s/2} f(t) \sin\left(\frac{2\pi n}{T_s} t\right) dt$$

The Fourier expansion of the voltage waveform can be calculated as:

$$V'(t) = \frac{4V_{dc}}{n\pi} \sum_{n=1}^{\infty} (\cos n\omega t_0) \sin n\omega t$$

The magnitude of harmonic voltages is given as shown in Eq. (5.16)

$$V'_n(t) = \frac{4V_{dc}}{n\pi} \cos n\omega t_0 \quad (5.16)$$

The change in magnitude of harmonic voltages due to change in switching angle is given by differentiating Eq. (5.16) with respect to t_0 ,

$$\delta'_r = \frac{dV'_n(t)}{dt_0} = \frac{-4V_{dc}\omega}{\pi} \sin n\omega t_0 \quad (5.17)$$

5.3.2 Fourier Analysis Considering the Switching Times

Figure 5.8 A Stepped waveform with Turn-On and Turn-Off periods

In usual analysis the switching periods are not considered as $(t_r, t_f \ll T_s)$. Where t_r is the Turn-On rise time, t_f is the Turn-Off fall time and T_s being the time period if the inverter switches. In this case, the switching frequency (f_s) is 20 kHz and hence the switching periods are comparable and cannot be neglected. In Figure 5.8, the waveform is shown with switching periods.

Hence, b_n now calculated as,

$$b_n = \frac{V_{dc} T_s}{\pi^2 n^2} \left[\frac{\sin\left(\frac{2\pi n}{T_s}(t_0 + t_r)\right) - \sin\left(\frac{2\pi n}{T_s}t_0\right)}{t_r} + \frac{\sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0 - t_f)\right) - \sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0)\right)}{t_f} \right] \quad (5.18)$$

Now the output voltage waveform is expressed as:

$$V(t) = \frac{V_{dc} T_s}{\pi^2 n^2} \left[\frac{\sin\left(\frac{2\pi n}{T_s}(t_0 + t_r)\right) - \sin\left(\frac{2\pi n}{T_s}t_0\right)}{t_r} + \frac{\sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0 - t_f)\right) - \sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0)\right)}{t_f} \right] \sin\left(\frac{2\pi n}{T_s}t\right) \quad (5.19)$$

The magnitude of the output voltage harmonics is given by,

$$|V_n(t)| = \left| \frac{V_{dc} T_s}{\pi^2 n^2} \left[\frac{\sin\left(\frac{2\pi n}{T_s}(t_0 + t_r)\right) - \sin\left(\frac{2\pi n}{T_s}t_0\right)}{t_r} + \frac{\sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0 - t_f)\right) - \sin\left(\frac{2\pi n}{T_s}(T_s/2 - t_0)\right)}{t_f} \right] \right| \quad (5.20)$$

Assuming $t_r = t_f$, the above Eq. (5.20) is rewritten as:

$$|V_n(t)| = \left| \frac{2V_{dc} T_s}{\pi^2 n^2 t_r} \left[\sin\left(\frac{2\pi n}{T_s}(t_0 + t_r)\right) - \sin\left(\frac{2\pi n}{T_s}t_0\right) \right] \right| \quad (5.21)$$

The change in magnitude of harmonic voltages due to change in switching angle is given by differentiating Eq. (5.21) with respect to t_0 ,

$$\delta_r = \frac{d|V_n(t)|}{dt_0} \quad (5.22)$$

As the numerical value of $\left(\frac{2\pi n}{T_s} t_r\right) \ll 1$, $\sin\left(\frac{2\pi n}{T_s} t_r\right) \approx \left(\frac{2\pi n}{T_s} t_r\right) = \omega_s t_r$ and $\cos\left(\frac{2\pi n}{T_s} t_r\right) \approx 1$

where, $\omega_s = \frac{2\pi n}{T_s} = n\omega$

And hence,

$$\delta_r = \frac{-V_{dc} T_s \omega_s^2}{\pi^2 n^2} \sin \omega_s t_0 \quad (5.23)$$

The ratio of Eq. (5.17) and Eq. (5.23) with $\omega_s = \frac{2\pi n}{T_s} = n\omega$ gives the ratio of rate change of peak magnitude with respect to rise time. The ratio as shown in Eq. (5.24), implies that rate of change of harmonic peak magnitude in ZCS inverter is twice slower than compared to regular PWM inverter without any induced delay as shown in Figure 5.9.

$$\frac{\delta_r'}{\delta_r} = \frac{\frac{-4V_{dc}\omega}{\pi} \sin n\omega t_0}{\frac{-V_{dc} T_s \omega_s^2}{\pi^2 n^2} \sin \omega_s t_0} = 2 \quad (5.24)$$

As the rate of change of magnitude is reduced, it implies that within a given constant switching time, the maximum achievable voltage peak is as well reduced. Hence, the harmonic voltage peaks are reduced by varying the switching time, which is case of ZCS inverter is the inherent delay.

Figure 5.9 Ratio of rate of change of magnitude in ZCS and PWM inverter

5.4 Simulation Results

Modeling of above-obtained mathematical expression Eq. (5.21) is carried out using MATLAB at 5 kHz, 10 kHz and 20 kHz switching frequencies. The results obtained were highly encouraging as a reduction harmonic peak is observed. Initial part of analysis was carried out without inducing any lead or lag time. Later we induce a lead and lag time of $t_r/2$. So in the latter case, the inverter switches are switched-on ($t_r+t_r/2$) earlier and switched-OFF ($t_r+t_r/2$) later. Here on, the lead and lag time are termed in one word as delay time for simplicity in understanding.

The proposed technique of achieving ZCS and ZVS minimizes the voltage stress on switches. This results a reduction in EMI. The simulation results presented encourage one to extend the proposed ZCS concept to multilevel inverters. The simulation results are presented as comparative study of two cases i.e., with and without delay time as discussed earlier.

The variation of peak harmonic magnitude of 3rd, 5th and 7th harmonics with respect to device rise time with and without induced is presented in Figure 5.10. The nominal rise times of IGBT's for inverter applications is about 2 μ s-4.5 μ s. Higher dead-time is usually used for high power and high current applications ($\sim >100$ kW)

There is no inherent or induced delay in the switching schemes of PWM inverters. Hence, the analysis without considering induced delay as presented Figure 5.11.a, Figure 5.11.c and Figure 5.11.e relates to the variations in peak harmonics occurring in a conventional PWM inverter. While the analysis presented in Figure 5.11.b, Figure 5.11.d and Figure 5.11.f

considers an induced or inherent delay. As mentioned earlier, ZCS inverter operates with an induced delay in order to achieve Zero current switching.

Figure 5.10 A simple stepped waveform considering switching times and induced $(t_r+t_r/2)$ delay time

Hence, the analysis presented in Figure 5.11.b, Figure 5.11.d and Figure 5.11.f relates to the variations in peak harmonics occurring in a conventional ZCS inverter. In Figure 5.11.a and Figure 5.11.b, a comparative analysis of the drop in nominal harmonic voltage (ratio of n^{th} order harmonic voltage to fundamental voltage) of the third order harmonic with respect to rise time and induced delay in rise time is presented respectively.

From Figure 5.11.b, Figure 5.11.d and Figure 5.11.f, it is noted that the nominal harmonic voltage tends to decrease at a faster rate for the proposed ZCS inverter when compared to possible harmonic peak reduction in conventional inverter configuration.

*Nominal Harmonic Voltage is the ratio of magnitude of n^{th} order harmonic to fundamental voltage waveform

Figure 5.11 Harmonic peak reductions due to change in switching times : (a) 3rd Harmonic Magnitude-PWM (b) 3rd Harmonic Magnitude- ZCS (c) 5th Harmonic Magnitude-PWM (d) 5th Harmonic Magnitude-ZCS (e) 7th Harmonic Magnitude-PWM (f) 7th Harmonic Magnitude-ZCS

5.5 Summary

The effect of switching of partitioning cell is similar to that of a PWM inverter switching at the same frequency. Due to soft switching capability of the all inverter switches, the transients arising due to such switching are minimal. The magnitude of harmonic components is lower when compared to that of PWM inverter. The RMS current through the DC-link capacitor is lower and hence aiding in less heating of capacitor bank. No additional control circuit is required to clamp the transient's peaks. The total number of switches possibly causing the transients in ZCS inverter is one, while it is two in PWM inverter.

Chapter 6 Control Aspects and Dead-Time Elimination Techniques in ZCS Inverter

This chapter details the performance characteristics of ZCS inverter and PWM inverter with well-known speed control techniques. As described in the previous chapters, ZCS inverter induces an inherent delay. The induced delay eliminates the need of additional dead-time and complexity involving it. Various aspects of dead-time and its effects on load current in ZCS inverter and PWM inverter are studied and comparative conclusions are drawn.

6.1 Effect of Dead-Time

As power electronic inverters with IGBT devices penetrate deeper into utility market, it is a prerequisite to design fault free switching and control strategies. Most of the inverter failures occur due to bridge shoot through, overheating due to high instantaneous current. The overlap of the current through the incoming and outgoing devices of the same phase is the prime reason for bridge shoot through. Practical IGBTs have inherent parasitic inductance, which prolongs the rise and decay of the load current through the device. As a result, additional power loss, fundamental voltage loss or even a thermal runaway are caused. In the worst case, failure of inverter switches leads to a complete system failure. In order to avoid shoot-through of inverter bridge switches, a small delay is given at the switching transition of outgoing and incoming switches. This delay is often referred to as dead time. The effect of dead time can be positive in terms of avoiding shoot through, but as well has adverse effects such as loss of the fundamental voltage, current/voltage waveform distortion and imbalance in common mode voltage as shown in Figure 6.1 for an LC load. The effect of dead time is predominantly seen during low power, low current and low frequency operation. This would result in very poor efficiency and performance, particularly in high power rated systems like marine propulsion systems.

Many dead time compensation, mitigation and elimination have been proposed [115-128]. Most of these techniques utilize an additional circuit or complex control algorithms to

Figure 6.1 Effect of dead time on output voltage wave forms

detect the direction of current at the zero crossing. This would require an accurate sensor at the motor terminals. Dead time elimination methods usually require additional isolated power supplies. In that case, two power supplies are required for each half bridge of a three phase inverter. The switching states of hard switching PWM inverter with dead time are explained in a sequential order in Figure 6.2. The effects of dead-time are elaborately explained in [115-117, 119-122, 124, 125, 127-129].

Figure 6.2 Switching states of PWM inverter with dead-time: (a) A+ is ON and A- is OFF

(b) A+ is OFF and A- is OFF (c) A+ is OFF and A- is ON

6.2 Switching States of ZCS inverter and Zero Crossing Transition

As mentioned earlier, the proposed ZCS inverter achieves soft switching without the use of any resonant tank. This is achieved by inducing a small delay between the operation of partitioning cell switches and inverter cell switches (ref to Section 3.2.3). This inherent feature acts as the buffer to avoid a bridge short through in the inverter cells.

It has to be noted that pulses for inverter cells switches are generated by logical AND'ing of PWM signals and ZCS signals with no actual dead-time introduced. No dead time is introduced during the operation of higher and subsequent lower side switch in the proposed ZCS inverter. The bridge short through is avoided as the partitioning cells are switched OFF before and after the instant of occurrence of switching transition between high side and lower side inverter cell switches of ZCS inverter.

The switching state transitions are explained in Figure 6.3. The pulses to partitioning cell switches are explained in detail in Chapter 3.2.3. The presence of dead time causes the load

Figure 6.3 Switching states of ZCS inverter: (a) P_1 is OFF, A_+ is ON and A_- is OFF (b) P_1 is ON, A_+ is ON and A_- is OFF (c) P_1 is OFF, A_+ is ON and A_- is OFF (d) P_1 is OFF, A_+ is OFF and A_- is ON (e) P_1 is ON, A_+ is OFF and A_- is ON (f) P_1 is OFF, A_+ is OFF and A_- is ON (g) P_1 is OFF, A_+ is ON and A_- is OFF

current to lag or lead depending on the direction of current. This in turn reduces the RMS value of the output power.

As the ZCS inverter does not need any delay compensation to avoid overlap, there is no lag or lead occurring in the load current as shown in Figure 6.4. In a hard switched PWM inverter, the load current through the inverter switch of a phase fluctuates at the instant of zero crossing. The distortion, thus caused at the zero crossing induces side band harmonics. Hence, no smooth transition occurs when the load current changes the direction.

Figure 6.4 Zero crossing of load current of ZCS and PWM inverter: (a) Phase current in PWM inverter without dead-time (b) Phase current with dead time in PWM Inverter (c) Phase current in ZCS inverter

Figure 6.5 Load current zero crossings: (a) Phase current in PWM inverter without dead-time (b) Phase current with dead-time in PWM inverter (c) Phase current with ZCS inverter

When dead time is induced, the voltage ripples are minimized and smoother zero crossing transition occurs. In Figure 6.5, the zero crossings of load current of PWM inverter with and without dead time and ZCS inverter through a particular inverter switch are presented.

In Figure 6.7, the output current waveform and its THD in PWM inverter with dead time and ZCS inverter at various lower speeds and power levels are presented. The effect of dead time on PWM inverter output current is more prominent than in ZCS inverter. The THD of the PWM inverter is about 6.94%, while that of ZCS inverter is 5.9%. The major advantage of ZCS inverter is the eliminating of the need of additional dead time and its control circuit.

Figure 6.7 Comparison of effects of dead time on PWM and ZCS Inverter at 0.15 p.u power: (a) Load current in PWM inverter (b) Load current in ZCS inverter (c) Speed Tracking in PWM inverter (d) Speed Tracking in ZCS inverter (e) THD in load current-PWM inverter current waveform (f) THD in load current-ZCS inverter

6.4 Effect of Dead-Time with Sensorless Control

A variety of motor drive applications use both sensor and sensor less vector control of induction motors. Sensor less control is usually utilized as an auxiliary control system in many vehicular systems [131]. The major advantages of sensor based control are 1) accurate measurement of position even at low speed 2) wide control ranges 3) better dynamic performance. The disadvantages are 1) added component cost and complexity 2) lower reliability and repair time [132]. Sensor less control addresses the limitations of sensor based control, but has poor performance during low speed operation. The comparative study of effect of dead-time between ZCS inverter and PWM inverter would be relevant for near to low speed operation (about 5% slip).

As mentioned earlier, the effect of dead time is more pronounced at low speeds. Hence the analysis was carried at low speeds which correlate the starting and ship maneuvering period speeds [126]. lists the load current waveforms of ZCS and PWM inverter at various speeds. ZCS inverter has inherent delay of 2us which acts as a dead time. While, in PWM inverter a deliberate delay time or dead time of 2us is introduced.

Figure 6.8 Sensor less Control of Induction Motors [126]

Table 6-1

Effect of dead time with sensor less control in ZCS and PWM inverters with induction motor load

N/p.u	PWM Inverter with dead time of 2 us	ZCS Inverter with induced delay time 2 us
Speed 60 RPM
Speed 48 RPM
Power 0.3 p.u
Power 0.2 p.u

The loss in linearity of PWM inverter results in the distortion of load current waveform. The inherent delay in ZCS inverter does not cause in any loss of linearity in PWM signals. These results in a lower distortion compared to conventional PWM inverter. The percentage distortion increases at a faster rate in PWM inverter than in ZCS inverter as the operational speed is lowered.

6.5 Experimental Results

In Figure 6.9, the experimental results of ZCS inverter with an induced delay of 2 μ s are presented. The results demonstrate the ability of ZCS inverter to produce smoother load current waveforms with an induced delay of 2 μ s. The load power is 0.2p.u.

Figure 6.9 Experimental Results of proposed ZCS Inverter configuration: (a) Current and gate signal-Inverter (b) Zero Current Turn-OFF (c) Zero Current Turn-ON

6.6 Summary

A comparative analysis in terms of control aspects of ZCS and PWM inverter is presented. The inherent delay in ZCS inverter eliminates the need of a dead time circuit. The ZCS inverter does not incur any loss of PWM linearity and hence resulting in a better load current waveform than PWM inverter. The simulation study presented with field oriented control and sensor less control demonstrate the ineffectiveness of dead time/delay to cause distortion in load current ZCS inverter. The experimental results of load current waveform obtained at a very low power without the use of dead time are satisfactory as well.

Chapter 7 Future Scope and Conclusion

This chapter presents key ideas of pursuing this interesting research in power inverters. The salient aspects of the research focusing on future research and applicability scope are discussed as well. Various methods to improve the efficiency and performance are highlighted. The salient features and inferences from the research work have been briefed leaving a scope for further analysis.

7.1 Conclusion

The energy demands and requirements of the modern society are ever increasing. High power electronics with high efficiency and safe operational features have paved the way to meet such high critical demand. With higher consumption of depleting fossil fuels, the percentage amount of CO₂ is increasing at a steep rate. Transportation sector is one of the highest in terms of CO₂ emissions. In order to reduce the consumption of fossil fuels, the power system could be made more efficient while integrating renewable energy. Power conversion systems play an important role in power system operations by connecting the end users to grid. Transportation industry requires the power conversion systems to be highly efficient, compact and light weight. Fundamental innovations in terms of configurational and operational changes are required in existing power electronic conversion systems to achieve such technological edge. The research work presented in this thesis attempts to provide one such solution.

Propulsion systems have come long way in past few decades, from direct engine propulsion to hybrid electric propulsion and now to full electric propulsion. Marine propulsion systems are traditionally thyristor based. However, these devices have found to be less space efficient, of poor waveform quality and limited operational frequency range. PWM converters with IGBT's as switching devices have addressed such limitations. The current power electronic converter systems are capable of operating up to 30 MVA. PWM converters have quickly replaced the thyristor based converters and have been instrumental in accelerating hybrid/electric propulsion in transportation systems especially marine.

PWM converters pose certain limitations such as current/ voltage distortion and high power loss due to switching of semi-conductor devices. Various control techniques and converters with different configurational features have been proposed to mitigate the above limitations. Soft switching converters, also called resonant converters have been quite successful in minimizing the switching power losses. Resonant converters incorporate a resonant tank circuit, which forces the current/voltage to zero, and during this time interval the semiconductor switches are operated. The most commonly known technique is ZCS. As the switches now incur minimal switching losses, the operational frequency can be increased resulting in a significant reduction of size and weight. With higher operational frequency, power quality and current regulation are improved as well. Due to these advantageous features resonant converters are widely employed in communication systems. However, resonant converters are not suitable for drive systems due to the presence of resonant tank, which increases the size and weight of the system and poor efficiency during non-resonant conditions. Resonant converters incur high circulating current losses and hence requiring more cooling equipment. The voltage across the passive elements in a resonant tank is twice the nominal value. This needs the switching devices to be rated twice higher than rated power. As the ratings of switching devices increase, the conduction losses would as well increase. Such limitations in resonant converters outweigh the advantages by an extent, particularly for wide load range applications. The research proposes a novel inverter topology which cumulates the advantages of PWM and resonant converters while mitigating and eliminating some of the limitations.

The initial attempt at proposing a novel inverter topology is to cumulate the merits of PWM and resonant converters. Zero current switching with PWM operation and elimination of resonant tank are two major features around which the new inverter configurations are proposed. Two novel inverter configurations, namely Topology-1 and Topology-2 have been proposed. The proposed inverter configurations carry out the power conversion process in two stages: Partitioning stage and Inversion stage. The fundamental operational idea is to partition the input DC current into discrete DC pulses and operate the inversion stage switches beyond the DC-pulses. In Topology-1, the partitioning cells are placed ahead of rectification stage. Topology-1 incorporates an individual rectifier unit for every

partitioning cell switch. This increases the number of devices and complexity of the system. Topology-2 segregates the input DC current after the DC-Link. The DC-pulses are now fed as an input to the inverter cells. The operational features of inverter cells are no different from conventional PWM inverter. The switching function of inverter cell switches is obtained by AND'ing the ZCS signal and SPWM signal. This ensures the PWM operation while achieving zero current switching. Topology-2 is preferred over Topology-1 due to its immediate retrofit ability, lower number of switching devices, minimum complexity and ease of operation. Hence, Topology-1 is chosen for further investigation and has been referred to as "ZCS Inverter" later on. Single-phase and 3-phase analysis of both topologies have been presented with emphasis on Topology-2. The waveforms obtained by Topology-2 are similar to that obtained by a conventional PWM inverter.

Cost and power loss analysis are carried to validate the competitive ness of the ZCS inverter with respect to conventional PWM inverter, and as well highlight the advantageous features of ZCS inverter. ZCS inverter achieves zero current switching irrespective of load conditions. This results in ZCS inverter to incur minimal switching losses. While PWM inverter due to its hard switching nature suffers with high switching losses. This results in a requirement of additional cooling equipment. The ZCS inverter incurs additional conduction losses due to the added partitioning cell switches. But the gains in switching losses compensate thoroughly for the slight increase in conduction losses. ZCS inverter incurs 50% less total power losses as compared to conventional PWM inverter. A cost comparison has been made considering the capital costs, cooling requirements and power losses (fuel consumed). The overall cost incurred in ZCS inverter after one year of operation is 40% lower compared to PWM inverter.

Reliability is given paramount importance during the development and assessment of modern day systems. This is due to the fact that reliability is a direct index of safety, operational costs, availability and productivity. Hence, it is a necessity to predict the reliability of ZCS inverter with respect to PWM inverter. For reliability assessment and comparison, the prime factors that are considered are (1) type of configuration (2) operational behavior (3) system environment and its impact. The analysis has been carried

in three well known methods: (1) MILHDBK 247 (2) Markov analysis and finally the results from the above two methods have been verified by WIND CHILL solutions software. ZCS inverter employs a parallel power conversion architecture with high redundancy and availability. Markov analysis considers the topological configuration and operational features of converters in predicting the failure rates probability. The life-time of semiconductor switches primarily depends on the current/ voltage stress the switch has been exposed to. The soft switching nature of ZCS inverter improves the life span of semiconductor switches when compared to hard switching. ZCS inverter has been found to be 30% more reliable due to the above two factors.

The ZCS inverter incorporates partitioning cell switches switching at DC link. The partitioning cells switches segregate the input DC current to discrete DC pulses which are then fed to corresponding inverter cells. The DC-link capacitor current is a function of switching on the inverter side: partitioning cell switches in ZCS inverter. The ZCS inverter incorporates a unique inherent delay to achieve zero current switching. This inherent delay limits the harmonic peaks in capacitor current. The THD content in capacitor current is reduced by 20% and as well limiting the thermal losses in the capacitors.

In PWM inverters dead-time is employed to avoid the shoot through of the high voltage side and low voltage switches. This has detrimental effects on output current waveform particularly during low power operations. The ZCS inverter due to its inherent delay eliminates the need of dead-time. Analysis on load current waveforms in comparison to PWM inverter shows that THD is lower in ZCS inverter. The effect of dead-time with various inverter control techniques is investigated. The load current waveform obtained at different speeds and load power for ZCS inverter have lower THD content when compared to that of PWM inverter.

The work described in this thesis concerns with design and development of novel inverter configurations for drive applications especially related to marine industry. A new breed of inverter configurations has been proposed to overcome the limitations of conventional PWM inverters and soft switching inverters. A detailed investigation of the proposed inverter configuration regarding feasibility of the concept is presented along with prime

business case aspects. The tools, methods and mathematical models have been described in this research work and demonstrated with experimental results. The ZCS inverter proves its competitiveness with conventional PWM inverter. The ZCS inverter presents a novel soft switching technique with immense research scope to validate and demonstrate effective operation of inverters. The significant original contributions of this research work are:

1. Design and development of a novel tank-less non-resonant ZCS inverter.
2. The proposed inverter achieves zero current switching without the use of any sort of resonant tank or passive elements. The ZCS capability of the proposed inverter is independent of frequency and load variations
3. The ZCS inverter combines the advantages of soft switching and PWM inverters.
4. The proposed inverter is highly modular and the overall systems redundancy is improved
5. Due to the soft switching and modular characteristics of the proposed inverter, the failure rate of ZCS inverter is 40% (refer Chapter 3) lower compared to conventional PWM inverters
6. The ZCS inverter incurs minimal device switching loss. The total power losses incurred in ZCS inverter are about 40% of that incurred in hard switched inverter.

7.2 Recommendations for Future Work

Although the results presented herein prove the effectiveness of the ZCS inverter and its features, it could further be developed for various applications.

7.2.1 Induction Heating

Over the past two decades' induction heating has been attracting greater research interest due to specific features such as safety, zero residual waste, quick heating, high efficiency

and the wide utilization of power electronic converters. Induction heating is replacing conventional fossil fuel burning technologies in many industrial processes [133].

The success of IH is due to its added advantages such as accurate controlled heating and improved industrial process. Most of the industrial applications require IH to be robust and reliable since they are utilized intensively in a harsh environment. Induction heating technologies have evolved fast for versatile applications with higher reliability and lower cost, and making it ubiquitous. Major IH industrial applications are hardening, tempering, brazing, preheating acceleration of polymerization of glue for adhesion of metallic parts, sealing of aluminum covers for food products, melting applications, steam generators and diesel particulate filters as shown in Figure 7.1.

Typical operating frequency of domestic and industrial heaters is 20 kHz and 100 kHz. Most of the commonly known induction heaters employ Load resonant converters (LRC) as they are very well suited for high power applications. High conversion efficiency, low current and voltage stress and reduction in size are major advantages of LRC's. However, LRC's has major limitations such as difficulty in regulating the output voltage under light load or no load conditions. The ripple current/ripple voltage of the DC-capacitor is high as it is

Figure 7.1 High frequency Inverters in Induction Heating [128]

connected in series/parallel to the resonant switch. This poses a major issue for high load current applications [134, 135].

The proposed ZCS inverter is highly suitable for this application in terms of efficiency, robustness, operational ease and cost effectiveness. Induction heaters operate in environments where temperatures vary extremely. This results in change of dimensions of resonant tank elements. The dimensional change causes the inductance values to vary and hence alters the pre-determined resonant frequency. Such occurrence is eliminated in ZCS inverter and achieves ZCS irrespective of load condition.

7.2.2 Zero Current Switching in Modular Multilevel Inverters

With many industrial drives and power utilities demanding more power, major industries such as marine, transportation and production have opted for HVDC transmission systems. Voltage Source Inverters (VSI) and Current Source Inverters (CSI) with HVDC transmission have proven to be an economical solution [136, 137]. Marine and Electric vehicle industry is making rapid strides for a HVDC platform [138, 139]. Numerous recent research studies promise Multilevel Modular Converters (MMC) as a cost effective, reliable and safe solution for HVDC integration.

The major advantage of a MMC is the cascaded structure and redundant configuration. Due to the cascaded structure, the number of replicative functional states is reduced and hence improving performance and reliability. The other key advantages described in [138, 140] are listed here:

- a) Voltage balancing of DC-link capacitors is not critical
- b) Modular realization and easily scalable
- c) Lower switching losses and voltage stress and THD
- d) Low cost interface transformer can be used while harmonic filters are eliminated
- e) Flexible and easy failure management. The faulty cells can be replaced easily

In Figure 7.2, the structural configuration of MMC or M2C is presented [141]. The MMC's inherit the advantageous features of multilevel inverters without comprising on power quality. The major disadvantage of multilevel converters is number of semiconductor

devices needed, operational frequency limitation. Though the semiconductor devices are cheap, the gate drive circuits for each switching device that result in higher system cost [140].

Figure 7.2 Multilevel Modular Converter [141]

The proposed ZCS inverter has been explained in detail in Chapter-3. The proposed inverter achieves Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) without using any resonant technique. The parallel path power conversion and modular realization of the proposed inverter makes it redundant and more reliable than existing converters.

In Figure 7.3, the reconfigured ZCS inverter for multilevel output is presented. The major circuitual reconfiguration includes two interchanges.

The partitioning cell switch SW_2 is connected to the mid node (M) of DC-link capacitor bank:

QP $\rightarrow$ MP

The lower leg switches of INV_1 are connected to mid node of DC-link capacitor bank:

NN₁ $\rightarrow$ MN₁

Figure 7.3 Multilevel ZCS Inverter with simple interchanged configuration

The operation of the proposed multilevel ZCS inverter differs a bit when compared to ZCS inverter and conventional two-level inverter. The reconfigured multilevel ZCS inverter utilizes a simple parallel path power conversion process to synthesize a multi-level output voltage waveform. Unlike common NPC's architectures, the multilevel ZCS inverter is a redundant configuration due to its ability to deliver power in two modes i.e., 2L and 3L output. The key features of multilevel ZCS inverter are listed as follows:

Dual mode delivery of output voltage

- High redundancy- Full power can be delivered even under faulty conditions
- Retains the advantageous features of multilevel inverter and PWM techniques
- Achieves zero current switching irrespective of mode of operation and load type

- d) Lower in component count than its counterpart 3L NPC inverter
- e) Incurs lower switching losses and very low voltage stress due to soft switching capability

Phase AB-BA is considered for explaining the operational principle of Multilevel ZCS inverter. In ZCS inverter (ref. Chapter-3), INV1 and INV2 operate similar to conventional 2L inverter. The switches involved in AB-BA phase conduction are T_{11} , T_{13} , T_{14} and T_{15} from INV1 and T_{21} , T_{23} , T_{24} and T_{25} from INV2.

The pair inverter switches (T_{11} , T_{21}), (T_{13} , T_{23}), (T_{14} , T_{24}) and (T_{15} , T_{25}) operate with similar switching function. Switches from one of the inverter cells conducting phase AB-BA are enough for deducing a multilevel output voltage waveform. In Figure 7.4, the 2 level output voltage waveform of a conventional inverter is presented. The lower side switches conducting for V_{AB-BA} are T_{14} , T_{15} and T_{24} , T_{25} . In Figure 7.5, the gating signal to one of the lower side switches and its respective modulating sine wave is presented. \

In Figure 7.3, the reconfigured schematic for multilevel output is presented. The load voltage V_{AB} is $+V_{dc}$ when T_{11} , T_{15} are conducting. While load voltage is $+2V_{dc}$, if similar conduction state is imposed on switches T_{11} , T_{25} . This feature is aids in synthesizing multilevel output voltage waveform. The set of PWM pulses for lower side switches in INV1 and INV2 are multiplexed in such a way that a multilevel output waveform is synthesized.

In Figure 7.6, the dotted region R1 indicates the probable time interval to operate the lower side switches of INV2. The operation of higher side INV1 switches remains unaltered. While the lower side switches of INV1 are turned off. The gating pulses to the lower side switches of INV1 and INV2 are shown in Figure 7.6. The output waveforms for multilevel ZCS inverter are presented in Figure 7.7. Though the output load current waveform is not satisfactory, there is an immense scope for further development and improvement.

Figure 7.4 Line to Line output voltage and respective sine modulating wave of a 2L inverter

Figure 7.5 Gating pulse and respective modulating sine wave form

Figure 7.6 Regions indicating the time interval for INV2 lower side switches to operate

Figure 7.7 Output Load voltage and current waveforms of Multilevel ZCS Inverter

7.3 Research Takeaway

“Analysis and design of tank-less, non-resonant and low-loss zero current switching inverter”, has been carried under the supervision of Prof. Iftekar. Ali Maswood (NTU) in collaboration with Rolls Royce Energy Systems PVT Ltd. The project has been completed within the scheduled time and budget frame. A novel inverter system has been designed for marine application. The research work yielded in one US patent, two top level publications in IEEE acclaimed transactions and two publications in international conferences.

The technology developed was expected to achieve to reduce switching power losses and improved reliability. These concepts have been thoroughly investigated and market feasibility has been carried out. It has been noted that, despite the ZCS inverter being novel and achieving lower switching, lacks market competitiveness due to higher capital cost and utilization of more semi-conductor switching units. Hence, the development of commercial standard prototype has not been pursued. Various other supporting topics have been

examined to support the design and development of ZCS inverter. We thank Rolls Royce Energy Systems and MPA for their constant mentoring and financial support.

In summary, this research has presented a new approach to realize DC-AC power conversion. We have analyzed and investigated various aspects of the *proposed ZCS inverter* and its features. Many comparative conclusions have been drawn in favor of the ZCS inverter with respect to conventional systems. Such inference demonstrates the high applicability of the proposed ZCS configuration. This in turn would lead to broader practical impact in power electronic DC-AC converters by investigating and refining conversion strategies and configurations at a fundamental level. This research work has presented one such investigation in terms of design of development of light weight, cost effective, efficient and reliable power inverter systems for marine and other utility applications, and we believe there is much learning and progress to be made.

Author's Publications

Patents

“A novel and highly efficient tank-less and non-resonant inverter”, **M. Abhinava Chaitanya** and Iftekhar. Ali. Maswood, US Patents: 61/694,533/ NTU Ref: PAT/132/12/12/US PRV.

Transactions/Journals

1. M. A. Chaitanya, A. I. Maswood, M. Y. Lee and G. A. Kumar, “Realization of ‘more electric ships’ through a modular, efficient, tank-less and non-resonant inverter”, *Power Electronics, IET*, 2015, DOI: 10.1049/iet-pel.2014.0869.
2. M. A. Chaitanya and A. I. Maswood, “Reliability, dead-time and feasibility Analysis between a modular tank-less ZCS inverter and PWM inverter” Special Issue on Green Power Supplies, 2015, *IEEE PES Journal of Emerging and Selected Topics in Power Electronics*- Accepted.
3. O. H. P. Gabriel, M. A. Chaitanya, A. I. Maswood, and L. Ziyu, "Input current shaping of a novel three-phase/six-switch/five-level multiple-pole multilevel unity power factor rectifier," *Industry Electronics, IEEE Transactions*.

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1. M. A. Chaitanya and A. Venkataraman, "A Novel Highly Efficient Tank-Less Inverter for Transportation Applications," *International Transportation and Electrification Conference and Expo*, 2013.- Available on request.
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