Design of low power fractional-N phase locked loop for FMCW radar application

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DESIGN OF LOW POWER FRACTIONAL-N PHASE LOCKED LOOP FOR FMCW RADAR APPLICATION

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SUMMARY

High performance digital phase locked loops (DPLLs) have been proposed as alternatives to traditional phase locked loops (PLLs) based on analog charge pump. DPLLs offer several advantages over their analog counterparts. CMOS technology scaling also favors digital circuits over their analog counterparts. Despite offering significant advantages in area, manufacturability and programmability, the performance of DPLL is limited by performance of its key building blocks including time to digital converter (TDC), high resolution digital controlled oscillator (DCO) and high speed counter in counter-assisted DPLL architecture. In addition, frequency prescaler/divider is another indispensable component in high frequency phase locked loop (PLL) implementations and a major source of power consumption.

In this report, each of the building blocks of DPLL is studied and both circuit level and architecture level innovations and implementations are proposed for low power DPLL implementation.

Ring oscillator based injection locked frequency dividers (ILFDs) generally feature higher power efficiency compared to conventional static frequency dividers and can function as frequency prescaler/divider in high frequency DPLLs. However it is difficult for ring oscillator based ILFDs to achieve large division ratio and wide input locking range at the same time. To increase the input locking range, a ring oscillator based ILFD utilizing dual injection technique is proposed. A differential buffer circuit with dual injection paths is proposed. Equivalent circuit modelling of the dual injection buffer and mathematical analysis of locking range enhancement are provided. The core ring oscillator consists of 4 stages of the dual injection buffers. It has been fabricated in a 65 nm CMOS technology and consumes less than 2 mW with supply

voltage of 1.2 V. Its locking range is from 1.2 GHz to 20.7 GHz without any tuning at 0 dBm injection power level. The proposed ILFD is compact with the core only occupying $15\ \mu\text{m} \times 30\ \mu\text{m}$ and does not need any extra controls, which makes it suitable for integrated PLL.

To improve TDC performance, TDC based on parallel sampling ring oscillator with power gating and dynamic element matching (DEM) is proposed. It is capable of achieving sub-gate-delay resolution and large detection range at the same time with low power consumption. Through digital background calibration, the time resolution is determined by delay difference between successive sampling clocks instead of buffer delay. The ring oscillator is only enabled during the incoming time pulse width, leading to low power consumption. A new buffer circuit implementation which enables the ring oscillator to settle to a known position after the ring oscillator stops and to achieve immunity to leakage issues is proposed. For each incoming time pulse, the ring oscillator starts oscillation from the buffer before which the previous conversion stops, and thus it also achieves barrel-shift algorithm for dynamic element matching and mitigates buffer mismatch impact. The design has been fabricated in a 65 nm CMOS technology and occupies $0.4\ \text{mm} \times 0.3\ \text{mm}$ chip area. Measurements of the prototype IC demonstrate detection range of 98 ns with 6 ps per LSB. It consumes 280 μW from a 1.2 V power supply when operating at 1 MS/s sampling rate. The measured INL and DNL are 0.5 LSB and 0.1 LSB respectively. Measurements of the prototype IC also demonstrate single shot precision of less than 11 ps. The proposed TDC can be used for Time-of-flight (ToF) measurement by itself and used in DPLLs in which both low resolution and large detection range is needed. Furthermore, the parallel sampling technique can also be incorporated into other TDC architectures to further improve their performance.

A low power and wide-band FMCW (frequency modulated continuous wave) synthesizer based on DPLL approach has been proposed. Phase noise performance of this particular architecture is modeled and analyzed. The low power FMCW frequency synthesizer has been implemented in a 65 nm CMOS technology. With less than 9 mW power excluding output buffer power consumption, it achieves 3 GHz output bandwidth which corresponds to 5 cm ranging resolution in radar application. This work eliminates high resolution voltage digital-to-analog converter (DAC) by adopting DPLL architecture with current DAC. The gated delay line based TDC helps to reduce power consumption further. Furthermore it is easy to incorporate digital calibration scheme into this DPLL based architecture to achieve two point modulation over wide output bandwidth for faster modulation rate.

A low power and low jitter fractional counter-assisted DPLL architecture with ILFD and parallel sampling phase samplers is proposed. By sampling the ILFD's output phases, TDC function is achieved. Parallel sampling technique is adopted to further improve the TDC resolution. Due to injection locking, it is no longer necessary to carry out any calibration to normalize the TDC step to the DCO output period. Moreover, a hybrid counter architecture, which combines an asynchronous 2-bit counter and a 6-bit synchronous counter, is proposed to achieve low power consumption and high operating speed at the same time. The proposed design is fabricated in a 65nm process and the core occupies 0.1 mm^2 . The total integrated rms jitter is less than 0.43 ps with power consumption of 8.5 mW.

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Chapter 1. Introduction

In this chapter, a brief introduction of the emerging digital phase locked loop (DPLL) is provided and DPLL architecture is compared to traditional analog charge pump based phase locked loop (PLL) architecture. Next, research motivation is discussed and major contributions are described. Thesis organization is provided at the end of this chapter.

1.1 Background

The phase locked loop (PLL) is a critical component in electronic systems. Its applications include clock generation and distribution, clock recovery, jitter and noise reduction, spread spectrum signal generation, frequency modulation and demodulation, clock and data recovery, synchronization, skew compensation, frequency synthesis and spread spectrum signal generation [1]. PLL implementations have been dominated by analog charge pump based PLL designs due to their robustness.

1.1.1 Analog Charge Pump Based Phase Locked Loop Design

Implementation of traditional analog charge pump based fractional-N high frequency PLL is shown in Figure 1.1. In this architecture, the phase frequency detector (PFD) compares the reference clock and the divided clock and generates pulses which correspond to the phase error. Those pulses control the charge pump. The loop filter (LF) filters the charge pump (CP) output current and generates control voltage for the voltage controlled oscillator (VCO). The layout of an analog charge pump based 13 GHz fractional-N PLL [2] is shown in Figure 1.2. The chip area

measures $1.6 \text{ mm} \times 1.8 \text{ mm}$ in a 130 nm CMOS process and it can be observed that the analog loop filter occupies a big portion of it.

Figure 1.1 Analog fractional-N PLL

Figure 1.2 Typical analog PLL layout

In deep sub-micron technologies, the voltage supply becomes less than 1 volt. Consequently, it brings difficulties to analog circuit design due to less voltage headroom. Traditional charge pump based PLLs involve charge pump design which is analog intensive. As a result, traditional charge pump based PLLs face difficulties in advanced technologies less than 65 nm. In addition, the loop filter (LF) design in traditional analog PLLs involves large capacitance (~ 200 pf) which consumes big silicon area and faces problem of leakage and ground noise. Furthermore, integrating a charge pump based PLL within a digital chip is difficult and charge pump based PLLs are also more susceptible to noise and more vulnerable under process variations.

1.1.2 Digital Phase Locked Loop Design

In this section, concept of DPLL is briefly introduced to give an overview of this research area. High performance DPLLs have been proposed as alternatives to traditional analog PLL based on charge pump. DPLLs offer several advantages over their analog counterparts. Figure 1.3 shows the block diagram of a typical DPLL implementation. In DPLL structure, the PFD and charge pump are replaced by time to digital converter (TDC), the voltage controlled oscillator (VCO) is replaced by digital controlled oscillator (DCO) and the analog RC loop filter is replaced by digital loop filter (DLF).

Analog PLLs require large on-chip capacitors and the capacitor leakage problem usually degrades PLL performance [3]. Digital filter is very compact in deep sub-micron CMOS process and does not have problems such as leakage and ground noise. Furthermore, the frequency response of digital filter only scales with clock frequency and does not vary with process, temperature or voltage [4]. Moreover, TDC is adopted

to avoid analog-intensive components such as charge pump which becomes difficult to implement and operate under low power supply voltage in advanced nano-scale CMOS technologies [5]. Also, it is easier to perform digital calibration in DPLLs. CMOS technology scaling also favors digital circuits over their analog counterparts. In contrast, silicon area and power consumption of analog PLLs do not scale down with the technology process.

Figure 1.3 Fractional-N DPLL architecture

1.2 Research Motivation

Despite offering significant advantages in area, manufacturability and programmability, DPLLs rely on high performance TDC, high resolution DCO and low power frequency prescaler.

The first limitation is TDC design complexity and high power consumption. Phase detection is done using TDC in DPLLs. TDC with fine resolution and high linearity is usually of high complexity and incurs significant power and area overhead. TDC finite resolution will degrade DPLL performance by increasing in-band phase

noise level. Furthermore, in counter-assisted DPLL architecture, the TDC output has to be normalized to DCO output period, which requires precise calibration [6]. TDC nonlinearity and inaccuracy in period normalization creates spurs at the synthesizer output [7]. The most conventional TDCs quantize time using inverter or buffer delay and are able to achieve time resolution of 15-30 ps in CMOS technology [8]. Many other TDC architectures including vernier, time amplifier, and gated ring oscillator have been proposed. However, they either require high design complexity or high power consumption for the TDC design. It is highly desired to develop a low complexity and low power TDC with fine resolution.

The second limitation is low noise and low power DCO design. Fine frequency quantization of less than tens of kHz is required to achieve low output phase noise level for low GHz frequency band [9, 10].

Besides RF oscillator, frequency prescaler/divider is another major source of power consumption in high frequency DPLL implementations. Ring oscillator based injection locked frequency dividers (ILFD) generally feature higher power efficiency compared to conventional static frequency dividers [11, 12]. However it is difficult for ring oscillator based ILFDs to achieve large division ratio and wide input locking range at the same time. Wide locking range not only prevents the ILFD from unlocking due to PVT variations but also helps minimizing its internal phase noise contribution [13]. It is thus also desirable to develop frequency prescaler/divider with wide locking range and high power efficiency.

1.3 Major Contribution

To overcome these limitations, this thesis conducts a comprehensive study on each building blocks of DPLL: TDC, DCO, high speed counter, and frequency prescaler/divider. Major contributions are listed below:

To increase the input locking range, a ring oscillator based ILFD utilizing dual injection technique is proposed. Equivalent circuit modelling of the dual injection buffer and mathematical analysis of locking range enhancement are presented. The core ring oscillator consists of 4 stages of the dual injection buffers. It has been fabricated in a 65 nm CMOS technology and consumes less than 2 mW with supply voltage of 1.2 V. Its locking range is from 1.2 GHz to 20.7 GHz without any tuning at 0 dBm injection power level. The proposed ILFD is compact with the core only occupying $15\text{ }\mu\text{m} \times 30\text{ }\mu\text{m}$ and does not need any extra controls, making it suitable for integrated PLL.

To improve the TDC resolution without requiring additional power, parallel sampling technique is proposed. A TDC based on parallel sampling ring oscillator with power gating and dynamic element matching (DEM) has been designed. It is capable of achieving sub-gate-delay resolution and large detection range at the same time with low power consumption. Through digital background calibration, the time resolution is determined by delay difference between successive sampling clocks instead of buffer delay. The ring oscillator is only enabled during the incoming time pulse width, leading to low power consumption. A new buffer circuit implementation which enables the ring oscillator to settle to a known position after the ring oscillator stops and to achieve immunity to leakage issues is proposed. For each incoming time pulse, the ring oscillator starts oscillation from the buffer before which the previous

conversion stops, and thus it also achieves barrel-shift algorithm for DEM and mitigates buffer mismatch impact. The design has been fabricated in a 65 nm CMOS technology and occupies $0.4 \text{ mm} \times 0.3 \text{ mm}$ chip area. Measurements of the prototype IC demonstrate detection range of 98 ns with 6 ps per LSB. It consumes 280 μW from a 1.2 V power supply when operating at 1 MS/s sampling rate. The measured INL and DNL are 0.5 LSB and 0.1 LSB respectively. Measurements of the prototype IC also demonstrate single shot precision of less than 11 ps. The proposed TDC can be used for Time-of-flight (ToF) measurement by itself and used in DPLLs in which both low resolution and large detection range is needed. Furthermore, the parallel sampling technique can also be incorporated into other TDC architectures to further improve their performance.

A low power and wide-band FMCW synthesizer based on DPLL approach has been proposed for X-band FMCW radar application. Phase noise performance of this particular architecture is modeled and analyzed. The FMCW frequency synthesizer has been implemented in a 65 nm CMOS technology. With less than 9 mW power excluding output buffer power consumption, it achieves 3 GHz output bandwidth which corresponds to 5 cm ranging resolution in radar application. This work eliminates high resolution voltage DAC by adopting DPLL architecture with current DAC. The gated delay line based TDC helps to reduce power consumption further. Furthermore it is easy to incorporate digital calibration scheme into this DPLL based architecture to achieve two point modulation over wide output bandwidth for faster modulation rate.

A fractional-N DPLL architecture with ILFD and parallel sampling phase samplers is proposed. The proposed parallel sampling phase sampler based TDC achieves sub-gate-delay resolution with reduced hardware complexity and power

consumption. Due to injection locking, it is no longer necessary to carry out any TDC normalization. A low power hybrid 8-bit counter architecture is proposed to achieve high speed operation. The prototype occupies 0.1 mm^2 in a 65 nm CMOS process and consumes 8.5 mW. The measured rms jitter is less than 430 fs.

1.4 Thesis Organization

The rest of this thesis is organized as follows.

Chapter 2 introduces the basic concepts in DPLL circuit design. Firstly, two major DPLL architectures are reviewed. Design considerations of important DPLL building blocks including TDC, DCO, high speed counter and frequency divider are presented.

In Chapter 3, ILFD techniques are reviewed at the beginning. Next, proposed ring oscillator based ILFD using dual injection buffers are presented. Measurement results are discussed at the end of the chapter.

In chapter 4, TDC architectures are briefly reviewed. Then, TDC based on parallel sampling ring oscillator with power gating and dynamic element matching (DEM) is presented. Measurement results and discussions are given at the end of the chapter.

In Chapter 5, basic concepts in radar applications are briefly introduced at the beginning. Then, linear frequency modulation (LFM) waveform synthesizers are reviewed. Next, a low power FMCW synthesizer based on DPLL approach is presented.

Chapter 6 draws the conclusions and suggests future works.

Chapter 2. Design of Phase Locked Loops

2.1 Phase Locked Loop Design Parameters

There are several design considerations for PLL including: frequency range, frequency resolution, phase noise, spurious tones, loop bandwidth, and switching speed.

Frequency range is usually determined by its application. The PLL output tuning bandwidth has to be large enough to cover the operational bandwidth.

Frequency resolution is referring to the smallest frequency increment possible. For integer-N PLL, its step size equals to its reference frequency. For fractional-N PLL, its step size is determined by the width of its frequency control word (FCW). For example, the GSM cellular system requires a 200 kHz step.

Phase noise performance is a very important performance indicator of PLL. Generally speaking, the phase noise (jitter) of the synthesized clock signal degrades the signal-to-noise ratio (SNR). In high speed and high resolution analog-to-digital converter (ADC), input voltage signal is sampled at the rising edges of the sampling clock. Consequently, the actual sampling moment deviates from the ideal one by jitter in the clock, resulting in an error in the sampled voltage and SNR degradation [1]. For another example, phase noise level also affects adjacent channel power (ACP) in wireless communication system.

Periodic interference in PLL creates spurious tones, which are unwanted frequency components, at its output spectrum. Stringent requirement on spur level is imposed by modern RF communication systems.

The length of locking time indicates how fast the PLL is able to re-tune the VCO from one frequency to another. The switching speed is important in frequency hopping communication systems, which utilize channel or frequency hopping to mitigate effect of channel fading and interference. In addition, switching speed is also important time-division multiple access systems for transiting from one cell to the neighbouring cells.

Other parameters deal with power, size, programmability, temperature range and reliability. Low power consumption is critical for battery operated devices. Die size impacts the mass production cost. In modern deep-submicron CMOS process, SOC (system on chip) solution is usually provided and all RF, analog, and digital based band are integrated on single chip. It is important for the PLL to work under low supply voltage and be immune to digital switching noise. Lastly, it is also beneficial for the design to be easily transferred from one technology to another, which can shorten the design time and improve design portability.

2.2 Charge Pump Based PLL Design

2.2.1 Integer-N and Fractional-N PLL

In Integer-N PLL, its output frequency is integer multiples of its reference frequency. The reference frequency is thus usually selected to be the same as the channel spacing. A low reference frequency limited by the narrow channel spacing implies large division ratio and narrow loop bandwidth. As the reference phase noise is multiplied by the division ratio to the output, a large division ratio usually degrades phase noise performance. Narrow loop bandwidth is undesirable because of long switching times, inadequate suppression of the VCO phase noise, and susceptibility to supply and substrate noise [14].

Suppose that output channel is centred at 1 GHz with spacing of 200 kHz. And a 200 kHz reference clock is adopted. The divider ratio can be calculated as $1\text{GHz}/200\text{kHz} = 5000$. Consequently, the phase noise level of this low frequency reference clock will be multiplied by 5000 and transferred to the output. As the reference clock is only 200 kHz, the loop bandwidth of the PLL is limited to below 10 kHz (1/20 of the reference clock rate), and thus the switching speed also suffers. Furthermore, as the 200 kHz reference spur is near the loop bandwidth, the spur attenuation provided by the PLL loop bandwidth is also limited.

The above limitation can be resolved by adopting a Fractional-N PLL, in which the choice of reference clock rate is not limited by the channel spacing. In other words, a much higher reference frequency can be adopted, which implies a lower divider ratio and availability of large loop bandwidth. Lower phase noise can be achieved due to smaller divider ratio. Furthermore, a larger loop bandwidth can be chosen to satisfy switching speed requirement without sacrificing spur performance. Fractional frequency resolution is achieved by changing the divider ratio of a programmable divider dynamically. The dynamic control of programmable divider can be done through swallow counter or $\Delta\Sigma$ modulator.

2.2.2 Fractional-N Charge Pump Based PLL

Analog charge pump based PLL have been widely adopted in electronic systems. A typical implementation is shown in Figure 2.1.

Figure 2.1 Implementation of Fractional-N charge pump based PLL

The phase frequency detector (PFD) measures the phase difference between the reference input f_{ref} and the divided clock f_{div} and produces UN/DN signal whose width is proportional to the time difference measured. Tri-state PFD is a popular choice in charge pump based PLL implementation. Compared with mixers or XOR gates, the PFD can resolve phase differences in the $\pm 2\pi$ range. In phase detect mode, the charge pump is only active for a portion of each reference clock cycle that is proportional to the phase difference between the reference and divided clock signals. The PFD usually has a dead zone. In other words, when the phase error is too small, the PFD cannot detect it due to the gate delays and parasitics [15]. In practical design, the dead zone is avoided by turning on both the charging and discharging current sources during the reset time. As shown in Figure 2.2, a delay can be inserted purposely to increase the reset time.

Figure 2.2 Tri-state phase frequency detector

The outputs of the PFD control on/off of the charge pump. A practical implementation of push-pull charge pump commonly used in a PLL is shown in Figure 2.3. The NMOS bias voltage V_{BN} is generated by extra biasing circuit. When the charge pump output voltage V_{CP_OUT} varies, the charging and discharging current are modulated by the short channel length effect. Although long channel devices can be adopted to mitigate short channel length effect, large parasitic capacitance is introduced, which limits the maximum operation speed of the charge pump and degrades the transient response of the charge pump circuit. In contrast, the PMOS bias voltage V_{BP} is dynamically controlled using an operational amplifier to eliminate current mismatch between the charging and discharging current caused by short-channel length effect. The drain voltage of transistor MP3, MP4, MN3 and MN4 are forced to be the same by the operational amplifier. While the current mismatch caused by short channel length effect can be significantly reduced with adoption of the operational amplifier, the variation of the charge pump current with V_{CP_OUT} still remains [16] [17]. The variation of charge pump current causes loop dynamics to vary with different output frequencies and PVT corners [18]. Furthermore, there is still current mismatch caused by process variation among the four current mirror transistors MP3, MP4, MN3 and MN4. The output voltage swing of the charge-pump circuit is

The diagram shows a differential amplifier circuit. At the core is an OPAMP (Operational Amplifier) represented by a triangle with a '+' sign at the non-inverting input and a '-' sign at the inverting input. The OPAMP's output is labeled V_{cp_out} . The circuit is biased using a 'Bias circuit' block connected to the gates of NMOS transistors MN3 and MN4. The gates of MP1 and MP2 are connected to VDD, while the gates of MP3 and MP4 are connected to ground. The gates of MN1 and MN2 are connected to VDD, and the gates of MN3 and MN4 are connected to ground. The sources of MP1 and MP2 are connected to VDD, and the sources of MP3 and MP4 are connected to ground. The sources of MN1 and MN2 are connected to ground, and the sources of MN3 and MN4 are connected to VDD. The output of the differential pair is taken from the nodes between the OPAMP inputs and the gates of MN3 and MN4. The current flowing into the output node is labeled I_{dis_charge} , and the current flowing out is labeled I_{charge} . The biasing voltages V_{BP} and V_{BN} are indicated at the gates of MP3 and MN3, respectively. The output node is also labeled V_{cp_out} .

In addition to current mismatch, leakage current and timing mismatch also contribute to the output spurs [20]. The reference spur due to leakage current is possibly substantial in frequency synthesizers in deep-submicron CMOS process [21].

Leakage current problem becomes more severe in deep-submicron CMOS process, especially at high temperatures and fast process corners. The leakage current also depends on the drain to source voltage, which means that the charge pump output voltage strongly influences the leakage current. In traditional charge pump designs the leakage current could be as high as 5% of the operating current in a 0.13 μm process [18]. The timing mismatch is inherent in the PFD because UP and the DN outputs have to drive PMOS and NMOS switches [20].

The output current of the charge pump is filtered by the loop filter and produce the control voltage for the VCO. The capacitor of the loop filter needs to be large enough to make the PLL stable. A typical implementation of loop filter for a second order charge pump based PLL is shown in Figure 2.1. C_2 is an integrating capacitor and introduces a pole at dc. Another pole at dc is due to the transfer function of the VCO. To ensure loop stability and enough phase margin, a pole-zero combination introduced by R_1 and C_1 is added. The loop filter not only stabilizes the feedback loop, but also filters the current glitches generated by the charge pump and suppresses the high-frequency noise. The transfer function of the loop filter can be derived as below:

$$F(s) = \left(R_2 + \frac{1}{sC_2} \right) \parallel \frac{1}{sC_1} = \frac{sC_2R_2 + 1}{s(sC_1C_2R_2 + C_1 + C_2)}$$

$$= \frac{1}{C_1 + C_2} \frac{sT_2 + 1}{s(sT_1 + 1)} \quad (2-1)$$

$$\text{where } T_1 = R_2 \frac{C_1C_2}{C_1 + C_2}, T_2 = R_2C_2, \omega_z = \frac{1}{T_2}, \omega_p = \frac{1}{T_1} = \omega_z \left(1 + \frac{C_2}{C_1} \right)$$

The open loop transfer function of the PLL loop is given by:

$$G(s) = \frac{1}{N} K_d F_{LF}(s) \frac{K_{VCO}}{s} \quad (2-2)$$

Where N is the divider ratio, K_d is the phase detector gain and $K_d = I_{CP}/2\pi$, and K_{vco} is the VCO gain. For sufficient phase margin, the zero generated by the loop filter need to be placed before the close loop bandwidth ω_c and the pole has to be far away enough from the close loop bandwidth ω_c . For phase margin around 70 degree,

$$\frac{\omega_c}{\omega_z} = \frac{\omega_p}{\omega_c} = 6$$

is a good design choice.

To implement the passive loop filter, which occupies a large active area, either MOS capacitor or metal capacitor can be chosen. In general, the value of C_2 typically is much larger than C_1 and varies from 50 to 400 pF. The capacitor of the loop filter needs to be big enough to make the PLL stable, but it also has a large gate-tunnelling leakage through the MOS capacitor in the loop filter, which degrades the PLL performance in the nanoscale CMOS technology. It is preferable to implement C_2 using MOS capacitor because of its large capacitance density. However, the leakage current problem becomes more severe in deep-submicron CMOS technology. As the value of C_1 is much smaller than C_2 , it is ok to implement C_1 either using MOS capacitor or metal capacitor.

In deep-submicron CMOS process, power-supply is lowered to reduce the power consumption. The standard supply voltage has been scaled down from above 2.5 V to below 1 V. The gate-oxide thickness of the transistors becomes thinner and thinner to lower its threshold voltage and to be able to operate under low supply voltage. Consequently, large gate-tunnelling leakage appear in deep-submicron CMOS technology [22]. The gate-tunnelling-leakage varies with gate oxide thickness, transistor size and its voltage biasing. Table 2.1 summarizes leakage per unit area of NMOS and PMOS capacitors with different threshold voltage in a 90 nm 1-V CMOS process [22].

Table 2.1 Gate-tunnelling leakage in a 90-nm CMOS process

MOS Capacitor			
NMOS		PMOS	
Structure	Gate Tunnelling Leakage	Structure	Gate Tunnelling Leakage
Standard-VTH	1.11 nA/ μm^2	Standard-VTH	0.654 nA/ μm^2
High-VTH	0.764 nA/ μm^2	High-VTH	0.401 nA/ μm^2
Low-VTH	1.161 nA/ μm^2	Low-VTH	0.701 nA/ μm^2
Native NMOS	1.571 nA/ μm^2		

The leakage current in the loop filter creates voltage ripple on the control voltage, degrading jitter and spur performance of the PLL. In the worst case, it may make the PLL unlocked. According to [23], the leakage current is more than 1 mA for a 200 pF PMOS capacitor ($650\mu\text{m} \times 20\mu\text{m}$) in 65-nm CMOS technology.

As CMOS technology continues to scale, it is more difficult to design high performance analog PLL in deep-submicron CMOS technology for the following reasons:

- As the supply voltage continue to drop, it is more difficult to design high performance analog intensive components such as charge pump and operational amplifier (opamp) in deep-submicron CMOS.
- The severe leakage problem degrades charge pump and loop filter performance.
- As the integration level becomes higher, analog design is more susceptible to switching noise coupled from other parts of the chip.
- It takes a lot of effort to shift an analog PLL design between different technologies. In other words, analog PLL design lacks of portability.

In older technology, sufficient voltage resolution and signal-to-noise ratio (SNR) can be achieved with high supply voltage. However, it becomes difficult in deep-submicron process with reduced voltage headroom. Furthermore, switching noise of surrounding digital circuit also degrades the performance of analog intensive circuit blocks. In a deep-submicron CMOS process, transistors can switch much faster. Consequently, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals [24]. In deep-submicron CMOS process, the rise and fall time is on the order of tens of picoseconds, and thus it is easier to achieve good timing accuracy. TDC assisted ADCs utilize these advantages to achieved good SNR. Similarly, digital PLL implemented with TDC, digital loop filter and DCO is more suitable in deep-submicron CMOS process.

2.3 Digital PLL Design

2.3.1 Major DPLL Architectures

Two major types of DPLL architectures have been proposed and adopted for high performance fractional-N frequency synthesis as shown in Figure 2.4 [25, 26]. The divider-assisted DPLL architecture is similar to analog fractional-N PLL and it still employs programmable divider controlled by delta-sigma modulator (DSM) to achieve fractional frequency resolution. The divider-assisted architecture mirrors a traditional analog PLL component for component. The TDC replaces the PFD and charge pump in the analog PLL and DCO replaces the VCO. The digital loop filter replaces the analog RC filter. Unfortunately the DSM causes unwanted high frequency noise at the TDC input and the DPLL loop bandwidth has to be narrow enough to attenuate the high frequency noise [27]. The asynchronous multi-modulus divider in

the feedback path may also cause spurs [28]. Furthermore, TDC nonlinearity may fold the high frequency noise to fall within DPLL loop bandwidth.

Figure 2.4 Fractional-N DPLL architectures. (a) Divider-assisted DPLL (b) Counter-assisted DPLL

The other type counter-assisted DPLL does not need any programmable divider controlled by DSM and thus there is no introduction of unwanted high frequency noise. The TDC is moved to the feedback path and the output phase is quantized to digital code directly using combination of high speed counter and TDC. The integer part is obtained with high speed counter and the fractional part is obtained using TDC. This

architecture does not require any programmable divider controlled by DSM. However, the TDC resolution step has to be normalized to the counter input clock period, which incurs the need of more accurate calibration [6, 28] and performance degradation due to inaccurate normalization.

2.3.2 Design of Time to Digital Converter

The transfer function of TDC quantization noise to output phase noise is a low pass function. The in band phase noise of a DPLL is usually dominated by the quantization noise of the TDC. Consequently, fine resolution TDC is required to achieve low in band phase noise level. The in band phase noise contributed by TDC quantization noise can be calculated by the following equation:

$$PN = \frac{(2\pi)^2}{12} \left(\frac{\Delta t_{res}}{T_{DCO}} \right)^2 \frac{1}{f_{ref}} \quad (2-1)$$

Where T_{DCO} is the DCO output period, Δt_{res} is the TDC resolution and f_{ref} is the reference frequency.

2.3.2.1 Delay Chain Based TDC

The most conventional TDC is based on delay lines. The delay can be generated by inverter or buffer and the resolution of such kind of TDC is determined by the inverter or buffer delay. In typical CMOS implementation, it can achieve time resolution in the range of 15 ps to 30 ps. Table 2.2 summarize device parameters of a typical 90 nm CMOS process [29]. The minimum achievable delay is 15 ps, which will be further degraded by parasitic routing capacitance after layout.

Table 2.2 Device options in 90nm technology

TSMC Process	Low-Vt	Std-Vt	High-Vt
Vdd (V)	1.2		
Tox (nm)	22		
Ids ($\mu\text{S}/\mu\text{m}$)	540/250	420/180	370/130
C _j (fF/ μm^2)	1.3/1.2		
Gate delay (ps)	15	21	26

Figure 2.5 Buffer delay chain based TDC

Figure 2.5 shows the basic structure of the buffer chain based TDC. The input clock f_{div} is divided from DCO output and f_{ref} is the reference clock input. Each buffer provides delay equals to τ . At the rising edge of the reference input f_{ref} , all the flip-flops read the buffer output and latch the results. The input f_{div} waveform before the reference f_{ref} rising edge will be recorded in the flip-flops. From the recorded values, the time difference between the input f_{div} rising edge (nearest one before f_{ref} rising edge) can be decoded. Furthermore, the input time difference has to be normalized with respect to the input f_{div} period in counter-assisted architecture.

In [8], a TDC based on pseudo differential inverter delay lines is proposed as shown in Figure 2.6. Pseudo differential architecture helps to eliminate rise and fall delay mismatch of the inverter. The TDC output is in the form of pseudo-thermometer code, which is then converted to binary.

Figure 2.6 Pseudo differential delay chain based TDC

The major drawbacks for delay chain based TDC are coarse resolution and poor linearity. The resolution is limited by the achievable inverter or buffer delay. The linearity is limited by the mismatch between the inverter or buffer elements.

2.3.2.2 Vernier Delay Chain Based TDC

A vernier delay chain consists of two parallel inverter/buffer delay chains with slight delay difference. One chain is driven by the input signal f_{div} and the other is driven by the reference signal f_{ref} . In this architecture, the time resolution is determined by the delay difference. The vernier delay chain based TDC architecture is shown in the Figure 2.7. The buffer in the top chain has delay of τ_1 per delay element. The buffer in the bottom chain has delay of τ_2 per delay element. The achievable resolution equals to $|\tau_1 - \tau_2|$.

Figure 2.7 Vernier delay line based TDC

With vernier delay line based TDC, sub-10ps resolution can be achieved. The problem with this architecture is that a large number of Vernier stages are needed to quantize a certain time difference input, which costs large chip area and power consumption. In order to make vernier delay line based TDC compact, techniques such as 2-step TDC and 2-dimensional TDC have been developed.

2.3.2.4 Two Step TDC

In [26], a two step TDC using inverter delay chain and vernier delay chain is proposed. The two-step TDC consists of an inverter-delay chain for coarse quantization and a vernier-delay chain for fine quantization. The first stage quantizes the input with inverter delay chain and the first stage time resolution is determined by the inverter delay. The second stage consists of a Vernier delay chain and quantizes the residue from the first stage. The second stage time resolution is determined by vernier delay difference which is around 5ps.

The draw backs of this architecture is that calibration is needed to normalize the fine resolution of the second stage to the coarse resolution of the first stage. In addition, its linearity is still limited by the mismatch between the inverter delay elements.

2.3.2.5 2-D Vernier TDC

The 2-dimensional vernier TDC is proposed in [30] and its architecture is shown in Figure 2.8.

Figure 2.8 2-D vernier TDC

This architecture consists of 2 delay lines and a time comparator matrix. Instead of running parallel to each other, one delay line is horizontal while the other is vertical. The target resolution of $\Delta=5$ ps is determined by the delay difference between τ_1 and τ_2 . This delay is calibrated by delay locked loop (DLL) running in the background. The two delay lines form the Vernier plane which consists of a matrix of SR latches. It achieves a full scale of 590 ps conversion range.

Although this technique achieves detection range of 590 ps and fine resolution of 5 ps with acceptable number of delay elements, it requires DLL for precise calibration of each delay line.

2.3.2.6 Gated Ring Oscillator Based TDC

In [31], gated ring oscillator based TDC is proposed and it is illustrated in Figure 2.9.

Figure 2.9 GRO TDC architecture

The TDC quantizes the time delay between the rising edge of start and rising edge of stop. The core of this architecture is the gated ring oscillator. The counter is used for counting integer number of 2π phases. State registers are responsible for sampling the phase when the gated ring oscillator is disabled. The output of state registers and counter are summed to calculate the phase information of the oscillator.

When the start signal rises, the ring oscillator is enabled and starts to oscillate. When the stop signal rises, the ring oscillator is disabled.

Figure 2.10 shows the states of gated ring oscillator. When being enabled, the oscillator oscillates like a normal ring oscillator. When being disabled, the power supply for the ring oscillator is disconnected and the inverter cannot charge or discharge the parasitic capacitance at the output nodes. The oscillator phase at the end of the enabled state remains freezed during the disabled state.

Figure 2.10 Conceptual implementation of gating a ring oscillator

It can be observed that the phase at the end of a given measurement $T_{stop}[k-1]$ is the starting phase for the next measurement interval $T_{start}[k]$.

$$T_{start}[k] = T_{stop}[k-1] \quad (2-2)$$

The quantization error for a given measurement interval, T_{error} , is given by

$$T_{error}[k] = T_{stop}[k] - T_{start}[k] = T_{stop}[k] - T_{stop}[k-1] \quad (2-3)$$

The above first order discrete time difference equation corresponds with a first-order noise shaping. As a result, the quantization noise is first order filtered. In addition, the delay element mismatch is also first-order filtered [31].

This architecture achieves fine resolution and large dynamic range. The drawback of this architecture is that it is not suitable for sub-90 nm process due to high leakage current which will destroy the freezed phase when the ring oscillator is disabled.

Table 2.3 summarizes performances of a few different TDC designs in literature.

Table 2.3 Performance summary of TDCs

	[26] JSSC 2010	[31] JSSC 2009	[8] RFIC 2005	[30] JSSC 2010	[32] JSSC 2012	[33] ISSCC 2012	[34] JSSC 2010	[35] TCASI 2014
Proc (nm)	90	130	90	55	130	90	130	130
Δt_{res} (ps)	5	1	20	5	6	7.7	8	7
Range (ns)	0.5	12.3	0.6	0.59	100	10	33	14
Power (mW)	1.08	31.5	1.69	0.75	0.7	2	7.5	0.33
fs (MHz)	40	50	26	26	50	80	15	1
Area (mm ²)	0.02	0.04	0.01	0.02	0.08	0.02	0.26	0.28
Architecture	2 step	GRO	invert er chain	2D vernier	3rd $\Delta\Sigma$	SRO	Vernier ring	3 D vernier
INL (LSB)	--	--	0.7	-1-3	--	--	--	-1.5 – 1.5
DNL (LSB)	--	--	<0.7	-1 - 0.8	--	--	--	-0.8 – 0.8

2.3.3 Design of Digital Controlled Oscillator

2.3.3.1 DCO Quantization and Modelling

Similar to DAC, DCO converts the input digital word to certain output frequency. The quantization step of the DCO is equal to its frequency resolution Δf . The DCO quantization step/resolution introduces additional phase noise, which can be modelled as additive random variable $\Delta f n$ as shown in Figure 2.11 [36]. The frequency quantization error is converted to phase through the $\frac{2\pi}{s}$ integration.

Figure 2.11 DCO quantization

2.3.3.2 DCO Implementation with voltage DAC and VCO

In [5], DCO implementation is realized by putting voltage digital-to-analog converter (DAC) before conventional VCO as shown in Figure 2.12. Firstly, the voltage DAC converts the input digital control word to analog output voltage. Then, the output voltage of DAC tunes the VCO output frequency.

Figure 2.12 DCO implementation with DAC and VCO

In this DCO implementation, discrete coarse frequency tuning is achieved with 4-bit switched MIM capacitor array. Two MOS varactors of different sizes are added for continuous tuning at coarse and fine level respectively. The coarse and fine tuning varactors are driven by two 10-bit voltage DACs separately. The VCO fine tuning gain K_{VCO_fine} is 5 MHz/V [5].

This DCO design approach does not need fine capacitor array for the oscillator design. However, it requires voltage DACs with sufficient resolution.

2.3.3.3 DCO Implementation with Switched Capacitance

Another popular approach for implementing DCO is using switched capacitance [26, 37]. When more capacitance is switched into the LC tank, the oscillator will run at slightly lower frequency. As shown in Figure 2.13, the capacitor array is usually segmented into coarse and fine capacitor arrays.

As shown in Figure 2.14, switched capacitance can be implemented with either metal capacitors or MOS capacitors. Metal capacitors including MOM capacitor and MIM capacitor are usually used for coarse step tuning for noise immunity and reducing supply pushing [10]. Inversion type PMOS varactors are usually chosen for fine step tuning due to their small size and well-defined “high” and “low” capacitance levels [9, 38].

To further improve the DCO resolution, dithering method is usually adopted [24]. However, the dithering process may produce additional high frequency phase noise. Careful calculation need to be done to ensure the DCO quantization noise contribution is sufficiently lower than the natural DCO noise.

Table 2.4 Performance summary of DCO designs

	[39]	[26]	[40]	[38]	[41]	[9, 42]
process	90nm	90nm	90nm	65nm	65nm	130 nm
Power (mW)	3.9	2.28	2.4	19.2	5.76	3.75
tuning range (GHz)	9.75-10.17	2.1-2.8	3-3.7	6.35-9.15	2.3-2.5	2.15-2.65
Design technique	$\Delta\Sigma$ dithering	$\Delta\Sigma$ dithering	One hot code	Capacitive divider	$\Delta\Sigma$ dithering	$\Delta\Sigma$ dithering
fres (Hz/LSB)	250	140	3000-6000	800	<1000	718
PN dBc/Hz@ 1MHz	-100	-115	-118	-129	-125	- 112@500 K
FOM	-174	-181	-185	-194	-185	-180

2.3.4 Design of High Speed Counter

2.3.4.1 Asynchronous Counter and Synchronous Counter

High speed counter is an indispensable part in counter-assisted DPLL architecture. Flip-flops in an asynchronous counter are not triggered by a common input clock and are usually clocked by the output pulse of the preceding flip-flop. Consequently, every flip-flop changes its state at different timing. An asynchronous counter can operate at high input clock rate with reduced power consumption. However, the accumulated timing skew due to flip-flop clock to data output delay can exceed one input clock period [26]. The accumulated timing skew of all the output bits is required to be within one input clock period to be latched by digital flip-flops for phase error calculation [26].

In contrast to an asynchronous counter, flip-flops in a synchronous counter are triggered by a common input clock and its output bits change state simultaneously. As a result, delay is not accumulated in the synchronous counter. However, synchronous counters usually consume significant power because every bit is clocked at the highest input clock rate. In addition, the long critical path in the synchronous counter limits its maximum input clock frequency.

2.3.4.2 Splitting Counter Architecture

The problem with synchronous counter is that all the flip-flops are clocked at input clock frequency and it requires high power consumption when operating at high speed. To reduce power consumption of synchronous counters, splitting counter architecture is proposed in [26]. As shown in Figure 2.15, the 8-bit high speed synchronous counter consists of a 2-bit synchronous counter for the two least significant bits (LSBs), another 6-bit synchronous counter for the remaining six most

significant bits (MSBs), and gating control logic for generating low speed triggering clock for the 6-bit synchronous counter. The purpose is to reduce the operation frequency of the 6-bit counter for the six MSBs to one quarter of the input clock frequency.

Figure 2.15 8-bit splitting architecture high speed synchronous counter

Figure 2.16 illustrates the signal timing of the split structure high speed counter. Input enable signal *En* is assumed to be '1'. The 6-bit synchronous counter operates at one quarter of the input clock speed instead.

Figure 2.16 Timing waveform for high speed counter

2.3.5 Design of Frequency Divider

2.3.5.1 Static Current Mode Logic Frequency Divider

Static frequency dividers (SFDs), which are based on edge-triggered flip-flops, are widely used in phase locked loop implementations [43]. The flip-flop usually consists of one pair of master and slave D-latches. The two latches are driven by anti-phase clock pulses as shown in Figure 2.17.

Figure 2.17 Static frequency divider based on edge triggered flip-flop

Current mode logic (CML) implementation, which features high operation frequency and differential architecture, is usually adopted for the D-latch

implementation. A typical CML implementation of D-latch is shown in Figure 2.18. Two current sources are placed at the bottom of the conventional CML divider in order to control its power consumption, and can be removed for low voltage application [44].

Figure 2.18 CML D-latch

The maximum operation frequency of the CML divider is limited by the propagation delay from input port D/DB to output port Q/QB in the D-latch. Analysis of different regions of operation and optimization of the transistor sizes for CML frequency dividers can be found in [45]. The maximum operation frequency increases with increasing self-oscillating frequency (f_{so}), which is defined to be the frequency divider's oscillation frequency when its input clock is removed. It is recommended to design $2f_{so}$ to be slightly higher than the maximum input frequency f_{in} to allow robust divider operation [45]. Furthermore, the locking range of a CML divider increases with increased input amplitude.

Poly-resistor is preferred to be used as the load for the CML latch for its smaller parasitic capacitance. On the other hand, active PMOS load can be adopted to realize variable resistance [46] or compact layout [47]. Also, inductive peak have been introduced to increase the operating frequency of CML frequency dividers [48, 49].

Note that the CML divider has a large static current, which is fatal for low power application. Nevertheless, CML dividers are still the most popular dividers used in moderate frequency band due to their simple structure and robustness.

2.3.5.2 Dynamic TSPC Frequency Divider

A true single phase clock (TSPC) divider is a dynamic frequency divider and the D-latch implementation is different from latch implementation in static frequency dividers.

Figure 2.19 TSPC frequency divider

The TSPC frequency divider as shown in Figure 2.19 only dissipates power during charging and discharging. The advantage of TSPC frequency dividers is that they consume less power and require less number of transistors. However, they cannot provide complementary or quadrature outputs. Due to single-ended structure,

common-mode noise also affects TSPC divider's output. It is also sensitive to parasitic effects such as leakage, and clock feed-through.

The extended true single phase clock (E-TSPC) frequency divider shown in Figure 2.20 is proposed to increase the operating frequency in [50].

Figure 2.20 E-TSPC frequency divider

The propagation delay of the E-TSPC flip-flop is less than that of the TSPC flip-flop as its load capacitance is reduced. However, there is a period during which a direct path from supply voltage to ground is established in the E-TSPC flip-flop in the operation of divide-by-2 and this causes additional power consumption [51].

2.3.5.3 Injection Locked Frequency Divider

The injection locking phenomenon can also be utilized to achieve frequency division. When a super-harmonic of the injection locked oscillator is locked to the fundamental frequency of the injected signal, frequency division is achieved. There are two types of injection locked frequency dividers: LC resonator based ILFD [52, 53] and ring oscillator based ILFD [54-57].

2.3.5.3.1 LC Resonator Based ILFD

The concept of injection locking is illustrated in Figure 2.21 and is analyzed in [58]. Consider the simple oscillator shown in Figure 2.21(a), the LC tank operates at the free running frequency $\omega_{O,free}$ without any injection. As shown in Figure 2.21(c), additional phase shift will be introduced by injection and the LC tank oscillation frequency will shift to ω_O to satisfy total phase shift of 360 degree. As illustrated in Figure 2.21(d), If the phase introduced by I_{inj} can compensate the phase shift $\Delta\phi$ due to the frequency shift to ω_O , the oscillator can be locked, that is $\omega_O = \omega_{inj}$.

(a) conceptual oscillator

(b) open-loop characteristics

(c) oscillator with injection

(d) phasor diagram

Figure 2.21 Concept of injection locked oscillator

The input locking range can be computed with the following equation:

$$\omega_{inj} - \omega_{o, free} = \frac{\omega_{o, free}}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (2-4)$$

LC resonator based ILFD can operate at high frequency. However, LC resonator based ILFD's input locking range is narrower due to the high quality factor of the LC tank. Tank quality factor and oscillator current have to be optimized to achieve larger locking range [59]. Besides tail injection, direct injection is proposed to reduce input capacitance and improve injection efficiency for high frequency input [60].

2.3.5.3.2 Ring Oscillator Based ILFD

The analysis of ring oscillator based ILFD is similar to LC resonator based ILFD. Figure 2.22(a) shows a ring oscillator based ILFD with single tail injection at the first buffer element. In conventional ring oscillator based ILFDs, RF input is injected to the gate of one of the biasing transistors. If no input is injected, the ring oscillator is free running at $\omega_{o, free}$. As shown in Figure 2.22(b), v_{inj} introduces injection current i_{inj, ω_i} at input frequency ω_i in M_0 . Assuming perfect matching of the differential pair, odd order harmonics will be generated at $\omega_o, 3 \cdot \omega_o, 5 \cdot \omega_o, \dots$. A general behavior model of the ILFD has been presented in Figure 2.22(c) [13]. The injection current i_{inj, ω_i} mixes with the super-harmonics of the output waveform through the mixer formed by the differential pair and the bottom biasing transistor. Low pass filter formed by the buffer stages rejects frequency components higher than ω_o and only the mixing product i_{inj, ω_o} at ω_o remains. The buffer load current $i_{load} = i_{osc} + i_{inj, \omega_o}$ and phase shift of $\Delta\Phi$ is introduced in i_{load} due to component i_{inj, ω_o} . As illustrated in Figure 2.22(d), the output frequency of the ring oscillator will shift away from its free running frequency $\omega_{o, free}$

to make the total phase shift in the loop equal to zero again. When the input RF signal is injected with sufficient power, the output of ILFD locks to a sub-harmonic of its input and $\omega_i = m \cdot \omega_o$. The locking range equals to the phase shift $\Delta\Phi$ caused by the input injection multiplied by the linearized phase response at $\omega_{o,free}$ of the low pass filter $H(j\omega)$ formed by the buffer stages [61].

Figure 2.22 (a) Conventional ILFD with single tail injection (b) Buffer with tail injection (c) ILFD behavior model (d) Frequency response of low pass filter formed by buffers.

2.3.5.3.4 Summary

The choice of frequency divider architecture depends on the requirements of maximum input frequency, quadrature generation, power consumption, locking range

and design complexity. Table 2.5 summarizes the advantages and disadvantages of different frequency divider architectures.

Static CML frequency dividers can operate in low and medium frequency band and are robust while consuming high power. TSPC frequency dividers usually operate in low frequency band and they are simple to design and very compact. However, it is not able to provide quadrature outputs and is susceptible to common-mode noise and parasitic effects. Injection locked frequency dividers (ILFDs) generally feature higher power efficiency and are able to divide by any integer larger than two directly. Ring oscillator based ILFDs have wider locking range due to their lower Q compared to LC oscillator based ILFDs and also less output amplitude variation [54, 56]. In addition, ring oscillator based ILFDs are much more compact than LC resonator based ILFDs. However it is still difficult for ring oscillator based ILFDs to provide division ratio larger than 2 and acceptable locking range at the same time [56].

Table 2.5 Performance summary of frequency dividers

Topology	f_{in_max}	Locking range	Power	Area
CML	Medium	Wide	High	Small
TSPC	Low	Wide	Very Low	Small
ILFD (Ring Osc)	Medium	Wide	Low	Small
ILFD (LC Osc)	High	Narrow	Low	Large

Chapter 3. Ring Oscillator Based Injection Locked Frequency

Divider with Dual Injection Paths

In this chapter, proposed divide-by-four ring oscillator based ILFD architecture with dual injection paths is presented. Review of ring oscillator based ILFD design techniques is firstly described. Next, the proposed differential buffer circuit with dual injection and the architecture of the divide-by-four ring oscillator based ILFD are presented. Equivalent circuit modelling of the dual injection buffer and analysis of locking range enhancement are discussed. Measurement results are presented thereafter.

3.1 Introduction

Compared to other technology, CMOS is preferred due to its low cost and high level integration for RFICs. Pre-scaler stage is indispensable in a phase-locked loop system and is usually power hungry because of running at high frequency. Conventional static frequency dividers can work at 20 GHz [62], but its power consumption is high. Injection locked frequency dividers (ILFDs) have recently received more attention due to their high power efficiency and the ability to divide by any integer larger than two directly. ILFDs can be classified into LC oscillator and ring oscillator based. LC oscillator based ILFD can operating at high frequency with low power consumption but also narrower locking range due to higher tank Q. In addition, inductors occupy a large area when the operating frequency is low. Its free running frequency is determined by L and C values. Tank Q and biasing current can be optimized for larger input locking range. Ring oscillator based ILFDs have wider

locking range due to their lower Q compared to LC oscillator based ILFDs and also less output amplitude variation [54, 56]. Compared to LC oscillators, Q for ring oscillators is 1 since it does not have energy storage capability. And its biasing current mainly affects its free running frequency. LC resonator is the load for LC resonator based ILFDs. In contrast, ring oscillator based ILFDs can have resistor, PMOS in triode region, or cross coupled latch as load. The low quality factor of ring oscillator does not worsen phase noise performance since the output phase noise of ILFDs is dominated by its input when ILFDs are locked. In addition, ring oscillator based ILFDs are much more compact than LC resonator based ILFDs. Furthermore, some ring oscillator based ILFD can provide multiple phase outputs which can be utilized for edge selection or phase quantization in PLLs [63, 64]. However, it is still extremely difficult for ring oscillator based ILFDs to provide division ratio larger than 2 and acceptable locking range at the same time [56]. For division ratio of 2, the RF input is mixing with the oscillator output frequency itself. While for division ratio of 4, the RF input is mixing with the third and fifth harmonic of the output frequency to create phase shift at ω_0 . consequently it is more difficult to have a large input locking range for division ratio larger than 2 due to reduced harmonic power.

Under variation of PVT (process, voltage and temperature), mismatch between input locking range of ILFD and VCO tuning range will result in unlocking. Hence it is important for the ILFDs to have wide input locking range to make the locking less vulnerable to PVT variations. Furthermore, it has been demonstrated that wide input locking range also helps minimizing output phase noise [13]. The internal noise of the ring oscillator is high pass filtered and the cut-off frequency of the high pass filter increases with the increase of input locking range.

Inductive peaking technique for the load has been introduced to boost high frequency gain for ILFDs to operate at higher frequency [65]. Shunt inductors are added parallel to the biasing transistor to improve injection efficiency at high frequency which leads to wider locking range [66]. The problem is that adding inductors significantly increases the chip area. Varactor or bias tuning methods have been implemented to enhance the input locking range of ILFDs [54]. Switched capacitances are employed in [55] for dual band operation. But it is still difficult to tune the voltage controlled oscillator (VCO) and ILFD in a PLL at the same time. Multi-phase injection has been proposed to widen the input locking range significantly in [11]. However multiple input phases may be difficult to generate at high frequency. Tail injection [11, 12, 54] and direct injection [67, 68] are two commonly used injection techniques for ring oscillator based ILFDs. Dual injection technique has been proposed in [53] to achieve wide input locking range for a LC resonator based ILFD with division ratio of 2.

RF input signal is AC coupled to the gate of the biasing transistor in tail injection. To increase injection efficiency, biasing transistor can be sized with a bigger W/L ratio to increase its trans-conductance. However, high transconductance g_m will make the circuit more susceptible to noise and the big transistor size will attenuate high frequency harmonics, which are essential for mixing. RF input signal is injected at the gate of a load transistor in direct injection. A bigger direct injection transistor can be used for stronger injection. Increasing the size of the direct injection transistor mainly has two effects: (1) increase the injection current, which helps to achieve wide locking range; (2) Due to more parasitic capacitance introduced at the output nodes, the free running frequency drops, which degrades the maximum locking frequency. When the size of the direct injection transistor is small, the first effect is dominant, and

the locking range increases with increasing size of direct injection transistor. However, the second effect becomes dominant when the injection transistor size is larger than a threshold value. Increasing the size of the direct injection transistor no longer improves locking range, and may even degrade the locking range or distort the output waveform. The injection efficiency for single injection is eventually limited and constrained by other considerations. In this work, tail injection and direct injection are both utilized to create much stronger harmonics by adding the outputs of the two mixing process constructively at the output node. A divide-by-4 ring oscillator based ILFD with dual injection has been implemented and tested. In addition, buffer delay has to be taken into consideration in the mathematic analysis for ring oscillator based ILFDs. This chapter provides detailed mathematical derivation and proves that the two injection paths are still constructive to each other for division ratio larger than 2 and can achieve larger input locking range for ring oscillator based ILFDs.

3.2 Ring Oscillator Based ILFD Using Dual Injection Buffers

3.2.1 Differential Buffer with Dual Injection

Although some single ended ILFDs based on single ended buffers have been proposed, differential buffer is still preferred because high performance and low noise systems usually require fully differential signals in the whole transceiver path. Figure 3.1(a) shows the proposed differential buffer design with dual injection. V_B and V_{BO} are DC biasing voltages. Due to the latch load formed by cross coupled M_3 and M_4 , buffer outputs are with rapid transition and large amplitude which increase super-harmonic contents. Figure 3.1(b) models the two harmonic mixing processes corresponding to each of the injection paths.

Figure 3.1 (a) Proposed differential buffer design with dual injection. (b) Equivalent circuit of the differential buffer.

Through the trans-conductance of M_0 , RF input v_{inj} injects current with amplitude of $|i_{inj1,\omega}| = |v_{inj}| \times g_{m0}$ at RF input frequency ω into the differential pair. As

the output swing amplitude is large, differential pair consisting of M_1 and M_2 can be considered as ideal switches controlled by square wave $\Pi(t)$.

$$\Pi(t) = \sum_{i=1,3,5..}^{\infty} (-1)^{(i-1)/2} \frac{4}{\pi \cdot i} \cos(i \cdot \omega_o \cdot t) \quad (3-1)$$

DC biasing current I_{bias} and injected current i_{inj1,ω_i} are effectively mixing with the output waveform and its higher order harmonics. DC current I_{bias} will be up-converted to output frequency ω_o . The amplitude of i_{osc} is $|i_{osc}| = (4/\pi) \cdot I_{bias}$. Since $\omega_i = 4 \cdot \omega_o$, i_{inj1,ω_i} will mix with the third and fifth super-harmonics to produce i_{inj1,ω_o} at output frequency ω_o . The amplitude of i_{inj1,ω_o} is $|i_{inj1,\omega_o}| = \alpha \cdot |i_{inj1,\omega_i}|$, where α is the mixer conversion factor and depends on the amplitude of the third and fourth harmonic.

M_5 is NMOS load connected between differential outputs. By injection at the gate of M_5 , v_{inj} is effectively mixing with the higher order harmonics. Assuming weak injection, v_{inj} also introduces injection current i_{inj2,ω_i} with amplitude of $|i_{inj2,\omega_i}| = |v_{inj}| \times g_{m5}$ at ω_i in M_5 . Since v_{op} and v_{on} transit fast, i_{inj2,ω_i} is modulated by a square wave function $v_{on}-v_{op}$ which is delayed by $(n+1)T/(2n)$ from $v_{inp}-v_{inn}$ and can be represented by $\Pi\left(t - \frac{(n+1)T}{2n}\right)$. T is the oscillator output period and n is the number of buffer stages which equals to 4 in this implementation. By mixing with the third and fifth harmonics, current i_{inj2,ω_o} due to injection at M_5 is produced at ω_o at the output nodes. Similarly, the amplitude of i_{inj2,ω_o} is $|i_{inj2,\omega_o}| = \alpha \cdot |i_{inj2,\omega_i}|$. Low pass filter $H(j\omega)$ formed by the buffer stages rejects frequency components higher than ω_o .

The output currents of the two mixing processes add up at the output nodes, which flows into the RC load.

$$i_{load} = i_{osc} + i_{inj1,\omega\omega} + i_{inj2,\omega\omega} \quad (3-2)$$

Note that the above summation is vector addition. The locus of the ending points of current phasor i_{load} is plotted in Figure 3.2 with estimated current ratio of $|i_{inj1,\omega\omega}| : |i_{inj2,\omega\omega}| : |I_{bias}| = 0.5:0.4:1$. The locking range equals to the phase shift Φ of i_{load} caused by the mixing processes multiplied by the linearized phase response of the low pass filter $H(j\omega)$ formed by the buffer stages [61]. Instead of calculating the locking range, the phase shift Φ of i_{load} is examined since it is proportional to locking range. Clearly, phase shift $\Delta\Phi3$ introduced by dual injection is much larger than phase shift $\Delta\Phi1$ or $\Delta\Phi2$ introduced by single injection. In other words, the output currents from the two mixing processes are added constructively near output frequency $\omega\omega$.

Figure 3.2 Locus of ending points of phasor i_{load} .

3.2.2 ILFD Architecture

Figure 3.3 Four stage differential ring oscillator ILFD consisting of dual injection buffers.

The block diagram of the complete frequency divider is shown in Figure 3.3. $Vin+$ and $Vin-$ are the differential inputs, which are coupled to the injection transistors M_0 and M_5 through AC coupled network formed by C_1 , C_2 and R_{bias} . V_B and V_{BO} are DC biasing voltages, which set the operating points of M_0 and M_5 respectively. The differential ring oscillator consists of 4 stages of the proposed differential buffer. The output of the last buffer is connected to the first buffer input with inverted polarity to provide 180° phase shift. Each buffer adopts the proposed dual injection technique for wider input locking range. Furthermore, 0 and π phases are injected to alternative buffer stage to achieve optimum multiple input injection [11].

3.3 Simulation and Measurement Results

The design has been fabricated in 65 nm CMOS process. The core size is only $30\ \mu\text{m} \times 15\ \mu\text{m}$. The micrographs of the chip and core layout are shown in Figure 3.4.

Figure 3.4 Chip photo and core layout.

Simulation of the output waveforms are depicted in Figure 3.5. The differential input, V_{in+} and V_{in-} , are at 15 GHz. The input sinusoidal amplitude is 300 mV. The ILFD's multiphase output V_{dp1} - V_{dp4} and V_{dn1} - V_{dn4} are at 3.75 GHz with one buffer delay in between. The output voltage swing is about 0.8 V.

Figure 3.5 Simulated ILFD output waveform

The injection transistors M_0 and M_5 add capacitive loading to its previous stage. According to post-layout simulation results with sinusoidal input of 300 mV amplitude at 20 GHz, the input power consumed are summarized in Table 3.1. Although the input power needed for drive two injection paths is higher than that of driving a single injection path, the input power needed is insignificant compared to the total power consumption of the ILFD. The summation of input capacitance due to all the injection transistors in the differential ring oscillator is about 40 fF. Furthermore, the ILFD is usually driven by a VCO in a PLL circuit. The input capacitance of the ILFD adds to the total capacitance of the VCO tank and thus resonates with the VCO inductor. Compared to the dominant capacitor tank inside the VCO, the input capacitance of the ILFD is negligible.

Table 3.1 Input power of ILFD

Input sinusoidal wave: 20GHz, 300 mV amplitude	Tail Injection	Direct Injection	Dual Injection
Input power driving the injection paths (μ W)	64.02	30.26	89.35

Simulation results of its input locking range are depicted in Figure 3.6. With dual injection technique, its locking range is extended by 35% - 85% compared with single injection at either biasing source or NMOS load. The measured free running frequency of the ring oscillator is 3 GHz. Input differential signal is generated by signal generator and balun. The device is measured on probe station and injection power loss is calibrated. The measured input locking range is also shown in Figure 3.6. For injection power of 0 dBm, the measured input locking range is from 1.2 GHz to 20.7 GHz.

Figure 3.6 ILFD input locking range simulation and measurement results.

Figure 3.7 Phase noise performance.

Figure 3.7 depicts input and output phase noise when injection locked to input of 20 GHz at 0dBm power level.

The results are summarized in Table 3.2 and compared with other state-of-art designs. The proposed design features the widest input locking range which is over 170 %.

Comparing with existing methods, the proposed implementation has the following advantages:

1: compact size. The proposed design is ring oscillator based ILFD and it does not need any inductor for oscillation. As shown in this chapter, the core only occupies $30\mu\text{m} \times 15\mu\text{m}$. Furthermore, it does not need any shunt inductor for frequency peaking as proposed in reference [4]. Its size is very compact and suitable for integrated solution.

2: no need of any tuning or external control. Some work has proposed bias tuning or switched capacitor method to cover different sections of frequency spectrum. For example, ILFDs are usually driven by a VCO in a PLL. The VCO can be wideband and tuning of VCO and ILFD at the same time is difficult and can interrupt PLL locking. Without any tuning, this work has achieved input locking range from 1.2 to 20.7 GHz.

3: This work apply dual injection technique to ring oscillator based ILFDs with division ratio larger than 2. Circuit modeling and mathematical proof are provided to serve as theoretical basis. It shows that the two injection path are constructively added for the ring oscillator based ILFD with division ratio of 4. The measurement results have demonstrated ultra wide input locking range without additional power, area, number of input injection phases or any calibration. The implementation only requires differential input. Most VCO are differential and thus differential input is easily available. Furthermore, ring oscillator based ILFDs have less output amplitude variation. In this design, the load of the buffer stage is formed by a cross coupled PMOS load which can help to maximize the output voltage swing between ground and VDD across the whole input locking range.

Table 3.2 Comparison of proposed ILFD with others

Year/Journal	[68] 2010 MTT	[69] 2011 WCL	[12] 2013 MTT	This work
Process	65 nm CMOS	180 nm CMOS	65 nm CMOS	65 nm CMOS
LR (GHz)	1.8-16.4 (0.3-0.6V)	4.5-5.4 (0 dBm)	9.8-16.7 (0 dBm)	1.2-20.7 (0 dBm)
Power (mW)	2	0.7	3.9	1.92
/n	2	5	4	4
RF input phases	Diff	Single	Diff.	Diff.
FOM1 (GHz/mW) ¹	8.2	7.71	4.28	10.78
FOM2 (GHz/mW) ²	7.3	1.29	1.77	10.16
1: maximum RF input frequency divided by power in mW. 2: locking range divided by power in mW.				

A novel ring oscillator based ILFD architecture using dual injection buffers has been proposed. The proposed ILFD is compact without any inductors needed. Measurements of the fabricated prototype divide-by-four ILFD circuit demonstrate power efficiency over 10 GHz/mW and over 170% input locking range without any need of bias or voltage tuning. Furthermore, ultra wide input locking range also prevents false locking to wrong division ratio.

There are certain applications which need wide output bandwidth. For example in X band ranging radar application, transmitter sends out wideband linear frequency modulated signal. The output bandwidth B is inversely proportional to ranging resolution according to the equation: $R_{res} = \frac{c}{2B}$, where c is the speed of light. For example, 5 GHz output bandwidth can provide 3 cm ranging resolution.

Furthermore, a wide locking range always makes the locking less vulnerable to PVT variations and helps minimizing output phase noise.

Although this design demonstrated an ILFD in X band, the proposed implementation can be adopted in ring oscillator based ILFDs in other frequency bands with different division ratio. Hence in general, the proposed method can be customized for applications with wideband frequency tuning requirements.

Chapter 4. A Low Power and Highly Linear 14 bit Parallel Sampling TDC with Power Gating and DEM in 65 nm CMOS

This chapter presents TDC architecture capable of achieving sub-gate-delay resolution and large detection range at the same time with low power consumption. Brief review of existing TDC architectures are provided firstly. Then, the proposed parallel sampling ring oscillator (PSRO) based TDC architecture is presented in the following section. Next, the CMOS key circuit implementations are described. Measurement results and discussions are given at the end of this chapter.

4.1 Introduction

High performance time to digital converters (TDCs) have become increasingly important for DPLLs [26], time domain analog to digital converters (ADCs) [70], time-of-flight (ToF) measurements [35, 71], and instrumentation applications [72]. It is difficult to achieve all the requirements of fine resolution, high linearity, low power, large dynamic range and being compact at the same time. For example, the measurement range typically varies from a few meters to tens of meters in industrial time-of-flight (ToF) applications. TDC resolution determines measurement precision and TDC dynamic range determines measurement range in ToF applications [73, 74]. It is also important for TDCs to be linear to ensure measurement accuracy. Successive measurements can be averaged to reduce error caused by noise but not static nonlinear behaviour. The most conventional TDCs quantize time using inverter or buffer delay and are able to achieve resolution of 15-30 ps in CMOS technology [8]. Sub-gate-delay resolution can be achieved with vernier architecture which faces problem of

element mismatch. In addition, TDCs based on buffer delay chain or vernier delay chain have very limited dynamic range as they have limited number of delay elements. Two step architecture [26] and 2-D vernier architecture [30] have been proposed to reduce the number of delay elements needed and still achieve sub-gate-delay resolution. However, 2-D vernier architecture has linearity problem when wide dynamic range is needed and the fine step resolution has to be normalized to the coarse step resolution through calibration in two-step architecture. Time amplifier (TA) based TDCs have been developed in [7, 75], which can achieve fine time resolution but suffer from limited detection range and high power consumption. Gated ring oscillator (GRO) based TDC has been developed in [31], which requires raw gate delay of 6 ps and suffers from leakage problem. Another TDC based on $\Delta\Sigma$ architecture has been developed in [76], but it suffers from limited detection range. For wide dynamic range and fine resolution, TDC based on vernier ring oscillator has been developed in [34]. However, it consumes high power due to the fact that two ring oscillators are running continuously at the same time and its decoding is sophisticated.

A parallel sampling ring oscillator based TDC with power gating and dynamic element matching (DEM) is proposed to achieve high resolution and large dynamic range at the same time with low power consumption. Furthermore, the static linearity is improved through DEM.

4.2 Parallel Sampling TDC Architecture

4.2.1 TDC Architecture

The proposed TDC is based on parallel sampling ring oscillator with power gating and DEM. Through digital background calibration, the time resolution is

determined by delay difference between successive sampling clocks instead of buffer delay. The ring oscillator is only enabled during the incoming time pulse width, leading to low power consumption. A new buffer circuit implementation which enables the ring oscillator to settle to a known position after the ring oscillator stops is proposed. Furthermore, the stop position is latched by cross-coupled inverters to achieve immunity to leakage issues. For each incoming time pulse, the ring oscillator starts oscillation from the buffer before which the previous conversion stops, and thus it also achieves barrel-shift algorithm for dynamic element matching and mitigates buffer mismatch impact.

The proposed parallel sampling ring oscillator (PSRO) based TDC is shown in Figure 4.1. The proposed TDC architecture consists of an 8-stage differential ring oscillator, 5 rows of sense amplifier based flip-flops (SAFFs) for sampling the ring oscillator states, two 8-bit high speed low power asynchronous counters for counting the integer number of oscillation cycles, digital to time converters (DTCs) for tuning the successive sampling clocks with sub-pico second accuracy and digital circuit part. The digital circuit part consists of phase_decoder, DTC_control and output_calculation. The phase_decoder decodes the ring oscillator phase states sampled by each row of SAFFs. The DTC_control can run at background and automatically tunes the successive sampling clock delays for fine resolution. Four 6-bit DTCs convert the digital control words (DCWs) provided by DTC_control to desired fine delays. The output_calculation calculates the output digital code by subtracting the starting phase from the ending phase.

Figure 4.1 Block diagram of parallel sampling ring oscillator based TDC.

4.2.2 Achieving Fine Resolution with Parallel Sampling

Each differential buffer provides delay of τ_{buf} . With single sampling of the ring oscillator phase states, resolution of τ_{buf} can be achieved. In the proposed parallel sampling architecture, multiple successive sampling of the oscillator phase is carried out. The sampled phase state of each sampling line is decoded by phase_decoder. The DTC_control block compares the sampled phase states and regulates successive sampling clocks to be delayed by $\tau_{ck} = \tau_{buf}/4$ from its previous clock. In this way, the time resolution is enhanced to 1/4 of the buffer delay. The extra SAFFs and DTC consume much lower power than the core ring oscillator and counters. Consequently,

the resolution is improved by 4 times without trading off with power consumption. The dynamic range is limited by accumulated phase noise of the ring oscillator.

Figure 4.2 Timing diagram of proposed parallel sampling ring oscillator based TDC.

The timing diagram of the PSRO based TDC is shown in Figure 4.2. The TDC quantizes the time interval between the rising edge of *In_A* and the rising edge of *In_B*. A time_gen block generates *EN/ENB* signal to enable/disable the ring oscillator and sampling signal *clk0* for clocking the SAFFs. At the rising edge of *In_A*, *EN* goes high and *ENB* goes low. Consequently, the differential ring oscillator starts to oscillate. When the rising edge of *In_B* arrives, sampling clock *clk0* rises. *clk1-clk4* is delayed from *clk0* by different amount of delay controlled by four DTCs. By properly controlling the DTC input digital control words *DCW1-DCW4*, *clk1-clk4* rises one

after another to sample the ring oscillator states *phase1* – *phase4*. Shortly after *clk1* - *clk4* trigger, the ring oscillator will be disabled and stops oscillation to save power. Consequently, disabling the ring oscillator does not affect sampling of the ring oscillator phase states *phase1* – *phase4*. Shortly after the oscillation stops, the stop state *phase5* will be sampled by *clk5*. *phase1* - *phase5* are decoded by the *phase_decoder*. *phase1*- *phase4* are used to calculate the stop position. And *phase5* is used to calculate the starting position for the next conversion. The *DTC_control* block compares the phase states *phase1* - *phase4* and regulates the delay between successive sampling clocks *clk1* - *clk4* to be one quarter buffer delay. Two asynchronous counters count the integer number of oscillation cycles. The asynchronous counters are sampled after they settle. An *output_calculation* block combines the counter output and phase states to generate the final 14 bit output value.

4.2.3 Digital Calibration of Successive Sampling Clocks

The purpose of digital calibration of the successive sampling clocks is to regulate them with 1/4 buffer delay between adjacent sampling clocks. The digital control word *DCW1* is set to 0 always and sampling clock *clk1* serve as the reference clock from which the other three sampling clocks are delayed. Since *clk2* - *clk4* are regulated in the same way, the following discussion focuses on description of regulating *clk2*. Sampling *clk1* and *clk2* trigger the first and the second row of sampling flip-flops respectively. The flip-flops' outputs *S1*<1:8> and *S2*<1:8>, which will be decoded as *phase1* and *phase2* respectively, depend on the ring oscillator nodes' voltage level. Decoded digital signal *phase1* and *phase2* represent the rising position of *clk1* and *clk2* respectively. The *DTC_control* block compares *phase1* and *phase2* and regulates the sampling clock delay between successive sampling clocks to

be 1/4 buffer delay. The sub-blocks in DTC_control are show in Figure 4.3. The difference between *phase1* and *phase2* are compared with 1 LSB (1/4 buffer delay), and the error is integrated to generate *DCW2* for the DTC. The DTCs close the negative feedback loops and convert digital control words (DCWs) to fine time delay.

Figure 4.3 DTC_control block diagram.

The digital calibration loop is in fact a first order digital delay locked loop (DLL) and it is redraw in Figure 4.4 to make it more obvious. Its close loop bandwidth is set to about 100 Hz to minimize calibration loop's output jitter and to compensate voltage and temperature variation. The ring oscillator, sampling flip-flops and phase decoder units form the digital phase detector and it has time resolution of τ_{buf} . Decoded digital signal *phase1* and *phase2* contain information of the rising position of *clk1* and *clk2* respectively. A simple digital integrator forms the digital loop filter and its gain adjusts the close loop bandwidth. The DTC functions as digital controlled delay line.

Figure 4.4 Digital calibration loop for regulating clk2.

The major sources of noise contribution in this calibration loop are from the digital phase detector quantization noise Δt_{q_DPD} and the DTC quantization noise Δt_{q_DTC} . Figure 4.5(a) presents the linearized modelling of the calibration loop. The noise analysis is similar to phase noise analysis in traditional DLLs [77-79]. The quantization noise of the digital phase detector Δt_{q_DTC} equals to τ_{buf} and it is first order low pass filtered with cut off frequency at the close loop bandwidth f_{loop_BW} . The quantization noise of the DTC Δt_{q_DTC} equals to DTC resolution t_{res_DTC} and it is first order high pass filtered with the lower cut-off frequency at the close loop bandwidth also. As seen in Figure 4.5(b), the close loop bandwidth should be chosen as small as possible to minimize the total output noise due to the fact that the noise power level of the digital phase detector is much higher than that of the DTC. To compensate for temperature and voltage supply variation, 100 Hz close loop bandwidth is chosen.

With 100 Hz close loop bandwidth, the total output noise power can be calculated as the integration of the noise spectrum density over the entire spectrum. With $\tau_{buf} = 24\text{ps}$ and $t_{res_DTC} = 0.5\text{ ps}$, the total rms jitter of $clk2$ at the calibration loop output is 0.17 ps with close loop bandwidth of 100 Hz.

Figure 4.5 (a) Linearized modelling of the digital calibration loop (b) Major noise contribution in the digital calibration loop.

The settling behaviour of the digital calibration loop has been tested and the DTC input digital control words (DCWs) have been recorded and plotted in Figure 4.6.

Figure 4.6 Measured digital calibration loop settling.

4.2.4 Dynamic Element Matching

The ring oscillator will start to oscillate from its previous stopped position. Consequently it may start from any of the buffer elements. The buffer element mismatch is translated from a dc error into a wideband AC noise which can be reduced by averaging multiple measurements [80]. As illustrated in Figure 4.7, oscillation travels through buffer 1 to buffer 3 in measurement 1 when the input pulse width is about 3 buffer delays. For subsequent measurements, oscillation travels through buffer 4 to buffer 6, buffer 7 to buffer 1, and buffer 2 to buffer 4. Different buffer mismatch contributes to different measurements, achieving dynamic element matching.

Figure 4.7 Ring oscillator with power gating achieving DEM

This DEM can randomize the linearity error due to buffer element mismatch [81]. Therefore, the spur free dynamic range is improved while its signal-to-noise-and-distortion ratio (SNDR) is not increased because the randomized error is spreaded over its noise floor. Furthermore, the randomized error may manifest itself as output code variation in single shot precision test since different buffer mismatch contributes to different measurements. The output variation can be reduced by averaging over a few samples to improve its accuracy.

Other architectures without DEM (e.g. vernier chain based TDC) may achieve excellent single shot precision in terms of output code variation because the input pulse always travel through the same sequence of buffers. However, its output code differs from the ideal value by big error due to its poor INL performance. Furthermore,

this error due to poor INL cannot be reduced by averaging since consecutive outputs all have the same error for the same input time width.

4.3 Circuit Implementation

In this section, implementation details and design considerations of the proposed TDC are provided.

4.3.1 Differential Ring Oscillator with Latch Load

8-stage differential ring oscillator with power gating is shown in Figure 4.8(a). The oscillator can be enabled/disabled through pin EN and ENB . Differential buffer with latch load is implemented as the delay element and its schematic is shown in Figure 4.8(b).

Differential input voltage $vin+$ and $vin-$ drive four input differential transistors $MN1$, $MN2$, $MP1$ and $MP2$. Transistors $MN5$ and $MP5$ connect the input transistors to ground and power supply respectively, achieving power gating. To reduce power consumption, the ring oscillator is only enabled slightly longer than the incoming pulse width. When $MN5$ and $MP5$ are disabled (ENB will be pulled to VDD and EN will be pulled to VSS), the ring oscillator stops oscillation. Consequently there cannot be any current flowing through $MP5$, $MN5$, $MP1$, $MN1$, $MP2$ or $MN2$. Unlike $MP1$ and $MP2$, the source of $MP3$ and $MP4$ are connected directly to VDD. Similarly, the source of $MN3$ and $MN4$ are connected directly to VSS. After $MP5$ and $MN5$ are disabled, the latch transistors $MP3$, $MP4$, $MN3$ and $MN4$ are still powered and thus able to drive one end of the differential output to high and the other to low and this is illustrated in Figure 4.9.

architecture, the parasitic capacitance needs to hold the voltage level at each output node and the hold state is the starting position for the next conversion.

Figure 4.9 Phase decoding of the differential ring oscillator

The differential ring oscillator has total 16 phase states which are decoded according to the voltage level of the internal output nodes as illustrated in Figure 4.9. At the moment the ring oscillator is disabled, *von1* is falling and *vop1* is rising. In GRO architecture, *von1* and *vop1* will hold their voltage level at the falling edge of *EN* using parasitic capacitance. While in this architecture, the latch load will force *von1* to *VDD* and *vop1* to *VSS* since *vop1* has not crossed *von1* when the oscillator is disabled. The stop position will be sampled by the fifth sampling line and decoded as the starting phase position for the next conversion. We not only know the starting phase for the next conversion, the voltage levels of *vop1* and *von1* are also known. For the scenario drawn in Figure 4.9, the next conversion will start from middle of ϕ_8 with

$von1$ at VDD and $vop1$ at VSS . Although there are leakage paths at output node $von1$ and $vop1$, $von1$ is held at VDD and $vop1$ is held at VSS through the much stronger conduction paths formed by on transistors $MP3$ and $MN4$ respectively.

Figure 4.10 Sense amplifier based D flip-flop for minimizing meta-stability.

The oscillator phase states are sampled by SAFFs. When the data change occurs near to clock rising edge, meta-stability is possible to occur. To minimize meta-stability, sense amplifier based flip-flop structure is adopted [82] and its schematic is shown in Figure 4.10.

4.3.2 High Speed Asynchronous Counter

Two high speed counters are used to count the integer number of oscillation cycles. Figure 4.11 shows the implementation of the asynchronous counter.

Figure 4.11 Implementation of the asynchronous counter.

The ring oscillator is disabled slightly after $clk4$ rises to avoid disturbing sampling the flip-flops as depicted in Figure 4.12. Due to this delay τ_d , which is less than half oscillation period, the 8 bit asynchronous counter driven by $vop8$ may change its state during this delay and thus wrong counter value may be latched. To avoid this problem, two asynchronous counters driven by $vop8$ and $von8$ respectively are added. When sampled $phase4$ is between $\phi0$ and $\phi7$, $count_p$ value is used for output calculation. When $phase4$ is between $\phi8$ and $\phi15$, $count_n$ value is used for output calculation.

Figure 4.12 Two asynchronous counters driven by oscillator differential output.

4.3.3 DTC

6 bit DTC is used to fine tune the sampling clock delay as shown in Figure 4.13. Clock input of the DTC travel through inverters. The internal inverter output node is loaded with 64 units of PMOS transistors ($W/L=240n/200n$). The PMOS gates are connected to the internal inverter output node *clkint*. The drain and source of PMOS transistors are short together and driven by inverters controlled by digital logic. Input binary digital control words (DCWs) are converted to thermal-meter coded output through binary to thermal meter code decoder to ensure monolithic behaviour which is most important in this application.

Figure 4.13 DTC block diagram.

It is less stringent for this 6 bit DTC to have good INL. When the digital calibration loop settles, the input DCW to the DTC only toggles between n and $n+1$ as very narrow loop bandwidth is chosen for the calibration loop. As a result it only requires that the delay difference between $DCW = n$ and $DCW = n+1$ is much smaller than the TDC resolution. Besides fine incremental time delay, the DTC has to provide delay difference range $\tau_{diff} = \tau_{max} - \tau_{min}$ larger than $3/4$ of the buffer delay because the spacing between $clk1$ and $clk4$ will be $3/4$ of the buffer delay when the calibration loops settle. Two configuration bits $SEL<1:0>$ select the size of the inverter which drives the capacitor array. When $SEL<1:0> = 00$, only one inverter ($\times 1$) is connected to drive the PMOS capacitor array and thus the longest delay difference is generated. When more inverters ($\times 2$, $\times 4$) are connected to the PMOS capacitor array through transmission gates, the maximum delay is reduced and delay resolution also improves. The delay difference range $\tau_{diff} = \tau_{max} - \tau_{min}$ is summarized in Figure 4.13. Post-layout

simulation result is shown in Figure 4.14. When setting $SEL<1:0> = 01$, the maximum delay difference is 35 ps which is much longer than the buffer delay and it can be calculated that the DTC resolution is $35 \text{ ps} / 2^6 = 0.55 \text{ ps}$.

Figure 4.14 DTC post-layout simulation with $SEL<1:0> = 01$

4.4 Measurement Results and Discussions

The whole design has been fabricated in a 65 nm CMOS process and the micrograph of the chip is shown in Figure 4.15. The TDC core area is only $400 \mu\text{m} \times 300 \mu\text{m}$. The TDC chip is packaged inside QFP40 and attached to PCB board for testing. To characterize the prototype, static test, dynamic test and also single shot precision test have been carried out. The core differential oscillator and high speed asynchronous counter consume 1.45 and 0.45 mA respectively when they are enabled

during the incoming pulse width. The rest circuits consume less than 60 μA when operating at 1MS/s sampling rate.

Figure 4.15 Chip micro-photograph.

4.4.1 Static Test

The nonlinearity of the TDC is measured with the statistical code density test. Due to lacking of expensive timing generator, a modified test setup is proposed and shown in Figure 4.16. Two crystal oscillators (TCXO) are adopted as input In_A and In_B . One crystal oscillator is running at 1 MHz and the other crystal oscillator is running at 10 MHz. Although crystals are very precise, their frequency are not exactly integer multiples of another. Effectively the input time pulse width between the rising edge of In_A and In_B to the TDC is like a ramp function. Ideally there would be the same amount of hits in every output bin.

Figure 4.16 Static test setup.

Figure 4.17 Nonlinearity measurements (a) INL (b) DNL.

The measured result is depicted in Figure 4.17 and the INL and DNL are less than 0.5 LSB and 0.12 LSB respectively. As discussed in section II, good linearity performance is achieved though DEM.

4.4.2 Dynamic Test

Dynamic test setup is shown in Figure 4.18. In_B is delayed from In_A through a buffer on PCB. The time width between the rising edge at the digital buffer input and the rising edge at the digital buffer output is the input time pulse width for the TDC. And thus the jitter contribution from the signal source input can be eliminated. In order to modulate the delay, the power supply of the buffer is modulated by an external signal generator.

Figure 4.18 Dynamic test set-up.

Time domain results are plotted in Figure 4.19(a) in which a sinusoidal output can be easily observed. Frequency domain result is shown in Figure 4.19(b). Besides the fundamental frequency, higher order harmonics can be observed due to non-linear voltage to delay transfer function of the external buffer.

(a)

(b)

Figure 4.19 Dynamic test (a) time domain output codes (b) frequency domain FFT results.

4.4.3 Single Shot Precision Test

The single-shot precision (σ value) over a few different length of input pulse has been measured after digital calibration is done and DCWs are locked. Time domain output codes are plotted on the left in Figure 4.20 and histograms of the outputs are plotted on the right in Figure 4.20. As seen in Figure 4.20, the single-shot precision is deteriorated when measuring longer time intervals. Single shot precisions increase from 0.6 LSB to 1.5 LSB as the input time width increases from 3.8 ns to 72 ns.

Figure 4.20 Single shot test results.

The variance in single shot precision test for short input time pulse width is mainly caused by buffer element mismatch. Due to dynamic element matching, different buffer delays contribute to different single shot measurement and output code variation is caused. However, the output code variation caused by element mismatch can be reduced by averaging several output codes. As the input time pulse width becomes longer, the accumulated jitter of the ring oscillator start to dominate the deterioration in single short precision. Although the jitter increases with the input time pulse width, it is not detrimental because repetitive measurements can be adopted to average out jitter error. In conclusion, the single shot accuracy can be improved by averaging because the error caused by element mismatch is randomized by DEM and the error caused by accumulated jitter is random by nature. By averaging 4 adjacent outputs, the single shot precision can be improved by 2 times.

To analyze the relationship between accumulated jitter and output code variation, the ring oscillator output phase noise is measured. The differential ring oscillator output is at 2.6GHz. The oscillator output is divided by 256 using internal frequency divider and the divided clock phase noise is measured and is shown in Figure 4.21.

Figure 4.21 Phase noise of free running ring oscillator output divided by 256.

The proposed TDC targets for 14 bit detection range which corresponds to maximum input of 256 free running oscillation cycles. From the measured phase noise spectrum, the 256 cycle jitter rms value can be calculated as 7.55 ps which corresponds to 1.25 LSB. The measured 1.25 LSB rms jitter is close to the 1.5 LSB single short precision for the maximum input time pulse width demonstrated in the single short precision test.

The measured performance of the prototype is summarized in Table 4.1 and compared to state of art designs. Its power consumption scales with the input time pulse width since the ring oscillator is only enabled during the incoming time pulse width. Furthermore, the asynchronous counters only consume power when the ring oscillator is enabled. The ring oscillator and the high speed asynchronous counter are

the major sources of power consumption. For the maximum input of 98 ns, its power consumption is only 280 μ W.

Table 4.1 Comparison of proposed TDC with others

	[35] 2014 TCASI	[30] 2010 JSSC	[34] 2010 JSSC	[83] 2013 TCASI	[84] 2013 JSSC	This work
Process (nm)	130	65	130	350	32	65
LSB (ps)	7	4.8	8	10	3.5	6
# of bits	11	7	12	15	6	14
Detect Range (ns)	14	0.59	33	160	0.224	98
fs (MHz)	1	50	15	3	40	1
Power (mW)	0.329	1.65	7.5	13	3	0.28
Area (mm ²)	0.28	0.068	0.26	0.3	0.004	0.12
Structure	3D vernier	2D vernier	Vernier ring	2-step	Re- circulate	Parallel sampling
INL (LSB)	1.5	-1-3	--	--	--	0.5
DNL (LSB)	0.8	-1-0.8	--	0.04	<0.8	0.1
Single shot (ps)	< 20.8	--	< 8	17.2	--	< 11

To summarize, TDC architecture based on parallel sampling ring oscillator with power gating and DEM is presented in this chapter. The prototype has been designed and implemented in a CMOS 65 nm technology. This architecture has achieved large

detection range of 98ns with 6 ps/LSB and it is compact at the same time. The prototype consumes 280 μ W from 1.2 V power supply at sampling frequency of 1 MHz. The prototype occupies 0.4 mm $\times$ 0.3 mm² chip area. The measured INL and DNL are 0.5 LSB and 0.1 LSB respectively. Measurements of the prototype IC also demonstrate single shot precision of less than 11 ps.

Chapter 5. Design of Low Power Fractional-N Counter-assisted DPLL

In this chapter, DPLL based wideband low power FMCW synthesizer for radar application is presented. Firstly, basic concepts in radar applications are briefly introduced. Then, linear frequency modulation (LFM) waveform synthesizers are reviewed. Next, a low power FMCW synthesizer based on DPLL approach is presented.

5.1 Introduction

5.1.1 Pulse Compression Radar Using LFM Waveform

Pulse compression technique is commonly adopted in radar systems to reduce required peak transmission power and maintain average power. The waveform for pulse compression should have a narrow, well defined autocorrelation peak. So it should have substantial bandwidth and also need to spread the total energy evenly throughout the duration of the pulse [85]. Linear frequency modulated (LFM) waveform, which is also referred to as chirp signal, is one of the commonly used waveform for pulse compression in radar systems. Figure 5.1 illustrates the concept of LFM pulse compression. Figure 5.1(a) and 5.1(b) shows the transmitted pulse frequency and amplitude versus time respectively. The transmitted waveform has constant amplitude and its frequency increases linearly from f_1 to f_2 over the duration of the pulse. Figure 5.1(c) shows the compressed pulse with higher peak and narrower duration. On reception, the frequency modulated signal is passed through matched filter which perform correlation between the received signal and the original copy of

the transmitted signal. The matched filter compresses the received signal to a pulse of time width of $\tau = 1/B$, where $B = f_2 - f_1$. In this case, the matched filter output is proportional to $(\sin \pi Bt)/\pi Bt$. The peak power of the pulse is increased by the pulse compression ratio $BT = T/\tau$ [86]. In short, pulse compression technique is used to compress energy spread over pulse duration T to be within a much shorter duration τ .

(a) transmit waveform frequency versus time

(b) transmit waveform amplitude versus time

(c) compressed pulse amplitude versus time

Figure 5.1 Pulse compression of LFM waveform

The pulse compression ratio (PCR) is defined as following:

$$PCR = \frac{\text{duration_of_tranmitted_pulse}}{\text{duration_of_received_pulse_after_matched_filtering}} = \frac{T}{\tau} \quad (5-1)$$

The matched filter mentioned before may be implemented by digital correlation processing for any waveform or else a stretch processing approach for a LFM waveform.

5.1.1.1 Correlation Processing

The frequency domain digital pulse compression processor operates on the principle that the discrete Fourier transform of the time convolution of two sequences is equal to the product of the discrete Fourier transforms of each of the time sequences[87].

The process of digital correlation processing is shown in Figure 5.2. Firstly, the received signal $y(t)$ is down converted to lower frequency and digitized. FFT (fast Fourier transform) is performed on the digitized input. $h(n)$ represents a digitized copy of the transmitted LFM waveform and FFT is also performed on it. Instead of performing correlation of received signal and $h(n)$, multiplication in the frequency domain is performed and then an IFFT processing converts it back into time domain. In this architecture, the ADC input bandwidth must be greater than the waveform bandwidth. For example, if the received signal has bandwidth of 1 GHz, the ADC must sample at rate larger than 2GHz to avoid aliasing.

Figure 5.2 Correlation processing

For a chirp with bandwidth of B and duration of T , correlation processing gives a narrow pulse of $1/B$ width in time domain. So the range resolution can be calculated by the following equation:

$$R_{res} = \frac{c \times t_{res}}{2} = \frac{c \times \frac{1}{B}}{2} = \frac{c}{2B} \quad (5-2)$$

5.1.1.2 Stretch Processing

Stretch processing is a technique for performing pulse compression of wideband waveforms using a signal processor with bandwidth that is much smaller than the waveform bandwidth without loss of signal to noise ratio or range resolution [87].

Figure 5.3 shows the architecture of the stretch processing receiver architecture.

Figure 5.3 Stretch processing receiver architecture

As illustrated in Figure 5.4, transmitter amplifies and transmits LFM waveform. Targets and clutter reflect part of the electromagnetic energy and receiver detects those reflections. In the receiver, the received signal $y(t)$ is firstly amplified and then it is mixed with a local LFM signal $r(t)$ which is the same as the one transmitted. Assume that the target is at distance R , it takes round-trip time of $2R/c$ to receive the reflection,

where c is the speed of light. Since the received signal $y(t)$ and the local LFM signal $r(t)$ are the same copy with only a time offset, the mixer output for a single target is a constant frequency. The constant frequency output of the mixer or the frequency offset is related to the round trip time of flight and the chirp slope. The beat frequency can be calculated by the following equation:

$$f_b = \frac{B}{T} \times TOF = \frac{B}{T} \times \frac{2R}{c} \quad (5-3)$$

Figure 5.4 Stretch processing of LFM waveform

The bandwidth of the signal after stretch processing depends on the frequency modulation rate and the target range. Within short range, the signal bandwidth after stretch processing can be reduced to a few megahertz. Consequently, only a low sampling rate ADC is needed. A highly linear frequency chirp is required to avoid degradation of ranging accuracy. Non-linearity in the frequency modulation severely degrades the radar performances for large distances.

5.1.2 Pulsed Radar and FMCW Radar

5.1.2.1 Pulsed Radar

Pulsed radar is the most widely adopted approach in the existing radar systems. It is more suitable for long range application as it does not suffer from leakage issue which presents in the continuous wave radars. Detection range of pulsed radar can be extended by increasing the transmission power. As shown in Figure 5.5, the pulse duration only occupy a portion of the whole modulation period T_m .

Figure 5.5 Pulsed radar transmitter waveform with LFM

Since the pulse duration is short, pulsed radar transmits high peak transmission power. This leads to large dimensions of the onboard RF power amplifier and the power supply. The high peak power requirement make CMOS technology unsuitable for pulsed radar implementation due to low supply voltage and limited gain at millimetre-wave band [88].

5.1.2.2 FMCW Radar

As shown in Figure 5.6, FMCW radars with LFM continuously transmit constant transmission power. As a result, FMCW radars require much lower peak transmission power compared to pulsed radar. Hence FMCW radars demand less on power device

and power management units for FMCW radars can also be made compact. Therefore, the FMCW radar is suitable for realizing a CMOS radar integrated IC chip.

Figure 5.6 FMCW radar transmitter waveform with LFM

Because of the simultaneous transmission and reception, transmission power can always leak from the transmitter into the receiver. The leakage may introduce additive noise above the thermal noise level and limits FMCW radars only for short range applications [89]. Thus it is important to maximize transmitter–receiver isolation in FMCW radar system. One way to improve the isolation is to use separate antennas (e.g. horn antenna with good directivity) for the transmitter and receiver [90, 91]. In addition, leakage cancellation methods have been developed to mitigate leakage effects [92, 93].

5.1.3 LFM Synthesizer Architectures

5.1.3.1 DDFS Based Architecture

DDFS (Direct digital frequency synthesizer) is widely used in radar systems and communication systems such as frequency hopping systems, spread spectrum communication and so on. It can provide fast frequency switching and also high frequency resolution [94]. The architecture of a conventional DDFS as shown in Figure 5.7 consists of the following basic building blocks: a digital phase accumulator,

a phase-to-sine amplitude ROM look-up table, and a linear DAC (digital to analog converter).

Figure 5.7 DDFS block diagram

During every input clock cycle, the phase is incremented by the value of the frequency control word (FCW). If the FCW is a constant value, then DDFS generate a constant output frequency according to the following equation:

$$f_{out} = \frac{FCW}{2^N} f_{CLK} \quad (5-4)$$

In brief, the reference clock frequency is divided down in DDFS. DDFS implementation can provide superior output frequency tuning resolution. As an open loop system, DDFS also features fast frequency (or phase) hopping speed with no settling issues.

However, a high frequency and stable reference oscillator is a prerequisite for broadband and high performance DDFS implementation, which impacts the total system costs significantly. Due to the high speed input clock and high speed high resolution DAC, DDFS consume high power and large area.

Furthermore, additional mixers and oscillators are usually adopted to up convert the LFM signal or chirp signal generated by DDFS to a higher frequency for transmission as shown in Figure 5.8.

Figure 5.8 Chirp generation with DDFS and mixer

Frequency synthesis using DDFS is precise and agile. But it consumes too much power. In addition, the maximum bandwidth which can be generated by DDFS is limited by its input clock and is usually less than 40 percent of the input clock.

5.1.3.2 DDFS Driven Integer-N PLL

Another popular architecture involving DDFS is using a low frequency DDFS to drive an integer-N PLL as shown in Figure 5.9. The low frequency DDFS serves as the reference clock for the integer-N PLL. The integer-N PLL multiplies the bandwidth width generated by the DDFS and also multiplies the centre frequency. Consequently the requirements on the DDFS can be greatly relaxed.

Figure 5.9 Chirp generation using DDFS driven integer PLL

In [88], a low performance DDFS ($f_{clk}=1.2\text{MHz}$, $W=8$ bits) drives an integer PLL to generate wideband LFM waveform. The DDFS only generates chirp with bandwidth of 600 kHz and the integer-N PLL multiplies it to 614 MHz.

The problem with low performance DDFS is the low frequency update rate. The low performance DDFS output frequency versus time is like a stair case as shown in Figure 5.9 and it can be smoothed by the PLL input to output low pass transfer function. The cut-off frequency of the PLL transfer function should be narrow enough to filter out the stair case shape. The cut-off frequency of the PLL transfer function should also be much higher than the triangular modulation frequency of the FMCW signal $1/T_m$. In [88], the FMCW modulation period is $500\text{ }\mu\text{s}$ which corresponds to 2 kHz. The PLL loop bandwidth is chosen as 30 kHz which is much smaller than DDFS update rate of 400 kHz to linearize the stair case input and much larger than 2 kHz to pass the LFM (chirp) modulation.

Comparing this approach with the DDFS approach, it supports a much wider bandwidth of 614 MHz with much lower power consumption. It only needs low performance DDFS and integer-N PLL. However, the low performance DDFS generates high phase noise floor which determines the in-band phase noise level of the PLL output. Consequently, only narrow loop bandwidth is allowed for the PLL to filter out this noise as much as possible. In addition, this approach is not as agile as the DDFS approach since the FMCW modulation frequency need to be much smaller than the PLL closed loop transfer function cut-off frequency.

5.1.3.3 Fractional-N PLL

Similar to DDFS, fractional-N PLL can achieve very fine frequency resolution. As long as the FMCW modulation frequency ($1/T_m$) is much lower than the PLL closed loop transfer function cut-off frequency, excellent linearity can be achieved. Figure 5.10 shows the implementation of FMCW synthesizer using fractional-N PLL [95].

Figure 5.10 Chirp generation using fractional PLL

Σ - Δ modulator drives the modulus divider and changes the divider ratio dynamically to achieve fractional frequency resolution. A modulation control logic block is added, which generates the input digital words to the Σ - Δ modulator. The Σ - Δ modulator input digital word is generated in the way to ensure the output frequency is linearly modulated according to the bandwidth B and modulation period T_m . A proper loop bandwidth of the PLL needs to be selected to pass the modulation to the output and minimize output phase noise.

5.1.4 Summary

FMCW radar systems find their applications in automotive anti-collision, precise ranging, synthetic aperture radar and others. Because of constant low transmission power and low data rate, FMCW radars are much more compact than pulsed radar systems. It is crucial for a FMCW frequency synthesizer to be compact, low power, be able to generate linear and low phase noise frequency sweep with wide output bandwidth [96]. Conventionally, direct digital frequency synthesizer (DDFS) is widely adopted in radar systems as it can provide fast frequency switching and also fine frequency resolution [94]. Unfortunately, DDFS is power hungry and additional mixers and oscillators are usually needed to up convert the DDFS output to higher frequency for transmission [97]. FMCW synthesizers based on phase locked loop (PLL) have been developed in [98-102]. Those PLL based architectures include DDFS driven integer-N PLL, fractional-N PLL, and offset PLLs. PLL based architectures consume less power than DDFS based synthesizers and still can provide excellent linearity due to closed loop feedback. However, the LFM modulation frequency should be kept to be much lower than the PLL closed loop bandwidth. Direct

modulated oscillators have also been used as FMCW synthesizer for very short range radar applications.

5.2 DPLL Based FMCW Synthesizer

A low power fractional-N counter-assisted DPLL based FMCW synthesizer is presented in this section. This DPLL based FMCW synthesizer does not need any DDS circuit block and thus it is a low cost and low power system. Time to digital converter (TDC), digital loop filter and digital controlled oscillator (DCO) are adopted to replace phase frequency detector (PFD), RC loop filter and voltage controlled oscillator (VCO) in traditional charge pump based PLLs. Compare to analog PLL approach, the DPLL approach demands less on the voltage head room, silicon area and also does not have analog filter leakage issues. Furthermore, it is much more convenient to incorporate digital calibration into DPLL based architectures. As discussed earlier, PLL based FMCW synthesizer approach can only support modulation frequency which is much lower than the PLL closed loop bandwidth. With assistance of digital calibration, continuous 2 point modulation over large output bandwidth can be realized for DPLL based approach.

5.2.1 DPLL Architecture

The proposed X band FMCW synthesizer adopts a DCO structure which consists of a VCO driven by a current digital to analog converter (IDAC) as proposed in [98]. In conventional DPLL, a high resolution voltage DAC which is used to drive the VCO is needed to reduce the output phase noise caused by limited frequency resolution. For DCO implemented with switched capacitance, its tuning curve is not continuous due to segmented structure consisting of coarse and fine tuning, and thus DCO with switched

capacitance is not suitable for continuous frequency sweep. The combination of a low resolution current DAC and an off-chip capacitor instead of a high resolution voltage DAC simplifies the DPLL design. The phase noise performance of this architecture has been analyzed. The synthesizer composed of frequency dividers, TDC, high speed counter, digital loop filter, current DAC and VCO has been implemented in a 65nm CMOS process and its block diagram is shown in Figure 5.11.

The reference clock is from a temperature compensated crystal oscillator (TCXO) of about 50 MHz. In the DPLL, an off-chip capacitor of 10 nF integrates the output current from a current DAC. The capacitor voltage is the control voltage (V_c) for the VCO. The VCO output is first divided by frequency dividers. The divided clock f_{div} is quantized by a TDC and a high speed counter. The differentiator converts phase information to frequency information. Then the measured frequency is compared with the digital frequency control word (FCW) to determine the error. The error is processed by the digital loop filter to close the feedback loop. The clock recovery (CKR) block is added for generating proper trigger signal for the registers.

Figure 5.11 DPLL based FMCW synthesizer architecture

5.2.2 Analysis of Noise Contribution

In this DPLL architecture, several major noise sources contribute to the output phase noise which include the TDC quantization noise (Δt_{res}), current DAC quantization noise (Δi_{res}) and VCO phase noise (Φ_{n_vco}).

The phase noise analysis is similar to analog PLL phase noise analysis. In DPLL architectures, TDC is used to quantize the divided clock phase and the TDC quantization noise mainly impacts the in-band phase noise due to the low pass characteristic of the DPLL transfer function from input to output. The introduced in-band phase noise due to TDC quantization noise is given by (5-5).

$$PN = \frac{(2\pi)^2}{12} \left(\frac{\Delta t_{res}}{T_{DCO}} \right)^2 \frac{1}{f_{ref}} \quad (5-5)$$

Similarly, transfer functions of VCO phase noise (Φ_{n_vco}) to output phase noise and Current DAC quantization noise (Δi_{res}) to output phase noise can be derived. In this design a second order digital loop filter is implemented and the close loop bandwidth is set to 400 KHz. The digital loop filter consists of a pole at origin, a zero lower than the close loop bandwidth and another pole beyond the close loop bandwidth. This close loop bandwidth is chosen to be much larger than the modulation frequency to pass the modulation signal without distortion. Meanwhile, the choice of close loop bandwidth also takes into consideration of output phase noise optimization.

Figure 5.12 shows the output phase noise contribution from each of the noise sources according to phase domain model. The TDC quantization step Δt_{res} is 24 ps according to post-layout simulation. The current DAC resolution Δi_{res} is 0.5 μ A and the VCO exhibits -105 dBc/Hz phase noise at offset of 1 MHz. The pink, red and blue

curves in Figure 5.12 represent the phase noise due to current DAC resolution Δi_{res} , TDC quantization noise Δt_{res} and VCO phase noise Φ_{n_vco} respectively. The parameters mentioned above are used as design values in the circuit design.

Figure 5.12 Phase noise contribution simulated by Matlab

5.2.3 Circuit Implementations

5.2.3.1 LC Oscillator

Figure 5.13 shows the schematic of the VCO. The oscillator adopts complimentary cross coupled pairs for its higher current efficiency. It also eliminates the biasing transistor to remove the thermal and flicker noise contribution from the biasing transistor [103].

The 0.5 nH symmetric inductor has Q value of about 10 at 10 GHz. The frequency is tuned by accumulation mode MOS varactors for their monotonic tuning

behaviour and large C_{max} to C_{min} ratio [104]. The quality factor Q of the accumulation mode MOS varactors is about 12.5 at frequency of 10 GHz.

Figure 5.13 Schematic of VCO circuit

The simulated tuning range is shown in Figure 5.14 and it extends from 8.2 GHz to 11.9 GHz. The simulated phase noise performance of the VCO is shown in Figure 5.15 and the VCO exhibits phase noise level of -108 dBc/Hz at 1MHz offset for 10 GHz oscillation frequency.

Figure 5.14 VCO tuning curve simulation result

Figure 5.15 Simulated phase noise performance of VCO

5.2.3.2 Frequency Dividers

For the first stage frequency divider, a current mode logic (CML) divider is adopted for its higher operating frequency as shown in Figure 5.16. PMOS load is adopted for compact layout and bottom biasing current source is removed for low voltage operation in this CML frequency divider implementation. The second stage frequency divider is a true single phase clock (TSPC) frequency divider for low power consumption. .

Figure 5.16 CML first stage frequency divider

5.2.3.3 High Speed Counter

The counter in the proposed architecture counts at 2-3 GHz clock speed. To reduce the power consumption of high speed synchronous counter, a splitting counter structure is adopted [26]. The 8-bit high speed synchronous counter consists of a 2-bit synchronous counter for the two least significant bits, another 6-bit gated synchronous counter for the remaining most significant bits, and a gating control signal generator. The input clock frequency of the 6-bit synchronous counter is reduced to one quarter of the input clock frequency f_{div} , which leads to lower power consumption. The counter schematic is shown in Figure 5.17.

Figure 5.17 8-bit splitting structure high speed synchronous counter

Figure 5.18 illustrates the detailed signal timing of the splitting structure high speed counter. Input enable signal En is assumed to be '1'. The goal is to trigger the 6-bit synchronous counter with $CLK4$ whose clock rate is $1/4$ of the input $CLKIn$. Furthermore, the rising edge of $CLK4$ should occur near the moment when $Q[1:0]$ change from '11' to '00'. Signal det_a changes to '1' when $Q[1:0] = 10$. Then signal det_a is delayed through two flip-flops to generate signal $CTRL$ whose envelop select one out of every 4 $CLKIn$ pulse. The 6-bit synchronous counter is only triggered when $Q[1:0]$ changes from '11' to '00' and thus the output bits of the 2-bit and 6-bit synchronous counter are aligned. Due to their higher operating speed, TSPC flip-flops are adopted for implementation of this high speed counter. In Figure 5.18, t_{and2} and t_{and3} represent combinational circuit delays and t_{cq} represents the clock to data output delay of TSPC flip-flops.

Figure 5.18 Timing waveform for splitting high speed counter

Figure 5.19 shows the current consumption of this high speed counter from a 1.2V power supply in post-layout simulation. It can be observed that its power consumption increase linearly with input clock frequency, and thus its power consumption is dominated by dynamic power.

Figure 5.19 Current consumption of high speed counter

5.2.3.4 Time to Digital Converter

In the proposed FMCW frequency synthesizer, a proposed gated delay chain based TDC performs the phase error detection. The gated delay chain TDC consists of 3 parts: chain of delay elements and sensing flip-flops, decoding logic, and normalization calculation circuit. The TDC block diagram is shown in Figure 5.20.

Fine delays are generated using buffers consisting of 2 inverters. Buffers are used instead of inverters to eliminate the mismatch between rise and fall time. The total delay provided by the delay chain must be larger than $2 \times T_{div}$ (period of divided clock f_{div}) in order to perform normalization. Post layout simulation shows that the buffer delay varies from 17 to 33 ps under different PVT corners. In this implementation, total 61 delay stages are connected in series. The divided clock f_{div} is about 2.5 GHz and thus the digital gates driven by f_{div} consume high power. In order to reduce power consumption, the f_{div} input is gated and is only enabled for slightly larger than $2 \times T_{div}$ duration in every reference clock period. The gated operation is achieved by generating the control signal with f_{ref} and delayed f_{ref} (i.e. f_{ref_d61}) at the output of the delay chain. Conventional digital flip-flops in digital circuit is not suitable for this TDC application due to metastability characteristic [105]. Sense amplifier based flip flops are implemented instead to minimize metastability.

The timing diagram of the TDC operation is shown in Figure 5.21. The reference clock f_{ref} is delayed by steps of τ which equals to the buffer delay. The delayed reference clocks sample the divided clock f_{div} from the frequency divider and record the waveform of f_{div} in steps of τ . From the sampled values, the rising positions of the divided clock f_{div} can be decoded. Furthermore, the relative position between the divided clock f_{div} and reference clock f_{ref} can be determined and normalized to divided clock period T_{div} through digital division operation.

Figure 5.20 Gated delay chain based TDC block diagram

Figure 5.21 Timing diagram of TDC operation

5.2.3.5 Other Circuits

A low power 7 bit current DAC is designed for charging and discharging the capacitor. The current DAC consists of PMOS current source for charging the integrating capacitor, NMOS current source for discharging the integrating capacitor, and binary-to-thermometer decoder for converting input binary code to thermometer

code. The current resolution is 0.5 μA which is proved to be sufficient for phase noise performance in the previous section.

5.2.4 Measurement Results

The proposed X band DPLL based FMCW frequency synthesizer has been implemented in 65 nm CMOS process and the chips are packaged using QFN40 packages and tested on PCB.

Figure 5.22 shows the overall chip layout of the DPLL based FMCW synthesizer. The total core circuit area is 0.2 mm² excluding pads.

Figure 5.22 Layout of the FMCW synthesizer Chip

Figure 5.23 shows the measured open loop VCO tuning curve, in which the tuning range is 8 GHz - 11 GHz for control voltage of 0.2 - 1.1 V. Its measured output spectrum and close loop phase noise performance str shown in Figure 5.24 and Figure 5.25 respectively. The measured fractional spur is below -50 dB.

Figure 5.23 Measured VCO open loop tuning curve

Figure 5.24 Measured synthesizer output spectrum

Figure 5.25 Measured phase noise

Sweep tests have been performed in which the output frequency is swept between 8 GHz and 11 GHz up and down in 2 ms by sweeping digital input FCW. Figure 5.26 shows the wideband output spectrum. The spectrum is not flat and this is due to the poor output buffer design and effects of parasitics. The frequency flatness of the generated chirp signal can be improved significantly after the limiting amplifier following the chirp synthesizer, which is normally employed in the FMCW transmitter after the chirp synthesizer and to drive the final stage of power amplifier. Figure 5.27 shows the control voltage of the VCO as the output frequency is sweeping. Although the open loop VCO tuning curve is very nonlinear, the DPLL can compensate it by applying nonlinear control voltage in the opposite direction to generate linear frequency sweep.

Figure 5.26 Measured FMCW output spectrum

Figure 5.27 Measured VCO control voltage waveform

In addition to the frequency domain test, the instantaneous frequency is measured during sweep test and plotted in Figure 5.28(a) and the triangular modulation is clearly observed. To quantify the linearity, its definition is given in Equation (5-6) [106, 107]. The instantaneous frequency error is plotted in Figure

5.28(b). The measured peak to peak frequency error is about 1.2 MHz and the rms frequency error is about 140 KHz.

$$linearity = \frac{frequency_error_rms}{bandwidth} \quad (5-6)$$

(a) Measured FMCW synthesizer output frequency

(b) Instantaneous output frequency error

Figure 5.28 Measured FMCW synthesizer output frequency versus time

Table 5.1 FMCW synthesizer performance comparison

	[88] JSSC 2010	[108] JSSC 2010	[101] ICC 2009	[99] ISSCC 2007	[102] COMCA S 2008	This work
Technology	90 nm	65 nm	0.25 μ m SiGe	0.25 μ m SiGe	180 nm	65 nm
fref (MHz)	77	700	25	37.1	24.557	50
fc (GHz)	77	77	5	19	5.8	10
Bandwidth (MHz)	614	700	1200	513	150	3000
Linearity ($\times 10^{-4}$)	17.1	0.9	--	--	--	0.5
Area (mm ²)	0.6	0.24	1.15	--	--	0.2
Power (mW)	101	73	100	157	25	8.4

The FMCW synthesizer performance is summarized and compared with others in Table 5.1. The proposed design achieves much lower power consumption through elimination of the high resolution voltage DAC and incorporation of the gated delay line based TDC. The output bandwidth is 3 GHz which corresponds to 5 cm ranging resolution in radar applications.

The chapter has presented a FMCW synthesizer based on DPLL approach. Phase noise performance of this particular architecture is analyzed. The FMCW frequency synthesizer has been implemented in a 65 nm CMOS technology. With less than 9 mW power excluding output buffer power consumption, it achieves 3 GHz output bandwidth which corresponds to 5 cm ranging resolution in radar application. This work eliminates high resolution voltage DAC by adopting DPLL architecture with

current DAC. The gated delay line based TDC helps to reduce power consumption further. Furthermore, it is easy to incorporate digital calibration scheme into DPLL based architectures to achieve two point modulation for faster modulation rate.

Chapter 6. CONCLUSION AND FUTURE WORK

This chapter will conclude the thesis and shed light on the possible improvement for future work.

6.1 Conclusion

This thesis conducts a comprehensive study on each building blocks of DPLL: TDC, DCO, high speed counter, and frequency divider. Major contributions are listed below:

To increase the input locking range, a ring oscillator based ILFD utilizing dual injection technique is proposed. Its locking range is from 1.2 GHz to 20.7 GHz without any tuning at 0 dBm injection power level. The proposed ILFD is compact with the core only occupying $15\ \mu\text{m} \times 30\ \mu\text{m}$ and does not need any extra controls, making it suitable for integrated wideband DPLL.

To improve the TDC resolution without requiring additional power, parallel sampling technique is proposed. A TDC based on parallel sampling ring oscillator with power gating and dynamic element matching (DEM) is proposed. It is capable of achieving sub-gate-delay resolution and large detection range at the same time with low power consumption. Furthermore, the parallel sampling technique can also be combined with other TDC architectures to further improve their performance.

A FMCW synthesizer based on DPLL approach has been proposed. With less than 9 mW power excluding output buffer power consumption, it achieves 3 GHz output bandwidth which corresponds to 5 cm ranging resolution in radar application. This work eliminates high resolution voltage DAC by adopting DPLL architecture

with current DAC. The proposed gated delay line based TDC helps to reduce power consumption further. Furthermore, it is easy to incorporate digital calibration scheme into DPLL based architectures to achieve continuous wideband two point modulation for faster modulation rate.

Some of the key technology is under patent disclosing.

6.2 Future Work

Several possible future works can be considered.

Firstly, two point modulation schemes can be adopted for the DPLL based FMCW synthesizer presented in chapter 5 to achieve faster FMCW rate. Two point modulation schemes have been adopted in analog phase locked loops for the purpose of frequency modulation. Its performance is mainly limited by gain mismatch between the two different paths and usually gain calibration needs to be performed. In DPLL, the oscillator is controlled by digital words, and thus two point modulation can be achieved by injecting digital words instead of analog voltage for controlling the frequency. Clearly the DPLL offers advantage over the analog PLL in this aspect. With DPLL architecture, it is easier to implement calibration and two point modulation compared to analog counter part. When the FMCW modulation frequency $f_m=1/T_m$ is much smaller than the loop bandwidth (less than 2% of PLL loop bandwidth), the modulation can be passed to the output without distortion and excellent linearity is achieved. When the $f_m=1/T_m$ gets bigger, the modulation will be distorted when passed to the output. When the frequency modulation period T_m is small, a calibration can be done first by generating a FMCW waveform with the same signal bandwidth with modulation period of $k \cdot T_m$. During the calibration, total $k \cdot T_m \cdot f_{ref}$

current DAC inputs are generated. Next every adjacent group of k samples are summed to become one sample. Consequently, $T_m \cdot f_{ref}$ samples are generated. Next these $T_m \cdot f_{ref}$ are injected to the DAC input when generating fast linear frequency modulation. With this method, no gain calibration is need. Two point modulation can effectively extend the PLL bandwidth. Furthermore, the stored DAC input inherently compensates the nonlinear DCO tuning curve over the entire tuning range, and thus enables sweeping over a large bandwidth in short sweep cycles.

Secondly, spur reduction technique can be developed to mitigate TDC nonlinearity impact and to reduce DPLL spur level which is another major limitation of DPLL.

Thirdly, the parallel sampling technique can also be combined with other TDC architectures to further improve their performance.

AUTHOR'S PUBLICATIONS

Journal papers:

(1) **S. Liu**, Y. Zheng, W. M. Lim, and W. Yang, "Ring Oscillator Based Injection Locked Frequency Divider Using Dual Injection Paths," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 5, pp. 322-324, May 2015.

(2) **S. Liu** and Y. Zheng, "A Low-Power and Highly Linear 14-bit Parallel Sampling TDC With Power Gating and DEM in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 3, pp. 1083-1091, Mar 2016.

(3) **S. Liu** and Y. Zheng, "A Fractional-N Counter-Assisted DPLL with Parallel Sampling ILFD," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1361-1373, Jun 2016.

(4) Y. Zheng, **S. Liu**, S. X. Diao, Y. Gao and C.-H. Heng, "A UWB Impulse Transceiver with Adaptive Beam-forming and Diversity," *IEEE Trans. Microw. Theory Tech.*, submitted.

(5) Y. Wang, L.H. Lou, B. Chen, Y. Zhang, K. Tang, **S. Liu** and Y. Zheng, "A Ku-band synthetic Aperture FMCW Radar Transceiver for UAV Synthetic Aperture Radar Imaging in 65nm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, submitted.

Conference papers:

(6) **S. Liu**, Y. Zheng, and X. He, "Design of a wideband low power FMCW synthesizer in 65 nm CMOS for radar applications," in *Proc. ISCAS*, 2014, pp. 1776-1779.

(7) Y. Wang, K. Tang, Y. Zhang, L.H. Lou, B. Chen, **S. Liu** and Y. Zheng, "A Ku-band 260 mW FMCW synthetic Aperture Radar TRX with 1.48GHz BW in 65nm CMOS for micro-UAVs," in *ISSCC Dig. Tech. Papers*, 2016, pp. 240-241.

(8) L. Lou, **S. Liu**, B. Chen, K. Tang and etc, "A broadband CMOS LC voltage-controlled oscillator for FMCW synthesizer", *International Symposium on Integrated Circuits (ISIC)2014*.

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