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A Multi-mode Sensor: Merge an Ambient Light Sensor Into a CMOS Image Sensor

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Abstract

Ambient light sensors are quite often used in the portable electronic devices. In a smartphone, the ambient light sensor enables automatic control of display backlight brightness over a wide range of illumination conditions from a dark environment to direct sunlight. The control reduces the power consumption and improves visibility under varying lighting conditions.

The conventional ambient light sensor consists of two parts: photodetectors and conversion circuits. A typical conversion circuit can be current-mode analog-to-digital convertor (ADC); pulse-width modulation (PWM) module; or pulse-frequency modulation (PFM) module. In this thesis, a new conversion circuit is proposed. The proposed ADC employs a two-step architecture combined with the time-domain measurement technique. A current-mode ADC is adopted as the coarse ADC. The residue current left by the coarse A/D conversion is finely quantized by a PWM module. The proposed architecture can improve the accuracy of detection, since PWM module can correct the possible coarse conversion errors. Meanwhile, it can shorten the conversion time, since the input current of the PWM module is compressed by the coarse ADC into a small range.

A multi-mode sensor can be developed by merging the proposed ambient light sensor into a CMOS image sensor. Since power consumption plays an important role in the sensor device, a low-power application can be achieved by separating the power supply and switching them in different modes. In other words, during ambient light sensing, the circuits for picture/video readout are in standby mode and do not consume power; and vice versa.

The thesis presents the design of the proposed multi-mode sensor. The chip with 64×64 pixel array is implemented in AMS $0.35\ \mu\text{m}$ 2P4M CMOS technology. In the following sections of the thesis, it will show the whole design flow of the proposed sensor chip.

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Contents

Abstract	i
Acknowledgments.....	iii
Contents	v
List of Figures	ix
List of Tables	xiii
List of Abbreviations	xiv
Chapter 1 Introduction.....	1
1.1 Background	1
1.2 Motivation and Objective	3
1.3 Thesis Organization.....	7
Chapter 2 Fundamentals of CMOS Image Sensor.....	9
2.1 Overall Architecture and Operating Principle	9
2.2 Photodetection	11
2.3 Basic Pixel Architectures	15
2.3.1 PPS.....	15
2.3.2 3T APS.....	16
2.3.3 4T APS.....	18
2.4 Correlated Double Sampling	20
2.5 Analog-to-Digital Convertor	22

2.6	Specifications of CMOS Image Sensor	24
2.6.1	Conversion Gain	24
2.6.2	Full Well Capacity	24
2.6.3	Sensitivity	25
2.6.4	Dark Current	25
2.6.5	Dynamic Range.....	27
2.6.6	Fixed Pattern Noise.....	27
2.6.7	Fill Factor.....	28
2.6.8	Resolution	28
2.6.9	Power Consumption.....	29
Chapter 3	Smart Applications in CMOS Image Sensor	31
3.1	Pulse Modulation.....	31
3.2	Ambient Light Sensor	35
3.3	Multi-mode Image Sensor	38
Chapter 4	Design of a Multi-mode Sensor which Merge an Ambient Light Sensor into a CMOS Image Sensor	45
4.1	Proposed Sensor Architecture and Operating Principle	45
4.2	Circuit Modules Design.....	47
4.2.1	Pixel and Column Circuit.....	47
4.2.2	Two-step Current-mode ADC.....	53
4.2.3	Motion Detector	66

4.3	Sensor Implementation	68
4.4	Simulation and Testing Results	72
4.4.1	Testing Setup	72
4.4.2	Testing Results	77
Chapter 5	Design Improvement: a Two-step Current-mode ADC with Calibration Schemes	81
5.1	Calibration Scheme I	82
5.2	Calibration Scheme II	83
Chapter 6	Conclusions and Future Work	85
6.1	Conclusion	85
6.2	Future Work	87
	Bibliography	89

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List of Figures

Figure 1-1: Front facing camera and ambient light sensor on the mobile phone.	2
Figure 1-2: General diagram of a conventional CMOS image sensor	4
Figure 1-3: Resistive coupling method to merge the two types of sensors	5
Figure 2-1: Architecture of a CMOS image sensor	10
Figure 2-2: Photo-generated carriers in a semiconductor [2]	12
Figure 2-3: P-N junction photodiode without light illumination [27]	14
Figure 2-4: P-N junction photodiode with light illumination [27]	14
Figure 2-5: Pixel architecture of PPS.....	15
Figure 2-6: Pixel architecture of 3T APS	16
Figure 2-7: Timing diagram of the control signals in 3T APS	16
Figure 2-8: Pixel architecture of 4T APS	18
Figure 2-9: Timing diagram of the control signals in 4T APS	18
Figure 2-10: Basic CDS circuit.....	20
Figure 2-11: Serial ADC implementation in CMOS image sensor	23
Figure 2-12: Column parallel ADC implementation in CMOS image sensor	23
Figure 2-13: In-pixel ADC implementation in CMOS image sensor	23
Figure 2-14: Three dominant sources of dark current (online resource)	26
Figure 3-1: Operating Principle of PM imaging technology	32
Figure 3-2: PM imaging categories (a) PWM (b) PFM	33

Figure 3-3: Sample architecture of a PWM pixel [7]	35
Figure 3-4: Block diagram of a sampled ambient light sensor [8]	36
Figure 3-5: Architecture of the sampled PFM circuitry [8]	37
Figure 3-6: Test result of temperature characteristics without illumination [8]	38
Figure 3-7: Sensor operational modes (a) image mode (b) communication mode [10]	39
Figure 3-8: Architecture of the proposed pixel circuit (a) overview (b) image mode (c) communication mode [10]	40
Figure 3-9: Equivalent circuit structure in communication mode [10]	41
Figure 3-10: Architecture of the proposed dual-mode sensor [11]	42
Figure 3-11: Architecture of the proposed reconfigurable ADC [11]	43
Figure 4-1: Architecture of the proposed multi-mode sensor	46
Figure 4-2: Architecture of the column circuit	48
Figure 4-3: Layout view of the 3T pixel	49
Figure 4-4: Schematic of the CDS circuit	50
Figure 4-5: Schematic of the CDS amplifier	51
Figure 4-6: Simulation result of the CDS amplifier	52
Figure 4-7: Timing diagram of the control signals in CIS mode	53
Figure 4-8: Architecture of the proposed two-step current-mode ADC	55
Figure 4-9: Architecture of the coarse SAR ADC	57
Figure 4-10: Schematic of the 8-bit binary-weighted current DAC	58

Figure 4-11: Histogram of a 1000-times Monto-Carlo simulation result ($I_{REF0} = 160\text{nA}$)	59
Figure 4-12: Schematic of the integration amplifier	60
Figure 4-13: Simulation result of the integration amplifier	61
Figure 4-14: Timing diagram of one comparison cycle.....	62
Figure 4-15: Schematic of the PWM module	63
Figure 4-16: Timing diagram of input current quantization (a) in normal case (b) with self-correction	65
Figure 4-17: Schematic of the motion detector.....	66
Figure 4-18: Schematic of the continuous-time comparator.....	68
Figure 4-19: Layout view of the proposed multi-mode sensor.....	69
Figure 4-20: Block diagram of the testing platform	72
Figure 4-21: Hardware setup for chip testing	73
Figure 4-22: Timing diagram of the control signals in CIS mode	74
Figure 4-23: Timing diagram of the control signals in ALS mode.....	75
Figure 4-24: Testing platform for ALS function test.....	77
Figure 4-25: Testing result of detection current versus light intensity	79
Figure 4-26: Sample images taken by the prototype chip.....	80
Figure 5-1: Block diagram of calibration scheme I	83
Figure 5-2: Block diagram of calibration scheme II.....	84

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List of Tables

Table 4-1: Characteristics of the CDS amplifier.....	52
Table 4-2: Characteristics of the integration amplifier	61
Table 4-3: Pin list of the sensor chip	71
Table 4-4: Control signals description in CIS mode.....	74
Table 4-5: Control signals description in ALS mode	75
Table 4-6: Testing result of power consumption	78
Table 4-7: Characteristics summary of the prototype sensor.....	79

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List of Abbreviations

ADC	Analog-to-Digital Converter
ALS	Ambient Light Sensing
CCD	Charge-Couple Device
CDS	Correlated Double Sampling
CG	Conversion Gain
CIS	CMOS Image Sensing
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DR	Dynamic Range
FOV	Full Field of View
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
FWC	Full Well Capacity
LCD	Liquid Crystal Display
PFM	Pulse-frequency Modulation
PLL	Phase Locking Loop
PPS	Passive Pixel Sensor
PWM	Pulse-width Modulation
3T APS	3-Transistor Active Pixel Sensor
4T APS	4-Transistor Active Pixel Sensor

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Chapter 1

Introduction

1.1 Background

There has been significant advancement in the area of portable devices, of which mobile phone is undoubtedly the most remarkable one. From black-and-white screen with keyboard to high resolution touchable color screen, mobile phones have become a part of our life. Manufacturers have been paying a lot of efforts to improve the user experience. One aspect is that the light-emitting part can be automatically adjusted against the ambient illumination to suit the users' eyes. On the other hand, the liquid crystal display (LCD) screen and its associated backlighting are the most power hungry parts in the portable devices. A critical design consideration is to save the power consumption in order to extend the battery life.

Currently, an ambient light sensor is employed to detect the ambient illumination condition and generate some control signals. With its output, the central controller can increase or decrease the display brightness depending on the environment illumination condition. This function has become a norm in the latest mobile devices. For ambient light sensors, technology choices available include photoelectric cells, photodiodes, phototransistors, and photo ICs. There are a number of manufacturers, such as Avago, Osram, Vishay, etc. The cost of an ambient light sensor is among the range of 0.5 ~ 1 USD.

Meanwhile, a large number of smart phones are equipped with a front facing camera. It is important for applications such as video call, video conference or self-imaging. As a result, these phones carry an ambient light sensor and a front facing camera at the same time as shown in Figure 1-1.

Figure 1-1 Front facing camera and ambient light sensor on the mobile phone

To further reduce the fabrication cost of the mobile devices, manufacturers hope to merge the functionality of the ambient light sensor into the front facing camera. Currently, the front facing camera is not suitable for this application, mainly due to the following reasons:

- 1) A camera always comes with a lens. In order to sense the ambient light, i.e. average light in the full field of view (FOV), the CMOS image sensor needs to take a full picture and then perform light averaging. Continuously shooting pictures will consume a lot of power and reduce the battery life.
- 2) Adding more functionalities into the image sensor usually needs additional transistors into the pixel, leading to a larger pixel footprint, and hence increases the cost of the front facing camera.

In this study, a multi-mode sensor is proposed which combines the two types of sensors into one microchip, without increasing power consumption and pixel size. Both of them are the key factors for today's mobile market. Furthermore, the proposed sensor can be applied to any exiting CMOS image sensor architecture.

1.2 Motivation and Objective

Figure 1-2 shows the general diagram of a conventional CMOS image sensor. It mainly consists of a pixel array, row controller, column controller & readout circuits. The pixel array is made up by a large number of 2-dimensional placed pixels, i.e., m rows and n columns. Each pixel consists of two parts: photo detector (PD) and in-pixel supporting circuit. There are a number of popular pixel structures, such as Passive Pixel Sensor (PPS), 3-Transistor Active Pixel Sensor (3T APS) and 4-Transistor Active Pixel Sensor (4T APS). The pixel array is powered by a global power bus. The row control circuit will generate row-level signals to control the operations of different pixel rows. The column control and readout circuits will control and select the specified columns, readout the photo signals and execute the further data conversion or image processing. Usually, the power supply is designed as an array-level bus; while the row control signals and column data are planned in row-wise and column-wise, respectively.

In this study, a multi-mode sensor is proposed which merge the functionality of an ambient light sensor into a CMOS image sensor. The proposed multi-mode sensor can be applied to any existing pixel architecture. Compared with the conventional structure of a CMOS image sensor, no additional transistors are added into the pixel. Instead, only an extra metal bus is inserted. The metal bus is shared by all the photo detectors, through a configurable dual-mode resistive path. The metal bus has two purposes: in CMOS image sensing (CIS) mode, it delivers power to pixels; in ambient light sensing (ALS) mode, it connects all the photo detectors in the array and carries ambient light signals.

Figure 1-2 General diagram of a conventional CMOS image sensor

Figure 1-3 shows the resistive coupling method to merge the two types of sensors. Symbol $\overline{\text{w}}\text{w}$ stands for the resistive path, which is used to link the photo detector and the extra metal bus by re-configuring the existing in-pixel circuit. In CIS mode, depending on the original pixel structure, the resistive path is used to reset the photo detector voltage or transfer the photo signals, and the extra metal bus is used to provide the power supply, denoted as “Power 2” in Figure 1-3. In ALS mode, the transistors in the resistive path are re-configured to constantly ON (i.e., conductive) mode, thus the path will act as a low impedance link, through which all the photo detectors are directly attached to the extra metal bus. Photo signal generated in all the

Figure 1-3 Resistive coupling method to merge the two types of sensors

PDs will be readout and processed as the ambient light intensity. As a result, switch SW_2 and switch SW_1 work alternatively. SW_1 is ON and SW_2 is OFF in CIS mode, while SW_2 is ON and SW_1 is OFF in ALS mode.

The proposed sensor has a number of advantages:

- 1) The proposed sensor can operate in dual modes: CIS mode and ALS mode. In ALS mode, the circuits for CIS readout are in standby mode, thus do not consume

power. Only the ALS circuit is working, which consumes very little power. In other words, the CMOS image sensor is re-configured into an ambient light sensor, with distributed light detectors. While in CIS mode, the ALS circuit shuts down, and the sensor falls back to a normal camera.

- 2) The proposed sensor does not need to add more transistors into the pixel, but only an extra metal bus is inserted. The metal bus is shared by all the photo detectors, through a configurable dual-mode resistive or capacitive data path. The metal bus has dual purposes: in CIS mode, it delivers power to pixels; while in ALS, it connects all the photo detectors in the array and carries ambient light signal.

In summary, the proposed multi-mode sensor combines the functionalities of an ambient light sensor and a CMOS image sensor into one microchip, without increasing power consumption and pixel size. Both of them are the key factors for today's mobile market.

1.3 Thesis Organization

The thesis consists of six chapters. Chapter 1 introduces the background of the design idea and the motivation on how to achieve it. Chapter 2 describes the fundamentals of the CMOS image sensor, including the architecture, the operating principle and the basic information of each circuit module. Chapter 3 illustrates some related projects and studies their advantages and disadvantages in order to do the comparison with the proposed project. Chapter 4 presents the whole design flow of the proposed sensor chip, including circuit modules design, operating principles as well as the testing results. Chapter 5 describes the design improvement which applies two calibration schemes in the proposed ADC design. The last chapter shows the conclusion of the project and the recommendations about the future work.

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Chapter 2

Fundamentals of CMOS Image Sensor

An image sensor is a device that converts optical signals into electronic signals [1-3]. When the first digital camera came up in the nineties, the main technology used for the image sensor was the Charge-Couple Device (CCD) technology. In order to be able to record color information, digital image sensors were typically equipped with a Bayer pattern color filter. With the advance of technology, another type of sensor started to emerge which was the Complementary Metal-Oxide Semiconductor (CMOS) image sensor. Nowadays, it has replaced the CCD image sensor in most types of digital cameras. The main difference between the two types of sensor is that, the charges in a CMOS image sensor are not passed along a column of pixels, but rather each pixel has its own readout unit. In other words, unlike a CCD image sensor outputs an analog signal which has to be converted into digital before the camera's image processor can interpret it, a CMOS image sensor outputs a digital signal directly. Compared with CCD image sensor, the main advantages of CMOS image sensors include low power consumption, high integration capability, high speed readout and so on.

2.1 Overall Architecture and Operating Principle

The architecture of a CMOS image sensor is illustrated in Figure 2-1. It mainly consists of five circuit modules including pixel array, correlated double sampling (CDS) circuit, analog-to-digital convertor (ADC), row & column selector and timing control logic. Pixel array is the core component of an image sensor since it is the image capture region. It is made up by a large number of two-dimensional placed

pixels. Each pixel is used to register the amount of light falling on it, and the received amount of light is converted into a corresponding number of electrons. The stronger the incident light, the more electrons are generated. After that, the received amount of electrons are converted into a voltage level and then quantized into a digital code by an ADC. CDS circuit is used to eliminate the noise generated during the above process. Row & column selector is used to control and select the specified pixel. Timing control logic is worked as a CPU which is used to provide the working sequence between each circuit modules.

Figure 2-1 Architecture of a CMOS image sensor

The operating principle of the CMOS image sensor can be summarized as follows:

- 1) When a picture is taken, the incident light intensity is recorded by the pixel array.

The generated photons in each pixel are converted into the electrons through the

photodetector and the number of induced electrons is proportional to the exposure time. The longer the exposure time, the more electrons are accumulated in the photodetector.

- 2) When the exposure is finished, the accumulated electrons are converted into a voltage level by the in-pixel circuit. In this case, each pixel has its own pixel signal.
- 3) The row selector scans the pixel array row by row. Therefore, the pixel signals in each row are sent to the column-parallel CDS circuit for noise cancellation.
- 4) The cleared pixel signals in each row are sent to the ADCs for further digital quantization.
- 5) The column selector scans the pixel array column by column. Therefore, the digital signals in each row are readout for further signal processing.
- 6) When last row finishes readout, one image frame is generated. The above process can be repeated for the next image frame generation.

2.2 Photodetection

Based on the operating principle of the CMOS image sensor, the photon generation procedure is the core step for taking an image since it carries the optical information. The photon is the fundamental particle of visible light. Photons travel through empty space at a speed of light. The shorter the wavelength of an electromagnetic disturbance, the more energy each photon contains [4]. In fact, the energy of the photon E can be expressed as equation Eq.2.1:

$$E = \frac{hc}{\lambda} \quad (Eq. 2.1)$$

where h is Planck's constant, c is speed of light, and λ is electromagnetic wavelength.

Figure 2-2 Photo-generated carriers in a semiconductor [2]

Every solid has its own characteristic energy-band structure. The term “bandgap energy (E_g)” refers to the energy difference between the top of the valance band and the bottom of the conduction band. A semiconductor material has a small but non-zero bandgap energy. In this case, an electron requires a specific minimum amount of energy to jump from a valence band to a conduction band. In order to achieve it, an electron can absorb a photon to gain enough energy.

When a beam of light is illuminated on the semiconductor, some of it is reflected and the rest is absorbed. The absorbed light can generate electron-hole pairs, which are also called photo-generated carrier, inside the semiconductor as shown in Figure 2-2. The absorption coefficient α determines how far the light particular can penetrate before it is absorbed. It can be expressed as equation Eq.2.2:

$$\alpha(\lambda) = \frac{1}{\Delta z} \frac{\Delta P}{P} \quad (Eq. 2.2)$$

where Δz is light travel distance and $\Delta P/P$ is ratio of decrease of light power.

When the absorbed photon energy is larger than the bandgap energy, the electron-hole pairs are created. The electrons are moved to the conduction band and the holes

are moved to the valence band. Such movement of the electron-hole pairs can be regarded as the induced photocurrent generation, which will be detailed in the upcoming paragraphs.

Photodetectors are used as an optical receiver which convert light into electricity. According to the different applications, there are many types of photodetectors including p-n junction photodiodes (PDs), photogates (PGs), phototransistors (PTrs), etc. Among them, PDs are the most commonly used in today's sensor market, since p-n junction can prevent the loss of electrons.

A p-n junction is an interface between two types of semiconductor material, p-type and n-type, inside a single crystal of semiconductor. Figure 2.3 shows the diagram of a p-n junction diode without light illumination. The p-type region contains an excess of holes, while the n-type region contains an excess of electrons. The junction in between is known as the depletion region, which is used to deplete the charge carriers in it. When no external voltage is applied, an equilibrium condition is reached in which a potential difference is formed across the junction. The potential difference is known as the built-in potential V_0 in Figure 2-3. Since the built-in potential exists, the electrons in n-type region cannot diffuse into p-type region, while the holes in p-type region cannot diffuse into n-type region. In this case, no charge carriers moves in the depletion region, so that no current flows in the photodiode.

When a photon of sufficient energy strikes the photodiode as shown in Figure 2-4, an electron-hole pair is created as discussed above. If the absorption occurs in the depletion region, the electron-hole pair is separated by the built-in electric field. Therefore, the hole moves toward p-type region, while the electron moves toward n-type region. In this case, the photocurrent is produced. In other words, the photodiode is designed to operate in the reverse bias condition.

Figure 2-3 P-N junction photodiode without light illumination [27]

Figure 2-4 P-N junction photodiode with light illumination [27]

2.3 Basic Pixel Architectures

The basic pixel architecture consists of a photodetector and different numbers of transistors. Historically, Passive Pixel Sensors (PPS) were the first image sensor devices used in the 1960s, where the photodetector is simply connected with a switch transistor. After that, Active Pixel Sensors (APS) were developed to improve image quality. A pixel which consists a photodiode with three transistors is known as 3-Transistor Active Pixel Sensor (3T APS). A pixel which consists a photodiode with four transistors is known as 4-Transistor Active Pixel Sensor (4T APS) [2]. Nowadays, both of them are widely used in image sensing applications.

2.3.1 PPS

The structure of a PPS is quite simple as shown in Figure 2-5. It is composed of a photodiode and a switch transistor M_{SEL} . C_{PD} is p-n junction capacitance of the photodiode. The photodiode converts photons into the corresponding electrical charges, which are then carried off the sensor and amplified. PPS are quite small and the main problem of the sensor is the noise that appears as a background pattern in the image. In order to cancel out the noise, the sensor often needs additional processing steps after receiving the signals.

Figure 2-5 Pixel architecture of PPS

2.3.2 3T APS

The structure of a 3T APS is illustrated in Figure 2-6. It is composed of a photodiode, a reset transistor M_{RST} , a source follower transistor M_{SF} and a row select transistor M_{SEL} . C_{PD} is p-n junction capacitance of the photodiode. M_{RST} is used to reset the voltage level of the photodiode. M_{SF} is used as a voltage buffer, which isolates the photo-generation region from the column output bus. M_{SEL} is used as a switch since each column output bus is shared for all rows. RST and RSEL are the control signals which are driven by the row selector. Figure 2-7 shows the timing diagram of the control signals.

Figure 2-6 Pixel architecture of 3T APS

Figure 2-7 Timing diagram of the control signals in 3T APS

The operation of a 3T APS can be summarized as follows:

- 1) M_{RST} is turned on, the voltage level of the PD is reset to $V_{DD} - V_{th}$, where V_{th} is the threshold voltage of M_{RST} .
- 2) M_{RST} is turned off, the PD is electrically floated. When light is incident, the photo-generated carriers accumulate in C_{PD} . The voltage level of the photodiode decreases based on the light intensity.
- 3) When exposure is finished, M_{SEL} is turned on. The output signal is read out in the column output bus.
- 4) When the read-out process is finished, M_{SEL} is turned off and the above process can be repeated for the next image signal generation.

Compared with PPS, 3T APS can be used to improve image quality. However, it still has some issues including:

- 1) Poor thermal noise suppression.
- 2) Photodiode design constraint.

In order to resolve the issues discussed above, 4T APS is developed.

2.3.3 4T APS

The structure of a 4T APS is illustrated in Figure 2-8. Compared with 3T APS, a transfer gate transistor M_{TG} and a floating diffusion FD are added. M_{TG} is used to separate the photo-detection region and photo-conversion region. Therefore, the photo-generated carriers need to be transferred from the photodiode to the floating diffusion, where the carriers are converted into voltage. RST, TG and RSEL are the control signals which are driven by the row selector. Figure 2-9 shows the timing diagram of the control signals.

Figure 2-8 Pixel architecture of 4T APS

Figure 2-9 Timing diagram of the control signals in 4T APS

The operation of a 4T-APS can be summarized as follows:

- 1) M_{RST} and M_{TG} are turned on. The voltage level of both the PD and the FD are reset to $V_{DD}-V_{th}$, where V_{th} is the threshold voltage of M_{RST} .
- 2) M_{RST} keeps turning on, M_{TG} is turned off. Since the photo-detection region and the photo-conversion region are separated, the photo-generated carriers accumulate in the PD.
- 3) M_{SEL} is turned on, the reset voltage value on FD is read out in the column output bus for correlated double sampling (CDS).
- 4) When exposure is finished, M_{RST} is turned off first, then M_{TG} is turned on. The signal charge accumulated in the PD is transferred to the FD. Since M_{SEL} keeps turning on, the voltage value on FD is read out in the column output bus.
- 5) When the read-out process is finished, both M_{TG} and M_{SEL} are turned off and the above process can be repeated for the next image signal generation.

Compare with PPS and 3T APS, 4T APS has better performance for low noise applications. However, it still has some issues including:

- 1) Low fill factor.
- 2) Accumulated signal charge lagging.
- 3) Complicated fabrication process.

2.4 Correlated Double Sampling

Correlated double sampling (CDS) is a method to measure electrical signals which can remove any undesired offsets. It is often used to measure the sensor outputs. Two results should be sampled with one in a known condition and the other one in an unknown condition. The value measured from the known condition is then subtracted from the one from the unknown condition to generate the final value, which has a known relationship with the physical quantity being measured. In this process, the undesired offsets has been cancelled during the subtraction.

In CMOS image sensor, CDS circuit is used to eliminate different kinds of noise, including thermal noise and fixed pattern noise (FPN). In order to achieve it, CDS circuit samples both reset value and signal value, and subtracts them to cancel the noise effect. The basic CDS circuit is shown in Figure 2-10. It is composed of a differential amplifier, two capacitors (C_1 and C_2), and two switches (SW_1 and SW_2).

Figure 2-10 Basic CDS circuit

The operation of CDS circuit can be summarized in two steps:

- 1) Both SW_1 and SW_2 are turned on. The reset value ($V_{RST} + V_N$) is sampled on capacitor C_1 , where V_N is the total noise value. The charge stored in each capacitor can be expressed as equations Eq.2.3 and Eq.2.4:

$$Q_1 = C_1 \times [V_{ref} - (V_{RST} + V_N)] \quad (Eq. 2.3)$$

$$Q_2 = 0 \quad (Eq. 2.4)$$

- 2) SW_1 keeps turning on, SW_2 is turned off. The signal value ($V_{SIG} + V_N$) is sampled on capacitor C_1 , then transferred to capacitor C_2 . The charge stored in each capacitor can be expressed as equation Eq.2.5 and Eq.2.6:

$$Q_1 = C_1 \times [V_{ref} - (V_{SIG} + V_N)] \quad (Eq. 2.5)$$

$$Q_2 = C_2 \times (V_{ref} - V_{out}) \quad (Eq. 2.6)$$

Since charge is conserved during the two steps, the final output signal can be expressed as equation Eq.2.7:

$$V_{out} = V_{ref} + \frac{C_1}{C_2} (V_{RST} - V_{SIG}) \quad (Eq. 2.7)$$

where the noise is cancelled in the subtraction term “ $V_{RST} - V_{SIG}$ ”.

2.5 Analog-to-Digital Convertor

Analog-to-Digital Convertor (ADC) is a device that converts a continuous physical quantity (usually voltage) to a digital number which is proportional to its amplitude. In CMOS image sensor, ADC is used to quantize the analog voltage value into digital code. According to different applications, three methods can be used to implement an ADC in a sensor. A serial ADC, as shown in Figure 2-11, converts the analog signals in the pixel array one by one. In other words, when the last pixel in the first row finishes quantization, the second row starts at once until the whole pixel array is complete. Therefore, high speed is the critical factor for serial ADC implementation and the pipeline ADC is a good choice to achieve it. Column parallel ADCs, as shown in Figure 2-12, convert the analog signals in the pixel array row by row. Pixels in the same row do the quantization at the same time. In this case, the conversion time for the whole pixel array depends on the number of rows. Compared with serial ADC implementation, it saves time with larger area. Successive Approximation (SAR) ADCs are the most commonly used for column parallel ADC implementation. In-pixel ADCs, as shown in Figure 2-13, convert the analog signals in the pixel array at the same time. Each pixel consumes large area since the ADC is implemented into the pixel. Although it is the fastest structure, it is difficult to implement for a large resolution.

Figure 2-11 Serial ADC implementation in CMOS image sensor

Figure 2-12 Column parallel ADC implementation in CMOS image sensor

Figure 2-13 In-pixel ADC implementation in CMOS image sensor

2.6 Specifications of CMOS Image Sensor

2.6.1 Conversion Gain

Conversion gain (CG) is defined as the amount of voltage variation when one photo-generated carrier is accumulated at the conversion node. Typically, the conversion node is known as the p-n junction capacitance of the photodiode. Therefore, it can be expressed as equation Eq.2.8:

$$CG = \frac{q}{C_{PD}} \quad (Eq. 2.8)$$

In order to achieve larger voltage swing, CG should be larger. In this case, the capacitance C_{PD} should be smaller.

2.6.2 Full Well Capacity

Full well capacity (FWC) is defined as the maximum amount of charge that can be held by a pixel. It can be expressed as equation E.q.2.9:

$$FWC = \frac{C_{node} V_{swing}}{q} \quad (Eq. 2.9)$$

where V_{swing} is the maximum voltage swing of the photodiode and C_{node} is the capacitance of charge storage node.

In order to achieve larger FWC, C_{node} should be larger. In 3T APS, C_{node} can be regarded as C_{PD} . In this case, FWC is inversely proportional to CG. To resolve the issue, 4T APS can be applied since the photo-detection region and photo-conversion region are separated. C_{node} in 4T APS can be regarded as the capacitance of the FD, so that both CG and FWC can be designed larger.

2.6.3 Sensitivity

Sensitivity can also be known as photon efficiency, which is the ratio of the photons striking the area of a pixel that can be converted into the detectable electron-hole pairs in the photodiode. It is defined as the ratio of the output signal to an incident illumination level in a second. In general, high CG leads to high sensitivity. The sensitivity mainly depends on the process. In order to increase the sensitivity, process optimization should be applied.

2.6.4 Dark Current

Dark current is defined as the number of charge generated during an exposure period without light illumination. It is an important source of both fixed pattern noise and thermal noise in a pixel. In general, there are three dominant mechanisms that give rise to the dark current as shown in Figure 2-14, including:

- 1) Surface generation current (J_{SG}).
- 2) Generation-recombination current (J_{g-r}) due to thermal generation of charge.
- 3) Diffusion current (J_{DIFF}).

They can be expressed in the following equations:

$$J_{SG} = \frac{1}{2} q n_i s_0 \quad (Eq. 2.10)$$

$$J_{g-r} = q \frac{n_i}{\tau_g} W \quad (Eq. 2.11)$$

$$J_{DIFF} = q \sqrt{\frac{D_n}{\tau_n} \frac{n_i^2}{N_A}} \quad (Eq. 2.12)$$

where n_i is the intrinsic carrier concentration, s_0 is the surface recombination rate, n_i/τ_g is the charge generation rate, W is the depletion width, D_n is the diffusivity of the electrons in silicon and N_A is the p-type doping concentration.

The total dark current is the summation of them as expressed in equation Eq.2.13:

$$J_{DARK} = J_{SG} + J_{g-r} + J_{DIFF} \quad (Eq. 2.13)$$

In order to minimize the dark current, three approaches can be taken including:

- 1) Minimize the depleted area.
- 2) Minimize the width of the space charge layer (SCL).
- 3) Maximize the carrier lifetime or minimize the surface recombination rate.

The third approach is typically a characteristic of the process and cannot be modified. The depleted area is depend on the implant well design and distribution, which requires a tradeoff with capacity. The width of the SCL can be reduced by increasing the doping concentration.

Figure 2-14 Three dominant sources of dark current (online resource)

2.6.5 Dynamic Range

Dynamic range (DR) is defined as the ratio between the maximum output signal level to the noise floor at minimum signal amplification, where the noise floor can be regarded as the root mean square (RMS) noise level without light illumination. The noise floor of an image sensor mainly consists of sensor readout noise, signal processing noise and dark current shot noise. DR represents the sensor's ability to display the brightest and darkest portions of the image. It can be expressed as equation Eq.2.14:

$$DR = 20\log \frac{V_{max}}{V_{dark,rms}} \quad (Eq. 2.14)$$

The unit of DR is dB (decibel). The maximum output signal level is proportional to FWC, which is described in Section 2.6.2. In order to achieve larger DR, the FWC of the photodiode should be larger and the noise floor should be smaller.

2.6.6 Fixed Pattern Noise

Fixed pattern noise (FPN) is defined as the spatially fixed variation of the pixels' output under the same illumination conditions. In a two-dimensional device, the FPN can be divided into two groups. One is pixel level FPN, and the other one is column level FPN. The pixel level FPN is mainly generated due to the mismatch of transistors in the pixel; while the column level FPN is mainly caused by the offset between the column readout circuits.

Although FPN is an undesired parameter, it is usually easy to be removed since it is repeatable. Usually, the sensor needs to know the pattern first, and then subtracts this noise away to reveal the true image. There are many on-chip techniques to suppress FPN. Among them, CDS is the most commonly used as described in Section 2.4.

2.6.7 Fill Factor

Fill factor (FF) is defined as the ratio between the photodiode area and the total pixel area. It can be expressed as equation Eq.2.15:

$$FF = \frac{A_{PD}}{A_{PIXEL}} \% \quad (Eq. 2.15)$$

Usually, higher FF is preferred since more incident light can be detected in a certain area. However, as the number of transistors in the pixel increased, FF becomes smaller. In order to improve it, micro lenses can be equipped by converging light from the whole pixel area into the photodiode.

2.6.8 Resolution

Resolution is defined as the number of effective pixels that an image sensor contains. It represents the capability of the sensor to measure the smallest object clearly with distinct boundaries. With a given area of the pixel array, the smaller the size of the pixel, the higher the resolution will be. The resolution is correlated to the amount of information within the image.

The resolution of an image sensor can be expressed as $M \times N$, where M is known as the number of pixel columns and N is known as the number of pixel rows. On the other hand, it can also be expressed as the total number of pixels in the image, typically given as a number of megapixels. For example, a pixel array with 2048 pixels in each row and 1024 pixels in each column. The resolution can be expressed as 2048×1024 , or 2.1 megapixels.

2.6.9 Power Consumption

Power consumption is simply defined as the total power cost of the image sensor. It is an important parameter for any electronic devices. To achieve low power consumption is the goal for the whole electronic industry. In an image sensor, power consumption can be divided into two parts, including power consumption for both analog and digital circuits. Power consumption for analog circuits is constant, while power consumption for digital circuits is flexible due to the switching noise.

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Chapter 3

Smart Applications in CMOS Image Sensor

A smart image sensor is known as a typical image sensor with some additional smart functions on it. The smart functions can be different operational modes, such as analog, digital or pulse processing modes. If these modes are implemented on a single chip, a smart image sensor is generated. The major advantages of such smart image sensors include high level of integration, high performance, low cost and so on. Nowadays, the common smart image sensors include accelerometer, optical sensor, infrared sensor and so on. In this chapter, several smart applications in CMOS image sensor are presented.

3.1 Pulse Modulation

As described in Chapter 2, in a typical CMOS image sensor, ADC is used as the signal output stage which quantizes the analog voltage value into digital code. Besides that, pulse modulation (PM) imaging technology is another method to do the analog signal processing. Instead, it converts the light intensity into timing of pulse [5]. Compared with typical CMOS image sensors, PM image sensors have higher dynamic range (DR) and better signal-to-noise ratio (SNR), but more complex circuit structure in pixel circuitry.

The basic operating principle of PM imaging technology is illustrated in Figure 3-1. The basic PM circuit consists of a reset transistor and a comparator. At beginning, a small pulse is applied to the reset transistor, so that the photodiode can be precharged to a defined voltage level ($V_{int,0}$). When light is illuminated to the photodiode, the

induced photocurrent starts to discharge the photodiode. The comparator is used to continuously compare the integration voltage level (V_{int}) and a fixed reference voltage level (V_{ref}). The integration time (t_{int}) will be recorded if the threshold is reached. The incident light intensity is inversely proportional to the integration time. Since the comparator has an offset voltage, a comparator with high accuracy is needed.

Figure 3-1 Operating Principle of PM imaging technology

PM imaging technology can be classified into two categories, one is pulse-width modulation (PWM) and the other one is pulse-frequency modulation (PFM). For PWM [Figure 3-2(a)], the incident light intensity is inversely proportional to the integration time. In other words, longer integration time means darker pixels and vice-versa. The integration time can be expressed as equation Eq.3.1:

$$t_{int} = \frac{C_{PD}(V_{int,0} - V_{ref})}{I_{ph} + I_d} \quad (Eq.3.1)$$

Where I_{ph} is the photo-generated current and I_d is the dark current.

For PFM [Figure 3-2(b)], a feedback is added between the output of the comparator and the reset transistor [6]. When the threshold is reached, a pulse is recorded. Meanwhile, the voltage level of the photodiode is reset by the output of the comparator. Such integration cycles are repeated within a certain amount of time. The

incident light intensity is proportional to the number of pulses generated. In other words, larger number of pulse means brighter pixels and vice-versa. The number of pulse (N_{pulse}) within a certain integration time (T_{int}) can be expressed as equation Eq.3.2:

$$N_{\text{pulse}} = \frac{T_{\text{int}}(I_{ph} + I_d)}{C_{PD}(V_{\text{int},0} - V_{\text{ref}})} \quad (\text{Eq. 3.2})$$

(a)

(b)

Figure 3-2 PM imaging categories (a) PWM (b) PFM

There are many advantages for PM image sensors. The most important one is that it is insensitive to supply voltage scaling. For a traditional APS pixel, the output voltage level is limited by V_{th} drops across both the reset transistor and the source follower transistor. In this case, low V_{th} transistors are always applied to compensate it. However, it will lead to increase the transistor leakage. In other words, to ensure adequate SNR, sufficient supply voltage must be provided (usually 3.3V). Since PM image sensors convert the image information into time domain instead of voltage domain, this problem can be solved. Furthermore, for recent CMOS process, shallow junction and high doping are used to increase the optical transmission ability. It will lead to higher dark current which limit dynamic range (DR) and signal-to-noise ratio (SNR). Normally, DR for a CMOS image sensor is around 60-70dB and DR for nature light is around 140dB. In order to enhance DR, PM imaging technology is an alternative method. Besides that, a PM image sensor can achieve low power consumption, low KTC noise, high frame-rate, etc.

The major limitation for PM image sensors is the complex pixel structure due to additional modules such as counter, memory, etc. it will lead to larger pixel size and higher fixed-pattern noise (FPN). Figure 3-3 shows the block diagram of a frame-based PWM pixel. Each pixel is composed of a SR latch driven by an amplifier and an 8-bit memory. The proposed image sensor can achieve high linearity and a DR of 85dB. However, since a memory module is integrated inside a pixel, the pitch is around 45um and the fill factor is quite small.

Figure 3-3 Sample architecture of a PWM pixel [7]

3.2 Ambient Light Sensor

An ambient light sensor is a device that is used to adjust the brightness of the screen automatically according to the ambient light conditions [8-9]. Nowadays, it is equipped on the most portable electronic devices in order to extend the battery life. A simple ambient light sensor consists of a photodetector and conversion circuit. The conversion circuit can be ADC or PWM/PFM, which are already described in the previous section.

Dark current is a major factor which may influence the performance of an ambient light sensor. Typically, it will increase with a rise of temperature, which may cause the failure of the sensor's functionalities. In this case, it is important to reduce the dark current. In addition, a wide dynamic range should be achieved so that the sensor can detect the illuminance change within a large range. The block diagram of a sampled ambient light sensor is illustrated in Figure 3-4. PFM is used to measure the ambient light intensity so that it can achieve a wide dynamic range. A dark current

compensation circuit is added to suppress the dark current effect. Meanwhile, adaptive resolution adjustment circuit is used to reduce the power consumption.

Figure 3-4 Block diagram of a sampled ambient light sensor [8]

The architecture of the proposed PFM circuitry is illustrated in Figure 3-5. Two photodiodes are applied in the circuit. PD_{LIGHT} is used to detect the light intensity (include dark current) and the induced photocurrent I_2 is generated. PD_{DARK} , which is covered by metals, is used to generate dark current I_1 . After mirroring I_1 into I_2 , the total induced current ($I_2 - I_1$) will be integrated at the node V_{store} . Therefore, dark current effect can be eliminated.

The proposed sensor is supposed to measure the light intensity up to 10Klux. For a typical measurement, a 14-bit system needs to be used with one count corresponds to one lux. In this sensor, a 10-bit system (7 fine bits and 3 coarse bits) is proposed. The operational range is divided into eight groups (3-bit counter). Each group has the same number of fine steps (7-bit counter), but different resolution per step as shown in Figure 3-5. For example, for group 000, one count corresponds to one lux; while for group 111, one count corresponds to 128 lux. When the integration is finished, the sensor can monitor the resolution based on the current 7-bit counter. If it is full, the 3-bit counter moves up to a higher group in order to extend the lux measurement

range. If it is less than half, the 3-bit counter drops to a lower group in order to measure more accurately. Therefore, lower power consumption can be achieved by using 10-bit system instead of 14-bit system.

Figure 3-5 Architecture of the sampled PFM circuitry [8]

Figure 3-6 shows the test result of temperature characteristics without illumination. Compared the proposed sensor (solid line) and the sensor without compensation circuit (dash line), the proposed sensor has negligible effect on the temperature, while the dark current of the sensor without compensation circuit increases drastically as temperature increases. Meanwhile, the output of the proposed sensor has good linearity up to 10klux measurement.

Figure 3-6 Test result of temperature characteristics without illumination [8]

3.3 Multi-mode Image Sensor

In this study, the objective is to design a multi-mode sensor which merge the functionality of an ambient light sensor into a CMOS image sensor. In this section, two relevant multi-mode image sensors will be presented.

The first relevant multi-mode sensor design is published in 2014 [10]. In this paper, a switchable dual-mode image sensor is proposed. The two operational modes include image mode and communication mode. In image mode, the sensor is worked as a normal camera, where the induced photocurrent in each pixel is integrated and readout as the digital outputs. In communication mode, the induced photocurrent in each column is summed together, then converted to voltage signal by a trans-impedance amplifier (TIA). The proposed dual-mode operation is illustrated in Figure 3-7.

Figure 3-7 Sensor operational modes (a) image mode (b) communication mode [10]

The proposed pixel architecture is illustrated in Figure 3-8. The structure is quite similar to that of the traditional 3T APS, with an extra mode select transistor M_{MS} . In image mode, as shown in Figure 3-8(b), M_{MS} is turned off and the pixel circuit works as a traditional 3T APS. In communication mode, as shown in Figure 3-8(c), M_{MS} is turned on and the other transistors are turned off. The induced photocurrent is directly transferred to the column bus, and the photocurrent in each column is summed together in order to increase the amount of signal. To further increase the sensitivity, additional column switches can be inserted to select the number of detection columns under illumination.

Figure 3-9 shows the equivalent circuit structure in communication mode. I_{in} is the total current summed up by the selected rows. C_{eq} is the total capacitance at the inverting node. R_f is the feedback resistor of the TIA. V_{CM} is the common mode bias voltage. The total current at node V_A can be expressed as equation Eq.3.3:

Figure 3-8 Architecture of the proposed pixel circuit (a) overview (b) image mode
(c) communication mode [10]

$$I_{in} + V_A \times sC_{eq} + \frac{V_A - V_{out}}{R_f} = 0 \quad (Eq. 3.3)$$

The transfer function can be expressed as equation Eq.3.4:

$$T(s) = \frac{V_{out}}{I_{in}} = \frac{A \times R_f}{sC_{eq}R_f + (1 + A)} \quad (Eq. 3.4)$$

where A is the open loop gain of the TIA.

The chip is implemented in TSMC 0.18 μ m 1P6M CMOS technology. In communication mode with a constant illumination, the linearity between output voltage signal and selecting number of columns (from $\times 1$ to $\times 64$) can be reached to 99.8%. The non-linearity is mainly caused by the edge effect of the sensor array. In order to improve it, dummy pixels can be added. The major disadvantage of the design is the extra transistor in pixel that may increase the pixel size, as well as the fabrication cost.

Figure 3-9 Equivalent circuit structure in communication mode [10]

The second relevant multi-mode sensor design is published in 2015 [11]. In this paper, a switchable dual-mode image sensor is proposed. The two operational modes include photo-shooting (PS) mode and always-on (AO) mode. In PS mode, the sensor is worked as a normal camera that is used to take pictures. In AO mode, the sensor is used to generate image without interruption with low power consumption. The architecture is illustrated in Figure 3-10. 4T APS structure is used in the pixel array. To minimize power consumption, full resolution with 12-bit images is applied in PS mode, while $\frac{1}{4}$ resolution with 8-bit images is applied in AO mode. Meanwhile, power supplies are separated under two modes. 3.3V analog power with 1.8V digital power is provided in PS mode, while 0.9V analog power with 0.9V digital power is provided in AO mode.

For a common 4T APS, the FD node needs to be reset at a high voltage level, which is used for charge transfer. In AO mode, since power supply is only 0.9V, a charge-sharing method is proposed to activate electronic shutter. In other words, the transistor TX is always turned on in this mode. The drawback of low power supply is the small output signal swing. In order to improve it, the source follower transistor with low- V_{th} needs to be used. In this design, the transistor with V_{th} ($\sim 0.2V$) is used. The output swing is approximately 0.5V in AO mode.

The structure of the analog signal readout circuit in this paper is a programmable-gain amplifier (PGA), followed by an ADC. In PS mode, the ADC works with a high frequency (12-bit in this case). However, it cannot be achieved at low power supply (0.9V for AO mode). To solve the problem, a reconfigurable ADC structure is illustrated in Figure 3-11. A capacitor C_3 is added in between the adjacent two columns. In PS mode, C_3 is floating. In AO mode, C_3 is connected and ADCs in two columns are reconfigured as one ADC. Therefore, it can operate with a lower frequency (8-bit in this case).

Figure 3-10 Architecture of the proposed dual-mode sensor [11]

Figure 3-11 Architecture of the proposed reconfigurable ADC [11]

The chip is implemented in 0.11μm 1P4M CMOS technology. The major advantage of the design is the low power consumption, since the power supplies for analog and digital circuits are separated in two modes. Based on the testing results, the power consumption in AO mode is 45.5μW; while the power consumption in PS mode is 2.28mW. In this case, the total power saving is almost half of the total power consumption. However, the major disadvantage of the design is the complex ADC design, which may reduce the accuracy of the detection.

After summarizing the characteristics of the above two types of multi-mode image sensors, the design of the proposed sensor in this study is presented in the next chapter.

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Chapter 4

Design of a Multi-mode Sensor which Merge an Ambient Light Sensor into a CMOS Image Sensor

According to the introduction in Chapter 1, a multi-mode sensor is proposed which merge the functionality of an ambient light sensor into a CMOS image sensor. The proposed multi-mode sensor can be applied to any existing pixel architecture. Compared with the conventional structure of a CMOS image sensor, no additional transistors are added into the pixel. Instead, only an extra metal bus is inserted. The metal bus is shared by all the photo detectors, through a configurable dual-mode resistive or capacitive data path. The metal bus has two purposes: in CMOS image sensing (CIS) mode, it delivers power to pixels; in ambient light sensing (ALS) mode, it connects all the photo detectors in the array and carries ambient light signals.

4.1 Proposed Sensor Architecture and Operating Principle

The architecture of the proposed multi-mode sensor is illustrated in Figure 4-1. Circuit in blue line can be regarded as a CMOS image sensor which is used to take pictures. Circuit in red line can be regarded as an ambient light sensor which is used to detect the ambient illumination condition. Two sensors are merged together by sharing the pixel arrays. The resolution of the proposed sensor is 64×64 , and 3T pixel architecture is used in this design. Beside the common pixel array, the sensor architecture is composed of a CDS circuit, a global buffer, a two-step current-mode ADC, a motion detector, row & column scanner and timing control logic.

Figure 4-1 Architecture of the proposed multi-mode sensor

The operational modes are controlled by two switches (SW_1 and SW_2) as shown in Figure 4-1. When SW_1 is turned on, the sensor is worked in CIS mode. During this mode, power supply is provided to the pixel array by the common metal bus. The signal value and reset value of each pixel (start from 1,1 to 1,64) are sampled by column parallel CDS circuit. The difference between them is then transferred one by one to an off-chip ADC through a global buffer. If the first row finishes readout, the second row starts at once until the whole pixel array is complete. In other words, when last row finishes readout, one image frame is generated. When SW_2 is turned on, the sensor is worked in ALS mode. During this mode, photodiode in each pixel is connected together as a large one. The total photocurrent is then sent to a 13-bit two-

step current-mode ADC for digital quantization. Motion detector is used to detect any light intensity changes. If light intensity changes in a certain range, the two-step current-mode ADC is in standby mode and do not consume power.

In order to achieve low power application, if the sensor works in one mode, the circuits in the other mode are in standby mode with no power consumption. The details of each circuit module design are described in the next section.

4.2 Circuit Modules Design

4.2.1 Pixel and Column Circuit

The architecture of the column circuit is illustrated in Figure 4-2. Each column consists of a number of pixels and a common CDS circuit. As mentioned above, 3T pixel architecture is used in this design. In each column, it has three row control signals (RST, RSEL and CDS) and one column control signal (CSEL). The number behind the signal represents which row/column it controls. For example, RST1 means the reset signal of the pixels in row one. RSEL2 means the select signal of the pixels in row two and so on.

The layout of the 3T pixel is illustrated in Figure 4-3. It consists of a diffusion layer, a poly layer, 4 metal layers and the vias in between of them that are used to connect the different layers. The pitch of the pixel is 10.4 μ m. As mentioned in Section 2.3.2,

Figure 4-2 Architecture of the column circuit

the 3T APS is composed of a photodiode and three types of transistors. The highlighted center area of the pixel is photodiode, which is the most important part in the pixel. In order to achieve large fill factor, the area of the photodiode should be maximized. Besides the photodiode, the source follower transistor M_{SF} is the most important transistor compared with the other two, since it is an analog component. In this case, the size of it should be larger to reduce the noise. Therefore, the size and the placement of all the components are determined.

Figure 4-3 Layout view of the 3T pixel

As mentioned in Section 2.4, CDS circuit is used to eliminate the noise. Typically, it is only applicable for 4T APS structure, since the transfer gate transistor M_{TG} separates the photo-detection region and photo-conversion region, the reset value and the signal value can be easily sampled separately. For 3T APS structure, CDS circuit cannot work in the traditional way. In this case, it can be achieved by sampling the signal value first, followed by sampling the reset value. The schematic of the CDS circuit is illustrated in Figure 4-4.

The operation of the CDS circuit in one row can be summarized below:

- 1) When the pixels in one row finish exposure, the control signal RSEL is turned on to select the corresponding row. The signal value ($V_{SIG} + V_N$) is sampled on

Figure 4-4 Schematic of the CDS circuit

capacitor C_1 , where V_N is the total noise value. Meanwhile, the control signal CDS is turned on. The charge stored in each capacitor can be expressed as equations Eq.4.1 and Eq.4.2:

$$Q_1 = C_1 \times [V_{ref} - (V_{SIG} + V_N)] \quad (Eq. 4.1)$$

$$Q_2 = 0 \quad (Eq. 4.2)$$

- 2) When the signal value finishes sampling, the control signal CDS is turned off. Then the control signal RST is turned on. The reset value ($V_{RST} + V_N$) is sampled on capacitor C_1 , then transferred to capacitor C_2 . The charge stored in each capacitor can be expressed as equation Eq.4.3 and Eq.4.4:

$$Q_1 = C_1 \times [V_{ref} - (V_{RST} + V_N)] \quad (Eq. 4.3)$$

$$Q_2 = C_2 \times (V_{ref} - V_{out}) \quad (Eq. 4.4)$$

Since charge is conserved during the two steps, the final output signal can be expressed as equation Eq.4.5:

$$V_{out} = V_{ref} - \frac{C_1}{C_2} (V_{RST} - V_{SIG}) \quad (Eq. 4.5)$$

- 3) When the outputs in one row are generated, the control signal CSEL is turned on. All the outputs are sent to the global buffer in sequence for further signal processing.

The term “ C_1/C_2 ” is known as the gain of the CDS amplifier. In order to increase the sensitivity of the detection range, a programmable capacitor C_2 is implemented in the CDS circuit as shown in Figure 4-2. Two options of the gain (2 or 4) can be chose according to the illumination conditions. When no light is illuminated to the photodiode, the subtraction term “ $V_{RST}-V_{SIG}$ ” should be closed to zero. In this case, V_{out} is closed to V_{ref} . When strong light is illuminated to the photodiode, the subtraction term “ $V_{RST}-V_{SIG}$ ” should be closed to V_{RST} . In this case, V_{out} is closed to zero. To get the suitable output swing, V_{ref} should be set at a high voltage level (2.4V in this design). Therefore, the amplifier with NMOS input differential pairs should be implemented. The schematic of the CDS amplifier is illustrated in Figure 4-5.

Figure 4-5 Schematic of the CDS amplifier

A typical two-stage operational amplifier consists of seven transistors. M_1 and M_2 are NMOS input differential pairs. M_3 and M_4 forms a current mirror. M_7 is the gain transistor of the second stage. M_5 and M_6 are the bias transistors for both stages. The resistor R_C and the capacitor C_C are used for compensation. The capacitor C_L is the approximate load capacitance. All the dimensions of the components are marked in the schematic.

The simulation result is shown in Figure 4-6. The green line represents the relationship between gain and bandwidth; while the red line represents the relationship between phase and bandwidth. Based on the result, the amplifier characteristics can be summarized in Table 4-1.

Figure 4-6 Simulation result of the CDS amplifier

Table 4-1 Characteristics of the CDS amplifier

Parameter	Value
Gain	80dB
Gain Bandwidth (GBW)	40MHz
Phase Margin (PM)	62deg
Current	30 μ A

In order to achieve the highest efficiency, rolling shutter is applied to complete the readout process. Rolling shutter is a method that an image is not captured at the same instant, but rather scanned vertically. In other words, each individual row is able to start its readout once the previous row is completed. The time delay between each row's readout is translated to a delay at the beginning of the exposure. The advantage of this method is that the sensor can gather photons continuously during the acquisition process, while the disadvantage is that the method is not suitable to capture a high-speed object. The timing diagram of some important control signals is illustrated in Figure 4-7.

Figure 4-7 Timing diagram of the control signals in CIS mode

4.2.2 Two-step Current-mode ADC

In ALS mode, a current-mode ADC is used to detect the total current of the pixel array, which is proportional to the ambient light illumination. Similar to the voltage-mode ADC, the potential implementations of the current-mode ADC include algorithm, cyclic, pipeline and successive-approximation register (SAR) architectures. Most of the current-mode ADC designs primarily rely on the fundamental current mirror or its varieties for current operation. Therefore, they are

expected to be more suitable for an area-efficient low-voltage design than their voltage-mode counterpart, in which more complicated switched-capacitor circuits are commonly adopted to manipulate the voltage signal. However, the accuracy of the basic current mirror is restricted by its finite output resistance as well as the mismatches of the transistors. The first limiting factor can be solved by using cascode or active current mirror. By contrast, the mismatches of the transistors could only be alleviated by enlarging the transistor size and careful layout. This issue is inevitable and becomes even worse when the current mirror works into the subthreshold region. In this case, the resolution of the current-mode ADCs is limited to only 6 to 8 bits, which makes them ineligible for lots of image sensor applications.

From another perspective, the quantization of a current could also be accomplished in the time-domain by using pulse width modulation or pulse frequency modulation method as described in Section 3.1. In comparison, the first method is easier in circuit implementation and enjoys more extensive applications. The PWM method first converts the input current into a linearly varying voltage through an integrator. Afterwards, with the help of a comparator, the time information is recorded when the voltage reaches a constant threshold. Based on the time information, the input current can be evaluated. It is an effective method to quantize current and has been widely applied in the time-based image sensors to broaden the dynamic range. However, according to the inverse correlation between the pulse width and the input current, the main drawbacks of this method are the reduced sensitivity and long integration time in resolving very large and small current.

Figure 4-8 Architecture of the proposed two-step current-mode ADC

In this study, a two-step current-mode ADC is proposed by combining the current-domain and time-domain quantization method. The coarse quantization of the input current is implemented in the current-domain with a current-mode SAR ADC. After the coarse A/D conversion, the residue current is finely quantized in the time-domain by a PWM module. Both of the two blocks in the proposed architecture coordinate well with each other. Firstly, the input current of the PWM module is compressed by the coarse SAR ADC into a small range. Therefore, it shortens the integration time and relaxes the time resolution required by the PWM module. Secondly, the PWM module can correct the possible coarse conversion errors which relaxes the design of the coarse SAR ADC. Furthermore, the integrator of the PWM module is reused in the coarse SAR ADC as a front-end part of the current comparator, which leads to a compact design. The details of the two-step current-mode ADC design are shown in the following section.

The architecture of the proposed two-step current-mode ADC is illustrated in Figure 4-8. It mainly consists of two circuit modules. Circuit in red line can be regarded as

a coarse SAR ADC. Circuit in blue line can be regarded as a PWM module. For a total 13-bit resolution, the SAR ADC quantizes the 8 coarse bits in the current-domain, while the PWM module quantizes the 5 fine bits in the time-domain. Assume the current detection range for each pixel is from 1pA to 10nA. Since the resolution of the proposed sensor is 64×64 , the total current detection range is from 4.096nA to 40.96μA. In this design, the MSB of the coarse SAR_ADC, denoted as SAR_MSB (20.48μA), is approximately equal to 128 LSBs of the coarse SAR_ADC. The LSB of the coarse SAR ADC, denoted as SAR_LSB (160nA), is approximately equal to 32 LSBs of the PWM module (5nA).

The operating principle can be summarized as follows: Firstly, the input current I_{IN} is quantized by the coarse SAR ADC, based on the classic binary trial-and-error algorithm. During this procedure, the output current of the inner 8-bit current DAC I_{ADC} would be adjusted step by step to approximate I_{IN} . After the coarse A/D conversion, I_{ADC} would be locked to a reference current which is smaller than but closest to I_{IN} . The difference between them, namely the quantization error E , should be less than 1 SAR_LSB. After that, the difference current, I_{PWM} is sent into the subsequent PWM module and finely quantized by the PWM module. As for the fine quantization, I_{PWM} is integrated through a capacitor C_{INT} . The required integration time T_{INT} is recorded when the integration voltage reaches the constant threshold V_{INT} . The current I_{PWM} can be evaluated by equation Eq.4.6. An outside counter is employed to stamp and digitalize T_{INT} , which in turn implements the fine quantization of I_{PWM} . The relationship between the several aforementioned currents is illustrated in equation Eq.4.7.

$$I_{PWM} = \frac{C_{INT} \times V_{INT}}{T_{INT}} \quad (Eq. 4.6)$$

$$I_{IN} = I_{ADC} + I_{PWM} \quad (Eq. 4.7)$$

The details of each circuit module design are described hereinafter.

4.2.2.1 Coarse SAR ADC

The architecture of the coarse SAR ADC is illustrated in Figure 4-9. It mainly consists of an 8-bit current DAC, a current comparator and SAR control logic. As mentioned before, the input current I_{IN} is firstly quantized by the coarse SAR ADC, based on the classic binary trial-and-error algorithm. In this case, the 8-bit current DAC is used to provide eight groups of reference current. The current comparator is used to compare the input current with the reference current. SAR control logic is used to provide the working sequence between each circuit modules.

Figure 4-9 Architecture of the coarse SAR ADC

Figure 4-10 Schematic of the 8-bit binary-weighted current DAC

The schematic of the 8-bit binary weighted current DAC is illustrated in Figure 4-10. The dimension (W/L) of the bias transistor, that is used to generate the unitary reference current ($I_{REF0} = 160\text{nA}$), is $5\mu\text{m}/5\mu\text{m}$. Up to the SAR_MSB, the dimension of the bias transistor increases twice a time for each adjacent units. The complementary switches (M_0, M_2, M_4, M_6) in each unit is used to eliminate the leakage current. For example, when the switch M_7 is turned off, the source terminal of the switch M_7 is pulled to V_{REF1} by complementary switch M_6 . At the same time, the drain terminal the switch M_7 is clamped to the same voltage by the subsequent PWM module. Therefore, the leakage current of the switch M_7 can be reduced. Since the reference current in each unit is quite sensitive to the final detection result, the layout of this circuitry should be well planned in order to reduce the mismatch effect. In order to test the mismatch effect of the reference current, a 1000-times Monto-Carlo simulation for the unitary reference current is shown as an example. The histogram of the Monto-Carlo simulation result is illustrated in Figure 4-11. Based on the result, the standard deviation of the unitary reference current I_{REF0} is about 4nA .

Figure 4-11 Histogram of a 1000-times Monte-Carlo simulation result ($I_{REF0} = 160\text{nA}$)

The schematic of the current comparator is illustrated in Figure 4-9. Instead of using simple cascade inverters, the current comparator in this design is composed of an integrator and a dynamic comparator (Cmp1). This combination speeds up the comparator without increasing too much area, since the front-end integrator is shared with the subsequent PWM module. The quantization range of the PWM module is determined by the resolution of the current comparator, which is 1 SAR_LSB (160nA). In this case, an integration capacitance C_{INT} with about 100fF is chosen, so that the integration voltage can be reached to 1V for a minimum input current. Such an integration voltage is large enough to overcome the offset of the amplifier and the dynamic comparator.

For the amplifier used in the integrator, the output load is mainly determined by the total capacitance of the pixel array as well as the common metal bus, which is approximately 100pF. In this case, a two-stage operational amplifier (shown in Figure 4-5) is difficult to be implemented, since a large compensation capacitor C_C is needed. In this design, a single-stage amplifier is used in order to drive a large load capacitance. The schematic of the amplifier is illustrated in Figure 4-12.

The structure of the amplifier is mainly evolved from a PMOS-input folded-cascade operational amplifier. The main difference is to change one input pairs into two. Compare with the traditional folded-cascade operational amplifier, it can double the gain with a few more transistors employed. All the dimensions of the transistors are marked in the schematic.

The simulation result is shown in Figure 4-13. The green line represents the relationship between gain and bandwidth; while the red line represents the relationship between phase and bandwidth. Based on the result, the amplifier characteristics can be summarized in Table 4-2.

Figure 4-12 Schematic of the integration amplifier

Figure 4-13 Simulation result of the integration amplifier

Table 4-2 Characteristics of the integration amplifier

Parameter	Value
Gain	80dB
Gain Bandwidth (GBW)	6.5MHz
Phase Margin (PM)	74deg
Current	1.2mA

Figure 4-14 shows the timing diagram of one comparison cycle which includes a reset phase and an integration phase. The output voltage of the integrator V_{OUT} firstly pulls back to V_{REF1} during the reset phase, and then rises or declines according to the direction of the input current I_{INT} during the integration phase. The comparator is triggered at the end of the integration phase and the outcome is determined by the comparison result between V_{OUT} and V_{REF1} . If $I_{IN} > I_{ADC}$ as shown in Figure 4-14, a digital bit “1” is set to SAR control logic and vice versa. In this design, eight comparison cycles are needed to adjust I_{ADC} in order to approximate I_{IN} . One comparison cycle is set to $1\mu s$ including $0.4\mu s$ T_{RST} and $0.6\mu s$ T_{INT} . Therefore, one coarse A/D conversion consumes $8\mu s$ in total.

Figure 4-14 Timing diagram of one comparison cycle

4.2.2.2 PWM Module

The schematic of the PWM module is illustrated in Figure 4-15. It consists of an integrator, two dynamic comparators and a 5-bit local memory. The PWM module is designed to quantize the residue current with a range from 1 LSB of the PWM module (5nA) to 1 SAR_LSB (160nA). The integrator of the coarse SAR ADC is reused in the PWM module. The integration capacitance C_{INT} is about 100fF. Typically, only one comparator (Cmp2) is used to do the voltage comparison. In this design, one more comparator (Cmp3) is implemented in order to correct the possible coarse conversion errors. The details will be shown in the next section. The reference voltage of Cmp2 (V_{REF2}) is set to 0.32V larger than V_{REF1} ; while the reference voltage of Cmp3 (V_{REF3}) is set to 0.32V lower than V_{REF1} . During each current detection process, only one comparator in the PWM module is triggered. In this case, the current quantization range is increased to from -1 SAR_LSB (-160nA) to 1 SAR_LSB (160nA). The schematic of the dynamic comparator is also shown in Figure 4-15. All the dimensions of the transistors are marked in the schematic. Moreover, a 5-bit local

memory is implemented to record the number of the global counter when either of the comparator is triggered. A Gray counter, instead of a binary counter, is used to eliminate the errors that might be induced during data transition since only one bit is changed for each state switching.

In order to illustrate the whole process on how the two-step current-mode ADC works, an input current $I_{IN} = 150\text{nA}$ is applied as an example. Figure 4-16(a) shows the timing diagram for the normal quantization. At the beginning, the input current is quantized by the coarse SAR ADC. During this stage, eight comparison cycles are

Figure 4-15 Schematic of the PWM module

used to do the current comparison. Each cycle includes a rest phase and an integration phase as described earlier. The slope of the integration output V_{OUT} in each cycle is proportional to the difference between the input current and the DAC current. In this design, the resolution of the current comparator, 1 SAR_LSB, is equal to 160nA which is larger than the input current. Therefore, the output of the 8-bit ADC is 00000000, and a residue current 150nA is set into the subsequent PWM module. During this stage, the residue current is finely quantized by the PWM module. The comparator Cmp2 is used to do the voltage comparison. The required integration time T_{INT} is recorded when the integration voltage reaches the constant threshold V_{INT} . In this design, V_{INT} is 0.32V, C_{INT} is 100fF. The required integration time T_{INT} can be evaluated by equation Eq.4.6, which is approximately 0.22 μ s.

The possible coarse conversion error can be generated by any non-idealities. For example, an undesired offset voltage (shown in Figure 4-16(b)) at the input of the dynamic comparator (coarse SAR ADC). It can be caused by the mismatch between the differential input pairs. In this case, the output of the 8-bit ADC is 00000001, where the SAR_LSB is wrong. Meanwhile, the residue current is changed from 150nA to -10nA, where the negative sign means the opposite direction. The new residue current is set into the subsequent PWM module. At this time, the comparator Cmp3 is used to do the voltage comparison, and the required integration time T_{INT} is approximately 3.2 μ s. As a result, the coarse conversion error is resolved by the PWM module.

In conclusion, compared with other current-mode ADCs, the advantages of the proposed two-step current-mode ADC can be summarized as follows:

- 1) The input current of the PWM module is compressed by the coarse SAR ADC into a small range. Therefore, it shortens the integration time and relaxes the time resolution required by the PWM module.

- 2) The PWM module can correct the possible coarse conversion errors which relaxes the design of the coarse SAR ADC.
- 3) The integrator of the PWM module is reused in the coarse SAR ADC as a front-end part of the current comparator, which leads to a compact design.

(a)

(b)

Figure 4-16 Timing diagram of input current quantization (a) in normal case (b) with self-correction

4.2.3 Motion Detector

To further reduce the power consumption of the two-step current-mode ADC, a motion detection module is implemented into the proposed multi-mode sensor. Motion detector is used to detect any light intensity changes in ALS mode. If light intensity changes in a certain range, the proposed ADC is in standby mode and do not consume power. Otherwise, the motion detector will send an enable signal to activate the ADC. During the process of the current quantization, the motion detector is in standby mode until the ADC finishes the quantization and sends an enable signal to it. Therefore, the working principle between the ADC and the motion detector is based on the handshake protocol.

The schematic of the motion detector is illustrated in Figure 4-17. It consists of a current-to-voltage convertor, a switched-capacitor amplifier and two continuous-time comparators. The operational principle of each circuit module is described hereinafter.

Figure 4-17 Schematic of the motion detector

The structure of the current-to-voltage convertor is developed by the general logarithmic photoreceptor. Since the current detection range of the proposed multi-mode sensor is too large in ALS mode, to detect such a wide range of current, the transistor (M_1) should be worked in the saturation region. The relationship between current and voltage of M_1 can be expressed as equation Eq.4.8. In this case, V_1 is proportional to the square root of I_{IN} . After that, the voltage V_1 is sent into a switched-capacitor amplifier. The switched-capacitor amplifier has the same structure as illustrated in Figure 4-5. The output signal (V_2) is used to detect the voltage difference of the input signal (V_1). It can be expressed as equation Eq.4.9. When V_2 reaches the threshold of either continuous-time comparator, the comparator will trigger and set the enable signal to the two-step current-mode ADC. In this design, the reference voltage of Cmp2 (V_{REF2}) is set to 0.3V larger than V_{REF1} ; while the reference voltage of Cmp3 (V_{REF3}) is set to 0.3V lower than V_{REF1} .

$$I_{IN} = \frac{1}{2} \mu_n C_{ox} (V_1 - V_{REF1} - V_{TH})^2 \quad (Eq. 4.8)$$

$$V_2 = V_{REF1} - \frac{C_1}{C_2} \times \Delta V_1 \quad (Eq. 4.9)$$

The schematic of the continuous-time comparator is illustrated in Figure 4-18. It consists of a two-stage operational amplifier (M_1 - M_7), followed by a latch. It consumes 400nA DC current and demonstrates 200 ns delay for an output with a 20 kV/s (0.4nA/20fF) voltage slope.

Figure 4-18 Schematic of the continuous-time comparator

4.3 Sensor Implementation

The proposed multi-mode sensor was fabricated in AMS 0.35 μm 2P4M CMOS technology. Figure 4-19 shows the layout view of the proposed sensor. The resolution of the sensor is 64×64 with a pixel size of $10.4 \times 10.4 \mu\text{m}^2$ and a fill factor of 34.3%. Beside the pixel array, the prototype chip consists of the column parallel CDS circuit, row & column scanner, a two-step current-mode ADC, a motion detector and the global controller. The total area including the pads is $2.23 \times 2.23 \text{mm}^2$. The total area of the inner chip is $1.27 \times 1.27 \text{mm}^2$.

In order to minimize the mismatch of the components, dummy transistors and capacitors were implemented as shown in the layout view of the CDS circuit (Figure 4-19). Meanwhile, symmetric layout was also applied. For mixed-signal parts, digital lines were routed vertically using metal 2; while analog lines were routed horizontally using metal 4. The intermediate layer metal 3 was placed in between and connected to ground, so that the noise coupling between the analog and digital parts can be eliminated. In order to further reduce the noise effect, guard ring was added in each

The pin list of the sensor chip is shown in Table 4-3. In order to achieve low power consumption, the power supplies for the sensor chip are divided into eight groups including power for pixel array, CIS mode (analog/digital), ALS mode (analog/digital), motion detector, pixel global bus and global switches. Therefore, power supplies in different modes can be switchable. Moreover, it can isolate the mutual effects between the different circuit modules. For digital input signals, master clock is used to provide the clock signal for the whole digital system of the sensor; global reset is the enable signal to initialize the whole system; mode select is used to switch the operational modes. Exposure clock, reset and count are used to set the exposure time based on different illumination conditions. For digital output signals, the 13-bit quantization digital codes of the two-step current-mode ADC (8-bit for coarse SAR ADC and 5-bit for PWM module) are scanned out in ALS mode. Besides that, two flag signals are used to indicate which dynamic comparator in PWM module is triggered. For the analog signals, reference and bias signals are applied to the analog circuit modules in the whole system. The only analog output is sent to the off-chip ADC for further signal processing.

Table 4-3 Pin list of the sensor chip

	Input	Output
Power	Power for Pixel Array	
	Power for CIS (Analog)	
	Power for CIS (Digital)	
	Power for ALS (Analog)	
	Power for ALS (Digital)	
	Power for Motion Detector	
	Power for Global Bus	
	Power for Global Switches	
Digital	Master Clock (CLK)	ADC : Coarse SAR ADC (B ₇ -B ₀) PWM Module (C ₄ -C ₀) Flag (F ₁ -F ₀)
	Global Reset (GRST)	
	Mode Select (MS)	
	Exposure Clock (EXP_CLK)	
	Exposure Reset (EXP_RST)	
	Exposure Count (EXP_CNT)	
Analog	Reference & Bias	Analog Output (CIS_OUT)

4.4 Simulation and Testing Results

4.4.1 Testing Setup

The block diagram of the testing platform is illustrated in Figure 4-20. The testing platform consists of a sensor board, a FPGA board and a PC. The sensor board consists of the sensor chip, ADC and DAC. ADC is used to collect the analog output in CIS mode; while DAC is used to provide the required reference and bias voltage to the sensor chip. In order to control the sensor board from PC, a FPGA board is connected in between as a bridge link. The FGPA board consists of the FPGA (Field Programmable Gate Array), memory and PLL (Phase Locking Loop). The FPGA provides the required signals from PC to the sensor board; meanwhile, it also receives and transfers the output digital signals from the sensor board to PC. The memory is used to store data and the PLL is used to generate the required clock signals to each module. The hardware setup for chip testing is shown in Figure 4-21.

Figure 4-20 Block diagram of the testing platform

Figure 4-21 Hardware setup for chip testing

After the hardware setup is finished, a virtual hardware model is needed to build up, in order to connect the hardware together. Two sets of the software coding are required. One is Verilog coding, which is used to generate the digital control signals of the sensor chip (shown in Table 4-3). The other one is C++ coding, which is used to establish the communication interface between the FPGA board and PC. The control signals generated from Verilog coding in different operational modes are shown below.

1) Control signals in CIS mode:

Figure 4-22 Timing diagram of the control signals in CIS mode

Table 4-4 Control signals description in CIS mode

Signal	Type	Direction	Description
CLK	Master Clock	FPGA to chip	Generated from PLL
Soft_Apply	Enable and Reset	PC to FPGA	HIGE enables CIS starting and processing; LOW resets all signals
EXP_RST	Exposure Time Reset	FPGA to chip	LOW enables exposure time writing; HIGH resets exposure time data
EXP_CLK	Exposure Time Clock	FPGA to chip	Clock signal for exposure time writing, should be exactly 10 cycles
EXP_CNT	Exposure Time Count	FPGA to chip	10-bit exposure time data
GRST	Chip Global Reset	FPGA to chip	LOW enables CIS mode; HIGH resets all signals
Data_Valid	Memory Data Valid	FPGA	Generated by FPGA itself, HIGH enables ADC_Data outputting
ADC_Data	Chip output	ADC to FPGA	8-bit onboard ADC output data

2) Control signals in ALS mode:

Figure 4-23 Timing diagram of the control signals in ALS mode

Table 4-5 Control signals description in ALS mode

Signal	Type	Direction	Description
CLK	Master Clock	FPGA to chip	Generated from PLL
Soft_Apply	Enable and Reset	PC to FPGA	HIGE enables ALS starting and processing; LOW stops ALS mode and resets all signals
GRST	Chip Global Reset	FPGA to chip	LOW enables ALS mode; HIGH resets all signals
Data_Valid	Data Valid	Chip to FPGA	Goes HIGH when the valid data is outputting.
DATA	Chip output	Chip to FPGA	15-bit output data: ADC (B ₇ -B ₀), PWM (C ₄ -C ₀), and FLAG (F ₁ -F ₀)

The testing of the sensor chip can be divided into three parts.

- 1) Power consumption test: as shown in Table 4-3, the power supplies for the sensor chip are divided into eight groups. In order to achieve low power consumption, power supplies in different operational modes should be switchable. In this case, the power consumption of different power supplies in each mode was tested.
- 2) ALS function test: the main test item is the linearity between the light intensity and the detection current I_{DET} . The testing platform is shown in Figure 4-24. The light generator is used to generate the uniform light source and the light intensity can be controlled by the lightmeter. In ALS mode, the input light intensity is converted to the induced photocurrent, and then quantized by the proposed two-step current-mode ADC. When light intensity is changed, the corresponding current value should be displayed on the PC screen. The detection current can be expressed as equation Eq.10, where 160nA is the resolution of the coarse SAR ADC.

$$I_{DET} = 160nA \times coarse_ADC + \frac{160nA}{PWM} \quad (Eq. 4.10)$$

- 3) Sensor characteristics test: the main test items include sensitivity, dark current, dynamic range and fixed pattern noise. All the characteristics have been introduced in Section 2.6, and the testing results are shown in the following section.

Figure 4-24 Testing platform for ALS function test

4.4.2 Testing Results

In order to do the testing, 3.3V supply voltage and 10MHz frequency clock is applied to the sensor chip. Table 4-6 shows the power consumption of different power supplies in different operational modes. During standby, almost no power is consumed for each power supply. In CIS mode, the power consumption of ALS readout circuitry is nearly zero and vice versa. The total power consumption in CIS mode is 17.32mW and the total power consumption in ALS mode is 4.68mW.

Figure 4-25 shows the testing result of the linearity between the light intensity and the detection current. The prototype chip is supposed to measure the light intensity up to 20klux. The blue curve represents the ideal result; while the red curve represents the testing result. For the light intensity up to 10klux, the testing result and the ideal result match well. However, for the light intensity from 10klux up to 20klux, the testing result is smaller than the ideal one. It may be caused by the inaccurate reference current in MSB of the current DAC. As mentioned in Section 4.2.2, the

reference current of the DAC is quite sensitive to the final detection result, any mismatch may cause inaccurate result. Therefore, a two-step current-mode ADC with a calibration scheme is proposed in the next chapter.

Table 4-7 shows the important characteristics of the proposed sensor chip. Two sample images taken by the prototype sensor are presented in Figure 4-26.

Table 4-6 Testing result of power consumption

Signal	Standby (μA)	CIS mode (mA)	ALS mode (no detection) (mA)	ALS mode (under detection) (mA)
Pixel Array	0.0175	0.520	0.005	0.005
CIS (analog)	0.0128	4.920	≈ 0	≈ 0
CIS (digital)	0.015	0.248	≈ 0	≈ 0
ALS (analog)	0.011	≈ 0	1.32	1.22
ALS (digital)	0.023	≈ 0	0.028	0.030
Motion Detector	0.031	≈ 0	0.032	0.025
Global Bus	0.002	0.001	0.001	0.001
Global Switch	0.022	0.027	0.031	0.032
Total	0.134	5.248	1.417	1.313

Figure 4-25 Testing result of detection current versus light intensity

Table 4-7 Characteristics summary of the prototype sensor

Process Technology	AMS 0.35μm 2P4M CMOS
Chip Size	2.23×2.23mm ²
Resolution	64×64
Fill Factor	34.3%
Sensitivity	0.35V/lux·s
Dynamic Range	46.63dB
Dark Current	10.6mV/s
FPN	1.25%
Power Consumption @V _{DD} =3.3V	17.32mW (CIS mode)
	4.68mW (ALS mode)

Figure 4-26 Sample images taken by the prototype chip

Chapter 5

Design Improvement: a Two-step Current-mode ADC with Calibration Schemes

According to the testing result of the linearity between the light intensity and the detection current, for the light intensity from 10klux up to 20klux, the testing result is smaller than the ideal one. It may be caused by the inaccurate reference current in MSB of the current DAC. As shown in Figure 4-9, the most sensitive part in the proposed two-step current-mode ADC is the 8-bit binary-weighted current DAC, since eight groups of reference currents (I_{REF0} - I_{REF7}) are implemented by the single transistor working in the subthreshold region. Although the size of the transistors used are quite large, it still show relatively large offsets which would cause severe nonlinearity of the ADC.

In order to improve it, the calibration scheme is indispensable for the ADC design. One common calibration method is to digitally adjust the real value of the parameter to its ideal one with an additional DAC circuit. For example, in order to calibrate I_{REF7} to its ideal value, a sub high-accuracy current DAC branch needs to be added in parallel with it. The DAC's digital inputs are constantly adjusted until its output current exactly cancels the offset of I_{REF7} . However, this method requires lots of extra hardware overhead in the original ADC design, which makes it impractical to be applied in this chip design. In comparison, another calibration method is more hardware-saving. Instead of cancelling the offset, this method directly measures the real values of the reference currents and employs them, instead of the ideal one, to reconstruct the original input. Compared with the first method, this method needs minor modifications to the original ADC design. Only several modules are employed

to measure the real values of the ADC's reference currents. Based on this method, two separate calibration schemes are added in this design to ensure the linearity of the ADC. The first scheme is in charge of calibrating the offsets of the reference currents ($I_{REF7} - I_{REF0}$) in the coarse SAR ADC, while the second one is responsible for the offsets concerned with the PWM modules ($C_{INT} \cdot V_{INT}$).

5.1 Calibration Scheme I

The block diagram of the first calibration scheme is illustrated in Figure 5-1. In this scheme, the real value of each reference current of the coarse SAR ADC is measured accurately with the help of the calibration module I, as shown in the dash line. For example, if the reference current I_{REF7} is selected for calibration, the transistor M_5 would turn on, and I_{REF7} is led to the calibration module I through the bus I_{CAL7} and being measured accurately there. It is noteworthy that all the leakage currents induced by the off switches along this path are minimized by their nearby dummy switches, as discussed in the previous section. For instance, the transistor M_1 turns off during this measurement, while the dummy switch M_0 turns on and pulls the source of M_1 to V_{REF1} . The drain of M_1 (bus I_{CAL1}) is also clamped to the same voltage by the integrator in calibration module I, so that the leakage of M_1 is reduced significantly and has little influence on the current being measured. The calibration module I is a complete PWM module that consists of an integrator, a continuous-time comparator and other digital building blocks. Since it is a global module, the hardware overhead and power consumption of this module have little limitations. A large integration capacitor with 2 pF is used to ensure the current resolution of the measurement. The amplifier and comparator are designed with very large-size transistors biased in the saturation region to reduce the relevant offsets and noises. As a result, the calibration module I is conveniently employed as a high-accuracy current meter. It successively scans all the reference currents ($I_{REF7} - I_{REF0}$) in ALS mode.

Figure 5-1 Block diagram of calibration scheme I

5.2 Calibration Scheme II

The block diagram of the second calibration scheme is illustrated in Figure 5-2. In this scheme, the offsets concerned with the PWM module in the proposed ADC are calibrated by means of a 10 pA calibration current I_{CAL} and the calibration module II. All the photodiodes and the coarse SAR ADC are turned off during this process. The calibration module II controls the calibration current I_{CAL} to flow into the PWM module. For a 10 pA I_{CAL} , the integration time for the PWM module is around 3.2 ms, which surpasses the recording capability of the small 5-bit local memory. In this design, the output of the comparator Cmp2 is transferred to the large 14-bit global memory in calibration module II. Besides that, the calibration scheme also consists of a gray counter, a readout memory and the digital controller. As a result, the parameter of the PWM module ($C_{INT} \cdot V_{INT}$) can be easily calculated by multiplying the corresponding integration time with I_{CAL} .

In summary, the proposed calibration schemes can help to improve the linearity between the light intensity and the detection current. The new architecture of the proposed two-step current-mode ADC will be applied in the next version of the sensor design.

Figure 5-2 Block diagram of calibration scheme II

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, a multi-mode sensor is proposed which merge the functionality of an ambient light sensor into a CMOS image sensor, without increasing power consumption and pixel size. Both of them are the key factors for today's mobile market. The proposed sensor can be applied to any exiting CMOS image sensor architecture.

The proposed sensor has two operating modes. In CIS mode, the sensor works as a normal camera. Power supply is provided to the pixel array by the common metal bus. The signal value and reset value of each pixel are sampled by column parallel CDS circuit. The difference between them is then transferred one by one to an off-chip ADC through a global buffer. In ALS mode, the sensor is used to detect the ambient light illumination. Photodiode in each pixel are connected together as a large one. The total photocurrent is then sent to a 13-bit two-step current-mode ADC for digital quantization. In order to achieve low power application, motion detector is applied to detect any light intensity changes. If light intensity changes in a certain range, the two-step current-mode ADC is in standby mode and do not consume power. Moreover, if the sensor works in one mode, the circuits in the other mode are in standby mode with no power consumption.

In order to detect the total current of the pixel array in ALS mode, a two-step current-mode ADC is proposed by combining the current-domain and time-domain quantization method. The coarse quantization of the input current is implemented in the current-domain with a current-mode SAR ADC. After the coarse A/D conversion,

the residue current is finely quantized in the time-domain by a PWM module. Both of the two blocks in the proposed architecture coordinate well with each other. Firstly, the input current of the PWM module is compressed by the coarse SAR ADC into a small range. Therefore, it shortens the integration time and relaxes the time resolution required by the PWM module. Secondly, the PWM module can correct the possible coarse conversion errors which relaxes the design of the coarse SAR ADC. Furthermore, the integrator of the PWM module is reused in the coarse SAR ADC as a front-end part of the current comparator, which leads to a compact design.

The proposed multi-mode sensor was fabricated in AMS 0.35 μm 2P4M CMOS technology. The size of the chip is 2.23 $\times$ 2.23mm². The resolution of the sensor is 64 $\times$ 64 with a pixel size of 10.4 $\times$ 10.4 μm^2 and a fill factor of 34.3%. Beside the pixel array, the prototype chip consists of the column parallel CDS circuit, row & column scanner, a two-step current-mode ADC, a motion detector and the global controller. The function and the performance of the chip were tested and summarized in the previous chapter.

Based on the testing results, the improvement of the two-step current-mode ADC is proposed. Since the 8-bit binary-weighted current DAC is the most sensitive part and may cause severe nonlinearity of the ADC, two separate calibration schemes are added in this design to ensure the linearity of the ADC. The first scheme is in charge of calibrating the offsets of the reference currents ($I_{\text{REF7}} - I_{\text{REF0}}$) in the coarse SAR ADC, while the second one is responsible for the offsets concerned with the PWM modules ($C_{\text{INT}} \cdot V_{\text{INT}}$). The new architecture of the proposed two-step current-mode ADC will be applied in the next version of the sensor design.

6.2 Future Work

The future work is mainly focused on the next version of the multi-mode sensor design. As mentioned in the previous section, two separate calibration schemes are added in the ADC design in order to ensure its linearity. Besides that, since the proposed sensor can be applied to any exiting CMOS image sensor architecture, 4T APS will be used as the pixel architecture in the next version. Based on it, the correlative circuits design, such as row & column scanner and control logic, should be changed accordingly.

Noise analysis is another consideration for the new version design. In this study, CDS circuit is used to eliminate different kinds of noise. Moreover, in the layout design of each circuit module, guard ring was added to further reduce the noise effect. However, according to the testing results, FPN can still be reached to 1.25%, which is higher than that of the similar sensor design. In this case, to minimize noise effect is quite important in the next version design.

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Bibliography

- [1] M.Bigas, et al., “Review of CMOS Image Sensors”, in *Microelectronic Journal* 37, pp. 433-457, 2006.
- [2] Jun Ohta, “*Smart CMOS Image Sensors and Applications*”, CRC Press, 2010.
- [3] Junichi Nakamura, “*Image Sensors and Signal Processing for Digital Still Cameras*”, CRC Press, 2005.
- [4] Gene P. Weckler, “Operation of p-n Junction Photodetectors in a Photon Flux Integration Mode”, in *IEEE Journal of Solid-State Circuits*, vol. SC-2, no.3, pp. 65-73, Sep 1967.
- [5] Denis Guangyin Chen, et al., “Pulse-Modulation Imaging - Review and Performance Analysis”, in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 1, pp. 64-82, Feb 2011.
- [6] Wang Xiuling, et al., “A High Dynamic Range CMOS Image Sensor with In-pixel Light-to-Frequency Conversion”, in *IEEE Transactions on Electron Device*, col. 53, no. 12, Dec 2006.
- [7] Alistair Kitchen, et al., “PWM Digital Pixel Sensor Based on Asynchronous Self-Resetting Scheme”, in *IEEE Transactions on Electron Device*, vol. 25, no. 7, pp. 171-173, Jul 2004.
- [8] S. -I. Cho, et al., “Low-Power Temperature-Independent Ambient Light Sensor” in *Electronic Letters*, vol. 47, no. 17, pp. 981-983, Aug 2011.
- [9] C.Basci, et al., “A Current-Mode Pixel-Level Ambient Light Suppression Scheme for CMOS Smart Image Sensors”, in *IEICE Society Conference*, Sep 2007.

- [10] Chih-Hao Lin, et al., “A Dual-Mode CMOS Image Sensor for Optical Wireless Communication”, in *IEEE VLSI Design, Automation and Test Conference*, pp. 1-4, Apr 2014.
- [11] Jaehyuk Choi, et al., “A 45.5 μ W 15fps Always-On CMOS Image Sensor for Mobile and Wearable Devices”, in *IEEE International Solid-State Circuits Conference*, pp. 1-3, Feb 2015.
- [12] Bhat, M.S. et al., “Design of Low Power Current-Mode Flash ADC”, in *IEEE Region 10 Conference*, pp. 241-244, Nov 2004.
- [13] Bhatia, V. et al., “Performance Comparison of an Algorithmic Current-Mode ADC Implemented using Different Current Comparators”, in *Multimedia, Signal Processing and Communication Technologies Conference (IMPACT)*, pp. 141-144, Dec 2011.
- [14] Liu Xilin, et al., “A Low Power Multi-mode CMOS Image Sensor with Integrated On-chip Motion Detection”, in *IEEE International Symposium on Circuits and Systems Conference*, pp. 2416-2419, May 2013.
- [15] Wen-Sin Liew, et al., “A Moving Binary Search SAR-ADC for Low Power Biomedical Data Acquisition System”, in *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 646-649, Nov 2008.
- [16] Johannes Uhlig, et al., “Hybrid Incremental- $\Sigma\Delta$ -ADC for Ambient Light Sensing Applications”, in *IEEE International Symposium on Circuits and Systems Conference*, pp. 1256-1259, May 2013.
- [17] Praveen Prabha, et al., “A VCO-based Current-to-Digital Converter for Sensor Applications”, in *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, pp. 1-4, Sep 2014.

- [18] Masaki Sakakibara, et al., “A High-Sensitivity CMOS Image Sensor with Gain-Adaptive Column Amplifiers”, in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1147-1156, May 2005.
- [19] Hon-Sum Wong, “Technology and Device Scaling Considerations for CMOS Imagers”, in *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2131-2142, Dec 1996.
- [20] Min-Woong Seo, et al., “A Low Noise Wide Dynamic Range CMOS Image Sensor with Low-Noise Transistors and 17b Column-Parallel ADCs”, in *IEEE Sensors Journal*, vol. 13, no. 8, pp. 2922-2929, Aug 2013.
- [21] A.Asalam-Siddiqi, et al., “A 128-pixel CMOS Image Sensor with Integrated Analog Nonvolatile Memory”, in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1497-1501, Oct 1998.
- [22] S. Kawahito, “Signal Processing Architecture for Low-Noise High-Resolution CMOS Image Sensors”, in *IEEE Custom Integrated Circuits Conference*, pp. 695-702, Sep 2007.
- [23] Hidekazu Takahashi, et al., “A 1/2.7-in 2.96 MPixel CMOS Image Sensor with Double CDS Architecture for Full High-Definition Camcorders”, in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2960-2967, Dec 2007.
- [24] S. W. Han and E. Yoon, “Area-Efficient Correlated Double Sampling Scheme with Single Sampling Capacitor for CMOS Image Sensors”, in *Electronic Letters*, vol. 42, no. 6, pp. 335-337, Mar 2006.
- [25] Matteo Perenzoni, et al., “A 160×120-Pixels Range Camera with In-Pixel Correlated Double Sampling and Fixed-Pattern Noise Correction”, in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1672-1681, Jul 2011.

- [26] Woongtaek Lim, et al., “A Low Noise CMOS Image Sensor with a 14-bit Two-Step Single-Slope ADC and a Column Self-Calibration Technique”, in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 48-51, Dec 2014.
- [27] Liu Lifen, “*Low-Power Column-Parallel ADC for CMOS Image Sensor by Leveraging Spatial Likelihood in Natural Scene*”, Master thesis, Nanyang Technological University, 2015.
- [28] Yang Liu, “*The Design of a High Dynamic Range CMOS Image Sensor in 110nm Technology*”, Master thesis, Delft University of Technology, 2012.
- [29] Wei Gao, “*Low Power Design Methodologies in Analog Blocks of CMOS Image Sensors*”, PhD thesis, York University Toronto, Ontario, 2011.
- [30] Jaehyuk Choi, “*An Energy-Efficient Adaptive CMOS Image Sensor*”, PhD thesis, The University of Michigan, 2013.