Topologically reduced multilevel power converters for alternative energy sources

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NANYANG
TECHNOLOGICAL
UNIVERSITY

**TOPOLOGICALLY REDUCED
MULTILEVEL POWER CONVERTERS
FOR ALTERNATIVE ENERGY SOURCES**

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**INTERDISCIPLINARY GRADUATE SCHOOL
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2016

For my beloved parents and family

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Abstract

The ever increasing demand of energy and the evidence of global warming have forced many nations to divert renewable and clean energy sources into the mainstream for power generation. Statistical results have proven that the total amount of power capacity installed yearly is increasing tremendously in order to meet the supply demands. In Singapore, the government bodies and authorities are also making plans in shaping a future sustainable city. With its known geographical location and its limited land size, solar PV power systems would be more recommendable for integration into the buildings. Clean energy such as fuel cells power systems are still under-going testing process to serve as the primary energy sources for many housing blocks. Hence, the design of higher power conversion is required to meet the pace of achieving higher power generation.

Multilevel converters are the recent trends for implementation in high power applications. With the multilevel approach, better power quality can be achieved more efficiently by synthesizing higher number of output voltage levels. Many research works on multilevel topologies are proposed constantly, but are still not available commercially. Therefore, this report investigates the advantages and disadvantages of the classical and the recent multilevel converters used in the industrial environment. By doing so, the investigation can provide a better understanding of the gap difference between research conducted and the current industrial needs. Hence, more industry based constructive research works can be carried out in this report based on the industry demand.

The research work outlined in this report begins with the study of fundamental needs in designing multilevel converters which is the switching modulation schemes. The designs and the implementation of multilevel modulation methods are relatively important in order to achieve better power quality. Investigations are carried out to address the limitation of existing switching strategies. Few proposed modulations are presented and have successfully attained the advantageous properties with the hybrid of sinusoidal carrier-based modulations. These proposed hybrid SPWM methods are explained with detailed mathematical analysis and verified with experimental results.

On top of that, the major concerns in multilevel converters for achieving higher output voltage levels are mentioned especially the classical multilevel flying capacitor inverter (MFCI) topology. MFCI is one of the most attractive multilevel topology but it is not welcome in many high power applications due to its restriction to synthesize higher number of output voltage levels. Thus, two proposed reduced modular cell inverters named as lightweight flying capacitor inverter (LFCI) and reduced flying capacitor inverter (RFCI) are presented and proven the feasibility with the experimental prototypes. Comparative analysis is also carried out to highlight the improvements made.

The proposed reduced flying capacitor approach is also investigated for the rectifier operation which achieved the reduced flying capacitor rectifier (RFCR). In this case, the RFCR allows having bidirectional power flow operation while reducing the component counts. Besides that, unity power factor control together with the closed-loop flying capacitor voltage balancing scheme are experimented to prove the feasibility. Dynamic performances are also evaluated with sudden stepped change in the power factor and the load conditions.

The thesis also continues to investigate the performance of the well-known active neutral point clamped (ANPC) inverter and highlighted the possible challenges faced, such as power quality and common mode voltage issues which are not reported in the literature till date. Hence, a multiple voltage quantities enhancement (MVQE) control is proposed to achieve better dc-link capacitor and flying capacitor voltages balancing while reducing the dc-link ripples.

Output voltage harmonic profile is further enhanced as well with another newly designed hybrid SPWM scheme named as interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM). Common mode voltage reduction technique is also presented using the new hybrid ISC-PD-PWM scheme to make ANPC more attractively suitable for its well-known higher medium voltage drive applications. Converter performances are further enhanced with significant reduction in the average switching frequency operation and the power device losses. Lastly, the future direction for the continuous research will also be discussed to optimize the converter design so that conceptual ideas can be realized in practices to meet the industrial needs.

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List of Notations

Abbreviations

GTO	Gate Turn-Off Thyristor
IGCT	Integrated Gate-Commutated Thyristor
IGBT	Insulated Gate Bipolar Transistor
THD	Total Harmonic Distortion
EMI	Electro-Magnetic Interference
VSI	Voltage Source Inverter
CSI	Current Source Inverter
LCI	Load Commutated Inverter
mL	Number of m Levels
NPC	Neutral Point Clamped Inverter
MDCI	Multilevel Diode Clamped Inverter
MFCI	Multilevel Flying Capacitor Inverter
LFCI	Lightweight Binary-Based Multilevel Flying Capacitor Inverter
RFCI	Reduced Flying Capacitor Inverter
MCHB	Multilevel Cascaded H-Bridge Inverter
M2I / M ² I	Modular Multilevel Inverter
ANPC	Active Neutral Point Clamped Inverter
DSP	Digital Signal Processors
CBM	Carrier-Based Modulation
SVM	Space Vector Modulation
PWM	Pulse-Width Modulation
SPWM	Sinusoidal PWM
LSC-PWM	Level-Shifted Carrier PWM
PD-PWM	Phase-Disposition PWM
POD-PWM	Phase-Opposition-Disposition PWM
APOD-PWM	Alternative Phase-Opposition-Disposition PWM
PSC-PWM	Phase-Shifted Carrier PWM
PSC-POD-PWM	Phase-Shifted Carrier Phase-Opposition-Disposition PWM
PSC-PD-PWM	Phase-Shifted Carrier Phase-Disposition PWM
ISC-PD-PWM	Interleaved Sawtooth Carrier Phase-Disposition PWM
$M_{x_{sine}}$	Modulation Index
f_s / f_c	Switching Frequency / Carrier Frequency
CMV	Common Mode Voltage

Chapter 1

Introduction

This chapter discusses briefly the trends of energy consumptions with the interest of pursuing renewable energies to reduce the amount of fossil fuels needed for power generation. Statistical results of energy consumption and trends of renewable energies production are presented based on global and Singapore perspective. Power electronic converters play an important role to improve energy efficiency during the energy conversion process.

1.1 Global Energy Consumption Demands

The demand for energy needs in our daily life has been increasing tremendously over the last two decades, partly due to the increased of the population growth. 12476.6 million tonnes of oil equivalent (Mtoe) of primary energy is consumed by the global in 2012 with an increase of 1.8% as compared to the previous year 2011 [1] in Fig. 1.1. The global primary energy consumption is expected to further increase by 36% to about 16 billion tonnes of oil equivalent (Btoe) in the year 2030 [2].

Fig. 1.1 Global primary energy consumption [1].

Fig. 1.2 Global primary energy consumption across respective regions in 2012 [1].

The amount of primary energy consumed by Asia Pacific (includes India and China) increased extremely high in the last decade as compared to the other regions. Asia Pacific has now become the major consumer (40.01%) of primary energy sources as shown in Fig. 1.2. The significant increases of primary energy consumption in Asia Pacific in 2012 over the previous year 2011 come from Bangladesh (7.5%), China (7.4%), India (5.1%), Thailand (5.5%) and Vietnam (7.1%). The amount of energy demands for these mentioned countries are increased due to the economic development and the industrialization process.

The evident of climate change in the recent years with the increasing demand of global energy consumption, these constraints have motivated many worldwide nations to build and develop towards a more sustainable environment by shifting renewable energy into mainstream. However, oil remains the leading fuel in global energy consumption in 2012 and followed by the coal consumption based on Fig. 1.3. In [1], Asia Pacific is the only region that has more than 50% of the primary energy consumption depends highly on coals, while natural gas is the dominant primary energy in Europe and Eurasia, and oil for the remaining regions.

Fig. 1.3 Principal components of global primary energy consumption [1].

Based on Fig. 1.3, the total amount of nuclear energy has been reduced by 6.9% due to the aftermath of natural disaster occurred in Japan Fukushima and the shutdown of nuclear power plants in Europe. Meanwhile, both hydropower and renewable energy have reached the recorded shares of global energy consumption of 6.7% and 1.9% respectively.

Even though there are many challenges encountered during the transition towards a sustainable future energy, many international agencies, government bodies and including the industrial associations which have been set up in joint action to facilitate and accelerate the pace for the improvements and the development of renewable energy power generations. International non-profitable association such as Renewable Energy Policy Network for 21st Century (REN21) provides a platform for worldwide nations to exchange knowledge in terms of policies, technologies and even economic financials based with the data collected in [3] while emphasizing the importance of renewable energy.

Many institutions like International Energy Agency (IEA) and International Renewable Energy Agency (IRENA) provide tracking of clean energy data, information on energy efficiency policy deployment with case studies and the market trends in renewable energy power generation [4-7] to support countries during this transition period. The future plans for global renewable energy markets and trends can be found in [2, 4, 8], as well as the White Papers on “Transitioning to a Renewable Energy Future” [9] and “Renewable Energy Future for the Developing World” [10] by International Solar Energy Society (ISES).

In 2012, renewable energy power generation has successfully supplied 19% of the global final consumption with total renewable power capacity installed exceeding 1470 GW [3], while targeting to provide 25% of the final electricity consumption from renewable energy by 2020 [4]. Fig. 1.4 shows the respective global renewable energy capacity installed and the amount of increment within a year.

Fig. 1.4 Global renewable energy capacity in 2012 [3].
(a) cumulative installed capacity. (b) Increment of Renewable Energy as compared to the previous year 2011.

Hydropower among the rest of the renewable energy provides the largest portion of energy supplies with approximately 990 GW of total installed capacity in the global, generating an estimation of 3700 TWh of electricity in 2012. However, only 3.13% of new hydropower capacity (30 GW) is added [3]. The growth for hydropower is modest due to its mature technologies. Besides that, geothermal power and bio power are also mature in its technologies, which result a slow and steady growth of 2.63% and 12.16% in 2012 respectively.

The second major renewable energy supplier is the wind power which has a total of 283 GW installed capacity up to date. On top of that, wind power is still growing fast at a steady exponential rate with an increase of 20.43% new capacity added in 2012 as well. The competitiveness among the industries helps to ensure further improvements to be made such as growing the scale of wind turbine to meet the global demands, as well as improving the overall efficiency while reducing the costs, operations and maintenances are also achieved. Therefore, there are still plenty of rooms for wind power to grow in the upcoming future to provide more renewable power generation.

Both Solar PV and Concentrating Solar Thermal Power (CSP) contribute significant growth of 40.85% and 66.67% within a year, by achieving a cumulative total capacity of 100 GW and 2.5 GW respectively. Solar energy is not the major contributor of renewable power generation as compared to hydropower and wind power, mainly due to the space constraints for the developed cities in order to achieve higher capacity installed. However, new solar technologies (such as higher efficiency solar modules) are developed in the recent years. Hence, the installed capacity of solar PV energy harvesting would be expected to increase exponentially in the next few years.

1.2 Singapore Energy Consumption Demands

Fig. 1.5 Singapore primary energy consumption [1].

The amount of primary energy consumption in Singapore has also increased linearly from 41.6 Mtoe to 74 Mtoe within the last decade as shown in Fig. 1.5. However, the rate of primary energy consumed in Singapore increases relatively slower as compared to the other countries in Asia Pacific regions [1]. Due to the geographical location of Singapore and its limited natural resources, Singapore is still highly dependent on the fossil fuels for its energy supplies while facing the challenges of replacing them with alternative energy [11].

Fig. 1.6 Singapore electricity demands across respective sectors in 2011 [11].

Fig. 1.7 Singapore electricity consumption from 2009 to 2011 [11].

Despite being one of the most densely populated in the world, the amount of primary energy consumed in 2012 over the previous year 2011 has increased only by 0.135%. This shows that Singapore has successfully slowed down the rate of energy consumption with the progressive sustainable energy growth in plan.

The industrial-related sector has the highest electricity consumption which takes up 40.20% of the overall energy consumption primarily due to the machine loads, followed by the commerce and service-related sector (37.51%) and the households sector (15.72%) as shown in Fig. 1.6. However, the increment of electricity consumption by the respective sectors over the recent years is not very high. Based on Fig. 1.7, the amount of electricity consumed in 2011 compared with the previous year 2010 shows an increase of 1.46% in the industrial sector, 3.57% in the commerce and service-related sector and 6.2% in the transport sector, meanwhile a decrease of electricity demands is achieved in the households sector and others [11].

Fig. 1.8 Singapore energy consumption based on: (a) HDB buildings. [12] (b) Residential households [13].

Further breakdown of energy consumption for the residential is shown based on the HDB buildings [12] and households context [13] in Figs. 1.8(a) and 1.8(b) respectively, where residential consumes 15.72% (about one-fifth) of Singapore total electricity demands. Lightings for both common area and outdoor are accounted for the most energy consumption (50%), followed by the lifts (23%) in the HDB blocks (Fig. 1.8(a)). The major energy demands for the residential households (Fig. 1.8(b)) would be the air conditioning systems (30%) due to tropical hot and humid weather, 24-hours operated refrigerator (17%) and followed by lighting (10%).

Singapore authorities and agencies such as Energy Market Authority (EMA) and National Environment Agency (NEA) play its roles in reducing the global warming by making future plans in shaping a new sustainable landscape [14, 15] as well as addressing the policies on energy efficiency [13]. Energy Efficient Programme Office (E²PO) is set up and led by NEA to ignite the energy efficiency revolution in green buildings, transportation and even electrical appliances. Several energy efficiency strategies are developed like creating awareness to the public, supporting the research

and developments of energy efficiency technologies while promoting and building both the knowledge base and the professional expertise in energy management.

Taken into consideration of Singapore limited geographical area with its population, location and weather condition, solar energy would be the most recommended renewable energy to be implemented here as compared to the others. Therefore, there is a record of leap increased in total solar PV systems installed in different areas of Singapore for past five years from 361.93 kWp to 9989.3 kWp [16] as shown in the Fig. 1.9.

Since Singapore has a well-covered national power grid, the solar PV systems would be more effective to be implemented as grid-connected applications where a reduction of dependency on utility can be achieved with the increased in renewable energy production. Knowing that industrial-related sector is the most energy intensive followed by the commerce and service-related sector (Fig. 1.6), hence the total cumulative installed capacity of the solar PV grid-connected systems for those non-residential is much higher as compared to those installed for residential purpose. As a

Fig. 1.9 Cumulative installed capacity of grid-connected solar pv systems in Singapore [16].

result, the dependency on the amount of fossil fuels needed for electricity production can be further reduced especially for those non-residential sectors. A detailed list of solar PV grid-connected systems installed at different sites of Singapore can be found in [17].

Standalone or off-grid solar PV systems are less preferable in Singapore, but are still applicable and installed at those areas where utility grid supply is outside its reach such as those street lamps, speed radars and parking sign lightings. However, these off-grid solar PV systems are needed to be operated with a rechargeable lead-acid battery bank which serves as an energy storage. Detailed policies deployed on solar PV systems planning, installation process, licensing, incentives, operations and maintenances by the Singapore authorities can be found in [18-20].

Not only focusing primarily in those non-residential sectors, Building and Construction Authority of Singapore (BCA) together with NEA are also encouraging more in designing sustainable buildings and zero energy buildings to reduce the energy cost. The important aspects for those energy efficient building passive designs are the natural ventilation, proper shading facades and thermal performance analysis of the buildings based on the ASHRAE Standards 55-2004, 90.1-2007, 189 and 62.1-2010, coupled these with the optimization of lighting and air-conditioning system control will help to ensure and provide an optimal energy performance.

Apart from harvesting energy from solar PV, alternative plans are explored by Housing & Development Board (HDB) such as using fuel cell technologies as the

primary sources to generate clean power and supplies to the electricity needs for common areas (lightings, lifts and water pumps) in residential HDB buildings [21].

On top of that, sustainable strategies are applied for transportation areas as well like Singapore's First Hybrid Fuel Cell-Battery Bus [22], Singapore's First Driverless Electric Vehicle [23] and also Singapore's Rapid Transit System [24]. There are many more green prints of clean and renewable energies planned for others areas and sectors, which are currently still on-going researches and testing phases under the management of the authorities.

1.3 Power Electronic Technologies and Market Trends

Energy efficiency plays a key role in our daily energy consumption. Many worldwide nations are diverting the renewable technology to substitute conventional energy systems powered by fossil fuels, coals and oil consumptions. Higher energy efficiency demonstrates better utilization of final site energy from the primary energy source, hence reducing the amount of energy losses during the conversion or transmission process is essential.

The first power rectification (AC to DC conversion) designed by a Hungarian engineer, Béla B. Schäfer, was heavily dependent on those big and bulky mercury-arc valves in the early 1910s [25] for Bernese Oberland railway application. However, with the rate of new technologies advances rapidly based on the Moore's Law, new power electronic switching devices with higher efficiency and better reliability are manufactured nowadays. The evolution of power electronics started from the thyristor (first power semiconductor proposed by William Shockley in 1950), to GTO (Gate Turn-Off Thyristor) in mid 1980s, IGCT (Integrated Gate-Commutated Thyristor) in mid 1990s and IGBT (Insulated Gate Bipolar Transistor) in late 1990s till to date. These power semiconductor devices are now popularly utilized to replace the old and bulky technologies; hence a lighter weight and better efficiency of power converters can be achieved.

In addition, power electronic converters are not only applied for power conversion purpose but also served as active filtering, compensation and power conditioning at the same time. By doing so, these allow to enhance the power quality, maximize the power transfer efficiency as well as meet the specific requirements of the subsystems

like motor drives or machines by controlling the voltage, frequency and power factor. Therefore, power electronic converters have become importance in our daily life technologies. The growth of power electronic inverter market is expected to be increased continuously due to the demands in electrical transportation and renewable energies from \$45 billion in 2012 up to \$71 billion by 2020 [26].

Conventionally, power conversion for DC to AC was achieved with bridge chopper inverter by Ray E. Morgan in 1964 [27]. However, due to the limitation of the power rating in the semiconductor devices, the topology of the bridge circuit (also named as two-level voltage source inverter – VSI) does not fit for those medium to high power applications.

The first multilevel approach based on three-level neutral-point clamped inverter (NPC) topology was proposed in 1981 and experimented with squirrel-cage induction motor by Akira Nabae *et al* in [28]. The performances of 3L-NPC have proven that better efficiency is achieved with lower total harmonic distortion (THD) as compared to the conventional VSI. On top of that, 3L-NPC is also applicable for high power variable-speed drive system.

Multilevel topologies have the ability to overcome the restriction of the power ratings of the semiconductor devices by synthesizing the output voltage waveform into multiple stepped levels. Moreover, when higher number of voltage stepped levels can be achieved, the output staircase stepped waveform will look closer to a sinusoidal-like waveform. Thus, lower harmonic distortion is achieved which in turns allow to further reduce the size of the bulky passive filter elements.

TABLE 1.1
CONFIGURATIONS AND TOPOLOGIES OF INDUSTRIAL MULTILEVEL CONVERTER DRIVES FOR MEDIUM-HIGH POWER APPLICATIONS

Manufacturers	Model	Power (kVA)	Voltage (kV)	Rectifier	Inverter	Power Semiconductors (Inverter)
ABB [29]	ACS1000	400-2000 (A)/ 400-5950/400-6090	2.3(A)/3.3/4.0	12(Standard)/24* Pulse Rectifier	3L-NPC	IGCTs (Without parallel or series connected)
	ACS1000i	400-1900 (A)/ 400-2330 (A)	3.3/4/4.16	24 Pulse Rectifier		
	ACS2000	344-2750/344-3080	6 / 6.6/6.9	5L-ANPC (BTB) (AFE)	5L-ANPC	IGBTs
	ACS5000	7000-31200 (W)/ 7700-34300 (W)/ 8000-35900 (W)	6/6.6/6.9	36 Pulse Rectifier	5L-VSI MF	IGCTs (Without parallel or series connected)
	ACS6000	7000-36000	3.3	3L-NPC (BTB) (AFE)	3L-NPC	IGCTS
	MEGA DRIVE	2000-72000	2 x (2(W)/3.4(W)/5(W)/ 6.6(W)/7.8(W)/9(W)/10.2(W)) 2 x (2(W)/3.4(W)/5(W))	12 Pulse Rectifier 24 Pulse Rectifier	2 x 2L-VSI 2 x 2L-VSI	Thyristors
ALSTOM [30]	ALSPA VDM5000	1400-7200 (W)	2.3/3.3/4.16	6/12/18 Pulse Rectifier	2L-VSI	HV IGBTs
	ALSPA VDM6000	300-3000 (A)/ 2200-8000 (W)	2.3/3.3/4.16	6/12/18 Pulse Rectifier	4L-FCI	HV IGBTs
	ALSPA VDM7000	7000-9500 (W)	3.3	6/12/18 Pulse Rectifier	3L-NPC	GTO
ANSALDO SISTEMI INDUSTRIALI [31]	Silcovert TN	1300-10400 (A)/ 21600(W)	2.4/3.3	12/24 Pulse Rectifier (DFE) /	3L-NPC	IGBTs
	Silcovert GN	9000-24000 (W)	3.3	3L-NPC (BTB) (AFE)		IGCTs
	Silcovert TH	8100 (A)/18700 (W)	4.16/6/6.6/7.2	6(2L- FB VSI)/ 12(3L-FB NPC) Pulse Rectifier per MC	13L-Cascaded (2L-FB VSI) /	IGBTs
	Silcovert NH	1500-3700 (A)/ 2900-14400 (W)	4.16/6/6.6		25L-Cascaded(3L-FB NPC) (6 sets MC)	IGBTs
ARROWSPEED [32]	AS7000	470-11690 (A)	2.3/4.16/6/11	6 Pulse Rectifier per MC	11L-Cascaded(2L-FB VSI) (5 sets MC)	IGBTs

(A): Air Cooling, (H): Heat Pipe Air Cooling. (W): Water Cooling, (*): Optional

(DFE): Diode Front End, (AFE): Active Front End, (BTB): Back to Back Configuration, (VSI): Conventional Voltage Source Inverter, (MF): Multilevel Fuse-less Topology, (NPC): Neutral Point Clamped

(FCI): Flying Capacitors Inverter, (ANPC): Active Neutral Point Clamped, (M2I): Modular Multilevel Inverter, (FB): Full-Bridge, (MC): Modular Cells

TABLE 1.1 (Continued)
CONFIGURATIONS AND TOPOLOGIES OF INDUSTRIAL MULTILEVEL CONVERTER DRIVES FOR MEDIUM-HIGH POWER APPLICATIONS

Manufacturers	Model	Power (kVA)	Voltage (kV)	Rectifier	Inverter	Power Semiconductors (Inverter)
EATON [33]	SC9000 NEMA	700-13445 (A)	2.4/4.16	24 Pulse Rectifier	3L-NPC	IGBTs
	SC9000 IEC	700-12860 (A)	3.3/4.16			IGBTs
BEIJING LEADER & HARVEST ELECTRIC TECH [34]	11kV Series	393.75-11000 (A/W)	11	6 Pulse Rectifier per MC	19L-Cascaded(2L-FB VSI) (9 sets Modular Cells)	IGBTs
INGETEA M [35]	MV100	800-4000 (A) (DFE)/ 2000-15000 (W) (AFE)	3.15/4.16 (DFE) / 3.3/4.16 (AFE)	12/24 Pulse Rectifier (DFE) / 3L-NPC (BTB) (AFE)	3L-NPC	IGBTs
	MV500	6000-36000 (W)	3.15 (DFE) / 3.3 (AFE)	12/24 Pulse Rectifier (DFE) / 3L-NPC (BTB) (AFE)	3L-NPC	IGCTs
LS INDUSTRIAL SYSTEMS [36]	LSMV-110 Series	800-13000 (A)	11	6 Pulse Rectifier per MC	13L-Cascaded(2L-FB VSI) (6 sets MC)	IGBTs
SIEMENS [37]	SM120	7200 (W)	4.16	3L-NPC (BTB) (AFE)	9L-M2I	IGBTs
	GM150	1300-10100 (A)/ 2000-13000 (W)	4.16	12/24 Pulse Rectifier	3L-NPC	HV IGBTs / IGCTs (3.3kV)
	SM150	4300-5800 (A)/ 5800-7200 (W)	4.16	3L-NPC (BTB) (AFE)	3L-NPC	HV IGBTs / IGCTs (3.3kV)
	Perfect Harmony	6150-33460 (W)	13.2/13.8	6 Pulse Rectifier per MC	13L-Cascaded(2L-FB VSI) (6 sets MC)	LV IGBTs
SCHNEIDER ELECTRIC [38]	ALTIVAR 1000	1260-5200 (A)/ 1490-13260 (W)	2.3/3.3/4.16*/6.6*/7.2*/10*/13.2*	12/24 Pulse Rectifier / 3L-NPC (BTB) (AFE)	3L-NPC	HV IGBTs
	ALTIVAR 1200	470-14750 (A)	10	6 Pulse Rectifier per MC	19L-Cascaded(2L-FB VSI) (9 sets MC)	LV IGBTs
RONGXIN POWER ELECTRONIC [39]	10kV Series	250-10000 (H/W)	10	6 Pulse Rectifier per MC	13L-Cascaded(2L-FB VSI) (6 sets MC)	LV IGBTs

Note: Information in the Table 1.1 is provided according to the respective references based on the author best knowledge valid to the submission of the report, therefore any differences or unintentional omissions could be possible.

TABLE 1.1 (Continued)
CONFIGURATIONS AND TOPOLOGIES OF INDUSTRIAL MULTILEVEL CONVERTER DRIVES FOR MEDIUM-HIGH POWER APPLICATIONS

Manufacturers	Model	Power (kVA)	Voltage (kV)	Rectifier	Inverter	Power Semiconductors (Inverter)
WEG [40]	MVW01	(Max) 7500 (A)	2.3/3.3/4.16	12/18/24 Pulse Rectifier	3L-NPC / 3L-FB NPC	IGBTs
			6/6.3/6.6/6.9	36 Pulse Rectifier	5L-NPC / 5L-FB NPC	
TOSHIBA MITSUBISHI- ELECTRIC INDUSTRIAL SYSTEMS CORPORATION [41]	TMdrive-30	2000 (H) / 4000 (H)	1.25	3L-NPC (BTB) (AFE) / 2 x 3L-NPC (BTB) (AFE)	3L-NPC / 2 x 3L-NPC	IGBTs
	TMdrive-50	3000 (W) / 6000 (W)	3.4	3L-NPC (BTB) (AFE) / 2 x 3L-NPC (BTB) (AFE)	3L-NPC / 2 x 3L-NPC	IGBTs
	TMdrive-70	5000-40000 (W)	3.3	12/24 Pulse Rectifier / 3L-NPC (BTB) (AFE)	3L-NPC / 3L-FB NPC	IEGTs
	TMdrive-80	5000-48000 (W)	3.3	3L-NPC / 2 x 3L-NPC (BTB) (AFE)	3L-NPC / 2 x 3L-NPC	IGCTs
	TMdrive-XL55	8000 (W) / 16000 (W)	6/6.6	12 Pulse Rectifier per MC	13L-Cascaded(3L-FB NPC) (3 sets MC)	IGBTs
	TMdrive-XL75	20000 (W)	6	12 Pulse Rectifier per MC	13L-Cascaded(3L-FB NPC) (3 sets MC)	IEGTs
	TMdrive-XL80	15000-30000 (W)	3.8	12/24 Pulse Rectifier per MC	3L-NPC / 2 x 3L-NPC	GCTs
	TMdrive-XL85	30000 (W)	6.6-7.2	12 Pulse Rectifier per MC	15L-Cascaded(3L-FB NPC) (3 sets MC)	GCTs
	TMdrive-MVG	600-9000 (A)/ 660-10000 (A)	10/11	6 Pulse Rectifier per MC	15L-Cascaded(2L-FB VSI) (3 sets MC)	IGBTs
	Dura-Bilt5i MV	470-7014 (H)/ 700-9352 (H)/ 935-16366 (H)	2.3/3.3/4.16	24 Pulse Rectifier	3L-FB NPC	MV IGCTs
YASKAWA [42]	FSDrive-MV1S	200-3000 (A) / 500-2900 (A) / 400-6000 (A)	3/3.3 / 4.16 / 6/6.6	6 Pulse Rectifier per MC	7L/9L/13L-Cascaded (2L-FB VSI) (3/4/6 sets MC)	LV IGBTs
	FSDrive-MV1000	200-3700 (A) / 400-7500 (A) / 660-12000 (A)	3/3.3 / 6/6.6 / 10/10.5/11	6 Pulse Rectifier per MC	9L/13L/21L-Cascaded (3L-FB NPC) (2/3/5 sets MC)	LV IGBTs

Based on the mentioned captivating advantages which can overcome the problems faced in conventional VSI, multilevel converters have become the preferred choice and attractive for high power applications. Hence, a series of latest multilevel converter drives available in today's market for the industrials' medium to high power motor applications [29-42] are listed in the Table 1.1. The popular multilevel converters topologies employed and developed by the manufacturers are 2L-FB VSI, 3L-NPC and cascaded modular structure. Currently, 25 levels output voltage stepped waveform have been successfully achieved for 14.4 MVA output power by an Italian company, Ansaldo Sistemi Industriali, using six cascaded modular cells of 3L-FB NPC.

Based on Table 1.1, multilevel converters are considered mature technologies in the industry. However, many leading manufacturers are still facing problems and challenges in developing advance multilevel converters while trying to improve energy efficiency by minimizing the losses occurred in the semiconductor devices and passive elements. This drastically affects the growth of power electronic converters using multilevel approach. Comprehensive solutions are required to solve these issues and hence motivating more research and inquisitiveness among power electronic engineers.

In the near future, silicon based semiconductor devices will be replaced by the silicon carbide (SiC) and even Gallium Nitride (GaN) materials due to their better efficiency performance. SiC technologies are used in the markets recently but are not popularly implemented due to their cost. The prices would be expected to decrease when it becomes more stabilized. However, the SiC device market has shown a growth of 38%

increment every year [43, 44]. With the emerging technology in mind, press-pack power module for IGBTs is also being explored to enable higher current ratings with the compact size of semiconductor switches for high power applications [45]. Alternative methods or technologies are currently undergoing in the research and development process.

Besides relying solely on the semiconductor industries for better energy performances, the design of multilevel topologies is also one of the major concerns for industrial developments in terms of structure complexity, controller design, reliability and the cost of the system. Most of the power electronic converters are interfaced between the utility grid and non-linear loads such as fluorescent lightings, air conditionings, industrial motor drives that result a flow of harmonic currents into the electrical power systems affecting the other equipments and interferences to any other communication circuits. Hence, voltage and current harmonic distortion will affect the energy efficiency performance.

Therefore, harmonic contents must be analyzed during the designing process and be controlled to comply with the IEEE Std 519-1992. For those power converters that are installed in any renewable energy power systems or distributed resources grid-connected systems like wind, solar and fuel cells have to fulfill the requirements of IEC 61400-21, IEC 61000-2-4, IEEE 1547 and UL 1741.

1.4 Motivations and Objectives of Work Orientation

The alarming rate of energy consumption increased yearly is a major concern to many nations worldwide due to the global warming. Tremendous research has been carried out to maximize the output power range harvested from the renewable and clean energy. Naturally, new designs and optimization of power electronic converters have to be explored in order to achieve higher energy efficiency while meeting the demand of continuous growth in renewable and clean energy market especially for wind, solar and fuel cell energy.

The recent trends of installing high power levels in terms of multi-MW for wind farms and solar power plants in many countries including Singapore motivated further in-depth research on power electronic converters. High power conversion is required to keep up its pace for achieving higher power generation from these alternative energy sources. Hence, multilevel approach is the only solution for high power conversion. Many research works have been developed in the past two decades in designing a better efficient topology. Moreover, multilevel converters are proven technologies in the industrials and are applicable for medium to high power motor drives as shown in Table 1.1.

Despite of many new multilevel designs have been proposed by the researchers, but those topologies are not welcome by the industrial markets yet. The motivation of the research work is to investigate the real problems behind that restrict the industrials to evolve in developing more advanced multilevel topologies. By doing so, more constructive methods can be proposed and carried out based on practical perspective.

The objectives of research work will be focused on optimizing the design of multilevel converters with appropriate control algorithms to achieve high reliability and excellent energy efficiency. In most cases, applications such as renewable energy suppliers and industrial motor drives are grid-connected systems, thus design has to comply with the IEEE and IEC standards to produce good power quality. Hence, research will also cover the studies on different modulation strategies to produce low harmonic distortion and prevent electromagnetic interference (EMI). Mathematical analysis for proposed modulation schemes is presented as well.

Power converters with topologically reduced component counts, size and cost are of great interest to industrial markets such as more electric aircraft (MEA), electric vehicles (EV), traction drives, and others applications where space is major concerns. Hardware prototypes are developed to prove the theoretical studies as well as the feasibility of the proposed concepts and designs of multilevel converters to meet these specifications.

1.5 Research Contributions

The contribution of the research work in this thesis constitutes the analytical studies and the development of experimental prototype to prove its feasibility in practical cases instead of proposing conceptual ideas only. The contribution mainly emphasizes on the important aspects and factors in designing multilevel converters while overcoming the problems faced in the existing topologies.

A. Advanced multilevel carrier-based sinusoidal PWM schemes:

- *Objectives:*
 - Avoid the constantly ‘turn on’ state for semiconductor devices during the under-modulation condition of the level-shifted carrier PWM.
 - Avoid the issues of EMI caused by the high switching frequency operation of phase-shifted carrier PWM when there is an increase in the number of phase-shifted carriers required for modulation.
 - Attain the advantageous properties of both level-shifted carrier PWM and phase-shifted carrier PWM.
- *Contributions:*
 - Proposed methods are explored by hybrid level-shifted carrier PWM and phase-shifted carrier PWM.
 - Harmonic characteristics and total harmonic distortion (THD) performances of the proposed hybrid SPWM schemes are mathematically evaluated and experimentally verified.
 - Proposed hybrid SPWM methods have successfully reduced the high switching frequency operations to avoid the issue of EMI while achieving comparative and even better THD performance.

B. Proposed reduced modular cell inverter topologies:

- *Objectives:*
 - Reduce the high switching frequency operation of classical multilevel flying capacitor inverter (MFCI) to enable its applicability in high power systems and to avoid the EMI issue.
 - Reduce the overall size of the converter while synthesizing higher number of output stepped voltage waveforms.
 - Reduce the amount of energy storage to allow the converter to reach its steady-state condition faster compared to the classical approach for higher output voltage levels.
 - Reduce the amount of in-rush current during the initial startup of the converters to prevent overstressing the semiconductor devices which in return increases the overall reliability.
 - Reduce the total distributed losses (conduction loss and switching loss) so that better converter efficiency can be achieved.
- *Contributions:*
 - Reduced modular cell inverters are proposed to synthesize higher output voltage stepped levels with topologically reduced component counts.
 - Laboratory prototypes are built to evaluate the performances of the proposed lightweight flying capacitor inverter (LFCI) and reduced flying capacitor inverter (RFCI) with the implementation of advanced hybrid SPWM schemes. Experimental results have proven its feasibility.
 - Comparative analysis is carried out to highlight the improvements made in the LFCI and RFCI as compared to the conventional approach.

C. Four quadrant bidirectional reduced flying capacitor rectifier:

- *Objectives:*
 - Achieve bidirectional power flow despite topologically reduced component counts in the proposed multilevel rectifier.
 - Reduce power losses and input line inductance filter size to increase the power density.
 - Maintain balanced flying capacitor voltages at the desired values at all times to increase the converter stability and reliability.
- *Contributions:*
 - Unity power factor controller incorporated with the voltage balancing control scheme is proposed.
 - Laboratory prototype of reduced flying capacitor rectifier is built to validate its feasibility of the converter design and the controller scheme using the enhanced hybrid PSC-PD-PWM scheme.
 - Dynamic conditions are evaluated experimentally as well such as stepped change in the power factor as well as the load conditions.
 - Comparative investigation and mathematical analysis are made to highlight the enhanced performances of the proposed rectifier compared to the classical multilevel flying capacitor rectifier.

D. Active neutral point clamped inverter:

- *Objectives:*
 - Investigate and address the limitations of the active neutral point clamped (ANPC) inverter because of the hybrid configuration of diode clamped and flying capacitor structure. Thus, deteriorating the output power quality.
 - Reduce common mode voltage actively since ANPC is well known for industrial drive systems to prevent premature bearing failure and avoid the EMI issue.
- *Contributions:*
 - Alternatively, new hybrid carrier-based PWM named as interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM) is proposed to further enhance the harmonic profile of the output voltage waveforms. Mathematical analysis is provided to investigate the THD performance.
 - Multiple voltage quantities enhancement (MVQE) control is proposed using the new enhanced ISC-PD-PWM scheme to achieve better voltage balancing across the dc-link capacitors and the flying capacitors. The dc-link ripples are also addressed to improve the output voltage quality.
 - New active common mode reduction (CMV) technique is proposed using the carrier-based PWM schemes especially for the ANPC inverter since those reported methods in the literatures cannot be applied directly. Comparative analysis showed that ISC-PD-PWM scheme is attractively better than the typically used classical PWM modulation scheme.
 - Hardware prototype is developed to verify the feasibility of the proposed MVQE control and the proposed CMV reduction technique using new hybrid ISC-PD-PWM scheme.

1.6 Organization of the Report

Chapter 1 gives the introduction and the motivation to carry out research on power electronic converters using multilevel approach for high power applications. The statistical results of energy demands have proven the need of high power conversion. Multilevel converters are proven technologies in the industry.

Chapter 2 gives the background on the existing multilevel topologies in the industry, the classification and literature review of respective multilevel topologies. The problems and limitations are discussed to search for the reasons that restrict multilevel to synthesize higher number of output voltage stepped waveforms.

Chapter 3 focuses mainly the multilevel modulation methods which are the principal elements in designing multilevel converters. Investigations are carried out to address the advantages and disadvantages of the classical SPWM schemes. As such, this motivates to propose new hybrid SPWM schemes so that the attractive advantages can be well retained while enhancing the converter performances.

Chapter 4 reviews the classical multilevel flying capacitor inverter (MFCI) topology and discusses the challenges faced when increasing the number of cells to synthesize higher number of output voltage levels. The harmonic characteristics of the popularly used classical phase-shifted carrier PWM (PSC-PWM) for MFCI are mathematically analyzed using the double Fourier series approach.

Chapter 5 proposes two distinct reduced modular cell inverter topologies named as lightweight flying capacitor inverter (LFCI) and reduced flying capacitor inverter

(RFCI) which has successfully overcome the limitations of the classical MFCI. Two hybrid SPWM schemes (phase-shifted carrier phase-opposition-disposition PWM – PSC-POD-PWM and phase shifted carrier phase-disposition PWM – PSC-PD-PWM) are proposed as well to enhance the voltage quality waveforms as proven mathematically and experimentally. The hardware prototype has proven the feasibility of the proposed reduced modular cell inverters in the practical applications. Comparative analysis is also performed and presented to highlight the enhanced performances.

Chapter 6 proposes a topologically reduced part-counts rectifier while retaining the four quadrant operations to enable bidirectional power flow in the systems unlike the recent proposed rectifiers. Design parameters for the proposed rectifier are theoretically expressed. Dynamic conditions are experimented to validate the feasibility of the proposed rectifier and control schemes (unity power factor control and flying capacitor voltage balancing control). The proposed rectifier greatly reduced the power semiconductor losses while achieving good input current shaping performance.

Chapter 7 addresses the common limitations faced in the active neutral point clamped (ANPC) inverter due to the hybrid structure of the diode clamped and flying capacitor topologies involving capacitors in the converter design. Challenges such as dc-link ripples for grid-connected applications, dc-link neutral point and flying capacitor voltage balancing are highlighted. Even though ANPC is industrial proven technology, but many research works are reported separately to treat the power quality issues. Hence, a multiple voltage quantities enhancement (MVQE) control is proposed to

overcome the aforementioned issues. Moreover, another new hybrid interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM) is also proposed to further enhance the performances. Active common mode reduction technique using the new ISC-PD-PWM is also presented for the well-known medium voltage ANPC drives with the comparative investigation conducted to validate the enhanced performances achieved.

Chapter 8 outlines the final conclusion of the research work up to date and the recommendations for future works are presented as well.

Chapter 2

Traditional and Recent Multilevel Inverter Topologies

Power electronic converters are classified mainly based on current source (CS) or voltage source (VS). In the early days around 1980s, the current source inverters (CSI) were popular when thyristors-based semiconductors were first developed. The CSIs are also named as load commutated inverters (LCI) in the industrials these days, which comprise mainly of GTO or IGCT in circuit. Usually, CSIs are operated under short-circuit condition using these current controlled switching devices, hence low switching frequency is required. Besides, gate driver circuitry design becomes complicated too.

In 1964, Ray E. Morgan has proven that the performance of an inverter will be more efficient for a fast switching operation where switching losses are greatly reduced through the experimented bridge chopper inverter [27]. Even though IGCT allows higher switching frequencies (up to the few kHz) than GTO, but the switching losses are considerably high. Hence, the switching frequency for IGCT is typically limited to few hundred hertz (around 500 Hz).

In mid 1990s, IGBTs become available in the markets which are designed to be open circuit voltage controlled semiconductor devices for fast switching purpose. As a result, IGBTs would be more favorable in VSI where lower switching losses, higher efficiency and higher reliability are achieved [46-48]. Moreover, VSI has low current harmonic distortion due to high switching frequency operation. VSI are proven in industrials applications (Table 1.1) due to numerous advantages, therefore multilevel VSI is the prime focus of research and will be further discussed in this chapter.

2.1 Traditional Two-Level Voltage Source Inverter

Fig. 2.1 Traditional three-phase two-level voltage source inverter (2L-VSI).

The configuration of the conventional three-phase two-level voltage source inverter as shown in Fig. 2.1 has been commonly used in the early 1960s for motor drives. The 2L-VSIs were constructed using thyristors-based switching devices during those times until the 1990s where IGBTs are used to replace the thyristors for faster switching purpose.

The topology of the three-phase 2L-VSI is simple in nature which consists only two switching devices in each phase leg. Thus, allowing the cost of implementation to be relatively low. Even though fast switching operation of up to 20 kHz can be performed with the IGBTs to reduce switching losses in 2L-VSI, but there is an implication of high stress in motor winding especially when long cable is connected between the inverter and the motor [49]. The increase in switching frequency operation causes high dV/dt (large voltage spikes) due to the characteristic impedances of cable; hence it has a detrimental impact on the motor.

In order to prevent motor performance deteriorating from those harmful spikes, filters are required to be placed at the output terminal of the inverter [50, 51]. Hence, the rule of thumb in [50] stated that the resonant frequency of the filter must be designed at least 10 times higher than the output frequency of the inverter and at most 0.5 times the switching frequency operation. According to the control theorem, the reduction of output filter size can only be achieved when the 2L-VSI operates at a higher switching frequency.

However, electromagnetic interference (EMI) becomes a major issue when the power electronic appliances are operating at a switching frequency range between 10 kHz to 30 MHz [52]. Since power electronic converters usually operate below the frequency of 10 MHz (typically around 10 kHz to 150 kHz), the EMI is spread by the conduction on the wires. Hence, conducted EMI is the key concern in the design of power converters instead of radiated EMI. Thus, EMI filter is required to suppress the conducted EMI for the 2L-VSI with 20 kHz switching frequency so that the filter size can also be minimized.

Apart from that, there is a limitation for 2L-VSI to drive high power (100 MW and above) applications due to the available voltage ratings of the semiconductor devices in the market. Based on the configuration of the 2L-VSI, each of the semiconductor devices has to support the total amount of DC voltage supply. Therefore, the design of 2L-VSI becomes complex when a number of semiconductor components are series-connected together in order to withstand high DC voltage [53, 54]. As a result, the reliability of the 2L-VSI will also be greatly affected due to the increase number of switching devices required in the circuit.

2.2 Recent Multilevel Voltage Source DC-AC Inverters

Multilevel power converters, a new breed of power electronic converters, have been developed and evolved ever since the 1980s till today. The ability to overcome the limitations and the challenges faced in the traditional 2L-VSI topology has gained favors in many industrial high power applications.

Multilevel converters synthesize the output voltage into multiple stepped levels (staircase-like) waveform; therefore, the word “multilevel” is named after. By doing so, the voltage stress across each semiconductor devices is greatly reduced. When higher number of output voltage stepped levels is increased, lesser voltage harmonic is achieved. Thus, the size of the output filter can be further reduced or even eliminated. On top of that, good output power quality can be achieved even with much lower switching frequency (less than 10 kHz). Hence, the problems of EMI and high switching losses can be avoided.

These numerous advantages have drawn a great interest and attention in the research over the last decade. Despite multilevel converters considered as proven mature technologies in many industrials today (Table 1.1), currently there are still many challenges encountered such as the unbalance of capacitor voltages when higher number of output voltage stepped levels are intended to be achieved. Therefore, an investigation of the existing multilevel topologies used in industrials will be discussed in the following subsections of this chapter. The advantages along with the drawbacks of each multilevel converter topology will be elaborated as well. These will serve as a clearer vision to remain focus in the research area and alternative solutions can be proposed to improve the performance of multilevel converters.

2.2.1 Multilevel Diode-Clamped Inverter

Fig. 2.2 Three-phase multilevel diode clamped inverter.

Three-level neutral point clamped inverter (3L-NPC) was the originated of multilevel power converter in 1981 by Akira Nabae *et al* [28]. The expansion of 3L-NPC has been discussed in [55] and the first 10 kVA four-level inverter prototypes have been experimented in [56].

Based on the fundamental 3L-NPC, the three-level output voltage stepped waveform is synthesized through the two diodes clamped to the middle of two dc-link capacitors. The middle connection of dc-link capacitors is referred as neutral point and also served as the output phase voltage reference point. Since the output voltage waveform is synthesized from the dc-link capacitor voltages, the number of diode elements required to be clamped will increase when higher number of output voltage levels is desired. Therefore, the topology of 3L-NPC evolves to multilevel diode clamped inverter (MDCI).

The number of switches i and clamping diodes D required for m -level (mL) output phase voltage level of MDCI can be determined with the following equations (2.1) and (2.2) respectively.

$$i_{\text{switches(MDCI)}} = 2[(mL) - 1] \quad (2.1)$$

$$D_{\text{diodes(MDCI)}} = 2[(mL) - 2] \quad (2.2)$$

While the number of dc-link capacitors Q needed for mL -MDCI can be known based on the following equation (2.3).

$$Q_{\text{capacitors(MDCI)}} = (mL) - 1 \quad (2.3)$$

Since there are no passive elements required for MDCI (excluding the dc-link capacitors), therefore only conduction losses and switching losses are accounted for the clamped diodes and switches in the converter.

When higher number of output voltage stepped levels is desired, higher number of capacitors will be needed in the dc-link. Theoretically, the dc voltage source should be distributed equally among the number of dc-link capacitors. However, in practical cases, the parameters of both active and passive elements can never be identically same. Due to that, an unbalanced condition is occurred in the dc-link capacitor voltages. Besides, the amount of charging and discharging current flow through the diodes clamped between each pair of dc-link capacitors is unequal because of the switching strategy used [55].

The unbalanced condition of dc-link capacitor voltages makes the MDCI topology become disadvantageous and challenging to achieve higher number of output phase voltage levels. Several methods have been proposed to overcome the dc-link unbalanced condition based on active control [57], active balancing circuit [58-60] or passive RLC technique [61, 62].

Even though many research works have contributed to resolve the unbalanced condition for three-level to five-level MDCI, [57] makes the control a little more complex or more losses are incurred from the active balancing circuit [58-60] and passive RLC technique [61, 62]. Additional costs are also required to implement these proposed methods for higher number of output phase voltage levels.

These factors could be the reason that MDCI with more than three-level output phase voltage is still not available in any of the industrial markets yet. Currently, 3L-NPC is the only MDCI topology popularly available in the market. This is due to its simplicity in design, low costs and high reliability as compared other multilevel topologies. The 3L-NPC is widely used for industrial medium power motor drives as well as power inverters for wind and solar systems nowadays.

2.2.2 Multilevel Flying Capacitor Inverter

Fig. 2.3 Three-phase n -cell multilevel flying capacitor inverter.

Multilevel flying capacitor inverter (MFCI) as shown in Fig. 2.3 was named as versatile multilevel commutation cell originally in 1992 by Meynard *et al* [63]. MFCI offers an alternative approach for multilevel conversion. Based on its origin name, the topology of MFCI is constructed with multiple cells concept. By increasing the number of cells in MFCI, higher number of output phase voltage levels can be obtained as well. The design does not only allow the topology to be versatile, but also achieved the objective of multilevel approach with the properties of voltage sharing among the switches.

MFCI has a similar structure as MDCI, where capacitors are clamped between the switches instead of diode elements. Hence, each cell in MFCI consists of two semiconductor devices and a capacitor clamped. The total number of switches i and capacitors p required for mL -MFCI can be determined based on the number of cells (n_{cells}) implemented as shown in following equations (2.4) and (2.5) respectively.

$$i_{\text{switches(MFCI)}} = n_{\text{cells}} \times 2 \quad (2.4)$$

$$p_{\text{capacitors(MFCI)}} = n_{\text{cells}} - 1 \quad (2.5)$$

Based on the topology of MFCI as shown in Fig. 2.3, the synthesized output phase voltage levels are not dependent of the dc-link capacitors. Hence, MFCI unlike the MDCI will not face the same challenge of unbalanced dc-link capacitor voltages when the higher number of output phase voltage levels is desired.

However, more capacitors are needed for higher mL -MFCI. Capacitors usually will lead large inrush current during the start-up period. Therefore, pre-charge circuits are needed to avoid high current during the transient period which may damage the power rating of the semiconductor devices [64]. In order to minimize the current from overstressing the switches during initial operation, the common practice in any converter is to place a resistor in between the DC source and the dc-link capacitors. High losses may be experienced during this process, thus a switch is also connected in parallel to the pre-charge resistor and will be turned on after pre-charging. So excess losses can now be avoided during normal operation by shorting the pre-charge resistor through the switch.

Besides that, capacitors are passive element which also serves as energy storage devices. The amount of energy stored in a capacitor will affect the voltage quality across it. The analytical and experimental results obtained in [65] have proven that higher carrier frequency can reduce or minimize the capacity of the flying capacitors,

and low voltage ripples can be achieved. However, high carrier frequency will limit MFCI for high power conversion and also lead to the issues of EMI.

On top of that, large amount of energy stored may affect the losses of the MFCI converter in addition to the switching and conduction losses of the switches. Reliability of capacitors especially electrolytic capacitors required for higher power rating is another major concern in the MFCI converter. Additionally, the space takes up by the number of flying capacitor will also increase as compared to the size of diodes clamped in the MDCI.

As a result, these mentioned factors are of great disadvantages in designing higher mL -MFCI for industry use. Therefore, MFCI is currently attractive for high speed drives and those applications that require low current ripples. MFCI is only available in ALSTOM industrial based on Table 1.1.

2.2.3 Multilevel Cascaded H-Bridge Inverter

Fig. 2.4 Three-phase n -cell multilevel cascaded h-bridge inverter.

An alternative multilevel approach was proposed by Fang Zheng Peng *et al* [66] in 1996 which used the similar concept of modularity as MFCI; hence flexibility for this multilevel converter can be allowed. The multilevel converter was named as multilevel cascaded H-bridge inverter (MCHB) based on the topology configuration shown in Fig. 2.4.

Each cell comprises of four switches to form a conventional full-bridge (H-bridge) VSI and an isolated dc capacitor. Higher output phase voltage levels can be achieved by cascading more cells together. The staircase-like voltage waveforms can only be synthesized using square pulses instead of chopped waveforms (Pulse-Width Modulation – PWM) which are commonly used in other multilevel converters. Hence, this experience higher conduction losses in each switching device.

MCHB will be advantageous when higher number of output phase voltage levels is attained (more than 11-level), the output voltage waveform will appear closer to a pure sinusoidal-like waveform. Thus, lower harmonic distortions can be achieved and the output filter size can also be reduced. However, the total number of switches i and capacitors p required will also be increased depending on the number of cells required based on the following equations (2.6) and (2.7) respectively.

$$i_{\text{switches(MCHB)}} = n_{\text{cells}} \times 4 \quad (2.6)$$

$$P_{\text{capacitors(MCHB)}} = n_{\text{cells}} \quad (2.7)$$

MCHB does not have the problem of unbalanced capacitor voltages like those MDCI and also does not require excessive flying capacitors like MFCI to achieve multilevel conversion. Nevertheless, MCHB experiences large circulating current in each cell due to its configuration. On top of that, MCHB also requires isolated dc sources to supply across the dc capacitors in each cell. This makes MCHB very disadvantageous, hence alternative solution like phase-shifted transformer is required to provide isolated dc voltages for each cell.

Phase-shifted transformers are usually hard to manufacture which result a more costly solution to be implemented. Besides that, high losses and heat dissipated are incurred from this bulky transformer when the load is not operated at its rated power. Even though phase-shifted transformer takes up large volume and space of the converter, but many industrials are using MCHB to achieve higher output phase voltage levels (currently 25-level is the highest as listed in Table 1.1) for high power motor drives.

2.2.4 Modular Multilevel Inverter

Fig. 2.5 Three-phase n -cell modular multilevel inverter.

Modular multilevel inverter (M^2I) as shown in Fig. 2.5 was introduced in 2003 by Marquardt *et al* [67, 68] and the prototype of 2MW power rating with 17L output voltage was experimented and verified [69]. The configuration of M^2I is similar to that of MCHB, the only difference between them is the placement of DC source. Based on Fig. 2.5, M^2I only requires a single DC source unlike the MCHB with many isolated DC sources. Hence, M^2I is highly suitable for HVDC systems.

Each cell consists of two semiconductor devices and a capacitor which forms a single phase half-bridge VSI (chopper cell). The configuration of each cell can also be done with full-bridge VSI (bridge cell) same as those used in MCHB modular cell. Hence, the number of switches i for both chopper cell and bridge cell configuration can be determined based on the number of cells with the following equations (2.8) and (2.9) respectively.

$$i_{\text{switches}(\text{M}^2\text{I-Chopper})} = n_{\text{cells}} \times 2 \quad (2.8)$$

$$i_{\text{switches}(\text{M}^2\text{I-Bridge})} = n_{\text{cells}} \times 4 \quad (2.9)$$

While the capacitors p required for both chopper cell and bridge cell configurations can be known based on the following equation (2.10).

$$p_{\text{capacitors}(\text{M}^2\text{I})} = n_{\text{cells}} \quad (2.10)$$

Bulky phase-shifted transformer is not required, but M²I experiences larger circulating current than in MCHB. Therefore, single coupled or center-tapped inductor is required for each phase-leg, connected between the positive and negative dc rail connected modular cells [70, 71] as shown in Fig. 2.5.

M²I would offer a more interesting and attractive for higher power applications as compared to the MCHB, but the implementation and design of either single coupled or center-tapped inductor would make M²I a bit complex and tedious. As listed in the Table 1.1, the 9L-M²I was first commissioned by SIEMENS industry for the HVDC PLUS transmission system. The M²I converters are also commercialized for the HVDC systems by other industries like ABB (HVDC Light) and ALSTOM (HVDC MaxSine).

2.2.5 Multilevel Active Neutral Point Clamped Inverter

Fig. 2.6 Three-phase n -cell multilevel active neutral point clamped inverter.

An alternative multilevel inverter as shown in Fig. 2.6 has been designed in 2005 by Steffen Bernet *et al* [72, 73] and was named as active neutral point clamped converter (ANPC) initially. The origin design was proposed to overcome the unequal loss distribution among the switches in 3L-NPC.

In latter, the origin was then expanded with multiple cells and multilevel ANPC is developed thereafter [74]. Higher number of output phase voltage levels can be achieved with addition commutation cells like those in MFCI. Therefore, each cell comprises of two switches and a capacitor clamped.

The total number of switches i and capacitors p in each phase-leg can be known based on the number of cells implemented with the following equations (2.11) and (2.12) respectively.

$$i_{\text{switches(ANPC)}} = 6 + (n_{\text{cells}} \times 2) \quad (2.11)$$

$$p_{\text{capacitors(ANPC)}} = n_{\text{cells}} \quad (2.12)$$

The configuration of ANPC as shown in Fig. 2.6 is basically the combination of both MDCI and MFCI. As a result, the multilevel ANPC has kept the advantageous characteristics of both MDCI and MFCI. This shows that ANPC will not be affected by the dc-link capacitors when the number of output phase voltage levels is increased. While the modularity of commutation cells allows the flexibility of ANPC in extending to higher number of voltage levels without encountering the unbalanced dc-link condition.

ANPC in this case does not require any bulky phase-shifted transformer, multiple isolated dc sources or any balancing circuit for dc-link capacitor voltages. Hence, ANPC offers an attractive method for medium-high industrial motor drives as compared to the other previous mentioned multilevel converters. A back-to-back configuration of 5L-ANPC is available in the current industrial market, ABB, for regenerative motor drives as listed in Table 1.1

2.3 Multilevel Applications and Future Trends

Multilevel converter topologies are well-known for its applicability in medium to high power drives and are popularly used for the industrial motor drives application as shown in Table 1.1. Moreover, many academia research works have also explored the applications of these multilevel converters in other areas such as transportation, renewable energy, utilities grid and even for low power Class D amplifier as shown in Table 2.1 [75].

These show that multilevel converters play an important role in our daily life applications and it will be the future trends of power electronic converters. Since the cost of semiconductor devices are depreciating, more industrials are investing also a

TABLE 2.1
HIGH-PERFORMANCE MULTILEVEL CONVERTER APPLICATIONS BASED ON TOPOLOGY [75]

Application		Multilevel Topology		
		MDCI/ANPC	MCHB	MFCI
Transportation	Marine Propulsion	[81], [93], [200], [201]	[81], [201]	[201]
	Train Traction	[43], [202]-[206]	[61], [115], [116], [202], [205]-[208]	[209], [210]
	Automotive	[211]	[212]-[214]	[215]-[218]
Renewable Energy	Solar Photovoltaic	[121], [181]-[185]	[181], [186]-[193]	[181]
	Wind Power	[165], [194]-[198]	[199]	-
	Hydro Power	[224]	-	-
Utilities Grid	FACTS	[225]	[117], [225]-[227]	[225]
	STATCOM	[228]-[230]	[55], [62], [192], [228], [231]-[234]	-
	UPFC/UPQC/DVR	[245]-[247]	[245], [248], [249]	[250]
	HVDC	[175]	[55], [56], [180]	-
	Active Filters	[235]-[239]	[240]-[242]	[243], [244]
Industrials/Commercial	Pumps/Motors	[219], [220]	-	-
Small Signals	Class D Amplifier	-	[221]-[223]	-

Note: The information in this Table 2.1 is extracted from [75], hence the numbering here is referred to the references in [75].

lot in developing new multilevel converters for other possible areas that are not listed in Table 2.1 such as more electric aircraft (MEA), heat ventilation and air conditioning (HVAC) and others.

With the involvement of markets, the cost of implementations is always the prime concern, which explains that why the some of the existing multilevel converters like MDCI and MFCI are not developed for higher mL output voltage due to the total number of components required as shown in Fig. 2.7. Therefore, only multilevel topologies like MCHB, MMI and ANPC are developed with more than 5L output phase voltages as shown in Table 1.1. Even though many academia research works have contributed alternative solutions to overcome the limitations of these existing multilevel converters to achieve higher mL output voltages, but these proposed solutions are still not very welcome in the industry. Thus, recently many research and development works are motivated to focus on designing new multilevel converters with reduced number of component counts to achieve better power quality more efficiently.

Fig. 2.7 Comparison of total component counts based on respective multilevel topologies.

Note: The total number of components per phase-leg presented in Fig. 2.7 includes dc-link capacitors for MDCI, MFCI, ANPC and coupled inductors for MMI

Fig. 2.8 The history of power electronics.

The advantages of reducing the amount of components needed do not only benefits for the industrial interests, but also helps to increase the global reliability of the converters. Low maintainability is required since lesser component counts are used in the multilevel converters. Furthermore, lower losses are incurred during the power conversion process; hence higher energy efficiency can be achieved. On top of that, reducing component counts enable the converters to be lighter weight and beneficial for many applications with space constraint such as MEAs, wind turbines, solar PV grid-connected systems and HVAC systems.

As a result, the developing trends in new multilevel converters in the near future will be involving cost, size, weight, losses and power quality [76]. It is factually known that the advancement of multilevel converter designs is closely co-related with the development of power electronic devices as shown in Fig. 2.8. As such, new electronic switching devices based on silicon carbide (SiC) and gallium nitride (GaN) shall be the upcoming technologies to support higher switching frequencies operation as well as sustain higher current handling capability. With that, higher power density converter can be achieved. These will be served as guidelines in optimizing the design of power electronic converters for both research and development works.

Chapter 3

Multilevel Modulation Methods

The design and implementation of modulation techniques are relevantly important with the growth of multilevel converter topologies. Modulation schemes are applied to synthesize a good output voltage quality while allowing better control over both magnitude and frequency of the output voltage at the same time.

Multilevel modulation methods presented in Fig. 3.1 are basically classified based on (i) Carrier-Based Modulation (CBM) and (ii) Space Vector Modulation (SVM). Both of these modulations belong to the same family of Pulse-Width Modulation (PWM). Both methods seem to be very different from each other, but there are no clear cut superior performances proven to distinguish between one another. Both methods do have own advantages and drawbacks.

SVM can generate additional switching states whereby CBM cannot, hence higher degree of freedom is provided. Many SVM 2D and 3D algorithms have been proposed for m -level and up to four-leg multilevel converters. However, any of SVM methods presented would still require to go through the three steps process as mentioned in [75] (i) vector selection (ii) duty cycle computation and lastly (iii) sequence of vectors generated. A simplified method has been proposed in [77], using the single-phase modulator (1DM) technique which can be extended for any number of output phase voltage levels and phase-legs. Equivalent performances have been realized by 1DM as compared to other conventional SVM methods [78]. But, lower computational cost is achieved for 1DM only when compared to multi-dimensional SVM (M-SVM).

Since SVM is heavily dependent on the computational calculations, hence there is no need to increase the number of carriers for higher m -level multilevel converters unlike CBM. Nevertheless, SVM except Nearest Vector Modulation in this case is not applicable for high power applications due to the high switching frequencies operation required.

Despite of many researches explored in the SVM methods, but CBM is more favorable in the industrials. Partly could be due to the computational methods required in SVM which must be programmed into the low-cost digital processors to generate the gating signals. Thus, this process makes SVM more complex. The gating signals of CBM could be generated by either programmed digital processors (results more complicated than SVM) or simplest way is through logic gates and analog comparators.

Comparative studies between both SVM and CBM methods have been done and evaluated in [79] and [80] for NPC and MCHB respectively, the results showed that the switching losses are comparable among the two methods. This results a clearer choice between CBM and SVM for the industrial applications.

Even though carrier-based sinusoidal PWM (SPWM) usually operates at high switching frequencies (above 1 kHz), but SPWM could go for much lower switching frequency (about 500 Hz) to meet the high power application requirements. The area between SPWM and hybrid PWM are not fully explored yet. Hence, the problems and advantages of each traditional SPWM schemes will be elaborated in this chapter. New hybrid carrier-based SPWMs are proposed and analyzed in the following chapters. Better performances and power quality are achieved and verified experimentally.

Fig. 3.1 Classification of multilevel modulation methods.

3.1 Carrier-Based Sinusoidal Pulse-Width Modulation Methods

Sinusoidal pulse-width modulation (SPWM) is proven to be the simplest method which can be achieved through comparator circuits directly without any tedious effort needed for programming the digital processors. Hence, SPWM is widely used not only in many research purposes but also in the industrial applications.

Comparative studies between the existing SPWM methods will be carried out in this section. On top of that, the limitation and problems of SPWM for multilevel converter topologies will also be discussed. These have further motivated the interest in exploring and analyzing the new proposed SPWM methods which will be explained in the following chapters with the respective multilevel converters.

3.1.1 Principle Operation of SPWM Methods

The gating signals of SPWM are generally achieved by comparing the reference sinusoidal wave with the triangular carriers. When the reference signal is greater than the gradient of the triangular carrier, the switching pulse will be at ‘turn on’ state; and vice versa when the reference signal is smaller than the gradient of the carrier, the switching pulses will be at ‘turn off’ state.

Hence, the duty ratio of the switching pulse is varied according to the reference sinusoidal signal $\sin(\omega t)$ which can be observed in the Fig. 3.2. The following equation (3.1) expressed the state of switching pulse during the modulation period.

$$S_x(t) = \begin{cases} 1 & \text{if } \sin(\omega t) > \text{tri}(t) \\ 0 & \text{if } \sin(\omega t) < \text{tri}(t) \end{cases} \quad (3.1)$$

Fig. 3.2 Gating signal of SPWM.

For any SPWM modulation techniques used, the number of carriers ($n_{carrier}$) required can be determined with the following equation (3.2) based on the m -level (mL) output phase voltage levels desired to synthesize.

$$n_{carrier} = (mL) - 1 \quad (3.2)$$

According to the equation (3.2), the $n_{carrier}$ needed for SPWM will be increased linearly with the number of output phase voltage levels produced. However, the increase of $n_{carrier}$ complicates the analog circuit designs for higher mL multilevel converters especially when more than seven-level (7L) output phase voltages are synthesized. Besides that, the overall switching frequency of the multilevel converters will also be affected by the $n_{carrier}$ implemented depending on the inherent characteristics of the SPWM methods used.

3.1.2 Limitation of SPWM in Multilevel Converters

Fig. 3.3 Limitation of modulation index (Mx) vs mL -output phase voltage.

Regardless of any SPWM techniques used in the multilevel converters, it should be noted that the modulation range is being restricted when higher mL output phase voltage levels are produced. It is relatively important as it affects the degree of freedom in controlling the amplitude of output voltage. Modulation index is usually referred to modulation amplitude ratio (Mx) as defined in the following equation (3.3).

$$M_x = \frac{\hat{V}_{control} (\text{Peak Amplitude of Reference Sinusoidal Signal})}{\hat{V}_{tri} (\text{Peak Amplitude of Carrier Signal})} \quad (3.3)$$

Fig. 3.3 illustrates the limitation of Mx and the degree of freedom in control with respect to the output voltage levels. The controllable range of Mx ratio becomes smaller between 0.9 Mx to 1.0 Mx when more than 21-level output phase voltage is being synthesized. This constraint controllability is undesirable for many applications. When Mx falls below the minimum required index for the respective voltage levels, SPWM is considered as under-modulation. As a consequence, the output phase voltage of the converter will become $[(mL)-2]$ voltage levels with higher harmonic distortion and may cause undesirable large dV/dt and dI/dt during the operation.

3.1.3 Performances of Level-Shifted PWM and Phase-Shifted PWM

The two common modulation strategies under SPWM are the level-shifted carrier PWM (LSC-PWM) and phase-shifted carrier PWM (PSC-PWM) as shown in Fig. 3.1. There are three types of carrier disposition PWM strategies that are further classified under LSC-PWM, namely the phase-disposition PWM (PD-PWM) (Fig. 3.4(a)), phase-opposition-disposition (POD-PWM) (Fig. 3.4(b)) and alternative phase-opposition-disposition (APOD-PWM) (Fig. 3.4(c)).

Fig. 3.4 Carrier disposition of LSC-PWM.

(a) PD-PWM. (b) POD-PWM. (c) APOD-PWM.

A comparison between PD-PWM, POD-PWM and APOD-PWM has been analyzed based on any number of output phase voltage levels in [81], and the detailed analytical studies of harmonic performances of LSC-PWM and PSC-PWM for MDCI and MCHB are also evaluated respectively in [82]. Both have proven that PD-PWM has superior performance in terms of lower harmonic components. Because of that, the LSC-PWM is sometimes directly referred as the popularly implemented PD-PWM.

However, one can observe that the carrier harmonics of LSC-PWM will always be at the same harmonic order despite of any $n_{carrier}$ used for comparing. Meanwhile, the carrier harmonics of PSC-PWM will be shifted accordingly depending on the $n_{carrier}$ and the carrier frequency. The harmonic characteristics of PSC-PWM will be proven again subsequently in the following chapter.

The amplitude of carrier harmonics is often an important factor to be taken note of, since the conducted EMI is concerned with the switching frequency operation between 10 kHz to 20 kHz which is typically used in power electronic converters. In this case, the conducted EMI for LSC-PWM methods applied to high power applications (switching frequency range between 500 Hz to 700 Hz) will not be a major concern.

Despite of its superior performances as compared to the other SPWM schemes, there is a concerning issue when LSC-PWM is performed under-modulation condition. This problem can be highlighted using the gating signals obtained from the LSC-PWM for the five-level output phase voltage (four triangular carriers required for modulation) as shown in Fig. 3.5. Two conditions (i) 0.9 Mx (normal operation) and (ii) 0.3 Mx (under-modulation) are considered for clearer illustration.

Fig. 3.5 Performances of LSC-PWM – Five-level modulation.
(a) Modulation index (M_x) = 0.9. (b) Modulation index (M_x) = 0.3.

Based on Fig. 3.3 shown earlier on, the normal operation range of M_x to synthesize five-level output phase voltage should fall between $0.5 M_x$ and $1.0 M_x$. Therefore, Fig. 3.5(a) shows the gating signals generated for normal operation. The under-modulation condition in Fig. 3.5(b) shows that the top gating signal (GS-1) will be at ‘turn off’ state all the way while the bottom gating signal (GS-4) will be at ‘turn on’ state all the way.

The constantly switch on state of GS-4 in the LSC-PWM under-modulation condition will bring undesirable harm to the semiconductor devices (especially the switches). As a result, the electronic devices will breakdown easily due to the over voltage and over current stresses. Thus, this affects the overall reliability of the multilevel converters.

On the other hand, PSC-PWM will not encounter the same problem as LSC-PWM during under-modulation condition as proven in Fig. 3.6. It can be observed that all the gating signals are still generated even in the event of under-modulation condition. Thus, higher reliability is achievable with PSC-PWM as compared to LSC-PWM.

Besides that, the gating signals generated from PSC-PWM are always symmetrical to each other be it in normal operation or under-modulation condition. Hence, stress and loss are equally distributed among the semiconductor devices [80]. These evidences have strongly driven the industrials to choose PSC-PWM over LSC-PWM for many multilevel converter topologies except 3L-NPC or family of mL -MDCI. Therefore, LSC-PWM is commonly used for those diode-clamped related multilevel topologies.

Fig. 3.6 Performances of PSC-PWM – Five-level modulation.
(a) Modulation index (M_x) = 0.9. (b) Modulation index (M_x) = 0.3.

3.2 Advanced Hybrid Sinusoidal Pulse-Width Modulation

LSC-PWM is known for its superior harmonic performance. Most importantly, the carrier harmonic components in LSC-PWM are not shifted despite of an increase in the $n_{carrier}$ utilized. Thus, conducted EMI will not be greatly affected in any high power applications due to its described carrier harmonic characteristics. But, a major problem is concerned when LSC-PWM is performed in the under-modulation condition.

While PSC-PWM is known for generating symmetrical gating signals. Thus, stress and loss are equally distributed. On top of that, the constantly ‘turn on’ state circumstance during under-modulation can avoided. However, the carrier and sideband harmonics will be shifted when there is an increase in $n_{carrier}$. The conducted EMI is likely to occur when higher $n_{carrier}$ implemented for modulation in this case. If EMI is under control, the shift of carrier harmonics in PSC-PWM can help to reduce the output filter size due to the resonant frequency (ω_f) of the filter as expressed in equation (3.4). This explains the interest of implementing PSC-PWM in the many industrial applications.

$$\omega_f = \frac{1}{\sqrt{L_{filter} C_{filter}}} \quad (3.4)$$

A better understanding of LSC-PWM and PSC-PWM through the study in the respective advantages and drawbacks has motivated to design a new hybrid SPWM schemes. The objective is to keep the advantageous properties of both LSC-PWM and PSC-PWM so that the optimum performance can be achieved. Therefore, new hybrid SPWM schemes are proposed in the following chapters with the detailed analytical studies verified against the experimental results.

Chapter 4

Review of Multilevel Flying Capacitor Inverter

Among the multilevel converter topologies presented, MFCI is one of the attractive classical topology in the early days. It was the first design of multilevel topologies with flexibility in extending for higher mL output voltage using multi-cell concepts. MFCI is a capacitor clamped design, hence it does not have any dc-link voltage balancing problem faced in MDCI. Besides that, no bulky phase-shifted transformer is required since it is a single-dc link configured converter unlike the MCHB.

The circuit structure of MFCI as shown in Fig. 2.3 is not restricted to any SPWM modulations for synthesizing the output stepped voltage waveforms. Thus, PSC-PWM is still popularly chosen over LSC-PWM due to the under-modulation problems. Besides, PSC-PWM can provide an equal voltage and current stresses among the semiconductor devices due to symmetrical duty ratio of the switching pulses [80]. The symmetrical duty ratio property of PSC-PWM provides the flying capacitor voltages with self-balancing properties.

However, when more than four cells (more than five-level output phase voltage) are implemented in the MFCI, the increase in flying capacitors will lead to larger inrush current during the pre-charging process. Moreover, longer time is also needed for the MFCI to reach the steady state due to the large energy storage in these flying capacitors.

Self-precharging technique has been proposed in [64] so that the flying capacitors can be charged to the desired voltage values through the modification of the modulation strategy. But the self-precharging method is only applicable for three-level and even-level modulations only. The flying capacitor voltages will be unbalanced when this technique is implemented for the odd-level modulations. In all cases, the unbalanced condition is trivial for the three-level modulation. In latter, the authors have mentioned that simple booster filter would still be required on top of the self-precharging technique for higher mL output voltage [83].

Therefore, simple pre-charging of these flying capacitors can be achieved easily without the complicated needs to modify the PSC-PWM switching techniques. This natural balancing technique is studied in the earlier days by the originated authors of MFCI (Meynard *et al*). Additionally, the implementation of simple booster filter can provide fast and dynamic response for balancing the flying capacitor voltages [84, 85].

The 2-cell 3L-MFCI and 3-cell 4L-MFCI have been successfully developed into a commercial product by ALSTOM (as shown in Table 1.1) in the 1990s with the simple booster filter included. MFCI is used as input chopper for the T13 locomotive for France, Belgium and Luxembourg; and also applicable commercially for medium-voltage drives [86].

Thus, the principle operations of conventional 3L (2-cell), 4L (3-cell) and 7L (6-cell) MFCI based on PSC-PWM modulation methods will be discussed in the following subsections of this chapter. Besides that, the harmonic performance of PSC-PWM is analyzed as well as summarizing the characteristics of classical MFCI in general forms.

4.1 Operating Principles of 2-Cell 3L-MFCI

Fig. 4.1 Schematic of three-phase 2-cell 3L multilevel flying capacitor inverter topology.

Conventionally, even till today, PSC-PWM is the most favorable SPWM used in MFCI to synthesize the output stepped voltage waveforms. In order to achieve the three-level output phase voltage, MFCI requires two cells which consists a number of four switching devices (S_{x1} , S_{x2} , S_{x2}' and S_{x1}') and a capacitor (C_{x1}) clamped in each phase-leg where x is referred to phase a , b or c in Fig. 4.1. A total number of twelve switching devices and three flying capacitors are required in a three-phase system.

Since four switching devices are utilized in each phase, thus two triangular carriers are required for the PSC-PWM scheme. The three-phase output voltage waveforms are synthesized by comparing the two triangular carriers with 180° phase-shifted apart against the three reference sinusoidal signals with 120° phase-shifted as shown in the Fig. 4.2. By doing so, the switching pulses generated with respect to Ref A signal are shown in Fig. 4.2. Similar switching pulses of Fig. 4.2 for phase-leg B and C are generated with 120° and 240° phase-shifted respectively following the phase-shifted of Ref B and Ref C.

Fig. 4.2 PSC-PWM for three-phase 2-cell 3L-MFCI.

The switching pulses Sp-A1 and Sp-A2 are modulated to drive the top two semiconductor devices S_{a1} and S_{a2} in phase-leg A respectively. Based on multilevel approach, complimentary switching signals are required to prevent short-circuited voltage across the flying capacitors and the voltage source during the normal converter operation. Therefore, the complimented switching pulses of Sp-A1 and Sp-A2 can be achieved using simple digital inverter (NOT gate) or small analog op-amp circuit. Thus, the inverted signals of Sp-A1 and Sp-A2 will be used to drive the bottom two switching devices S_{a1}' and S_{a2}' of phase-leg A respectively. It is similarly applied for the switching devices in phase-leg B and C.

In this case, since two triangular carriers are used for PSC-PWM modulation, there will be a combination of $2^2 = 4$ switching states ('00' to '11') created as summarized in the Table 4.1. The four switching states can also be observed from the generated switching pulses Sp-A1 and Sp-A2 in Fig. 4.2(b). Among them, two switching states are generated for the zero output voltage level. As a result, a three-level output phase voltage waveform is being synthesized.

TABLE 4.1
2-CELL 3L-MFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States		Charging/Discharging States of Capacitors	Phase Leg xn Voltage
	S_{x1}	S_{x2}	C_{x1}	V_{xn}
1	1	1		$+V_{dc}/2$
2	1	0	+	0
3	0	1	-	
4	0	0		$-V_{dc}/2$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while '■' represents neither states.

Apart from that, these redundant switching states produced from the PSC-PWM allow the MFCI to have a self-balancing capability, where equal amount of charging and discharging current can be flown through these flying capacitors. Thus, unbalanced voltage condition in the 3L-MFCI is trivial. During the steady-state and balanced voltage condition, the capacitor voltages of C_{a1} , C_{b1} and C_{c1} in Fig. 4.1 will be equal to half the dc-link voltage ($1/2 V_{dc}$). The operation modes of the 2-cell 3L-MFCI under PSC-PWM scheme can be observed clearly in Fig. 4.3.

Fig. 4.3 Operation modes of 2-cell 3L-MFCI – PSC-PWM.

According to the switching states in Table 4.1 and the operation modes shown in the Fig. 4.3, the three output phase voltage levels of V_{xn} (measured across the terminal a , b or c with respect to terminal n in Fig. 4.1) are obtained at $+V_{dc}/2$, $0V$ and $-V_{dc}/2$. The three-level output phase voltages are achieved according to the following conditions:

- 1) State 1 – The current flows through the path from the positive DC rail and the terminals a , b and c via the top two switches (S_{x1} and S_{x2}) at ‘on’ states. Hence, the voltage level of $+V_{dc}/2$ is achieved. During this state, none of the capacitors (C_{x1}) is in the charging or discharging modes.
- 2) State 2 – When the switch S_{x1} is ‘on’ and the switch S_{x2} is ‘off’, the current flows through the path from the positive DC rail to the terminals a , b and c via switch S_{x1} , capacitor C_{x1} and switch S_{x2}' . Therefore, there will be $0V$ across the terminal n and terminals a , b and c . The capacitor C_{x1} is in the charging mode during this state ‘10’.
- 3) State 3 – The current flows through the path from the negative DC rail and the terminals a , b and c via switch S_{x1}' , capacitor C_{x1} and switch S_{x2} to obtain the $0V$ voltage level. During this state ‘01’, the capacitor C_{x1} is in discharging mode.
- 4) State 4 – The current flows through from the negative DC rail to terminal a , b and c via the turned on bottom two switches (S_{x1}' and S_{x2}'). Thus, the voltage level of $-V_{dc}/2$ is obtained. It should also be noted that none of the capacitors C_{x1} is in the charging or discharging modes during this state.

Fig. 4.4 Simulated results of 2-cell 3L-MFCI with PSC-PWM modulation.
(a) Output phase voltages. (b) Output line-to-line voltages.

The simulated results of output phase voltages and output line-to-line voltages for the 2-cell 3L-MFCI are shown in Figs. 4.4(a) and 4.4(b) respectively. The output phase voltages are synthesized with the three stepped levels at $+V_{dc}/2$ (150V), 0V and $-V_{dc}/2$ (-150V). While the output line-to-line voltages are measured between the two phases, hence five-level stepped voltages are achieved as shown in Fig. 4.4(b).

4.2 Operating Principles of 3-Cell 4L-MFCI

Fig. 4.5 Schematic of three-phase 3-cell 4L multilevel flying capacitor inverter topology.

A 3-cell MFCI can achieve a four-level output stepped phase voltage waveforms based on the PSC-PWM methods. Each phase-leg of 3-cell 4L-MFCI consists of six switches (S_{x1} , S_{x2} , S_{x3} , S_{x3}' , S_{x2}' and S_{x1}') and two capacitors clamped (C_{x1} and C_{x2}) as shown in Fig. 4.5. Hence, the three-phase system requires a total number of eighteen switches and six flying capacitors.

Since there are six switches in each phase-leg, the semiconductor devices S_{x1}' , S_{x2}' and S_{x3}' are the complementary switches of S_{x1} , S_{x2} and S_{x3} respectively. So, three triangular carriers are needed for PSC-PWM modulation in order to synthesize the four-level output phase voltages. The carriers are 120° phase-shifted between one another in this case as shown in Fig. 4.6. While the switching pulses shown in Fig. 4.6 are modulated with respect to the Ref A signal. The Sp-A1, Sp-A2 and Sp-A3 in the Fig. 4.6 are used for driving the switches S_{x1} , S_{x2} and S_{x3} respectively while the inverted switching pulses are applied to the respective complimentary switches.

Fig. 4.6 PSC-PWM for three-phase 3-cell 4L-MFCI.

A combination of $2^3 = 8$ switching states from '000' to '111' is created from the three phase-shifted triangular carriers used in the PSC-PWM scheme, which can be observed from the generated Sp-A1, Sp-A2 and Sp-A3 in Fig. 4.6. These eight switching states as listed in the Table 4.2 will affect the charging and discharging states of the capacitors. Thus, the voltage across the capacitors C_{x1} and C_{x2} of Fig. 4.5 must be maintained at $1/3 V_{dc}$ and $2/3 V_{dc}$ respectively during the steady-state condition.

The charging and discharging states of the two capacitors C_{x1} and C_{x2} can be understand better based on the current flow according to the operation modes as shown in Fig. 4.7. Hence, the four-level output phase voltage stepped waveforms with respect to the neutral terminal n are synthesized correspondingly at $+V_{dc}/2$, $+V_{dc}/6$, $-V_{dc}/6$ and $-V_{dc}/2$ based on the switching states in Table 4.2.

TABLE 4.2
3-CELL 4L-MFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States			Charging/Discharging States of Capacitors		Phase Leg xn Voltage
	S_{x1}	S_{x2}	S_{x3}	C_{x1}	C_{x2}	V_{xn}
1	1	1	1			$+V_{dc}/2$
2	1	1	0	+		$+V_{dc}/6$
3	1	0	1	-	+	
4	1	0	0		+	$-V_{dc}/6$
5	0	1	1		-	$+V_{dc}/6$
6	0	1	0	+	-	
7	0	0	1	-		$-V_{dc}/6$
8	0	0	0			$-V_{dc}/2$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while '■' represents neither states.

(a) Switching State 1 '111'

(b) Switching State 2 '110'

(c) Switching State 3 '101'

(d) Switching State 4 '100'

(e) Switching State 5 '011'

(f) Switching State 6 '010'

(g) Switching State 7 '001'

(h) Switching State 8 '000'

Fig. 4.7 Operation modes of 3-cell 4L-MFCI – PSC-PWM.

Fig. 4.8 Simulated results of 3-cell 4L-MFCI with PSC-PWM modulation.
(a) Output phase voltages. (b) Output line-to-line voltages.

The simulated results in Fig. 4.8 have verified the theoretical explanation to achieve the four-level output phase voltages and the seven-level output line-to-line voltages based on the operation modes shown in Fig. 4.7. Therefore, under the balanced voltage condition, the output phase voltages of 3-cell 4L-MFCL are synthesized with the voltage levels at $+V_{dc}/2$ (150V), $+V_{dc}/6$ (50V), $-V_{dc}/6$ (-50V) and $-V_{dc}/2$ (-150V) as shown in Fig. 4.8(a).

4.3 Operating Principles of 6-Cell 7L-MFCI

Fig. 4.9 Schematic of three-phase 6-cell 7L multilevel flying capacitor inverter topology.

The three-phase 7L-MFCI using 6-cell configuration based on PSC-PWM modulation is shown in Fig. 4.9. In order to achieve the seven-level output phase voltage waveforms, each phase-leg of 7L-MFCI in this case requires a number of twelve switching devices included the complimentary switches (S_{x1} , S_{x2} , S_{x3} , S_{x4} , S_{x5} , S_{x6} , S_{x6}' , S_{x5}' , S_{x4}' , S_{x3}' , S_{x2}' and S_{x1}') and five flying capacitors (C_{x1} , C_{x2} , C_{x3} , C_{x4} and C_{x5}). Therefore, for a three-phase system, the 7L-MFCI now requires thirty-six switches and fifteen capacitors.

The operating principles of the 6-cell 7L-MFCI share the same approach with the previously presented 2-cell 3L-MFCI and 3-cell 4L-MFCI. In this case, six triangular carriers are required for the PSC-PWM scheme to synthesize the seven-level output phase voltage stepped waveforms. These six carriers are 60° phase-shifted apart between one another as shown in Fig.4.10.

Fig. 4.10 PSC-PWM for three-phase 6-cell 7L-MFCI.

The six switching pulses (Sp-A1, Sp-A2, Sp-A3, Sp-A4, Sp-A5 and Sp-A6) shown in Fig. 4.10 are modulated with respect to Ref A signal. These six generated switching pulses are used to drive the top six switches S_{x1} , S_{x2} , S_{x3} , S_{x4} , S_{x5} , and S_{x6} respectively, while the inverted of these six switching pulses are needed for the respective complimentary switches. Since six carriers are used, there is a combination of $2^6 = 64$ switching states as summarized in Table 4.3. Hence, the charging and discharging states of the capacitors clamped in each phase-leg can also be determined based on the operation modes described in Table 4.3 with the respective switching states.

TABLE 4.3
6-CELL 7L-MFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States						Charging/Discharging States of Capacitors					Phase Leg xn Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	C_{x1}	C_{x2}	C_{x3}	C_{x4}	C_{x5}	V_{xn}
1	1	1	1	1	1	1						$+V_{dc}/2$
2	1	1	1	1	1	0	+					$+V_{dc}/3$
3	1	1	1	1	0	1	-	+				
4	1	1	1	1	0	0		+				$+V_{dc}/6$
5	1	1	1	0	1	1		-	+			$+V_{dc}/3$
6	1	1	1	0	1	0	+	-	+			$+V_{dc}/6$
7	1	1	1	0	0	1	-		+			
8	1	1	1	0	0	0			+			0
9	1	1	0	1	1	1			-	+		$+V_{dc}/3$
10	1	1	0	1	1	0	+		-	+		$+V_{dc}/6$
11	1	1	0	1	0	1	-	+	-	+		
12	1	1	0	1	0	0		+	-	+		0
13	1	1	0	0	1	1		-		+		$+V_{dc}/6$
14	1	1	0	0	1	0	+	-		+		0
15	1	1	0	0	0	1	-			+		
16	1	1	0	0	0	0				+		$-V_{dc}/6$
17	1	0	1	1	1	1				-	+	$+V_{dc}/3$
18	1	0	1	1	1	0	+			-	+	$+V_{dc}/6$
19	1	0	1	1	0	1	-	+		-	+	
20	1	0	1	1	0	0		+		-	+	0
21	1	0	1	0	1	1		-	+	-	+	$+V_{dc}/6$
22	1	0	1	0	1	0	+	-	+	-	+	0
23	1	0	1	0	0	1	-		+	-	+	
24	1	0	1	0	0	0			+	-	+	$-V_{dc}/6$
25	1	0	0	1	1	1			-		+	$+V_{dc}/6$
26	1	0	0	1	1	0	+		-		+	0
27	1	0	0	1	0	1	-	+	-		+	
28	1	0	0	1	0	0		+	-		+	$-V_{dc}/6$
29	1	0	0	0	1	1		-			+	0
30	1	0	0	0	1	0	+	-			+	$-V_{dc}/6$
31	1	0	0	0	0	1	-				+	
32	1	0	0	0	0	0					+	$-V_{dc}/3$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while '■' represents neither states.

TABLE 4.3 (Continued)
6-CELL 7L-MFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States						Charging/Discharging States of Capacitors					Phase Leg xn Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	C_{x1}	C_{x2}	C_{x3}	C_{x4}	C_{x5}	V_{xn}
33	0	1	1	1	1	1					-	$+V_{dc}/3$
34	0	1	1	1	1	0	+				-	$+V_{dc}/6$
35	0	1	1	1	0	1	-	+			-	$+V_{dc}/6$
36	0	1	1	1	0	0		+			-	0
37	0	1	1	0	1	1		-	+		-	$+V_{dc}/6$
38	0	1	1	0	1	0	+	-	+		-	0
39	0	1	1	0	0	1	-		+		-	$-V_{dc}/6$
40	0	1	1	0	0	0			+		-	$-V_{dc}/6$
41	0	1	0	1	1	1			-	+	-	$+V_{dc}/6$
42	0	1	0	1	1	0	+		-	+	-	0
43	0	1	0	1	0	1	-	+	-	+	-	$-V_{dc}/6$
44	0	1	0	1	0	0		+	-	+	-	0
45	0	1	0	0	1	1		-		+	-	$-V_{dc}/6$
46	0	1	0	0	1	0	+	-		+	-	0
47	0	1	0	0	0	1	-			+	-	$-V_{dc}/6$
48	0	1	0	0	0	0				+	-	$-V_{dc}/3$
49	0	0	1	1	1	1				-		$+V_{dc}/6$
50	0	0	1	1	1	0	+			-		0
51	0	0	1	1	0	1	-	+		-		$-V_{dc}/6$
52	0	0	1	1	0	0		+		-		0
53	0	0	1	0	1	1		-	+	-		$-V_{dc}/6$
54	0	0	1	0	1	0	+	-	+	-		$-V_{dc}/3$
55	0	0	1	0	0	1	-		+	-		$-V_{dc}/6$
56	0	0	1	0	0	0			+	-		$-V_{dc}/3$
57	0	0	0	1	1	1			-			0
58	0	0	0	1	1	0	+		-			$-V_{dc}/6$
59	0	0	0	1	0	1	-	+	-			$-V_{dc}/3$
60	0	0	0	1	0	0		+	-			$-V_{dc}/6$
61	0	0	0	0	1	1		-				$-V_{dc}/3$
62	0	0	0	0	1	0	+	-				$-V_{dc}/6$
63	0	0	0	0	0	1	-					$-V_{dc}/3$
64	0	0	0	0	0	0						$-V_{dc}/2$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while '■' represents neither states.

Fig. 4.11 Simulated results of 6-cell 7L-MFCI with PSC-PWM modulation.
(a) Output phase voltages. (b) Output line-to-line voltages.

In the event of the steady-state condition, the nominal voltage across these capacitors C_{x1} , C_{x2} , C_{x3} , C_{x4} and C_{x5} are $1/6 V_{dc}$, $2/6 V_{dc}$, $3/6 V_{dc}$, $4/6 V_{dc}$ and $5/6 V_{dc}$ respectively. Therefore, the seven-level output phase voltages can be synthesized with voltage levels at $+V_{dc}/2$ (150V), $+V_{dc}/3$ (100V), $+V_{dc}/6$ (50V), $0V$, $-V_{dc}/6$ (-50V), $-V_{dc}/3$ (-100V) and $-V_{dc}/2$ (-150V) as shown in Fig. 4.11(a), while the thirteen-level output line-to-line voltage waveforms are presented in Fig. 4.11(b).

4.4 General Characteristics of Classical MFCI

Based on the presented operating principles of the 2-cell 3L-MFCI, 3-cell 4L-MFCI and 6-cell 7L-MFCI using the classical PSC-PWM methods, the operation of n -cell mL -MFCI can be summarized and expressed in general forms. Since the output voltage levels are increased according to the series-connected n_{cells} in the conventional MFCI, therefore the mL output voltage can be determined with the equation (4.1).

$$(mL)\text{MFCI} = n_{cells} + 1 \quad (4.1)$$

The number of switches $i_{switches}$ and capacitors clamped $p_{capacitors}$ for mL -MFCI can now be determined using the equations (2.4) and (2.5) respectively since n_{cells} can be determined from the expression (4.1). Fig. 4.12 shows that the total number of components required increases linearly when more n_{cells} are connected to achieve higher mL output phase voltage. Fig. 4.12 is presented based on single-phase configuration, thus the total number of components required for a three-phase system will definitely be three times the components used in single-phase system.

Fig. 4.12 Number of components required for n -cell single-phase classical multilevel flying capacitor converter topology.

For n -cell mL -MFCI, the voltage across the respective capacitor clamped at p^{th} position (C_{xp}^{th}) shown in Fig. 2.3 can be determined using the following equation (4.2).

$$V_{C_{xp}^{th}}^{MFCI} = \frac{p^{th}}{mL-1} \times V_{dc} \quad (4.2)$$

According to the equation (4.2), the voltage difference between $V_{C_{xp}^{th}}$ and $V_{C_{x(p-1)}^{th}}$ will always be $V_{dc}/(mL-1)$. This shows that the voltage stress across all the switches for any n -cell mL -MFCI are equally distributed. Hence, the voltage stress across the respective switches can be calculated approximately based on the equation (4.3).

$$V_{S_{x(cell n^{th})}}^{MFCI}(t) \approx \begin{cases} -\left(\frac{(mL-1)-p^{th}}{mL-1}\right) V_{dc} \times S_{x(cell n^{th})}(t) & \text{if } cell n^{th} = 1 \\ -\left(\frac{p^{th}-(p^{th}-1)}{mL-1}\right) V_{dc} \times S_{x(cell n^{th})}(t) & \text{if } cell n^{th} \geq 2 \end{cases} \quad (4.3)$$

where

$$S_{x(cell n^{th})}(t) = \text{corresponding switching states '0' (off) and '1' (on)}$$

In order to achieve higher mL output voltage, more n_{cells} will be required for the conventional MFCI using classical PSC-PWM modulation method. This is due to the linearly increased relationship as expressed in (4.1). Consequently, more $p_{capacitors}$ are used which result higher energy storage of capacitors installed. Higher losses are incurred in the converter as well as longer period of time is taken to reach the steady-state condition. Moreover, the overall cost, size and weight of the converter will also be a major concern for the industrial markets and those applications with space constraint.

4.5 Harmonic Characteristics of PSC-PWM Modulation Scheme

Fig. 4.13 Phase-shifted carrier PWM.

Phase-shifted carrier PWM is distinguished for many capacitor-based topologies which allow the converter to have natural balancing capability. Lower output current ripples and more dynamic response performance are hence achieved due to the high switching frequency operation.

Under PSC-PWM scheme, the triangular carriers must be shifted evenly over the switching period (T_s) of the carrier as shown in Fig. 4.13. Therefore, the amount of phase angle (Δ_{phase}) difference between each triangular carrier is determined based on the $n_{carrier}$ used for modulation as expressed in the following equation (4.4).

$$\Delta_{phase} = \frac{360^\circ}{n_{carrier}} (\text{deg}) = \frac{2\pi}{n_{carrier}} (\text{rad}) \quad \text{for } n_{carrier} > 1 \quad (4.4)$$

Since the total harmonic distortion (THD) contents of the voltage and current waveforms are greatly affected by the SPWM methods used, therefore it is important to analyze and verify the harmonic performances. Hence, a series of simulation results for several different mL output phase voltage and line-to-line voltage of MFCI will be shown for the verification of the theoretical analysis.

The spectrum analysis of output voltage using any SPWM can be expressed from the fundamental expression (4.5) based on double Fourier series analysis.

$$\begin{aligned}
 f(t) = & \underbrace{\frac{A_{00}}{2}}_{DC\ Offset} + \underbrace{\sum_{n=1}^{\infty} [A_{0n} \cos(n[\omega_o t + \theta_o]) + B_{0n} \sin(n[\omega_o t + \theta_o])]}_{Fundamental\ Component\ \&\ Baseband\ Harmonics} \\
 & + \underbrace{\sum_{m=1}^{\infty} [A_{m0} \cos(m[\omega_c t + \theta_c]) + B_{m0} \sin(m[\omega_c t + \theta_c])]}_{Carrier\ Harmonics} \\
 & + \underbrace{\sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} [A_{mn} \cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o]) + B_{mn} \sin(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])]}_{Sideband\ Harmonics}
 \end{aligned} \tag{4.5}$$

where

$\omega_o t = y$ = fundamental angular frequency

θ_o = offset angle for reference sinusoidal waveform

$\omega_c t = x$ = carrier angular frequency

θ_c = offset angle for carrier phase shifted waveform

m = order of carrier harmonic component

n = order of fundamental harmonic component

The coefficients of equation (4.5) can be determined through the complex form of double Fourier integrals in equation (4.6):

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) e^{j(mx+ny)} dx dy \tag{4.6}$$

where

$f(x, y)$ = switching function

Fig. 4.14 Reference sinusoidal signal with single triangular carrier – PSC-PWM.

The double Fourier series equation (4.5) can clearly express the harmonic characteristics of any SPWM schemes based on the magnitude of the presence (i) DC offset component, (ii) fundamental component and baseband harmonic, (iii) carrier harmonics and (iv) sideband harmonics in the spectrum.

Since the triangular carriers in PSC-PWM are phase-shifted away from the fundamental carrier, therefore the harmonic analysis of PSC-PWM can be simplified by using a reference sinusoidal signal and a single triangular carrier as shown in the Fig. 4.14. The switching function of PSC-PWM is expressed in Table 4.4. Two conditions are observed in this case which are ‘turn on’ (V_{dc}) and ‘turn off’ (0V) based on the given equation (3.1). The reference sinusoidal signal $\sin(\omega t)$ is now represented as $M \cos y$ where M is referred to modulation index (M_x).

TABLE 4.0
SWITCHING FUNCTION OF PSC-PWM

$f(x, y)$	$-\pi < x < 0$	$0 < x < \pi$
V_{dc}	$M \cos y > -\frac{2x}{\pi}$	$M \cos y > \frac{2x}{\pi}$
0	$M \cos y < -\frac{2x}{\pi}$	$M \cos y < \frac{2x}{\pi}$

The transition from ‘off’ (0V) to ‘on’ (V_{dc}) state determines the lower boundary which is expressed as follows:

$$\begin{aligned} x_{LOWER} &= -\frac{\pi}{2} - \frac{\pi}{2} M \cos y \\ &= -\frac{\pi}{2} (1 + M \cos y) \end{aligned} \quad (4.7)$$

Meanwhile the transition from ‘on’ (V_{dc}) to ‘off’ (0V) state determines the upper boundary as expressed in equation (4.8).

$$\begin{aligned} x_{UPPER} &= \frac{\pi}{2} + \frac{\pi}{2} M \cos y \\ &= \frac{\pi}{2} (1 + M \cos y) \end{aligned} \quad (4.8)$$

The known boundary conditions can now be substituted into the equation (4.6) to achieve the fundamental complex form of the double Fourier analysis as expanded in the following equation (4.9).

$$\begin{aligned} C_{mn} &= \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) e^{j(mx+ny)} dx dy \\ &= \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M \cos y)}^{\frac{\pi}{2}(1+M \cos y)} V_{dc} e^{j(mx+ny)} dx dy \end{aligned} \quad (4.9)$$

Given that the integral of zero will result zero, thus only $f(x, y)$ equal to V_{dc} in the Table 4.4 is integrated with the boundary conditions of equations (4.7) and (4.8).

Following the given equation (4.5), let $m = n = 0$ in equation (4.9) to find the DC component. Thus, the DC offset component is determined as follows:

$$\begin{aligned}
 A_{00} + jB_{00} &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M \cos y)}^{\frac{\pi}{2}(1+M \cos y)} e^{j(0+0)} dx dy \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} [\pi(1+M \cos y)] dy \\
 &= \frac{V_{dc}}{2\pi} [y + M \sin y]_{-\pi}^{\pi} \\
 &= V_{dc}
 \end{aligned} \tag{4.10}$$

The fundamental baseband component is derived in equation (4.11) by equating $m = 0$ and $n > 0$ for the fundamental expression (4.9).

$$\begin{aligned}
 A_{0n} + jB_{0n} &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M \cos y)}^{\frac{\pi}{2}(1+M \cos y)} e^{j(ny)} dx dy \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} [\pi(1+M \cos y)] e^{j(ny)} dy \\
 &= \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} e^{j(ny)} + e^{j(ny)} M \cos y dy \\
 &= \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} e^{j(ny)} + \frac{M}{2} (e^{j(ny)} e^{jy} + e^{j(ny)} e^{-jy}) dy \\
 &= \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} e^{j(ny)} + \frac{M}{2} e^{jy(n+1)} + \frac{M}{2} e^{jy(n-1)} dy
 \end{aligned} \tag{4.11}$$

The integral of the term $e^{j(ny)}$ in equation (4.11) equals to zero for any non-zero condition of n . So, let $n = 1$ since $A_{0n} + jB_{0n} = 0$ for all conditions when $n > 1$. Thus, equation (4.11) is further expressed in the following equation (4.12).

$$\begin{aligned}
 A_{01} + jB_{01} &= \frac{V_{dc}}{2\pi} \int_{-\pi}^{\pi} \frac{M}{2} e^{jy(n-1)} dy \\
 &= \frac{MV_{dc}}{2}
 \end{aligned} \tag{4.12}$$

Next, let $m > 0$ and $n = 0$ for the equation (4.9) to determine the carrier harmonic components as expressed in the equation (4.13).

$$\begin{aligned}
 A_{m0} + jB_{m0} &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+M \cos y)}^{\frac{\pi}{2}(1+M \cos y)} e^{j(mx)} dx dy \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \left[\frac{e^{jm\frac{\pi}{2}(1+M \cos y)} - e^{-jm\frac{\pi}{2}(1+M \cos y)}}{jm} \right] dy \\
 &= \frac{V_{dc}}{jm2\pi^2} \int_{-\pi}^{\pi} \left[e^{jm\frac{\pi}{2}} e^{jm\frac{\pi}{2}M \cos y} - e^{-jm\frac{\pi}{2}} e^{-jm\frac{\pi}{2}M \cos y} \right] dy
 \end{aligned} \tag{4.13}$$

The expression (4.13) can be simplified to the equation (4.15) using the Bessel function integral relationships given in equation (4.14).

$$\int e^{j(\beta) \cos \tau} d\tau = 2\pi J_0(\beta) \tag{4.14}$$

$$\begin{aligned}
 A_{m0} + jB_{m0} &= \frac{V_{dc}}{jm2\pi^2} \left[e^{jm\frac{\pi}{2}} 2\pi J_0\left(m\frac{\pi}{2}M\right) - e^{-jm\frac{\pi}{2}} 2\pi J_0\left(-m\frac{\pi}{2}M\right) \right] \\
 &= \frac{V_{dc}}{jm\pi} J_0\left(m\frac{\pi}{2}M\right) \left[e^{jm\frac{\pi}{2}} - e^{-jm\frac{\pi}{2}} \right] \\
 &= \frac{2V_{dc}}{m\pi} J_0\left(m\frac{\pi}{2}M\right) \sin\left(m\frac{\pi}{2}\right)
 \end{aligned} \tag{4.15}$$

Lastly, the sideband harmonics component can be expressed in equation (4.16) by letting $m > 0$ and $n \neq 0$ into equation (4.9).

$$\begin{aligned}
 A_{mn} + jB_{mn} &= \frac{V_{dc}}{2\pi^2} \int_{-\pi - \frac{\pi}{2}(1+M \cos y)}^{\pi - \frac{\pi}{2}(1+M \cos y)} \int e^{j(mx+ny)} dx dy \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\pi}^{\pi} \left[\frac{e^{jm\frac{\pi}{2}(1+M \cos y)} - e^{-jm\frac{\pi}{2}(1+M \cos y)}}{jm} \right] e^{jny} dy \\
 &= \frac{V_{dc}}{jm2\pi^2} \left[e^{jm\frac{\pi}{2}} 2\pi j^n J_n \left(m \frac{\pi}{2} M \right) - e^{-jm\frac{\pi}{2}} 2\pi j^{-n} J_n \left(-m \frac{\pi}{2} M \right) \right] \quad (4.16) \\
 &= \frac{V_{dc}}{m\pi} J_n \left(m \frac{\pi}{2} M \right) \left[\frac{e^{j\frac{\pi}{2}(m+n)} - e^{-j\frac{\pi}{2}(m+n)}}{j} \right] \\
 &= \frac{2V_{dc}}{m\pi} J_n \left(m \frac{\pi}{2} M \right) \sin \left[\frac{\pi}{2}(m+n) \right]
 \end{aligned}$$

The harmonic analysis for sine-triangular modulation in Fig. 4.14 is expressed in the equation (4.17) by substituting the equations (4.10), (4.12), (4.15) and (4.16) back into the initial equation (4.5).

$$\begin{aligned}
 f(t) &= \frac{V_{dc}}{2} + \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_o) \\
 &+ \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0 \left(m \frac{\pi}{2} M \right) \sin \left(m \frac{\pi}{2} \right) \cos(m[\omega_c t + \theta_c]) \\
 &+ \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{m} J_n \left(m \frac{\pi}{2} M \right) \sin \left[\frac{\pi}{2}(m+n) \right] \cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])
 \end{aligned} \quad (4.17)$$

The equation (4.17) describes the voltage spectrum analysis according to the magnitude of the pulses defined by $f(x,y)$ in Table 4.4 that is between 0V and V_{dc} .

However, the DC offset component of equation (4.17) is cancelled away in nature for the output phase voltage spectrum. Since the output phase voltage is referred from the respective phase x to the neutral point of the dc-link n , the peak-to-peak amplitude of synthesized output phase voltage falls between $+V_{dc}/2$ and $-V_{dc}/2$. The output phase voltage $V_{xn}(t)$ spectrum based on the sine-triangular modulation of Fig. 4.14 is now expressed in (4.18).

$$\begin{aligned}
 V_{xn}(t) = & \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_o) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m \frac{\pi}{2} M\right) \sin\left(m \frac{\pi}{2}\right) \cos(m[\omega_c t + \theta_c]) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{m} J_n\left(m \frac{\pi}{2} M\right) \sin\left[\frac{\pi}{2}(m+n)\right] \cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o])
 \end{aligned} \tag{4.18}$$

where

$V_{xn}(t)$ = phase a, b and c voltages with respect to neutral point of dc-link

The equation (4.18) is expressed for the 2L-VSI output phase voltage only but not for the mL output phase voltage spectrum. When more than one triangular carrier is implemented in the PSC-PWM scheme and phase-shifted evenly with respect to equation (4.4), the first group of sideband harmonics for the mL output phase voltage will be shifted away from the fundamental baseband harmonic. The shifting behavior of the sideband harmonics can be observed clearly in Fig. 4.15 based on different output phase voltage levels with the same carrier frequency (f_c) applied in the modulation.

(a)

(b)

(c)

Fig. 4.15 Output phase voltage spectrum based on PSC-PWM.
(a) Three-level modulation. (b) Four-level modulation. (c) Seven-level modulation.

The sideband harmonics in Fig. 4.15 are in fact produced away from the baseband component depending on the $n_{carrier}$ and the f_c used in the PSC-PWM modulation, which can be determined in terms of frequency (f_{shift}) using equation (4.19) or Carrier Harmonic Orderth as expressed in (4.20).

$$f_{shift} = f_c \times n_{carrier} \quad (4.19)$$

$$\begin{aligned} \text{Carrier Harmonics Order}^{th} &= \text{Harmonics Order}^{th} \times n_{carrier} \\ &= \frac{f_c}{f_o} \times n_{carrier} \end{aligned} \quad (4.20)$$

where

f_c = carrier frequency,

f_o = fundamental frequency of the reference sinusoidal signal

The final expression of any mL output phase voltage harmonic spectrum based on PSC-PWM is expressed as follows accordingly to the $n_{carrier}$ being phase-shifted:

$$\begin{aligned} V_{xn_{PSCPWM-xL}}(t) &= \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_o) \\ &+ \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} J_0\left((Nm)\frac{\pi}{2}M\right) \sin\left((Nm)\frac{\pi}{2}\right) \cos((Nm)[\omega_c t + \theta_c]) \\ &+ \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_n\left((Nm)\frac{\pi}{2}M\right) \sin\left[\frac{\pi}{2}((Nm)+n)\right] \\ &\quad \times \cos((Nm)[\omega_c t + \theta_c] + n[\omega_o t + \theta_o]) \end{aligned} \quad (4.21)$$

where

M = modulation index (Mx)

$N = n_{carrier}$ = total number of carriers used in PSC-PWM

x = number of voltage levels

The carrier harmonics in equation (4.21) carries the $\sin((Nm) \pi/2)$ term meaning that carrier harmonics are cancelled away for any odd-level output phase voltages when even number of triangular carriers are used in the PSC-PWM modulation. Besides that, the $\sin[((Nm)+n) \pi/2]$ term carried in the sideband harmonics describes that the odd sidebands occur around the even N multiples of Harmonic Orderth while the even sidebands occur around the odd N multiples of Harmonic Orderth. It should be noted that when the first group of sideband harmonics is being shifted further away, the magnitude of these sidebands becomes much smaller. This explains that the size of the resonant filter can be greatly reduced with respect to the relationship in (3.4).

The theoretical results obtained from the calculated values based on equation (4.21) are verified with the simulation results obtained in Fig. 4.15. Hence, the analytical seven-level output phase voltage harmonic spectrum is compared in Fig. 4.16. Thus, it is proven that the equation (4.21) describes exactly the harmonic characteristic of the PSC-PWM modulation for any mL output phase voltage.

Fig. 4.16 Simulation and analytical results – Output phase voltage spectrum PSC-PWM (Seven-level modulation).

The harmonic analysis for output line-to-line voltages (V_{l-l}) based on PSC-PWM can be realized from the differences between any two adjacent output phase voltages. For that reason, the output phase voltages V_{an} and V_{bn} are expressed in (4.22) and (4.23) respectively by taking into consideration of the 120° ($2\pi/3$) phase-shifted of Ref B.

$$\begin{aligned}
 V_{an_{PSCPWM-xL}}(t) = & \frac{MV_{dc}}{2} \cos(\omega_o t) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} J_0\left((Nm)\frac{\pi}{2}M\right) \sin\left((Nm)\frac{\pi}{2}\right) \cos((Nm)[\omega_c t]) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_n\left((Nm)\frac{\pi}{2}M\right) \sin\left[\frac{\pi}{2}((Nm)+n)\right] \\
 & \quad \times \cos((Nm)[\omega_c t] + n[\omega_o t])
 \end{aligned} \tag{4.22}$$

$$\begin{aligned}
 V_{bn_{PSCPWM-xL}}(t) = & \frac{MV_{dc}}{2} \cos\left(\omega_o t - \frac{2\pi}{3}\right) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} J_0\left((Nm)\frac{\pi}{2}M\right) \sin\left((Nm)\frac{\pi}{2}\right) \cos((Nm)[\omega_c t]) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_n\left((Nm)\frac{\pi}{2}M\right) \sin\left[\frac{\pi}{2}((Nm)+n)\right] \\
 & \quad \times \cos\left((Nm)[\omega_c t] + n\left[\omega_o t - \frac{2\pi}{3}\right]\right)
 \end{aligned} \tag{4.23}$$

$$\begin{aligned}
 V_{ab_{PSCPWM-xL}}(t) = & V_{an_{PSCPWM-xL}}(t) - V_{bn_{PSCPWM-xL}}(t) \\
 = & \frac{\sqrt{3}MV_{dc}}{2} \cos\left(\omega_o t + \frac{\pi}{6}\right) \\
 & + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_n\left((Nm)\frac{\pi}{2}M\right) \sin\left[\frac{\pi}{2}((Nm)+n)\right] \sin\left((2n-1)\frac{\pi}{3}\right) \\
 & \quad \times \cos\left((Nm)[\omega_c t] + (2n-1)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right)
 \end{aligned} \tag{4.24}$$

(a)

(b)

(c)

Fig. 4.17 Output line-to-line voltage spectrum based on PSC-PWM.
(a) Three-level modulation. (b) Four-level modulation. (c) Seven-level modulation.

The spectrum analysis of output line-to-line voltage V_{ab} is derived in equation (4.24). Same approach is applied to achieve the harmonic spectrum of V_{bc} and V_{ca} , just that the offset angle of both fundamental frequency and carrier frequency are different. The output line-to-line voltage is referred to V_{ab} for simplicity since the harmonic analysis is the same for V_{bc} and V_{ca} , thus V_{ab} will be discussed frequently in the latter part.

When subtracting equation (4.23) from (4.22), the carrier harmonics are cancelled away in nature due to the crossover point between two phase reference sinusoidal signals at every multiples of 60° . On top of that, the triplen sideband harmonics are also being cancelled away. Hence, there is a $\sin((2n-1)\pi/3)$ term added in the sideband harmonics of equation (4.24). The cancellation of carrier harmonics and triplen sideband harmonics can be observed in Fig. 4.17 as compared with those in Fig. 4.15.

The analytical results of seven-level PSC-PWM modulation for output V_{l-l} as shown in Fig. 4.18 are obtained based on the calculated values from equation (4.24). The theoretical analysis is exactly matched with the simulation result shown in Fig. 4.17.

Fig. 4.18 Simulation and analytical results – Output line-to-line voltage spectrum PSC-PWM (Seven-level modulation).

Chapter 5

Proposed Reduced Modular Cell Inverters

Despite the proven facts that producing high resolution waveforms are favorable at all times, there are still many complications involved such as the increase in component counts, cost, size as well as the design complexity. As a result, the overall reliability and efficiency of the system are also affected. Such implications motivate many researchers to design and develop alternative new multilevel topologies.

Several multilevel topologies are developed to synthesize higher mL output voltages with reduced component counts, and have been reported in the recent literature are: (I) multilevel inverter based on switched DC sources [87], (II) improved double flying capacitor multicell converter [88], (III) symmetric hybrid multilevel inverter [89], (IV) packed-u cells converter [90], and (V) stacked multicell inverter with reduced dc voltages sources [91].

Fig. 5.1 Recent single-phase multilevel topologies (I) to (V) with reduced component counts. (a) 5L multilevel inverter with switched DC sources. (b) 11L improved double flying capacitor multicell inverter. (c) 5L symmetric hybrid multilevel inverter. (d) 7L packed-u cells inverter. (e) 5L stacked multicell inverter with reduced DC sources.

Multilevel inverters (I) to (V) share similarity in their circuit designs with the H-bridge configuration as shown in Fig. 5.1. It can be observed that one leg is being replaced with multilevel flying capacitor inverter (MFCI) or active neutral point clamped inverter (ANPC) topologies while the other leg is remained with two low frequency (LF) power switches. These converters (I) to (V) have the ability to synthesize higher mL output voltages with reduced component counts as compared to the commercially available MFCI and ANPC. High flexibility is also found in these converters due to the modular cells concept being utilized in their designs.

Nevertheless, bulky phase-shifted transformer is required to provide isolated dc sources for (I and II) in a single phase system and (III to V) in a three phase system. Thus, multiple bridge rectifiers are also needed at the secondary side of the transformer. As a result, additional cost, losses and larger installation space are incurred [92].

Therefore, in this Chapter, two approaches to achieve transformerless modular cell inverters with reduced flying capacitors and switching devices are proposed using the novel hybrid carrier-based modulation methods. The two proposed multilevel reduced modular cell converters are named as lightweight flying capacitor inverter (LFCI) and reduced flying capacitor inverter (RFCI). Both topologies are designed based on clamping a series of modular cells onto the low operational frequency cell.

By doing so, both proposed LFCI and RFCI retain the modularity approach and eliminate the need of transformer at all times for both single and three phase topologies. On top of that, higher mL output voltages can be synthesized with the

component counts significantly reduced. Similarity in converter design is found between the proposed topologies and the classical MFCI.

The advanced hybrid SPWM schemes are also proposed in this Chapter namely the phase-shifted carrier phase-opposition-disposition PWM (PSC-POD-PWM) and the phase-shifted carrier phase-disposition PWM (PSC-PD-PWM). The harmonic characteristics analysis of both hybrid SPWM schemes are detailed and proven to have successfully overcome the issues of classical modulation LSC-PWM and PSC-PWM in Chapter 3 with their respective advantageous properties well attained.

The classical MFCI proposed by Meynard *et al.* [63] has been commercially developed in the industries by ALSTOM Power Conversion [75, 86, 93] for medium voltage (MV) up to 4.16 kV drives. Commonly, the output voltages of classical MFCI are synthesized using phase-shifted carrier PWM (PSC-PWM) as explained previously in Chapter 4. However, the following factors make the MFCI unfeasible for higher voltage applications [75, 92, 93] due to: (a) high switching frequency operation, (b) large inrush dc-link current, and (c) increase flying capacitor energy storage.

Hence, a detailed comparative study made between the proposed LFCI, the proposed RFCI and the classical MFCI based on 7-level (7L) output voltages is presented to highlight the enhanced performances. The perceived merits of both proposed LFCI and RFCI allow the converter to be attractively suitable for higher MV drives and also for applications where space constraint is a major concern. The performance of both LFCI and RFCI with hybrid SPWM is evaluated under dynamic conditions to verify its feasibility.

5.1 Lightweight Flying Capacitor Inverter Topology

The problems associated with the classical MFCI based on PSC-PWM modulation as addressed earlier on, those issues make the topology becomes impractical to realize for higher mL output phase voltage. On top of that, the MFCI is not applicable for high power applications due to its high switching frequency PSC-PWM [75].

As higher mL output voltage is always desired to be achieved for high power applications, those challenges encountered in the classical MFCI motivates to work on designing a lighter weight MFCI while achieving higher mL output voltage. Hence, a new approach has been proposed to overcome those mentioned limitations.

In order to achieve higher mL output voltage with reduced number of components needed, the proposed method is designed in such the way that the output voltage levels are achieved based on the binary progression when more n_{cells} are connected. Therefore, the number of output voltage levels for the lighter weight version of multilevel flying capacitor inverter (LFCI) is expressed in the equation (5.1).

$$(mL)LFCI = 2^{n_{cells}} - 1 \quad (5.1)$$

According to the equation (5.1), the three-level output phase voltage is synthesized with 2-cell LFCI which is exactly the same as the classical 2-cell 3L-MFCI. However, LFCI is perfectly suitable for achieving higher incremental voltage stepped waveform at an exponential rate. This shows that a seven-level output phase voltage is achievable with a 3-cell LFCI and a fifteen-level output voltage is synthesized by the 4-cell LFCI.

Since natural balancing technique is still required for higher mL -MFCI despite of the excessive redundant switching states generated by the PSC-PWM, therefore capacitor voltage balancing will no longer be an issue for the flying capacitors based converter topology. Instead of having $2^6 = 64$ states in the 6-cell 7L-MFCI, now only $2^3 = 8$ switching states are needed for the 3-cell 7L-LFCI. This shows that the minimum number of switching states (n_{states}) needed for the mL -LFCI or mL -MFCI is actually depending on the n_{cells} implemented which can be determined with the equation (5.2).

$$n_{states} = 2^{n_{cells}} \quad (5.2)$$

The reason for expressing the n_{states} in equation (5.2) based on binary progression is simple. This is because of the given condition in equation (3.1), only either ‘turn on’ or ‘turn off’ state is permitted for a normal operation of the semiconductor devices. Thus, in order to minimize the number of components required, the n_{states} must also be reduced when synthesizing the desired mL output voltage.

The performance of the proposed LFCI under the two advanced hybrid sinusoidal PWM schemes (PSC-POD-PWM and PSC-PD-PWM) is analyzed. The feasibility of the LFCI is also validated through both simulation and experimental results to highlight the enhanced performances achieved compared to the classical MFCI.

5.1.1 Generalized Structure of Lightweight Flying Capacitor Inverter (LFCI)

Fig. 5.2 Proposed transformerless three-phase n -cell lightweight flying capacitor inverter (LFCI) topology.

The general circuit configuration of the proposed three-phase lightweight flying capacitor inverter is shown in Fig. 5.2. Each modular cell consists a pair of semiconductor switches S_x including its complementary S_x' and a capacitor p clamped in between the cells. Hence, the number of switches i_{switches} and capacitors clamped $p_{\text{capacitors}}$ can be determined based on the number of modular cells (n_{cells}) used.

The proposed LFCI is constructed using a series-connected of modular cells (Cell 1 to Cell n) that is based on the binary progression ratio. It is intentionally to synthesize the desired mL output voltage waveforms (5.1) using the maximized n_{states} generated (5.2) according to the n_{cells} implemented. By doing so, the number of components required is further minimized as well even though the proposed LFCI share similarity in converter design as the classical MFCI topology.

In order to maximize (5.2), the pair of switches (S_{x1} and S_{x1}') in Cell 1 must always operate at low frequency of 50 Hz. However, it should be noted that the two LF switches are not served as H-bridge leg like those in Fig. 5.1. Thus, it allows the proposed LFCI to remain transformerless for the three-phase systems because of its single dc-link configuration.

5.1.2 Operating Principles of 3-Cell 7L-LFCI

By having three modular cells (Cell 1, Cell 2 and Cell 3) connected in series for each phase-leg, it results a single-phase seven-level (7L) lightweight flying capacitor inverter (LFCI) as presented in Fig. 5.3(a). In this case, a minimum number of 6 i_{switches} (S_{x1} to S_{x3} and $S_{x1'}$ to $S_{x3'}$) and 2 $p_{\text{capacitors}}$ (C_{x1} and C_{x2}) clamped in between the modular cells are required for each phase-leg depending on the voltage ratings of the converter design. Thus, the total component counts are greatly reduced when comparing with the classical 6-cell 7L-MFCI (12 i_{switches} and 5 $p_{\text{capacitors}}$ per phase-leg) which can be clearly observed from the Fig. 5.3(b). The difference would be greater when designing the three-phase systems.

Since three cells of six active switches are used for the proposed 3-cell 7L-LFCI, therefore there is a combination of $2^3 = 8$ operating modes from '000' to '111' as summarized in Table 5.1. It should be clearly observed that only two redundant states are being produced for the zero output level. By reducing the excessive switching states, higher mL output voltage waveforms can now be synthesized using lesser components.

Fig. 5.3 (a) Proposed 3-Cell 7L-LFCI. (b) Classical 6-Cell 7L-MFCI.

TABLE 5.1
3-CELL 7L-LFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	SSignalLevel	Switching States			Charging/Discharging States of Capacitors		Phase Leg xn Voltage V_{xn}
		S_{x1}	S_{x2}	S_{x3}	C_{x1}	C_{x2}	
1	2	1	1	1			$+V_{dc}/2$
2	3	1	1	0	+		$+V_{dc}/3$
3	4	1	0	1	-	+	$+V_{dc}/6$
4	5	1	0	0		+	0
5	-5	0	1	1		-	
6	-4	0	1	0	+	-	$-V_{dc}/6$
7	-3	0	0	1	-		$-V_{dc}/3$
8	-2	0	0	0			$-V_{dc}/2$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while ' ' represents neither states

Besides that, the pair of switches (S_{x1} and S_{x1}') in Cell 1 is always performing at the fundamental frequency of 50 Hz where the all the positive output levels are produced when S_{x1} conducts and vice versa all the negative levels are obtained when S_{x1}' conducts. Therefore, the output seven-level phase voltage waveforms are synthesized correspondingly at $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$ and zero level based on the given switching states in Table 5.1.

The charging and discharging states of the two flying capacitors (C_{x1} and C_{x2}) for 3-cell 7L-LFCI in Table 5.1 are observed to be the same as the 3-cell 4L-MFCI in the Table 4.2. Therefore, the operation modes of the 3-cell 7L-LFCI can be referred to the same illustrations of current flows with respect to the corresponding switching states shown earlier in Fig. 4.7. The reduction in n_{states} allows the charging time for the C_{x1} and C_{x2} of the proposed 3-cell 7L-LFCI to be shorten and reach its steady-state operation faster when compared with the classical 6-cell 7L-MFCI.

Fig. 5.4 Proposed advanced hybrid sinusoidal PWM schemes.
(a) PSC-POD-PWM. (b) PSC-PD-PWM.

The operational principles of the proposed 3-cell 7L-LFCI are achieved using two proposed advanced hybrid sinusoidal PWM schemes named as phase-shifted carrier phase-opposition-disposition PWM (PSC-POD-PWM) and the phase-shifted carrier phase-disposition PWM (PSC-PD-PWM) as shown in Fig. 5.4. Generally, for all carrier-based PWM, $(mL - 1)$ number of triangular carriers (n_{tri}) would be required for any mL modulation scheme despite of the converter topological design.

In the case of proposed 3-cell 7L-LFCI, n_{tri} are used and divided into 2 sets equally where one set level-shifted above zero reference magnitude ($tri_{TOP(1,2,3,...,(n_{tri}/2))}$) and the other set below the zero reference magnitude ($tri_{BOT(1,2,3,...,(n_{tri}/2))}$). The top and bottom carriers are 120° phase-shifted evenly based on (5.3).

$$\Delta_{phase} = \frac{360^\circ}{(n_{carrier} / 2)} (\text{deg}) = \frac{2\pi}{(n_{carrier} / 2)} (\text{rad}) \quad \text{for } n_{carrier} = \text{even} > 2 \quad (5.3)$$

The modulation technique for the n -cell mL -LFCI under the proposed two advanced hybrid sinusoidal PWM schemes (PSC-POD-PWM and PSC-PD-PWM) is achieved based on analog design as shown in Fig. 5.5. The top and bottom set of triangular carriers with 120° phase-shifted apart are fed into the respective comparators in the Stage A of Fig. 5.5. The six switching pulses (Sp-x1, Sp-x2, Sp-x3, Sp-x4, Sp-x5 and Sp-x6) in Fig. 5.6 are modulated after comparing the reference sinusoidal signal (Mx_{sine}) with respective carriers.

Fig. 5.5 Proposed analog modulation technique for n -cell mL -LFCI.

Fig. 5.6 Output switching pulses (Sp-x) at Stage A of Fig. 5.5 under PSC-POD-PWM modulation scheme.

The switching pulses Sp-x1, Sp-x2 and Sp-x3 are generated during the positive half cycle of the $M_{x\text{sine}}$, which is the only period that the sinusoidal signal will be greater than the three phase-shifted (120°) carriers above the zero reference magnitude. The other three switching pulses Sp-x4, Sp-x5 and Sp-x6 are generated when the $M_{x\text{sine}}$ is greater than the three inverted phase-shifted (120°) triangular carriers below the zero reference magnitude. From the Sp-x4, Sp-x5 and Sp-x6 of Fig. 5.6 show that the switching pulses are always at 'on' state during the positive half cycle of the $M_{x\text{sine}}$, where the conditions described in the equation (3.1) are met.

After the six switching pulses (Sp-x1, Sp-x2, Sp-x3, Sp-x4, Sp-x5 and Sp-x6) are modulated in the Stage A, these signals are further level-shifted again respectively in Stage B based on Fig. 5.5. During the positive cycle of the $M_{x\text{sine}}$, the first two top

switching pulses modulated with respect to the tri_{TOP1} and tri_{TOP2} are always level shifted to the +1V above the zero reference, while the rest of the switching pulses modulated with respect from tri_{TOP3} up to $\text{tri}_{\text{TOP}(\text{ntri}/2)}$ are not required to be level-shifted. With respect to the negative cycle of the M_{Xsine} , the switching pulses modulated with respect to tri_{BOT1} up to the $\text{tri}_{\text{BOT}((\text{ntri}/2)-2)}$ are level-shifted to -1V below the zero reference and the remaining last two bottom switching pulses modulated with respect to $\text{tri}_{\text{BOT}((\text{ntri}/2)-1)}$ and $\text{tri}_{\text{BOT}(\text{ntri}/2)}$ are always level-shifted to -2V below the zero reference.

The results of the six switching pulses modulated after level-shifted respectively in Stage B (LS-x1, LS-x2, LS-x3, LS-x4, LS-x5 and LS-x6) are shown clearly in Fig. 5.7 according to the conditions explained. After level-shifted the six switching pulses in Stage B, the LS-x1, LS-x2, LS-x3, LS-x4, LS-x5 and LS-x6 are then summed together in Stage C of Fig. 5.5. The resulted waveform of the summed signal (SSignal) is shown in Fig. 5.8.

The purpose of level-shifting the six switching pulses in the Stage B and then summed together the signals at the Stage C is to create the SSignalLevel states as shown in Table 5.1. These SSignalLevel states are mapped to the eight switching states condition designed previously by determining the amplitude level of the SSignal using the look-up table which is also referred as switching state table in Fig. 5.5 based on Table 5.1. Hence, the significant reduction of excessive switching states from 64 states to the minimum required 8 switching states can now be practically achieved.

Fig. 5.7 Output level-shifted switching pulses (LS-x) at Stage B of Fig. 5.5 under PSC-POD-PWM modulation scheme.

Fig. 5.8 Output summed signal (SSignal) at Stage C of Fig. 5.5 under PSC-POD-PWM modulation scheme.

Fig. 5.9 Voltage stress across Sa1(top) to Sa3(bottom) for 3-cell 7L-LFCI based on hybrid PSC-PD-PWM with $M_x = 0.9$ and $V_{dc} = 300V$.

Hence, the final gating signals for the switches S_{x1} , S_{x2} and S_{x3} of the 3-cell 7L-LFCI are achieved from the SSignal according to conditions set in the switching state table. The resulting gate signals can be observed from Fig. 5.9 over two fundamental cycle period. As for the complimentary switches S_{x1}' , S_{x2}' and S_{x3}' , the gating signals are in fact the inverted signals of the switches S_{x1} , S_{x2} and S_{x3} which can be obtained simply with the use of the inverter NOT gates.

On the other hand, due to the symmetrical geometry in the modulation carriers (combination of in-phase disposition and phase-shifted properties) of the proposed advanced hybrid PSC-PD-PWM scheme, the bottom sets of carriers ($\text{triBOT}_{(1,2,3,\dots,(n_{tri}/2))}$) in Fig. 5.4 can be totally eliminated as shown in Fig. 5.10. It can also be alternatively named as reduced PSC-PD-PWM (R-PSC-PD-PWM). Instead of having n_{tri} to synthesize the desired mL output phase voltage methods using any SPWM based on the equation (3.2), the R-PSC-PD-PWM can successfully synthesize the same mL output phase voltage with 50% reduced of n_{tri} required which is now re-expressed again in the following equation (5.4).

$$n_{tri(RPSCDPWM)} = \frac{n_{tri(SPWM)}}{2} = \frac{(mL)-1}{2} \quad (5.4)$$

Despite greatly reducing the n_{tri} by 50%, the Δ_{phase} between each triangular carrier must still be evenly phase-shifted accordingly to the same (5.3). However, it is required to have another set of same reference sinusoidal signal being level-shifted up with respect to the peak of the triangular carriers in order to achieve the same PWM modulation effect as shown in Fig. 5.11. By rebuilding it this way, the control signal Mx_{sine} will not be affected.

Fig. 5.10 Reduced carrier of phase-shifted carrier phase-opposition-disposition PWM.

Fig. 5.11 Level-shifted of reference sinusoidal signal in R-PSC-PD-PWM.

The motivation of R-PSC-PD-PWM is to avoid the complexity of generating switching pulses with the digital signal processors (DSP) or the design of analog comparator circuitries, especially when more n_{tri} is required for higher mL output phase voltage. Besides that, the computational effort is greatly reduced with the reduction of n_{tri} as compared to level-shifting another set of reference signal Mx_{sine} . Thus, the sampling time needed for DSP can be decreased to minimize the delays.

In the case of R-PSC-PD-PWM, only the stage A of the modulation technique in the Fig. 5.5 has to be modified again to satisfy the described operating condition with the rebuilding of Mx_{sine} as shown in Fig. 5.12. Hence, the same modulation method in Stages B and C of Fig. 5.5 are remained the same for the R-PSC-PD-PWM modulation technique in Fig. 5.12.

Fig. 5.12 Proposed analog modulation technique for n -cell mL -LFCL.

5.1.3 Alternative Digital Modulation Technique for n -cell mL -LFCI

The modulation technique to achieve the desired gating signals for the LFCI as presented previously is based on the analog approach. The modulation technique presented in both Figs. 5.5 and 5.12 is achievable with the digital signal processors. But it may become more complicated to achieve the same desired gating signals by developing the hardware circuit due to the level-shifter, multiplier and summation properties shown in Stage B and Stage C of both Figs. 5.5 and 5.12.

Fig. 5.13 Digital modulation technique for 3-cell 7L-LFCI.

An alternative approach to avoid these complications during the hardware development is to use the digital logic gates instead. The design of alternative digital modulation technique for the same 3-cell 7L-LFCI is presented in Fig. 5.13. This digital modulation technique will replace the Stage B and Stage C of Figs. 5.5 and 5.12 including the need of determining the switching state conditions in Table 5.1 by using the look-up tables. The digital logic gates proposed in Fig. 5.13 consists of AND gate, NAND gate, OR gate, XNOR gate as well as the inverter NOT gates.

The PWM1, PWM2, PWM3, PWM4, PWM5 and PWM6 of Fig. 5.13 are referred to the switching pulses (Sp-x) modulated right after the comparators in the Stage A of Figs. 5.5 and 5.12. While the S_{x1} , S_{x2} , S_{x3} , S_{x3}' , S_{x2}' and S_{x1}' at the output of Fig. 5.13 are referred to the output gating signals for the respective switches of 3-cell 7L-LFCI.

According to the digital modulation technique shown in Fig. 5.13 using logic gates, the final expression of the gating signal for the switch S_{x1} is given as follows:

$$S_{x1}(t) = \begin{cases} 1 & \text{if } \sin(\omega t) > 0 \\ 0 & \text{if } \sin(\omega t) < 0 \end{cases} \quad (5.5)$$

The result of the final gating signal for S_{x1} will be a square wave when the reference sinusoidal signal is greater than the zero reference. The gating signal of S_{x1} is achieved with a single analog comparator for each phase-leg. This is the only analog comparator in this case which cannot be replaced with any digital logic gates due to the need of controlling the reference signal $M_{x\text{sine}}$.

The final expression of the modulated gating signal for the switch S_{x2} ' is formulated with the following equation (5.6) based on the digital logic gates used in Fig. 5.13.

$$\begin{aligned} \overline{S_{x2}}(t) = & \left[\begin{aligned} & \left(\overline{\text{PWM1}(t) \bullet \text{PWM2}(t) \bullet \text{PWM3}(t)} \right) \bullet \left(\text{PWM1}(t) + \overline{\text{PWM2}(t)} + \overline{\text{PWM3}(t)} \right) \\ & \bullet \left(\overline{\text{PWM1}(t)} + \text{PWM2}(t) + \overline{\text{PWM3}(t)} \right) \bullet \left(\overline{\text{PWM1}(t)} + \overline{\text{PWM2}(t)} + \text{PWM3}(t) \right) \\ & \bullet S_{x1}(t) \end{aligned} \right] \\ & + \left[\begin{aligned} & \left(\overline{\text{PWM4}(t) \bullet \text{PWM5}(t) \bullet \text{PWM6}(t)} \right) \bullet \left(\text{PWM4}(t) + \overline{\text{PWM5}(t)} + \overline{\text{PWM6}(t)} \right) \\ & \bullet \left(\overline{\text{PWM4}(t)} + \text{PWM5}(t) + \overline{\text{PWM6}(t)} \right) \bullet \left(\overline{\text{PWM4}(t)} + \overline{\text{PWM5}(t)} + \text{PWM6}(t) \right) \end{aligned} \right] \end{aligned} \quad (5.6)$$

The method applied to achieve the gating signal for the switch S_{x2} ' requires a number of logic gates such as NAND, AND, and OR gates based on the given equation (5.6). Besides that, part of the expression in the equation (5.6) also depends on the switching state condition of S_{x1} based on the given expression (5.5) previously. Hence, the gating signal for the switch S_{x2} is achieved with aid of NOT gate to obtain its inverted signals from its complimentary switch S_{x2} ' as shown in Fig. 5.13.

While the final expression of the gating signal for switch S_{x3} ' is given in the following equation (5.7).

$$\overline{S_{x3}}(t) = \left\{ \begin{aligned} & \left[\left(\text{PWM1}(t) \bullet \text{PWM2}(t) \bullet \text{PWM3}(t) \right) + \left(\overline{\text{PWM1}(t)} \bullet \overline{\text{PWM2}(t)} \bullet \overline{\text{PWM3}(t)} \right) \bullet S_{x1}(t) \right] \\ & + \left[\left(\text{PWM4}(t) \bullet \text{PWM5}(t) \bullet \text{PWM6}(t) \right) + \left(\overline{\text{PWM4}(t)} \bullet \overline{\text{PWM5}(t)} \bullet \overline{\text{PWM6}(t)} \right) \right] \end{aligned} \right\} \quad (5.7)$$

The gating signal for S_{x3}' is achieved simply with two XNOR gates, one AND gate and one OR gate in Fig. 5.13 based on the equation (5.7). The gating signal for S_{x3} can be achieved with the inverter NOT gate as well to obtain its inverted signal from its complimentary switch S_{x3}' .

The same gating signals modulated based on the proposed digital modulation technique shown in Fig. 5.13 can achieve the exactly the same results of gating signal from the previous analog modulation technique presented in Figs. 5.5 and 5.12. Even though the proposed alternative approach for modulation technique uses digital logic gates, but the control of reference sinusoidal signal based on M_x will not be affected for practical applications. As a result, this proposed method can help to reduce the complication process in the hardware development. On top of that, the computational effort required can also be reduced and simplified in the digital signal processors to provide faster and dynamic control response in the converters.

5.1.4 Voltage Characteristics Expressions

For the n -cell mL -LFCI, the voltage across the respective capacitor clamped at p^{th} position (C_{xp}^{th}) in Fig. 5.2 can be determined based on the following expression (5.8).

$$V_{C_{x(p^{th})}^{LFCI}} = \frac{2^{(p^{th})} - 1}{mL - 1} \times V_{dc} \quad (5.8)$$

In this case of the proposed 3-cell 7L-LFCI, the flying capacitor voltages V_{Cx1} and V_{Cx2} are maintained $V_{dc}/6$ and $V_{dc}/2$ respectively under the steady-state operation. Even though 3-cell 7L-LFCI has the same operation modes as the 3-cell 4L-MFCI, but the voltage across the two flying capacitors are now different which can be observed from Table 5.2. It should be noted that not only the number of flying capacitors are being reduced when comparing based on the number of output phase voltage levels (proposed 3-cell 7L-LFCI and classical 6-cell 7L-MFCI) but also significantly reduced the voltage ratings of these flying capacitors based on the number of modular cells used (proposed 4-cell 15L-LFCI and classical 4-cell 5L-MFCI).

TABLE 5.2
CAPACITOR VOLTAGES FOR CLASSICAL MFCI AND PROPOSED LFCI

Capacitors Clamped at p^{th} Position	Phase x Capacitor Voltages $V_{Cx,p}^{th}$			
	MFCI		LFCI	
	4-Cells (5-Levels)	6-Cells (7-Levels)	3-Cells (7-Levels)	4-Cells (15-Levels)
1	$V_{dc}/4$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/14$
2	$2V_{dc}/4$	$2V_{dc}/6$	$3V_{dc}/6$	$3V_{dc}/14$
3	$3V_{dc}/4$	$3V_{dc}/6$	~	$7V_{dc}/14$
4	~	$4V_{dc}/6$	~	~
5	~	$5V_{dc}/6$	~	~

Where x represents phase a, b and c
and p^{th} represents the placing position number of flying capacitor being clamped.

Since the voltage across Cx1 and Cx2 are now maintained at $1/6 V_{dc}$ and $3/6 V_{dc}$, the voltage stress across the six switches are no longer the same as compared to those in classical MFCI approach. The voltage stress across the switches is affected by the voltage differences between V_{Cx}^{th} and $V_{Cx(p-1)}^{th}$ using (5.8) and the switching states given in Table 5.1. Hence, the voltage stress across the respective switches is determined using (5.9).

$$V_{S_{x(cell n^{th})}}^{LFCI}(t) \approx \begin{cases} -\left(\frac{mL - 2^{(p^{th})}}{mL - 1}\right) V_{dc} \times S_{x(cell n^{th})}(t) & \text{if } cell n^{th} = 1 \\ -\left(\frac{2^{(p^{th})} - 2^{(p^{th}-1)}}{mL - 1}\right) V_{dc} \times S_{x(cell n^{th})}(t) & \text{if } cell n^{th} \geq 2 \end{cases} \quad (5.9)$$

Therefore, the voltage stress across the switches S_{x1} , S_{x2} and S_{x3} (V_{Sx1} , V_{Sx2} and V_{Sx3}) in 3-cell 7L-LFCI are approximately at $V_{dc}/2$, $V_{dc}/3$ and $V_{dc}/6$ respectively as shown in Fig. 5.9 with the dc voltage source of $300 V_{dc}$ supplied. According to the expression (5.9), it is worth noting that the blocking voltage capability of the two LF switches S_{x1} and S_{x1}' in Cell 1 must be able to withstand $V_{dc}/2$ for n -cell mL -LFCI at all times. The same amount of voltage stress also applies to its respective complimentary switches.

The output phase voltages and output line-to-line voltages for LFCI are expressed with (5.10) and (5.11) respectively based on the corresponding switching states in Table 5.1 and the flying capacitor voltages calculated using (5.8).

$$V_{xn}(t) = V_{dc}(t)(S_{x1}(t) - 0.5) + \sum_{m=2}^{n_{cells}} V_{Cx((P_{capacitors} + 2) - m)}(t)(S_{x(m)}(t) - S_{x(m-1)}(t)) \quad (5.10)$$

$$\begin{aligned}
\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix}_{mL} &= V_{dc}(t) \begin{bmatrix} (S_{a1}(t) - S_{b1}(t)) \\ (S_{b1}(t) - S_{c1}(t)) \\ (S_{c1}(t) - S_{a1}(t)) \end{bmatrix} \\
&+ \sum_{m=2}^{n_{cells}} V_{Cx((P_{capacitors}+2)-m)}(t) \begin{bmatrix} (S_{a(m)}(t) - S_{a(m-1)}(t) - S_{b(m)}(t) + S_{b(m-1)}(t)) \\ (S_{b(m)}(t) - S_{b(m-1)}(t) - S_{c(m)}(t) + S_{c(m-1)}(t)) \\ (S_{c(m)}(t) - S_{c(m-1)}(t) - S_{a(m)}(t) + S_{a(m-1)}(t)) \end{bmatrix}_{x \in \{a,b,c\}}
\end{aligned} \tag{5.11}$$

Both expressions of phase voltages (5.10) and line-to-line voltages (5.11) are also applicable for the classical n -cell mL -MFCI using PSC-PWM. The output voltages of both the classical 6-cell 7L-MFCI with PSC-PWM and the proposed 3-cell 7L-LFCI under the two advanced hybrid sinusoidal PWM schemes are shown in Figs. 5.14 and 5.15 respectively.

Fig. 5.14 Output phase voltages (top) and output line-to-line voltages (bottom) of classical 6-cell 7L-MFCI using PSC-PWM with $M_x = 0.9$ and $V_{dc} = 300V$.

Fig. 5.15 Output phase voltages (top) and output line-to-line voltages (bottom) of proposed 3-cell 7L-LFCI using (a) PSC-POD-PWM and (b) PSC-PD-PWM with $M_x = 0.9$ and $V_{dc} = 300V$.

However, one can observe that the overall switching frequency is greatly reduced for the proposed 3-cell 7L-LFCI employing the hybrid PWM schemes as compared to the classical 6-cell 7L-MFCI using PSC-PWM. The harmonic characteristics of both proposed hybrid PSC-POD-PWM and PSC-PD-PWM are detailed and analyzed in subsection 5.1.5 of this Chapter.

5.1.5 Harmonic Characteristics of Advanced Hybrid Sinusoidal PWM Schemes

In this Chapter, two hybrid sinusoidal carrier-based PWM schemes are proposed for the transformerless n -cell mL -LFCI namely PSC-POD-PWM and PSC-PD-PWM as described in Fig. 5.4. Both proposed modulation schemes greatly reduce the overall switching frequency operation by 50% as compared to the classical PSC-PWM modulation. These will be proven analytically in the following using the double Fourier series approach.

5.1.5.1 PSC Phase-Opposition-Disposition PWM (PSC-POD-PWM)

For the first proposed hybrid PSC-POD-PWM, same number of triangular carriers is required to achieve m -level modulation according to the same equation (3.2). As shown in the Fig. 5.4(a), half of the n_{tri} is level-shifted above the reference magnitude zero ($tri_{TOP(1,2,3,\dots,(n_{tri}/2))}$) while the other half is inverted (phase-opposition-disposition) and level-shifted below the reference magnitude zero ($tri_{BOT(1,2,3,\dots,(n_{tri}/2))}$).

It can be observed that the triangular carriers are phase-shifted away with one another instead of further level-shifting like those in POD-PWM. On top of that, the hybrid PSC-POD-PWM can avoid the complication of phase shifting carriers for higher mL output voltage as compared to PSC-PWM since only half of the n_{tri} are phase-shifted for both above and below the reference zero. Thus, the Δ_{phase} for both upper and lower triangular carriers is determined based on equation (5.3).

Fig. 5.16 Reference sinusoidal signal with two fundamental triangular carriers – PSC-POD-PWM.

The harmonic analysis of PSC-POD-PWM is simplified using single phase reference sinusoidal signal and two fundamental triangular carriers as shown in Fig. 5.16. The switching function of PSC-POD-PWM expressed in Table 5.3 can be derived based on the three-level modulation representation shown in Fig. 5.16. Thus, there are three conditions ($+V_{dc}$, $0V$ and $-V_{dc}$) generated according to the condition given in (3.1). The lower and upper boundaries for the transition conditions stated in Table 5.3 are determined by the equations (5.12) and (5.13) respectively.

$$x_{LOWER} = -\pi M \cos y \quad (5.12)$$

$$x_{UPPER} = \pi M \cos y \quad (5.13)$$

TABLE 5.3
SWITCHING FUNCTION OF PSC-POD-PWM

$f(x, y)$	$-\pi < x < 0$	$0 < x < \pi$
$+V_{dc}$	$M \cos y > -\frac{x}{\pi}$	$M \cos y > \frac{x}{\pi}$
0	$\frac{x}{\pi} < M \cos y < -\frac{x}{\pi}$	$-\frac{x}{\pi} < M \cos y < \frac{x}{\pi}$
$-V_{dc}$	$M \cos y < \frac{x}{\pi}$	$M \cos y < -\frac{x}{\pi}$

With the boundary conditions known, the equations (5.12) and (5.13) are substituted into the complex form of double Fourier integrals as expressed previously in equation (4.6). Thus, the complex form of double Fourier series for PSC-POD-PWM modulation is expressed in equation (5.14).

$$\begin{aligned}
 C_{mn} &= \frac{1}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} V_{dc} e^{j(mx+ny)} dx dy - \int_{-\pi}^{-\frac{\pi}{2}} \int_{\pi M \cos y}^{-\pi M \cos y} V_{dc} e^{j(mx+ny)} dx dy \right. \\
 &\quad \left. - \int_{\frac{\pi}{2}}^{\pi} \int_{\pi M \cos y}^{-\pi M \cos y} V_{dc} e^{j(mx+ny)} dx dy \right] \quad (5.14) \\
 &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx+ny)} dx dy \right]
 \end{aligned}$$

Based on the general spectrum analysis equation (4.5), the DC offset component of the PSC-POD-PWM can be determined with equation (5.15) by letting $m = n = 0$ in the equation (5.14).

$$\begin{aligned}
 A_{00} + jB_{00} &= \frac{V_{dc}}{2\pi^2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(0+0)} dx dy \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} [2\pi M \cos y] dy \quad (5.15) \\
 &= 0
 \end{aligned}$$

In order to determine the fundamental baseband component, let $m = 0$ and $n > 0$ for the equation (5.14). Thus, the baseband harmonic is determined based on equation (5.16).

$$\begin{aligned}
 A_{0n} + jB_{0n} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(ny)} dx dy \right] \\
 &= \frac{MV_{dc}}{\pi} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} [\cos y] e^{j(ny)} dy \\
 &= \frac{MV_{dc}}{2\pi} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} (e^{jy(n+1)} + e^{jy(n-1)}) dy
 \end{aligned} \tag{5.16}$$

In equation (5.16), the integral of the term $e^{j(ny)}$ is equal to zero for any non-zero condition of n . Since $A_{0n} + jB_{0n} = 0$ for all conditions when $n > 1$, therefore let $n = 1$ for the equation (5.16). Hence, the equation (5.16) can be further expressed with the equation (5.17).

$$\begin{aligned}
 A_{01} + jB_{01} &= \frac{MV_{dc}}{2\pi} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} (e^{jy(0)}) dy \\
 &= MV_{dc}
 \end{aligned} \tag{5.17}$$

The carrier harmonic components can be expressed in equation (5.18) by letting $m > 0$ and $n = 0$ for the equation (5.14).

$$\begin{aligned}
 A_{m0} + jB_{m0} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx)} dx dy \right] \\
 &= \frac{V_{dc}}{m\pi^2} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} 2 \sum_{k=1}^{\infty} \sin k \frac{\pi}{2} J_k(m\pi M) \cos ky dy \\
 &= 0
 \end{aligned} \tag{5.18}$$

Let $m > 0$ and $n \neq 0$ for the equation (5.14) to determine the sideband harmonic components which is derived as shown in equation (5.19).

$$\begin{aligned}
 A_{mn} + jB_{mn} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx+ny)} dx dy \right] \\
 &= \frac{V_{dc}}{m\pi^2} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} e^{jny} \left[2 \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \cos ky \right] dy \\
 &= \frac{V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} \left[e^{jy(n+k)} + e^{jy(n-k)} \right] dy \\
 &= \left(\frac{4V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \left[\frac{\pi}{2} \right]_{n=k} \right. \\
 &\quad \left. + \frac{4V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \left[\frac{\sin \frac{\pi}{2}(n+k)}{(n+k)} \right]_{-n \neq k} + \frac{\sin \frac{\pi}{2}(n-k)}{(n-k)} \left[\right]_{n \neq k} \right) \\
 &= \frac{2V_{dc}}{m\pi} J_n(m\pi M) \cos n\pi
 \end{aligned} \tag{5.19}$$

Substitute the equations (5.15), (5.17), (5.18) and (5.19) into equation (4.5) to achieve the spectrum analysis expression for the switching function in Table 5.3 which describes Fig. 5.16. The expression is shown in the equation (5.20).

$$\begin{aligned}
 f(t) &= \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_0) \\
 &\quad + \frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{m} J_n(m\pi M) \cos n\pi \times \cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_0])
 \end{aligned} \tag{5.20}$$

By observing the seven-level PSC-PWM modulation in Figs. 4.15(c) and 4.17(c) with the seven-level PSC-POD-PWM modulation in Fig. 5.17, it should be noted that the first group of sideband harmonics is being shifted away to 3 kHz from the fundamental baseband harmonic for PSC-POD-PWM instead of 6 kHz for the classical PSC-PWM. This is due to half the n_{tri} of PSC-POD-PWM is used in upper level-shifted (above the reference magnitude zero) and the other half for lower level-shifted (below the reference magnitude zero).

Therefore, the behavior of sideband harmonics phase-shifted in PSC-POD-PWM can be determined generally based on frequency (f_{shift}) or multiple of Harmonic Orderth which are redefined again in the equations (5.21) and (5.22) respectively.

$$f_{shift} = f_c \times \frac{n_{tri}}{2} \quad (5.21)$$

$$Harmonics\ Order^{th} = \frac{f_c \times n_{tri}}{2 \times f_o} \quad (5.22)$$

Hence, the final m -level output phase voltage spectrum expression for PSC-POD-PWM scheme is derived in equation (5.23).

$$\begin{aligned} V_{Xn_{PSCPODPWM-XL}}(t) = & \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_0) \\ & + \frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_{(2n-1)}((Nm)\pi M) \cos[(2n-1)\pi] \\ & \times \cos((Nm)[\omega_c t + \theta_c] + (2n-1)[\omega_o t + \theta_0]) \end{aligned} \quad (5.23)$$

where

N = half the total number of triangular carriers used in PSC-POD-PWM

Fig. 5.17 Voltage spectrum based on seven-level modulation PSC-POD-PWM.
(a) Output Phase Voltage. (b) Output Line-to-Line Voltage.

Based on the expression of equation (5.23), there are no existence of DC offset and carrier harmonic components. Thus, only fundamental baseband harmonic and sideband harmonics are created in PSC-POD-PWM. The sideband harmonics carry the term of $\cos[(2n-1)\pi]$ which shows that only odd sidebands are occurred at multiples of Harmonic Orderth based on equation (5.22). The equation (5.23) describes exactly the characteristic of output phase voltage for seven-level PSC-POD-PWM modulation in Fig. 5.17(a).

The numerical values of equation (5.23) are calculated for analytical results based on the seven-level modulation under the same condition of $M_{x\text{sine}} = 0.9$ and $f_c = 1$ kHz. The analytical results match similarly to the simulation results shown in Fig. 5.18(a). The experimental results are also obtained in Fig. 5.18(b) for the seven-level modulation. Once again, this proved that the theoretical analysis from the equation (5.23) describes exactly the characteristic of PSC-POD-PWM for any mL output phase voltage.

(a)

(b)

Fig. 5.18 Output phase voltage spectrum – seven-level PSC-POD-PWM modulation.
 (a) Simulation and Analytical Results. (b) Experimental Results.

The spectrum analysis of the output line-to-line voltage V_{ab} using PSC-POD-PWM method is determined with the equation (5.24).

$$\begin{aligned}
 V_{ab_{PSCPODPWM-xL}}(t) = & \frac{\sqrt{3}MV_{dc}}{2} \cos\left(\omega_o t + \frac{\pi}{6}\right) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \frac{1}{(Nm)} J_{(2n-1)}((Nm)\pi M) \cos[(2n-1)\pi] \sin\left((2n-1)\frac{\pi}{3}\right) \\
 & \times \cos\left((Nm)[\omega_c t] + (2n-1)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right)
 \end{aligned} \quad (5.24)$$

(a)

(b)

Fig. 5.19 Output line-to-line voltage spectrum – seven-level PSC-POD-PWM modulation.

(a) Simulation and Analytical Results. (b) Experimental Results.

Because of the three-phase power system, the crossover point between the two phase reference sinusoidal signals at every multiples of 60° cancels away all the triplen sideband harmonics only since there is no carrier harmonics existed in the output phase voltage. Thus, the same $\sin((2n-1) \pi/3)$ term is appeared in the sideband harmonics content of equation (5.24). The cancellation of the triplen sideband harmonics can be clearly observed in Fig. 5.17 between the output phase voltage and the output line-to-line voltage.

The analytical results of output line-to-line voltage for the seven-level PSC-POD-PWM modulation are obtained with the numerical calculation from the equation (5.24). The comparison between the analytical results and the simulation results is shown in Fig. 5.19(a). Besides that, experimental results are obtained in Fig. 5.19(b) as well to verify the characteristics of PSC-POD-PWM expressed in equation (5.24) for any mL output line-to-line voltage.

5.1.5.2 PSC Phase-Disposition PWM (PSC-PD-PWM)

Fig. 5.20 Reference sinusoidal signal with two fundamental level-shifted carrier – PSC-PD-PWM.

The derivation of the second proposed advanced hybrid PSC-PD-PWM (or alternatively equivalent to R-PSC-PD-PWM in Fig. 5.10) is the resulting combination of both LSC-PWM and PSC-PWM. Hence, the harmonic spectrum analysis for hybrid PSC-PD-PWM is simplified using the single phase reference sinusoidal signal and the two level-shifted fundamental triangular carriers in Fig. 5.20.

The switching function of PSC-PD-PWM is expressed in Table 5.4 which is derived based on Fig. 5.20. Since two fundamental level-shifted carriers are used in Fig. 5.20 for analysis, therefore there are only three conditions generated which are $+V_{dc}$, $0V$ and $-V_{dc}$ following the switching condition expressed in equation (3.1).

TABLE 5.4
SWITCHING FUNCTION OF PSC-PD-PWM

$f(x, y)$	$-\pi < x < 0$	$0 < x < \pi$
$+V_{dc}$	$M \cos y > -\frac{x}{\pi}$	$M \cos y > \frac{x}{\pi}$
0	$-1 - \frac{x}{\pi} < M \cos y < -\frac{x}{\pi}$	$-1 + \frac{x}{\pi} < M \cos y < \frac{x}{\pi}$
$-V_{dc}$	$M \cos y < -1 - \frac{x}{\pi}$	$M \cos y < -1 + \frac{x}{\pi}$

However, the boundary conditions for LSC-PWM (referred to PD-PWM) in this case are slightly more complex. Thus, the boundary conditions for the transitions between 0V to $+V_{dc}$ and $+V_{dc}$ to 0V are given in equations (5.25) and (5.26).

$$x_{LOWER} = -\pi M \cos y \quad (5.25)$$

$$x_{UPPER} = \pi M \cos y \quad (5.26)$$

In order to achieve $-V_{dc}$ level, the reference sinusoidal signal has to be lesser than both of upper and lower triangular carriers. Therefore, the boundary conditions for the transitions between 0V to $-V_{dc}$ and $-V_{dc}$ to 0V are given based on the upper carrier and lower carrier.

The lower and upper boundary conditions for this transition based on upper carrier are given in the equations (5.27) and (5.28) respectively.

$$x_{LOWER} = -\pi \quad (5.27)$$

$$x_{UPPER} = -\pi(1 + M \cos y) \quad (5.28)$$

While the lower and upper boundary conditions based on lower carrier are given in the equations (5.29) and (5.30) respectively.

$$x_{LOWER} = \pi(1 + M \cos y) \quad (5.29)$$

$$x_{UPPER} = \pi \quad (5.30)$$

The complex form of double Fourier analysis for PSC-PD-PWM modulation is expressed in equation (5.31) based on the boundary conditions equations given applied into the equation (4.6).

$$\begin{aligned}
 C_{mn} &= \frac{1}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} V_{dc} e^{j(mx+ny)} dx dy \right. \\
 &\quad \left. - \int_{-\pi}^{-\frac{\pi}{2}} \left[\int_{-\pi}^{-\pi(1+M \cos y)} V_{dc} e^{j(mx+ny)} dx + \int_{\pi(1+M \cos y)}^{\pi} V_{dc} e^{j(mx+ny)} dx \right] dy \right. \\
 &\quad \left. - \int_{\frac{\pi}{2}}^{\pi} \left[\int_{-\pi}^{-\pi(1+M \cos y)} V_{dc} e^{j(mx+ny)} dx + \int_{\pi(1+M \cos y)}^{\pi} V_{dc} e^{j(mx+ny)} dx \right] dy \right] \\
 &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi(1-M \cos y)}^{\pi(1+M \cos y)} e^{j(mx+ny)} dx dy \right]
 \end{aligned} \tag{5.31}$$

Again, the DC offset component can be determined with the equation (5.32) by letting $m = n = 0$ in the equation (5.31).

$$\begin{aligned}
 A_{00} + jB_{00} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(0+0)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi(1-M \cos y)}^{\pi(1+M \cos y)} e^{j(0+0)} dx dy \right] \\
 &= \frac{V_{dc}}{2\pi^2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} [2\pi M \cos y] dy + \frac{V_{dc}}{2\pi^2} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} [2\pi M \cos y] dy \\
 &= 0
 \end{aligned} \tag{5.32}$$

While the fundamental baseband component is determined with the equation (5.33) based on the condition $m = 0$ and $n > 0$. The equation (5.33) will experience the same

term $e^{j(ny)}$ during the integral process. The integral of the term $e^{j(ny)}$ will be equal to zero for any non-zero value of n . Therefore, n will be equal to 1 since $A_{0n} + jB_{0n} = 0$ for all conditions when $n > 1$. The expression is further simplified into equation (5.34).

$$\begin{aligned}
 A_{0n} + jB_{0n} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi(1-M \cos y)}^{\pi(1+M \cos y)} e^{j(ny)} dx dy \right] \\
 &= \frac{MV_{dc}}{\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} [\cos y] e^{j(ny)} dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} [\cos y] e^{j(ny)} dy \right] \quad (5.33) \\
 &= \frac{MV_{dc}}{2\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} (e^{jy(n+1)} + e^{jy(n-1)}) dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} (e^{jy(n+1)} + e^{jy(n-1)}) dy \right]
 \end{aligned}$$

$$\begin{aligned}
 A_{01} + jB_{01} &= \frac{MV_{dc}}{2\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} (e^{jy(0)}) dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} (e^{jy(0)}) dy \right] \quad (5.34) \\
 &= MV_{dc}
 \end{aligned}$$

The carrier harmonic components are determined with the equation (5.35) based on the condition of $m > 0$ and $n = 0$ for the equation (5.31).

$$\begin{aligned}
 A_{m0} + jB_{m0} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi(1-M \cos y)}^{\pi(1+M \cos y)} e^{j(mx)} dx dy \right] \\
 &= \frac{V_{dc}}{m\pi^2} 2 \sum_{k=1}^{\infty} \sin k \frac{\pi}{2} J_k(m\pi M) \left[\frac{2 \cos \frac{k \left(\frac{\pi}{2} - \frac{\pi}{2} \right)}{2} \sin \frac{k \left(\frac{\pi}{2} + \frac{\pi}{2} \right)}{2}}{k} \right. \\
 &\quad \left. + (e^{jm\pi}) \frac{2 \cos \frac{k \left(\frac{3\pi}{2} + \frac{\pi}{2} \right)}{2} \sin \frac{k \left(\frac{3\pi}{2} - \frac{\pi}{2} \right)}{2}}{k} \right] \\
 &= \frac{4V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \frac{\left(\sin \frac{k\pi}{2} \right)^2}{k} (1 - e^{jm\pi}) \quad (5.35)
 \end{aligned}$$

The term of $(\sin k\pi/2)^2$ in equation (5.35) is equal to non-zero solution if the value of k is odd. Hence, the term $(1 - e^{jm\pi})$ will be equal to 2 when the value of m is odd as well. Thus, the m must be an odd value at all times and the final expression for carrier harmonics is simplified into the equation (5.36).

$$A_{m0} + jB_{m0} = \frac{8V_{dc}}{\pi^2} \frac{1}{2m-1} \sum_{k=1}^{\infty} \frac{J_{2k-1}((2m-1)\pi M)}{2k-1} \quad (5.36)$$

Lastly, the sideband harmonics are defined by the equation (5.37) with the condition of $m > 0$ and $n \neq 0$ set for the equation (5.31).

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi M \cos y}^{\pi M \cos y} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi(1-M \cos y)}^{\pi(1+M \cos y)} e^{j(mx+ny)} dx dy \right] \\ &= \frac{V_{dc}}{m\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} e^{jny} \sin(m\pi M \cos y) dy + e^{jm\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} e^{jny} \sin(m\pi M \cos y) dy \right] \\ &= \frac{2V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \left[\frac{\pi}{2} \right]_{n=k} \\ &\quad + \frac{2V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} \left[\frac{\sin \frac{\pi}{2}(n+k)}{(n+k)} \right]_{-n \neq k} + \frac{\sin \frac{\pi}{2}(n-k)}{(n-k)} \left[\right]_{n \neq k} \\ &\quad + \frac{2V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} (e^{jm\pi}) \left[\frac{\pi}{2} \right]_{n=k} \\ &\quad + \frac{2V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_k(m\pi M) \sin k \frac{\pi}{2} (e^{jm\pi}) \left[-\frac{\sin \frac{\pi}{2}(n+k)}{(n+k)} \right]_{-n \neq k} - \frac{\sin \frac{\pi}{2}(n-k)}{(n-k)} \left[\right]_{n \neq k} \end{aligned} \quad (5.37)$$

Since k must be an odd value due to the term $(\sin k\pi/2)$ in equation (5.37) to determine a non-zero solution, therefore the value of n can only be an even value for the term $[\sin (\pi(n+k))/2]$. The equation (5.37) is further formulated as the equation (5.38).

$$A_{mn} + jB_{mn} = \frac{V_{dc}}{m\pi} \sum_{n=1}^{\infty} J_n(m\pi M) \sin n \frac{\pi}{2} (1 + e^{jm\pi}) - \frac{4V_{dc}}{m\pi^2} \sum_{k=1}^{\infty} J_{2k-1}(m\pi M) \left[\frac{(2k-1)\cos\left(\frac{n\pi}{2}\right)}{(n+(2k-1))(n-(2k-1))} \right]_{n \neq 2k-1} (1 - e^{jm\pi}) \quad (5.38)$$

Based on the exponential terms in (5.38), these terms will be further simplified when the conditions in equation (5.39) are met.

$$\begin{cases} (1 - e^{jm\pi}) = 2 & \text{if } m = \text{ODD} \\ (1 + e^{jm\pi}) = 2 & \text{if } m = \text{EVEN} \end{cases} \quad (5.39)$$

The final expression for the sideband harmonics is given in the equation (5.40).

$$A_{mn} + jB_{mn} = \frac{2V_{dc}}{\pi} \frac{1}{2m} \sum_{n=1}^{\infty} J_n(2m\pi M) \sin n \frac{\pi}{2} - \frac{8V_{dc}}{\pi^2} \frac{1}{2m-1} \sum_{k=1}^{\infty} J_{2k-1}((2m-1)\pi M) \left[\frac{(2k-1)\cos\left(\frac{n\pi}{2}\right)}{(n+(2k-1))(n-(2k-1))} \right]_{n \neq 2k-1} \quad (5.40)$$

The spectrum analysis for the switching function based on the two fundamental level-shifted carriers can be derived with the substitution of the equations (5.32), (5.34), (5.36) and (5.40) back into the equation (4.5). Due to the lengthy equation, the final expression after substitution will not be presented.

The phase-shifted of the carriers and sideband harmonics in the PSC-PD-PWM can be determined using the same equations (5.21) and (5.22) which are applied earlier on for PSC-POD-PWM methods.

The final expression for mL output phase voltage spectrum analysis based on PSC-PD-PWM scheme is given in equation (5.41).

$$\begin{aligned}
 V_{Xn_{PSCPD PWM-XL}}(t) = & \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_o) \\
 & + \frac{4V_{dc}}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{N(2m-1)} \sum_{k=1}^{\infty} \frac{J_{2k-1}(N(2m-1)\pi M)}{2k-1} \times \cos(N(2m-1)\omega_c t + \theta_c) \\
 & + \left(\frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{N(2m)} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} J_{2n-1}(N(2m)\pi M) \sin\left((2n-1)\frac{\pi}{2}\right) \right. \\
 & \quad \times \cos(N(2m)[\omega_c t + \theta_c] + (2n-1)[\omega_o t + \theta_o]) \\
 & \left. + \left(\frac{4V_{dc}}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{N(2m-1)} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} J_{2k-1}(N(2m-1)\pi M) \left[\frac{(2k-1)\cos\left(\frac{(2n)\pi}{2}\right)}{((2n)+(2k-1))((2n)-(2k-1))} \right] \right. \right. \\
 & \quad \left. \left. \times \cos(N(2m-1)[\omega_c t + \theta_c] + (2n)[\omega_o t + \theta_o]) \right] \right) \Bigg|_{n \neq 2k-1} \Bigg)
 \end{aligned} \tag{5.41}$$

where

N = the total number of triangular carriers used in PSC-PD-PWM

Fig. 5.21 Voltage spectrum based on seven-level modulation PSC-PD-PWM.
(a) Output Phase Voltage. (b) Output Line-to-Line Voltage.

Equation (5.41) describes that the output phase voltage based on PSC-PD-PWM carries only the fundamental baseband harmonic, carrier harmonics and sideband harmonics. Equation (5.41) shows that the carrier harmonics will occur only at odd multiples of Harmonic Orderth of equation (5.22). On top of that, even sideband harmonics occur around the odd multiples of Harmonic Orderth and odd sideband harmonics occur around the even multiples of Harmonic Orderth. The characteristics of output phase voltage for seven-level PSC-PD-PWM modulation in Fig. 5.21 is described exactly the same by equation (5.10).

(a)

(b)

Fig. 5.22 Output phase voltage spectrum – seven-level PSC-PD-PWM modulation.
 (a) Simulation and Analytical Results. (b) Experimental Results.

The analytical results are obtained based on the numerical values calculated from the equation (5.41) for the seven-level PSC-PD-PWM modulation with the same condition of $M_{x\text{sine}} = 0.9$ and $f_c = 1 \text{ kHz}$. The analytical results shown in Fig. 5.22(a) based on the theoretical description earlier on are matched with the simulation results shown in Fig. 5.21(a). On top of that, the experimental results have also verified the exact characteristic of carrier and sideband harmonics for PSC-PD-PWM derived with the analysis work.

The output line-to-line voltage V_{ab} spectrum analysis for PSC-PD-PWM is expressed with the following equation (5.42).

$$\begin{aligned}
 V_{ab_{PSCPD PWM-xL}}(t) = & \frac{\sqrt{3}MV_{dc}}{2} \cos\left(\omega_o t + \frac{\pi}{6}\right) \\
 & + \left(\frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{N(2m)} \right. \\
 & \left. + \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} J_{2n-1}(N(2m)\pi M) \sin\left((2n-1)\frac{\pi}{2}\right) \sin\left((2n-1)\frac{\pi}{3}\right) \right. \\
 & \left. \times \cos\left(N(2m)[\omega_c t] + (2n-1)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \right) \\
 & + \left(\frac{8V_{dc}}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{N(2m-1)} \right. \\
 & \left. + \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \sum_{k=1}^{\infty} J_{2k-1}(N(2m-1)\pi M) \left[\frac{(2k-1) \cos\left(\frac{(2n)\pi}{2}\right)}{((2n)+(2k-1))((2n)-(2k-1))} \right]_{n \neq 2k-1} \right. \\
 & \left. \times \cos\left(N(2m-1)[\omega_c t] + (2n)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \right) \sin\left((2n)\frac{\pi}{3}\right) \right)
 \end{aligned} \tag{5.42}$$

The crossover point between the two phase reference sinusoidal signals at every multiple of 60° will also cancel away the carrier harmonics and the triplen sideband harmonics by its nature. As a result, the term $\sin((2n-1)\pi/3)$ and $\sin((2n)\pi/3)$ are added in the equation (5.42) for the sideband harmonic components. Thus, the cancellation of both carrier and sideband harmonics can be clearly observed from output phase voltage in Figs. 5.21(a) and output line-to-line voltage in Fig. 5.21(b).

(a)

(b)

Fig. 5.23 Output line-to-line voltage spectrum – seven-level PSC-PD-PWM modulation
 (a) Simulation and Analytical Results. (b) Experimental Results.

The analytical results for the seven-level PSC-PD-PWM modulation based on the output line-to-line voltage are calculated with the equation (5.42). Once again, the analytical results are compared with the simulation results of Fig. 5.21(b) as shown in Fig. 5.23(a). Lastly, the experimental results in Fig. 5.23(b) have validated both the analytical and simulation results. Thus, the equation (5.42) has described exactly the characteristics of PSC-PD-PWM for any mL output line-to-line voltage.

5.1.6 Experimental Verification Results

The studies of both classical 6-cell 7L-MFCI using PSC-PWM and proposed 4-cell 7L-RFCI under PSC-PD-PWM are co-simulated between PSIM v9.0.4 Simcouple and MATLAB R2010b Simulink®. The hardware prototype has been developed to verify the results discussed previously with the aid of dSPACE RT1103 Real-Time Workshop (RTW). All results presented are based on the detailed settings given in Table 5.5.

The experimental harmonic spectrums of the two proposed hybrid PSC-POD-PWM and PSC-PD-PWM for the output phase voltages (Figs. 5.18 and 5.22) as well as the line-to-line voltages (Figs. 5.19 and 5.23) are closely matched with the mathematical harmonic characteristics analysis. Therefore, one can conclude that reduced overall switching frequency operation is achievable with the proposed modulation method for the modular cell converter.

Besides that, the inherent natural balancing of LFCI using the PSC-POD-PWM and PSC-PD-PWM is well maintained with the aid of RC balance booster filter. The synthesized output seven-level phase voltage stepped waveforms can be clearly observed from the Figs. 5.24(a) and 5.25(b) based on the hybrid PSC-POD-PWM and PSC-PD-PWM respectively, while the experimental output line-to-line voltages are shown in Figs. 5.24(b) and 5.25(b). The experimental results of 3-cell 7L-LFCI matched with the simulation results presented previously in Fig. 5.15. Hence, it could be clearly observed that there is slight difference in the magnitude of the synthesized output line-to-line voltages between the PSC-POD-PWM and PSC-PD-PWM as which the comparative evaluation of harmonic contents will be discussed later.

TABLE 5.5
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE OF 3-CELL 7L-LFCI

System Parameters	Settings
Reference Sinusoidal Frequency (f_o)	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz
Modulation Amplitude (M_a)	0.9
DC Voltage Source	300 Vdc
Flying Capacitors ($C_{p^{th}}$)	2200 μ F
Load – Resistors / Inductors	37.5 Ω / 40 mH
Filter – Resistors / Capacitors	4 Ω / 25 μ F

(a)

(b)

Fig. 5.24 Experimental results of 3-cell 7L-LFCI with PSC-POD-PWM modulation.
(a) Output Phase Voltages. (b) Output Line-to-Line Voltages.

(a)

(b)

Fig. 5.25 Experimental results of 3-cell 7L-LFCI with PSC-PD-PWM modulation.
(a) Output Phase Voltages. (b) Output Line-to-Line Voltages.

The agreement between simulation and experimental results has validated the feasibility of the proposed LFCI using the two advanced hybrid sinusoidal PWM modulation schemes. In addition to that, the aforementioned issues such as the high switching frequency operation of PSC-PWM and the increase flying capacitor energy storage that have restricted the classical MFCI for higher medium voltage drive applications are successfully overcome. Because of these advantageous features, the proposed LFCI can now be more attractively suitable for higher voltage applications where the space is a major concern.

5.1.7 Challenges Encountered for Proposed LFCI

The feasibility of the proposed LFCI under both hybrid PSC-POD-PWM and PSC-PD-PWM schemes was proven experimentally and also agreed with the presented simulation results based on its natural balancing capability at $0.9 M_{x_{sine}}$. Thus, the proposed LFCI is theoretically now more attractively suitable for higher voltage drive applications.

However, more research works are required to validate its performances in the event of the undesirable conditions so that the converter stability can be better analyzed. It is necessary to observe the flying capacitor voltages of the proposed LFCI especially during the under-modulation situations (where $M_{x_{sine}}$ is lesser than 0.67 for the 7L modulation). By doing so, the amount of charging and discharging period will be greatly affected by the pulse width of the gating signals since those pulses get broader when the $M_{x_{sine}}$ decreases. Consequently, these flying capacitor voltages may deviate away from its desired values, causing the converter to be unstable.

Fig. 5.26 Flying capacitor voltages (V_{Ca1} , V_{Ca2} , V_{Ca3} , V_{Ca4} and V_{Ca5}), output phase voltage (V_{an}) and currents (I_a , I_b and I_c) of proposed 6-cell 7L-MFCI based on $0.6 M_{x_{sine}}$.

Fig. 5.27 Flying capacitor voltages (V_{Ca1} and V_{Ca2}), output phase voltage (V_{an}) and currents (I_a , I_b and I_c) of proposed 3-cell 7L-LFCI based on $0.6 M_{x_{sine}}$ using (a) PSC-POD-PWM. (b) PSC-PD-PWM.

In this case with the $300 V_{dc}$ supplied, the performances of classical 6-cell 7L-MFCI under PSC-PWM and proposed 3-cell 7L-LFCI under the hybrid modulation schemes are evaluated in Figs. 5.26 and 5.27 respectively based on $0.6 M_{x_{sine}}$ (under-modulation condition). One can observe that the flying capacitor voltages of the classical 6-cell 7L-MFCI in Fig. 5.26 are remained balance following (4.2). On the

contrary, the flying capacitor voltages of the proposed 3-cell 7L-LFCI in Fig. 5.27 are not perfectly tracked and maintained at its desired values ($V_{Ca1} = V_{dc}/6 = 50$ V and $V_{Ca2} = V_{dc}/2 = 150$ V) according to the (5.8) even with the aid of balance booster filter. This is mainly due to the overly reduced switching states used for synthesizing the desired output phase voltages.

Hence, it is proven that the inherent natural balancing capability for the LFCI is restricted only to the normal modulating conditions ($M_{x_{sine}} > 0.67$). Moreover, poorer resolutions are found in the output voltages and current waveforms. As a result, higher losses are incurred as well. As such, a new alternative reduced modular cell converter named as reduced flying capacitor inverter (RFCI) is proposed to enhance the discussed performances of LFCI in the following Section 5.2 of this Chapter.

5.2 Reduced Flying Capacitor Inverter Topology

The proposed reduced flying capacitor inverter (RFCI) is designed to synthesize the output voltage levels doubly according to the number of series-connected modular cell (n_{cells}) as compared to the classical MFCI. Therefore, the number of output voltage levels for the RFCI can be determined with the following equation (5.43).

$$(mL)_{RFCI} = (2 \times n_{cells}) - 1 \quad (5.43)$$

It is clearly observed that the proposed approach (2-cell 3L-RFCI) also synthesizes the three-level output phase voltage using two modular cells, which is exactly the same as the classical 2-cell 3L-MFCI. However, the differences between the classical MFCI and the proposed RFCI would be obvious when producing higher mL output stepped voltage waveforms with every incremental modular cell implemented.

The key objectives of designing the proposed RFCI is to overcome the aforementioned issues faced in the classical MFCI such as (a) high switching frequency operation, (b) large inrush dc-link current, and (c) increase flying capacitor energy storage. On top of that, the RFCI also greatly enhanced the performances of LFCI as presented previously. The performance of the proposed RFCI using both hybrid PSC-POD-PWM and PSC-PD-PWM schemes is evaluated under dynamic conditions to verify its feasibility.

5.2.1 Generalized Structure of Reduced Flying Capacitor Inverter (RFCI)

Fig. 5.28 Proposed transformerless three-phase n -cell reduced modular cell inverter topology.

The general circuit configuration of transformerless three-phase modular cell inverter with reduced flying capacitors (RFCI) is shown in Fig. 5.28. Each modular cell consists a pair of semiconductor switches S_x including its complementary S_x' and a capacitor p clamped in between the cells. Hence, the number of switches i_{switches} and capacitors clamped $p_{\text{capacitors}}$ can be determined based on the number of modular cells (n_{cells}) used. The first pair of power switches S_{x1} and S_{x1}' in Cell 1 nearest to the dc-link is operating at low frequency of 50 Hz based on the modulating frequency (f_o) while the rest of the switches in Cell 2 to Cell n are operating at constant frequency depending on the carrier frequency (f_c).

Instead of having two LF switches served as an H-bridge leg like those in Fig. 5.1, the proposed RFCI clamps the series-connected modular cells (Cell 2 to Cell n) onto a low operational frequency cell (Cell 1). High modularity and flexibility are remained in the proposed RFCI converter. Thus, the proposed RFCI is allowed to synthesize higher mL output voltages easily by extending the n_{cells} .

Even though similarity is found between the proposed RFCI and the classical MFCI, but the number of component counts, cost and size of the converter are significantly

reduced with the proposed approach of clamping the modular cells onto a low frequency operated cell. The output voltage levels doubly increase with every incremental modular cell without the aid of any phase-shifted transformer. Moreover, lower and better output voltage harmonic distortion is also achieved.

5.2.2 Operating Principles of 4-Cell 7L-RFCI

By clamping three modular cells onto the low operational frequency Cell 1, it results a single-phase seven-level (7L) transformerless reduced flying capacitor inverter (RFCI) as presented in Fig. 5.29(a). Each phase-leg requires a minimum of 8 i_{switches} (S_{x1} to S_{x4} and S_{x1}' to S_{x4}') and 3 $p_{\text{capacitors}}$ (C_{x1} to C_{x3}) clamped in between the modular cells depending on the device voltage ratings considered during the design of the converter. It can be clearly observed that the total component counts are greatly reduced as compared to the classical 6-cell 7L-MFCI (12 i_{switches} and 5 $p_{\text{capacitors}}$ per phase-leg as shown in Fig. 5.29(b)). The difference would be even obvious when the converter is designed for three-phase systems.

Since four pairs of active switches are used in the proposed 4-cell 7L-RFCI, there is a combination of $2^4 = 16$ valid operating modes from '0000' to '1111' as summarized in Table 5.1. Two redundant states are produced for zero output level and three redundant states for each $\pm V_{dc}/3$ and $\pm V_{dc}/6$ output level. It should be noted that all positive output levels are achieved when S_{x1} conducts while all negative output levels are obtained when S_{x1}' conducts. Therefore, the two switches S_{x1} and S_{x1}' in Cell 1 are always performing at fundamental frequency of 50 Hz. Hence, the seven-level output phase voltage stepped waveforms are synthesized accordingly at $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$ and zero level based on the given corresponding switching states in Table 5.6.

Fig. 5.29 (a) Proposed 4-Cell 7L-RFCI. (b) Classical 6-Cell 7L-MFCI.

TABLE 5.6
4-CELL 7L-RFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States				Charging/Discharging States of Capacitors			Phase Leg xn Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	C_{x1}	C_{x2}	C_{x3}	V_{xn}
1	1	1	1	1				$+V_{dc}/2$
2	1	1	1	0	+			$+V_{dc}/3$
3	1	1	0	1	-	+		
4	1	1	0	0		+		$+V_{dc}/6$
5	1	0	1	1		-	+	$+V_{dc}/3$
6	1	0	1	0	+	-	+	$+V_{dc}/6$
7	1	0	0	1	-		+	
8	1	0	0	0			+	0
9	0	1	1	1			-	
10	0	1	1	0	+		-	$-V_{dc}/6$
11	0	1	0	1	-	+	-	
12	0	1	0	0		+	-	$-V_{dc}/3$
13	0	0	1	1		-		$-V_{dc}/6$
14	0	0	1	0	+	-		$-V_{dc}/3$
15	0	0	0	1	-			
16	0	0	0	0				$-V_{dc}/2$

Where x represents phase a, b and c

Logic '1' and '0' represent 'on' and 'off' state respectively

'+' and '-' represent the 'charging' and 'discharging' state of capacitors while '■' represents neither states.

Fig. 5.30 Proposed modulation technique for n -cell mL -RFCI.

The operational principles of proposed 4-cell 7L-RFCI are achieved using two proposed advanced hybrid sinusoidal PWM schemes named as phase-shifted carrier phase-opposition-disposition PWM (PSC-POD-PWM) and the phase-shifted carrier phase-disposition PWM (PSC-PD-PWM) as shown in Fig. 5.4. Generally, for all carrier-based PWM, $(mL - 1)$ number of triangular carriers (n_{tri}) would be required for any mL modulation scheme.

Similarly for 4-cell 7L-RFCI, six n_{tri} are used and divided into 2 sets equally where one set level-shifted above zero reference magnitude ($tri_{TOP(1,2,3)}$) and the other set below the zero reference magnitude ($tri_{BOT(1,2,3)}$). The top and bottom carriers are 120° phase-shifted evenly based on (5.3).

According to the switching states given in Table 5.6, S_{x1} and S_{x1}' are always low frequency operated switches with the frequency matching to the reference signal (Mx_{sine}). Thus, the final gating signals for S_{x1} and S_{x1}' are achieved directly by comparing Mx_{sine} with respect to zero magnitude as shown in Fig. 5.30. While for the remaining final gating signals, the 6 n_{tri} are compared with the Mx_{sine} respectively with the aid of simple comparators.

Fig. 5.31 Voltage stress across Sa1(top) to Sa4(bottom) for 4-cell 7L-RFCI based on hybrid PSC-PD-PWM with $M_x = 0.9$ and $V_{dc} = 300V$.

Thereafter, the output comparator signals of proposed advanced hybrid sinusoidal PWM schemes are further multiplied with S_{x1} and S_{x1}' through the AND logic gates to extract the desired modulated pulses from the respective positive and negative half-period of $M_{x\text{sine}}$. Finally, the modulated pulses after the AND gates are then summed together using the OR logic gates to achieve the desired gating signals for S_{x2} to S_{xn} . Hence, the gating signals for the complementary switches (S_x') are obtained simply through the NOT gates. The final gating signals achieved for 4-cell 7L-RFCI can be observed from Fig. 5.31 over two fundamental cycles period.

5.2.3 Voltage Characteristics Expressions

For the n -cell mL -RFCI, the voltage across the respective capacitor clamped at p^{th} position (C_{xp}^{th}) in Fig. 5.2 can be determined based on the following expression (5.44).

$$V_{C_{x(p^{th})}}^{RFCI} = \frac{p^{th}}{mL-1} \times V_{dc} \quad (5.44)$$

According to the (5.44), in the case of 4-cell 7L-RFCI, the flying capacitor voltages V_{Cx1} , V_{Cx2} and V_{Cx3} are maintained $V_{dc}/6$, $V_{dc}/3$ and $V_{dc}/2$ respectively during the steady-state operation. Even though (5.44) is expressed the same as the equation (4.2) which is used for determining the flying capacitor voltages of the classical MFCI, but there are two important factors to be taken note in Table 5.7. It can be clearly observed in the reduced number of flying capacitors and the voltage ratings. The proposed 4-cell 7L-RFCI does not only reduced the total number of flying capacitors but also reduced the flying capacitor voltage ratings as compared to the classical 4-cells 5L-MFCI.

TABLE 5.7
CAPACITOR VOLTAGES FOR CLASSICAL MFCI AND PROPOSED RFCI

Capacitors Clamped at p^{th} Position	Phase x Capacitor Voltages $V_{Cx,p}^{th}$			
	MFCI		RFCI	
	4-Cells (5-Levels)	6-Cells (7-Levels)	3-Cells (5-Levels)	4-Cells (7-Levels)
1	$V_{dc}/4$	$V_{dc}/6$	$V_{dc}/4$	$V_{dc}/6$
2	$2V_{dc}/4$	$2V_{dc}/6$	$2V_{dc}/4$	$2V_{dc}/6$
3	$3V_{dc}/4$	$3V_{dc}/6$	~	$3V_{dc}/6$
4	~	$4V_{dc}/6$	~	~
5	~	$5V_{dc}/6$	~	~

Where x represents phase a, b and c
and p^{th} represents the placing position number of flying capacitor being clamped.

The voltage stress across the switches of the proposed transformerless RFCI is highly affected by the flying capacitor voltages and is determined using (5.45). In the case of proposed 4-cell 7L-RFCI with 300 V_{dc} supplied, the voltage stress across the switches are shown in Fig. 5.6. It is observed that the voltage stress V_{Sx1} is V_{dc}/2, while the rest V_{Sx2}, V_{Sx3} and V_{Sx4} are equally distributed and maintained at V_{dc}/6. According to the expressions (5.44) and (5.45), the blocking voltage capability of the two low operational frequency switches S_{x1} and S_{x1}' in Cell 1 must be able to withstand V_{dc}/2 for *n*-cell *mL*-RFCI at all times. The same voltage stress calculated from (5.45) applies to the respective complimentary switches.

$$V_{Sx(\text{cell } n^{\text{th}})_{\text{RFCI}}}(t) \approx \begin{cases} -\left(\frac{(mL-1)-p^{\text{th}}}{mL-1}\right)V_{\text{dc}} \times S_{x(\text{cell } n^{\text{th}})}(t) & \text{if } \text{cell } n^{\text{th}} = 1 \\ -\left(\frac{p^{\text{th}}-(p^{\text{th}}-1)}{mL-1}\right)V_{\text{dc}} \times S_{x(\text{cell } n^{\text{th}})}(t) & \text{if } \text{cell } n^{\text{th}} \geq 2 \end{cases} \quad (5.45)$$

The same output phase voltage (5.10) and output line-to-line voltage expressions (5.11) are applied for RFCI respectively based on the corresponding switching states in Table 5.6 and the flying capacitor voltages obtained from (5.44). The output line-to-line voltages of 4-cell 7L-RFCI under the two proposed hybrid sinusoidal PWM schemes are shown in Figs. 5.32. One can observe that the overall switching frequency is greatly reduced for the proposed 4-cell 7L-RFCI employing the hybrid PWM schemes when compared to the classical 6-cell 7L-MFCI using PSC-PWM as shown previously in Fig. 5.14.

Fig. 5.32 Output phase voltages (top) and output line-to-line voltages (bottom) of proposed 4-cell 7L-RFCI using (a) PSC-POD-PWM and (b) PSC-PD-PWM with $M_x = 0.9$ and $V_{dc} = 300V$.

5.2.4 Design of Flying Capacitors

The critical flying capacitance value for the proposed n -cell mL -RFCI is estimated using (5.46):

$$C_{x,p^{th}(\text{critical})} \approx \frac{Mx_{\text{sine}} V_{\text{dc}}}{2 \times Z_L(j\omega) \times \Delta V_{C_{x,p^{th}}} \times f_{Os}} \approx \frac{\hat{I}_x \cos(\varphi)}{\Delta V_{C_{x,p^{th}}} \times f_{Os}} \quad (5.46)$$

where $x \in \text{phase } \{a,b,c\}$

p^{th} = position of the flying capacitors

Mx_{sine} = modulation index of phase $\{a,b,c\}$

$Z_L(j\omega)$ = complex load impedance

$\Delta V_{C_{x,p^{th}}}$ = permissible maximum peak-to-peak flying capacitor ripple voltage

f_{Os} = overall switching frequency (Hz)

$\hat{I}_x \cos(\varphi)$ = output peak phase $\{a,b,c\}$ current with power factor angle

The flying capacitance is inversely proportional to the overall switching frequency ($f_{Os} = n_{tri} \times f_c / 2$) as well as the maximum permissible flying capacitor ripple voltage ($\Delta V_{C_{x,p^{th}}}$). Due to the asynchronized gating signals, there are periods where the flying capacitors are connected in series with one another. It can be observed from the charging and discharging states of the flying capacitors corresponding to the particular switching state condition as shown in Table 5.8. This means that the amount of charging and discharging current (the effect of ripple current) for the respective capacitor depends on the series connection of the flying capacitors at that particular switching state condition of the converter.

TABLE 5.8
CHARGING AND DISCHARGING STATES OF FLYING CAPACITORS AND CORRESPONDING SWITCHING STATES

Switching States				Charging / Discharging States			Series Connection of Flying Capacitors
				I_{Cx1}	I_{Cx2}	I_{Cx3}	
0	0	0	0				
0	0	0	1	-			
0	0	1	0	+	-		C_{x1}, C_{x2}
0	0	1	1		-		
0	1	0	0		+	-	C_{x2}, C_{x3}
0	1	0	1	-	+	-	C_{x1}, C_{x2}, C_{x3}
0	1	1	0	+		-	C_{x1}, C_{x3}
0	1	1	1			-	
1	0	0	0			+	
1	0	0	1	-		+	C_{x1}, C_{x3}
1	0	1	0	+	-	+	C_{x1}, C_{x2}, C_{x3}
1	0	1	1		-	+	C_{x2}, C_{x3}
1	1	0	0		+		
1	1	0	1	-	+		C_{x1}, C_{x2}
1	1	1	0	+			
1	1	1	1				

Thus, the flying capacitor ripple current and ripple voltage are both having the same ripple frequency matching to the f_{os} . It should be noted that the critical flying capacitance value is affected by the desired permissible maximum peak-to-peak flying capacitor ripple voltages based on the f_{os} operation. Besides that, the critical flying capacitance value is also determined based on the peak magnitude of the output phase current ($\hat{I}_x$) which is affected by the power factor angle (φ) due to the output load impedance ($Z_L(j\omega)$). Therefore, it is important to select the flying capacitors appropriately by ensuring that both maximum ripple voltage and peak current must be lesser than the rated voltage and current ratings given by the manufacturer datasheet.

5.2.5 Experimental Verification Results

The studies of both classical 6-cell 7L-MFCI using PSC-PWM and proposed 4-cell 7L-RFCI under PSC-PD-PWM are co-simulated between PSIM v9.0.4 Simcouple and MATLAB R2010b Simulink®. The hardware prototype has been developed to verify the results discussed previously with the aid of dSPACE RT1103 Real-Time Workshop (RTW). All results presented are based on the detailed settings given in Table 5.9.

The experimental results as shown in Figs. 5.33 and 5.34 verified the feasibility of the proposed 4-cell 7L-RFCI based on the hybrid PSC-POD-PWM and PSC-PD-PWM respectively. The output seven-level phase voltage V_{an} (Figs. 5.33(a) and 5.34(a)) and output line-to-line voltage V_{ab} (Figs. 5.33(b) and 5.34(b)) are synthesized correspondingly with their frequency spectrum. The experimental harmonic spectrums of the synthesized output voltages have validated the analytical results in Figs. 5.18, 5.19, 5.22 and 5.23. Thus, one can conclude that reduced overall switching frequency by 50% is also achievable for the proposed RFCI with the two hybrid modulation schemes.

TABLE 5.9
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE OF 4-CELL 7L-RFCI

System Parameters	Settings
Reference Sinusoidal Frequency (f_o)	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz
Modulation Amplitude (M_a)	0.9
DC Voltage Source	300 Vdc
Flying Capacitors (C_{φ}^{th})	2200 μ F
Load – Resistors / Inductors	37.5 Ω / 40 mH
Filter – Resistors / Capacitors	4 Ω / 25 μ F

Fig. 5.33 Experimental results of 4-cell 7L-RFCI with PSC-POD-PWM modulation.
 (a) Output Phase Voltages (V_{an}). (b) Output Line-to-Line Voltages (V_{ab}).
 (c) Output Phase Currents (I_a , I_b and I_c).

Sinusoidal output currents are also achieved with low harmonic distortion as shown in Figs. 5.33(c) and 5.34(c) under the hybrid PSC-POD-PWM and PSC-PD-PWM schemes respectively.

Fig. 5.34 Experimental results of 4-cell 7L-RFCI with PSC-PD-PWM modulation.
 (a) Output Phase Voltages (V_{an}). (b) Output Line-to-Line Voltages (V_{ab}).
 (c) Output Phase Currents (I_a , I_b and I_c).

Moreover, the proposed 4-cell 7L-RFCI under the hybrid PSC-POD-PWM and PSC-PD-PWM is also evaluated with low modulation index of 0.3 M_a (under-modulation range) in Figs. 5.35 and 5.36. Despite of the under-modulation condition, the flying

capacitor voltages in Figs. 5.35(a) and 5.36(a) are remained balance at their desired voltage levels while the output line-to-line stepped voltage waveform is synthesized with lower voltage levels compared to the result in Figs. 5.33(b) and 5.34(b). In addition to that, the voltage stress across the switches Sa1, Sa2, Sa3 and Sa4 are kept constantly due to the balanced flying capacitor voltages as observed in Figs. 5.35(b) and 5.36(b). The results in Figs. 5.35 and 5.36 demonstrated that the inherent natural balancing property is well retained for the proposed RFCI with the aid of RC balance booster filter. Thus, it is proven that the second proposed RFCI approach has better converter stability even under low modulation condition as compared to the first proposed LFCI.

(a)

(b)

Fig. 5.35 Experimental results of 4-cell 7L-RFCI under 0.3 $M_{x\text{sine}}$ with PSC-POD-PWM.
(a) Output Line-to-Line Voltage (V_{ab}) and flying capacitor voltages (V_{Ca1} , V_{Ca2} , V_{Ca3}).
(b) Voltage Stress across Sa1 (V_{Sa1}), Sa2 (V_{Sa2}), Sa3 (V_{Sa3}) and Sa4 (V_{Sa4}).

(a)

(b)

Fig. 5.36 Experimental results of 4-cell 7L-RFCI under 0.3 $M_{x\text{sine}}$ with PSC-PD-PWM.
(a) Output Line-to-Line Voltage (V_{ab}) and flying capacitor voltages (V_{Ca1} , V_{Ca2} , V_{Ca3}).
(b) Voltage Stress across Sa1 (V_{Sa1}), Sa2 (V_{Sa2}), Sa3 (V_{Sa3}) and Sa4 (V_{Sa4}).

The agreement between the simulation and experimental results have confirmed the practicality of the proposed RFCI and also addressed the issues (a) to (c) faced in the classical MFCI. Therefore, the proposed RFCI synthesizes higher output voltage stepped waveforms with reduced component counts and costs. Besides that, the proposed RFCI has evidently enhanced the performances of the first proposed LFCI and improved the converter reliability as well. Hence, the RFCI is believed to be more attractively applicable for higher medium voltage drives compared to the classical MFCI and first proposed LFCI as well as for applications with space constraint.

5.3 Comparative Evaluation of Modular Cell Inverter Topologies

The classical MFCI is an attractive and interesting multilevel topology due to its single dc-link configuration without the worries of unbalanced dc-link voltage condition like MDCI and the need of bulky phase-shifted transformer in the MCHB. However, many challenges arise when higher mL output phase voltage is desired for MFCI. Hence, these issues have restricted its applicability for any high power systems.

The proposed reduced modular cell inverter topologies are designed to overcome these mentioned problems. The experimental results have proven the feasibility based on the two proposed hybrid SPWM methods. Therefore, it is important to carry out the comparative studies in order to verify the differences and improvements made between classical MFCI, proposed LFCI and RFCI.

The comparative studies will be discussed in the following subsection of this chapter, mainly based on the factors on (i) performances of modulation schemes, (ii) overall cost, size and weight, (ii) total energy storage of flying capacitors, (iii) pre-charge of flying capacitors, and (iv) power semiconductor losses. The overall performance of both classical and proposed modular cell inverters will be summarized again.

5.3.1 Performance Comparison of Classical and Proposed Modulation Schemes

The theoretical analysis and the validation of experimental results haven proven the feasibility of the proposed hybrid SPWM discussed earlier. Therefore, comparative studies are required to show the differences and improvements achieved as compared to the conventional SPWM methods. Comparative studies on the THD performances and the EMI risk factors are carried out based on two factors (i) modulation index (M_a) and (ii) overall switching frequency (f_s) respectively.

The output voltage quality can be determined using the THD performance, which is one of the requirements that the power electronic converters must comply with the IEEE Std 519-1992 as well as others. At the same time, the lower the THD of the output voltage achieved proves that lesser filtering effort is required; hence the output filter size can be further reduced. The THD can be determined based on the general expression shown in the equation (5.47).

$$\text{THD}(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100 \quad (5.47)$$

where

V_n = amplitude of the respective n^{th} harmonic

Since THD is calculated with the equation (5.47) which is solely based on the amplitude of the respective harmonic contents, therefore THD performances are not affected by f_c and f_s under the circumstance of same m -level modulation. Hence, the factor f_s is not considered for THD comparison in this case.

TABLE 5.10
COMPARISON OF THD PERFORMANCES BASED ON m -LEVEL MODULATION
 $M_a = 0.9, f_c = 1 \text{ kHz}$

m -Level Modulation	Output Phase Voltage	Output Line-to-Line Voltage
3L PSC-PWM	58.5278 %	48.1141 %
4L PSC-PWM	40.9258 %	34.3406 %
7L PSC-PWM	21.2544 %	17.4012 %
7L PSC-POD-PWM	21.3910 %	17.7293 %
7L PSC-PD-PWM	21.8122 %	15.2026 %

According to Table 5.10, as the m -level modulation increases, the THD of output voltages will decrease. Besides that, the THD for 7L output phase voltages are comparatively same despite of different modulation schemes implemented. However, the THD of output line-to-line voltage for 7L R-PSC-POD-PWM is observed to be much lower compared to other seven-level modulations. This proves that higher mL output voltage will achieve lower THD, thus higher mL multilevel converters are desired for high power applications.

To have a clear comparison, the detailed THD performances of output voltages are again evaluated for PSC-PWM, PSC-POD-PWM and PSC-PD-PWM in the following Figs. 5.37, 5.38 and 5.39 respectively. The results are obtained based on the following three conditions (i) M_a range from 0.1 to 1 (ii) 1 kHz of carrier frequency and (iii) m -Level modulation from 3L to 21L. Since the THD of 3L modulation is usually the highest and the THD of 21L modulation will be the lowest in this case, therefore both serve the boundary of highest and lowest THD for the comparison.

There are two aspects which can be observed from Figs. 5.37 to 5.39 regardless of any SPWM techniques used. Firstly, the THDs are incredibly high in the under-

modulation condition especially for lower mL output voltages. Secondly, as higher mL output voltage is achieved, the THD becomes constantly stable and smaller despite of any Ma range.

Fig. 5.37 PSC-PWM modulation – THD performances
(a) Output Phase Voltage (b) Output Line-to-Line Voltage
 $Ma = 0.1$ to 1.0 , $f_c = 1$ kHz, m -Level Modulation = 3L to 21L

Fig. 5.38 PSC-POD-PWM modulation – THD performances
(a) Output Phase Voltage (b) Output Line-to-Line Voltage
 $Ma = 0.1$ to 1.0 , $f_c = 1$ kHz, m -Level Modulation = 3L to 21L

Fig. 5.39 PSC-PD-PWM modulation – THD performances
(a) Output Phase Voltage (b) Output Line-to-Line Voltage
 $Ma = 0.1$ to 1.0 , $f_c = 1$ kHz, m -Level Modulation = 3L to 21L

The output phase voltage THD performances shown in Figs. 5.37(a), 5.38(a) and 5.39(a) are comparatively similar to each other. But there are great differences in the output line-to-line voltage THD performances as shown in Figs. 5.37(b), 5.38(b) and 5.39(b). Based on the worst case scenario (upper boundary of the graphs), both proposed hybrid SPWM methods have significantly better performances as compared to the conventional PSC-PWM. The proposed PSC-PD-PWM has the superior performances among the other two methods.

These can be explained with the analytical equations (5.41) and (5.42) derived for the PSC-PD-PWM. Even though the carrier harmonics do exist in the output phase voltage as compared to PSC-PWM and PSC-POD-PWM as shown in Fig. 5.40, but these carrier harmonics are cancelled out in the output line-to-line voltage (Fig. 5.41). On top of that, the amplitude of sideband harmonics in PSC-PD-PWM is insignificantly low according to the double summation of Bessel function coefficients carried in the equations.

In industrials and commercial buildings, the motors are always line-to-line voltage operated as high power can be achieved as compared to phase voltage operation. Hence, both the proposed hybrid SPWM methods are now more attractive for motor applications as compared to the conventional PSC-PWM strategy according to the results obtained in Figs. 5.37 to 5.39. Among the comparison for THD performance, PSC-PD-PWM is proven to have the superior performances.

As mentioned earlier, the conducted EMI is usually concerned with the range of the switching frequency operation between 10 kHz to 150 kHz. Thus, Ma in this case will

not be focused for EMI risk studies. The harmonic spectrums of the PSC-PWM, PSC-POD-PWM and PSC-PD-PWM for the output phase voltages and output line-to-line voltages are presented again in Figs. 5.40 and 5.41 respectively for clearer illustration. The results shown in both figures are based on the same carrier frequency of 1 kHz and modulation index of $0.9 M_{x_{\text{sine}}}$.

Fig. 5.40 Output phase voltage spectrum – seven-level modulation
 $Ma = 0.9, f_c = 1 \text{ kHz}$

Fig. 5.41 Output line-to-line voltage spectrum – seven-level modulation
 $Ma = 0.9, f_c = 1 \text{ kHz}$

Based on Figs. 5.40 and 5.41, the first group of carrier and sideband harmonics for the proposed hybrid SPWM methods are occurred at 60th harmonic order (which is around 3 kHz based on equation (5.22)). Meanwhile for the PSC-PWM, the first group of harmonics occurred at 120th harmonic order (which is around 6 kHz based on equation (4.20)).

In this case for seven-level modulation, the proposed hybrid SPWM methods have three sets of 1 kHz triangular carriers phase-shifted equally, while the conventional PSC-PWM has six sets of 1 kHz triangular carriers phase-shifted. This explains why first group of harmonics at the 60th order for proposed hybrid SPWM methods and 120th order for PSC-PWM. This shows that the overall switching frequency of the converter is greatly affected by the phase-shifted carriers.

This proves that phase-shifted carriers SPWM can help to reduce the output filter size as compared to LSC-PWM due to the thumb of rule theory and the resonant frequency of the filter as expressed in equation (3.4). But on the other side, the risk of generating EMI problems is higher. Therefore, if higher number of carriers is phase-shifted in any modulation strategies, the switching frequency of the converter will increase.

Since both proposed hybrid SPWM methods have reduced the number of phase-shifted carriers, the risk of generating EMI is reduced as the first group of carrier and sidebands harmonics are not shifted that much as compared to the PSC-PWM based on same m -level modulation. In order to conclude the study for EMI risk factor, the output voltage spectrums are plotted up to 20 kHz range in Figs. 5.42 and 5.43 so that the amplitude of the harmonics can be observed from 10 kHz onwards.

(a)

(b)

(c)

Fig. 5.42 Output phase voltage spectrum based on seven-level modulation
(a) PSC-PWM (b) PSC-POD-PWM (c) PSC-PD-PWM
 $M_a = 0.9, f_c = 1 \text{ kHz}$

(a)

(b)

(c)

Fig. 5.43 Output line-to-line voltage spectrum based on seven-level modulation
 (a) PSC-PWM (b) PSC-POD-PWM (c) PSC-PD-PWM
 $M_a = 0.9, f_c = 1 \text{ kHz}$

In terms of THD performance for seven-level modulations presented previously, the three SPWM methods have comparatively same results. But in terms of f_s now, the amplitude of the harmonics in PSC-PWM is the highest especially from 10 kHz onwards and the harmonics are much denser compared to the two proposed hybrid SPWM methods as shown in Fig. 5.42. While the harmonic components in PSC-PD-PWM are less dense compared to those in PSC-POD-PWM.

Similar results can be observed for the output line-to-line voltage shown in Fig. 5.43. Therefore, both Figs 5.42 and 5.43 have proven that the smaller EMI filter size can be achieved for both hybrid SPWM methods, especially PSC-PD-PWM. This is because since lesser effort is required to filter those less dense and insignificantly small amplitude of harmonic spectrum from 10 kHz onwards.

The comparison for the PSC-PWM and the two proposed hybrid SPWM has been summarized again in Table 5.11. The theoretical analysis of the proposed hybrid SPWM has been verified and yet again proven their respective performances in achieving better voltage quality.

TABLE 5.11
PERFORMANCE COMPARISON OF PSC-PWM, PSC-POD-PWM AND PSC-PD-PWM
BASED ON SEVEN-LEVEL MODULATION
Ma = 0.9, $f_c = 1$ kHz

Performances	PSC-PWM	PSC-POD-PWM	PSC-PD-PWM
V_{xn} THD	21.2544 %	21.3910 %	21.8122 %
V_{ab} THD	17.4012 %	17.7293 %	15.2026%
n_{tri}	6	6	6
f_s	6 kHz	3 kHz	3kHz
ω_f	2.4 kHz	1.2 kHz	1.2 kHz
EMI Risk Factor	High	Medium	Medium

The first proposed PSC-POD-PWM achieves similar THD performances as those in the conventional PSC-PWM. Even though same number of n_{tri} are used, but the proposed PSC-POD-PWM reduces the overall switching frequency, thus the risk of generating EMI is lower also. Besides that, the complication of phase-shifted and level-shifted is avoided with higher n_{tri} as compared to POD-PWM and PSC-PWM.

Whereas the second proposed PSC-PD-PWM achieves even better results in terms of output line-to-line THD performances and also lesser n_{tri} is required compared to the other methods. The issue of EMI can also be even avoided since the overall switching frequency is reduced as well. The proposed PSC-PD-PWM is concluded to have superior performances among the other SPWM methods.

The output filter size of both proposed hybrid SPWM methods may not be able to reduce much as compared to PSC-PWM, but will be definitely much smaller when compared to LSC-PWM. However, most importantly both hybrid SPWM methods have overcome the problems of LSC-PWM and PSC-PWM such as under-modulation condition and issues of EMI mentioned earlier on. The comparative results presented have proven that the proposed hybrid SPWM methods have successfully attained the respective advantageous properties.

Hence, both hybrid SPWM schemes could be more attractive for high power applications now as compared to the PSC-PWM which is popularly used in the industrials and applied for many multilevel converter topologies. Especially the proposed PSC-PD-PWM could be more recommendable for motor applications due to its lowest output line-to-line voltage THD performances.

5.3.2 Component Counts, Cost and Size

Fig. 5.44 Comparison of total component counts and output phase voltage levels

One of the challenges for multilevel converter is the increment of components required to achieve for higher mL output voltages. Especially the size and the weight of the overall converter will be major concerns for applications with space constraints. Electrolytic capacitors are one of the principle components which are commonly used in all converters be it any topologies design. However, electrolytic capacitors usually occupy the most space in power electronic converters. Particularly for MFCI topology, the output voltage levels are synthesized based on the voltage across those flying capacitors. Hence, the increase of mL output voltage for classical MFCI will lead to a huge increase in number of capacitors and semiconductor devices.

The classical MFCI synthesizes the output voltage levels linearly using (4.1), while the output phase voltage levels are increased exponentially in (5.1) for proposed LFCI and doubly in (5.43) for proposed RFCI with the incremental n_{cells} implemented. The number of voltage levels based on the n_{cells} for MFCI, LFCI and RFCI can be observed clearly in Fig. 5.44. This also proves that LFCI is no longer affected by the total number of components required to achieve higher mL output phase voltages.

Fig. 5.45 Comparison of total component counts and amount of reduction achieved.

The amount of reduction in terms of percentage (%) achieved by both proposed LFCI and RFCI using the advanced hybrid sinusoidal carrier-based PWM schemes as compared to the classical MFCI can be determined with (5.48) and (5.49) respectively based on the mL output phase voltage.

$$\Delta Components_{LFCI}(\%) = \frac{3 \left[\frac{((mL)-1)\log(2) - \log((mL)+1)}{\log(2)} \right]}{[3(mL)-4]} \times 100\% \quad (5.48)$$

$$\Delta Components_{RFCI}(\%) = \frac{3(mL)-9}{6(mL)-8} \times 100\% \quad (5.49)$$

Since the overall cost, size and weight of the converter are closely related to one another due to the total number of components needed, the amount of reduction that LFCI and RFCI can achieved is compared with MFCI is shown in Fig. 5.45 based on the same number of output phase voltage levels. In this case, the proposed 3-cell 7L-LFCI and 4-cell 7L-RFCI achieve a reduction of 52.9412% and 35.2941% respectively as compared to classical 6-cell 7L-MFCI. The difference becomes larger when the n_{cells} increases by using both proposed reduced modular cell approaches.

5.3.3 Flying Capacitors Total Energy Storage

With the demand of achieving higher mL output voltage levels, the number of flying capacitors in classical MFCI approach will be greatly increased as shown in Fig. 5.45. Eventually, the total amount of energy storage in these flying capacitors for MFCI will increase as well.

Higher amount of energy storage in the power electronic converters will incur higher losses during the process of power conversion. The increase in energy storage will also affect the capacitors charging time which means longer period is required for the power converter to reach its steady-state condition. Moreover, capacitors have the lowest reliability compared to other components used in the power electronic converters due to its lifetime cycle. Hence, the overall reliability of the converter is significantly improved based on the proposed LFCI and RFCI approach.

The total amount of energy storage for LFCI can be calculated based on (5.50) while classical MFCI and proposed RFCI share the same expression (5.51). In this case, the total amount of energy storage in the proposed 3-cell 7L-LFCI and 4-cell 7L-RFCI are reduced by 81.82% and 74.55% respectively as compared to the classical 6-cell 7L-MFCI due to the reduced flying capacitors and the voltage ratings of these capacitors.

$$W_{\text{total(LFCI)}} = \sum_{p=1}^{n_{\text{cells}}-1} \frac{C_{x,p}^{\text{th}}}{2} \left(\frac{\left(2^{(p^{\text{th}})} - 1 \right) \times V_{\text{dc}}(t)}{(mL) - 1} \right)^2 \quad (5.50)$$

$$W_{\text{total(MFCI/RFCI)}} = \sum_{p=1}^{n_{\text{cells}}-1} \frac{C_{x,p}^{\text{th}}}{2} \left(\frac{(p^{\text{th}}) \times V_{\text{dc}}(t)}{(mL) - 1} \right)^2 \quad (5.51)$$

5.3.4 Pre-Charge of Flying Capacitors

The process of initializing the capacitor charge is a complicated matter, which usually leads to large in-rush current during the transient period. Thus, it may over-stress the semiconductor devices of the converter. As a result, an additional pre-charge circuit is required to avoid the large initial peak current during the split second of starting up the power converter directly. Alternatively, the pre-charging issue can also be solved by slow starting-up the converter instead of having an additional circuit. This explains why the classical MFCI is not so popularly implemented in the industrial applications yet, as compared to those NPC and MCHB topologies used for high power applications.

Fig. 5.46 Transient dc-link current.

The transient dc-link current of the classical MFCI and both the proposed RFCI and LFCI is shown in Fig. 5.46. The results are obtained without any pre-charge circuit and have evidently proven that the transient peak current of the proposed 4-cell 7L-RFCI and 3-cell 7L-LFCI are significantly reduced by approximately 44% compared to both classical MFCI in terms of same output voltage levels synthesized or same number of modular cells implemented.

The transient peak current is reduced with the aid of two low operational frequency switches S_{x1} and S_{x1}' in the Cell 1 based on the advanced hybrid modulation schemes (PSC-POD-PWM and PSC-PD-PWM). These two switches function as slow start-up for the RFCI and LFCI converters by allowing more time for the flying capacitors to charge. Hence in this case, the size and design of the pre-charge circuit can be further optimized for the proposed transformerless RFCI and LFCI.

5.3.5 Power Semiconductor Device Losses

Fig. 5.47 Comparison of per phase-leg losses in classical MFCI, proposed RFCI and proposed LFCI.

The total distributed losses (total switching loss and total conduction loss) of per phase-leg discrete components shown in Fig. 5.47 are obtained based on the low rated power condition given in Tables 5.5 and 5.9. The loss comparison is evaluated between the classical MFCI, the proposed LFCI and the proposed RFCI under the hybrid modulation schemes based on the same number of modular cells and the same number of synthesized output phase voltage levels.

The results clearly showed that the lowest total loss is experienced in the proposed 3-cell 7L-LFCI followed by the second proposed 4-cell 7L-RFCI. The total distributed losses in both proposed LFCI and RFCI configuration are notably decreased mainly because of the reduced number of component counts as well as the reduced flying capacitor voltages. Therefore, one can conclude that the proposed reduced modular cell inverter topologies (LFCI and RFCI) under the advanced hybrid sinusoidal carrier-based PWM schemes (PSC-POD-PWM and PSC-PD-PWM) feature higher efficiency than the classical MFCI using PSC-PWM.

5.3.6 Overall Performances

The performances of the classical 6-cell 7L-MFCI as well as the proposed 3-cell 7L-LFCI and 4-cell 7L-RFCI are summarized in Table 5.12. The two proposed reduced modular cell inverters have greatly reduced the overall cost, size and weight compared to the classical MFCI approach. Moreover, the reduction of total energy storage of flying capacitors allows both LFCI and RFCI to reach its steady-state condition faster which also result an increased in the overall reliability of the converter.

Large in-rush current during the transient period of starting up the converter can now be avoided for the proposed LFCI and RFCI due to the low frequency operated pair of switches S_{x1} and S_{x1}' involved in the converter design. Hence, the design and the size of the pre-charge circuit could be simplified or further reduced.

TABLE 5.12
OVERALL PERFORMANCES BASED ON SEVEN-LEVEL MODULAR CELL INVERTERS

Performances	6-cell 7L-MFCI	4-cell 7L-RFCI	3-cell 7L-LFCI
Modulation Schemes	PSC-PWM	PSC-POD-PWM PSC-PD-PWM	PSC-POD-PWM PSC-PD-PWM
No. of Switches (Single-phase / Three-phase)	(12 / 36)	(6 / 18)	(6 / 18)
No. of Capacitors (Single-phase / Three-phase)	(5 / 15)	(2 / 6)	(2 / 6)
Cost, Size and Weight	Expensive, Bulky and Heavy	Cheaper and Smaller	Cheaper, Smaller and Lighter
Design Complexity	High	Medium	Low
Overall Switching Frequency (kHz)	6 kHz	3 kHz	3 kHz
Semiconductor Losses	High	Medium	Low
Device Voltage Stress	Equal	High (S_{x1} and S_{x1}') Equal (Remaining)	Unequal
Flying Capacitor Voltage Ratings	High	Low	Lowest

However, it is clearly noted that the limitation of LFCI is the case of under-modulation condition which leads to poorer power efficiencies due to its unbalanced flying capacitor voltages even though under-modulation operation is typically avoided in many applications. This is caused by the overly reduced number of redundant switching states.

As such, this explains the motivation to design the second RFCI to overcome the challenge faced in the first proposed LFCI. It is experimentally proven that natural balancing is inherited in the RFCI even in the case of under-modulation unlike the LFCI, thus increases the stability and reliability of the converter. Even though the design of RFCI requires additional switches and flying capacitors compared to LFCI, but RFCI has also successfully overcome all the challenges faced in designing the classical MFCI for higher medium voltage drives as evidenced in this Section 5.3 – Comparative Evaluation of Modular Cell Inverter Topologies.

The two proposed hybrid SPWM schemes (PSC-POD-PWM and PSC-PD-PWM) are investigated as well. According to the analyzed harmonic characteristics, both modulation schemes allow the LFCI and RFCI to achieve better performances. Hence, the issues of EMI can be avoided due to the reduction of overall switching frequency. Furthermore, the proposed PSC-PD-PWM scheme can alternatively allow the design of converter to be even simpler with carriers being further reduced (R-PSC-PD-PWM) for the modulation technique which is achieved by rebuilding the command reference sinusoidal signal ($M_{x_{sine}}$). On top of that, better output line-to-line voltage quality is produced which is beneficial for the motor applications.

The enhanced performances achieved by the proposed reduced modular cell inverters allow them to be more applicable for higher power applications, since good output voltage quality can be achieved with lower switching frequency. Therefore, the need of filter size can be further reduced, which in return allows lower production cost, lower maintainability and lighter weight for the converter. As a result, the overall system reliability is increased also.

The proposed LFCI and RFCI approaches are also attractively suitable for many applications where space constraint is major concern especially in those transportation industries such as traction drives, electric vehicles or even in more electric aircraft. They can also be retrofitted into rectifier mode for those grid-connected applications with unity power factor performance.

5.4 Proposed Flying Capacitor Voltage Balancing Control for RFCI

Since the pole voltage waveforms of the proposed RFCI are synthesized accordingly depending on the flying capacitor voltages, therefore it is important to ensure that the voltage across the respective flying capacitor must be tracked to their desired reference values based on the given (5.44) at all times. In the event of unbalanced flying capacitor voltages, there will be an increase in the voltage stress on the power semiconductors and affect the stability of the entire system. Even though this issue can be resolved easily by oversizing the component ratings, but it is not a cost-effective solution.

Such undesirable conditions can be prevented with the aid of balance booster filter implemented because of the well-retained inherent natural balancing of flying capacitor voltages in the proposed RFCI as presented previously. However, the converter may take longer time to response and stabilize for any dynamic conditions. Alternatively, a closed-loop flying capacitor voltage balancing control is designed for the proposed n -cell mL -RFCI in Fig. 5.48 using the hybrid PSC-PD-PWM scheme.

Fig. 5.48 Proposed flying capacitor voltage balancing control with modulation logic gate signals.

Since the voltage across the flying capacitors depends on the current through the respective capacitors as expressed in (5.52) and is affected by the switching states of the two adjacent switches, therefore the flying capacitor voltages can be balanced by varying the duty ratios of the switching pulses.

$$C_{x,p^{th}} \times \frac{dV_{C_{x,p^{th}}}}{dt} = I_{C_{x,p^{th}}}(t) = \left(S_{x(n-p^{th}+1)} - S_{x(n-p^{th})} \right) I_x \quad (5.52)$$

The flying capacitor voltage dynamic in (5.53) is expressed in a local average form over a switching period using duty ratio instead of switching states.

$$\frac{\Delta \bar{V}_{C_{x,p^{th}}}}{\Delta t} = \frac{\left(\Delta d_{x(n-p^{th}+1)} - \Delta d_{x(n-p^{th})} \right) \bar{I}_x}{C_{x,p^{th}}} \quad (5.53)$$

Thus, the flying capacitor voltages can be regulated by varying the duty ratios of the switching pulses based on the voltage errors between the reference voltage ($\epsilon_{x(n)}$) in Table 5.7 and the measured values. These voltage errors are then minimized using a proportional (P) controller which allows simple implementation as well as easy tuning of the gain to achieve the desired performance.

$$\Delta d_{x(n)} = \text{sign}(I_x) \left(\epsilon_{x(n-1)} - \epsilon_{x(n)} \right) P \quad (5.54)$$

Besides that, the duty cycle ratios are also varied depending on the directional flow of the phase current which is defined as 1 and -1 for the respective positive and negative cycle using the sign term. The varied duty ratios will then be added to the reference

sinusoidal signal (M_{Xsine}) to achieve the modulation sine templates ($M_{Xsine(n)}$) which are required for the proposed hybrid PSC-PD-PWM scheme as shown in Fig. 5.4(b).

For the case of 4-cell 7L-RFCI, a total of six triangular carriers will be divided equally into two sets where one set is level-shifted above zero reference magnitude ($tri_{TOP(1,2,3)}$) and the other set remains in-phase and level-shifted below zero reference magnitude ($tri_{BOT(1,2,3)}$). Both the top and bottom carriers are 120° phase-shifted apart evenly according to (5.3).

Based on the switching states given in the Table 5.6, the switches S_{x1} and S_{x1}' are low frequency operated switches with the frequency matching to the $M_{Xsine(n)}$. Hence, the final gating signals for S_{x1} and S_{x1}' are obtained directly by comparing $M_{Xsine(1)}$ with respect to zero magnitude as shown in the Fig. 5.48. The remaining gating signals are achieved by comparing $M_{Xsine(2,3,4)}$ respectively with six triangular carriers $tri_{TOP(1,2,3)}$ and $tri_{BOT(1,2,3)}$ using simple comparators. The output comparator signals will be further multiplied with S_{x1} and S_{x1}' through the AND logic gates to extract the desired modulation signals from the respective positive and negative half cycle of the $M_{Xsine(n)}$. Thereafter, the extracted modulating pulses after the AND gates are summed together using the OR logic gates to achieve the final gating signals for S_{x2} to S_{xn} . Thus, the complementary switches are simply obtained using the NOT gates. The overall voltage balancing control using the hybrid PSC-PD-PWM for the proposed 4-cell 7L-RFCI is shown in Fig. 5.48 which can be extended for any n -cell mL -RFCI configuration as well.

5.4.1 Experimental Verification Results

The dynamic performances of the 4-cell 7L-RFCI are evaluated with a series of step changed in the modulation index ($M_{x\text{sine}<\text{rectifier}>}$) and with the unbalanced load conditions to verify the feasibility of the proposed voltage balancing control. The detailed configuration settings for both simulation and experimental results are presented based on Table 5.13.

The proposed 7L-RFCI in Fig. 5.28 is simulated to have the modulation index step changed from 0.9 M_x to 0.3 M_x between $t = 2\text{s}$ to 2.1s and 0.9 M_x to 0.6 M_x between $t = 2.3\text{s}$ to 2.4s as shown in Fig. 5.49(a). Meanwhile, an unbalanced load condition is occurred during $t = 2.15\text{s}$ to 2.25s when the two series-connected RL of $25\ \Omega$ 100 mH and $100\ \Omega$ 100 mH are connected respectively to Phase B and C. The flying capacitor voltages of 7L-RFCI in Fig. 5.49(b) are observed to be well maintained constant at their corresponding levels even in the events of drastic M_x change and the introduction of unbalanced load condition.

TABLE 5.13
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE
OF 4-CELL 7L-RFCI

System Parameters	Settings
Reference Sinusoidal Frequency (f_o)	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz
Flying Capacitors ($C_{\text{sp}}^{\text{th}}$)	2200 μF
DC Voltage Source	170 Vdc
Load – Resistors / Inductors	37.5 Ω / 40 mH
Filter – Resistors / Capacitors	4 Ω / 25 μF

Fig. 5.49 Simulated dynamic performance of 4-cell 7L-RFCI with $M_{x\text{sine}}$ variation and unbalanced load change.

(a) Output currents. (b) Output phase voltage and flying capacitor voltages.

The feasibility of the proposed 7L-RFCI in conjunction with the flying capacitor voltage balancing control is also validated according to the same condition presented in the simulation. The steady-state performances of the inverter operating at 0.9 Mx, 0.6 Mx and 0.3 Mx are shown in Figs. 5.50 to 5.55. The seven-level pole voltage (V_{an}) waveform is synthesized with reduced number of flying capacitors and capacitor voltage ratings as clearly observed from Fig. 5.50. Besides that, the dynamic performances of the 7L-RFCI are experimented with the sudden step change in the Mx and the unbalanced load conditions which are presented in Figs. 5.56 to 5.61. It should be noted that the flying capacitor voltages are also experimentally proven to be balanced.

The strong agreements between the simulation results and the experimental results have proven the feasibility of the proposed RFCC with reduced component counts. Good dynamic responses using the closed-loop voltage balancing control are achieved as well.

(a)

(b)

Fig. 5.50 Results of 4-Cell 7L-RFCI with 0.9 $M_{x\text{sine}}$ performance based on output currents (I_a , I_b and I_c) and output phase voltage (V_{an}).

(a) Simulation results. (b) Experimental results.

(a)

(b)

Fig. 5.51 Results of 4-Cell 7L-RFCI with 0.9 $M_{x\text{sine}}$ performance based on output phase voltage (V_{an}) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}).

(a) Simulation results. (b) Experimental results.

Fig. 5.52 Results of 4-Cell 7L-RFCI with 0.6 $M_{x\text{sine}}$ performance based on output currents (Ia, Ib and Ic) and output phase voltage (Van).
 (a) Simulation results. (b) Experimental results.

Fig. 5.53 Results of 4-Cell 7L-RFCI with 0.6 $M_{x\text{sine}}$ performance based on output phase voltage (Van) and flying capacitor voltages (VCa1, VCa2 and VCa3).
 (a) Simulation results. (b) Experimental results.

(a)

(b)

Fig. 5.54 Results of 4-Cell 7L-RFCI with 0.3 $M_{x\text{sine}}$ performance based on output currents (Ia, Ib and Ic) and output phase voltage (Van).

(a) Simulation results. (b) Experimental results.

(a)

(b)

Fig. 5.55 Results of 4-Cell 7L-RFCI with 0.3 $M_{x\text{sine}}$ performance based on output phase voltage (Van) and flying capacitor voltages (V_{Ca1}, V_{Ca2} and V_{Ca3}).

(a) Simulation results. (b) Experimental results.

Fig. 5.56 Results of 4-Cell 7L-RFCI with modulation index step change from 0.9 to 0.6 $M_{x_{sine}}$ based on output currents (I_a , I_b and I_c) and output phase voltage (V_{an}).
(a) Simulation results. (b) Experimental results.

Fig. 5.57 Results of 4-Cell 7L-RFCI with modulation index step change from 0.9 to 0.6 $M_{x_{sine}}$ based on output current (I_a) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}).
(a) Simulation results. (b) Experimental results.

Fig. 5.58 Results of 4-Cell 7L-RFCI with modulation index step change from 0.9 to 0.3 $M_{x_{sine}}$ based on output currents (I_a , I_b and I_c) and output phase voltage (V_{an}).

(a) Simulation results. (b) Experimental results.

Fig. 5.59 Results of 4-Cell 7L-RFCI with modulation index step change from 0.9 to 0.3 $M_{x_{sine}}$ based on output current (I_a) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}).

(a) Simulation results. (b) Experimental results.

Fig. 5.60 Results of 4-Cell 7L-RFCI with unbalanced load change based on output currents (Ia, Ib and Ic) and output phase voltage (Van). (a) Simulation results. (b) Experimental results.

Fig. 5.61 Results of 4-Cell 7L-RFCI with unbalanced load change based on output current (Ia) and flying capacitor voltages (Vca1, Vca2 and Vca3). (a) Simulation results. (b) Experimental results.

Chapter 6

Four Quadrant Reduced Modular Cell Rectifier

Multilevel converters are popularly recognized for their perceived merits such as having higher power handling capability as well as delivering excellent power quality with the intelligent synthesis of m -level (mL) waveforms. Such attractive benefits have emerged multilevel converters as the most viable industrial solutions for medium-high voltage drives [75, 93], renewable energy systems [92, 94], power transmission systems [95, 96], and electrical transportations [97, 98].

Producing low harmonic profile with the high incremental stepped voltage waveforms are clearly evidenced to be advantageous at all times. However, several complications are concerned in these established multilevel topologies especially the increase in component counts, production cost and converter size. Besides complicating the converter design, the overall reliability and the system efficiency are also greatly affected. An extensive research is further carried out on the multilevel converters by enhancing the performance with alternatively new topologies.

Several multilevel topologies thus far reported in the recent literatures are developed to synthesize higher mL voltages with the reduced component counts. But most of these converters are employed as high power inverters to perform DC-AC electrical conversion. Even though higher resolution waveforms and better efficiency are achieved with these multilevel inverters [87-91], but none of them is retrofittable as a three-phase front-end active rectifier in the AC/DC/AC system due to the multiple isolated dc sources configuration involved in the designs.

Fig. 6.1 Recent three-phase multilevel rectifier with reduced parts topologies (I) to (IV).
 (a) 4L unidirectional flying capacitor rectifier. (b) 4L unidirectional diode clamped rectifier.
 (c) 4L reduced-parts-count rectifier. (d) 5L hybrid PWM rectifier.

Multilevel rectifiers with reduced part counts are proposed previously as well as shown in Fig. 6.1, which are known as (I) unidirectional flying capacitor rectifier [99], (II) unidirectional diode clamped rectifier [100], (III) reduced-parts-count multilevel rectifier [101] and (IV) hybrid PWM rectifier [102]. The active switch counts of these high power rectifiers are reduced because of the replacement made with the power diodes. As a result, these multilevel rectifiers are two quadrants operated as the positive switched voltage waveforms are produced only with the positive polarity of

input currents and vice versa for the negative cycle. In this case, the applicability of (I) to (IV) is restricted to non-regenerative systems where bidirectional power flow is not required.

Therefore, a modular cell rectifier with reduced flying capacitors and active switches (RFCR) is proposed using a hybrid carrier-based PWM named as hybrid phase-shifted carrier phase-disposition PWM (PSC-PD-PWM). The proposed topological design is achieved by clamping a series of modular cells onto a low operational frequency cell. By doing so, high flexibility in imbricating the cells is retained in the RFCR with the modularity approach incorporated. In addition to that, the RFCR can synthesize higher mL voltages with the component counts significantly reduced without affecting its full four quadrants operation. Moreover, the single dc-link configured RFCR eliminates the need of additional bulky transformer at all times. Hence, lower cost and compact size are achieved with the RFCR.

Similarity in the converter design is found between the proposed RFCR and the classical multilevel flying capacitor converter (MFCC) developed by Meynard *et al.* [63]. The MFCC is commercially available in ALSTOM Power Conversion for medium voltage (MV) up to 4.16 kV drives [75] and also operated as the input chopper for the European railways T13 locomotives [86]. Typically, the voltage waveforms of the classical MFCC are synthesized using the commonly known phase-shifted carrier PWM (PSC-PWM). Nevertheless, several factors such as high switching frequency operation and large flying capacitor energy make the MFCC unfeasible for higher voltage applications.

Therefore, a comparative study is evaluated between the proposed RFCR and the classical flying capacitor rectifier (MFCR) to highlight the enhanced performances achieved based on the seven-level (7L) stepped voltage levels. The proven merits of the proposed RFCR make it attractively suitable for higher MV applications with space constraint. The feasibility of the near unity power factor operated RFCR is verified with a proposed closed-loop flying capacitor voltage balancing control using hybrid PSC-PD-PWM under various dynamic conditions.

6.1 Generalized Structure

Fig. 6.2 Proposed transformerless three-phase n -cell reduced flying capacitor rectifier (RFCR) topology.

The general configuration of the proposed transformerless three-phase modular cell rectifier with reduced component counts (RFCR) is shown in Fig. 6.2. Each modular cell is constructed using a pair of semiconductor switches S_x and its complimentary S_x' with a capacitor p clamped between the cells. The number of active switches i_{switches} and flying capacitors $p_{\text{capacitors}}$ can be determined according to the number of modular cells (n_{cells}) utilized. The pair of switches S_{x1} and S_{x1}' in Cell 1 nearest to the dc-link operates at low frequency (LF) of 50 Hz depending on the modulating frequency (f_o) while the remaining switches in Cell 2 to Cell n operate at constant frequency matching with the carrier frequency (f_c).

The proposed design of clamping the series-connected modular cells (Cell 2 to Cell n) onto the LF operated cell (Cell 1) allows the RFCR to synthesize higher mL voltages flexibly by extending the n_{cells} . Thus, the stepped voltage levels are now doubly increased with every incremental modular cell based on (6.1) while retaining the transformerless operation with its single dc-link structure.

$$(mL)_{\text{RFCR}} = n_{\text{cells}} \times 2 - 1 \quad (6.1)$$

Even though the similarity is found between the proposed RFCR and the classical MFCR, but the component counts, cost and size of the converter are significantly reduced with the proposed modularity approach. Since the semiconductor switches are reduced with the introduction of LF switches instead of replacing with the power diodes like those (I) to (IV), the RFCR can continue to perform the four quadrants operation which is suitable for those regenerative drive systems. Hence, higher efficiency is achieved while having the harmonic profile improved as well.

6.2 Operating Principles of 4-cell 7L-RFCR

Having three modular cells being clamped onto the low frequency operated Cell 1 results a single-phase seven-level (7L) reduced flying capacitor rectifier (RFCR) in Fig. 6.3(a). A minimum of 8 i_{switches} (S_{x1} to S_{x4} and $S_{x1'}$ to $S_{x4'}$) and 3 $p_{\text{capacitors}}$ (C_{x1} to C_{x3}) are required to construct each phase-leg depending on the device voltage ratings considered for the converter design. The number of component counts is clearly observed to be reduced when compared to the classical 7L-MFCR (12 i_{switches} and 5 $p_{\text{capacitors}}$ per phase-leg) in Fig. 6.3(b). The difference would be even greater when the converter is designed for the three-phase systems.

Fig. 6.3 (a) Proposed 4-Cell 7L-RFCR. (b) Classical 6-Cell 7L-MFCR.

A total combination of $2^4 = 16$ valid operating states from '0000' to '1111' as listed in the Table 6.1 are required to drive the four pairs of semiconductor switches. There are two additional switching states generated for zero voltage level and three redundant states for each $\pm V_{dc}/3$ and $\pm V_{dc}/6$ voltage level. Apart from that, one can observe that all the positive voltage levels are produced only when S_{x1} conducts while the negative voltage levels are synthesized when S_{x1}' conducts. Hence, only the two switches S_{x1} and S_{x1}' in Cell 1 are always performing at fundamental frequency of 50 Hz.

The seven-level stepped voltage waveforms are synthesized at $\pm V_{dc}/6$, $\pm V_{dc}/3$, $\pm V_{dc}/2$ and zero level accordingly based on the given switching states in Table 6.1 and the flying capacitor voltages in Table 6.2. The flying capacitor voltages V_{Cx1} , V_{Cx2} and V_{Cx3} of 4-cell 7L-RFCR are maintained at $V_{dc}/6$, $V_{dc}/3$ and $V_{dc}/2$ respectively. The voltage across the corresponding p^{th} flying capacitor of n -cell mL -RFCR can be determined using (6.2).

$$V_{C_{x(p^{th})}}^{RFCR} = \frac{p^{th}}{mL-1} \times V_{dc} \quad (6.2)$$

It is worth mentioning to observe the two key factors in Table 6.2 which are the number of flying capacitors and the capacitor voltage ratings. The proposed 4-cell 7L-RFCR does not only reduced the total number of flying capacitors but also greatly decreases the required voltages across the flying capacitors as compared to the same number of modular cells implemented in the classical 4-cell 5L-MFCR.

TABLE 6.1
3-CELL 7L-RFCR VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

Switching States ($S_{x1}, S_{x2}, S_{x3}, S_{x4}$)	Phase Leg x Voltage V_{xn}
(0000)	$-V_{dc}/2$
(0001) (0010) (0100)	$-V_{dc}/3$
(0011) (0101) (0110)	$-V_{dc}/6$
(0111) (1000)	0
(1001) (1010) (1100)	$+V_{dc}/6$
(1011) (1101) (1110)	$+V_{dc}/3$
(1111)	$+V_{dc}/2$

Where x represents phase a, b and c
 Logic '1' and '0' represent 'on' and 'off' state respectively

TABLE 6.2
CAPACITOR VOLTAGES FOR CLASSICAL MFCR AND PROPOSED RFCR

Capacitors Clamped at p^{th} Position	Phase x Capacitor Voltages $V_{Cx,p}^{\text{th}}$			
	MFCR		RFCR	
	4-Cells (5-Levels)	6-Cells (7-Levels)	3-Cells (5-Levels)	4-Cells (7-Levels)
1	$V_{dc}/4$	$V_{dc}/6$	$V_{dc}/4$	$V_{dc}/6$
2	$2V_{dc}/4$	$2V_{dc}/6$	$2V_{dc}/4$	$2V_{dc}/6$
3	$3V_{dc}/4$	$3V_{dc}/6$	~	$3V_{dc}/6$
4	~	$4V_{dc}/6$	~	~
5	~	$5V_{dc}/6$	~	~

Where x represents phase a, b and c
 and p^{th} represents the placing position number of flying capacitor being clamped.

6.3 General Characteristics of Proposed RFCR

The following analysis in this section is expressed to determine the appropriate switching device ratings as well as designing both the input filter inductors and the flying capacitors. It is imperative to have the parameters calculated when designing the converter so that the reliability and the efficiency can be optimized. Hence, this section provides the theoretical expressions for obtaining the voltage stress, current stress, input inductance and flying capacitance values.

6.3.1 Voltage Synthesis Expressions

The synthesized phase voltages and line-to-line voltages for RFCR are determined using (6.3) and (6.4) respectively based on the given switching states in Table 6.1 and the corresponding flying capacitor voltages determined from (6.2).

$$V_{xn}(t) = V_{dc}(t)(S_{x1}(t) - 0.5) + \sum_{k=2}^{n_{cells}} V_{Cx((P_{capacitors} + 2) - k)}(t)(S_{x(k)}(t) - S_{x(k-1)}(t)) \quad (6.3)$$

$$\begin{aligned} \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix}_{mL} &= V_{dc}(t) \begin{bmatrix} (S_{a1}(t) - S_{b1}(t)) \\ (S_{b1}(t) - S_{c1}(t)) \\ (S_{c1}(t) - S_{a1}(t)) \end{bmatrix} \\ &+ \sum_{m=2}^{n_{cells}} V_{Cx((P_{capacitors} + 2) - m)}(t) \begin{bmatrix} (S_{a(m)}(t) - S_{a(m-1)}(t) - S_{b(m)}(t) + S_{b(m-1)}(t)) \\ (S_{b(m)}(t) - S_{b(m-1)}(t) - S_{c(m)}(t) + S_{c(m-1)}(t)) \\ (S_{c(m)}(t) - S_{c(m-1)}(t) - S_{a(m)}(t) + S_{a(m-1)}(t)) \end{bmatrix}_{x \in \{a,b,c\}} \end{aligned} \quad (6.4)$$

6.3.2 Voltage Stress Analysis

The voltage stress across the switching devices of the proposed RFCR as expressed in (6.5) is prominently affected by the instantaneous flying capacitor voltages.

$$V_{S_{x(\text{cell } n^{\text{th}})}^{\text{RFCI}}}(t) \approx \begin{cases} -\left(\frac{(mL-1)-p^{\text{th}}}{mL-1}\right)V_{\text{dc}} \times S_{x(\text{cell } n^{\text{th}})}(t) & \text{if cell } n^{\text{th}} = 1 \\ -\left(\frac{p^{\text{th}}-(p^{\text{th}}-1)}{mL-1}\right)V_{\text{dc}} \times S_{x(\text{cell } n^{\text{th}})}(t) & \text{if cell } n^{\text{th}} \geq 2 \end{cases} \quad (6.5)$$

According to (6.2) and (6.5), it should be noted that the blocking voltage of the two LF switches S_{x1} and S_{x1}' in the Cell 1 must be capable to withstand $V_{\text{dc}}/2$ for n -cell mL -RFCR at all times. Same voltage stress expression (6.5) applies to the respective complimentary switches as well.

6.3.3 Current Stress Analysis

The maximum current stress must be determined too since it is one of the dominant factors considered for designing the converter with proper selection of device rating. The average current stress experienced in each active switches of the proposed RFCR is approximated in the following (6.6) over one fundamental period.

$$I_{S_{x1}}(t) \approx \frac{\hat{I}_x}{2\pi} \int_{0-\theta_x}^{\pi-\theta_x} \sin(\omega t - \delta + \theta_x) d\omega t$$

$$I_{S_{x(\text{cell } n^{\text{th}})}}(t) \approx \frac{\hat{I}_x}{2\pi} \left[\int_{0-\phi_{(n-1)}-\theta_x}^{\pi-\phi_{(n-1)}-\theta_x} \left[m_x \sin(\omega t + \phi_{(n-1)} + \theta_x) \right] d\omega t + \int_{\pi-\phi_{(n-1)}-\theta_x}^{2\pi-\phi_{(n-1)}-\theta_x} \left[\left(m_x \sin(\omega t + \phi_{(n-1)} + \theta_x) + 1 \right) \right] d\omega t \right]_{n \geq 2} \quad (6.6)$$

where $M_{x\text{sine}\langle\text{rectifier}\rangle}$ is the voltage transfer ratio of the system between the dc-link voltage and the respective input phase voltage as expressed in (6.7):

$$M_{x\text{sine}\langle\text{rectifier}\rangle}(t) = \frac{V_{dc}(t)}{2\sqrt{2}V_{xm(rms)}(t)} \geq 1 \quad (6.7)$$

The average current stress is determined based on the power factor between the grid voltage and current in radians (δ) as well as the peak magnitude of phase current ($\hat{I}_x$) assuming that the ripple free current is sinusoidal. Since the active switches S_{x1} and S_{x1}' of Cell 1 are conducting only during half of the fundamental period, there is low to no reverse current through the pair of LF switches depending on the power factor. Therefore, the net average current stress of the Cell 1 switches is found higher as compared to the remaining other switches.

It is proven that the average current stress of the switches in the Cell 2 to Cell n is equivalently the same even though the carriers are being phase-shifted evenly by ϕ_n in radians. The maximum average current stress analysis is expressed for all the three phases considering the respective reference phase angle (θ_x).

6.3.4 Design of Input Inductors

Low input current total harmonic distortion (THD) is importantly concern for the grid connected system which must be strictly complied with the stringent regulations to guarantee excellent power quality and maintain high grid reliability. Thus, it is essential to obtain the critical input inductance value according to (6.8) so that the ripple current is limited within the permissible range (ΔI_{Lx}).

Fig. 6.4 Incremental input voltage waveforms of proposed 4-cell 7L-RFCR.

$$L_{x(\text{critical})} \approx \frac{k \left(\frac{\sqrt{2}V_{xm(\text{rms})} \times \sin(\omega t)}{\text{Sec}_n \times m_{x(\text{rectifier})} \times 2\sqrt{2}V_{xm(\text{rms})}} \right)}{\Delta I_{Lx} \times f_{Os}} \quad (6.8)$$

The input inductance is determined based on the duty ratio (k) of the switching states with respect to the sectors (Sec_n) in Fig. 6.4 while inversely proportional to the overall switching frequency (f_{Os}). The sectors I ($\text{Sec}_I = 1$) to III ($\text{Sec}_{III} = 3$) from 0 to $\pi/2$ radians defined in (6.9) are considered for the analysis due to the phase symmetry.

$$\begin{aligned} \text{Sec}_I \quad k &= 3 \sin(\omega t) & 0 \leq \omega t \leq 0.1082\pi \\ \text{Sec}_{II} \quad k &= 3 \left(\sin(\omega t) - \frac{1}{3} \right) & 0.1082\pi \leq \omega t \leq 0.2323\pi \\ \text{Sec}_{III} \quad k &= 3 \left(\sin(\omega t) - \frac{2}{3} \right) & 0.2323\pi \leq \omega t \leq 0.5\pi \end{aligned} \quad (6.9)$$

The ripple current is observed higher when the controlled dc-link voltage increases at the 50% duty ratio ($k = 0.5$) assuming the input filter inductance value and output load are fixed. Consequently, the ripple current can be reduced by increasing the f_{Os} or controlling the dc-link voltage in (6.7) to attain near unity modulation index value ($m_{x(\text{rectifier})} \approx 1$). Apart from that, the ripple current is also greatly reduced due to the incremental stepped voltage waveforms according to the $\text{Sec}_n / (mL - 1)$ term in

expression (6.8). Hence, the maximum current rating included the peak ripple current must be taken into consideration when designing the input inductors windings on top of the f_{Os} which affects the number of turns.

6.3.5 Design of Flying Capacitors

Since the proposed n -cell mL -RFCR is constructed with flying capacitors clamped between the modular cells, the critical flying capacitance value is estimated using (6.10):

$$C_{x,p}^{th/critical} \approx \frac{4 \times m_{x<rectifier>} \times \cos(\varphi) \times \bar{I}_{dc}}{3 \times \Delta V_{Cx,p}^{th} \times f_{Os}} \quad (6.10)$$

The flying capacitance is inversely proportional to the maximum permissible flying capacitor ripple voltage ($\Delta V_{Cx,p}^{th}$) and the overall switching frequency (f_{Os}). The critical flying capacitance value is determined based on the modulation index ($m_{x<rectifier>}$), the average dc-link current ($\bar{I}_{dc}$) affected by the output load as well as the power factor angle (φ) between the input voltage and the input current.

High flying capacitor ripple voltage is experienced when the rectifier operates at near unity power factor ($\cos(\varphi) = 1$). However, the ripple voltage can be ensured low similarly by controlling the V_{dc} and the f_{Os} . Selecting the flying capacitors appropriately is important to achieve a safety operating environment by ensuring that both maximum ripple voltage and peak current are lesser than the rated voltage and current ratings given by the manufacturer datasheet.

6.4 Unity Power Factor Operation Control Design

The closed-loop control is proposed for the 4-cell 7L-RFCR in this section as shown in Fig. 6.5. It is constructed based on the two control schemes (Synchronous-Reference-Frame Current Control and Flying Capacitor Voltage Balancing Control) which are comprehensively described in the following subsections.

Fig. 6.5 Proposed three-phase unity power factor operated RFCR with flying capacitor voltage balancing control scheme using hybrid PSC-PD-PWM.

6.4.1 Synchronous-Reference-Frame Current Control

The unity power factor controller for the 4-cell 7L-RFCR proposed in Fig. 6.5 is constructed using the synchronous reference frame current (SRFC) control as detailed in [103]. The SRFC controller provides good dynamic response and shapes input current with high resolution quality while maintaining unity power factor operation. The SRFC consists of a dc-link voltage control, a feed-forward current control and a reference current generator (dq0 Park's transformation).

In order to achieve stable control system, the outer-loop dc-link voltage control is designed following the open-loop transfer function as expressed in (6.11).

$$L(s) = \frac{K_p s + K_i}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{(\sqrt{3} V_p / L_x I_d) - s}{s + (I_{dc} / C_{eq} V_{dc})} \quad (6.11)$$

The proportional gain (K_p) and integral gain (K_i) of the dc-link voltage control loop are selected at 0.16 and 8 respectively. The C_{eq} and L_x are total equivalent dc-link capacitance and the filter inductance. An additional feed-forward current parameter (K_f) is implemented in the control loop as well, which is expressed in (6.12) based on the power balanced principle where V_p is the peak amplitude of the instantaneous ac supply voltage. Even though it requires an additional sensor, but the feed-forward current control allows better dc-link voltage response to load disturbance and increases the system stability.

$$K_f = \frac{2V_{dc}}{3V_p} \quad (6.12)$$

The active current (I_d) fed into the SRFC control is achieved by summing the outputs of the dc-link feed-forward and feedback controls while the reactive current (I_q) must be remained null to attain near unity power factor performance. As such, the three-phase reference currents (I_x^*) are now obtained using the Park's transformation.

6.4.2 Flying Capacitor Voltage Balancing Control

It is necessary to ensure that the flying capacitor voltages of the proposed RFCR are tracked to their desired reference at all times. Unbalanced flying capacitor voltages will cause an increased voltage stress on the power semiconductors and affect the entire system stability. This issue can be resolved easily by oversizing the device ratings which is not a cost-effective solution.

Alternatively, a flying capacitor voltage balancing control is developed using the simple proportional gain. It is clearly observed in (6.13) that the current through the respective flying capacitor is affected by the switching states of the two adjacent switches.

$$C_{x,p^{th}} \times \frac{dV_{C_{x,p^{th}}}}{dt} = I_{C_{x,p^{th}}}(t) = \left(S_{x(n-p^{th}+1)} - S_{x(n-p^{th})} \right) I_x \quad (6.13)$$

The flying capacitor current in (6.13) can be expressed in local average form over a switching period by replacing the switching states with the duty ratio. The locally average capacitor voltage balancing dynamic is given in the following:

$$\frac{\Delta \bar{V}_{C_{x,p^{th}}}}{\Delta t} = \frac{\left(\Delta d_{x(n-p^{th}+1)} - \Delta d_{x(n-p^{th})} \right) \bar{I}_x}{C_{x,p^{th}}} \quad (6.14)$$

Fig. 6.6 Proposed flying capacitor voltage balancing control with modulation logic gate signals for 4-cell 7L-RFCR.

Hence, the flying capacitor voltages can be regulated by varying the duty ratios of the switching pulses accordingly to the respective capacitor voltage errors ($\epsilon_{x(n)}$) between the desired reference voltage in Table II and the instantaneous measured values. These voltage errors are minimized using the proportional (P) controller with the gain of 0.4.

$$\Delta d_{x(n)} = \text{sign}(I_x) (\epsilon_{x(n-1)} - \epsilon_{x(n)}) P \quad (6.15)$$

The duty cycle varies depending on the magnitude of the instantaneous input current which is defined as 1 and -1 for the respective positive and negative cycle using the sign term.

$$Mx_{\text{sine}(n)} = I_x^* + \Delta d_{x(n)} \quad (6.16)$$

The variation of the duty ratio will be added to the three-phase reference current I_x^* (output of the Park transformation) to obtain the modulation sine templates ($M_{x\text{sine}(n)}$). The proposed flying capacitor voltage balancing control scheme for the 4-cell 7L-RFCR is shown in Fig. 6.6.

6.4.3 Hybrid Carrier-Based PWM Schemes

The proposed RFCR is operated using the hybrid phase-shifted carrier phase-disposition PWM (PSC-PD-PWM) in Fig. 5.4(b) as presented previously in Chapter 5. The alternative hybrid PSC-POD-PWM can also be applied for synthesizing the input voltages of the RFCR. However, the hybrid PSC-PD-PWM is chosen in this case over the other proposed PSC-POD-PWM due to its improved voltage harmonic profile.

Same for all cases, $(mL-1)$ number of triangular carriers (n_{tri}) would be needed for any mL modulation scheme. Thus, a total of six n_{tri} are required for the proposed 7L-RFCR which are divided equally into 2 sets. One set is level-shifted above zero reference magnitude ($\text{tri}_{\text{TOP}(1,2,3)}$) and the other set level-shifted below zero reference magnitude ($\text{tri}_{\text{BOT}(1,2,3)}$). The top and bottom carriers are 120° phase-shifted apart evenly.

The final gating signals for the switching devices are achieved directly by comparing the $M_{x\text{sine}(n)}$ with the respective top and bottom phase-shifted carriers using simple comparators and logic gates as shown in Fig. 6.6. Since there are only three carriers being phase-shifted at the top and the bottom level in this case compared to the six phase-shifted carriers in PSC-PWM, the f_{os} is also reduced by 50% which are also proven in Chapter 5.1.5 – Harmonic Characteristics of Advanced Hybrid Sinusoidal PWM Schemes.

6.5 Comparative Evaluation of Classical MFCR and Proposed RFCR

The performances of the proposed four quadrants RFCR are compared against the classical MFCR in terms of the input current harmonic distortions as well as the distributed semiconductor losses as discussed in the following subsections. Significant improvements can be observed in the proposed RFCR over the classical MFCR.

6.5.1 Input Current Shaping Performance

Shaping the input current to near pure sinusoidal waveforms is always desired to be achieved for the grid-connected rectifier. The performance of the grid current response for the proposed RFCR is evaluated in Fig. 6.7 based on different parameters such as (i) output power, (ii) input filter inductance, (iii) controlled V_{dc} and (iv) f_{Os} . Generally, the input current THD is observed high for the light-load conditions despite of any f_{Os} and $M_{Xsine<rectifier>}$ operation. This is because the fundamental current harmonic amplitude is low with the accompanied ripple harmonics. Thus, the input current THD can be greatly reduced with the increasing magnitude of the fundamental current harmonic which can be achieved by increasing the output load power or the $M_{Xsine<rectifier>}$ with higher controlled V_{dc} .

Alternatively, the ripple current can also be further decreased with larger input filter inductance. Apart from that, the synthesis of higher mL voltages reduces the ripple current as well. It is clearly proven in Fig. 6.7 that the input current THD of the proposed 7L-RFCR is approximately same as the classical 7L-MFCR and is much lower than the classical 5L-MFCR. Therefore, the input inductance of the proposed RFCR can be further reduced while achieving good input current shaping with reduced component counts.

Fig. 6.7 Comparison of input current total harmonic distortion based on different dc-link voltage reference. (a) 170 Vdc (1.0 $M_{x_{sine}}$). (b) 187 Vdc (0.9 $M_{x_{sine}}$).

6.5.2 Power Semiconductor Device Losses

The total distributed losses consisting of both total switching loss and total conduction loss of per phase-leg discrete components are shown in Fig. 6.8 based on the different parameters (i) to (iv) as mentioned previously. The power converters achieve better efficiency with near unity $M_{x_{sine<rectifier>}}$ operation since higher losses are experienced when the controlled V_{dc} reference is increased ($M_{x_{sine<rectifier>}} > 1$) as well as for larger output loads. The total distributed losses are also reduced with the increasing input

filter inductance due to the lower input current THD since conduction loss is dominantly affected by the current performances.

The results in Fig. 6.8 have clearly evidenced that the proposed 7L-RFCR experienced similar amount of loss as the classical 5L-MFCR and much lower compared to the classical 7L-MFCR. The total distributed losses in RFCR configuration are notably decreased because of the reduced component counts which lead to the lower dominant conduction loss and the reduced flying capacitor voltages. Hence, the proposed RFCR features higher efficiency than the classical MFCR.

Fig. 6.8 Comparison of per phase-leg semiconductor losses based on different dc-link voltage reference. (a) 170 Vdc (1.0 Mx_{sine}). (b) 187 Vdc (0.9 Mx_{sine}).

6.6 Experimental Verification Results

The comparative studies between the proposed RFCR using hybrid PSC-PD-PWM and the classical MFCR under PSC-PWM are carried out using PSIM v9.0.4 Simcouple and MATLAB R2010b Simulink®. The hardware prototype is developed to verify the discussed performances with the aid of dSPACE RT1103 Real-Time Workshop (RTW). All the presented results are based on the detailed settings given in Table 6.3.

TABLE 6.3
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE
OF 4-CELL 7L-RFCR

System Parameters	Settings
Reference Sinusoidal Frequency (f_o)	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz
AC Voltage Source	60 Vrms
Output DC-Link Voltage Reference	170 Vdc
Flying Capacitors ($C_{x,p}^{th}$)	2200 μ F
Filter – Inductors	5 mH
Load – Resistors	28.9 Ω (1kW)

Fig. 6.9 Simulated dynamic performance of 4-cell 7L-RFCR with PF variation and load change.
(a) Grid voltage and current ($\times 5$). (b) Input rectifier pole voltage and flying capacitor voltages.

The dynamic performances of the 4-cell 7L-RFCR are evaluated with a series of step changed in the power factor (PF), modulation index ($M_{\text{sine} < \text{rectifier} >}$) and load parameters to verify the feasibility of the proposed voltage balancing control.

The proposed 7L-RFCR is simulated with leading PF (0.8 PF) between $t = 2\text{ s}$ to 2.1 s , lagging PF (0.8 PF) between $t = 2.3\text{ s}$ to 2.4 s as well as unity PF for the remaining period as shown in Fig. 6.9(a) while having the dc-link voltage (V_{dc}) controlled to the output voltage command reference of 170 V. Besides that, the output load is step changed from 1 kW to 0.5 kW at $t = 2.15\text{ s}$ and back from 0.5 kW to 1 kW at $t = 2.25\text{ s}$. However, it can be clearly observed in Fig. 6.9(b) that the flying capacitor voltages $V_{\text{Ca}1}$, $V_{\text{Ca}2}$ and $V_{\text{Ca}3}$ are remained balance at their respective desired voltage levels (28.33 V, 56.67 V and 85 V) despite of the variations in the PF and the load changed condition. The simulated dynamic performances of 4-cell 7L-RFCR in Fig. 6.9 are also validated with the experimental results.

The unity power factor controlled performance of the 4-cell 7L-RFCR following the control scheme in Fig. 6.5 using hybrid PSC-PD-PWM can be clearly observed in the Fig. 6.10. Sinusoidal grid current shaping waveform is achieved while yielding a near unity power factor (0.999 PF). The dc-link voltage V_{dc} is also tracked to the output voltage command reference at 170 V. Besides that, the flying capacitor voltages $V_{\text{Ca}1}$, $V_{\text{Ca}2}$ and $V_{\text{Ca}3}$ in Fig. 6.11 are well balanced at 28.3 V, 56.7 V and 85.1 V respectively. Hence, the input pole voltage V_{an} in Fig. 6.10 is synthesized correspondingly to the seven-level.

Fig. 6.10 Results of 4-Cell 7L-RFCR with near unity power factor performance based on input grid voltage (V_{am}), input grid current (I_a) and output dc-link voltage (V_{dc}).
(a) Simulation results. (b) Experimental results.

Fig. 6.11 Results of 4-Cell 7L-RFCR with near unity power factor performance based on input pole voltage (V_{an}) and flying capacitor voltages (V_{ca1} , V_{ca2} and V_{ca3}).
(a) Simulation results. (b) Experimental results.

(a)

(b)

Fig. 6.12 Results of 4-Cell 7L-RFCR with leading power factor performance based on input grid voltage (V_{am}), input grid current (I_a), output dc-link voltage (V_{dc}) and input pole voltage (V_{an}). (a) Simulation results. (b) Experimental results.

(a)

(b)

Fig. 6.13 Results of 4-Cell 7L-RFCR with leading power factor performance based on input pole voltage (V_{an}) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}). (a) Simulation results. (b) Experimental results.

Fig. 6.14 Results of 4-Cell 7L-RFCR with lagging power factor performance based on input grid voltage (V_{am}), input grid current (I_a), output dc-link voltage (V_{dc}) and input pole voltage (V_{an}). (a) Simulation results. (b) Experimental results.

Fig. 6.15 Results of 4-Cell 7L-RFCR with lagging power factor performance based on input pole voltage (V_{an}) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}). (a) Simulation results. (b) Experimental results.

Moreover, the proposed 4-cell 7L-RFCR is also evaluated with the leading (0.872 PF) power factor in Figs. 6.12 and 6.13 as well as with the lagging (0.808 PF) power factor in Figs. 6.14 and 6.15. Despite of the variations in the power factor, the dc-link voltages in Figs. 6.16, 6.18 and 6.20 are well maintained at 170 V constantly. However, there is difference between the input current magnitudes in Figs. 6.12 and 6.14 which are caused by the angle displacement. Thus, affecting the input seven-level pole voltage waveforms to be synthesized differently when compared to those waveforms shown in Figs. 6.10 and 6.11.

Apart from that, it should be noted that the flying capacitor voltages in Figs. 6.13 and 6.15 are remained balance at their desired voltage levels, even in the event of power factor and load change condition as proven in Figs. 6.17, 6.19 and 6.21. The experimental results have demonstrated the dynamic response and the stability of the proposed unity power factor operated RFCR using the flying capacitor voltage balancing control.

The matched experimental results with the simulation result in Fig. 6.9 have confirmed the practicality of the proposed RFCR which have overcome the challenges faced in the classical MFCR. The proposed RFCR synthesizes higher voltage stepped waveforms with the component counts and costs significantly reduced. Therefore, the four quadrants operated RFCR can be attractively applicable for any higher MV drive systems with space constraint as compared to the classical MFCR.

Fig. 6.16 Results of 4-Cell 7L-RFCR with power factor varies from unity to leading based on input grid voltage (V_{am}), input grid current (I_a), output dc-link voltage (V_{dc}) and input pole voltage (V_{an}). (a) Simulation results. (b) Experimental results.

Fig. 6.17 Results of 4-Cell 7L-RFCR with power factor varies from unity to leading based on input grid current (I_a) and flying capacitor voltages (V_{ca1} , V_{ca2} and V_{ca3}). (a) Simulation results. (b) Experimental results.

Fig. 6.18 Results of 4-Cell 7L-RFCR with power factor varies from unity to lagging based on input grid voltage (V_{am}), input grid current (I_a), output dc-link voltage (V_{dc}) and input pole voltage (V_{an}). (a) Simulation results. (b) Experimental results.

Fig. 6.19 Results of 4-Cell 7L-RFCR with power factor varies from unity to lagging based on input grid current (I_a) and flying capacitor voltages (V_{ca1} , V_{ca2} and V_{ca3}). (a) Simulation results. (b) Experimental results.

Fig. 6.20 Results of 4-Cell 7L-RFCR under load change from 1 kW to 0.5 kW based on input grid voltage (V_{am}), input grid current (I_a), output dc-link voltage (V_{dc}) and input pole voltage (V_{an}). (a) Simulation results. (b) Experimental results.

Fig. 6.21 Results of 4-Cell 7L-RFCR under load change from 1 kW to 0.5 kW based on input grid current (I_a) and flying capacitor voltages (V_{Ca1} , V_{Ca2} and V_{Ca3}). (a) Simulation results. (b) Experimental results.

Chapter 7

Active Neutral Point Clamped Inverter

Multilevel converters have emerged as the most viable solutions and are widely employed in many industries for medium to high power applications. They are popularly known for their distinguished merits such as having high power handling capability and delivering excellent power quality with the intelligent synthesis of m -level (mL) waveforms.

The commercialized converters available in the markets are the commonly known classical multilevel topologies, which are three-level (3L) neutral point clamped inverters (3L-NPC), multilevel flying capacitor inverters (MFCI) and multilevel cascaded H-bridge inverters (MCHB) [75]. Among these, only MCHB is considered for high voltage drives up to 11kV while 3L-NPC and 4L-MFCI are only applicable for the medium voltage (MV) applications below 6kV.

In the last decade, an alternative multilevel converter named as five-level active neutral point clamped (5L-ANPC) inverter was first proposed by P. Barbosa *et al* [74]. The mL -ANPC (in Fig. 2.6) has successfully addressed the drawbacks faced in the aforementioned classical topologies since the converter design is constructed based on the hybrid combination of NPC and MFCI configurations. Moreover, the costs, size and weight of the overall mL -ANPC converter are significantly reduced as compared to the classical multilevel topologies [74].

The first 5L-ANPC technology, ACS 2000, has been successfully introduced by ABB Ltd in the industries for voltage drives up to 6.9 kV [104-106]. Over the recent years, several different modulation methods are implemented for the 5L-ANPC such as space vector PWM (SVPWM) [104, 105, 107-110], selective harmonic elimination PWM (SHE-PWM) [106, 111, 112] and carrier-based PWM (CB-PWM) [74, 113-115].

Despite many previous researches have improved the multilevel converter performances utilizing SV-PWM and SHE-PWM schemes, but CB-PWM is still the one of the most favorable modulation techniques for all multilevel converters in the industries [75]. This may be because of its simplicity and low cost solution to achieve the desired gating signals. However, CB-PWM is not fully explored and investigated for the ANPC. Currently, level-shifted carrier PWM (LSC-PWM) [74] and phase-shifted carrier PWM (PSC-PWM) [113-115] are the only CB-PWM modulation schemes employed for ANPC.

Therefore, in this chapter, a new hybrid CB-PWM modulation strategy named as interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM) is proposed for the mL -ANPC. High resolution waveforms especially the output line-to-line voltages are produced employing the proposed ISC-PD-PWM which makes the ANPC even more attractively suitable for the drive applications. The low harmonic profiled ISC-PD-PWM is also proven mathematically against the conventional PSC-PWM used in [113-115].

Nonetheless, it should be noted that the quality of the synthesized output line-to-line voltage waveforms also depends on the operating conditions of the inverter. Since

ANPC is configured using both dc-link capacitors and flying capacitors, in the event of experiencing unbalanced capacitor voltages, the output power quality will be greatly affected. Besides that, in practice, ripples are found in the dc-link when the inverters are connected to the non-linear loads or when a front-end rectifier is connected to a weak or unbalanced grid [111, 116]. Thereafter, low order harmonics are introduced in the output voltages.

Consequently, these mentioned factors deteriorate the output power quality of the ANPC. It is essentially important to address these issues to assure that good power quality can be delivered at all times. Even though there are various methods reported in the literatures, but those issues are separately treated using different modulation techniques. Hence, a multiple voltage quantities enhancement (MVQE) control using the hybrid ISC-PD-PWM is proposed for the mL -ANPC.

Apart from that, the common mode voltage (CMV) reduction technique for the ANPC has not been reported in the literature so far till date. Since the hybrid configured ANPC is designed for higher MV drive applications, thus it is also imperative to minimize the common mode voltage so that premature bearing failure and electromagnetic interference (EMI) can be avoided and reduced. The mentioned CMV issue can be resolved by implementing an extra fourth phase-leg in the converter design [117] or by adopting magnetic circuits like common-mode inductors and common-mode transformers [118-120]. As a result, additional cost, losses and larger installation space are incurred. Alternatively, the CMV can also be reduced or eliminated through an actively manner by manipulating the modulation techniques [121-123], but these strategies cannot be directly imposed on the ANPC.

Therefore, a CMV reduction technique is proposed for the *mL*-ANPC using the manufacturers' most favorable CB-PWM modulation method due to its inherent simplicity and reduced computational efforts when compared to both SHE-PWM and SV-PWM [75]. In this chapter, the proposed CMV reduction technique is applied in conjunction with the alternative new proposed advanced sinusoidal PWM scheme (hybrid ISC-PD-PWM). The performance of the proposed CMV reduction technique using ISC-PD-PWM is also compared with the popularly implemented PSC-PWM schemes in [113-115].

Thus, this chapter focuses on the proposed MVQE control and the proposed CMV reduction technique using the advanced hybrid ISC-PD-PWM scheme in the following Sections 7.4 and 7.5 of this chapter respectively. The enhanced performances of the ANPC based on the presented proposed principles are verified experimentally with a three-phase seven-level (7L) ANPC hardware prototype.

7.1 Generalized Structure

Fig. 7.1 Proposed transformerless three-phase n -cell active neutral point clamped (ANPC) inverter topology.

The active neutral point clamped (ANPC) topology was fundamentally derived from the three-level (3L) active NPC in [124-126] which is constructed using three pairs of semiconductor switches (S_{x1} to S_{x3}) including its complimentary (S_{x1}' to S_{x3}'). It was later extended to synthesize higher mL output voltages by clamping a series of modular cells (n_{cells}) onto it. The hybrid configuration of the active NPC and the imbricated cells (Cell 1 to Cell n) results the design of the mL -ANPC as shown in the Fig. 7.1.

High modularity and flexibility are well-retained in the converter with each modular cell comprises of two switching devices S_x and S_x' along with a capacitor p clamped in between the cells. The number of switches i_{switches} and flying capacitors $p_{\text{capacitors}}$ can be determined directly from the n_{cells} used. Besides that, the six switches from the basic structure must also be included towards the total switch counts. Because of the hybrid configuration, the mL -ANPC converter does not only address the drawbacks encountered in the classical multilevel topologies but also significantly reduced its cost, size and weight [74].

7.2 Operating Principles of 2-Cell 7L-ANPC

Fig. 7.2 Proposed transformerless single-phase 2-cell 7L-ANPC.

By having two series-connected modular cells clamped onto the 3L active NPC, it results a single-phase seven-level (7L) ANPC inverter as presented in Fig. 7.2. Each phase-leg requires a minimum of 10 i_{switches} (S_{x1} to S_{x5} and $S_{x1'}$ to $S_{x5'}$) and 2 $p_{\text{capacitors}}$ (C_{x1} and C_{x2}) excluding the 2 dc-link capacitors (C_{dc1} and C_{dc2}) depending on the voltage ratings considered for the converter design.

Hence, a total combination of 16 valid operating modes required for the 7L-ANPC is summarized in Table I. It is clearly observed that among the 5 pairs of active switches, both switch pairs (S_{x1} – S_{x2}) and ($S_{x1'}$ – $S_{x2'}$) share the same switching sequences at low frequency (LF) of 50 Hz matching with the modulating frequency (f_o). Meanwhile, the remaining switches S_{x3} to S_{x5} are operating between the modes ‘000’ to ‘111’ correspondingly to the carrier frequency (f_c).

All the positive output levels are generated when S_{x1} and S_{x2} conduct while all negative output levels are achieved when the complimentary LF switches $S_{x1'}$ and $S_{x2'}$ conduct. There are two redundant states for the zero output level and three redundant states for each $\pm V_{dc}/3$ and $\pm V_{dc}/6$ output level. Therefore, the seven-level output

stepped voltage waveforms are synthesized accordingly at $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$ and zero level with respect to the switching states given in Table 7.1. Therefore, the flying capacitor voltages V_{Cx1} and V_{Cx2} of the 7L-ANPC must be maintained at $V_{dc}/6$ and $V_{dc}/3$ respectively all the time. The voltage across the corresponding p^{th} capacitor of n -cell mL -ANPC can be determined in Table 7.2 using the following expression (7.1).

$$V_{C_{x(p^{th})}}^{ANPC} = \frac{p^{th}}{mL-1} \times V_{dc} \quad (7.1)$$

TABLE 7.1
2-CELL 7L-ANPC VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

Switching States ($S_{x1}, S_{x2}, S_{x3}, S_{x4}, S_{x5}$)	Phase Leg x Voltage V_{xn}
(00000)	$-V_{dc}/2$
(00001) (00010) (00100)	$-V_{dc}/3$
(00011) (00101) (00110)	$-V_{dc}/6$
(00111) (11000)	0
(11001) (11010) (11100)	$+V_{dc}/6$
(11011) (11101) (11110)	$+V_{dc}/3$
(11111)	$+V_{dc}/2$

Where x represents phase a, b and c
Logic '1' and '0' represent 'on' and 'off' state respectively

TABLE 7.2
CAPACITOR VOLTAGES FOR ANPC

Capacitors Clamped at p^{th} Position	Phase x Capacitor Voltages $V_{Cx,p^{th}}$		
	2-Cells (7-Levels)	4-Cells (11-Levels)	6-Cells (15-Levels)
1	$V_{dc}/6$	$V_{dc}/10$	$V_{dc}/14$
2	$2V_{dc}/6$	$2V_{dc}/10$	$2V_{dc}/14$
3	~	$3V_{dc}/10$	$3V_{dc}/14$
4	~	$4V_{dc}/10$	$4V_{dc}/14$
5	~	~	$5V_{dc}/14$
6	~	~	$6V_{dc}/14$

Where x represents phase a, b and c
and p^{th} represents the placing position number of flying capacitor being clamped.

7.3 Voltage Characteristics Expressions

Higher number of output voltage stepped levels can be synthesized easily for the modular structured ANPC by extending the n_{cells} . Hence, the mL -ANPC is expressed in (7.2) showing that two additional stepped levels will be produced in the output phase voltage waveforms with every n_{cells} added.

$$(mL)\text{ANPC} = 3 + (2 \times n_{\text{cells}}) \quad (7.2)$$

The output phase voltages for mL -ANPC is determined with (7.3) based on the corresponding operating modes in Table I, the flying capacitor voltages obtained using (7.1) as well as the voltage across both dc-link capacitors C_{dc1} (V_{dc1}) and C_{dc2} (V_{dc2}). According to the voltage divider, V_{dc1} and V_{dc2} should be equivalent to $V_{\text{dc}}/2$.

$$\begin{aligned} V_{\text{xn}}(t) \approx & \frac{V_{\text{dc1}}}{2}(t)(S_{\text{x1}}(t) + S_{\text{x3}}(t)) - \frac{V_{\text{dc2}}}{2}(t)(1 - S_{\text{x2}}(t) + S_{\text{x3}}'(t)) \\ & + \sum_{n=1}^{n_{\text{cells}}} \frac{V_{\text{Cx}}((P_{\text{capacitors}} + 1) - m)}{2}(t) \left[\begin{aligned} & (S_{\text{x}(3+n)}(t) - S_{\text{x}(3+n)}'(t)) \\ & (-S_{\text{x}(3+n-1)}(t) + S_{\text{x}(3+n-1)}'(t)) \end{aligned} \right] \end{aligned} \quad (7.3)$$

It is important to determine the voltage stress so that the semiconductor devices rating can be selected appropriately to optimize the converter design. The voltage stress across the switches of the mL -ANPC is heavily dependent on the instantaneous values of dc-link capacitor voltages and flying capacitor voltages which are clearly expressed in (7.4).

$$V_{S_{x(\text{switch}_i^{\text{th}})}_{\text{ANPC}}}(t) \approx \begin{cases} V_{\text{dc}(\text{switch}_i^{\text{th}})}(t) \times (1 - S_{x(\text{switch}_i^{\text{th}})}(t)) \Big|_{i < 3} \\ \left[\sum_{q=1}^2 \left(\frac{p^{\text{th}} \times V_{\text{dc}}(t)}{mL - 1} - V_{\text{dc}(q)}(t) \right) \times ((q-1) - S_{x(q)}(t)) \right] \times (1 - S_{x3}(t)) \Big|_{i=3} \\ \left(\frac{p^{\text{th}} - (p^{\text{th}} - 1)}{mL - 1} \right) V_{\text{dc}}(t) \times (1 - S_{x(3+n)}(t)) \Big|_{\substack{i > 3 \\ n = i - 3}} \end{cases} \quad (7.4)$$

Hence, it is also imperative to take note of the peak voltages and inrush currents during the transient period when starting up the converter. Therefore, pre-charging of these dc-link capacitors and flying capacitors in the ANPC is necessarily required to prevent these switching devices from being damaged [127].

Referring to the circuit configuration in Fig. 7.1 and (7.4), the blocking voltage capability of the LF switch pairs S_{x1} and S_{x2} for mL -ANPC must be practically able to withstand the instantaneous $V_{\text{dc}1}$ and $V_{\text{dc}2}$ respectively. As for the switch pair S_{x3} which is clamped onto the LF switch pairs S_{x1} and S_{x2} , the voltage stress $V_{S_{x3}}$ is hence greatly affected by the voltage across the flying capacitor at p^{th} position ($V_{C_{x,p}^{\text{th}}}$) on top of the two dc-link capacitor voltages ($V_{\text{dc}1}$ and $V_{\text{dc}2}$). Lastly, the voltage stress across the remaining switches ($S_{x(3+n)}$) in Cell 1 to Cell n depends solely on the adjacent flying capacitor voltages. The same voltage stress expression (7.4) applies to the respective complimentary switches.

7.4 Proposed Multiple Voltage Quantities Enhancement Control

Fig. 7.3 Proposed multiple voltage quantity enhancement (MVQE) control scheme for three-phase 2-cell 7L-ANPC using hybrid ISC-PD-PWM.

The objectives of proposing the MVQE control are to ensure that the (i) dc-link capacitor voltages and (ii) flying capacitor voltages are tracked to their reference values despite of any undesirable conditions, as well as (iii) compensating the dc-link ripples so that the low order harmonic components can be eliminated in the output voltages. The delivered output power quality is further enhanced using the proposed hybrid ISC-PD-PWM modulation scheme. The harmonic characteristic of the ISC-PD-PWM is analyzed mathematically as well in the following subsection.

7.4.1 DC-Link Neutral Point Offset Regulator

Despite the proven facts that the topological design of the mL -ANPC (in Fig. 7.1) is favorably preferred in terms of its simplified dc-link configuration when compared to the classical mL -NPC, however a potential difference is experienced in the split dc-

link voltage across C_{dc1} and C_{dc2} . This is mainly due to the non-identical parameters of the physical capacitors in the dc-link as well as the presence of non-zero average neutral point current regardless of any modulation scheme used.

Various methods had been reported for the neutral point potential balancing using either vector sequence selection based on SVPWM [104, 105, 110] or zero sequence voltage injection technique with CB-PWM [114] for the ANPC. Hence, this section proposes an alternative solution in Fig. 7.3 to balance the neutral point potential by offsetting the DC component in the modulation scheme.

It is clearly understood that output phase voltage across the respective phase x and the neutral point n will experience an additional dc component $V_o(t)$ when V_{dc1} is not equal to V_{dc2} on top of the high frequency components generated by the switching devices as shown in Fig. 7.4. Therefore, the phase voltages of ANPC expressed in (7.5) includes the dc component $V_o(t)$.

$$V_x(t) = V_{xn}(t) + V_o(t) \quad (7.5)$$

As V_{dc1} and V_{dc2} are not exactly the same due to the tolerance value of the dc-link capacitance, (7.3) is expanded into (7.6) assuming that all $V_{C_{x,p}}^{th}$ are ripple free which can now be equivalently expressed in terms of V_{dc1} and V_{dc2} instead.

Fig. 7.4 Performance of unbalanced dc-link capacitors 7L-ANPC without regulator.
 (a) Dc-link voltages. (b) Magnified view of dc-link capacitor voltages.
 (c) Harmonic spectrum of dc-link voltages. (d) Harmonic spectrum of output phase voltages.

$$V_{xn}(t) \approx \frac{V_{dc1}}{2}(t)(S_{x1}(t) + S_{x3}(t)) - \frac{V_{dc2}}{2}(t)(1 - S_{x2}(t) + S_{x3}'(t)) \\ + \sum_{n=1}^{n_{cells}} \left(\frac{p^{th} \times V_{dc1}(t)}{mL - 1} [S_{x(3+n)}(t) - S_{x(3+n-1)}(t)] \right. \\ \left. + \frac{p^{th} \times V_{dc2}(t)}{mL - 1} [-S_{x(3+n)}'(t) + S_{x(3+n-1)}'(t)] \right) \quad (7.6)$$

In this case, the switching functions for 7L-ANPC in (7.6) are replaced with the modulating functions given in (7.7) and (7.8).

$$S_{x1}(t) + \frac{2}{6}S_{x5}(t) + \frac{2}{6}S_{x7}(t) + \frac{2}{6}S_{x9}(t) = Mx(t) + 1 \quad (7.7)$$

$$2 - S_{x1}(t) - \frac{2}{6}S_{x5}(t) - \frac{2}{6}S_{x7}(t) - \frac{2}{6}S_{x9}(t) = 1 - Mx(t) \quad (7.8)$$

Based on (7.6) – (7.8), the resulting modulation signal $Mx^*(t)$ is derived in (7.9) which also equates to (7.10). It is noticed that there is a presence of additional dc component $Mo(t)$ in the expressions when both $V_{dc1}(t)$ and $V_{dc2}(t)$ are diverged from one another.

$$\frac{2V_{xn}(t)}{V_{dc}(t)} = Mx(t) + \frac{V_{dc1}(t) - V_{dc2}(t)}{V_{dc}(t)} \quad (7.9)$$

$$Mx^*(t) = Mx'(t) + Mo(t) \quad (7.10)$$

As a result, the neutral point of the 7L-ANPC is achieved balance by offsetting the dc component term from the modulating signal $Mx(t)$ which can be observed in Fig. 7.5.

Fig. 7.5 Performance of unbalanced dc-link capacitors 7L-ANPC with dc-link neutral point offset regulator. (a) Dc-link voltages. (b) Magnified view of dc-link capacitor voltages. (c) Harmonic spectrum of dc-link voltages. (d) Harmonic spectrum of output phase voltages.

7.4.2 Feedforward DC-Link Ripple Compensation

Practically, significant ripples are experienced in the dc-link mainly when the front-end rectifier is fed by a weak or unbalanced ac source or when the inverter output is connected to nonlinear or unbalanced loads [116]. In the event of such cases, the negative sequence caused the fundamental harmonics to be unbalanced as well as low order harmonics are generated in the output voltages as observed in Fig. 7.6.

Fig. 7.6 Performance of 7L-ANPC with dc-link ripples without compensator.
 (a) Output line-to-line voltages. (b) Harmonic spectrum of output line-to-line voltages.
 (c) Magnified view of harmonic spectrum in (b).

Fig. 7.7 Performance of 7L-ANPC with dc-link ripples with compensator.
 (a) Output line-to-line voltages. (b) Harmonic spectrum of output line-to-line voltages.
 (c) Magnified view of harmonic spectrum in (b).

Ripple compensation method for ANPC has been proposed in [111] using SHE-PWM but not applicable for CB-PWM. This chapter proposes simple dc-link ripple compensation and yet different from [116] that is based on the modified feedforward of modulating functions according to (7.11). The normalized dc-link voltage quantity $\tilde{V}_{dc}$ is achieved with the instantaneous $V_{dc}(t)$ over the average V_{dc} value.

$$Mx'(t) = \frac{Mx(t)}{\tilde{V}_{dc}} = \frac{Mx(t)}{V_{dc}(t)/V_{dc}} \quad (7.11)$$

With the proposed dc-link ripple compensator, the low order harmonics found in the Fig. 7.6 are being mitigated to high orders. But the amplitude of those mitigated harmonics in Fig. 7.7 is comparatively low with those in Fig. 7.6, which have no significant impact on the output voltage THD. However, a slight improvement is noted in the output line voltage THD using the proposed compensation method due to the elimination of low order harmonics caused by the ripples on top of achieving balanced fundamental harmonics in Fig. 7.7.

7.4.3 Flying Capacitor Voltage Balancing Control

As the $p_{\text{capacitors}}$ increases for higher mL -ANPC, the flying capacitor voltages are likely to be unbalanced as shown in Fig. 7.8 especially when there is more than one $p_{\text{capacitors}}$ in each phase-leg. Such consequences lead to an increasingly high voltage stress being imposed on the switching devices, thus greatly affecting the stability of the entire system. Even though the issue can be overcome easily by oversizing the device ratings, however it is not a cost-effective solution.

Therefore, it is very important to ensure that the flying capacitor voltages of the ANPC are tracked to their desired reference values based on (7.1) at all times. Hence, flying capacitor voltage balancing control is required to increase the converter reliability. There are reported control methods such as modifying the switching pulse width of PSC-PWM through a PI regulator [115], using redundant switching states based on SHE-PWM [112] or nearest-level modulator [108, 109]. However, the computational efforts of these are increased especially for higher mL -ANPC.

Fig. 7.8 Performance of 7L-ANPC flying capacitor voltages without voltage balancing control. (a) Phase A flying capacitor voltages. (b) Output phase voltages.

Fig. 7.9 Performance of 7L-ANPC flying capacitor voltages with voltage balancing control. (a) Phase A flying capacitor voltages. (b) Output phase voltages.

Alternatively, a flying capacitor voltage balancing is developed using a simple proportional (P) gain. The current through the respective flying capacitor in (7.12) is dependent on the switching condition of the two adjacent switches.

$$C_{x,p^{th}} \times \frac{dV_{C_{x,p^{th}}}(t)}{dt} = I_{C_{x,p^{th}}}(t) = \left(S_{x(3+n-p^{th})}(t) - S_{x(3+n-p^{th}+1)}(t) \right) I_x(t) \quad (7.12)$$

The time domain flying capacitor current in (7.12) can be expressed in local average form by replacing those switching state functions with the duty ratio as follows:

$$\frac{\Delta \bar{V}_{C_{x,p^{th}}}}{\Delta t} = \frac{\left(\Delta d_{x(3+n-p^{th})} - \Delta d_{x(3+n-p^{th}+1)} \right) \bar{I}_x}{C_{x,p^{th}}} \quad (7.13)$$

$$\Delta d_{x(n)} = \text{sign}(I_x) \left(\varepsilon_{x(n-1)} - \varepsilon_{x(n)} \right) P \quad (7.14)$$

Therefore, the flying capacitor voltages can now be regulated by varying the pulse width of the switching pulses according to the voltage errors ($\varepsilon_{x(n)}$) between the reference capacitor voltage (7.1) and the instantaneous measured values. These errors are then minimized through the P controller which can be tuned to obtain the desired performance.

The duty cycle $\Delta d_{x(n)}$ is varied according to the directional flow of the instantaneous output phase current which is defined as 1 and -1 for the respective positive and negative cycle. The modified duty ratio is then added to the resulting $Mx^*(t)$ of (7.10) and (7.11) to obtain the finalized modulation signal $Mx_{\text{sine}(n)}$ as shown in Fig. 7.10.

Fig. 7.10 Proposed flying capacitor voltage balancing control with modulation logic gate signals for 2-cell 7L-ANPC.

Fig. 7.11 Proposed advanced hybrid sinusoidal PWM schemes – Interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM).

The flying capacitor voltages in Fig. 7.9 are observed to be well maintained balance at their corresponding voltage levels with the proposed balancing control. Moreover, the output phase voltage THD of Fig. 7.9 is significantly improved compared to those in Fig. 7.8 due to the clear synthesis of the seven-level stepped voltage waveforms.

7.4.4 Interleaved Sawtooth Carrier Phase-Disposition PWM

The operational principles of the 2-cell 7L-ANPC are achieved using proposed hybrid CB-PWM named as interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM) shown in Fig. 7.11. Generally, for any carrier-based mL modulation scheme, a $(mL-1)$ number of sawtooth carriers (n_{saw}) would be needed.

In the case of 2-cell 7L-ANPC, six n_{saw} are required which is then divided equally into two sets. One set is level-shifted above the zero reference magnitude ($\text{saw}_{\text{TOP}(1,2,3,\dots,(n_{\text{saw}}/2))}$) and the other set in-phase deposited below zero reference magnitude ($\text{saw}_{\text{BOT}(1,2,3,\dots,(n_{\text{saw}}/2))}$). Both top and bottom sawtooth carriers are 120° phase-shifted apart evenly based on the given (7.15).

$$\Delta_{\text{phase}} = \frac{360^\circ}{(n_{\text{saw}} / 2)} (\text{deg}) = \frac{2\pi}{(n_{\text{saw}} / 2)} (\text{rad}) \quad n_{\text{saw}} = \text{even} > 2 \quad (7.15)$$

Fig. 7.12 Proposed hybrid ISC-PD-PWM modulating waveforms with the corresponding switching gate signals for the 2-cell 7L-ANPC.

The final gating signals for the respective switching devices are achieved directly by comparing $M_{x\text{sine}(n)}$ with the corresponding top and bottom phase-shifted sawtooth carriers using simple comparators and logic gates as shown in Fig. 7.10. Under the proposed hybrid modulating technique, the switching states in Table 7.1 are achieved based on the gating signals in Fig. 7.12.

It can be observed that the difference between the proposed hybrid ISC-PD-PWM in this chapter and the commonly employed conventional PSC-PWM approach in [99-101] is the cross degree of freedom for the three-phase reference wave signals ($M_{x\text{sine}}$) during the positive and negative cycle period. Thus, the modulating gate signals in this case can be produced without the complicated needs to rebuild the $M_{x\text{sine}}$ for the comparative logic stage.

As a result, the PSC-PWM in [99-101] can also be redefined as a hybrid carrier-based PWM since another set of phase-shifted triangular carriers can be level-shifted below the zero reference magnitude instead of having the negative cycle of $M_{x\text{sine}}$ shifted up based on the peak magnitude of triangular carrier ($\hat{V}_{\text{tri}}$). In fact, the PSC-PWM in [99-101] is equivalent to the presented advanced hybrid PSC-PD-PWM as analyzed previously in Chapter 5.

Even though similarity is found between the proposed ISC-PD-PWM and the classical PSC-PWM (PSC-PD-PWM) in [99-101], but the geometric characteristic of the carriers are totally different. Subsequently, the switching sequences are changed as well. Because of that, the performances of ANPC are greatly affected in terms of the voltage harmonic distortion which will be discussed in the following subsection.

7.4.5 Harmonic Characteristics of Proposed Hybrid ISC-PD-PWM

Fig. 7.13 Reference sinusoidal signal with two fundamental level-shifted sawtooth carrier ISC-PD-PWM.

Similar approach of analyzing the carrier-based PWM schemes using the double Fourier series is applied to the alternatively new advanced hybrid ISC-PD-PWM of Fig. 7.11. The harmonic spectrum analysis for the proposed ISC-PD-PWM is simplified using the single phase reference sinusoidal signal and the two in-phase level-shifted sawtooth carriers as shown in Fig. 7.13.

The switching function of ISC-PD-PWM is expressed in Table 7.3 which is derived based on Fig. 7.13. Since two level-shifted sawtooth carriers are used in Fig. 7.13 for analysis, therefore there are only three conditions generated which are $+V_{dc}$, $0V$ and $-V_{dc}$ following the switching condition expressed in equation (3.1).

TABLE 7.3
SWITCHING FUNCTION OF ISC-PD-PWM

$f(x, y)$	$-\pi < x < \pi$
$+V_{dc}$	$M \cos y > \frac{x}{2\pi} + \frac{1}{2}$
0	$\frac{x}{2\pi} - \frac{1}{2} < M \cos y < \frac{x}{2\pi} + \frac{1}{2}$
$-V_{dc}$	$M \cos y < \frac{x}{2\pi} - \frac{1}{2}$

In this case, the boundary conditions for two in-phase level-shifted sawtooth carriers are different from the previous advanced hybrid PSC-POD-PWM and PSC-PD-PWM. Thus, the boundary conditions for the transitions between 0V to $+V_{dc}$ and $+V_{dc}$ to 0V are given in following equations (7.15) and (7.16).

$$x_{LOWER} = -\pi \quad (7.16)$$

$$x_{UPPER} = 2\pi \left(M \cos y - \frac{1}{2} \right) \quad (7.17)$$

While achieving the $-V_{dc}$ level, the reference sinusoidal signal has to be lesser than both of upper and lower sawtooth carriers. Since the carrier used in the ISC-PD-PWM is a ramped (asymmetrical) waveform unlike those symmetric triangular carriers in the other advanced hybrid sinusoidal PWM schemes, the lower and upper boundary conditions for the transitions between 0V to $-V_{dc}$ and $-V_{dc}$ to 0V are the same for both upper carrier and lower carrier which are given in the equations (7.18) and (7.19) respectively.

$$x_{LOWER} = 2\pi \left(M \cos y + \frac{1}{2} \right) \quad (7.18)$$

$$x_{UPPER} = \pi \quad (7.19)$$

Hence, by substituting the boundary conditions equations (7.16), (7.17), (7.18) and (7.19) into (4.6), the complex form of double Fourier analysis for ISC-PD-PWM modulation can now be expressed in equation (7.20).

$$\begin{aligned}
C_{mn} &= \frac{1}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} V_{dc} e^{j(mx+ny)} dx dy \right. \\
&\quad \left. - \int_{-\pi}^{-\frac{\pi}{2}} \int_{2\pi \left(M \cos y + \frac{1}{2} \right)}^{\pi} V_{dc} e^{j(mx+ny)} dx dy \right. \\
&\quad \left. - \int_{\frac{\pi}{2}}^{\pi} \int_{2\pi \left(M \cos y + \frac{1}{2} \right)}^{\pi} V_{dc} e^{j(mx+ny)} dx dy \right] \\
&= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi}^{2\pi \left(M \cos y + \frac{1}{2} \right)} e^{j(mx+ny)} dx dy \right]
\end{aligned} \tag{7.20}$$

In order to determine the DC offset component based on the general spectrum analysis equation (4.5), the m and n in (7.20) must be equals to 0 ($m = n = 0$). The DC offset component for the ISC-PD-PWM can be determined in the following (7.21).

$$\begin{aligned}
A_{00} + jB_{00} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} e^{j(0+0)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi}^{2\pi \left(M \cos y + \frac{1}{2} \right)} e^{j(0+0)} dx dy \right] \\
&= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} [2\pi M \cos y] dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} [2\pi M \cos y] dy \right] \\
&= \frac{MV_{dc}}{\pi} \left[\sin\left(\frac{\pi}{2}\right) - \sin\left(-\frac{\pi}{2}\right) \right] + \frac{MV_{dc}}{\pi} \left[\sin\left(\frac{3\pi}{2}\right) - \sin\left(\frac{\pi}{2}\right) \right] \\
&= 0
\end{aligned} \tag{7.21}$$

By letting $m = 0$ and $n > 0$ for the equation (7.20). The baseband harmonic of the proposed ISC-PD-PWM scheme is determined in the following (7.22).

$$\begin{aligned}
 A_{0n} + jB_{0n} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} e^{j(ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi}^{2\pi \left(M \cos y + \frac{1}{2} \right)} e^{j(ny)} dx dy \right] \\
 &= \frac{MV_{dc}}{\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} [\cos y] e^{j(ny)} dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} [\cos y] e^{j(ny)} dy \right] \quad (7.22)
 \end{aligned}$$

$$\begin{aligned}
 &= \frac{MV_{dc}}{2\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \left(e^{jy(n+1)} + e^{jy(n-1)} \right) dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \left(e^{jy(n+1)} + e^{jy(n-1)} \right) dy \right] \\
 A_{01} + jB_{01} &= \frac{MV_{dc}}{2\pi} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \left(e^{jy(0)} \right) dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \left(e^{jy(0)} \right) dy \right] \quad (7.23) \\
 &= MV_{dc}
 \end{aligned}$$

The same term $e^{j(ny)}$ is found in the integral expression (7.22) which will be equal to zero for any non-zero condition of n . Thus, n can only be equated to 1 since $A_{0n} + jB_{0n} = 0$ for all conditions when $n > 1$. Let $n = 1$ for the equation (7.22), the baseband harmonic of ISC-PD-PWM can be further expressed in (7.23).

The carrier harmonic components of ISC-PD-PWM is also expressed in the expression (7.24) by having $m > 0$ and $n = 0$ for the equation (7.20).

$$\begin{aligned}
 A_{m0} + jB_{m0} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} e^{j(mx)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi}^{2\pi \left(M \cos y + \frac{1}{2} \right)} e^{j(mx)} dx dy \right] \\
 &= \frac{V_{dc}}{jm2\pi^2} \left[e^{jm(-\pi)} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \left[e^{jm(2\pi M \cos y)} - 1 \right] dy + e^{jm(\pi)} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \left[e^{jm(2\pi M \cos y)} - 1 \right] dy \right] \quad (7.24)
 \end{aligned}$$

The expression (7.24) can be further simplified to the equation (7.26) using the Bessel function integral relationships as expressed in (7.25).

$$\int e^{j(\beta)\cos\tau} d\tau = 2\pi J_0(\beta) \quad (7.25)$$

$$\begin{aligned} A_{m0} + jB_{m0} &= \frac{V_{dc}}{jm2\pi^2} \left[e^{jm(-\pi)} (\pi J_0(m2\pi M) - \pi) + e^{jm(\pi)} (\pi J_0(m2\pi M) - \pi) \right] \\ &= \frac{V_{dc}}{jm\pi} [J_0(m2\pi M) - 1] (\cos(m\pi)) \end{aligned} \quad (7.26)$$

The sideband harmonic components of ISC-PD-PWM are determined by having $m > 0$ and $n \neq 0$ for (7.20) which is expressed in the following (7.27).

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{V_{dc}}{2\pi^2} \left[\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \int_{-\pi}^{2\pi \left(M \cos y - \frac{1}{2} \right)} e^{j(mx+ny)} dx dy + \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \int_{\pi}^{2\pi \left(M \cos y + \frac{1}{2} \right)} e^{j(mx+ny)} dx dy \right] \\ &= \frac{V_{dc}}{jm2\pi^2} \left[e^{jm(-\pi)} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} e^{jny} [e^{jm(2\pi M \cos y)} - 1] dy + e^{jm(\pi)} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} e^{jny} [e^{jm(2\pi M \cos y)} - 1] dy \right] \\ &= \frac{V_{dc}}{\pi^2} \left[\frac{1}{m} [\pi J_n(m2\pi M)] \cos(m\pi) \sin\left(n \frac{\pi}{2}\right) \right. \\ &\quad \left. - j \frac{1}{m} [\pi J_n(m2\pi M)] \cos(m\pi) \cos\left(n \frac{\pi}{2}\right) \right. \\ &\quad \left. + \frac{j}{mn} \left(e^{jm(-\pi)} \sin\left(n \frac{\pi}{2}\right) + e^{jm(\pi)} \sin\left(n \frac{3\pi}{2}\right) \right) \right] \\ &= \frac{V_{dc}}{\pi} \left[\frac{1}{m} [J_n(m2\pi M)] \cos(m\pi) \left(\sin\left(n \frac{\pi}{2}\right) - j \cos\left(n \frac{\pi}{2}\right) \right) \right] \end{aligned} \quad (7.27)$$

It should be noted that the n in the $\sin(n\pi/2)$ and $\sin(n3\pi/2)$ must be odd values while the n in the $\cos(n\pi/2)$ must be even values so that these terms will not be nulled. The final spectrum analysis for the switching function of the ISC-PD-PWM can be achieved by substituting the equations (7.21), (7.23), (7.26) and (7.27) back into the fundamental (4.5). The same approach of phase-shifting the carrier and sideband harmonics is also applied for the hybrid ISC-PD-PWM using (5.21) and (5.22). Hence, the final expression for the output mL phase voltage spectrum analysis is given in the following (7.28).

$$\begin{aligned}
 V_{xn_{ISC-PD-PWM-xL}}(t) = & \frac{MV_{dc}}{2} \cos(\omega_o t + \theta_o) \\
 & + \frac{V_{dc}}{2\pi} \left(\sum_{m=1}^{\infty} \frac{1}{(Nm)} \left[J_0((Nm)2\pi M) - 1 \right] (\cos((Nm)\pi)) \right) \\
 & \quad \times \sin((Nm)[\omega_c t + \theta_c]) \\
 & + \frac{V_{dc}}{2\pi} \left(\sum_{m=1}^{\infty} \frac{1}{(Nm)} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} J_n((Nm)2\pi M) (\cos((Nm)\pi)) \right) \\
 & \quad \times \left[\begin{aligned} & \sin\left(n \frac{\pi}{2}\right) \times \cos((Nm)[\omega_c t + \theta_c] + (n)[\omega_o t + \theta_o]) \\ & - \cos\left(n \frac{\pi}{2}\right) \times \sin((Nm)[\omega_c t + \theta_c] + (n)[\omega_o t + \theta_o]) \end{aligned} \right]
 \end{aligned} \tag{7.28}$$

where

N = the total number of sawtooth carriers used in ISC-PD-PWM

Similarly, the output line-to-line voltage V_{ab} spectrum analysis for the proposed hybrid ISC-PD-PWM is expressed in the following (7.29).

$$\begin{aligned}
V_{ab_{ISC\text{PD}PWM-xL}}(t) = & \frac{\sqrt{3}MV_{dc}}{2} \cos\left(\omega_o t + \frac{\pi}{6}\right) \\
& + \frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} \left(\sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} J_n((Nm)2\pi M) (\cos((Nm)\pi)) \left(\sin\left(n\frac{\pi}{3}\right) \right) \right. \\
& \times \left. \left(\sin\left(n\frac{\pi}{2}\right) \times \cos\left((Nm)[\omega_c t] + (n)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \right) \right. \\
& \times \left. \left(-\cos\left(n\frac{\pi}{2}\right) \times \sin\left((Nm)[\omega_c t] + (n)\left[\omega_o t - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \right) \right) \right)
\end{aligned} \tag{7.29}$$

The expression (7.28) describes that the carrier harmonics are occurred at all multiples of f_c for the ISC-PD-PWM unlike those in PSC-PD-PWM (in Chapter 5). Besides that, the magnitudes of these ISC-PD-PWM carrier harmonics are also greater because of the Bessel function of order zero (J_0) term. Apart from that, it is also worth noting that there is infinite number of sideband harmonics occur around the carrier harmonics for ISC-PD-PWM. However, the magnitudes of these sideband harmonics are far much lower compared to those in the hybrid PSC-PD-PWM due to the rapid roll-off of the Bessel function (J_n) term compared to the (J_{2k-1}) term carried in the PSC-PD-PWM.

As for the output line-to-line voltage spectrum analysis in (7.29), both triplen sidebands and carrier harmonics terms in (7.28) are eliminated by its nature due to the crossover of 60° between the adjacent phase-leg reference sinusoidal signals. Thus, the magnitudes of the remaining sideband harmonics are insignificantly smaller. The spectrum analysis of the new proposed ISC-PD-PWM can be clearly observed in the Fig. 7.14 and compared against the classical PSC-PWM (alternatively equivalent to PSC-PD-PWM) used for ANPC.

Fig. 7.14 Magnified view of output voltages spectrum synthesized using PSC-PD-PWM and ISC-PD-PWM schemes.

Fig. 7.15 Comparison of output voltages THD between the hybrid PSC-PD-PWM and ISC-PD-PWM modulation schemes.

The THD comparison between both ISC-PD-PWM and PSC-PD-PWM can also be observed in Fig. 7.15. The mathematical analysis of the ISC-PD-PWM harmonic characteristics has evidently proven that the performance of the output line-to-line voltage THD is greatly enhanced for the new proposed hybrid ISC-PD-PWM compared to the PSC-PD-PWM even in the low modulation range. Such attractively low THD performances made ANPC even more beneficially suitable for any drive applications. The proposed ISC-PD-PWM in this chapter is also applicable for the proposed reduced modular cells converter in Chapter 5 previously.

7.4.6 Experimental Verification Results

The performances of the 2-cell 7L-ANPC based on the proposed MVQE control under hybrid ISC-PD-PWM is investigated using the co-simulation between PSIM v9.0.4 Simcouple and MATLAB R2010b Simulink®. The hardware prototype is developed to verify the presented studies with the aid of the dSPACE RT1103 Real-Time Workshop (RTW).

In order to verify the feasibility of the proposed MVQE in conjunction with the hybrid ISC-PD-PWM, an uncontrolled three-phase diode rectifier is connected at the front-end of the 2-cell 7L-ANPC (Fig. 7.3) so that ripples can be generated in the dc-link. Besides that, the two dc-link capacitance values are different as well to create the unbalanced neutral point effects. All the results are presented based on the detailed settings given in Table 7.4.

It is clearly observed from the experimental results that the average dc-link capacitor voltages V_{dc1} and V_{dc2} in Fig. 7.16(b) are closely tracked using the proposed regulator in the MVQE control as compared to those without control in Fig. 7.16(a). Ripples are

TABLE 7.4
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE OF
2-CELL 7L-ANPC

System Parameters	Simulation	Experiment
Reference Sinusoidal Frequency (f_o)	50 Hz	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz	1 kHz
AC Voltage Source (V_{rms})	170, 185, 155	100, 115, 85
Output DC-Link Voltage Reference (V_{dc})	300	250
Flying Capacitors ($C_{x,p}^{th}$)	2200 μ F	2200 μ F
DC-Link Capacitors (C_{dc1} , C_{dc2})	3000 μ F, 1000 μ F	2400 μ F, 1000 μ F
Load – Resistors, Inductors	25 Ω , 122 mH	37.5 Ω , 40 mH

Fig. 7.16 Experimental results of the 2-cell 7L-ANPC dc-link capacitor voltages.
(a) Without dc-link neutral-point offset regulator. (b) With regulator.

found in the dc-link because of the front-end connected rectifier which has caused the low order harmonics in Fig. 7.17(a). Thus, the low order harmonics in Fig. 7.17(a) are being mitigated away in Fig. 7.17(b) using the dc-link ripple compensator in the MVQE control scheme.

The steady-state conditions as well as the dynamic performances are also evaluated in Fig. 7.18. Despite of the ripples experienced in the dc-link in Fig. 7.18(a) and the sudden load changed in Fig. 7.18(b), the flying capacitor voltages are remained balance at their desired voltage levels. As a result, both output line-to-line voltage and output phase voltage waveforms are clearly synthesized. Hence, this means that better

stability is achieved for the ANPC from the evidenced results in Fig. 7.18 with the flying capacitor voltages tracked to the desired values at all times using the proposed voltage balancing method.

Both experimental harmonic spectrums of output stepped phase voltage and line-to-line voltage in Figs. 7.19(a) and 7.19(b) respectively have validated the analytical results in Fig. 7.14. One can conclude that high resolution waveforms especially the output line-to-line voltages are synthesized using the proposed hybrid ISC-PD-PWM scheme for the ANPC in comparison with the PSC-PD-PWM (the typically known PSC-PWM implemented for the ANPC [113-115]).

(a)

(b)

Fig. 7.17 Experimental results of the 2-cell 7L-ANPC output line-to-line voltage and the FFT spectrum. (a) Without dc-link compensator. (b) With compensator.

(a)

(b)

Fig. 7.18 Experimental results of the 2-cell 7L-ANPC performances at 0.9 Mx_{sine}.
 (a) Under steady-state condition – Output line-to-line voltage and flying capacitor voltages.
 (b) Dynamic condition – Output phase current, phase voltage and flying capacitor voltages.

The agreement between the simulation and experimental results has confirmed the feasibility of the proposed MVQE control which has successfully addressed the voltage quality issues (i) to (iii). Therefore, the overall reliability of the converter can be increased and better power quality can be achieved with the lower harmonic distorted voltage waveforms (especially the output line-to-line voltages) using the proposed ISC-PD-PWM. As such, the perceived merits of the ANPC under the proposed MVQE control with ISC-PD-PWM make it attractively applicable for its well-known medium voltage drive systems.

Fig. 7.19 Experimental results of the harmonic spectrum under proposed ISC-PD-PWM.
 (a) Output phase voltage. (b) Output line-to-line voltage.

7.5 Proposed Common Mode Reduction Technique

Common mode modulation techniques are proposed for the classical multilevel topologies as reported in [121-123], but these strategies cannot be applied directly for ANPC since hybrid synthesis method is required. Therefore, the second objective of this chapter is to offer an alternative technique to reduce the CMV using the hybrid carrier-based PWMs (conventional PSC-PWM and proposed ISC-PD-PWM) for mL -ANPC.

The CMV is typically the potential difference between the neutral point of the three-phase load (o) and the dc-link neutral point (n) as equated in (7.30) according to the output phase voltages of the inverter.

$$\text{CMV}(V_{on}) = \frac{V_{an} + V_{bn} + V_{cn}}{3} \quad (7.30)$$

As observed from (7.30), the CMV is usually created due to the differential phase voltage levels which are synthesized by the respective phase-leg under normal modulation technique. Moreover, only the odd mL output phase voltage that contains the states of zero voltage level can be controlled to achieve the complete CMV cancellation unlike those even mL inverters. Since zero output voltage level is produced in the 7L-ANPC following the Table 7.1, thus CMV elimination can only be guaranteed if the three-phase voltages in (7.30) are summed to zero at all times.

In order to produce zero CMV for the seven-level inverter, a total of $7^3 = 343$ possible combinations is now restricted to the 37 switching combinations in Fig. 7.20 without

Fig. 7.20 Vector diagram of a seven-level inverter with zero CMV states.

any redundancy. For example, the state indexes of zero CMV $\{S_A, S_B, S_C\} = \{5, 1, 3\}$ is referred to the respective phase voltage levels $\{V_{an} = +V_{dc}/3, V_{bn} = -V_{dc}/3, V_{cn} = 0\}$ at that particular switching instant. To nullify the summation of the phase voltages in (7.30), the zero CMV vectors for any mL inverter must satisfy the following condition in (7.31) through the combinational value of three-phase switching states.

$$\sum \{S_A, S_B, S_C\} = \frac{3(mL-1)}{2} \quad (7.31)$$

It is worth noting in Fig. 7.20 that the entire zero CMV vector diagram (blue lines) has been 30° phase displaced from the outer voltage hexagon lattice of a seven-level inverter (black lines). According to [122], the zero CMV vector diagram of the mL inverter (e.g., 7L-ANPC) is in fact equivalent to the simplified vectorial representation of a conventional $((mL+1)/2)$ -level (i.e., four-level) inverter comprising only the exclusive switching states.

By associating the normal carrier-based modulation strategy with the simplified vector diagram as described to achieve the common mode reduction, the zero CMV vectors are determined basically from the differences between the adjacent phase-leg switching indexes $\{S_A, S_B, S_C\} = \{S_P - S_Q, S_Q - S_R, S_R - S_P\}$ where $\{S_P, S_Q, S_R\}$ are referred as the equivalent switching indexes of $\{S_A, S_B, S_C\}$. This essential approach results a 30° phase displacement between the two vector diagrams.

For instance, for the 7L-ANPC inverter in this paper, three four-level modulators are required principally without any exceptional techniques. This means that always only half of the $(mL - 1)$ carrier bands (i.e., three reduced carrier bands C_1, C_2 and C_3) are used. The carrier bands can be sawtooth waves for the proposed ISC-PD-PWM or triangular waves for the classical PSC-PWM (PSC-PD-PWM). On account of the hybrid carrier-based PWM schemes as described previously in Section 7.4.4 – Interleaved Sawtooth Carrier Phase-Disposition PWM of this chapter, it should be noted that the magnitude of these reduced carriers is now normalized between -1 to +1. Nevertheless, the reduced carriers should remain evenly interleaved among them.

Hence, normal comparing logical rules are remained the same for the four-level modulators. The equivalent counterpart switching indexes $\{S_P, S_Q, S_R\}$ are generated independently by comparing the respective three-phase command references (V_P, V_Q and V_R) as given in (7.32) with the three phase-shifted carrier bands C_1, C_2 and C_3 .

$$\begin{aligned} V_P &= M a_{\text{sine}} \cos(\omega t) \\ V_Q &= M b_{\text{sine}} \cos(\omega t - 2\pi/3) \\ V_R &= M c_{\text{sine}} \cos(\omega t + 2\pi/3) \end{aligned} \quad (7.32)$$

Subsequently, the subtracted $\{S_{PQc}, S_{QRc}, S_{RPc}\}$ are obtained simply by the abstracting the differences between the counterpart state indexes of $\{S_P, S_Q, S_R\}$ and its adjacent phase, with respect to c as referred to the same carrier band. However, the output zero CMV vectors of mL -ANPC cannot be explicitly achieved as desired according to the above-mentioned description $\{S_A, S_B, S_C\} \neq \{S_{PQc}, S_{QRc}, S_{RPc}\}$.

Fig. 7.21 Switching pulses of equivalent counterparts (S_P and S_Q), as well as the derivation of gating signal (G_{PQ1}) with respect to the command references V_P and V_Q .

Additional modulation technique is required to modify the $\{S_{PQc}, S_{QRc}, S_{RPc}\}$ in order to achieve the zero CMV vectors. This modification is necessary due to the working principles of *mL*-ANPC which involves the low frequency operation across the switches S_{x1} , S_{x2} and their complimentary ones. Secondly, the subtracted $\{S_{PQc}, S_{QRc}, S_{RPc}\}$ create three-level PWM pulses as observed in Fig. 7.21 which cannot be served as the final gating signals.

The three-level PWM pulses (e.g., S_{PQ1} in Fig. 7.21) must be split into two set of train pulses where one set is the positive switching pulses (PS_{PQ1}) between 0 to 1 and the other set is the negative switching pulses (NS_{PQ1}) between -1 to 0. The extraction method is done by comparing S_{PQ1} with respect to a zero reference. Intrinsically, the PS_{PQ1} is obtained when S_{PQ1} is greater than zero. But, the switching pulses (NS_{PQ1}) that is being abstracted when S_{PQ1} is less than zero, must be inverted again in order to attain the desired NS_{PQ1}' that is similar to those switching transitions between -1 to 0.

It can be clearly observed from the S_{PQ1} in Fig. 7.21 that both PS_{PQ1} and NS_{PQ1} are now 30° phase-shifted with reference to V_P due to the adjacent phase subtraction $V_{PQ} = (V_P - V_Q)$. Before combining PS_{PQ1} and NS_{PQ1} to achieve the final gating signal G_{PQ1} for the switch S_{a3} in the 7L-ANPC, the 30° phase-shifted switching transitions of PS_{PQ1} and NS_{PQ1} must be extracted out from the respective positive and negative half-period of V_{PQ} . This can be done simply by multiplying the resulting logics (PV_{PQ} and NV_{PQ}) of comparing V_{PQ} with the zero reference. Same approach is applied for the remaining two interleaved carrier bands C_2 and C_3 to determine the final gating signals G_{PQ2} and G_{PQ3} respectively for the switches S_{a4} and S_{a5} .

Fig. 7.22 Proposed CMV reduction technique using hybrid carrier-based PWM modulation schemes for mL -ANPC.

The output logic of V_{PQ} and zero reference comparisons is indeed a 30° phase-shifted 50 Hz squared pulse. These low frequency squared pulses shall be the final gating signal G_A for S_{a1} and S_{a2} to satisfy the switching conditions described in Table 7.1. Meanwhile, the gating signals for the complimentary switches (S_x') can be obtained through the inverter 'NOT' gates.

The described CMV reduction technique is hence achieved using the logic gates as shown in Fig. 7.22, which is applicable for any of the two mentioned hybrid carrier-based modulation strategies (classical PSC-PWM and proposed ISC-PD-PWM). The switching signal waveforms obtained after each stage of the proposed CMV reduction technique in Fig. 7.22 can be better visualized from those switching pulses in Fig. 7.21. Ultimately, the zero CMV vectors for 7L-ANPC are now achieved $\{S_A, S_B, S_C\} = \{(G_A + G_{PQ1} + G_{PQ2} + G_{PQ3}), (G_B + G_{QR1} + G_{QR2} + G_{QR3}), (G_C + G_{RP1} + G_{RP2} + G_{RP3})\}$.

Even though the CMV magnitudes developed under the proposed hybrid ISC-PD-PWM in Fig. 7.23(b) is slightly higher than using the conventional PSC-PWM scheme in Fig. 7.23(a), but they are greatly reduced as observed in Fig. 7.24 using the

proposed CMV reduction technique. Therefore, this approach can be extended for any mL -ANPC despite of utilizing any hybrid carrier-based modulation schemes to reduce the CMV.

Fig. 7.23 Performance of 7L-ANPC without CMV reduction: (top) output phase voltage, (middle) output line-to-line voltage, (bottom) common mode voltage. (a) Conventional PSC-PWM (PSC-PD-PWM). (b) Proposed hybrid ISC-PD-PWM.

Fig. 7.24 Performance of 7L-ANPC using proposed CMV reduction: (top) output phase voltage, (middle) output line-to-line voltage, (bottom) common mode voltage.
 (a) Conventional PSC-PWM (PSC-PD-PWM). (b) Proposed hybrid ISC-PD-PWM.

7.5.1 Vector Equivalence Mapping

In the three-phase 7L-ANPC, the modulating reference signals V_X ($X = P, Q$, and R) according to the working principle of the proposed CMV reduction strategy can be divided into the following four different parts where Part I: $0.33 < V_X < M_{x_{\text{sine}}}$; Part II: $0 < V_X < 0.33$; Part III: $-0.33 < V_X < 0$; and Part IV: $-M_{x_{\text{sine}}} < V_X < -0.33$. With regard to that, the synthesis of the output line-to-line voltage can be analyzed using the arbitrary two-phase command references. Hence, the combinations of any two adjacent phases are given as follows: (II, IV), (I, IV), (I, III), (I, II), and (III, IV).

For the simplification of the analysis using the vector representation, the combination (I, IV) is used as an example here for both conventional PSC-PWM in [113-115] and proposed hybrid ISC-PD-PWM as shown in Figs. 7.25 and 7.27 respectively. Under the condition of (I, IV), V_P (red line) is greater than the three interleaved carriers C_1 , C_2 and C_3 while V_Q (green line) is lesser than C_1 , C_2 and C_3 .

By observing the synthesized three-phase voltage PWM pulses (V_{an} , V_{bn} , and V_{cn}) in both Figs. 7.25 and 7.27, multiple steps (the overlapping of layers over a carrier period T_C) are produced in the phase voltage waveforms of Fig. 7.25 by the symmetrical geometric characteristics of the triangular carriers used in the conventional PSC-PWM as compared to those in Fig. 7.27 using the proposed hybrid ISC-PD-PWM. When multiple stepped levels are generated in the waveforms over a carrier period, undesirable higher order harmonics distortion is also being introduced.

Fig. 7.25 Synthesis of output phase voltages using CMV reduction under conventional PSC-PWM (PSC-PD-PWM) scheme [113-115].

Fig. 7.26 Vector representation diagram of CMV reduction under conventional PSC-PWM (PSC-PD-PWM) scheme [113-115].

Fig. 7.27 Synthesis of output phase voltages using CMV reduction under proposed hybrid ISC-PD-PWM scheme.

Fig. 7.28 Vector representation diagram of CMV reduction under proposed hybrid ISC-PD-PWM scheme.

On top of that, the switching states of the conventional PSC-PWM in Fig. 7.25 employing the proposed CMV reduction technique are as follows: 513 – 522 – 612 – 513 – 612 – 522 – 531 – 522 – 612 – 513 – 612 – 531 – 621 – 612 – 513 – 612 – 621 – 531. Therefore, a total of five vectors 513, 522, 612, 531, and 621 are created within the carrier period as shown in Fig. 7.26 using the vector representation. Even though zero CMV vectors are achieved, but the sequences of these states under the classical PSC-PWM violate the nearest three vectors (NTV) technique.

However, it is clearly noted in Fig. 7.28 that the number of vectors utilized within a carrier period using the proposed ISC-PD-PWM scheme is greatly reduced from five to three (513, 522 and 612). Because of the asymmetrical geometric characteristics of the sawtooth carriers, the PWM pulses in Fig. 7.27 are produced accordingly to the four switching points of the carrier period (0, $T_c/3$, $2T_c/3$ and T_c). As such, the switching states are in the following sequences: 513 – 522 – 612 – 513 – 522 – 612 – 522 – 612 – 513 – 522 – 612 – 522 – 612 – 513 – 522. These sequences have conformed the NTV approach with respect to the three zero CMV vectors 513, 522 and 612 as shown in the optimized vector diagram of Fig. 7.28.

7.5.2 Spectral Harmonic Characteristics

The classical PSC-PWM scheme is popularly used in many multilevel converters especially those designs that involved flying capacitors, not surprisingly this scheme is also utilized for the mL -ANPC as reported in [113-115]. However, the typically employed conventional PSC-PWM for the mL -ANPC is an alternative hybrid carrier-based PWM scheme as described previously which is equivalent to the hybrid PSC-PD-PWM scheme. In the event of normal modulation, only half of the $(mL - 1)$ carriers are required and evenly interleaved apart which is much alike to the proposed hybrid ISC-PD-PWM scheme.

Because of the phase-shifted characteristics [85, 128] in both classical PSC-PWM and proposed ISC-PD-PWM, natural balancing for the flying capacitors can be achieved easily by connecting a balance booster filter to the load side without the need of any control scheme. Nevertheless, the phase-shifting features will cause the first group of sideband harmonics to be produced further away from the fundamental component. Basically, it is affected by the number of carriers being phase-shifted and the carrier

Fig. 7.29 Magnified view of output voltages harmonic spectrum synthesized using classical PSC-PWM [113-115] and proposed hybrid ISC-PD-PWM.

frequency. This theoretical concept does not only apply to the normal modulation, but also to the proposed CMV reduction technique.

It is proven with the spectrum analysis of the output phase voltages and line-to-line voltages as expressed in (7.33) and (7.34) for the classical PSC-PWM (alternatively PSC-PD-PWM), also (7.35) and (7.36) for the proposed ISC-PD-PWM respectively. Due to the N term in (7.33) to (7.36), it can be observed in Fig. 7.29 that the first group sideband harmonics of both hybrid carrier-based PWM schemes occurs around 60th harmonic order (3 kHz) since three phase-shifted carriers of 1 kHz are used for the four-level modulators in the CMV reduction technique.

$$\begin{aligned}
 V_{xn_{CMVR-PSCPD PWM-mL}}(t) = & \left(\frac{\sqrt{3}MV_{dc}}{4} \right) \cos \left(\omega_o t + \theta_0 + \frac{\pi}{6} \right) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} \sum_{n=-\infty}^{\infty} \left[J_n \left((Nm) \frac{\pi}{2} M \right) \sin \left(\frac{n\pi}{3} \right) \sin \left(\frac{\pi}{2} [(Nm) + n] \right) \right] \\
 & \times \cos \left((Nm) [\omega_c t + \theta_c] + (n) \left[\omega_o t + \theta_0 - \frac{\pi}{3} \right] + \frac{\pi}{2} \right) \Bigg]
 \end{aligned} \tag{7.33}$$

$$\begin{aligned}
 V_{ab_{CMVR-PSCPD PWM-mL}}(t) = & \left(\frac{3MV_{dc}}{4} \right) \cos \left(\omega_o t + \frac{\pi}{3} \right) \\
 & + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} \sum_{n=-\infty}^{\infty} \left[J_n \left((Nm) \frac{\pi}{2} M \right) \sin^2 \left(\frac{n\pi}{3} \right) \sin \left(\frac{\pi}{2} [(Nm) + n] \right) \right] \\
 & \times \cos \left((Nm) [\omega_c t] + (n) \left[\omega_o t - \frac{\pi}{3} \right] + \pi \right) \Bigg]
 \end{aligned} \tag{7.34}$$

$$\begin{aligned}
 V_{xn_{CMVR-ISC DPWM-mL}}(t) = & \left(\frac{\sqrt{3}MV_{dc}}{4} \right) \cos\left(\omega_o t + \theta_0 + \frac{\pi}{6}\right) \\
 & + \frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} \sum_{n=-\infty}^{\infty} \left[\begin{aligned} & J_n((Nm)\pi M) \sin\left(\frac{n\pi}{3}\right) \\ & \times \left(\sin\left(n\frac{\pi}{2}\right) \times \cos\left((Nm)[\omega_c t + \theta_c] + (n)\left[\omega_o t + \theta_0 - \frac{\pi}{3}\right] + \frac{\pi}{2}\right) \right. \\ & \left. + \cos\left(n\frac{\pi}{2}\right) \times \sin\left((Nm)[\omega_c t + \theta_c] + (n)\left[\omega_o t + \theta_0 - \frac{\pi}{3}\right] - \frac{\pi}{2}\right) \right) \end{aligned} \right]
 \end{aligned} \tag{7.35}$$

$$\begin{aligned}
 V_{ab_{CMVR-ISC DPWM-mL}}(t) = & \left(\frac{3MV_{dc}}{4} \right) \cos\left(\omega_o t + \frac{\pi}{3}\right) \\
 & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{(Nm)} \sum_{n=-\infty}^{\infty} \left[\begin{aligned} & J_n((Nm)\pi M) \sin^2\left(\frac{n\pi}{3}\right) \\ & \times \left(\sin\left(n\frac{\pi}{2}\right) \times \cos\left((Nm)[\omega_c t] + (n)\left[\omega_o t - \frac{\pi}{3}\right] + \pi\right) \right. \\ & \left. - \cos\left(n\frac{\pi}{2}\right) \times \sin\left((Nm)[\omega_c t] + (n)\left[\omega_o t - \frac{2\pi}{3}\right] - \pi\right) \right) \end{aligned} \right]
 \end{aligned} \tag{7.36}$$

According to the double Fourier Series expressed (7.33) to (7.36), all the carrier harmonics terms are being removed away when obtaining the (S_{PQc} , S_{QRc} , S_{RPc}). Besides that, the crossover intersection of these adjacent phase reference signals will also cancel away the triple sideband harmonics naturally, which explains the $\sin(n\pi/3)$ terms carried in these expressions.

However, the alterations in the geometry of the carrier will generate the sideband harmonics differently as well. For the classical PSC-PWM (alternatively equivalent PSC-PD-PWM), both (7.33) and (7.34) describe that odd sideband harmonics occur around even N multiples of f_c and vice versa even sideband harmonics occur around

odd N multiples of f_c . On the contrary, an infinite number of sideband harmonics are found at all N multiples of f_c for the proposed ISC-PD-PWM in (7.35) and (7.36).

Despite of such differences, it is necessarily to highlight the magnitudes of the sideband harmonics in the PSC-PWM are twice greater than those in the proposed hybrid ISC-PD-PWM scheme. Together with the cancellation of the triplen sideband harmonics, the harmonic profile is proven to be greatly enhanced for the proposed ISC-PD-PWM modulation as compared to the classical PSC-PWM (PSC-PD-PWM) in Fig. 7.30.

Fig. 7.30 Comparison of output voltages THD performance under CMV reduction technique.

Fig. 7.31 Comparison of output voltages WTHD performance under CMV reduction technique.

Based on the proposed CMV reduction approach, the total harmonic distortion (THD) of the respective output phase voltages and line-to-line voltages are identically same since both voltages share the same spectral harmonic characteristics. Given the proven facts that higher resolution voltage waveforms can be produced using the ISC-PD-PWM, thus the input filter size can be further reduced as THD is popularly used as a figure of merit for filter designing.

While in the case of motor drive applications, it is necessary to analyze the current harmonic performances based on the two hybrid modulation schemes used for the ANPC. Hence, the current THD can be predicted using the load independent metric which is the weighted total harmonic distortion (WTHD). The comparative result in Fig. 7.31 shows that the CMV reduction technique under the proposed ISC-PD-PWM achieves much lower output current THD except for the case of under-modulation conditions ($M_{x\text{sine}} < 0.33$).

7.5.3 Switching Frequency Reduction

When implementing the symmetrical geometry of the triangular carriers in both the normal modulation technique and the CMV reduction strategy, it should be noted that the next switching state will be remained the same as the previous conditions whenever a carrier period is over. The continuous switching transitions can be clearly observed in Fig. 7.32 for the triangular PWM modulation.

However, these continuous switching transitions can be eliminated away by changing the carrier shape to the asymmetrical ones (sawtooth). Hence, the switching transitions for the sawtooth PWM modulation are now between the consecutive carrier periods. Therefore, the number of switching transitions is significantly reduced using the sawtooth carrier. The reduction of switching transitions would be more obvious every time when the reference signal Mx_{sine} crosses over the zero reference magnitude in Fig. 7.32.

Fig. 7.32 Switching conditions based on different geometry characteristics of the carriers during modulation.

As such, the average switching frequency of the converter is determined by taking the mean of the total switching frequency across the switches S_{x1} , S_{x2} , S_{x3} , S_{x4} and S_{x5} for the case of the 7L-ANPC here. The comparative result between the classical PSC-PWM and the proposed ISC-PD-PWM schemes employed in the CMV reduction technique is shown in Fig. 7.33. It is evidently proven that the proposed hybrid ISC-PD-PWM had remarkably reduced the average switching frequency especially for the low modulation indices.

Fig. 7.33 Comparison of average switching frequency under the proposed CMV reduction technique.

Fig. 7.34 Total distributed losses comparison of a 7L-ANPC phase-leg under the proposed CMV reduction technique.

7.5.4 Power Device Losses

The total distributed losses (total switching loss and total conduction loss) of the discrete components are shown in Fig. 7.34 based on the low rated power conditions given in Table 7.5. The loss comparison is evaluated between the two modulation schemes (classical PSC-PWM and proposed hybrid ISC-PD-PWM) under the CMV reduction method based on different modulation indices. The results have clearly showed that both conduction loss and switching loss are notably decreased for the ANPC employing the proposed ISC-PD-PWM modulation scheme.

It is worth noting that the differences in the total distributed losses between the ISC-PD-PWM and the PSC-PWM are relatively smaller especially during the under-modulation condition ($M_{x_{\text{sine}}} < 0.33$). This is due to the high conduction loss being incurred in this case since it is greatly affected by the expectedly poor current harmonic performance based on the voltage WTHD in Fig. 7.31.

Nevertheless, the total distributed losses for ISC-PD-PWM are still considerably lower because of the greatly reduced switching loss. It is clearly owing to its asymmetrical wave that eliminates the continuous switching transitions. Hence, the ANPC converter employing the proposed hybrid ISC-PD-PWM features higher efficiency than the classical PSC-PWM modulation scheme (alternatively equivalent PSC-PD-PWM).

7.5.5 Experimental Verification Results

The proposed common mode reduction technique using both classical PSC-PWM and proposed ISC-PD-PWM is applied to the three-phase 7L-ANPC. The performance is co-simulated between PSIM v9.0.4 Simcouple and MATLAB R2010b Simulink® as well as validated experimentally with the aid of dSPACE RT1103 Real-Time Workshop (RTW). All the results are presented based on the detailed settings given in Table 7.5.

The output voltages of the 7L-ANPC in Fig. 7.35 are clearly synthesized using normal modulation technique based on both discussed hybrid PWM schemes. The CMV under the proposed ISC-PD-PWM in Fig. 7.35(b) is slightly distorted as compared to the CMV under the classical PSC-PWM in the Fig. 7.35(a). However, the common mode voltages are significantly reduced in Fig. 7.36 by applying the proposed common mode reduction technique to the ANPC. It is also noted that the CMV in Fig. 7.36(b) is now much reduced than the one in the Fig. 7.36(a). Even though the CMV is supposed to be totally eliminated as simulated in Fig. 7.24, but those spikes as seen in Fig. 7.36 are caused by the dead-time interval effects.

TABLE 7.5
CONFIGURATION SETTINGS FOR SIMULATION AND HARDWARE PROTOTYPE
OF 2-CELL 7L-ANPC

System Parameters	Settings
Reference Sinusoidal Frequency (f_o)	50 Hz
Triangular Carrier Frequency (f_c)	1 kHz
Modulation Amplitude ($M_{x_{sine}}$)	0.9
DC Voltage Source	250 Vdc
DC-Link and Flying Capacitors ($C_{x,p}^{th}$)	2200 μ F
Load – Resistors / Inductors	37.5 Ω / 40 mH
Filter – Resistors / Capacitors	4 Ω / 25 μ F

(a)

(b)

Fig. 7.35 Experimental results of 7L-ANPC under normal modulation technique – (top) output phase voltage, (middle) output line-to-line voltage, (bottom) common mode voltage.

(a) Conventional PSC-PWM. (b) Proposed hybrid ISC-PD-PWM.

The harmonic spectrum of the output phase voltages and line-to-line voltages for the 7L-ANPC employing the CMV reduction approach is shown in Figs. 7.36 and 7.37 respectively under different PWM schemes. The magnitudes of the sideband harmonics in the classical PSC-PWM as shown in Figs. 7.36(a) and 7.37(a) are approximately twice greater than those in the proposed ISC-PD-PWM in Figs. 7.36(b) and 7.37(b).

Fig. 7.36 Experimental results of 7L-ANPC using the proposed CMV reduction technique – (top) output phase voltage, (middle) output line-to-line voltage, (bottom) common mode voltage. (a) Conventional PSC-PWM. (b) Proposed hybrid ISC-PD-PWM.

Moreover, the experimental harmonic spectrums are exactly matched with the analytical results in Fig. 7.29. Thus, one can conclude that high resolution waveforms are synthesized for the ANPC when employing the proposed ISC-PD-PWM scheme in conjunction with the CMV reduction technique. The agreement between the simulation and the experimental results has also confirmed the feasibility of the proposed CMV reduction technique as well as the enhanced THD and WTHD performances achieved using the proposed ISC-PD-PWM.

Fig. 7.37 Experimental result of 7L-ANPC output phase voltage and its FFT spectrum.
 (a) Conventional PSC-PWM. (b) Proposed hybrid ISC-PD-PWM.

In addition to that, the asymmetrical geometry of the sawtooth carriers eliminates the continuous switching transitions which results a great reduction in the switching frequency of the power devices. Because of these features, the efficiency of the ANPC is further improved as well with the total device power losses significantly decreased especially under the low rated power condition. As such, the perceived merits of employing the proposed technique with the hybrid ISC-PD-PWM modulation makes ANPC more attractively fitted for its well-known MV drive systems.

Fig. 7.38 Experimental result of 7L-ANPC output line-to-line voltage and its FFT spectrum.
 (a) Conventional PSC-PWM. (b) Proposed hybrid ISC-PD-PWM.

Chapter 8

Conclusions and Future Works

This last chapter will present the final conclusion of the research work which has addressed the problems and challenges encountered by worldwide researchers and industry professionals. Even though the proposed concepts in this research are verified with simulation and experimental prototypes to prove its feasibility, but still there are many more issues which could not have been discussed in this report yet. Hence, these created motivations to carry out plans for continuing direction for the research works.

8.1 Conclusions

Multilevel converters are well-known for high power application due to its ability of synthesizing high number of output voltage levels, which can provide a more efficient energy conversion with excellent power quality. Hence, the literature review of those multilevel converters that are available in the industrials is carried out to study the advantages and disadvantages of each topology design. The addressed limitations of each multilevel topology encourage research work to come out with possible solutions.

Modulation methods are one of the principal elements in designing multilevel converters, which will eventually affect the synthesized voltage waveforms and current quality. This motivates to carry out further research on the existing switching schemes. There are various types of modulation methods which are classified mainly into the SVM and CBM as well as the classification based on switching frequency operation.

SVM requires heavy computational effort and complex algorithms while CBM can be achieved with simplest approach to modulate the desired gating signals. This explains why CBM is popularly chosen over SVM in the industrial applications even though both have high switching frequency except for nearest vector selection, nearest level selection and selective harmonic elimination methods. SPWM is one of the modulation methods classified under the CBM category. Hence, the study on the conventional SPWM is done, especially with the PSC-PWM which is one of the most commonly used modulation schemes in many multilevel converter topologies.

The advantages and problems of both LSC-PWM and PSC-PWM are analyzed and addressed to enable a more in-depth research studies and explore new modulation schemes. Two modulation schemes are proposed in this report with the aim to attain the advantages of both LSC-PWM and PSC-PWM. The proposed modulation strategies are the hybrid combination of both LSC-PWM and PSC-PWM. The two proposed hybrid SPWM schemes are named as PSC-POD-PWM and PSC-PD-PWM.

Mathematical analysis is derived for both proposed hybrid SPWM methods to demonstrate the respective harmonic characteristics. The experimental results have verified the analytical works and also demonstrated its feasibility. Comparative analysis has proven that good output voltage quality can be achieved using the proposed hybrid SPWM methods especially the PSC-PD-PWM. Moreover, the proposed PSC-PD-PWM can achieve the same mL output voltage with 50% reduction of n_{tri} needed for modulation as compared to other SPWM. Meanwhile both proposed modulation schemes have successfully reduced overall switching frequency without affecting the THD performance. Thus, the issue of EMI can be avoided now.

Among many classical and recent advanced multilevel converter topologies, MFCI is one of the most attractive multilevel designs. The problems of unbalanced voltage condition in the dc-link will not be encountered in MFCI unlike MDCI, even though both are single dc-link configuration. On top of that, no bulky phase-shifted transformer or multiple isolated DC sources is required as compared to the MCHB. Furthermore, MFCI allows the flexibility in extending for higher mL output voltage due its modularity design. Apart from that, voltage balancing is not an issue since MFCI has inherent natural-balancing capability. However, MFCI is still not favorable in many high power applications despite of these advantageous properties compared to other topologies. This is due to its high switching frequency operation caused by the PSC-PWM methods as well as the increasing flying capacitance energy storage.

Synthesizing higher mL output voltage is always desired for any multilevel topologies, but eventually this leads to an increase in the total number of components required which is one of the most common problems faced. The increase of component counts does not only affect the overall size but also makes the design impractical to realize with the limitation of the physical hardware. Moreover, the reliability of the converter will also be affected. In the case of MFCI, the increase in number of cells leads to the large inrush current during the initial transient period because of the flying capacitors involved in the design. The increased amounts of energy storage will take longer time for the converter to reach its steady-state and at times may also lead to the unbalanced flying capacitor voltages condition despite of the aid with the booster filter. Lastly, the chances of generating EMI are very high in MFCI with the PSC-PWM methods due to the phase-shifted n_{tri} carriers implemented for modulation.

Two different reduced modular cell inverter topologies are proposed to overcome the challenges faced in the classical MFCI when designing for higher medium voltage drive applications. The reduced modular cell inverters are the lightweight flying capacitor inverter (LFCI) and the reduced flying capacitor inverter (RFCI) which both can synthesize higher mL output voltage levels with the component counts significantly reduced using the hybrid SPWM schemes (PSC-POD-PWM and PSC-PD-PWM). Experimental results have verified the proposed concepts and proven its feasibility with the hardware prototype. A comparative analysis between MFCI, LFCI and RFCI is discussed to demonstrate the improvements made.

Inherent natural balancing has been proven to be well retained with the aid of balance booster filter for the proposed RFCI as compared to the proposed LFCI. Hence, a simple closed-loop voltage balancing scheme using proportional control based on the hybrid PSC-PD-PWM is also proposed for the RFCI in the thesis. The feasibility of the control scheme for RFCI is validated through a series of dynamic experimental condition such as sudden stepped change in the modulation index and the unbalanced load conditions. Nevertheless, there are tradeoffs between the balance booster filter and the closed-loop control for having the flying capacitor voltages tracked to the desired values at all times to increase the converter stability.

The proposed reduced flying capacitor approach is attractively investigated for the performing rectifier operation (RFCR). By doing so, the proposed RFCR does not only topologically reduce the component counts but also allow having bidirectional power flow (four quadrants operation) unlike those recent multilevel rectifier topologies. A unity power factor control together with the flying capacitor voltage balancing scheme

are experimented to prove the feasibility of the proposed RFCR. Dynamic conditions such as power factor variations and load changed are also evaluated to validate the four quadrant operation. Comparative investigations are carried out to conclude that the proposed RFCR has successfully reduced the power losses while shaping the input current waveforms with smaller line inductance filter.

The thesis also studies the popular active neutral point clamped (ANPC) inverter which is well-known for its industrial higher medium voltage drives compared to the classical NPC and MFCI. Since it is hybrid configuration between the NPC and the MFCI, the converter can synthesize higher mL output voltage levels with reduced component counts. Nonetheless, the output voltage quality will be a major concern due to the capacitors involved in the converter design. Many research works are reported in the literatures which treat the voltage quality issue separately with different modulation schemes. Therefore, a multiple voltage quantities enhancement (MVQE) control is proposed to address the important topics such as balancing the neutral potential and the flying capacitor voltages as well as reducing the dc-link ripple contents. The output voltage quality is further enhanced with another new proposed hybrid interleaved sawtooth carrier phase-disposition PWM (ISC-PD-PWM). The feasibility of the MVQE control under the proposed hybrid ISC-PD-PWM scheme is validated experimentally.

The common mode voltage (CMV) reduction technique is also proposed for the ANPC because of its well-known drive applications since no investigation are explored in the literature yet. The proposed CMV reduction technique is designed based on the operating principles of the ANPC using the industry's most favorable SPWM schemes.

The proposed hybrid ISC-PD-PWM is implemented for the CMV reduction technique in this case and compared with the classical PSC-PWM modulation scheme (which is proven to be equivalent to PSC-PD-PWM) for the ANPC. The common mode voltage is greatly reduced as demonstrated in the experimental results. In addition to that, the average switching frequency of the ANPC converter is greatly reduced, thus allowing the total power semiconductor losses to be remained low at all times when using the enhanced harmonic profile of new hybrid ISC-PD-PWM scheme.

This thesis investigates the challenges faced in the classical multilevel converters which restricted engineers to design higher voltage drive systems. Topologically reduced multilevel power converters are hence proposed to overcome those issues with their feasibility experimentally proven. On top of that, new hybrid SPWM schemes are designed for these proposed converters to further enhance the converter performances in terms of voltage and current quality, filter size and power device losses. Multiple enhancements are also made for the industrial available multilevel ANPC to improve the voltage quality issues and reduce the common mode voltage. The research works presented in this thesis will be a stepping stone to the future directions for the continuous research work.

8.2 Future Directions

The aim of the research work was to study the multilevel converters and its practical roles in the industry. Further investigation was carried out to find out the reasons behind that have restricted the industrials to move forward despite of many new ideas and research works contributed by worldwide researchers up to date. Hence, the research work will be focused on solving the addressed limitations and optimizing the design of multilevel converters to achieve better efficiency.

Proposed reduced modular cell (RFCI and LFCI) approach has been presented and successfully overcome the major problems faced in the conventional MFCI. New hybrid SPWM schemes are also especially designed for the proposed converters to greatly enhance the harmonic profile of the voltage and current waveforms. The hybrid SPWM schemes are proven theoretically and experimentally to have well-retained the advantages of the classical modulation schemes. Even though comparative analysis is done, but there are still rooms for further improvements and investigations on the proposed converters.

The proposed LFCI can be much more attractive compared to the second proposed RFCI with the component counts and the power losses greatly reduced. However, the overly reduced redundant switching states made LFCI to have problem achieving balanced flying capacitor voltages at all times especially during the low modulation index control as stated in Chapter 5.1. Thus, it is worth to design a closed-loop voltage balancing control for the LFCI which can increase the stability and the reliability of the converter.

On the other hand, better voltage balancing performance is achieved for the second proposed RFCI. But a simple closed-loop voltage balancing scheme using proportional control is still proposed for the RFCI. It should be noted that the number of voltage sensors for measuring the flying capacitor voltages is huge which resulted a higher cost implementation. Proposing a reduced sensor closed-loop flying capacitor voltage balancing control with fault tolerance capability would be a promising solution to increase the converter reliability. However, most of the modular cell topologies are still heavily dependent on the natural-balancing technique with the aid of booster filter at the output of the converter, so that the flying capacitor voltages can be achieved balance easily. Hence, the optimum sizing of the booster filter has to be analyzed with the dynamic performance tests.

Electrolytic capacitor is one of the principal components used in multilevel modular cell inverter topologies to synthesize the output voltage stepped waveforms. On top of that, electrolytic capacitors are also commonly used in many other multilevel converter topologies. Noting that electrolytic capacitor is also the only component with lowest reliability in the power electronic converters due to its lifetime cycles which is affected by the amount of charging and discharging, the voltage stress and the temperature. Therefore, it is important to optimize the size of these electrolytic capacitors in the converters or even having the capacitors being replaced with those film or ceramic materials. Future research work can also investigate the performance of these flying capacitors in the classical MFCI, proposed LFCI and RFCI based on different capacitance materials, modulation strategies and switching frequency so that optimum performances can be achieved while minimizing the size of these capacitors. By doing so, this allows the global reliability of the converter to be improved as well.

Apart from analyzing the switching losses and the conduction losses across the respective semiconductor devices of the proposed converters, it is also interesting to further investigate the thermal performance under severe environmental conditions since different voltage stresses are experienced. Typically, the thermal stress across each device is different when the power is not equally distributed. As a result, the heat sink designs as well as the semiconductor device ratings will be affected. These factors should be considered for optimizing the converter design.

With the loss distribution presented, the dominant conduction loss of the particular switching devices can be replaced with the silicon carbide (SiC) semiconductor devices. Future work can also explore on the hybrid combination of different semiconductor materials to achieve optimum performance for the proposed converters. By doing so, this could avoid the increase of cost implementation while minimizing the losses occurred in the converters.

Moving forward with the future trends of achieving higher mL output voltage with reduced number of component counts, alternative new multilevel converter topologies can be designed to overcome the existing limitations of the classical multilevel converters. New multilevel converter designs shall involve the hybrid combinations, for instance by clamping two different structured poles to form a single phase-leg configuration. Thus, modularity can be well-retained to allow flexibility in the converter design. Proposing hybrid structured multilevel converters could highly possible overcome the existing problems faced in the classical converters. The proposed improvements for the future works focus on optimizing the converter design so that the research concepts can be realized in practice to meet the industrial needs.

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