Design of continuous-time delta sigma converters for high fidelity audio applications

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DESIGN OF CONTINUOUS-TIME DELTA SIGMA CONVERTERS FOR HIGH FIDELITY AUDIO APPLICATIONS

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Abstract

Audio signal processing is one system that demands high resolution A/D converters. The healthy human ear can decipher sound with intensities varying from 0~3dB to more than 160dB (Sound Pressure Level) SPL with a theoretical frequency bandwidth of up to 20~25kHz. Traditional audio signal processing channels rely on standalone modules where each component is optimized in their own chosen technology. Consequentially, high fidelity but huge products result. The luxury of having a higher supply voltage for the noise sensitive analog circuitries whereas a lower supply voltage in speed demanding digital processing circuits addressed the ADC resolution. Recent audio codec systems present a set of different requirements. Heavy Digital Signal Processing (DSP) fueled with cost and aesthetics of the final product demand a consolidation of components along the audio signal processing channel.

The Continuous-Time (CT) $\Delta\Sigma$ modulator offers a number of advantages over its discrete counterpart in some fields of application. Traditionally, the DT $\Delta\Sigma$ modulator has dominated this market. The moderately low bandwidth requirement (i.e. 20 kHz–25 kHz) means the design of OTAs with a reasonable speed consuming an acceptable power can still be achieved. In order to maximize the suppression of quantization noise, ADC designers resort usually to either high order (4-6) or multibit feedback DAC structures; not to mention the usage of high OSR of above 64. However in the advent of nanoscale technology, the former apparent choice of DT architectures becomes less justifiable. Feature size down scaling with technology advancements gives rise to weaker devices that can only tolerate low supply voltages. The input dynamic range of the frontend Sample and Hold (S/H) ADC buffer has to be maximized under the constrained VDD supply

while maintaining linearity. This warrants the use of more complicated switching control techniques such as boot strapping. On the other hand, the inputs to a CT $\Delta\Sigma$ modulator can be built without a S/H buffer with the possibility of reaching high input dynamic ranges via linear resistors of a opamp RC integrator. This generates interest in the research for high resolution ADCs for high fidelity audio applications in advanced nanoscale technologies.

This work researches into the design of CT $\Delta\Sigma$ modulators targeted for high fidelity audio applications. The literature review chapter presents an evolution of oversampling CT $\Delta\Sigma$ modulators in this field of area. Subsequently, high level detailed modelling will be discussed leading to the development of a circuit-based model for rapid verification that shorten optimization turn-around time. Two CT $\Delta\Sigma$ modulators with different architectural approaches are presented. Chapter 5 described the realization of a 4th order CT $\Delta\Sigma$ modulator. System level non-idealities such as clock jitter uncertainties and process variation tolerance were discussed and relaxed with proposed circuitries. This modulator, implemented in 180nm technology with a supply of 1.5V was fully verified in simulation and achieved an SNR/SNDR of 90.6dB/88.7dB with a reasonable input dynamic range of differential peak-to-peak of 2V while consuming a current consumption of only 153 μ A. Chapter 6 proposed a third order audio CT $\Delta\Sigma$ modulator developed in advance 65nm standard CMOS technology. To enhance the NTF, Noise Coupling (NC) was applied in a second order ClFF architecture. The input dynamic range achieved a differential peak-to-peak voltage of 2V even at the ultra-low supply of 1V considering such a high resolution design target. The modulator achieved a measured DR/SNR/SNDR of 103.1dB/100.1dB/95.2dB while dissipating 0.8mW.

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List of Notations

Abbreviations and Acronyms

ACR	Active Comparison Region
AD	Analog-to-Digital
ADC	Analog to Digital Converter
ADSM	Asynchronous Delta Sigma Modulator
BJT	Bipolar Junction Transistor
BW	Bandwidth
CDF	Cumulative Density Function
CIFB	Cascade of Integrators with Distributed Feedback
CIFF	Cascaded Integrators Feed Forward
CM	Common Mode
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CRFB	Cascade of Resonators with Distributed Feedback
CT $\Delta\Sigma$	Continuous-Time Delta Sigma
CT	Continuous Time
CTF	Continuous-Time Filter
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DLTC	Delay-Line based Timing Control
DM	Differential Mode
DR	Dynamic Ranges
DSP	Digital Signal Processing
DT $\Delta\Sigma$	Discrete Time Delta Sigma
ELD	Excess Loop Delay
ELD FL	Excess Loop Delay Feedback Loop

EMI	Electromagnetic Interference
FDCSC	Floating Differential Charge Storage Capacitor
FF	Feed Forward
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FOM	Figure of Merit
FS	Full Scale
GBW	Gain Bandwidth
GF	Global Foundries
gmC	Transconductor Capacitor
HRZ	High-Return-to-Zero
ISI	Intersymbol Interference
JIE	Jitter Immunity Enhancement
JIR	Jitter Impulse Response
LDO	Low Dropout
LSB	Least Significant Bit
LTF	Loop Transfer Function
MASH	Multi-Stage Noise Shaping
MBQ	Multi-Bit Quantizers
MEM	Microelectromechanical
MFL	Main Feedback Loop
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSA	Maximum Stable Amplitude
MSB	Most Significant Bits
NC	Noise Coupling
NCFL	Noise Coupling Feedback Loop
NMOS	N-Channel Metal Oxide Semiconductor Field Effect Transistor
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OOB	Out of Band
OOBG	Out of Band Gain

OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PDF	Probability Density Function
PMOS	P-Channel Metal Oxide Semiconductor Field Effect Transistor
PSD	Power Spectral Density
PTAT	Proportional to Absolute Temperature
PVTE	Process Variation Tolerant Enhancement
RC	Resistor Capacitor
RZ	Return-to-Zero
S/H	Sample and Hold
SA	Successive Approximation
SAB	Single Amplifier Biquad
SAR	Successive Approximation Register
SARCP	SAR Comparison Phase
SC	Switch Capacitor
SCR	Switched Capacitor Resistive
SLD	Shifted Loop Delay
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
SPL	Sound Pressure Level
SQNR	Signal to Quantization Noise
SR	Slew Rate
STF	Signal Transfer Function
TDC	Time to Digital Converter
UGBW	Unity Gain Bandwidth
V/I	Voltage-to-Current
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
ZOH	Zero Order Hold

Chapter 1 Introduction

Abstract This chapter discusses the motivation of research into high resolution CT $\Delta\Sigma$ modulators. The application of a digital hearing aid is used to highlight the advantages of having a CT $\Delta\Sigma$ modulator developed in advanced nanoscale technology. This chapter also presents the thesis organization.

1.1 Motivation

1.1.1 High Performance Audio ADC Application

In the development of high fidelity audio applications, the management of signal channel integrity is of paramount importance. Each component within the signal acquisition chain has to be optimized for the audio signal without distortion. Of the constituting circuit blocks, the ADC is a major impediment in achieving a high overall channel dynamic range. Modern digital audio codec roadmaps reveal the trend of utilizing higher resolution oversampled $\Delta\Sigma$ modulators rather than lower resolution companding techniques. One such application observing this advance is the hearing aid. In general, the requirement for higher resolution ADCs in a hearing aid is fueled by the requirements for music hearing [1]. There are two major differences between speech and music hearing. In speech, the average amplitude level is about 65dB SPL at a distance of 1m. On the other hand, music, can reach high amplitudes of 100dB SPL. One reason is because it can be derived from various sources such as through earphones, speakers or a concert stage. Another

difference is between the average level and the peak sound known as the Crest Factor (CF). In speech, the CF is about 12dB while it can vary from 18-20dB for music.

The typical digital hearing aid uses a 16b ADC to convert the microphone output to the digital code required for DSP. The dynamic range is therefore limited to 96dB at the input of the ADC. The hearing aid is normally tuned to receive from 7dB-103dB SPL. In doing so, various compression schemes have evolved to allow a contiguous fit into the ADC dynamic range. They can be broadly categorized into 3 major types [2], namely Compression Limiting (CL), Automatic Volume Control (AVC) and Wide Dynamic Range Compression (WDRC). Compression Limiting is performed by providing a linear gain to attenuate the input when the compression threshold is reached. AVC is similar to CL. The difference is in a prolonged release time upon activation above compression threshold. As a result of the long release time, the input remains low after the compression cycle. This reduces the need to adjust the volume control. The WDRC does not provide a linear gain to all input signal intensity range. Instead, it applies a gain to low intensity signals while attenuation to the higher intensity ranges respectively. As a result, softer sounds can be heard while loud sounds can be prevented from clipping distortions due to the limitation in the ADC, hence making it the best compression technique utilized by modern hearing aids.

However, although the WDRC can be very effective in speech hearing, it is not ideal for music hearing. This is because it is important to preserve both the temporal and spectral properties of music to create the best acoustic performance. Hence, the hearing aid with WDRC had to be custom tuned for speech or music hearing. For example, due to the higher CF of music (18-20dB), the compression threshold should be tuned 5-8dB higher.

In addition, the compression attack and release time had to be made faster to cope with quick tonal intensity changes in music.

Due to the above discussed inconveniences, another scheme was proposed. This method manipulates the input dynamic range to the ADC by upshifting the detection limits to about 15-111dB SPL. With this, the hearing aid can cope with the high CF of music without having to pre-distort the input signal. [3] had shown that this technique is preferred as compared to the other compression schemes. However so, it should be noted that due to the less sensitivity to low intensity signals, speech in noisy environments are not significantly improved.

Fig.1.1 shows the manipulation of sound passing through a typical digital hearing aid that is fitted with WDRC. Due to hearing impairment, the receiving DR at the human ear is much reduced. The MEM microphone is sensitive enough to receive up to 125dB.

Fig. 1.1 Illustration of sound processing through a hearing aid fitted with WDRC scheme

With the WDRC scheme, the input to the ADC is attenuated at high intensities while amplified at the other lower extreme. The orange shaded area shows the input range that will be either compressed or magnified by WDRC. The compression and amplification thresholds are set differently to optimize for speech or music. When adjusted for music, due to the high CF and larger DR, the attenuation threshold is typically brought higher. The ratio of the original signal amplitude to the final amplified or compressed signal is known as the amplification and compression ratios respectively. Fig.1.1 shows the sound processing with a 16b ADC. As can be seen, if the ADC resolution is brought higher, the attenuation and amplification ratios can be reduced, which will ideally be better to preserve the tonal and spectral characteristics of a musical signal. After the ADC, DSP post processing is then applied to produce the sound best suited to the patient's hearing condition.

Recently, it had been reported that hearing aids with high resolution (24b) ADC is gaining popularity [4-5]. With this, input signals can reach the ADC and finally the DSP without any prior distortion. This implies the digital post processing can be optimally tuned to cope with differences in individual hearing profiles. This paved the first motivation for research of high resolution ADC in nanoscale technology.

In addition, due to the miniaturized physique of a typical hearing aid, it is important for the hearing aid to be constructed with minimal number of components. The state of art hearing aid may consist of a mechanical microphone frontend which can be packaged together or separately with the ADC. It is in the vision of this research to have the ADC fabricated with the digital DSP backend. This is only possible if the high resolution ADC can be realized in an advanced nanoscale technology. This is important to keep the digital

power of the DSP down. When this is achieved, the inclusion of the mechanical MEM microphone, the ADC with the DSP can result in a single package solution for the main signal processing channel. This is the second motivation for the research of high resolution ADC in nanoscale technology.

1.1.2 Optimized System Level Architecture

In the words of Bob Adams, a Fellow and manager of audio development for high-end audio applications [6], “...many engineers no longer use discrete ADCs, but design with audio codecs instead. You can get from one to eight ADCs and two to eight DACs in one codec package. The dynamic range of these codecs can be as high as 100 dB, which makes them a suitable choice for many consumer applications. Many of these devices also offer low power consumption for portable devices...”

The reason for this trend is supported by the need for the development of devices with a shrinking feature size. The platform physical area of a circuit board translates directly to cost implications. From the aesthetics viewpoint, it is also more desirable to have a device that is smaller in nature.

Due to this shift in paradigm, high performance ADCs have to be integrated in multiple channels within the same SoC. The SoC silicon area has to be minimized for cost reasons. As such, it becomes beneficial to utilize technologies with smaller feature sizes for area, speed and performance trade-offs of the typically heavy digital counterpart. The usage of nanoscale advanced technology can be detrimental to the design and implementation of analog circuitries especially the ADC. To be feasible, the ADC has to meet high SNR

requirements at low supply voltages in a typical nanoscale CMOS technology, which is a challenge in current state of the art designs.

1.1.3 Integration of Multi ADC Channels SoCs

Compacting the overall application board into a single SoC has been the objective of many IC developers. Operating multi-channel adjacent ADCs can be problematic due to several reasons. Firstly, the high integration level can cause cross-coupling of switching noise through the substrate. Conversion along adjacent channels that possess heavy switching can degrade the inter-channel isolation, hence resulting in a poorer channel distortion level. Secondly, the usage of input sampling ADCs have to be managed for EMI emissions. The effect of this is primarily due to the sampling of charges which resulted in glitches of current back flowing into the signal source [7]. This phenomenon is aggravated in high resolution DT ADCs where the sampling capacitors have to be huge to minimize the kT/C_s noise. This is especially important in automotive applications that are highly sensitive to EMI interferences. This effect can be worse with the implementation of multi-channel SoCs. Thirdly, the operation of multiple ADCs together can be an issue if they require numerous reference voltages. This is because such reference lines can be a channel for noise and kickback propagation.

Therefore, it will also be beneficial if the ADC chosen can be operated with minimal switching. This is because the handling of multiple switching phases for the sampling and operation of multiple ADCs can be a major work. The design of ADCs with a low number of references is hence of value here.

With the above mentioned issues, it is observed that the ADC most suitable for the highly packed SoC has to be quiet in its operation with minimal references for the ADC core.

1.2 Research Objectives

The objectives of this research are targeted at high fidelity audio applications. To achieve low power dissipation with the possibility for extension to large scale integration, the CT $\Delta\Sigma$ modulator is chosen for a number of benefits.

- The CT $\Delta\Sigma$ modulator samples only at the input to the quantizer. As such, the minimal sampling operation and switching can be appropriately isolated to the backend quantizer, hence keeping cross-coupling under control and achieving good inter channel isolation.
- Since sampling is only performed at the quantizer input post filtering, anti-aliasing is inherently applied to the input signal without a deliberate front-end passive filtering which in general attenuates the microphone output voltage.
- Due to the continuous accumulation of feedback charge, the CT $\Delta\Sigma$ modulator can be optimized for performance at a lower integrator speed requirement. This is because there is no necessity for full settling of the integrator outputs (especially the 1st integrator) unlike the DT $\Delta\Sigma$ modulator. As such, it is perceived that the CT $\Delta\Sigma$ modulator should achieve a better Figure of Merit (FoM).

However, the CT $\Delta\Sigma$ modulator does possess some issues that could hinder the implementation for a high Signal to Noise Ratio (SNR).

- Although the CT integration nature of the integrators helps in power conservation, it also means non-idealities along DT transient instances can also be injected into the filter. Since the sampling of the filter output is noise-shaped, noise injected at that point should be much attenuated for consideration. However, noise entering via the main feedback into the first integrator can directly influence the modulator performance. Such noise source can be from a jittery clock, non-linearity of the feedback DAC, finite output impedance of the sourcing DAC or the finite rise and fall time of the feedback pulses. Fig.1.2 shows the linearized system level block diagram of a $\Delta\Sigma$ modulator.

Fig. 1.2 Illustration showing that feedback errors, $Fb_e(z)$ are not attenuated by the $NTF(z)$

The combined noise injected in the feedback path, L_1 is included in $Fb_e(z)$. As can be observed, the input to the linearized quantizer contains shaped quantization noise, $E(z)[NTF(z) - 1]$ and unshaped signal with the combined feedback noise, $[Fb_e(z) + U(z)] \cdot STF(z)$.

- For linearity reasons, the filter integrators are primarily design with the opamp-RC structure. These CT integrators, as of any other CT integrator structures, are susceptible to process variation tolerance. The impact of such technological imperfections results in the shift in the modulator filter coefficients. These coefficients

define the poles of the loop filter and hence the zeroes of the Noise Transfer Function (NTF). As such, the variation in filter coefficients can degrade the efficiency of the noise shaping modulator.

With the discussed motivations in Section 1.1, the proposed CT $\Delta\Sigma$ modulator for its paramount application-based benefits and the issues that comes along with the architecture of choice, the objectives for this research are listed below.

In the research to meet SoC integration requirements:

- i. To develop CT $\Delta\Sigma$ modulators in advanced technology nodes whereby the supply voltage is minimized to an extreme level of 1V. In spite of the low supply, the modulator should also achieve high SNR values suitable for high fidelity audio applications. For this, the optimum final targeted dynamic range is 96dB and above.
- ii. To develop CT $\Delta\Sigma$ modulators that can be supported with minimal voltage and clock references suitable and desirable for high level integration of today's audio codec chipsets.

In the research to mitigate the issues of CT $\Delta\Sigma$ modulators to achieve high performance:

- iii. To research into the appropriate filter and top level architectural considerations (such as single or multibit internal quantizers) for the development of high resolution CT $\Delta\Sigma$ modulators for audio applications.
- iv. To research and develop ways to mitigate the CT $\Delta\Sigma$ modulator's dependence on RC process corner variations due to technological imperfections

- v. To research into the impact of clock jitter in the choice of CT $\Delta\Sigma$ modulator architectures and therefore to develop techniques to increase the ADC immunity to the clock imperfections.

1.3 Thesis Organization

The main body of the thesis is comprised of 7 chapters, of which:

Chapter 1 gives the introduction, justifying the motivation, listing the objectives and giving the thesis organization.

Chapter 2 reviews past reported circuit design techniques in the area of CT $\Delta\Sigma$ modulators mainly in the architectural sense and further explains the reason for the choice of modulator structure of choice.

Chapter 3 describes the proposed Circuit-based model developed for the verification, analysis and specification derivation for a CT $\Delta\Sigma$ modulator. Specifically, a 4th order modulator is chosen for illustration.

Chapter 4 proposes an improvement to the typically used internal flash quantizer, which, because of its high speed, can be even extended to high speed, high bandwidth applications. Nevertheless, it should be noted that the developed technique can also be useful to low input BW modulators for optimizing the power consumption of multibit quantizers.

Chapter 5 presents the developed modulator of choice with a 4th order single loop, single bit CIFF architecture with mixed integrator structures featuring a condensed gmC

feedforward technique and an adder-less filter transition to the quantizer with Process Corner Calibration together with a Jitter Immunity enhancement circuitry.

Chapter 6 showcases the flagship pseudo 3rd order Audio CT $\Delta\Sigma$ modulator with Enhanced Noise Shaping utilizing a 5 bits SAR-based internal quantizer which also features techniques to mitigate SAR capacitor DAC array mismatch and improved CM mismatch immunity in the Noise Coupling (NC) feedback branch.

Chapter 7 highlights the achievements made in this research, gives the final conclusion and proposes suggestions for future work.

1.4 References

- [1] Chasin M. Hearing aids for musicians. *Hearing Review*. 2006; 13(3):11-16
- [2] Hockley NS, Bahlmann F, Fulton B. analog to digital conversion to accommodate the dynamics of live music in hearing instruments. *Trends Amplif.* 2012;16(3):146-158
- [3] Chasin M. A hearing aid solution for music listening. *Hearing Review*. 2014;21(1):28-30.
- [4] Chasin M. The “best hearing aid” for listening to music: Clinical tricks, major technologies, and software tips. *Hearing Review*. 2014;21(8):26-28.
- [5] Chasin M. Back to Basics: Our Heads are Finally Above Water! Hearing Aid Processing Moves Into a New Era. *Hearing Review*. Jul 2015;22(8):12
- [6] Jon Titus, “Audio ADCs Hit the High Notes”, *ECN Magazine*, 2009
- [7] Khiem Nguyen, “ Input Common-mode Voltage Feedback Circuit for Continuous-time Sigma-Delta Analog-to-Digital Converter,” U.S. Patent US 7009541 B1, Mar. 7th, 2006.

Chapter 2 Literature Review of Circuit Techniques in CT $\Delta\Sigma$ Modulators

Abstract This chapter reviews the design of CT $\Delta\Sigma$ modulators in the literature. The focus was to look into the techniques developed to conserve power yet achieve high performance in especially audio applications. This chapter first looked at classical techniques such as implementation with high order filter structures to recent techniques such as using VCO quantizers or having a hybrid DT and CT filter frontend.

2.1 Introduction

In the design for high resolution CT $\Delta\Sigma$ modulators, there are various important aspects and trade-offs that will affect the performance of the system. In the initial stage of development, the architecture and high level structure has to be scrutinized for power, resolution, stability or even area considerations. Conventional filter structures such as the Cascade of Integrators with Distributed Feedback (CIFB), Cascade of Resonators with Distributed Feedback (CRFB) and Cascade of Integrators with Feed-Forward (CIFF) each has their own merits and disadvantages. This work focuses on the CIFF structure since there is no individual feedback DACs to the respective filter integrators. As a result, the CT filter is only required to process the quantization noise that does not need integrators with large output dynamic ranges manifesting on the system power consumption due to the necessity for high active OTA bandwidths and slew rates. Further architectural

considerations also depend on the kind of feedback schemes employed. Such decisions impact overall sensitivity to modulator pitfalls such as clock jitter and intersymbol Interference (ISI). In addition, the modulator order has to be traded off with power whereby the need for resolution can also be mitigated by having a multibit quantizer on board or an increase in the Over Sampling Ratio (OSR).

This chapter reviews the innovations made to this date for the purpose of achieving the specified performance by resolving certain detrimental issues that could be generic to the CT $\Delta\Sigma$ modulator. Important key breakthroughs will be discussed to understand the underlying reasons and potential issues that can be improved. It is in the interest of the research's focus to search for an efficient yet high performance CT $\Delta\Sigma$ modulator suitable for high fidelity audio applications. The organization of this chapter will be categorized into the research area of focus. Published works specializing in the targeted areas with significant achievements will be discussed. The selected categories presented in this chapter include designs proposing ideas in the filter structure, feedback and quantizer choice. Finally, the research direction is justified based on the records of published works.

2.2 Continuous-Time Filters (CTF)

The push for higher resolution starts out in the optimization of the Noise Transfer Function (NTF). The CTF in the modulator dictates how aggressively the quantization noise will be shaped. It determines the rate of quantization noise descent into the frequency band of interest as observed in the PSD plot as shown in Fig. 2.1. As seen, higher order filters increase the rate of attenuation with frequency. Each order added to

the CTF will result in a 20dB/dec increase in the slope of the NTF function. However so, stability is one of the considerations for this option whenever resolution is required. In addition, the input dynamic range might also be a concern especially with technology advancements. The breakdown voltages of silicon device structures (i.e. MOSFETS) are limited to the system supply voltage, which means the input has to be further attenuated to keep the voltage swing at the quantizer inputs from going into saturation, a condition that will render the modulator unstable.

Fig. 2.1 Integrated Noise with Frequency with 1MHz Sampling Rate

Restricted input dynamic range implies that the Variable Gain Amplifier (VGA) will have to cater for a larger gain configurability.

Nevertheless, there had been development of high order $\Delta\Sigma$ modulators achieving very high SNRs in technology of larger feature size that will be discussed in this section. (2.1) show the relation in the modulator SNR with filter order. For a sinusoidal input, the Signal to Noise Ratio (SNR) can be related to the filter order as follows:

$$SNR \approx \frac{1}{\sqrt{8}} * \frac{\sqrt{6\pi} * \sqrt{(2L+1)!}}{L!} * \left(\frac{OSR}{2\pi}\right)^{\frac{2L+1}{2}} \quad (2.1)$$

There have been studies to achieve the level of noise attenuation with a reduced filter order [5]. These include the usage of biquads that have transfer functions of 2nd order as compared to the typical integrator. However so, the primary purpose of such techniques is to minimize the power of the CTF by reducing the number of active components. The dynamics of the filter and hence the modulator are inherently preserved.

There are alternatives to the usage of opamp RC integrators. Recently, there had been exploration into employing inverter-based integrators for extreme power savings. Such integrators are in general very prone to process variations. In CT integrators, charge integration is typically carried out by converting the input voltage to a charging current. The charging current is expressed as $I_{ch} = (V_{in} - V_{opamp,vir})/R_{in}$ where $V_{opamp,vir}$ is the virtual summing node of an opamp. Due to the large gain of the opamp, the differential inputs to the opamp is very small and is commonly reference to a common mode voltage in fully differential implementation. For regulation, the opamp is arranged in a negative feedback configuration. However, due to the lack of differential inputs in an inverter, negative feedback cannot be easily achieved in CT. However, inverter-based integration can be done in a 2 phase operation as shown in Fig. 2.2, [32]. In the first phase, ϕ_1 , the input and output of the inverter is shorted together. This is the autozero phase whereby the offset of the inverter from its common mode voltage is stored in C_c . In addition, the input signal V_{in} is also sampled onto C_s . During ϕ_2 , C_1 is connected in a negative feedback. As a result, a virtual ground node is formed between C_s and C_c . Subsequently, the charge stored in C_s during ϕ_1 can be transferred to C_1 to complete the integration cycle. Although power

Fig. 2.2 A 2 phase DT inverter-based integrator [32]

is much reduced, these techniques are still isolated to DT applications.

Another filter variation is combining DT with CT integrators to exploit the strengths of both techniques [14]. The CT integrator is mostly utilized in the first stage since sampling is not required. This minimizes the requirement on the bandwidth of the OTA which otherwise has to support the sampling process in DT operations. The DT integrator in the 2nd stage is less susceptible to process variations and can be used to regulate the first integrator integration time in the presence of clock jitter.

2.2.1 High Order Structures

High order filters are considered as the primary method in pushing for high SNR values for large feature sized technology nodes whereby supply voltage is relatively high. In the consumer electronics sector, the highest SNR requirement for oversampling ADC is in the digital audio applications. [1] reported a 5V supply $\Delta\Sigma$ Modulator achieving a SNR of 118dB utilizing a 7th order filter whereas [2] and [3] presented single loop 5th order multibit modulators reaching Dynamic Ranges (DR) of 114dB and 124dB respectively. Fig. 2.3 shows the architecture of the 5th order modulator. In the design of high order filter structures, the cascading filter stages make it hard to reach a high modulation index

without the use of a multibit internal quantizer. In [3], a 5b internal quantizer is utilized. With a supply of 5V, the input voltage swing is reported to be at a magnitude of fully differential $2V_{rms}$. The scaling of each integrator output is summarized in Table 2.1 for the modulators in [2] and [3] respectively. In [3], the number of quantization steps are increased to 33 to improve the modulation index to 0.95. The modulation index is a direct representation of the stability of the modulator. The stability of the modulator in most cases is a reflection of the Maximum Stable Amplitude (MSA) swing at the input to the quantizer. Fig. 2.1 shows the plot of the Noise Transfer Functions (NTFs) from order 2 to 7. It can be observed that the more aggressive the inband quantization noise shaping, the higher will be the high frequency Out of Band (OOB) gain. Fig. 2.4 shows the Oversampling converter in the Loop Filter linearized conceptual block level diagram. If the Signal Transfer Function (STF) gain is assumed to be 1, then the input to the quantizer will be a combination of the shaped noise as given by (2.2).

$$Q_{in}(z) = U(z) * STF(z) + E(z) * [NTF(z) - 1] \quad (2.2)$$

where $E(z)$ is the additive quantization noise in the linearized model.

When the order of the NTF is increased with the same quantizer bits, the inband noise will be shifted outwards. As a result, the input to the quantizer will be presented with a noisier input that is wideband in nature. In other words, the modulation index is decreased. Since the quantizer input cannot exceed the MSA for stability reasons, the input dynamic range will have to be compromised. As a result, the modulation index for higher order modulators in general is lesser than their lower order counterparts. This is also one of the reasons why the outputs of integrators have to be kept low to avoid saturating the quantizer. In [3], there are two feedforward paths. The first feedforward path to the inputs

Fig. 2.3 5th Order Feedforward Modulator in [2] and [3]

Output	Int1	Int2	Int3	Int4	Int5
Max. Swing (V) [2]	0.62	0.78	1.1	1.5	1.45
Max. Swing (V) [3]	0.52	0.65	0.78	0.95	0.89

Table 2.1 Table of Output Voltage swing for the 5th Order Modulator implemented in [2] and [3]

Fig. 2.4 Conceptual Block Level Diagram for a typical $\Delta\Sigma$ Converter

of the quantizer ensures that the filter does not process the signal energy. A second feedforward path is introduced to the input of the last integrator to prevent any signal from leaking back into the filter which may limit the integrator output swing amplitudes. With the increased quantizer bits, the wideband noise level is already reduced. Therefore, the 5th order modulator can achieve a high modulation index while maintaining stability since

the quantizer receives an input that contains lesser noise. However so, the inclusion of the multibit quantizer implies extra care to be taken to ensure the modulator's feedback linearity. Such considerations are often taken care of by inserting a Dynamic Element Matching (DEM) clock in the feedback path.

2.2.2 Design for Power Optimization of CTF

The current consumption of the filter active components takes up a large proportion of the total dissipated power. To optimize power for a high order structure, it would be reasonably fruitful to attempt reducing the power of the CTF. There had been ways to optimize power by applying circuit techniques to relax active component requirements on the performance. The power consumption of high order modulators presented in Section 2.2.1 can be rather high. To minimize this, [4] and [5] presented a methodology to realize filter structures with a reduced number of opamps. This is done by replacing two active integrators with a biquad filter. Fig. 2.5 shows a biquad example that can be used to take the operation of two integrators proposed in [5]. A 4th order CT $\Delta\Sigma$ modulator was designed and the architecture is shown in Fig. 2.6. For a 4th order modulator, there are 3 main active components, namely, the first integrator, the second integrator and an active summing adder circuit to the input of the quantizer. Considering the Single Amplifier Biquad (SAB) of Fig. 2.5, the transfer function taking into account of finite gain, A , is shown in (2.3). The implemented top level circuit level diagram is shown in Fig. 2.6. It can be seen that an active adder is required for this implementation with biquads. Conventional feedforward summation with normal integrators is performed through capacitive coupling into the virtual grounded active summing node of the last integrator.

Fig. 2.5 Proposed Biquad Circuitry in [5]

Fig. 2.6 Top Level Implementation of Modulator with Biquads from [5]

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_1} \left[(C_1 + C_2)s + \left(\frac{1}{R_2} + \frac{1}{R_4} \right) \right]}{C_1 C_2 \left(1 + \frac{1}{A} \right) s^2 + \left\{ \frac{C_1 \left(\frac{1}{R_2} + \frac{1}{R_4} \right) + (C_1 + C_2) \left(\frac{1}{R_1} + \frac{1}{R_3} \right) + \frac{(C_1 + C_2) C_1}{R_3}}{A} + \frac{C_1}{R_4} \right\} s + \left\{ \left(\frac{1}{R_3} + \frac{\left(\frac{1}{R_1} + \frac{1}{R_3} \right)}{A} \right) \left(\frac{1}{R_2} + \frac{1}{R_4} \right) \right\}} \quad (2.3)$$

However, when biquads are utilized, the feedforward coefficients will be affected if feedforward capacitors are added into the last integrator summing nodes due to the added coupling capacitors and resistors needed to realize the required biquad transfer function.

The active adder consumes power with a magnitude equivalent to an active integrator. This decreases the power advantage promised with biquads. Not only this, the active adder acting as the Sample and Hold (S/H) of the quantizer will receive high signal voltage swinging signals in optimization for a high modulation index. This implies under low voltage applications, the switches have to be boot strapped to ensure minimal on-resistances for proper sampling especially under high speed operations. With the inclusion of the Switch Capacitor (SC) adder, the inherently perceived superior speed performance of a typical CT $\Delta\Sigma$ modulator now becomes compromised.

To reduce the power of the CTF, another approach attempts to minimize the power of the first integrator, which is generally the highest power consuming component in a CT $\Delta\Sigma$ modulator due to the requirement for high slew rate and bandwidth. [6], [7] presented a topological improvement that provided charging current assist to the first integrator output to relax the slew requirements while [8] presented a filter systematic improvement by improving the first integrator dynamics through manipulation of filter coefficients. Fig. 2.7 shows the assisted opamp technique that is used in a single stage OTA. The assisted opamp technique is proposed primarily for single bit feedbacks where the current fluctuations can be substantially large. There are essentially two limitations in the OTA performance required to handle abrupt current changes.

The OTA bandwidth helps to manage the sudden change in current magnitudes while its slew rate performance manages the feedback current magnitude that translates to integration speed. Fig. 2.8a shows the comparison between the transient responses at the output of the active opamp RC integrator having two different OTA bandwidths. It can be observed that there is a time lag in the final integration output. When the feedback pulse

Fig. 2.7 Single Stage Integrator with opamp assisting gm and DAC

Fig. 2.8a Integration Output Transient Waveforms between an Ideal and BW-limited Integrator (Left)

Fig. 2.8b Integration Output Transient Waveforms between an Ideal and SR-limited Integrator (Right)

ends, the integration stops, resulting in a gain error due to the time skew. Fig. 2.9b shows the comparison between two integrator outputs having a different output slew rates. It is observed that the slope of the integrator having insufficient slew rate integrates at a different rate, which also ended up with an erroneous final output voltage. In the single bit feedback architecture, the full range upward and downward integration occurs from cycle to cycle. As such, an insufficient bandwidth and slew rate can result in a slow reaction at the output of the integrator. These performance limitations manifest themselves to

fluctuations at the virtual ground to the summing inputs of the active OTA forming the integrator, hence resulting in the formation of distortions.

To relax this speed requirement, it can be seen in Fig 2.7 that an assistant gm cell and DAC is used to provide the current otherwise required by the OTA to sink or source during discharging and charging respectively. The added gm cell and DAC will contribute to the noise and distortion of the first amplifier. The slew rate of the OTA can be greatly relaxed. However, it should be noted that the distortions contributed by the assistant gm cell and DAC has to be mitigated by having a large bandwidth OTA. Intuitively, if the OTA response in the initial phase is slow, the integrating current shortfall that originally comes from the integrator through the integrating capacitor will be injected by the much faster gm cell. This can result in distortions if the assistant gm cell or DAC are linearity-relaxed. Therefore, this limits the actual power savings on the first OTA if distortion is of priority to the design specifications.

Another approach to reduce the power consumption of the 1st integrator is proposed in [8]. In this methodology, the solution to the problem is to model the GBW-induced error as delays in the feedback loops. Depending on the type of feedback pulse, the appropriate tuning to the coefficients or addition of direct feedback path is included to mitigate the errors. In the reported work, only the Return-to-Zero (RZ) and the Non-Return-to-Zero (NRZ) feedback pulses are studied. Fig. 2.9 shows the top level model for GBW-induced error as feedback delays, τ_{D1} and τ_{D2} for the main and auxiliary feedback paths respectively. It should be noted that similar to the compensation of quantizer and DAC Excess Loop Delay (ELD), an introduction of delay in a RZ pulse that is within $0.5T_s$ can

be simply compensated by a tuning of the scaling coefficients. In [8], for a 2nd order modulator, the DT Loop Transfer Function (LTF) is expressed in (2.4).

$$LTF_{DT,MOD2} = -a_1 a_2 H(z)^2 - a_2 H(z) = -\frac{a_1 a_2}{(z-1)^2} - \frac{a_2}{z-1} \quad (2.4)$$

Performing the Time-Invariant Impulse Transformation,

$$LTF_{DT-CT,MOD2} = \frac{\frac{1}{2}a_1 a_2 (\alpha + \beta - 2)s + a_1 a_2}{(\beta - \alpha)s^2} - \frac{a_2}{(\beta - \alpha)s} \quad (2.5)$$

where the coefficients of (2.5) are compared to the coefficients of the CT modulator LTF as expressed in (2.6).

$$LTF_{CT,MOD2} = -\frac{k_1 k_v f_s^2}{s^2} - \frac{k_2 f_s}{s} \quad (2.6)$$

Upon comparing the coefficients, the CT modulator scaling coefficients worked out to be:

$$k_s = a_1 a_2 \quad k_v = 1 \quad k_1 = \frac{a_1 a_2}{2(\beta - \alpha)}$$

$$k_2 = \frac{a_2(2 + a_1 \alpha + a_1 \beta - 2a_1)}{2(\beta - \alpha)} \quad (2.7)$$

Fig. 2.9 GBW Induced Error Model in a 2nd Order CT $\Delta\Sigma$ modulator

For the compensation of GBW-induced errors for RZ pulses that causes a delay shifts of smaller than $(1 - \beta)T_s$, then, the coefficients from (2.7) can be tuned for compensation.

However, for NRZ feedback pulses where each pulse span $1T_s$, then a direct High-Return-to-Zero (HRZ) feedback pulse is proposed as shown in Fig. 2.10. Each feedback paths are then individually considered for in the CT domain and transformed into their corresponding DT form using the Impulse Invariant Transformation. Subsequently, the overall transformed LTF in DT is obtained and compared with the ideal 2nd order modulator LTF, yielding the results shown below in (2.8).

$$k_s = k_1 = \frac{1}{4} \quad k_v = 1 \quad k_2 = \frac{6\tau_{D1} + 4\tau_{D1}\tau_{D2} - \tau_{D2}^2}{8\tau_{D1}} \quad k_h = \frac{3\tau_{D1} + 2\tau_{D1}\tau_{D2} - \tau_{D2}^2}{4\tau_{D1}} \quad (2.8)$$

This compensation technique models the GBW-induced errors as delays in the feedback paths and subsequently introduced systematic coefficient shifts or direct feedback compensating paths to nullify the induced errors. In other words, this compensation method shifts a design parameter realization that is process dependent into a shift in coefficients that is also process dependent. As such, for this technique to work well there

Fig. 2.10 Compensation of BW-Induced Errors with a Direct High-Return-to-Zero (HRZ) Feedback Pulse

has to be substantial post silicon calibration to nail the exact coefficients for the optimum expected performance. Since the process variation especially in advance technology nodes might be more than 30%, there could be a possibility that the modulator might require a long and tedious trimming procedure which is not desired in actual industrial applications. In addition, it should be noted that the insertion of a HRZ direct feedback can introduce abrupt current transient that require a faster response from the second integrator. This implies a higher slew rate requirement which leads to a higher power consumption in the second OTA.

2.2.3 Hybrid Structure – DT and CT combination

The combination of both the DT and CT based architecture can be capitalized for both their advantages [14]. Due to the Sample and Hold (S/H) nature of the DT second integrator, a dedicated S/H is not required prior to the quantizer, which saves on power and reduces the complexity of the architecture. The usage of a CT frontend yields three important advantages.

Firstly, the signal dependent clock feedthrough generic to DT sampler is not present at the modulator frontend, which naturally is not noise-shaped. Coupled noise to the modulator frontend will also not be sampled since it is only performed at the quantizer. Secondly, due to CT integration of the first integrator, any glitches will be averaged out by the accumulation process. Thirdly, the resistive input of the first CT integrator minimizes on the EMI emission that typically couples to the input pins of a DT modulator. Fig. 2.11 shows the hybrid architectural diagram. Having a DT second stage with RZ feedback,

means only the main feedback has to be designed for better jitter immunity by fixing the integration period. This is because the main sampling at the quantizer is inherently jitter sensitivity enhanced since a well-designed RC time constant will ensure proper voltage settling within the clock period before the next sampling instance. Moreover, any non-idealities injected at this point will be noise shaped by the modulator's NTF.

The process variation consideration is only required for the 1st integrator. Due to the gain of prior stages, standard matching of capacitors for the second stage onwards is sufficient if proper layout considerations were taken. However, it should be noted that employing hybrid structures means compromising on the pre-existing benefits of CT $\Delta\Sigma$ modulators. The original sampling at the input to the quantizer is now up shifted to the input of the second stage in this case. As such, any kickback noise will only see one level of attenuation by the 1st integrator when input referred. This could potentially cause distortion if not managed well. In addition, the second SC stage has to be designed to have a high bandwidth to ensure SC charge transfers to be properly settled during operation. The input sampling capacitors for the second stage also loads the output to the 1st

Fig. 2.11 2nd Order Hybrid CT/DT Modulator Architecture

integrator, which may require a larger power to drive while increasing the difficulty to compensate the 1st active OTA.

2.3 Internal Quantizer

The variation in the type of quantizer used is usually an attempt for the optimization of the multibit feedback protocol. This is because the typical usage of a flash converter is not only high power consuming but also occupies a silicon area that increases exponentially with bit length.

2.3.1 Successive Approximation (SA) Quantizer

In place of the flash architecture, [9-12] proposes the use of a Successive Approximation (SA) converter. The SA quantizer architecture only requires one comparator. Fig. 2.12 shows the conceptual block level diagram of a SA converter. The input is sampled and undergoes comparison. The digital output is fed into a Successive Approximation Register (SAR) that feeds back via a DAC a radix 2 analog output that again compares with the input. The SAR generates a digital output that slowly approaches the input by switching in a converging binary sequence. In this manner, the SA converter trades area and speed with time. In other words, the SA converter utilizes a time period that is a multiple of the quantizer resolution. As such, if it is decided to use the SA converter within a CT $\Delta\Sigma$ modulator, the delay introduced by the bit cycling process has to be compensated as Excess Loop Delays (ELDs). In [11], a capacitive charge redistribution SAR is used with a proposed embedded ELD capacitive DAC shown in Fig. 2.13. Although convenient, the

additional capacitive array requires extra switching instances which will be generating charge feedthrough that can affect the precision of the quantizer. In addition, the delay compensating sampling capacitors are to be exactly matching the main DAC.

Fig. 2.12 SAR Conceptual Block Diagram

As such, the fully differential implementation will require 4 sets of capacitive arrays that can be rather area consuming, which defeats the purpose of implementing with SA architecture in the first place. Not only this, the extra set of DAC capacitors can load the prior driving integrator, hence necessitating a large bandwidth requirement on the active OTA which can only be achieved by increasing the power consumption. It can arguably be proposed that the unit capacitors can be of small size but this approach might compromise on the matching between the capacitors which can be detrimental in this implementation.

2.3.2 Time Based Quantizer

Time based quantizers can be categorized in VCO-based or time-encoding converters. Fig. 2.14 shows a typical VCO-based quantizer [13]. The input to the quantizer comes from

the CTF last integrator output, which is used to modulate the output frequency of the VCO. To know the input voltage, it is necessary to recognize that it is proportional to the

Fig. 2.13 SAR-Based Quantizer with ELD Compensation as proposed in [11]

frequency of the VCO. Therefore, the difference between the samples gives the rate of change of edge propagation (i.e. phase accumulated) along the inverter chain forming the ring oscillator. This means the output frequency is proportional to the input voltage scaled with a gain K_v . The difference can be simply implemented with a XOR gate whose inputs are the time consecutive inverter stages outputs of the ring oscillator chain. It is also reported that due to the mismatches between the inverter delays, the gain K_v is susceptible to linearity issues. This non-uniformity in gain with input can result in distortion and hence the generation of tonal spurs in the modulator output FFT spectrum. To curb this issue, a feedback loop is proposed as shown in Fig. 2.15. Instead of frequency, the phase is now the variable that is operated within the loop. The input voltage from the CTF output is passed to the VCO whereby the voltage parameter is converted into frequency.

To obtain the phase, the outputs from the delay stages are compared with a reference frequency. This reference frequency measures the phase accumulated along the delay line

Fig. 2.14 Typical VCO-based Quantizer Using Frequency Parameter reported in [13]

Fig. 2.15 Improved VCO-based Quantizer Using Phase Parameter reported in [13]

within a reference period of time. As such, the feedback loop operates as a first order $\Delta\Sigma$ Modulator. The VCO accumulates the phase component, which is later being fed back through a DAC that converts the digitized phase into an analog voltage that will be subtracted from the input. Due to the VCO phase accumulator, the gain at DC is very large. This causes the difference error signal between the input and feedback to become extremely small. This is the reason for the enhanced linearity. The delay stages of the

VCO are essentially implemented with inverters chain. These inverter chains consume relatively large current that has to be supplied from the input reference driver. In this case, the input reference is coming from the CTF output. The abrupt switching spikes necessitate high speed buffers that are able to cope with a sudden demand in current.

Because of this requirement, it could be an issue driving the VCO with the last integrator. Therefore, a dedicated buffer might be necessary to provide the drivability, hence increasing the current consumption dramatically.

The buffer also acts as a shield for the frontend filter from the kickback voltage spikes that typically result from a bandwidth limited VCO driver output. Due to this, the VCO-based quantizer is mostly utilized in modulators that do not have high SNR requirements where the objective could alternatively be to attain high speed.

2.4 Feedback

The most common feedback protocols are of the Non-Return-to-Zero (NRZ) and Return-to-Zero (RZ) feedback pulses. The difference between the two types of feedback pulse shapes are summarized in Chapter 5 as one of the design consideration for the development of the 4th order CT $\Delta\Sigma$ modulator. Implementation deviations from these two conventional feedback pulses can originate from different objectives. Jitter performance is one of the considerations. The source of jitter for a CT $\Delta\Sigma$ modulator is injected along the feedback pulse. In particular, the feedback DAC is the largest contributor to the degradation due to jitter. The source of this jitter stems primarily from the jittery clock that is supposedly responsible for synchronizing the feedback. Fig. 2.16 shows the Full Period SCR with the NRZ and RZ feedback pulse shapes [14-16]. By utilizing a pulse with diminishing amplitude, the feedback can be made much less sensitive to the synchronizing clock fluctuations. This is illustrated with a simplified Full Period Switched

Capacitor Resistive (SCR) feedback. Although the initiating pulse edge might have shifted due to clock uncertainties, the total amount of charge integrated as determined

Fig. 2.16 Overlay of SCR, NRZ and RZ Feedback Pulse Shapes

by the area under the feedback pulse remains relatively constant. This is because of the comparatively lesser erroneous accumulated charge towards the end of the pulse, thanks to the exponentially decaying amplitude. Intuitively, the total charge under a feedback pulse remains constant as the charge feedback per unit time is now much skewed towards the starting pulse edge. Since the total charge is constant, it can be deduced that the pulse amplitude will be larger than a typical NRZ pulse in the beginning before tapering down rapidly. As a result of this, the integrating process required from the receiving first integrator has to respond to a high initial charging/discharging phase before relaxing towards the end of the feedback cycle. To ensure the integrity of this dynamic process, it is essential for the core OTA supporting the integration function to be able to handle a high slewing process despite the relaxation phase towards the end. Consequentially, a generic less efficient Class A amplifier will mean a large output DC bias that translates to higher power consumption. Alternatively, to optimize power, a Class AB is usually required, which increases the complexity for compensation especially with a heavy

integrating capacitor loading at the output. Besides clock jitter, [17-20] reported works implementing a FIR feedback. Such a feedback attempts to achieve the merits of a multibit feedback while conserving the inherent linearity of the single bit DAC. In particular, [14] used this concept to achieve high resolution for a CT $\Sigma\Delta$ modulator in the targeted audio signal bandwidth. Fig. 2.17 shows the block level diagram of the implemented structure. The objective for the inclusion of a FIR filter ideally lowers the high frequency component of the feedback and therefore results in only the feedback of the in-band signal and quantization noise. When the difference between the inputs is taken with the FIR output, only the quantization noise will be computed by the CTF which provides high gain to minimize the noise level. However, in the implementation of a causal FIR filter, the output presents some delay and therefore has to be compensated via an auxiliary feedback FIR filter as proposed in [19]. The real implementation of the FIR filter can be done in the voltage or current domain. In the voltage domain, it includes the generation of coefficient-weighted reference voltages that are resistively connected to the summing inputs of the integrator. On the other hand, a current mode implementation is done with multiple different current branches weighted by the FIR filter coefficients.

This could potentially be complex due to the non-integer scaled feedback currents that cannot be trivially realized with simple current mirrors. The voltage domain is utilized in [14] and therefore required multiple different reference voltages scaled according to the FIR filter coefficients. Moreover, each of the reference voltages has to be well buffered for drivability. This requirement can be demanding for a typical audio System on Chip (SoC).

Fig. 2.17 Block Level Diagram of a Modulator with FIR DAC Feedback

2.5 Review of High Resolution CT $\Sigma\Delta$ Modulators for Audio Applications

Table 2.2 tabulates recent high performance audio $\Delta\Sigma$ modulators that were reported. It can be observed that most of the works reported are of 2nd order with only a few reported using 3rd order structures. This trend is most likely a result of the lowering of supply voltages with technology advancements that had caused a decrease in the maximum modulation index achievable. However, it can be seen that the lowest $FoM_{schreier}$ reported in [23] is implemented in a 3rd order structure however with a multibit design. Multibit designs are prone to feedback linearity issues and as a result, a DEM becomes mandatory. Therefore, it is interesting to explore into increasing the modulator order to a 4th order structure while reducing the internal quantizer to a 1b comparator. Increasing the order by one improves the noise shaping effect. Keeping the quantizer as a single bit comparator maintains its inherent linearity but at the expense of the sacrifice in MSA due an elevation of high frequency noise. As a tradeoff, CIFF architecture is utilized to keep internal integrators node swing to be minimal with only quantization noise to process. This is one of the designs that have been explored in Chapter 5 where mixed integrator structures are employed. Other architectures researched into noise shaping enhanced structures whereby

Reference	BW (kHz)	DR (dB)	SNR (dB)	SNDR (dB)	Power (μ W)	Tech (nm)	VDD (V)	Area (mm ²)	Order	Quant Lvls	CT/DT	FoM ₁ (dB)	FoM ₂ (fJ/conv)
[21] P. Morrow, et.al	20	102	-	95	37000	180	3.3	0.65	2	16	CT/DT	159	20122
[22] K. Nguyen, et.al	20	106	106	97	18000	330	3.3	0.82	2	17	CT/DT	166	7776
[23] S. Pavan, et.al	24	92.5	91	88	110	180	1.8	0.24	3	2	CT	176	112
[24] M.Y. Choi, et.al	20	101	101	85	15000	65	3.3	0.28	3	3	CT/DT	162	25800
[20] A. Sukumaran, et.al	24	103	99	98.2	280	180	1.8	1.25	3	2	CT	182	88
[25] Dorrer. L, et.al	20	91.7	79	76.5	1200	45	1.1	0.0895	2	15	CT	164	5492
[26] Dorrer. L, et.al	20	95	77	74	2200	65	1.2	0.149	2	15	CT	165	13428
[27] S. Pavan, et.al	24	93.5	93	92.5	90	180	1.8	0.72	3	16	CT	178	54
[28] Y. G. Kim, et.al	20	106	106	97.5	9900	130	3.3	0.49	2	17	CT	169	4037
[29] Hyunsik. P, et.al	25	100	100	95	870	180	0.7	2.16	2	18	DT	175	379
[30] Tao Wang, et.al	20	101	100	99.3	1100	180	5	0.3784	2.5	15	DT	174	365
[31] L. Liu, et.al	24	96.4	96	95	371	65	1	0.41	2	32	DT	175	168

Table 2.2 Tabulated Recent Works of High Resolution Oversampled Modulators for Audio Applications

the NTF order is increased with circuit design techniques as reported in [31]. This work accentuates noise shaping by harnessing the quantization noise energies and subsequently feeding them back into the filter in DT domain. As of today, it is still perceived that such structures are only suitable for DT implementation. This is because of the sampling required at the quantizer input and the time necessary for the local quantization noise feedback loop that renders it extremely challenging for a CT domain. Because of this sampling required, in order to maximize the Maximum Stable Amplitude (MSA) at the filter output, bootstrapping of the switches cannot be avoided.

In order to make it possible in the CT domain, it is necessary to identify suitable circuit techniques for achieving both an inherent acquisition of quantization noise and a quiet

feedback into the filter that would otherwise result in the generation of detrimental kickback noise. It will therefore be interesting to research into the possibility of realizing an enhanced noise shaping filter with noise coupling in the CT domain. This has therefore been identified as one of the research scope in this work and a prototype has been realized and fabricated which will be extensively discussed in Chapter 6. The modulator achieved enhanced noise shaping while preserving all the benefits of using a typical CT modulator. Distortions from kickback noise are well controlled as observed in the PSD without any severe elevation in harmonic tones.

The table also reveals that the supply VDD of state of the art high resolution audio band ADC are still >90% above 1V. When higher order (i.e. >5) filters are used, the aggressive noise shaped quantization noise results in a reduced MSA due to instability, hence leading to a lower input voltage swing. With low supply VDD, it becomes even more challenging to reach high resolution with minimal voltage headroom. As a result, to increase the MSA, there had been a paradigm shift towards multibit designs. As explain in Section 2.3, it is desirable to have multibit feedback characteristics even when a single bit quantizer is used. Therefore, the work in Chapter 6 also attempts to develop a CT $\Sigma\Delta$ modulator under a low supply of 1V. The MSA for this work is enhanced with a high resolution (5bit) internal quantizer. Together with the Noise Transfer Function (NTF) enhancement, the overall quantization noise is reduced to a minimum to maximize the input dynamic range.

As such, the work in Chapter 6 also achieved a fully differential rail to rail of 2V input voltage peak to peak amplitude (i.e. comparable to 5V designs) which would greatly relax the driving VGA requirements typically located prior to the ADC in a high fidelity audio signal acquisition system.

2.6 References

- [1] Ka Y. Leung, et.al “A 5V, 118dB $\Delta\Sigma$ Analog-to-Digital Converter for Wideband Digital Audio,” *ISSCC Dig. Tech. Papers*, pp. 218-219, 1997
- [2] Yuqing Yang, et. al, “A 114-dB 68-mW Chopper-Stabilized Stereo Multibit Audio ADC in 5.62 mm²,” *Solid-State Circuits, IEEE Journal of*, vol.38, Issue 12, pp. 2061-2068, 2003.
- [3] Yuqing Yang, et. al, “A Single-Die 124 dB Stereo Audio Delta-Sigma ADC With 111 dB THD,” *Solid-State Circuits, IEEE Journal of*, vol.43, Issue 7, pp. 1657-1665, 2008.
- [4] Zanbaghi, R., et. al, “An 80-dB DR, 7.2-MHz Bandwidth Single Opamp Biquad Based CT $\Delta\Sigma$ Modulator Dissipating 13.7-mW,” *Solid-State Circuits, IEEE Journal of*, vol.48, Issue 2, pp. 487-501, 2013.
- [5] Kanemoto, D., et. al “A 7.5mW 101dB SNR Low-Power High-Performance Audio Delta-Sigma Modulator Utilizing Opamp Sharing Technique,” *SoC Design Conference (ISOCC), International*, pp. 66-69, 2011.
- [6] Pavan, S., et. al, “Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique,” *Solid-State Circuits, IEEE Journal of*, vol.45, Issue 7, pp. 1365-1379, 2010.
- [7] Pavan, S., et. al, “Analysis and Design of a High Speed Continuous-time $\Delta\Sigma$ Modulator Using the Assisted Opamp Technique,” *Solid-State Circuits, IEEE Journal of*, vol.47, Issue 7, pp. 1615-1625, 2012.

- [8] Ortmanns, M., et. al, "Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time Sigma-Delta Modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.51, Issue 6, pp. 1088-1099, 2004.
- [9] L. Samid, et. al, "A new kind of low power multibit third order CT $\Delta\Sigma$ Modulator", *IEEE Int. Symp. On Circuits and Systems*, vol. 3, pp. 293-296, 2002.
- [10] L. Samid, M. Abu-Ghazi, and Y. Manoli, "A Novel Continuous-Time $\Delta\Sigma$ Modulator with a Successive Approximation Multibit Quantizer", *Proc. IEEE Int. Symp. Circuits*, pp. 59-63, 2003.
- [11] Ranjbar, M., et. al, "A 3.1 mW Continuous-Time $\Delta\Sigma$ Modulator With 5-bit Successive Approximation Quantizer for WCDMA," *Solid-State Circuits, IEEE Journal of*, vol.45, Issue 8, pp. 1479-1491, 2010.
- [12] Liu, L., et. al, "A 95dB SNDR Audio $\Delta\Sigma$ Modulator in 65nm CMOS," *Custom Integrated Circuits Conference (CICC), IEEE*, pp. 1-4, 2011.
- [13] A 16-mW 78-dB SNDR 10-MHz BW CT $\Delta\Sigma$ ADC Using Residue-Cancelling VCO-Based Quantizer
- [14] Ortmanns, M., et. al, "A Continuous-Time $\Sigma\Delta$ Modulator With Reduced Sensitivity to Clock Jitter Through SCR Feedback," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.52, Issue 5, pp. 875-884, 2005.
- [15] Anderson, M., et. al, "Design and Measurement of a CT $\Delta\Sigma$ ADC With Switched-Capacitor Switched-Resistor Feedback," *Solid-State Circuits, IEEE Journal of*, vol.44, Issue 2, pp. 473-483, 2009.
- [16] Jun-Gi Jo, et. al, "A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC

- and High-Speed DWA,” *Solid-State Circuits, IEEE Journal of*, vol.46, Issue 11, pp. 2469-2477, 2011.
- [17] Oliaei, O., “Sigma-Delta Modulator With Spectrally Shaped Feedback,” *Circuits and Systems II: Analog and Digital Signal Processing, IEEE, Transactions on*, vol.50, Issue 9, pp. 518-530, 2003.
- [18] Putter, B.M., et. al, “ $\Sigma\Delta$ ADC with Finite Impulse Response Feedback DAC,” *Solid-State Circuits Conference, Digest of Technical Papers (ISSCC), IEEE International*, vol.1, pp. 76-77, 2004.
- [19] Shettigar, P., et. al, “Design Techniques for Wideband Single-Bit Continuous-Time $\Delta\Sigma$ Modulators With FIR Feedback DACs,” *Solid-State Circuits, IEEE Journal of*, vol.47, Issue 12, pp. 2865-2879, 2012.
- [20] Sukumaran, A., et. al, “Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback,” *Solid-State Circuits, IEEE Journal of*, vol.49, Issue 11, pp. 2515-2525, 2014.
- [21] P. Morrow *et al.*, “A 0.18 μ m 102 dB SNR mixed CT-SC audio-band Delta-Sigma ADC,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2005, pp. 178–592.
- [22] K. Nguyen, B. Adams, K. Sweetland, H. Chen, and K. McLaughlin, “A 106 dB SNR hybrid oversampling ADC for digital audio,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2005, vol. 1, pp. 176–591.
- [23] S. Pavan and P. Sankar, “A 110 W single bit audio continuous-time oversampled converter with 92.5 dB dynamic range,” in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2009, pp. 320–323.

- [24] M.-Y. Choi *et al.*, “A 101-dB SNR hybrid delta-sigma audio ADC using post integration time control,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2008, pp. 89–92.
- [25] Dorrer, L., et.al. “A Continuous Time $\Delta\Sigma$ ADC for Voice Coding with 92dB DR in 45nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2008, pp. 502-631.
- [26] Dorrer, L., et.al. “A 2.2mW, Continuous-Time Sigma-Delta ADC for Voice Coding with 95dB Dynamic Range in a 65nm CMOS Process,” in *Solid-State Circuits Conference (ESSCIRC), Proceedings of the 32nd European*, pp. 195-198, 2006.
- [27] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, “A power optimized continuous-time delta-sigma ADC for audio applications,” *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 351–360, Feb. 2008.
- [28] Y.-G. Kim, M.-H. Cho, K.-D. Kim, J.-K. Kwon, and J. Kim, “A 105.5 dB, 0.49 mm audio delta-sigma modulator using chopper stabilization and fully randomized DWA,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2008, pp. 503–506.
- [29] H. Park, K. Nam, D. Su, K. Vleugels, and B. Wooley, “A 0.7 V, 870 W digital-audio CMOS sigma-delta modulator,” *IEEE J. Solid-State Circuits*, vol. 44, pp. 1078–1088, 2009.
- [30] T.Wang, W. Li, H. Yoshizawa,M. Aslan, and G. C. Temes, “A101 dB DR, 1.1 mW audio delta-sigma modulator with direct-charge-transfer adder and noise

shaping enhancement,” in *Proc. IEEE Asian Solid- State Circuits Conf. (ASSCC)*, 2012, pp. 249–252.

- [31] L. Liu, D. Li, Y. Ye, L. Chen, and Z. Wang, “A 95 dB SNDR audio delta-sigma modulator in 65 nm CMOS,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2011, pp. 1–4.
- [32] Youngcheol Chae and Gunhee Han, “Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator”, *IEEE Journal of Solid-State Circuits*, vol. 44, No.2 February 2009.

Chapter 3 **Modelling of Non-Idealities and Trade-offs in the Design of CT $\Delta\Sigma$ Modulators**

Abstract This chapter discusses the high level modelling of CT $\Delta\Sigma$ modulators with the final objective to obtain the block level specifications of the constituting components. The primary tool used is MATLAB SIMULINK where the modelling techniques of various important non-idealities were demonstrated with a 4th order CT $\Delta\Sigma$ modulator. Subsequently, performance sensitivity studies were made between CIFF modulators of different filter orders using quantizers of various resolutions.

3.1 Introduction

In the evaluation of CT $\Delta\Sigma$ modulators, the generation of highly accurate results requires long simulation time due to the nonlinear nature of the system. In most cases, a compromise has to be made to trade off precision for speed [2]. This chapter presents a circuit-based high level model implemented in the MATLAB SIMULINK environment so as to achieve a faster speed of simulation. Designed in a differential manner, the model provides good visualization of the actual circuit at the early stage of design. To maintain simulation accuracy, circuit non-idealities such as system clock jitter, integrator noise, opamp finite gain and bandwidth as well as slew rate are included in the model. For demonstration purpose, a 4th-order CT $\Delta\Sigma$ modulator with NRZ feedback and CIFF architecture is implemented. With the proposed models, key design specifications for the

functional building blocks are derived. In recent years, the CT $\Delta\Sigma$ modulator has been gaining popularity, attributed mainly to characteristics such as its inherent anti-aliasing property and the possibility of achieving lower power consumption as a result of less stringent requirements on the speed of the CT integrators [1]. Due to the non-linear nature of the sampling process at the internal quantizer, the analysis of CT $\Delta\Sigma$ modulators is a tedious process. This often translates to lengthy time domain simulations especially when evaluating high performance CT $\Delta\Sigma$ modulators. It is therefore necessary to have a high level model that can be used to determine the performance of the modulator under the influence of circuit level non-idealities. With the aim to improve the speed of simulations, the accuracy of simulations is often sacrificed.

This work proposes a high level circuit-based fully differential model for the CT $\Delta\Sigma$ modulator implemented entirely in the MATLAB SIMULINK environment. In preserving the accuracy of the simulations, detailed modeling of circuit level non-idealities is included. The model allows comprehensive time domain analysis of the modulator nonlinear system at a much faster rate compared to SPICE simulations. The chapter is organized as follows. Section 3.2 describes the modeling concepts for the individual blocks with non-idealities. In section 3.3, the implementation of the 4th-order CT $\Delta\Sigma$ modulator is discussed. Section 3.4 discusses the simulations obtained before concluding the modelling work. In addition, Section 3.5 also discusses some trade-offs in the choice of modulator architecture for power versus performance optimization. To simplify the large configuration matrix, this work focuses on the CIFF filter structure, which is known for its power efficiency. Comparisons are then made to evaluate the modulator with

various combinations of structure order with quantizer bit lengths with respect to the design requirements to achieve the required performance.

3.2 Modelling Concepts

3.2.1 MATLAB Physical Domain Modeling

In MATLAB SIMULINK, it is possible to include physical components such as resistors and capacitors for simulations. These components reside in the physical domain. For implementation purpose, the basic resistors and capacitors required in the proposed model are taken from the SIMULINK SimPowerSystems toolbox [3]. An interface has to be inserted between the normal SIMULINK data signal domain and the physical domain. These interfaces are required when signals propagate to and from the two domains. This is similar to mixed signal simulation in well-known design tools such as Cadence or Synopsys. In these design tools, interfacing A/D or D/A elements are placed to allow the simulator to recognize the transition into the respective digital or analog domains. In SIMULINK, a controlled voltage source is required when moving from the signal to the physical domain. Conversely, transiting in the reverse direction from the physical domain back to the signal domain needs a voltage measurement block. Fig. 3.1 illustrates the propagation of signals between the two domains.

3.2.2 CT $\Delta\Sigma$ Modulator Non-idealities

A typical single loop single bit CT $\Delta\Sigma$ modulator may consist of a CT opamp-RC integrator as the first stage, transconductor (gmC) cells as the subsequent stages, a

quantizer and a single bit feedback Digital-to-Analog converter (DAC). This section focuses on the modeling of nonidealities of the functional blocks within the CT $\Delta\Sigma$ modulator. The main non-idealities that are considered include the following:

1. System Clock Jitter;
2. Thermal and Flicker noise of first integrator;
3. Finite gain and bandwidth of first opamp;
4. Slew rate of first opamp;
5. Linearity and distortion of first opamp;
6. Saturation voltage of first opamp.

Fig. 3.1 Transition of data between the signal and physical domains

3.2.3 System Clock Jitter

Clock jitter has always been the fundamental performance limitation for CT $\Delta\Sigma$ modulators. The continuous integration of the feedback implies that any jittery clock edges will result in the accumulation of errors as a result in the fluctuation of the clock edges. Variations from ideal clock edges vary the feedback pulse length and hence the total effective feedback charge. This behavior increases the noise floor across the frequency band. This phenomenon is especially critical when occurring at the feedback DAC. It is because this noise cannot be shaped by the system when injected at that point.

Independent clock jitter approximation is the most widely used model for performance prediction in high level simulations. In this approach, clock jitter is modeled as an additive timing error on the ideal clock edges. A SIMULINK model has been proposed by [4]. Alternatively, phase noise modulation can be applied to an ideal clock. However, such approaches produce time domain simulations that are extremely time consuming due to small timing variations. A more efficient method would be to transform pulse width variance to pulse amplitude variation. In [5], the author proposed a jitter model specifically for NRZ feedback pulse. A jitter model for the NRZ feedback pulse is shown in Fig. 3.2. It is to be mentioned that the amplitude modulation only ensure first order accuracy since pulse position jitter is not considered. However, since pulse position variation is at least first order noise shaped, its effect is relatively insignificant. Specifically speaking, for feed forward structures, only one feedback path is used, thus this model is particularly suitable for CIFF implementation.

Fig. 3.2 Jitter Model for Non Return-to-Zero (NRZ) Implementation

In CIFF architecture, the injection of jitter occurs at two locations. Basically, they are the two components that require a clock to function, namely the quantizer and the feedback DAC. At the quantizer, the discrepancy in the clock edges results in the sampling of the integrated carried forward signal. However, at the quantizer, the slow frequency error

captured is digitized and compared with the input whereby a corrective response will be generated by the loop dynamics. In other words, the jitter injected at the quantizer will be noise-shaped by the loop filter. This is as opposed to the feedback at the main DAC. Assuming the quantizer is ideal, the jittery feedback DAC results in the production of an erroneous differential feedback charge that will be directly carried forward to the output. The injection of error at the main feedback DAC therefore does not enjoy any attenuation since the modulator treats this error as coming from the input signal. Fig 3.4 shows the treatment of the noise injected from the two positions.

3.2.4 Thermal and Operational Amplifier Noise

The dominant noise source in an active opamp RC integrator comprised of the white noise contributed by both the input and feedback resistors in addition to the input referred amplifier noise which consists of input flicker (1/f) noise, wide band thermal noise and amplifier dc offsets. These values are obtained through SPICE simulation. Subsequently, each individual input referred noise power spectral density attributed to all the noisy devices are summed together before being integrated across the signal bandwidth of concern.

According to [1], the total input-referred noise power is given by (3.1):

$$V_{noise}^2 = 16K T f_B (R_{in} + R_{fb}) + \frac{128K T f_B n_{e,th}}{3g_{m,OTA}} + \frac{8K_f n_{e,th}}{C_{ox}^2 W L} \ln\left(\frac{f_B}{f_u}\right) \quad (3.1)$$

The total RMS noise voltage, V_{noise} is superimposed to the input signal leading to equation (3.2):

$$V_{out}(t) = V_{in}(t) + V_{noise} \cdot n(t) \quad (3.2)$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation. (3.2) can be implemented by the SIMULINK model shown in Fig. 3.4.

3.2.5 Operational Amplifier and Nonidealities

The integrator circuit implementation deviates from the ideal behavior due to several non-ideal effects such as the finite op-amp gain and bandwidth, slew rate and output saturation voltage. To make it as realistic as possible, an amplifier with a two pole and one zero transfer function has been adopted. The non-dominant amplifier second pole and amplifier zero are chosen such that the result is a practical amplifier with a phase margin of approximately 60° . Modelling of such a real integrator with all the non-idealities is shown in Fig. 3.3. The finite gain bandwidth product (GBW) of the opamp can be modelled as some form of ‘leakage’ whereby only a fraction of the previous output is added to each new input sample. Hence, the transfer function of a real op amp is given by (3.3).

$$H(s) = \frac{\sqrt{A_V}}{\left(\frac{s}{\omega_1} + 1\right)} \cdot \frac{\sqrt{A_V}}{\left(\frac{s}{\omega_2} + 1\right)} \cdot \left(\frac{s}{\omega_Z} + 1\right) \quad (3.3)$$

where A_V denotes the op amp dc gain; ω_1 , ω_2 , ω_Z represents the first, second amplifier pole and zero respectively.

The op-amp slew rate limitation and the saturation levels are modelled in SIMULINK using the slew rate and saturation blocks, placed in series with the integrator as shown in

Fig.3.3. According to [6], the 3rd harmonics distortion of the CT $\Delta\Sigma$ modulator is given by (3.4).

$$HD3 = \frac{g_3}{16g_1^4} \cdot \left(\frac{1}{R_{in}} + \frac{1}{R_{fb}} \right) \cdot \left(\frac{\hat{v}_{in}}{R_{in}} \right)^2 \quad (3.4)$$

Fig. 3.3 First opamp RC Integrator nonidealities model including opamp 1/f noise, resistors thermal noise, finite opamp linearity, finite dc gain and GBW, slew rate and saturation voltage

Using the square-law model of a MOS transistor, the non-linear transconductance of the opamp input pair can be derived from transistors operating in the strong inversion region as given by (3.5a) and (3.5b).

$$g_1 = \frac{I_D}{V_{GT}} = \frac{g_m}{2} \quad (3.5a)$$

$$g_3 = \frac{I_D}{8V_{GT}^3} = \frac{g_m^3}{64I_D^2} \quad (3.5b)$$

where V_{GT} is the effective gate-source voltage and g_m is the transconductance of the input transistors.

3.2.6 Transconductor (gmC) Modeling

In the design of higher order CT $\Delta\Sigma$ modulators, the more power efficient transconductor (gmC) structure can be considered from the second integrator onwards. The S-domain transfer function for a generic transconductor based integrator (gmC) is given by $H(s)=g_m/sC$. Fig. 3.4 illustrates the model for the gmC cell. The input voltage signal is converted into a current signal that charges the load capacitor. Since the non-idealities of the integrators beyond the first do not generate significant degradation in the performance of the CT $\Delta\Sigma$ modulator [5] [6], their non-idealities are often neglected when considering the high level model.

Fig. 3.4 Model of Transconductor (gmC) Cell

3.3 Implementation Example – A 4th Order CT CIFF CT $\Delta\Sigma$ modulator

To illustrate some key design insights and to validate the modelled non-idealities, a

 Fig. 3.5 Entire differential model for the 4th-Order Non Return-to-Zero (NRZ) CIFF CT $\Delta\Sigma$ modulator

4th-order CT $\Delta\Sigma$ modulator in the NRZ architecture is designed. As such, the top level design target specifications for the implementation example are summarized in Table 3.1. The proposed modeling technique will be used to simulate for the key functional blocks requirements for this fourth order CT $\Delta\Sigma$ modulator needed to fulfill the above specifications. The opamp RC integrator is chosen for the first integrator for linearity reasons. The second, third and fourth integrators are realized with transconductors (gmC) structures so as to conserve power. The model is done in a fully differential fashion, hence allowing a closer visualization of the actual circuit. In particular, the first integrator design specifications will be fully derived.

Design Parameters	Design Summary for NRZ Implementation
Architecture	Cascade Integrators Feed Forward (CIFF)
Order	4
Input Signal Bandwidth	25kHz
Oversampling Ratio (OSR)	64
Peak SNR	85dB
Peak Dynamic Range (DR)	90 dB

Table 3.1 Table showing the Modelling Example Targeted Performance

3.3.1 Modeling of 4th-order NRZ CIFF CT $\Delta\Sigma$ Modulator

In the NRZ implementation, the DAC feedback pulses are held constant for each entire sampling period without being returned to the common mode voltage as in the case of the return-to-zero (RZ) case. The coefficients for the loop filter are used to calculate for the physical design values of the resistors and charge storing load capacitors. With the realization of this model, the translation from model to schematic in the later design phase will be much smoother. This is essential since the simulation in actual low level

transistor level will be extremely time consuming and hence difficult for debugging of architectural errors.

Fig. 3.5 shows the structure for the NRZ architecture. With the choice of a partial zero optimization, a local feedback is necessary as performed by gm4. In the first integrator, the active noise and the non-linearity of the OTA are both modelled. The actual loop filter consisted of one opamp-RC integrator with three gmC cells. The feed forward output currents from the gmC cells are summed across two resistors in accordance to the CIFF structure. The last gm cell acts as a Voltage-to-Current (V/I) conversion, whereby the output current passes differentially through the resistors. This technique is seen in [7] to convert the current back into a voltage signal for comparison by the single-bit voltage comparator. The excess loop delay is compensated by having a direct path across the loop filter. In order to model this compensation feedback path, it should be noted that the path can be thought of as a single-bit feedback DAC that feeds back a scaled current signal back into the summing resistor whose value is decided by the quantizer output signal. In this work, the delay compensated is IT_s .

This DAC current feedback implementation allows the modeling of DAC mismatches which can also be included in the main feedback branch. Jitter in the clock is injected at both the main DAC and auxiliary feedbacks. Clock variation is not considered at the quantizer as it is not the dominant source of performance degradation. Each key component specification was then simulated against the design requirements to find out the least stringent value necessary.

3.4 Results

The implemented modulator was simulated to evaluate the maximum tolerance of the architecture on the modeled non-idealities while fulfilling the specifications presented in section 3.3. Table 3.2 summarized the minimum functional blocks requirements needed to achieve the targeted specifications with the non-idealities modeled. Fig. 3.6b shows the PSD plots for the implemented modulator. For comparison, the PSD of the ideal modulator is also shown in Fig. 3.6a below. The input frequency is chosen to be at 6.25 kHz for the simulations so that the third harmonics falls within the signal bandwidth. To evaluate the peak Signal to Noise Ratio (SNR), the input range was swept across the entire dynamic range. A plot of the SNR was then plotted against the input values as shown in Fig. 3.7a and Fig. 3.7b.

Modulator Non-idealities	Value
Input referred noise	150 μ Vrms
Linearity (HD3) with Vgt of the op-amp input devices	0.14V
Finite gain bandwidth (GBW)	4.9MHz
Finite DC gain	75dB
Slew rate (positive & negative slew)	1.2V/ μ s
Saturation voltages	$\pm$ 0.5V
Clock jitter	0.005%Ts
Excess loop delay	1*Ts

Table 3.2 Summary of Design Specification for Required Performance

In this section, a high level circuit-based fully differential model for the CT $\Delta\Sigma$ modulator implemented in SIMULINK has been proposed. To ensure accurate simulations, various non-ideal effects have been discussed and incorporated into the

Fig. 3.6a PSD of the Ideal 4th Order CIFF CT $\Delta\Sigma$ modulator Fig. 3.6b PSD of the Modelled 4th Order CIFF CT $\Delta\Sigma$ modulator

proposed model. The fully differential structure enables realistic and intuitive modelling. A 4th-order CT $\Delta\Sigma$ modulator was implemented using the proposed modelling. Results indicating the minimum requirements for the functional blocks were presented. This modelling technique can be included as a high level evaluation step within the design flow and hence improving the design time for CT $\Delta\Sigma$ modulators.

Fig. 3.7a Dynamic Range Plot of the Modelled 4th Order CIFF $\Delta\Sigma$ Modulator (Top)Fig. 3.7b Zoomed Dynamic Range Plot of the Modelled 4th Order CIFF $\Delta\Sigma$ Modulator (Bottom)

3.5 Architectural Design Considerations

Once the oversampling CT approach is chosen, fulfilling a performance specification can be achieved with more than one architectural decision. In other words, there are various choices to be made to trade-off performance and power. Some top level design considerations could be the filter order and multi/single bit internal quantization. This study chose the Cascade Integrator Feed Forward (CIFF) structure for its power

efficiency due to the following apparent reasons. Firstly, the CIFF structure essentially only requires one main DAC feedback path which saves on design complexity and also power consumption. In addition, the output of the filter integrators in feedback structures have to process both the signal and quantization noise, which necessitates OTAs with higher Bandwidth (BW) and Slew Rates (SR) with larger output dynamic ranges. This section presents MATLAB modelling which showcases some interesting analysis that have not been extensively treated by the research community such as, firstly, the dependency of the modulator's immunity to clock jitter with the filter order. Secondly, this section also presents the sensitivity of the modulator performance to process variation with respect to the choice of filter order. Since the performance varies in first order to both the choice of filter order and quantizer resolution, the results used for benchmarking are normalized to the optimized SNR for each chosen configuration.

3.5.1 Modulator Performance Dependency to Clock Jitter

It was mentioned in Section 3.2 that the prominent degradation caused by clock jitter is through injection to the main feedback DAC. This is because the modulator will not be able to differentiate if this error is from the input or not. This is especially detrimental for slow frequency noise. For high frequency noise, the low pass nature of the loop transfer function will provide some attenuation synonymous to the anti-aliasing effect. In view of this weakness, there had been several techniques proposed to ease the requirements of the clock source, which otherwise may even be impossible to achieve high modulator SNRs [8], [9] and [10]. The intuitive approach to ease phase noise requirement is to incorporate a multibit internal quantizer [11] and [12]. This reduces the rate of change of feedback signal and hence making the main DAC less susceptible to jitter. This is generally the most straight forward way for improving jitter immunity

as it minimizes the wideband error propagating into the filter. However, multibit feedback DACs are prone to mismatches that will result in signal related errors that can cause distortions. Hence, Dynamic Element Matching (DEM) is usually required to maintain linearity [13] and [14]. Another method is to use a Return-to-Zero (RZ) feedback whereby the first half integration T_s cycle is made independent to jitter by realising a time constant that is derived from a stable capacitor integration time for example. This technique removes most of the error from the first integration but not from the subsequent cascaded integrators in the filter chain. This is because the sampling by the internal quantizer has an aperture uncertainty caused by jitter. This sampled error although noise shaped, is dependent on the filter order. The higher the order, the larger will be the accumulated error. To analyse this it is only possible to perform simulations at high level. The simulation time for transistor level schematics will be too time consuming to visualise any fruitful results. Fig. 3.8a, Fig. 3.8b and Fig. 3.8c shows the SNR for each modulator with filter order 2, 3 and 4 when the jitter injected is increased from 10fs to 1ns. The SNRs are all normalized to their respective peak values for fair comparisons. In addition, the Out of Band (OOB) gain is kept uniformly to 1.5 and the Oversampling Ratio (OSR) maintained at 64. It can be seen that jitter degrades the performance of the fourth order modulator the most rapidly. When the internal quantizer resolution is increase from 1b to 5b, the SNR improves as shown across all figures. Without any jitter immunity enhancement, for a second order modulator with 1b internal quantizer, to maintain 90% of the maximum achievable SNR, the phase noise from the clock source should not give rise to a period jitter of more than 380ps at a sampling frequency of 3.2MHz. On the other hand, for a fourth order modulator with 1b quantizer, the clock source should not generate more than 13.3ps jitter to keep SNR drop within 10%. In compensating for jitter, for CIFF

architectures, it is generally achieved through rendering the feedback pulse length or shape to increase immunity to clock edge fluctuations. From the analysis above it shows that compensation to improve jitter immunity is most likely necessary when higher order architectures are employed. Since a higher order structure also reduces the loop timing for quantization and feedback processing, it is also typically harder to add high resolution quantizers for the linearization of multibit DACs that usually take away a fraction of the sampling period.

Nevertheless, it is also useful to re-analyze the findings to obtain the optimized filter order for a given specification such as the SNR. The objective of this section is to evaluate the architecture trade-off between design complexity and jitter sensitivity to achieve the required performance. Although feedback pulse shaping [9][15][16] is effective in relaxing clock jitter requirements, it entails a necessity for enhance OTA bandwidth to cope with the faster feedback transients. Fixed Time On Return-to-Zero (RZ) feedback [8][10] helps but also increases the speed requirements for the OTA in the first integrator due to a more frequently switching feedback pulse. Hence, the common approach to the jitter design constraint is incorporating of multibit quantizers. The use of high resolution internal quantizers increases complexity of design substantially. Therefore, it is useful to keep the internal quantizer resolution to its minimal.

The thesis considers the architecture with Non-Return-to-Zero feedback (NRZ) feedback pulse. From [17], the total In-Band-Jitter-Noise (IBJN) can be expressed as (3.6).

$$IBJN = 2\pi^2 \frac{V_{sig}^2 \cdot BW^2 \cdot \sigma_j^2}{OSR} + \frac{OSR \cdot BW^2 \cdot \Delta^2 \cdot \sigma_{NTF,RMS}^2 \cdot \sigma_j^2}{3} \quad (3.6)$$

Fig. 3.8a Normalized SNR Plot of 4th Order Modulator with Injected Period Jitter (Top)
 Fig. 3.8b Normalized SNR Plot of 3rd Order Modulator with Injected Period Jitter (Middle)
 Fig. 3.8c Normalized SNR Plot of 2nd Order Modulator with Injected Period Jitter (Bottom)

where

$$\sigma_{NTF,RMS}^2 = \frac{1}{\pi} \int_{-\pi}^{\pi} \left[|NTF(e^{j\omega})|^2 \cdot (1 - \cos\omega) \right] d\omega \quad (3.7)$$

(3.6) reveals two portions to the IBJN contributed via the main feedback path. They are attributed to the input signal and out of band shaped noise respectively. Since the OSR for high SNR audio range CT $\Delta\Sigma$ Modulators are typically high (>64), the second constituting term in (3.6) will be dominant. This source of IBJN can therefore be reduced by using a higher resolution quantizer with a smaller step size Δ , reducing the OSR and also adopting a less aggressive NTF with a smaller RMS value.

The SQNR of a 3rd order modulator with 1b quantizer sampled at 3.2MHz (OSR=64) can achieve a SQNR of 85dB. To achieve the same performance with a 2nd order modulator, either the OSR be increased or a multibit quantizer is utilized. It can be simulated that an increase of OSR to 128 can meet the target SQNR of the 3rd order modulator. With this change, the sensitivity to jitter is evaluated. Fig.3.9 shows the degradation of normalized SNR, $\frac{SNR(\sigma_j)}{SNR(\sigma_j = 10fs)}$ of the two modulators

under the influence of jitter injected at the feedback path. It can be observed that the jitter sensitivity is now increased as compared to the original modulator with OSR of 64. In order to maintain the same jitter sensitivity, the resolution of the quantizer can be increased optimally to b=2. With this approach, the jitter requirements can be met while keeping the design complexity low.

It is also interesting to discuss the relationship of modulator filter order with jitter sensitivity [18]. Fig.3.10 shows the PSD of the modulator's NTF superimposed onto the clock phase noise. When the modulator order is increased, the Out of Band (OOB) shaped quantization noise is increased. Since the feedback signal is sampled by the

modulator clock, it can be described as a multiplication in the time domain. Hence, the frequency convolution of the clock phase noise with the shaped quantization noise can result in an in-folding of quantization noise into the frequency band of interest. As such, when the filter order is increased, the modulator becomes more sensitive to clock phase noise in this aspect.

Fig. 3.9 Normalized SNR of CT $\Delta\Sigma$ Modulators with NRZ feedback with different architectural considerations

Fig. 3.10 Quantization Shaped Noise trend with Filter Order and superimposed on the Jittered Clock Phase Noise

3.5.2 Modulator Performance Dependency to Process Variation

CT $\Delta\Sigma$ modulators are susceptible to process variations because the integration constants are realized with physical resistors and capacitors which cannot be precisely matched. As opposed to CT $\Delta\Sigma$ modulators, the DT $\Delta\Sigma$ modulators have both the integrating resistors and capacitors implemented using capacitors. The current flowing through a resistor in CT can be explained intuitively in DT as the time average periodic charge transfer (i.e. rate of charge transfer) of a sampling capacitor. Since both the resistor and integrating capacitors can be designed with the same unit size, they can be placed close together while taking into account of careful layout considerations. As such, this drawback has long been one of the reasons why the DT modulators have been chosen over their CT counterparts especially for low signal bandwidth applications. This section presents the results of a series of analysis visualizing the sensitivity of the modulator SNR to process RC variation with different internal quantizer resolution, modulator filter order and also the Oversampling Ratio.

The background reason for the shift in SNR due to RC variation is primarily caused by the movement of the Loop Transfer Function (LTF) poles. This leads to a less efficient noise shaping filter dynamics that causes an elevation of noise floor. Fig. 3.11a and 3.11b shows the SNR of the modulator with orders 2 and 4 respectively when the RC process variation is varied from -50% to 50%. There are several observations worth mentioning. Firstly, it can be seen that across all filter orders, increasing the internal quantization resolution can decrease the sensitivity to RC variations. The general trend with RC variations indicates a decrease in SNR and even becomes unstable when RC varies to a smaller value. In addition, decreasing filter order improves the robustness and also decreases RC sensitivity. It can be observed that a 5b internal quantization in combination with a low 2nd order filter can tolerate RC variation up to 20% with only a

minimal fluctuation of $\pm 5\%$ in SNR performance. This has heavy implications in the precision of the tuning circuitry. For a single bit 4th order modulator, in order to maintain performance within $\pm 5\%$, it is essential to keep RC variation to be within $\pm 10\%$.

Fig. 3.11a Normalized SNR Plot of 4th Order Modulator with Overall RC Percentage Variation

Fig. 3.11b Normalized SNR Plot of 2nd Order Modulator with Overall RC Percentage Variation

It increases the complexity of the tuning circuitry to design with small unit sized capacitors covering the typical corner variations, resulting in a huge tuning array. The variations in resistor and capacitor values due to process corners result in the shifting of NTF zeroes. This zero movements degrade the noise shaping efficiency of the modulator, therefore affecting the final achievable SNR. In practical development of audio band CT $\Delta\Sigma$ Modulators where OSR is typically large, it is common for the modulator to be thermal noise limited. In such a situation, the in-band noise is constituted mainly of the input resistor thermal noise that is not affected by the NTF. The quantization noise, which is shaped by the NTF, is embedded under the thermal noise level. Under RC variations, the in-band quantization noise might be elevated. These process dependent variations are sometimes addressed by post silicon trimming which increases circuit implementation complexities as well as consumes valuable production tester time. It is thus beneficial to work out through architectural considerations to resolve this process dependent deficiency. One such strategy is to lower the quantization noise to a level such that any RC variation-caused quantization elevation will not impact the SNR as much. One possible way is to increase the OSR. However so, this improvement in modulator robustness to RC variations comes with the expense of larger power consumption.

Fig. 3.12 shows the changes in the modulator SNR with RC variation for OSR of 64 and 128 respectively. The thermal noise boundary is included too. In this analysis, the targeted reference SNR of 95dB was chosen. This is the performance for the modulator when the quantization and thermal noise matches. The SNR of the modulator under study with OSR of 64 and 128 is normalized to this thermal noise target under nominal conditions. It can be observed that the modulator with high OSR of 128 is more resilient towards RC variations as it is sufficiently thermal noise limited.

Fig. 3.12 Diagram showing Normalized SNR of modulators with OSR of x64 and x128 with Thermal Noise Boundary

3.5.3 Modulator Performance Dependency to First Integrator Bandwidth

The last parameter that is of paramount importance to the performance of the modulator that might involve heavy trade off with power is the bandwidth of the first integrator. The performance of the first integrator directly affects the modulator since there are no prior gain stages to attenuate any non-idealities. As such, similar to distortions of the feedback DAC, noise injected (i.e either in the form of random noise or circuit-based, signal-related distortions) at the first integrator inputs especially is viewed by the system as coming from the inputs themselves, hence reacting to them. Because of the sensitivity of the system to the first integrator, the opamp-RC structure is often used as shown in Fig. 3.13. This structure gives the best overall linearity while providing a virtual ground at the OTA inputs for feedback summation. Insufficient bandwidth in the first integrator can result in the generation of excess loop delay, which might cause a shift in the LTF and hence affect the efficiency of the noise shaping dynamics. In addition, the underperforming OTA can also affect other interfacing blocks. For example, a slow OTA will result in an enlarged fluctuations at the summing node of the

Fig. 3.13 A typical Opamp-RC Integrator used for its high linearity

integrator. In a normal feedback structure whereby a current steering based DAC is used, these voltage swings can affect the feedback charges in the second order. This is due to the finite output impedance of the current sources that are sourcing the charging current. Since this phenomenon is signal related, it will amount to distortions and the formation of frequency spurs in the output PSD spectrum.

This section studies the effect of modulator order and the choice of internal quantizer resolution to the requirements of the first integrator OTA bandwidth. This is benchmarked against the SNR of the modulator achievable with each bandwidth and quantizer resolution decision. As of the above treatment in section 3.5.1 and 3.5.2, the SNR values predicted by MATLAB are normalized to the values when the OTA bandwidth is at $1 \cdot F_s$. It should be noted that this study is carried out on an unscaled modulator with the same Noise Transfer Function (NTF) generation settings.

Fig. 3.14a shows the plot of the normalized SNR with different modulator orders of 2, 3 and 4. This is done when the quantizer is configured as a 1b comparator. The X-axis is the OTA1 Unity Gain Bandwidth (UGBW) in terms of multiples of the sampling frequency F_s . It can be seen that the modulator is most affected by the OTA bandwidth

with a 4th order filter structure. This is primarily due to the large total phase delay when signal propagates down 4 cascaded stages of integration. When the bandwidth drops to around 63% F_s , the 4th order modulator experiences a dramatic drop in SNR.

Fig. 3.14a Normalized SNR Plot with Percentage (%) Variation in 1st Integrator OTA Bandwidth with 1b Internal Quantizer

Fig. 3.14b Normalized SNR Plot with Percentage (%) Variation in 1st Integrator OTA Bandwidth with 5b Internal Quantizer

This is as oppose to the 2nd and 3rd order structures whereby they only suffer a degradation of SNR to 87% and 77% of the SNR when bandwidth is at 1Fs. It is also interesting to observe that for the 2nd order modulator, the SNR keep on increasing when the OTA1 bandwidth widened. At the other extreme when OTA1 bandwidth keep increasing to 4Fs, the SNR of the 3rd and 4th order modulator remains relatively flat. Next, the quantizer resolution is increased from 1b to 5b. The same plots are obtained and shown in Fig. 3.16b. The first observation is the improvement in the sensitivity of the modulator to OTA1 bandwidth. Instead of a cliff dropping SNR for the 4th order modulator when the bandwidth falls below 63%, this value had become lower to 45%. The other observation noted was that the gradual increase in SNR performance with OTA1 bandwidth in the 2nd order modulator observed in Fig. 3.15a is not present in Fig. 3.15b anymore. With the quantizer resolution increased to 5b, the gain of the quantizer becomes fixed to a constant as opposed to the single bit comparator.

As the analysis is done on an unscaled modulator without any hard voltage limitation placed at each integration outputs in order to isolate other non-idealities, it should be noted that the usable OTA1 bandwidth ranges might be reduced. Not only this, second order effects such as OTA1 virtual ground fluctuation that might manifest as a result of a slow OTA1 is also not considered here. Therefore, to allow for sufficient margin for such variations, the bandwidth for the first OTA1 has been conveniently chosen to be at 1.5Fs. However so, it should be mentioned that in comparison with a Discrete Time (DT) modulator, the bandwidth of OTA1 is already much relaxed.

3.6 References

- [1] M.Ortmanns, F.Gerfers, “Continuous time sigma delta A/D conversion-fundamentals, performance limits and robust implementations,” Springer, Netherlands, 2006.
- [2] M. Lansirinne and K. Halonen, “SSDSIM—a very fast and versatile simulator for SD modulators,” in *Proc. ECCTD ’99*, Sept. 1999
- [3] Inc. The mathworks. Matlab 2007a and Simulink 6.6. The MathWorks, Inc. Natick, MA(2007)
- [4] P. M. Chopp and A. A. Hamoui, “ Analysis of Clock-Jitter Effects in Continuous-Time $\Delta\Sigma$ Modulators Using Discrete-Time Models,” *IEEE Trans. Circuits and Systems I, Regular Papers*, vol. 56, no. 6, June 2009.
- [5] L. Hernández, A. Wiesbauer, S. Patón, A. Di Giandomenico, “Modelling and optimization of low-pass continuous-time sigma-delta modulators for clock jitter noise reduction,” *Proceedings of the 2004 International Symposium on Circuits and Systems*, vol. 1
- [6] Lucien L.Breems, Eric J.van der Zwan and Johan H.Huijsing-Design for optimum performance-to-power ratio of a continuous time sigma delta modulator. *Proc.Eur.Solid State Circuits Conf.* 318-321, September, 1999.
- [7] Paton, S., Di Giandomenico, A., Hernández, L., Wiesbauer, A., Pötscher, P. and Clara, M., A 70-mW 300-MHz CMOS continuous-time sigma-delta ADC with 15-MHz bandwidth and 11-bits of resolution. *IEEE J. Solid-State Circuits.* v39 i7. 1056-1062.

- [8] O. Oliaei and H. Aboushady, "Jitter effects in continuous-time $\Delta\Sigma$ modulators with delayed return-to-zero feedback," in *Proc. IEEE Int. Conf. Electronics Circuits Syst.*, Sep. 1998, pp. 351-354.
- [9] M. Ortmanns, F. Gerfers, Y. Manoli, „ A continuous-time $\Delta\Sigma$ modulator with reduced sensitivity to clock jitter through SCR feedback," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 875-884, May 2005
- [10] K. Nguyen, B. Adams, K. Sweetland, H. Chen, and K. McLaughlin, "A 106 dB SNR hybrid oversampling ADC for digital audio," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2005, vol. 1, pp. 176–591.
- [11] F. Gerfers, M. Ortmanns, P. Schmitz, Y. Manoli and K. M. Soh "A clock insensitive multibit DAC architecture for high performance low-power continuous-time $\Delta\Sigma$ modulators," in *Elect., Circuits and Syst. (ICECS) IEEE Proc International Conf*, 2003.
- [12] R. Tortosa, J. M. de la Rosa, A. Rodriguez-Vazquez, and F. V. Fernandez, "Analysis of clock jitter error in multibit continuous-time $\Delta\Sigma$ modulators with NRZ feedback waveform," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 4, pp. 3103-3106, May 2005
- [13] R. Adams, K. Q. Nguyen, and K. Sweetland, "A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling," *IEEE J. Solid State Circuits*, vol. 33, pp. 1871-1878, Dec 1998
- [14] R. Radke, A. Eshraghi, and T. S. Fiez, "A spurious-free $\Delta\Sigma$ DAC using rotated data weighted averaging," in *Proc. IEEE, Custom Integrated Circuits Conf. (CICC)*, pp. 125-128, May 1999.

- [15] Van Veldhoven, R.H.M. "A triple-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver", *Solid-State Circuits, IEEE Journal of*, pp. 2069 - 2076 Volume: 38, Issue: 12, Dec. 2003
- [16] Jo, J.-G.; Noh, J.; Yoo, C. "A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC and High-Speed DWA", *Solid-State Circuits, IEEE Journal of*, On page(s): 2469 - 2477 Volume: 46, Issue: 11, Nov. 2011
- [17] Chen X., "A Wideband low-power continuous-time Delta-Sigma modulator for next generation wireless applications" Ph.D. dissertation, Sch. Elect. Eng. Comp. Sci., Oregon State University, Corvallis, OR., 2007
- [18] Ramy. S, Sebastian. H and Samuel. P, "Analysis and Modeling of Clock Jitter Effects in Delta-Sigma Modulators" *MATLAB – A Fundamental Tool for Scientific Computing and Engineering Applications (Book Chapter) – Volume 1*, ISBN 978-953-51-0750-7, Sep 2012.

Chapter 4 Chapter 4 An Improvement in Multibit Internal Quantizers utilizing the Flash Architecture

Abstract This chapter addresses the need to conserve the power of the multibit quantizer, particularly when implemented with the popular flash architecture in a CT $\Delta\Sigma$ Modulator. This is achieved by observing that most of the comparators in a multibit flash quantizer are actually idling. As such, a rapid detection scheme is devised to locate the idling comparators and switch them off to save power.

4.1 Introduction

The design of Oversampling $\Delta\Sigma$ modulators experience various paradigm shifts. These design changes were made as a result of the need for higher resolution for higher performance Analog-to-Digital (AD) conversions. While high order filter structures were heavily exploited to provide large in-band gain to attenuate quantization noise, the stability of the modulator becomes largely compromised and the input voltage dynamic range drops proportionately. Not only this, to keep signal integrations within 1Ts, the speed of the supporting active components had to be enhanced, hence burning power at the expense for performance. Due to this, another way to boost modulator performance considered is minimizing the inherent quantization noise level. Essentially, it is to increase the internal quantizer resolution. Fig. 4.1 shows the graphical output waveform of a single versus a multibit feedback signal. A modulator with a multibit internal quantizer will experience lower quantization noise level across wide frequencies. There are several folds of advantages when multi-bit quantizers are

used. Firstly, from the system's perspective, the overall quantization noise becomes smaller.

Fig. 4.1 Waveform showing Single Bit (Top Left) Versus Multibit (Top Right) Conversion Transfer Characteristics

Fig. 4.2 Waveform showing the Quantization Noise for Single Bit (Red) and Multibit (Blue) Quantizer

(4.1) shows the immediate enhancement in SNR when the internal quantizer resolution is increased. Fig. 4.2 shows the increase in SNR with the internal quantizer bit length. Fig. 4.2 shows the quantization noise variation across the input voltage range. Fig. 4.1 shows the input and quantized output signals together. As the input varies, the quantization error is given by the difference between the continuous input and discrete output signals, which is bounded between $-\Delta/2$ to $\Delta/2$.

If it can be assumed that the sample to sample input changes is uncorrelated and not saturating the quantizer, the quantization error is then a random process with uniformly distributed amplitude just like that of an additive white noise. With this assumption, it is well known that the total quantization noise can be derived to be $\Delta^2/12$. In order to

derive the SNR of the quantizer, the input signal power of a sinusoidal output with the maximum amplitude without saturating the quantizer can be derived to be

$V_{out,max}^2/2 = 2^{2B-3}\Delta^2$, where B is the quantizer resolution. Therefore, the SNR can be evaluated as the ratio between the signal and noise power. This power ratio can be expressed as $3/2 (2^{2B})$ or in decibels (dB) (4.1). It becomes clear that for each bit increase in the quantizer resolution, there is a 6dB improvement in SNR.

$$SNR(dB) = 1.76 + 6.02B \quad (4.1)$$

The above derivation can then be placed into the context of a $\Delta\Sigma$ modulator. Due to the oversampling and noise shaping characteristics, the quantization noise in the signal band is smaller as compared to a Nyquist rate quantizer. The SNR of a $\Delta\Sigma$ modulator depends on its maximum input power versus the total inband noise. As the quantizer resolution increases, the level of Out of Band quantization noise up to $f_s/2$ decreases as discussed before. As a result, the input to the quantizer can reach higher amplitude before saturating the quantizer. This results in a higher MSA without going unstable. With the lowering of the Out of Band quantization noise, it is also possible to design for a more aggressive NTF that pushes more inband noise out to higher frequencies.

Another effect of utilizing a multibit quantizer is the reduced jitter noise sensitivity of the feedback. This is because the rate of change of feedback is now slower as the quantizer resolution increases. Due to a larger number of quantization steps used, the change in feedback signal between samples is smaller, hence resulting in a decrease in feedback noise in the presence of jitter. All of the above discussed can improve the SNR of a modulator. In addition, Multibit Quantizers (MBQ) provides feedbacks that track the input much closely. Since only the difference is integrated especially for CIFF architectures, the dynamic requirements on the power hungry active OTA1 of the first integrator will be greatly relaxed.

These advantages come with the cost of a more complex design. The feedback DAC has to be enlarged to accommodate bitwise charge feedback into the filter. These are controlled by multiple signal lines which also occupy substantial routing silicon area. The linearity of the multibit feedback DAC has to be seriously considered now. To ensure this, Dynamic Element Matching (DEM) is commonly employed to randomize mismatches between individual current cells. This synchronized digital block consumes precious loop delay. In order to still keep within $1T_s$ sampling cycle, Continuous-Time (CT) modulators compensate for Excess Loop Delay (ELD) to account for the delay required.

Conventionally, to implement multibit quantizers, the flash architecture had been commonly utilized. Intuitively, the flash converter provides minimal latency A/D conversion. However, it is well-known that flash converters can be rather area consuming when the bit length is increased. This is due to the 2^N comparators required

Fig. 4.3 Diagram showing comparison in the number of Comparators for Flash and SAR Architecture

for N -bit conversion. Fig. 4.3 shows the exponential increment in comparators with the increase in bit length. Not only this, the rapid increase in comparators quickly loads the output of the last integrator. In order to keep offset low for each comparator, the input differential devices (NMOS or PMOS) as shown in Fig. 4.4 has to be sized up, hence worsening the last integrator output loading conditions. Although there had been proposals to use minimal device size while employing calibration, this will be at a

higher backend production cost. Although at the lower frequency spectrum whereby architectures exploiting hardware recycling such as of the SAR structures can be used, it will not be viable in high speed high bandwidth applications. This is because higher bandwidth structures necessitates high sampling rates that results in a minimal sampling period available for the quantization, integration and miscellaneous (such as DEM rotation) events. In addition, such techniques typically increase implementation complexities in order to achieve a low power consumption.

Fig. 4.4 Diagram showing the Single Sided Flash Converter with NMOS input stage sized up

Therefore, there seems to be no available replacement for the flash architecture quantizer for high performance modulators requiring speed.

It is understood that multibit feedback has been conventionally adopted for the implementation of high performance CT $\Delta\Sigma$ modulators for relaxing multiple design requirements for the system. The need for speed has rendered a large portion of the power budget to be assigned to the quantizer comparators, which often is implemented with the flash architecture. Previous researches [1-3] had proposed the concept of a tracking quantizer to reduce the number of comparators but are primarily more suited

for low speed applications. In this chapter, a technique is proposed to enable fast detection of comparator redundancies prior to making decisions for optimizing power consumption. The simplicity of the proposed circuit results in good speed performance with power reduction to the overall multi-bit quantizer design.

High performance CT $\Delta\Sigma$ modulators are often employed in communication applications, where the Oversampling Ratio (OSR) is often kept low due to technology and circuit limitations. Recent literatures [4-6] have reported CT $\Delta\Sigma$ modulators with the capability of handling input signal Bandwidth (BW) up to 20MHz or more. With low OSR values, these CT $\Delta\Sigma$ modulators are quantization noise limited. This is in contrary to modulators having high OSR values which are typically limited by the input thermal noise. With the added requirement for higher input bandwidth, even at low OSR values, the sampling rates can be very high. This therefore works out to smaller coefficients and translating to small integrating capacitors and resistors. This implies a smaller filter silicon area and the added advantage of low input thermal noise contribution. This pushes the emphasis in the attenuation of overall modulator noise to the filter order and quantizer resolution. The usage of multi-bit feedback can lower the wideband quantization noise synonymous with a high sampling rate. In such CT $\Delta\Sigma$ modulators, the first integrator BW and Slew Rate (SR) has to be large if the feedback is not made to track the input signal close enough. Multibit feedback reduces this requirement. A well-known issue of CT $\Delta\Sigma$ modulators is the system susceptibility to clock jitter. It is natural that the immunity to jitter can be improved by using a multi-bit feedback approach as much discussed in Chapter 3. This is because jitter error is manifested in the amount of CT charge feedback to the first integrator. Multibit feedback has the feature of reducing the amount of feedback charge at each sampling instance. Despite the advantages, multibit feedback comes with an exponential

increase in power consumption for each additional bit of resolution when the flash topology is used.

Researches explored into various methodologies to minimize this power penalty. One approach is by changing the entire quantizer architecturally. [7] proposed a Voltage Controlled Oscillator (VCO) based quantizer while [8] did the design with a time encoding quantizer. Along with implementation utilizing a time encoder, Asynchronous Delta Sigma Modulator (ADSM) also evolved. Although such time based implementation scheme proves to be power efficient, a Time to Digital Converter (TDC) is often required. The implementation is thus not straight forward with an increased computation requirement on the digital side primarily due to the finite time resolution that could possibly be resolved by doing digital interpolation.

The next approach is to make the quantizer more power optimized. In [1], the concept of a tracking quantizer is put forward. Publications [2] and [3] followed with similar concept with slight implementation variations. Fig. 4.5 illustrates the block level diagram of a CTSDM with a tracking quantizer. For a 4 bit multi-bit quantizer, instead of 16 comparators, only three are used, which incorporates a quantizer local feedback

Fig. 4.5 Block Level Diagram of Tracking Quantizer Concept

that switches the references into the correct conversion region. A counter is then made to track the Most Significant Bits (MSBs) output digital code. The addition of a counter increases the delay within the feedback signal path, hence resulting in a

reduced stability. By counting the signal in single steps, the BW of the local quantizer feedback becomes limited, which results in the following system requirement on the OSR chosen as shown in (4.2) where n is the number of bits of the multi-bit quantizer.

$$2^n < \frac{2}{\pi} \bullet OSR \quad (4.2)$$

(4.2) shows that the maximum resolution of the quantizer is restricted by the OSR. This chapter is organized as follows. Section 4.2 describes the conventional multi-bit quantizer design. Section 4.3 discusses the proposed design. Section 4.4 presents the simulation results and the conclusion.

4.2 Conventional Quantizer Design

This section reviews the conventional multi-bit quantizer design and discusses the necessity for a reduced comparator design while focusing on the flash topology.

4.2.1 Comparator Design

In order to handle high speed conversion so as to avoid generating too much delay and hence phase lag, typical voltage comparators are designed with two stages. Fig. 4.6 shows the first stage of the comparator as designed in [4]. Prior to the actual evaluation, the outputs of this stage are shorted together, giving a low time constant with a small gain. This creates a short sampling period and the outputs will swing to the correct values when the outputs are opened again following which the latch behind will be activated. It is important to note that the comparator continues to draw power even though the previous output values remains unchanged as the output zeroing procedure is mandatory for fast speed operations. Moreover, the capacitance looking into the quantizer inputs are constituted mainly by the gate to source parasitic

capacitances. This capacitance not only loads the last integrator output, demanding extra power to be allocated for driving them but also varies with the biasing conditions. This implies that there is a signal depending loading on the CTF outputs. In order to reduce this, it will be desirable to reduce the input capacitance of the quantizer by reducing their numbers while keeping the resolution. In addition, this pre-amplification provides small gain due to the small output impedance required for speed. The input stages are sized up for small offset caused by statistical mismatches

Fig. 4.6 Pseudo Differential Comparator Preamp Stage

resulting from fabrication non-idealities. When the differential inputs are small, the preamp stage will be slower. To hasten the comparison for high speed applications, the preamp has to be biased with a relatively large current to increase the input transconductance. All these result in a significant contribution to the overall modulator power consumption wherein optimization is highly justifiable.

4.2.2 Quantizer Output Analysis

The bit stream output from the multi-bit quantization process can be observed to contain excessive redundancies. Fundamentally, the CT $\Delta\Sigma$ modulator is oversampled

by a factor (i.e. OSR) decided during the generation of the Noise Transfer Function (NTF). Looking from another perspective, this implies that the input signal will be band limited. Fig. 4.7 shows a section of the consecutive digital output stream from a four bit quantizer of a CT $\Delta\Sigma$ modulator. The data is thermometer coded and indicated regions, R1 and R2, where dormant comparators are residing. These comparators regenerate the same digital output for an extended period of time. These dormant conversion periods are predictable and appropriate intervention can be devised to stop these unnecessary preamp regeneration steps. They can hence be turned off by using a quantizer tracking algorithm with sufficient redundancies.

Fig. 4.7 Output bit stream from 4 bit quantizer

4.2.3 Quantizer Comparator Efficiency

It is necessary to define a method to measure the power efficiency of the comparators for a multi-bit quantizer within a CT $\Delta\Sigma$ modulator whereby a sufficiently large OSR is applied. This is also to provide a fair comparison to quantify the improvement made by the proposed technique in the implementation of the tracking quantizer that will be presented in the Section 4.3. It is obvious that the power consumption is proportional to the switching activity. The higher the switching activity, the larger the power

required. The efficiency of the i th comparator for N_i number of clocking cycles can be expressed as follows in (4.3):

$$E_i = \frac{S_i}{N_i} \times 100\% \quad (4.3)$$

Where S_i is the number of times the comparator output changes state. Since S_i will be unchanged for a particular input signal at a fixed frequency and amplitude, the tracking quantizer concept essentially alters N_i to improve the comparator efficiency. In other words, the total number of comparisons per comparator is reduced given a fixed N comparison. Without the tracking quantizer, for N system clock cycles, the power consumption for the i th comparator P_i is therefore given by (4.4). Although the rate of state change is signal amplitude dependent, all comparators go through the same preamp regeneration phase which resulted in an almost equivalent power consumption of all comparators regardless of the quantizer amplitude. (4.5) gives the expression for the power consumption of the i th comparator when the tracking mechanism is installed. This implies that N_i is equivalent to N . P_Q is the total power consumption of the multi-bit quantizer and n is the number of bits for the quantizer. In (4.5), it can be seen that the power consumption is now really dependent on the individual comparator output transition frequency.

$$Q_i = \frac{P_Q}{2^n - 1} \quad (4.4)$$

$$Q_{i,tq} = P_Q * \frac{N_i}{N} \quad (4.5)$$

Where N_i is given as and p_i is the probability of the input of the quantizer at a particular amplitude.

$$N_i = p_i * N \quad (4.6)$$

To understand the quantity p_i , it is imperative to note that for a modulator with a multibit quantizer, the input to the quantizer is essentially very close to a sinusoidal waveform. Without the loss of generality, if it is assume that the maximum amplitude is ± 1 , the probability that the random variable, x_i lies within the interval can be given as in (4.7).

$$P(-1 < x_i < 1) = \int_{-1}^1 f(x_i) dx \quad (4.7)$$

If the Probability Density Function (PDF), $f(x_i)$ is integrated across the interval $[-\infty, \infty]$, it should be noted that the result will be 1. Therefore, from (4.7), the Cumulative Distribution Function (CDF) can be derived. The probability that a random variable y_i assumes a value equal or lesser than k can be expressed as in (4.8).

$$F(k) = P(y_i < k) = \int_{-\infty}^k f(x_i) dx \quad (4.9)$$

Now, if the PDF $f(x_i)$ is substituted by the sine function, (4.8) becomes (4.9). Fig. 4.8 gives the CDF plot of the sine wave when the input is restricted to the range of $[-1, 1]$.

$$P(y_i < k) = \frac{\arcsin(k)}{\pi} + \frac{1}{2} \quad (4.9)$$

From (4.9), the derivative can then be evaluated to obtain the PDF of the sine wave as given in (4.10). Fig. 4.9 shows the PDF of the sine wave.

$$p_i = f(x_i = k) = \frac{d[\arcsin(k)]}{dx_i} = \frac{1}{\pi\sqrt{1-k^2}} \quad (4.10)$$

Based on (4.2), a table is tabulated in Table 4.1 for the efficiency of the comparators for a third order single loop CT $\Delta\Sigma$ modulator with an OSR of x24 and input signal frequency BW of 20MHz. A 4 bit quantizer is utilized and all simulations are done with the input signal frequency at 18.75MHz with 8192 clock periods. Table 4.1 shows that the comparators activity is centred at the region of high signal concentration with efficiency that does not exceed more than 36%. In general, for each comparator, the trend is that efficiencies peak at middle input signal amplitudes and

Fig. 4.8 Cumulative Density Function with k within $[-1,1]$ Fig. 4.9 Probability Density Function with k within $[-1,1]$

Amp (FS)	Comparators Efficiency (%)							
	C1	C2	C3	C4	C5	C6	C7	C8
0.1	0	0	0	0	0	0.18	20	36
0.3	0	0	0	0	4.5	17	14	11
0.5	0	0	0.62	10	12	8.7	8.1	7.2
0.7	0.11	4.9	11	7.7	6.1	6.0	5.6	5.9

Table 4.1 Tabulated Efficiency of Comparators Without Tracking Quantizer

taper off on either ends. Only 8 comparators are plotted as the results will be symmetrical for the remaining comparators due to the sinusoidal input.

4.3 Proposed Quantizer Architecture

In order for the tracking mechanism to be applicable to high performance CT $\Delta\Sigma$ modulators, it has to be as simplified as possible. At the same time, the algorithm has to be able to lock in to a fast changing signal. From the system level, this translates to a system with a low OSR value, which is often the case when a large input BW is desired. From Fig. 4.7, it can be seen that the comparators prone to an output transition in the following sampling cycle lies in the region between R1 and R2. We define this region as the Active Comparators Region (ACR). The essential key for fast operation therefore lies in a rapid detection of the ACR.

This information can then be utilized to change either the active reference region or switching off dormant comparators for power conservation. Fig. 4.10 illustrates the ACR signal that is required for subsequent reference or comparators processing.

Fig. 4.10 Output bit stream from 4 bit quantizer showing detected ACR

4.3.1 Generation of the ACR Signal

Looking at Fig. 4.7, it can be observed that the ACR signal can be produced by subtracting the consecutive thermometer coded output bits. Mathematically, the expression describing this operation is as follows in (4.11):

$$y_{15}, y_{14}, \dots, y_0 = |(0 - x_{15})|, |(x_{15} - x_{14})|, \dots, |(x_1 - x_0)| \quad (4.11)$$

It may be thought that this subtraction of consecutive bits can be cumbersome but it can actually be accomplished by a mere logical XOR gate. The XOR logic identifies and evaluates the dividing boundaries between 0 and 1. With this, it is then possible to localise the region with the highest switching activity. Extra redundant comparators are set to remain active to capture out of range signals. Fig. 4.11 shows the practical implementation for the generation of the ACR signal.

Fig. 4.11 Method to generate the ACR signal using XOR for subtraction

4.3.2 Implementation of Tracking Quantizer

Upon generation, the ACR signal can be applied in various ways to achieve a power efficient design. The ACR signal can be used to turn off the dormant comparators. [1] and [2] used the ACR to change the reference voltage region for the comparators so that only the active number of comparators has to be realized in circuit. [3] proposed an auto-ranging algorithm for its tracking mechanism.

For demonstration purpose, the ACR signal in this chapter is used to turn off the dormant comparators for an analysis on the achievable efficiency. The single ended system is illustrated in Fig. 4.12 and verified via MATLAB simulations.

Fig. 4.12 Proposed fast ACR detection tracking quantizer

4.3.3 Speed of Proposed Tracking Quantizer

It should be noted that the local feedback from the output latches to the control multiplexers to turn off the sampling process of the dormant comparators can take a maximum of a one sampling clock delay. In the case for a 960MHz system clock, it translates to a delay of about 1.042ns. It would not have been possible if not for the proposed ACR detection technique, which inherently only incurred the delay of the

XOR gates if the multiplexers delay are assumed to be negligible. As such, the period delay can allow the insertion of logic gates to implement tracking algorithm that may be required should for example the active voltage reference is to be changed instead.

The number of comparators that has to be turned on each time can be derived from the CTSDM Signal Transfer Function (STF) and the Noise Transfer Function (NTF). If the STF is assumed to have unity gain, for an input sinusoidal of $v_{in}=A_{max}\sin(\omega_{int})$, the maximum rate of change of signal at the input to the quantizer can be evaluated by solving for $\left|\frac{dv_{in}}{dt}\right|_{max}$. From this analysis, it can be deduced that when OSR is reduced, a larger ACR would be needed to ensure system performance. It can be expected that there will be some variation from this value as a result of the quantization noise being fed back to the quantizer input. However, this additional discrepancy should be controlled due to the noise shaping NTF.

4.4 Results

This section summarizes the results of the model implemented in MATLAB for the proposed tracking quantizer. The CTSDM is a third order single loop system where a 4-bit multibit quantizer is used. The OSR is x24 and maximum input BW is 20MHz. The frequency of the input signal used for the simulations is at 18.75MHz.

The 4-bit tracking quantizer consists only of 4 active comparators at each sampling instance instead of 16. With this, the table of efficiency is tabulated below in Fig. 4.2.

Amp (FS)	Comparators Efficiency (%)							
	C1	C2	C3	C4	C5	C6	C7	C8
0.1	100	100	25	25	0.17	0.05	20	36
0.3	100	33	0.32	0.14	9.1	32	16	11
0.5	25	0.17	0.37	32	27	18	18	19
0.7	0.08	18	32	18	22	25	20	21

Table 4.2 Efficiency of Comparators with Tracking Quantizer

Comparing Table 4.1 and Table 4.2, it can be observed that the efficiencies are in general all increased. This shows the effectiveness of the tracking quantizer. Consider one input signal amplitude of $0.7F_s$, Table 4.3 shows the number of transitions made for the eight comparators for both with and without the tracking quantizer.

Comparators Transitions Count for $0.7F_s$, N_i							
C1	C2	C3	C4	C5	C6	C7	C8
8192	8192	8192	8192	8192	8192	8192	8192
1135	2018	2673	2977	2547	2109	1929	1965

Table 4.3 Number of Switching per Comparator for 8192 Cycles

Summing up the total number of transitions without the tracking quantizer gives $15 \times 8192 = 122880$. With the tracking quantizer, the number of transitions becomes:

$$\left[2 \times \sum_{i=1}^{2^n-1} (N_i) \right] - N_8 = 32741 \quad (4.12)$$

If the power consumed for one transition is a constant, then the power consumption with the tracking quantizer will ideally be only 26.6% of that without resulting in 73.4% savings.

4.5 Role of Multibit Quantizers in Low Bandwidth Applications

From the other application spectrum, there have been aggressive initiatives to reduce the power consumption of low to moderately fast $\Delta\Sigma$ Modulators. Every block within the modulator had been studied for power optimization. In the audio bandwidth range, for example, it had been proposed to reduce power consumption by keeping to single bit quantizers [9-10]. In addition to the extra current needed to power the flash quantizer, the larger number of comparators normally means a larger load for the driving integrator. The speed of the OTA forming this driving integrator therefore has to be increased, which implies a trade-off with power. From this point of view, this

technique can be put to good use. Not only can the power of the idling comparators be saved, the loading at the output of the driving integrator can be designed to be much lower. It is therefore apparent that low BW CT $\Delta\Sigma$ modulators can also benefit from this scheme.

4.6 Conclusions

In this chapter, the conventional quantizer design is briefly discussed, revealing the possibility for optimization due to the presence of dormant comparators. Although the concept of a tracking quantizer already existed, they are not targeted at high performance CT $\Delta\Sigma$ modulators. A fast tracking design for the detection of the ACR is proposed. Together with that, a method to evaluate the efficiency of the quantizer comparators was also put forward. A third order CT $\Delta\Sigma$ modulator with a 4-bit quantizer, input bandwidth of 20MHz and OSR value of x24 is modelled in MATLAB to demonstrate the feasibility of the idea. Although a high speed CT $\Delta\Sigma$ modulator is used as the test vehicle to demonstrate the proposed technique, it should be noted that the detection scheme can be equally as useful when applied to low BW CT $\Delta\Sigma$ modulators. On comparison with the same system without a tracking quantizer, the improvement in power consumption of the quantizer can potentially be significant.

4.7 References

- [1] L. Dorrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, "A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2416-2427, Dec. 2005.
- [2] X. Lu, "A novel signal-predicting multibit delta-sigma modulator," in *Proc. Of the IEEE Intl. Conf. on Electronics, Circuits and Sys., dec 2004*, pp. 105-108
- [3] S. Pesenti, P. Clément, and M. Kayal, "Reducing the number of comparators in multibit $\Sigma\Delta$ modulators," *IEEE Trans. Circuits Syst. I, Reg Papers*, vol. 55, no. 4, pp. 408-415, May 2008.
- [4] G. Mitteregger *et al.*, "A 14 b 20 mW 640 MHz CMOS CT $\Sigma\Delta$ ADC with 20 MHz signal bandwidth and 12 b ENOB," in *Proc. Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, 2006, pp. 131–140.
- [5] Matsukawa, K. Mitani, Y. Takayama, M. Obata, K. Dosho, S. Matsuzawa, A. "A Fifth-Order Continuous-Time Delta-Sigma Modulator With Single-Opamp Resonator" *Solid-State Circuits, IEEE Journal of*, vol.45, no.4, pp.697-706, May 2010.
- [6] A. Di Giandomenico, S. Paton, A. Wiesbauer, L. Hernandez, T. Pötscher, and L. Dörrer, "A 15 MHz bandwidth sigma-delta ADC with 11 bits of resolution in 0.13- μ m CMOS," in *Proc. Eur. Solid-State Circuits Conf.(ESSCIRC)*, Lisbon, Portugal, Sep. 2003.
- [7] M. Park and M. Perrott, "A 0.13 μ m CMOS 78 dB SNDR 87 mW 20 MHz BW CT Sigma Delta ADC with VCO-based integrator and quantizer," presented at the IEEE Int. Solid-State Circuits Conf., San Francisco, CA, 2009, paper 9.5.

- [8] L. Hernandez and E. Prefasi, "Analog-to-digital conversion using noise shaping and time encoding," *IEEE Trans. Circuits Syst. I, Analog Digit. Signal Process.*, vol. 33, no. 7, pp. 2026-2037, Aug. 2008.
- [9] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1.5-V 12-bit power-efficient continuous-time third-order $\Delta\Sigma$ modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1343–1352, Aug. 2003.
- [10] A. Sukumaran and S. Pavan, "Low power design techniques for single-bit audio continuous-time delta sigma ADCs using FIR feedback," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, Nov. 2014.

Chapter 5 A 95dB 230 μ W 4th Order Single Bit CT $\Delta\Sigma$ Modulator with Transconductance gmC Cells and Reduced Jitter Immunity for High Fidelity Audio Applications

Abstract This chapter presents a 4th order RZ CT $\Delta\Sigma$ Modulator using gmC transconductor cells as integrators for the second to fourth stages. A single bit quantizer is utilized, which is known for the consequential inherently linear DAC in the feedback. However, a JIE circuitry is included to reduce degradation in performance due to jitter. Process variation effects are also minimized with an on-chip PVTE circuitry. The overall power consumption is 153 μ A and was fabricated in 0.18 μ m CMOS technology. The simulated performance of this ADC achieved a SNR/SNDR of 87.1dB/85.4dB.

5.1 Introduction

In high fidelity audio applications, the Dynamic Range (DR) should be high (>90dB) to minimize the amount of gain variation required by the frontend Variable Gain Amplifier (VGA). One of the techniques in the design of oversampled Analog to Digital Converters (ADCs) to achieve high resolution is to have a high order filter structure. An increased order in the ADC will enhance the attenuation of the quantization noise [1], [2] and [3]. To ensure good linearity of the modulator, single bit quantizer is utilized for [4] and [5]. The comparator output is directly employed to generate the single bit feedback current to the first opamp RC integrator summing

node. The inherent linearity of such a DAC is beneficial since the timing required for the insertion of a Dynamic Element Matching (DEM) block places extra loop delay constraint especially critical in 4th order architectures. The proposed 4th order filter is implemented with mixed integrator structures consisting of a 1st opamp-RC integrator for linearity and power efficient gmC integrators from the 2nd stage thereafter. The feedforward with gmC is done by exploiting its output versatility, therefore removing the need for feedforward capacitors. This reduces the loading of driving integrator outputs which otherwise will require more stringent active OTA bandwidth requirements hence leading to a better filter power efficiency. An adder-less feedforward scheme is also proposed without loading the summing node of a typical opamp-RC last integrator, which allows the quantizer to directly sample the last gmC outputs. To enable this, a low gain preamp is proposed to minimize the input MOSFET gate to source capacitance of the comparator input differential pair, which have to be sized up for matching considerations. The preamp achieved <1fF variation across the targeted MSA, without which, the modulator will be distorted with the signal dependent capacitance transients. Process variation among the integrating resistors and capacitors are mitigated with an on-chip Process Variation Tolerant Enhancement (PVTE) circuitry which is initiated during the power up sequence but turned off during normal operation. The precision achieved by the PVTE enables the system to detect up to 2.08% variations in RC time constants. The jitter performance is reinforced with a fixed turn 'ON' Return-to-Zero feedback with a Jitter Immunity Enhancement (JIE) timing loop control that relaxes system sensitivity. The prototype is fabricated in 180nm CMOS technology, clocked with an OSR of 64 at 3.2 MHz and achieved a performance of SNR/SNDR of 91.4dB/89.2dB, hence obtaining a FoM_{SNDR} and $FoM_{Schreier}$ of 0.195pJ/conv and 171.8dB respectively while considering the power

from the JIE. The PVTE power consumption is not considered since it is only active during power up.

5.2 System Architecture Design

The system level architecture is realized with the Cascaded Integrator Feed Forward (CIFF) structure as shown in Fig. 5.1. The 4th order Noise Transfer Function (NTF) is generated with the Delta Sigma Toolbox [6], which is given in (5.1) as shown below. The Out of Band Gain (OOB) is chosen to be at 1.5 with an OSR of 64. With a 4th order design, the aggressive shaped quantization noise is pushed to high frequencies. This decreases the Maximum Stable Input (MSA) at the quantizer before instability kicks in. The OOB of 1.5 just manages an input dynamic range of fully differential input pk-pk of slow OTA responded without having to increase the quantizer bit length. The corresponding Loop Transfer Function (LTF) is given in (5.2).

Fig. 5.1 4th Order CIFF Continuous-Time $\Delta\Sigma$ Modulator Model

$$H_{NTF}(z) = \frac{(z^2 - 2z + 1)(z^2 - 1.998z + 1)}{(z^2 - 1.492z + 0.5643)(z^2 - 1.702z + 0.7869)} \quad (5.1)$$

$$H_{LTF}(z) = \frac{0.80465(z-0.8279)(z^2-1.79z+0.8345)}{(z^2-2z+1)(z^2-1.998z+1)} \quad (5.2)$$

When visualized within the z -domain Discrete Time (DT) unit circle as shown in Fig.5.2, it can be observed that the NTF possesses two origin and two conjugate zero pairs. The NTF is chosen to be partially optimized with only one conjugate pole pair. The reason is as follows. Due the moderately small input signal bandwidth (25kHz), conjugate pole pairs have to be placed close to the origin. Such distance generates coefficients that are very small and therefore resulting in a very small resonator feedback current. Moreover, since the quantization noise is already much attenuated at the origin, the noise shaping enhancement by the closer conjugate pole pair is not significant as flicker noise becomes the dominating noise source. Increasing the NTF noise shaping in spite of this will only add on to further elevation of high frequency noise. Moreover, a second resonator feedback will require additional circuitry that incurs both area and power. The NTF and Loop Transfer Function (LTF) are plotted in Fig. 5.3 and Fig. 5.4 respectively.

Fig. 5.2 PZ Plot of 4th Order Single Zero Optimized NTF

Fig. 5.3 Bode Plot of 4th Order Single Zero Optimized NTF

Fig. 5.4 Bode Plot of 4th Order Single Zero Optimized LTF

The introduction of zero optimization resulted in a nullification of quantization noise at around 22 kHz. The two origin zeroes provided stronger noise shaping effect when approaching DC. This reduces the integrated noise level within the signal bandwidth to

a sufficiently low level as compared to the thermal noise contribution by the opamp-RC input integrating resistors. With the input resistors design to $150\text{k}\Omega$, the quantization noise is well attenuated to 10dB below the thermal noise at the frequency of 1kHz. Frequency below this is dominated by flicker noise contributed by the active OTA.

5.2.1 Non-Return to Zero (NRZ) Versus Return to Zero (RZ) Feedback

The main feedback path has to be highly linear for our application to prevent distortion or harmonic tones from generating at the output bitstream. Besides the first integrator which will be discussed in the later section, the feedback protocol can also be a major contributor to distortions. In addition, the decision in the implemented feedback pulse shape can result in some trade-offs for consideration. The first issue is jitter sensitivity of a CT $\Delta\Sigma$ modulator. The continual integration of feedback charges implies that any discrepancies in timing clock edges can result in a wrong amount of charge being carried through the CTF. This is in contrast to a DT $\Delta\Sigma$ modulator whereby the charge integrated is not dependent on the clock edges. The second issue for consideration is Intersymbol Interference (ISI) that can lead to the generation of distortion related spurs at the output spectrum.

This phenomenon is a result of memory effects of the feedback pulse which generally is also attributed to the CT nature of the system. The two feedback pulse shapes considered in this work are the NRZ and the RZ schemes. Although there had been other feedback pulse shaping proposals for single bit designs to mitigate jitter sensitivity such as of a Switched Capacitive (SC) [7][8] feedback, they often penalizes

Fig. 5.5 Waveform of NRZ and RZ feedback pulses. NRZ pulse exhibit memory dependence on previous state while RZ shows a higher transition count

on power consumption as they typically places heavier requirements on the first integrator dynamic performance, not to mention the complexities involved in the generation of such feedback pulses. The NRZ and the RZ pulse shapes are shown in Fig. 5.5. Table 5.1 shows the comparison between these two feedback pulse shapes. In summary, NRZ feedback is more susceptible to ISI but slightly better off in jitter immunity as compared to RZ implementation. It should also be noted that RZ feedback constitutes heavier switching activities that requires a faster OTA, which implies that a higher GBW is required. To understand the reason behind the merits of the individual feedback scheme, it is imperative to take a closer look at the pulse shapes. The RZ pulses returns to zero integrating current in the latter half of every feedback cycle. As such, ISI becomes less prominent since the first integrator sees the similar distortion on every feedback cycle.

Hence, such an error in the feedback is therefore not signal dependent and hence do not result in distortions. On the other hand, the NRZ pulse holds its output should the preceding output feedback possesses the same value. As such, depending on what the

Non-Return-to-Zero (NRZ)	Return-to-Zero (RZ)
<p>Lesser transition count. This is because NRZ feedback allows a complete integration period.</p> <ul style="list-style-type: none"> • Less Susceptible to Clock Jitter 	<p>Higher transition count. This is because RZ allows only 0.5Ts integration period. If feedback is '1', the second integration cycle has to be returned to zero.</p> <ul style="list-style-type: none"> • More Susceptible to Clock Jitter
<p>NRZ feedback considers the entire integration period. Due to finite rise/fall times, the actual charge accumulated is dependent on the previous state, hence exhibiting a memory effect.</p> <ul style="list-style-type: none"> • More Susceptible to Intersymbol Interference (ISI) 	<p>RZ feedback considers only the first half of the integration cycle. When the feedback is '1', although there is finite risetime, the first integrator always receives a less than complete 'half' integration cycle. Hence, there is no memory effect.</p> <ul style="list-style-type: none"> • Less Susceptible to Intersymbol Interference (ISI)
<p>NRZ has the entire integration cycle. Hence, the feedback coefficient to ensure the targeted input dynamic range can be smaller. This relaxes the slew rate requirement on the first integrator.</p>	<p>RZ has 0.5 time integration cycle. The feedback coefficient c_1 is therefore two times as implemented in the NRZ scheme. This increases the slew rate requirement on the first integrator.</p>

Table 5.1 Table of comparison between features of NRZ and RZ Feedback schemes

previous feedback value is, the first integrator will be receiving a transition error that occurs when switching is required. Since it depends on the preceding feedback value, it can also be deemed as a memory effect. Such an error can result in the formation of output spurs. As for jitter immunity, a NRZ pulse is slightly better due to its reduced switching activity. However so, due to the single bit implementation, the jitter immunity for both RZ and NRZ are generally poor. This is due to the large voltage transition per unit quantizer step that causes large erroneous integrated charge when there are jittery fluctuations at the timing clock edges.

This work utilizes the RZ scheme for its ISI advantage. To relax the jitter performance short fall on the supply clock, a Jitter Immunity Enhancement (JIE) scheme is

implemented which will be discussed in section 5.2.3. With this, the only constrain will be on the first integrator opamp, which adopted a Class AB configuration to ensure sufficient gain while providing a high slew rate capability. Class AB amplifiers also has a better power efficiency due to a lower quiescent current consumption.

5.2.2 Coefficient Generation and Excess Loop Delay (ELD) Compensation

The filter coefficients are derived from the generated DT NTF. The architecture chosen is first decided to be of a CIFF configuration whereby the NTF for a 4th order zero optimized modulator is generated via the Delta Sigma Toolbox [6] as seen in (5.1). The Out of Band Gain (OOBG) is chosen to be 1.5 for this work. Subsequently, the LTF as shown in (5.2) is then derived. With this, ELD compensation is carried out. The ELD compensated in this work is 1Ts due to the high sensitivity to loop timing of a high order (4th Order) system. In addition, it is also necessary to provide ample time for the quantizer during small differential inputs. The implemented ELD is achieved with an auxiliary direct feedback as shown in Fig. 5.1 for simplicity since it is just a single bit feedback. From (5.2), 1Ts delay is removed by multiplying it with z. The remaining LTF_{ND} is given in (5.3).

$$H_{LTF}(z) = \frac{0.80465(z-0.8279)(z^2-1.79z+0.8345)}{(z^2-2z+1)(z^2-1.998z+1)} \quad (5.3)$$

This residual LTF_{ND} then has to be factorized to extract the direct feedback path coefficient, k required for the compensation. With the direct feedback, the impulse response for a delayed loop transfer function can be compensated at the sampling instances. This is represented by (5.4). (5.5) shows the CT transformed equation that

can then be mapped to the coefficients taking the compensated delay into account.

Prior to scaling, the direct feedback coefficient is evaluated to be $k=0.8046$.

$$LTF_{ND}(z) = k + \frac{1.1107z^3 - 2.9612z^2 + 2.6613z - 0.8046}{z^4 - 3.9983z^3 + 5.9966z^2 - 3.9983z + 1} \quad (5.4)$$

$$LTF_{ND}(s) = \frac{0.9476s^3 + 0.3056s^2 + 0.0618s + 0.0062}{s^4 + 0.0017s^2} \quad (5.5)$$

After comparing the coefficients of (5.5) with the CTF in S domain in a 4th order CIFF structure, poles and zeroes defining gain factors are evaluated to be as shown below:

$$\begin{array}{cccc} a1: 0.9476 & a2: 0.3058 & a3: 0.0602 & a4: 0.0056 \\ & b1: 1 & & \\ c1: 1 & c2: 1 & c3: 1 & c4: 1 \\ & g2: 0.0017 & & \\ & k: 0.8046 & & \end{array}$$

Modulator Coefficient Values Prior to Scaling

It should be noted that the above coefficient derivation is for a NRZ pulse feedback implementation. As such, since the RZ scheme reduces the integration time to only half the original ITs , to adopt the coefficients to a RZ feedback, the feedback coefficient, $c1$ has to be multiplied by a factor of two to make up the original integrated charge. In addition, these coefficients are still not scaled to the actual circuit integrators' output dynamic ranges. As such, a scaling procedure is required which will be discussed in section 5.2.6.

5.2.3 Jitter Immunity Enhancement

The single bit CT $\Delta\Sigma$ modulator is notorious for its susceptibility to clock jitter. For this reason, high resolution CT $\Delta\Sigma$ modulators require clock generators with excellent

jitter performance. Some designs relax this requirement by resorting to multibit structures. However, the linearity of multibit feedback DACs has to be maintained to prevent distortions. This increases the complexity of the design as well as increases the loop timing constraints when DEMs are inserted.

In most literature, the noise estimation is done by considering the feedback pulse jitter as additive noise sequence. The calculation of SNR boundary is achieved by assuming that the jitter induced noise dominates the performance. Applying the results and derivation from [9], the comparison between RZ and NRZ feedback is performed.

In general, the jitter bounded SNR is calculated as:

$$SNR_{jitter} = \frac{P_{\text{SIGNAL}}}{P_{\text{jitter}}} = \frac{A^2/2}{\sigma^2/OSR} \quad (5.6)$$

where σ^2 denotes the variance of a particular noise

For NRZ feedback pulses,

$$\sigma^2_{e|NRZ} = \sigma^2_{\Delta y|NRZ} \frac{\sigma^2_{\Delta t}}{T_s^2}, \text{ hence}$$

$$SNR_{jitter|NRZ} = \frac{P_{\text{SIGNAL}}}{P_{\text{jitter}}} = \frac{A^2/2}{\sigma^2_{e|NRZ}/OSR} = \frac{A^2 \cdot OSR \cdot T_s^2}{2\sigma^2_{\Delta y|NRZ} \cdot \sigma^2_{\Delta t}} \quad (5.7)$$

where $\sigma^2_{\Delta y|NRZ}$ is the standard deviation of the adjacent output difference, and $\sigma^2_{\Delta t}$ is the standard deviation of the clock jitter.

For RZ feedback pulses,

$$\sigma^2_{e|RZ} = 2\sigma^2_{y|RZ} \frac{\sigma^2_{\Delta t}}{T_s^2}, \text{ hence}$$

$$SNR_{jitter|RZ} = \frac{P_{SIGNAL}}{P_{jitter}} = \frac{A^2/2}{\sigma_{e|RZ}^2 / OSR} = \frac{A^2 \cdot OSR \cdot T_s^2}{4\sigma_{\Delta y|NRZ}^2 \cdot \sigma_{\Delta t}^2} \quad (5.7)$$

Where $\sigma_{y|RZ}^2$ is the standard deviation of the output sequence.

Thus, a comparison can be made as

$$\frac{SNR_{jitter|NRZ}}{SNR_{jitter|RZ}} = \frac{2\sigma_{y|RZ}^2}{\sigma_{\Delta y|NRZ}^2} \quad (5.9)$$

If the single bit quantizer is used, it is shown that the NRZ pulse shape is around 5dB better than RZ pulse shape in terms of jitter performance. The behavioural simulation showing the degradation in the Signal to Noise Ratio (SNR) with increasing jitter is illustrated in Fig. 5.6.

Fig. 5.6 Comparison showing degradation in SNR (Normalized to SNR without Jitter) with increasing Jitter for NRZ (Red) versus RZ (Blue)

At a clock frequency of 3.2MHz and a normalizing SNR of 100dB, it can be observed that at 31.25ps, the SNR achievable for NRZ and RZ feedback schemes is 85dB and 73dB respectively.

In this work, in order to attain 90dB SNR with sufficient design margin, utilizing the RZ feedback pulse shape, it can be read off that the jitter performance from the clock has to be better than 4.6ps. Since a clock with such a phase noise performance can be

hard to achieve, it is necessary for a jitter enhancement circuitry to be developed with the modulator.

Fig. 5.7 shows the jitter immunity enhancement circuit similar to that proposed in [10]. A resistive ladder is used to generate two reference voltages, V_{ref1} and V_{ref2} . A feedback configured OTA is used to generate a charging current that charges the capacitor that is connected on the other end to VSS.

As such, a second threshold V_{ref2} is used to time the capacitor charging time, hence creating a window insensitive to clock jitter that starts upon the modulator rising clock edge and stops when charging reaches V_{ref2} . With the OTA feedback resistor set to $50k\Omega$, the integrating capacitor is chosen to be $1pF$ while V_{ref1} and V_{ref2} are both designed at $400mV$. The charging current can therefore be determined to be $8\mu A$. To achieve jitter immunity, this enhancement circuit should possess good noise performance. The charging current charges the capacitor to $400mV$ in a period of $134.07ns$. For the OTA, high frequency white noise is averaged and attenuated through the charging cycle. The low frequency flicker noise on the other hand can be reduced through chopper stabilization that alternates every charging cycle. Assuming the OTA noise contribution is minimal, with $<5ps$ jitter limit, the noise contribution from the high speed comparator has to be limited to rms noise of $< 9.6 \mu V / \sqrt{Hz}$. This is achieved with a low noise low offset auto zeroed comparator. With this circuit, the immunity to jitter is greatly improved. In Fig. 5.8, it can be observed that the SNR achieved is $90.5dB$ and $86dB$ with a period jitter of $50ps$ and $100ps$ respectively, which is more than 10 times less stringent on the clock phase noise performance. However, it can be noted that despite the JIE circuitry, the SNR only slows down the jitter degradation. This is generic to a high order modulator whereby the sampling at the quantizer frontend is more sensitive to jitter fluctuations as compared to its lower

order counterparts. This causes the RZ fixed “ON” jitter immunity enhancement to be less effective as compared to utilization on a lower order structure. To understand this, let us examine the problem more closely. The fixed time ‘ON’ jitter immunity enhancement took care of the feedback charge fluctuation. Assuming the JIE circuitry is perfect, the period to period feedback charge will be independent from clock edge jitter.

However, the jitter noise leaks into the 4th order filter since the sampling clock is also jittery. One may argue that at this point, a 4th order filter should provide sufficient noise shaping to attenuate any degradation to be negligible. However, because of the fixed tuned ‘ON’ RZ feedback, the modulator loses the information on feedback

M1p M2p	20 μ /1 μ	M12 M13	12 μ /0.4 μ
M8 M9	8 μ /4 μ	Rref	400k
M6 M7	4 μ /0.4 μ	Cref	1pF
M3p	12 μ /3 μ	RL1	210k
M4 M5	4 μ /3 μ	RL2	240k
M10 M11	12 μ /4 μ	RL3	550k

Fig. 5.7 Jitter Immunity Enhancement (JIE) Circuitry whereby the output controls the RZ clock edge

charge variations. As a result of this, the jitter noise can leak into the filter hence rendering the jitter immunity circuit less efficient with increasing filter order.

Fig. 5.8 Simulated SNR comparison plot with and without JIE turned ON

5.2.4 Architectural Design Consideration

To implement the 4th order CT $\Delta\Sigma$ modulator while trading off between performance and power consumption, the final overall architecture is improved from Fig. 5.9. The filter for the modulator is compacted and shown in Fig. 5.10 which targets to conserve power as well as minimizes implementation complexities. This is possible because of the usage of gmC transconductance integrators which will be discussed more in depth in this Section.

The first integrator dictates the final modulator performance. As such, the Opamp RC integrator structure is chosen for its high linearity. The noise contribution for the opamp RC integrator can be mathematically expressed as (5.10), [11]. The first term is the thermal noise coming from the input R_{in} and feedback R_{fb} resistors. The second and third term originates from the thermal and 1/f noise respectively. It can be observed that the resistances in front of the opamp contribute directly to the noise of the CT $\Delta\Sigma$ modulator without any attenuation. This thermal noise will be manifested as noise

floor within the inband region, putting a limit to the maximum performance achievable. This is especially true for a CT $\Delta\Sigma$ modulator with a high OSR. This is because the quantization error level will be very low and thermal noise becomes the dominant performance

Fig. 5.9 Primitive 4th order CIFF Architecture with 1st opamp-RC Integrator and subsequent gmC 2nd-4th Integrators

Fig. 5.10 Proposed Condensed Filter Architecture with resource sharing to optimize power and area

$$v_{noise}^2 = 16KTf_B(R_{in} + R_{fb}) + \frac{128KTf_B n_{e,th}}{3g_{m,OTA}} + \frac{8Kf n_{e,th}}{C_{ox}^2 WL} \ln\left(\frac{f_B}{f_\mu}\right) \quad (5.10)$$

Fig. 5.11 Basic Structure of a gmC cell showing current flow

limitation factor. As observed in Fig. 5.10, the feed forward is implemented with the conventional feedforward capacitors C_{ffa1p} and C_{ffa1n} . The input resistance is chosen to be at $150k\Omega$, which places the thermal noise to be 10dB above the quantization noise level. The circuit design for the class AB OTA is discussed in Section 5.3.1. The subsequent integrators are implemented with gmC transconductance cells. They are chosen for a number of reasons. Firstly, the transconductance gmC cells can easily be shared to minimize on power consumption in the realization of the many coefficients in a 4th order structure. The architectural evolution can be seen to advance from Fig. 5.9 to Fig. 5.10. To share the gmC cell, an extra pair of outputs can easily be added to the output branch. A simplified gmC cell is shown in Fig. 5.11. With such a strategy, the numbers of gmC cells are reduced from 8 to 3. Not only is this beneficial to the power efficiency of the modulator but also implies a big reduction in area necessary for implementation. Secondly, the gmC cells are in general open loop structures that resulted in their energy efficiencies. As depicted in Fig. 5.11, each integrator function required for each modulator order can easily be realised by a voltage to current conversion through the degeneration resistor followed by integration into the output capacitors conveniently without the need for a feedback route. Thirdly, from the

system level perspective, the input loading capacitors of the quantizer can be absorbed into the output gmC capacitance easily. In conventional architectures, the input capacitance to the quantizers typically adds delay to the modulator filter output when the last integrator used is typically of an opamp-RC structure, hence slowing the loop response and compromises on stability. These input capacitances are also one of the challenges faced in high speed high bandwidth modulators. By taking into account of the input capacitance to the quantizer in the sizing of the last gmC integrating capacitors, the input capacitance of the quantizers can virtually be removed. This also implies that no extra power is required to boost the last opamp GBW and slew rate that drives the quantizer inputs. Lastly, it is also important to note that in the gmC implementation as compared to conventional opamp-RC integrators, the feedforward branches present a much lesser loading to integrators outputs. This is because the output of gmC cells can be exploited for its versatility and the feedforward branches are therefore implemented in current mode. This helps to optimize the power consumption of the filter by relaxing on the performance requirement of the active OTAs.

5.2.5 Process Variation Tolerance

The CT $\Delta\Sigma$ modulator suffers from process variation in contrast to its DT counterpart due to the usage of physical resistors and capacitors to form the integrating $(F_s * k_i)/s$ function. The DT $\Delta\Sigma$ modulator on the other hand governs its integration function with a charge transfer between two capacitors, rendering it insensitive to process corner variations due to the superior matching characteristics between capacitors. To illustrate the impact of process variation on the performance of the CT $\Delta\Sigma$ modulator, the

integration constant is varied individually for each integrator to observe the impact on the SNR of the modulator. Fig. 5.12 shows the changes in SNR when the integration constant RC changes between $\pm 30\%$ in the first, second, third and fourth integrators respectively. It can be clearly seen that process variation in the first integrator affects the performance the most. The fourth integrator is least sensitive to process variations. This is reasonable since the forward filter gain attenuates the non-idealities originating from the later stages. It is also observed that the modulator performance is much worse off affected on one side (-30%) of the process variation, i.e., when there is a reduction in device resistance or capacitance. In technological terms, the modulator will therefore be expected to perform worse off at FF (Fast) Corners if calibration is not performed. Design consideration can therefore be made to oversize the integrating resistors and capacitors so maintain performance under the worst case shift during fast corners. However, this is not favored if power optimization is of concern. This is because the increased loading at the output of integrators warrant higher slew rate and bandwidth requirements when opamp RC are utilized at nominal and slower corners.

To maintain the SNR of the modulator above 90dB, it is essential to control the integration constant $R_{int1}C_{int1}$ process variation to be larger than -2% variations. To ensure that, a Process Variation Tolerance Enhancement (PVTE) Circuitry is proposed to ensure robustness against process corner variations in the integration constant. In this work the process variation tolerance is achieved via a one-time calibration of the R_iC_i integration constant. To save area, it is assumed that there are minimal local mismatches and that our technique primarily tunes the global process variation tolerance only. Since the first integrator is the most crucial to the overall modulator performance, the capacitor and resistor in the tuning circuitry as shown in Fig. 5.13, is placed within the first R_I and C_I to allow matching optimization.

The proposed tuning circuitry to enhance process tolerance is shown in Fig. 5.13. This circuit generates a process dependent frequency that is monitor off-chip via a pin. Should there be process variation such that the integration constant $R_i C_i$ is changed, the frequency detected will be shifted away from the target frequency.

Fig. 5.12 Modulator SNR performance (dB) with process shift (%) applied to important integrating Resistors and Capacitors individually to Integrator 1 (Blue); Integrator 2(Orange); Integrator 3(Grey) and Integrator 4 (Yellow)

In contrast to the jitter immunity enhancement circuitry, the adapted structure to curb process variation has to perform integration of a replica C_{int} , in both directions, depending on the two comparators. This circuit is activated by first setting $PVTE_{en}$ to '1'. Conversely, when the tuning is completed, the tuning circuitry can be shut down by simply setting $PVTE_{en}$ to '0'. When this happens, the capacitor C_{int} will be completely discharged and the output of both the comparators will be '0'. When $PVTE_{en}$ is initiated to '1', the tuning protocol begins. The signal $chrg_status$ will switch to '1' and this causes both swa_p and swa_n to be set to '0'. As such, the PMOS M11 and M13 will start charging the node cap_int . This will continue until both comparator output turns '1'. This happens when cap_int is above 800mV. When

this occurs, *charg_status* becomes '1' and the multiplexer will start to monitor the output from the lower comparator. At the same time, the switching of *charg_status* to '1' will cause discharging of *cap_int* to begin via the NMOS M16 and M18 sinking path. The multiplexer will change side only when both Comp1 and Comp2 outputs turn '0', indicating that *int_cap* is below 400mV. This process cycles itself until *PVTE_en* is set back to '0'. The charging and discharging current magnitude is given in (5.11).

$$I_{ch/disch} = 0.5V_{ref1}/R_{int} \quad (5.11)$$

In order to ensure both the input and feedback integration paths are taken care of, the feedback configured amplifier also provides the current responsible for the modulator single bit DAC feedback. The up/down integration time governing the tuning circuit in Fig. 5.13 is given as follows in (5.12).

$$T_{int,UP/DOWN} = \frac{(V_{ref2H}-V_{ref2L})C_{int}}{0.5V_{ref1}/R_{int}} \quad (5.12)$$

Since the charging and discharging themselves are alternating, the period of the generated square pulse is given as in (5.13).

$$F_{sq} = \frac{1}{2*T_{int,UP/DOWN}} = \frac{1}{2*R_{int}C_{int}} \quad (5.13)$$

When there is process variation that changes the integration constant, a corresponding change in $T_{int,UP/DOWN}$ and consequentially a shift in F_{sq} will occur. In this work, the actual tuning is done by making the integrating capacitors tunable.

There are several design considerations that may otherwise affect the performance of the tuning circuitry. Firstly, it should be mentioned that the thermal and active noise

from R_{int} and the OTA respectively is averaged with the charge accumulation cycle together with the large oversampling when acquiring the frequency of the square wave. By taking a large number of cycles, high frequency noise can thus be attenuated. However, the offset in the amplifier can result in DC static error. Together with this, there are also static offsets that may originate from the two comparators. As such, such DC offsets are mitigated via a two times frequency acquisition procedure. The inputs of the OTA and comparators are designed to be chopped in a static manner. A first frequency measurement is obtained with the amplifiers and comparators set to positive polarity. Subsequently, a second frequency will be obtained with the amplifiers and comparators toggled to the negative polarity. As such, the final frequency of the square wave will be the average of the two obtained frequencies. The process dependent resistors and capacitors are cancelled as a result of this circuit. This reduces the process variation to around 2% if layout matching is taken into consideration during implementation. In this work, the second to the fourth integrators has provision for manual tuning of the output integration capacitors that are controlled by externally controlled bits too. However, only global process variations are taken into account here. Since there is only one process tracking circuitry on chip, the local statistical mismatches can result in some residual tuning errors. As such, the matching considerations can only be optimized at the first integrator. This is still acceptable as the forward gain in the first integrator is sufficiently large to keep the effect of statistical mismatches to be negligible for the second integrator, whereby the impact of mismatch-related residual error diminishes down the filter. Fig. 5.14 shows the SNR plot of the CT $\Delta\Sigma$ modulator with process variation applied to all the integrators.

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Fig. 5.14 Modulator Performance SNR (dB) with Process Variation (%) when process parameters for all Integrators are varied together

5.2.6 Scaling Coefficients

The coefficients generation as discussed in section 5.2.2 is not bounded by the integrators' output dynamic range. In other words, direct implementation with coefficients straight out of the discussed generation procedure will result in saturation at the integrator outputs. In order to prevent that from happening, the coefficients should be scaled systematically to the desired operating voltages. The scaling procedure begins at the first integrator. Fig. 5.15 shows the MATLAB model, whereby the first integrator single ended output swing is scaled to $0.8V_{DD}$ at the maximum differential peak to peak input of 2V.

The output of the first integrator should be optimized for two reasons. Firstly, the first integrator provides attenuation to input referred non-idealities. To capitalise on this effect, the forward gain for the first integrator should be maximized to relax design requirements beyond the first integrator to improve power efficiency. Secondly, a large integrated output from the first integrator creates a compounded effect on the scaling considerations of integrators cascaded down the CT filter. When the gain of the first integrator is maximized, the second integrator can be scaled for lower power consumption with larger capacitors at the

same noise performance due a better input referred attenuation. As for the second and third transconductor gmC cells, the basic underlying scaling consideration lies in keeping the output integrator swing within the maximum output dynamic range. The scaling sequence begins in the first integrator and concludes when the last integrator output fits into the quantizer input dynamic range, which is the targeted MSA. The voltage swing at the output of each integrator is illustrated in Fig. 5.32. After scaling, the modulator coefficients are derived to be as shown below. The last integrator output has to be scaled to the designated input dynamic range of the quantizer which will be discussed in detail in section 5.3.4. This is because the input capacitance of the quantizer is input voltage dependent and the variation should be kept minimal to maintain the filter linearity. In addition, since the MSA primarily determines the maximum overall modulator dynamic range, it is necessary to optimize quantizer dynamic range to meet overall application system level requirements. As such, after scaling, the modulator coefficients are as listed below:

Fig. 5.15 Model used for Scaling Coefficients where the scaling of the 1st integrator is used as an example

a1: 0.4738	a2: 1.018667	a3: 0.4816	a4: 0.448
	b1: 0.4		
c1: 0.621566	c2: 0.15	c3: 0.416667	c4: 0.1
	g2: 0.017		
	k: 0.10728		

Modulator Coefficient Values After Scaling

5.3 Circuit Implementation Considerations

The design of the 4th order CIFF CT $\Delta\Sigma$ modulator includes the realization of the following circuit blocks whose functionalities, power consumption and area occupied are summarized in Table 5.2. The overall top level block diagram is shown in Fig. 5.16.

5.3.1 First Integrator (OTA RC)

The schematic of the OTA in the first integrator is shown in Fig. 5.17. To keep quiescent power consumption down, a minimum selector M14-23 is included for each channel. During low input signal idling mode, the current biasing the output transistors will be limited to a minimal quiescent current, I_q . It can be seen that the PMOS sourcing transistors M24/M26 conducts only when output charging is required. On the contrary, during output sinking, M25/M27 will be responsible for conduction. Otherwise, the respective output drivers will only carry the minimal quiescent current. The operation of the minimum selector is as follows. The regulation for minimal quiescent current conduction through the output transistors is done solely via the PMOS drivers M24/M26. M14/15 and M22/23 are the current sensors for the PMOS and NMOS output drivers respectively. M19/M21 is sized to have the same V_{gs} with M14/M15 during idling condition, which causes the current mirrors

Functional blocks	Circuit Architecture	Power Consumption (μA)	Area Occupied (μm^2)
First Integrator	OTA RC	53	22500
Second Integrator	gmC	25	5625
Third Integrator	gmC	15	5200
Fourth Integrator	gmC	12	5890
Main DAC	1b Current Steering	10	240
Auxiliary DAC	1b Current Steering	4	200
Quantizer	1b Comparator	12	1620
Jitter Enhancement	OTA & AZ comparator	20	11500
Biasing	Current Mirrors	2	180
Process Variation Tolerant Enhancement	OTA & Comparators	32 (Not Consuming during Actual Operation)	22200

Table 5.2 Summary of functional blocks within the 4th order CIFF CT $\Delta\Sigma$ modulator

to have a ratio of 0.5 into the current branch M15/M17/M20. In other words, the transistors M18/M20 are biased at the corner between linear and saturation operation region during zero load condition. During high sourcing condition, M24/M26 will experience high current flow, increasing its V_{gs} correspondingly. As such, the current mirrors M18-M21 function as per normal since M18/M20 biased in saturation. With this, current sensing on the idling drivers M25/M27 is done by M22/M23, which through M4-7/M10-13 configured in a negative feedback, regulates M24/M26 to ensure that only I_q is flowing. On the other hand, during high sinking condition, M25/M27 are active and the quiescent current sensing is therefore performed by M14/M15. However, in contrast to high sourcing condition, M18/M20 are now operating in their linear region, acting like resistors due to low current conduction through M24/M26. With this, regulation is achieved by modulation of the on resistance of M18/M20. The common mode feedback circuitry is similar to OTA1 whereby a feedback from the

Fig. 5.16 Proposed 4th Order CIFF Continuous-Time $\Delta\Sigma$ Modulator Model with Shared resources and low gain Preamplifier

output is loop back to control the V_{gs} of M8/M9. As discussed for OTA1, the CMFB is frequency stabilized together with the differential mode compensation. The first OTA is designed with a Class AB structure. The class AB structure consumes low quiescent current while providing a fast slew performance. The Unity Gain Bandwidth (UGBW) is designed at $2Fs$. Fig. 5.18 shows the degradation in SNR with the OTA UGBW. In order to maintain a SNR of more than 90dB, a GBW of $2Fs$ is sufficiently large enough. The Class AB OTA structure used here is similar to the one used in Section 6.5 with a minimum selector to achieve low quiescent current consumption. The detailed transistor level design considerations are elaborated in that chapter. With the power scaled down, the Class AB OTA achieved a UGBW of 6.9MHz with 82.4dB gain while having a current consumption of 53 μ A. The bode plot is shown in Fig. 5.19 indicating a phase margin of 78 degrees. The coefficients governing the first integrator b1 and c1 post scaling is determined in section 5.2.6 to be 0.4 and 0.622 respectively. The value of c1 is more than that of b1 due to the RZ scheme chosen; which only has $T_s/2$ integration period. In addition, the coefficient C1 also takes into account of the JIE compensation and supply normalization at the quantizer. For a target of

90dB, based on (5.10), the integrating resistor R_{int1} can be designed to be at 150k Ω . With this, the corresponding integrating capacitor C_{int1} can be calculated to be 5.21pF. This forms the primary loading capacitor on the output of the Class AB OTA1 that has to be driven. With this design, the modulator will be thermal noise limited since the quantization noise will be lower than the resistive noise contribution.

M1 M2	100 μ /1 μ	M8 M9	24 μ /6 μ	M16 M17	2 μ /6 μ	M24 M26	40 μ /0.4 μ	M32 M33	6 μ /2 μ
M3	36 μ /2 μ	M10 M11	3 μ /2 μ	M18 M20	20 μ /0.4 μ	M25 M27	16 μ /0.4 μ	M34 M35	16 μ /6 μ
M4 M5	2 μ /0.4 μ	M12 M13	3 μ /2 μ	M19 M21	20 μ /0.4 μ	M28 M29	6 μ /1 μ	C ₁ C ₂	2.5pF
M6 M7	2 μ /0.4 μ	M14 M15	20 μ /0.4 μ	M22 M23	8 μ /1 μ	M30 M31	6 μ /1 μ	C ₃ C ₄	2.5pF

Fig. 5.17 Fully Differential Opamp with Class AB output stage for First Integrator

Fig. 5.18 Plot of Modulator Performance SNR (dB) with 1st opamp-RC OTA gain bandwidth in multiples of F_s

5.3.2 Second to Fourth Transconductor gmC

The transconductor gmC structures are used for the second to the fourth integrators in this work. They are utilized for their open loop characteristics with the versatility for multiplexing to provide multiple outputs with the same differential input signals. The base structure for the gmC cells is shown in Fig. 5.20. It shows a poly resistor R_{int} used for inherent linearity. In commercial ICs, such resistors (R_{int}) when used in high precision sensors are typically post silicon laser trimmed to remove any process related variations. For this work, since we do not have the provision for such sophisticated post silicon trimming, a shared PVTE Circuitry

Fig. 5.19 Bode Plot of implemented Class AB OTA used for 1st opamp-RC integrator

Fig. 5.20 Basic gmC cell showing Common Mode Feedback utilize in Transconductor cells 3 & 4

as shown in Fig. 5.13 is utilized. However, due to the CT nature of the second to the fourth integrators for both their inputs and outputs, the $R_n C_n$ integration constant has to be hand tuned. The trimming protocol for process variation mitigation is discussed in section 5.2.5. This section will be focusing primarily on the transistor circuit design considerations. Fig. 5.21 shows the slight modification to the basic gmC structure for better linearity that is used for Integrator 2 whereby there is only one prior stage for input-referred attenuation of non-idealities such as non-linearities. When the input differential voltage is applied, the current flowing through R_{int} should not be drained into the input differential pairs themselves, which will otherwise modulate the V_{gs} of the MOSFETs.

In contrast, the current is drained into an alternative path provided by M3/M4. In the basic structure shown in Fig. 5.20, M3/M4 is configured in a common source configuration to provide a gain that under negative feedback minimizes the current flowing into the input differential pair. This is achieved by keeping the drain voltage of M1/M2 to be relatively constant. For instance, when the gate voltages of M3/M4 (i.e. Drain Voltage of M1/M2) has the tendency to upshift, M3/M4 will sink in more current flowing across R_{int} to ensure that it

M1 M2	2μ/2μ	R _{int}	966kΩ
M3 M4	2μ/1μ	C _{int}	1pF
M5 M6	2μ/1μ	V _{bias}	1V
M7 M8	4μ/2μ	V _{cm}	1.6V

Fig. 5.21 Second Transconductor Cell with Linearity Boosting OTAs and W/L Ratio

does not happen. M3/M4 then mirrors both its common mode DC current and differential mode current to the output branches (M5-M12). The common mode feedback circuitry is implemented with a 3 input OTA, this OTA takes the average of the differential output voltages for comparison with an input reference voltage, v_{cm} . The output of this OTA then regulates the PMOS current sources (M7-M10). With this common mode feedback, the common mode DC current will not be flowing out, leaving only the differential current flowing through R_{int} being brought to the output to charge the capacitors. Having said that, it should also be noted that the I_{ds} equation shown in (5.14) is also in second order affected by channel length modulation as modelled by the second term involving V_{ds} . Therefore, while V_d of N1/N2 can be maintained unchanged with a negative feedback configured OTA, their V_{ds} can still be changing with the input signal. As such, this change in V_{ds} can modulate in the second order the current that may still be flowing into N1/N2.

$$I_{sd,N1/N2} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right) (V_{sg,M1/M2} - V_{th})^2 (1 - \lambda V_{sd,M1/M2}) \quad (5.14)$$

To minimize this, since λ is proportional to $1/L_{M1/M2}$, it is imperative to maximise the length of M1/M2 to minimize this effect. On the other hand, the more influential component is attributed to the finite input impedance seen by the integrating current into the source of N1/N2. In the basic gmC structure that is utilized in integrators 3 and 4, this input impedance is increased by a factor of approximately $g_m \left[\left(R_{int}/2 \right) \parallel (R_{out,M3/M4}) \right]$ given by the gain of the common source configured M3/M4. As such, when the coefficient for the particular integrator is small, the resistor R_{int} will be large and hence resulting in a better overall linearity. Therefore, it can be inferred that in a transconductor based modulator, the modulator linearity can be quite dependent on a proper and strategic scaling of the coefficients.

To improve on the linearity of the second integrator in view of the above discussed considerations, two single stage auxiliary amplifiers are added to boost the local negative feedback gain. This greatly increases the impedance seen into the source of M1/M2, hence channeling the integrating current primarily into N3/N4. In other words, with the inclusion of the auxiliary amplifiers, the minimum coefficient value to maintain the linearity to satisfy the modulator Signal to Noise and Distortion Ratio (SNDR) can be larger. In addition, the DC biasing current for the gmC cell can also be optimized smaller, hence saving power.

Another shortcoming that may affect the performance of the gmC integrator is in the mirroring of the current to the output integrating capacitors. There are two components to achieving proper current replication. Firstly, cascoding is applied to minimize systematic mismatches as a result of channel length modulation. In addition, the local statistical mismatches can be mitigated by applying Dynamic Element Matching (DEM) rotation to the current mirrors which is not implemented in this design.

5.3.3 Main and Auxiliary DACs

The two DACs utilized in this work are single bit current steering DAC. However, there are several design considerations especially in the main DAC. Since the errors in the main DAC are not shaped by the overall modulator NTF, they have to be much more optimized to achieve the targeted performance. Before discussing in detail on the implementation issues, the properties of a single bit DAC is briefly discussed.

The main feedback DAC's linearity is very important to the overall performance of the modulator since it is directly used by the first integrator. As such, there is no way that the integrator is able to distinguish if any non-idealities received are from the DAC or the modulator input signals themselves. One main advantage of using the single bit DAC feedback is its property of inherent linearity. In contrast to multibit DACs, the output from a single bit DAC is either '1' or '0'. As such, from the system's perspective, the transfer function of the DAC can only suffer from a gain or offset error that may result from a shift in the feedback current of the current steering architecture in this work but are in general rather immune to non-linearity issues. This is typically true for the design of moderately high SNR modulators whereby second order effects including the harmonic distortion related frequency spikes are often buried beneath the noise floor of the PSD plot. Fig. 5.22 shows the transfer characteristics of the single bit DAC.

However, in higher order modulators targeting high SNR, some imperfections to circuit design might contribute, though second order in nature, to signal dependent error, which eventually lead to distortions. Such errors manifest themselves when high resolution is needed and therefore surfaced as frequency distortion peaks when the noise floor is lower. One such potential issue is the finite output impedance of the current cell, typically provided by a tail current MOSFET as shown in Fig. 5.23. The current source becomes modulated with

the MOSFET V_{ds} variation, hence resulting in even harmonic distortions. This issue is also one of the reasons why an opamp-RC structure is chosen as the modulator's first integrator.

In order to ensure that the current output from sourcing output MOSFETs are not varying with the input signal, it is important to ensure that the channel length modulation effect is negligible. To model this finite output impedance, a resistor R_{leak} is connected in parallel to the output sourcing transistor as shown in Fig. 5.23.

Fig. 5.22 Feedback Current with targeted input dynamic range of differential pk-pk of 2V and compensated for Jitter

Fig. 5.23 Unit Current DAC showing finite output current source impedance and first Integrator configuration

The summing nodes to the first integrator are generally much attenuated as a result of the large gain provided by the Class AB opamp as discussed in section 5.3.1. With a gain of approximately 80dB, the single-ended scaled amplitude of first integrator output voltage swing of 500mV translates to a transient voltage fluctuation of around 50uV amplitude at the summing inputs. To work out a rough estimation, let's consider the -90dB input signal magnitude for the single ended Full Scale (FS) amplitude of 500mV.

The -90dB input signal is given as: $0.5 * 10^{-90/20} = 15.8\mu V$

As an estimate, this indicates that a -90dB input signal can be as low as 15.8μV in amplitude when presented at the modulator inputs due to the OTA gain. Hence, by doing a ratiometric comparison, the output impedance of the current cell required can be calculated

$$\text{as } \frac{50\mu V}{15.8\mu V / 150000} = 474.7k\Omega.$$

Hence, as can be seen, in order to achieve a distortion lower than the Signal to Quantization Noise (SQNR) floor, the output impedance of the current cell has to be very high. As such, this is not possible to achieve with just a simple lengthening of the output sourcing MOSFET. In this work, regulated cascodes are employed (Not shown in Fig. 5.23) to increase the output impedance of the PMOS current source. To increase the output impedance further, one can even insert OTAs configured in negative feedbacks. It can be seen in Fig. 5.23 that additional auxiliary OTAs are included to enhance the common mode output impedance. This is necessary to provide regulation to match the sourcing and sinking current, which may cause large voltage transients that will limit the dynamic range. The auxiliary OTA also improves the Common Mode Rejection Ratio (CMRR).

Otherwise, common mode fluctuations can result in differential signal distortions in the presence of circuit mismatches of R_{int} for example. Care should be taken to not oversize the output transistor too much as it may cause frequency dependent effects which are essentially

a result of a large coupling capacitance associated with large transistor dimensions. The auxiliary DAC is embedded within the modulator and its second order effects are sufficiently attenuated both by the modulator noise shaping effects as well as the high CTF forward gain provided by the preceding integrator stages.

5.3.4 Quantizer Design

This section discusses the design of the single bit quantizer. Before analysing the circuit design, it is worthwhile discussing the interface from the output of the CTF to the quantizer input, of which some design considerations were taken which resulted in some power optimization. The simplified overall block level diagram including the CTF output transition to the quantizer input is shown in Fig. 5.24. This work utilizes a dual stage quantizer that consists of an input preamp and a second latch. The final integrating capacitors are shared among all feed forward, last integrator output and Excess Loop Delay (ELD) direct feedback path. This implementation is similar to [12] but is more area and power efficient due to the gmC implementation.

In [12], all the integrators are design with opamp-RC architectures. As such, the feedforward coefficients have to be implemented with additional feedforward capacitors to the last Voltage-to-Current (V/I) outputs. In contrast, this work capitalizes on the versatility of the gmC integrator output. Each transconductor cell can function as a gmC integrator or simply a V/I converter (i.e. transconductance cell). Hence, the feedforward capacitors for the second to fourth integrators can be omitted, hence saving area. In addition, since only the integrating capacitors are loading on the gm cell outputs, the power consumption can be much more optimized as compared to a opamp RC implementation whereby each pair of integrator outputs are loaded with both the integrating and feedforward capacitors. There are no dedicated sampling capacitors for the quantizer. Instead, the capacitors holding the charges

for the last integrator are also shared and used to maintain the input voltage to the single bit quantizer. This is beneficial to the system architectural implementation for the following reasons. Firstly, there is no need for a last V/I conversion [12] before the quantizer. The inclusion of a last V/I conversion consumes both extra area and power. In addition, the

Fig. 5.24 Overall Modulator Structure showing interfacing considerations such as Parasitic Input Capacitance to Preamp and Output Impedance of CTF that can affect kickback performance

quantizer has to be designed in the current mode if a V/I conversion is used. Secondly, the parasitic capacitance of the preamp input device can be absorbed into the last pair of integrating capacitors. As such, the preamp inputs can be size relatively larger to enjoy better matching property without loading explicitly onto the integrator outputs.

Although the parasitic capacitance to the input pair of the preamp can be designed with the last integrating capacitances, care should be taken as they are classified as MOSFET capacitors. MOSFET capacitors have capacitances that are known to vary with their biasing voltages, primarily sub-divided into three major operating regions. Fig. 5.25 shows the typical characteristics of a MOSFET capacitor. In order to minimize the capacitance variation effect caused by the biasing conditions, the comparator is designed with a cascading structure. The first stage consists of a low gain preamp. The gain of the first stage is established by a

differential input PMOS stage P1/P2 loaded with diode configured NMOS load N1/N2. The first stage output swing is minimized and linearized with source degeneration resistors RS1/RS2. With this structure, the quantizer input MOSFETs can be operating in the saturation region even when the input is at the maximum amplitudes of 500mV. This is the operating region with constant capacitance while having the maximum gm. As a result, the input capacitance fluctuation can be kept to the minimum, hence enhancing the linearity of the filter.

Fig. 5.25 Typical MOSFET Capacitor Variation with Changing V_{GS} with targeted region of operation highlighted in Yellow

To verify this, the input capacitance measured with AC simulation by placing series resistors on the gate, whereby the -3dB cutoff is determined at both inputs during extreme voltage swings. After obtaining the -3dB cutoff frequency, the parasitic capacitances C_{gs} can be back-calculated knowing the inserted series resistor values. Fig. 5.26 shows the schematic of the proposed comparator structure and Fig. 5.27 the input capacitance variation with comparator differential input voltage. It can be observed that the targeted input dynamic range of $\pm 500\text{mV}$ shows only very minor variation in capacitance. The absolute contribution in

capacitance is also relatively low at 2fF. As V_{gs} increases on both the positive and negative end of $\pm 1V$, the input capacitance can vary up to 20fF, which can restrict the minimum output integrating capacitor values. The inclusion of the preamp also reduces the impact of kickbacks from the subsequent high gain stages as shown in Fig. 5.28. To emulate the output impedance of the gmC cell, the series gate resistors are increased to typical output gmC resistance values of around 500k Ω with the

M1 M2	4 μ /1 μ	M9 M10	4 μ /0.4 μ	M17 M18	4 μ /0.4 μ	M23 M26	1 μ /0.4 μ
M3 M4	8 μ /0.4 μ	M11 M12	12 μ /0.4 μ	M19 M20	0.8 μ /3.6 μ	M24 M25	6.4 μ /0.4 μ
M5 M6	4 μ /0.4 μ	M13 M14	1.6 μ /1 μ	M21 M22	4 μ /0.4 μ	M27 M28	6.4 μ /0.4 μ
M7 M8	0.9 μ /2 μ	M15 M16	4 μ /0.4 μ	RL1 RL2	80k Ω	M29	6.4 μ /0.4 μ

Fig. 5.26 Proposed Comparator with low gain Preamp and Latch

capacitive loading of 1pF on the differential lines. With this setting, the kickback is measured to an amplitude of 80uV, which will be sufficiently attenuated when input referred.

In multi-channel SoC, by isolating the switching noise to the quantizer, substrate coupling can be much better controlled. The gain of the comparator is progressively boosted with

cascaded common source configured output stages before passing the outputs to normal digital buffers. This is to avoid metastability, slow conversion and large shoot through currents when the input differential voltage to the comparator is small. The preamp is continuously turned on to avoid abrupt startup transients that will back propagate as kickbacks. In contrast, in order to save power, the cascaded stages are turned off and pulled to ground during idling. A conversion ready signal can be generated when comparison is completed, which is characterized by complementary outputs. Fig. 5.29 shows the simulated waveforms showing the delay in the comparator and the generation of the conversion ready signal via a XOR gate. This simulation is performed with a small input differential voltage of 1mV. The delay at with this input is 59ns, which is well within $0.5T_s$.

Fig. 5.27 Comparator Input Capacitance variation with Input Differential Voltage

Fig. 5.28 Kickback voltage at Comparator Inputs when loaded with 1pF and 500kΩ

Fig. 5.29 Simulated Comparator Output with 1mV Differential Input

5.4 Results Discussion

The performance of the modulator had been verified through extensive simulations. This section presents the results of the modulator at each phase of the modulator development stage. The software used to evaluate the performance of the modulator are MATLAB and Cadence SPECTRE during the system modelling and schematic design steps.

The MATLAB software is used to generate the NTF. The basic model shown in Fig. 5.30 is used to evaluate the PSD against the raw NTF plot with the proposed CIFF architecture. Fig. 5.31 shows the result of the PSD plot, which reveals the frequency notch at around 22 kHz indicating zero optimization. The only noise considered here is quantization noise. With this, the SQNR calculated is 100dB. This gives the PSD spectrum when the modulator is still not scaled. As such, this phase evaluates the implementation of the NTF with 4th order CIFF architecture. As observed, the CIFF structure produces a PSD plot that matches the potential of the targeted NTF. The integrator output signal swing levels are shown in Fig. 5.32. After

Fig. 5.30 Basic MATLAB Model Using in Coefficient Generation Verification

scaling, the output swing levels are plotted and overlaid onto the unscaled waveforms. It can be seen that they are clearly reduced to meet the realistic voltage dynamic range requirements in the actual circuit design. The scaling ratios for the single ended pk-pk swing of the four integrators are tabulated in Table 5.3.

The PSD of the scaled modulator in Fig. 5.31b is again re-confirmed to match the pre-scaled PSD in Fig. 5.31a to ensure the scaling procedure is correctly applied. It matches exactly to the PSD as plotted. From here on, the results shown are generated with CADENCE SPECTRE simulator that strongly emulates actual silicon performance. Upon the full design in the schematic level, the effectiveness of the Process Variation Tolerance Enhancement (PVTE) circuitry is studied. The modulator is simulated in nominal, fast and slow corners. For each corner, the frequency generator of the square pulse produced by PVTE circuit is tabulated in Table 5.4. Fig. 5.33a, b and c shows the PVTE output at nominal, fast and slow conditions respectively. The output frequency is determined by the integration rates which are essentially a function of the process variation in the integration constants. Referring to Fig. 5.13, with $V_{ref1}=400\text{mV}$; $R_{int}=200\text{k}\Omega$; $\Delta V_{ref}=(700\text{mV}-400\text{mV})=400\text{mV}$; $C_{int}=12\text{pF}$;

Fig. 5.31a PSD Plot of Pre-scaled CIFF Model (Top)
 Fig.5.31b PSD Plot of Post-scaled CIFF Model (Bottom)

Integrator	Scaling Factor, k (Normalized to Supply of 1.5V)
1	0.8
2	0.4
3	0.4
4	0.68

Table 5.3 Scaling Factor, k for each integrator

Fig. 5.32 DC Normalized Waveforms at the output of the four integrators overlaying both the unscaled and scaled

Let Q be the percentage change in targeted integration constant $R_{int} * C_{int} = 2.4 \times 10^{-6}$, then

$$Q(\%) = 100 * \left[\frac{V_{ref1}}{(4.8 \times 10^{-6}) * F_{meas} * \Delta V_{ref}} - 1 \right] \quad (5.15)$$

Process Corner	F_{meas} , Frequency Detected (Hz)	Q, Percentage Shift (%)
Nominal	204079.1335	2.08
Fast	341682.3532	-39.03
Slow	135875.7705	53.33

Table 5.4 Tabulated frequency output of the Process Variation Tolerant Enhancement Circuit.

It can be observed that the nominal process variation does not contribute to a significant coefficient change. The slow corner in particular can cause more than 50% shift. The nominal corner shows a shift of 2.08% from the targeted integration RC time constant value. However, this is due to the inaccuracies of the PVTE circuitry which is acceptable. After tuning the coefficients, the modulator is simulated at the various corners to study the effectiveness of the PVTE circuitry. The improvement in SNR before and after calibration is tabulated in Table 5.5.

Process Corner	Before Calibration SNR (dB)	Post Calibration SNR (dB)
Nominal	90.5	91.4
Slow	78.2	90.1
Fast	15.4	89.4

Table 5.5 Comparison of SNR simulated at 3 process corners before and after PVTE Calibration

The PVTE circuit is also evaluated under temperature variations. In these simulations, the temperature is swept from -40°C to 125°C . The output frequency of the PVTE pulse is obtained and plotted. Fig. 5.34, Fig. 5.35 and Fig. 5.36 shows the variation in output frequency with temperature for the nominal, fast and slow corners. Interestingly, the output frequency

Fig. 5.33a PVTE output signals cap_int and chrg_status under Nominal conditions at 25°C (Top)

Fig.5.33b PVTE output signals cap_int and chrg_status under Fast conditions at 125°C (Middle)

Fig.5.33c PVTE output signals cap_int and chrg_status under Slow conditions at -40°C (Bottom)

seems to be much less varying with temperature. This implies that the integration constant do not change much with temperature. As such, the integration constant only need to be tuned once during startup for corner compensation. Subsequently, the performance of the modulator under temperature variation should be maintained with respect to integration RC variations.

The Jitter Immunity Enhancement (JIE) circuitry is evaluated with injected jitter into the system in CADENCE. The clock signal generated from a VerilogA script has a frequency fluctuation of +/- 10% and symmetrical rise and fall time of 1ps. The period jitter can be provided via its property GUI. As an illustration, the FFT of the clock signal is performed with a jitter of 100ps and plotted in Fig. 5.37. It is overlaid on a similar FFT plot of a clock signal without jitter provided.

The enhancement in jitter performance is evaluated by simply plotting the PSD of the modulator output bitstream under the influence of a jittered clock. The modulator PSD comparison with JIE turned on and off is shown in Fig. 5.38 and 5.39 with the period jitter of the input clock source set to be at 50ps.

The noise floor when JIE is turned on clearly shows a much attenuated noise floor as compared to the PSD plot when JIE is off. It shows the effectiveness of the JIE circuitry at a period jitter of 50ps. The SNR with injected jitter plot is shown in Fig. 5.9. The 4th order CT $\Delta\Sigma$ modulator is simulated further for system evaluation. Fig.5.40a and Fig.5.40b shows the PSD of the modulator at high and low input amplitudes of -6.5dBFS and -67dBFS at a frequency of 6.25kHz. In Fig.5.41a, b and the PSD of the calibrated modulator for process variation is plotted at fast, slow and with a supply of VDD=1.5V. The power consumption of the PVTE circuitry is not included since it is not turn on during normal operation. With this, the FoM_{SNDR} and

Fig. 5.34 Variation in PVTE output frequency with temperature at nominal corner

Fig. 5.35 Variation in PVTE output frequency with temperature at fast corner

Fig. 5.36 Variation in PVTE output frequency with temperature at slow corner

$FoM_{Schrier}$ is calculated to be. The chip micrograph is provided in Fig. 5.43 when the area allocation. The chip measurement was not successful and was found to be a result of an improper startup condition. The integrator capacitors were not properly initialized during startup and resulted in the high gain filter saturating. This is detrimental to the system and resulted in the modulator's inability to recover itself. The total power consumption is $230\mu W$ with a supply of $VDD=1.5V$. The power

consumption of the PVTE circuitry is not included since it is not turn on during normal operation. With this, the FoM_{SNDR} and $\text{FoM}_{\text{Schrier}}$ is calculated to be 0.195pJ/conv and 171dB respectively. The chip micrograph is provided in Fig. 5.43 with the area allocation.

Fig. 5.37 FFT of Jitter clock (100ps) against Ideal Clock

Fig. 5.38 PSD Plot of 4th Order CIFF Modulator with JIE ON (Black) and JIE OFF (Grey)

Fig. 5.39 PSD Plot of 4th Order CIFF Modulator with JIE ON (Black) and JIE OFF (Grey)

Fig. 5.40a Simulated PSD of 4th order $\Delta\Sigma$ modulator at input of -6.5dBFS (FFT Points=16384) (Top)
 Fig. 5.40b Simulated PSD of 4th order $\Delta\Sigma$ modulator at input of -67dBFS (FFT Points=16384) (Bottom)

Fig. 5.41a Simulated PSD of PVT calibrated Nominal corner at -6.5dBFS (FFT Points=16384) (Top)
 Fig.5.41b Simulated PSD of PVT calibrated Fast corner at -6.5dBFS (FFT Points=16384) (Middle)
 Fig.5.41c Simulated PSD of PVT calibrated Slow corner at -6.5dBFS (FFT Points=16384) (Bottom)

5.5 References

- [1] YuQing Yang, et al., “A 114 dB 68 mW chopper-stabilized stereo multi-bit audio A/D converter”, *ISSCC Dig. Tech. Papers*, pp. 56-477, 2003.
- [2] Prasad, A., et al., “A 120dB 300mW stereo audio A/D converter with 110 THD+N”, *Solid-State Circuits Conference, ESSCIRC, Proceeding of the 30th European*, pp. 191-194, 2004.
- [3] YuQing Yang, et al., “A Single-Die 124 dB Stereo Audio Delta-Sigma ADC With 111 dB THD”, *Solid-State Circuits, IEEE Journal of*, vol.43, Issue 7, pp. 1657-1665, 2008.
- [4] Pavan S., et al., “Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique”, *Solid-State Circuits, IEEE Journal of*, vol.45, Issue 7, pp. 1365-1379, 2010.
- [5] Sukumaran, A., et al., “A 280 μ W audio continuous-time $\Delta\Sigma$ modulator with 103dB DR and 102dB A-Weighted SNR ”, *Solid State Circuits Conference (A-SSCC), IEEE Asian*, pp. 385-388, 2013
- [6] R. Schreier, The Sigma-Delta Toolbox, Delsig Matlab Toolbox, Version 7.1 ed., 2004.
- [7] Gerfers, F., et al., “A clock jitter insensitive multibit DAC architecture for high-performance low-power continuous-time $\Sigma\Delta$ modulators”, *Electronics, Circuits and Systems (ICECS), IEEE International Conference*, pp.958-961, 2003.
- [8] Jun-Gi Jo, et al., “A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR)

- DAC and High-Speed DWA”, *Solid-State Circuits, IEEE Journal of*, vol.46, Issue 11, pp. 2469-2477, 2011.
- [9] Li. Z, “Design of a 14-bit Continuous-Time Delta-Sigma A/D Modulator with 2.5MHz Signal Bandwidth” PhD Thesis, Oregon State University, 2006.
- [10] Moo-Yeol Choi, et al., “A 101-dB SNR hybrid delta-sigma audio ADC using post integration time control”, *Custom Integrated Circuits Conference (CICC), IEEE*, pp.89-92, 2008.
- [11] Lucien L.Breems, et al., “Design for optimum performance-to-power ratio of a continuous time sigma delta modulator”, *Proc. European Solid State Circuits Conference (ESSCC), IEEE*, pp.318-321, 1999.
- [12] Bolatkale, M., et al., “A 4GHz CT $\Delta\Sigma$ ADC with 70dB DR and -74dBFS THD in 125MHz BW”, *ISSCC Dig. Tech. Papers*, pp. 470-472, 2011.

Chapter 6 A 1V 103dB Pseudo 3rd Order Audio Continuous-Time $\Delta\Sigma$ ADC with Enhanced Noise Shaping in 65nm CMOS

Abstract This work proposes an efficient 2nd order hybrid CT $\Delta\Sigma$ modulator with a DT feedback Noise Coupling (NC) strategy for digital audio application utilizing a 5b SAR quantizer in an advanced nanoscale CMOS 65nm technology at a low supply VDD of 1V. Mismatches in SAR comparator and DAC array is mitigated with a proposed calibration scheme while CM mismatches are solved by a Floating Differential Charge Storage Capacitor (FDCSC) coupling method. In order to allow ample time for SAR conversion bit cycling and noise charge feedback settling, 1Ts Excess Loop Delay (ELD) compensation is proposed with a digital differentiation technique that minimizes both the power and complexity of the auxiliary feedback DAC. The prototype obtained DR/SNR/SNDR of 103.1dB/100.1dB/95.2dB while dissipating 0.8mW, hence achieving a FoM_{SNDR} and $FoM_{schreier}$ of 0.34pJ/level and 178dB respectively.

6.1 Introduction

In Chapter 5, the utilization of high filter order to achieve performance is explored. The quantizer employed is a simple 1b comparator. It was also discussed that the consequential single bit DAC feedback is highly sensitive to clock jitter. As such, the JIE circuitry is proposed to relax requirements on the sampling clock. Instead of an auxiliary JIE circuitry, a more direct approach to mitigate jitter is to reduce the high frequency noise. It can be perceived that the sampling process is a multiplication of the

sampling clock with the input feedback signal in the time domain. As such, the resultant convolution in frequency domain will give rise to an elevated inband noise floor due to in-folding of clock phase noise. In this respect, reducing the high frequency noise can minimize this aliasing effect. Intuitively, the system can therefore be de-sensitized by minimizing the feedback rate of change by having a multibit feedback DAC structure. In advanced nanoscale technology where voltage headroom is scarce, multibit feedback also reduces the amplifier output voltage swing as well as optimizes power consumption otherwise needed for achieving fast transients. Resorting to high order filter structures [1-2] for improvement of performance can lead to complex implementations, of which increasing active components required for charge accumulation may result in higher power consumption.

Improving noise shaping efficiency without increasing the number of active opamps is a better approach since excess loop latency can degrade the ADC stability. In view of this, there are a number of researches conducted to enhance noise shaping with reduced number of opamps. [3] targeted to achieve a desired filter order via high order single opamp integrator structures. However, such architectures presented a filter frontend often with a reduced degree of freedom for design trade off optimizations.

The other line of research looked into noise shaping enhancement by harnessing the quantization error, whereby it is then coupled back to the filter for nullification at low frequency noise energies [4],[5]. This approach had been pre-dominantly employed in DT $\Delta\Sigma$ modulator. [6] presented a solution implemented in a CT $\Delta\Sigma$ modulator. However, the design necessitates an active adder block that incurs a power penalty. We propose in this work an embedded noise shaping SAR as the 5b quantizer in a CT $\Delta\Sigma$ modulator. This novel structure took advantage of the SAR charge redistribution algorithm that inherently stores the residue on its sampling capacitors upon bit cycling

completion, hence making the quantization noise conveniently available for the noise coupling protocol. This work improvised on the noise coupling technique otherwise dominated by DT modulators, proposes an enhanced solution resolving former shortcomings present in DT structures, making it suitable for CT implementation without any additional active components from system's architectural perspective. It also proposes solutions to mitigate non-idealities in both Differential Mode (DM) and Common Mode (CM) mismatches in the noise coupling structure. Section 6.2 describes the evolution of the noise-coupling concept and the proposed method which is structurally more suitable for CT $\Delta\Sigma$ modulator architectures.

Section 6.3 explains the integration of the proposed noise-coupled technique into the CT $\Delta\Sigma$ modulator system together with a proposed digital differentiating ELD compensation method resulting in a simplified, power efficient auxiliary feedback loop. Section 6.4 discusses the circuit implementation and non-idealities in detail. Section 6.5 presents and discusses the measurement results of the prototype built in 65nm standard CMOS technology. Finally section 6.6 concludes the presentation of this work.

6.2 NC $\Delta\Sigma$ Modulator

The NC $\Delta\Sigma$ modulator architecture was first proposed in [4]. The simplified block level diagram of the system with one added order quantization noise attenuation is shown in Fig. 6.1a and Fig. 6.1b with and without timing constraints via addition delay paths respectively. The quantization noise is derived from the difference between the quantizer input and the digitized output. It is then injected back into the filter with a unit delay. In a conventional $\Delta\Sigma$ modulator, the noise shaping effect is a result of the

Fig. 6.1a Basic NC DT $\Delta\Sigma$ modulator Architecture with Timing Constraints on DEM

Fig. 6.1b NC DT $\Delta\Sigma$ modulator with added Delay Paths to mitigate Timing Constraints

high forward gains that forces the noise level at the quantizer input to be complementary to the actual quantization noise for nullification.

It ensures a high signal to noise ratio at the modulator output. This intuition extends itself when there is additional coupled noise feedback, making the filter output contain a lower quantization noise level at low frequencies. Referring back across the high gain feed forward filter, the output of the modulator therefore experiences an enhanced noise shaping effect. However, these improvements come with the penalty for an active adder implying extra power consumption while incurring design complexities.

causing distortions and noise elevations. This is especially important for CT implementation since signal and feedback charges are constantly accumulated down the filter. The sampling of high amplitude signals also means boot strapping is needed for the switches. This increases the complexity of design implementation especially when it has to be realized in nanoscale technologies where voltage headroom is scarce. Implementation of this topology in CT domain can therefore be challenging due to the presence of high switching energies. As a result of the above reasons, the development of NC $\Delta\Sigma$ modulators is in majority limited to the DT domain that manages switching issues through a highly synchronized scheme.

6.2.1 Noise Shaping SAR in NC $\Delta\Sigma$ Modulator

The charge redistribution SAR converter is considered as one of the most energy efficient ADC structures. It utilizes only one comparator for bit determination comparison and a SAR algorithmic controlled capacitive DAC array. Oversampled CT $\Delta\Sigma$ modulator researchers recognized this and had attempted to replace the power hungry internal multibit flash quantizers with SAR ADCs [8][9][10][11], however, without NTF noise shaping enhancements. An N bit SAR ADC requires N-1 refresh cycles of the DAC capacitor array, which is inclusive of the initial input charge sampling. Fig. 6.3a shows an example of the single ended input voltage transition of a 5 bit SA controlled capacitive DAC to the comparator.

The input signal is first top plate sampled onto the DAC capacitor array. On the first cycle window, the comparator will decide if the sampled input is larger than the common mode voltage in this single ended case. If the output is high, the MSB capacitor (i.e. 16C) connected to the high reference will be switched to 0V (GND)

Fig. 6.3a SAR Conversion Sequence showing that the 5th Charge Redistribution is not necessary as SAR ADC output is achieved by the Nth comparison (Top)

Fig. 6.3b Single-Ended Capacitor array movement with SAR conversion algorithm (Bottom)

while the binary MSB output for this SAR conversion can be deemed as 1 (high). In Fig. 6.3a, it can be observed that this transition will result in a drop in voltage level on the capacitor array by a magnitude of $V_{ref}/4$.

This routine repeats itself until all the binary conversion result is determined. At the end of the fifth comparison cycle, the comparator will make the decision for the determination of the final LSB based on the residue from the previous cycle. However, it becomes clear that the Nth (i.e. 5th) charge redistribution cycle is not necessary for the conventional SAR A/D conversion. Fig. 6.3b shows the switching sequence of the single ended DAC capacitive array. In [12], it was observed that an additional charge redistribution (i.e. the Nth cycle) post LSB determination reveals the residual stored voltage on the DAC capacitors. In the context of a $\Delta\Sigma$ modulator, this residual voltage is the quantization noise. This work proposes utilizing this stored residual charge for noise coupling purposes as described in Section 6.2.

Utilizing the SAR as the multibit quantizer has the following advantages. Fig. 6.4a and Fig. 6.4b shows the simplified block level diagram showing the difference in the conventional SLD NC $\Delta\Sigma$ modulator with the proposed SAR NC $\Delta\Sigma$ modulator architecture. Firstly, the residual voltage for quantization noise feedback is inherently generated by the SAR conversion cycles. The residual voltage at the capacitor array top plates after each SAR conversion is available for backward injection. Hence, there is no high signal level charge storing and discharging performed at the frontend filter, which minimizes opportunities for kick back and high energy spikes related distortion issues. The feedback residue carries the actual quantization noise, which is limited only to within 1 LSB of the quantizer resolution. Secondly, there is only one set of bootstrap switches required to sample the transient output of the last integrator. This

simplifies the implementation complexity on the synchronization of the switching instances. Third, as compared to a typical flash architecture, the SAR quantizer is much more energy efficient as only one comparator is needed without the need for generation of comparator references.

Fig. 6.4a Nth order SLD NC $\Delta\Sigma$ modulator with Shifted Loop Delay (SLD) indicating the sampling and feedback paths indicative of the processing of the various signal nature

Fig. 6.4b Proposed SAR NC $\Delta\Sigma$ modulator sampling backend revealing the required handling of only a small feedback signal magnitude

6.3 Architectural Implementation Considerations

This section discusses the system level considerations for the implementation of the CT $\Delta\Sigma$ modulator. The development of the architecture was approached via the well-established DT methodology before adding critical structural components such as the Excess Loop Delay (ELD) signal path and the noise coupling feedback.

6.3.1 NC $\Delta\Sigma$ Modulator Architecture

Fig. 6.5 illustrates the simplified architecture with the noise-coupling path in the DT domain with symbolically represented integrators.

Fig. 6.5 Block level diagram of the DT NC $\Delta\Sigma$ modulator structure for analysis

The Noise Transfer Function (NTF) of a typical second order CIFF DT $\Delta\Sigma$ modulator without enhanced noise shaping is shown in (6.1).

$$NTF_{2nd}(z) = \frac{(z-1)^2}{z^2 + (a_1-2)z + 1 + a_2 - a_1} \quad (6.1)$$

To include the noise coupling feature, an additional feedback path is added to the output of the second integrator. The difference between the modulator output and the quantizer input gives the resultant quantization noise targeted for attenuation. The Noise Transfer Function (NTF) of this second order noise coupled modulator can then be worked out to be as shown in (6.2). The corresponding Loop Transfer Function (LTF) is derived as (6.3).

$$NTF_{2nd,NC}(z) = \frac{(z-1)^3}{z[z^2 + (a_1-2)z + 1 + a_2 - a_1]} \quad (6.2)$$

$$LTF_{2nd,NC}(z) = \frac{(a_1+1)z^2 + (a_2-a_1-2)z + 1}{(z-1)^3} \quad (6.3)$$

The NTF of this structure revealed a noise shaping function with all three zeroes placed at DC, indicating an increased noise shaping efficiency. The in band noise of the ADC is therefore shaped with a 3rd order function. The out of band noise is primarily dictated by the poles of the NTF.

Rearranging (6.2) and grouping the terms for the second order NTF, it is observed that the resultant transfer function, (6.4), can be expressed as the original second order noise shaping system with an additional DC zero and origin pole. This multiplicative function $(z-1)/z$ can be recognized as a delay line canceler whereby the frequency response can be simply plotted as shown in Fig. 6.6 with nulls seen at multiples of the sampling frequency, F_s .

Fig. 6.6 Intuitive illustration revealing the effect of Noise Coupling (NC) on the NTF

$$LTF_{2nd,NC}(z) = \left(\frac{z-1}{z}\right) * NTF_{2nd}(z) \quad (6.4)$$

From Fig. 6.6, it becomes apparent as to how NC brings about an enhanced NTF. In effect, NC pushes low frequency noise to higher frequencies through a slow nullification process, hence improving noise shaping without physically increasing active filter components. As such, for this implementation, the choice made was to choose the complex conjugate poles be positioned identically as for a second order NTF. The phase margin of the pseudo 3rd order system does not have any significant

phase margin degradation. This was ensured by a choice of a lower OOB gain in the design of NTF. With a OOB gain choice of 1.25, the phase margin of the LTF is evaluated to be 49 degrees.

Compared to a typical third order system, the stability conditions of this noise coupled pseudo third order system is more favored. Conventional third order system suffers from three integrator stages of phase lag contribution. Especially for a multibit design, conservation of the loop integration time is important as DEM is usually required to curb feedback DAC linearity issues. Higher order systems also cannot achieve as high a modulation index as compared to lower order architectures.

Conventional NC CT $\Delta\Sigma$ modulator suffers from a necessity for active signal accumulation at the quantizer. In a CT $\Delta\Sigma$ modulator, the inclusion of such active components will result in additional phase lag that will degrade the system stability. It will also result in extra power consumption required to maintain signal integrity and noise requirements.

In Section 6.2, the DT $\Delta\Sigma$ modulator research on shifted loop delay is discussed. This architecture targets to achieve noise coupling without the additional active adder. However, there are fundamental differences between CT and DT $\Delta\Sigma$ modulators. Unlike the DT $\Delta\Sigma$ structure, the CT $\Delta\Sigma$ modulator does not have a delaying integrator structure to leverage on. The technique to shift the delay from the second integrator is therefore not applicable. To resolve this, we propose a deliberate addition of a unit sampling clock delay to the quantizer in contrast to a typical $0.5T_s$ delay.

The derivation of this delay from the quantizer serves three roles, that is, to allow ample time for the multibit quantizer conversion, quantization noise coupling signal acquisition cum feedback and lastly DEM bit shuffling in the main feedback branch.

With this inclusion, Excess Loop Delay (ELD) compensation is necessary to maintain stability. This consideration is discussed in Section 6.3.2.

Due to the tight loop feedback timing requirements in a typical CT $\Delta\Sigma$ modulator; it is paramount that each operation should be allocated with an adequate proportion of the introduced unit delay.

6.3.2 Continuous-Time Architecture Realization

The CT nature of the CT $\Delta\Sigma$ modulator means the architectural construction should be performed in the S-domain. In this design, the pseudo third order structure has to be compensated for excess loop delay due to the added 1Ts delay. For compensation, this time delay is replicated in the DT domain to derive the compensating coefficient before mapping it into the CT regime. The Nth order DT $\Delta\Sigma$ modulator with a Cascade of Integrators with weighted Feed Forward (CIFF) summation topology has a generalized transfer function as shown in Eqn 6.5.

$$LTF_{DT}(z) = \sum_{i=1}^N \frac{a_i}{(z-1)^i} \quad (6.5)$$

For adaptation to the CT $\Delta\Sigma$ modulator, the delay can be seen as extracted from the multibit quantizer instead of the Nth integrator. As such, after removing a unit delay, the residual $LTF_{DT,res}(z)$ has to be identical to the residual $LTF_{CT,res}(z)$ in the CT domain.

Removing an unit delay of 1Ts from the DT $LTF_{DT}(z)$,

$$LTF_{DT,res}(z) = \sum_{i=1}^N \frac{a_i z}{(z-1)^i} \quad (6.6)$$

Expanding (6.6), we have

$$LTF_{DT,res}(z) = \frac{a_1 \cdot z}{z-1} + \frac{a_2 \cdot z}{(z-1)^2} + \dots + \frac{a_N \cdot z}{(z-1)^N} = \frac{\sum_{i=1}^N a_i \cdot z(z-1)^{N-i}}{(z-1)^N} \quad (6.7)$$

In order to extract the zero order coefficient necessary to compensate for the unit delay, (6.7) is further factorized,

$$LTF_{DT,res}(z) = a_1 + \frac{\sum_{i=2}^N [a_i \cdot z(z-1)^{N-i}] + (z-1)^{N-1}}{(z-1)^N} = a_1 + \frac{a_1}{(z-1)} + \sum_{i=2}^N \frac{a_i \cdot z}{(z-1)^i} \quad (6.8)$$

From (6.8) it is imperative to observe that the zero order coefficient responsible for the compensation of the introduced unit delay is a_1 .

To ensure the loop characteristics in the CT domain matches the derived DT LTF, the *Impulse-Invariant Transformation* [13], (6.9) is used.

$$H_{DT,LTF}(z) = \mathcal{Z}\{\mathcal{L}^{-1}[H_{DAC}(s) \cdot H_{CT,LTF}(s)]|_{t=nT_s}\} \quad (6.9)$$

The Nth order $LTF_{CT,res}(z)$ can be derived to be as shown in (6.10).

$$LTF_{CT,res}(s) = \sum_{i=1}^N \frac{b_i}{s^i} \quad (6.10)$$

Applying the Inverse Laplace transformation, with a Zero Order Hold (ZOH) NRZ DAC feedback with the following expression, $H_{DAC,NRZ}(s) = \frac{1}{s}(1 - s^{-sT_s})$, (6.10) becomes,

$$Y_{CT,LTF}(t) = \mathcal{L}^{-1}\left[H_{DAC,NRZ}(s) \cdot \sum_{i=1}^N \frac{b_i}{s^i}\right] = \sum_{i=1}^N \left[\frac{b_i}{N!} \cdot [t^i - (t - T_s)^i]\right] \quad (6.11)$$

For a normalized sampling frequency with $T_s = 1$ and taking Z-Transform of the sampled time domain function $Y_{CT,LTF}(kT_s)$,

$$LTF_{CTDT,res}(z) = \mathcal{Z}\left\{\sum_{i=1}^N \left[\frac{b_i}{N!} \cdot [k^i - (k-1)^i]\right]\right\} \quad (6.12)$$

Where the Z-Transform of k^i can be expressed in (6.13).

$$G(z) = \sum_{n=0}^{\infty} k^i \cdot z^{-n} \quad (6.13)$$

Hence, for a second order function, using (6.13), (6.12) simplifies to (6.14).

$$LTF_{CT,res}(z) = \mathcal{Z} \left\{ \sum_{i=1}^2 \left[\frac{b_i}{2!} \cdot [k^i - (k-1)^i] \right] \right\} = b_1 \frac{1}{z-1} + b_2 \frac{0.5(z+1)}{(z-1)^2} \quad (6.14)$$

The coefficients of the CT $\Delta\Sigma$ modulator can then be obtained by comparing the coefficients of z between (6.14) and the discrete LTF (6.15) ignoring the zero feedback coefficient responsible for the compensation of the added 1Ts ELD.

From Eqn 6.8, for a second order DTSD ADC structure,

$$LTF_{DT,res}(z) = \sum_{i=1}^2 \frac{a_i \cdot z}{(z-1)^i} - a_1 = a_1 \frac{1}{z-1} + a_2 \frac{z}{(z-1)^2} \quad (6.15)$$

The MATLAB model of the 2nd order NC CT $\Delta\Sigma$ modulator is shown in Fig. 6.7. The model includes the main DAC loop, ELD compensation and NC feedbacks. The CT filter frontend and the 5 bits quantizer is common for these 3 feedback routes. For the main DAC feedback, the important components are only the Dynamic Element Matching (DEM) block with the actual 32 cell DAC. In the model, the actual DEM is not included. However, due to its finite processing time, a delay has to be accounted for its operation. As such, from system requirements, an allocated 0.5Ts is inserted in this path. For the DAC, the quantizer output is maintained in its discrete voltage format, whereby it is directly taken to complement the input signal.

The ELD compensation path is modelled with a simple signal subtraction between the direct SAR digital output with its delayed form. Due to the SAR quantizer conversion time of 0.5Ts, the ELD compensation feedback has to be completed within the second 0.5Ts of the assigned unit delay. As a result, the original compensation coefficient is multiplied by a factor of two to accommodate for this effect. In order to eliminate the

necessity for an active adder, the second integrator is doubled up for signal summation in addition to its filter integration function. To allow for this, the ELD feedback has to be done at the 2nd integrator input summing node. Since the ELD feedback now undergoes an integration function, to ensure an equivalent compensating coefficient, a prior differentiation has to be performed. In this design, this differentiation can be performed in the discrete time domain. In the model, the differentiation operation can simply be modelled as a difference between the actual and unit delayed quantizer output. In the actual architecture, this is done purely in the digital domain with a binary subtractor that conveniently takes the SAR binary output for computation, hence simplifying the routing complexities of a thermometer coded output flash converter. In order to ensure the ELD feedback integrator is only done on the second $0.5T_s$, a synchronizer is included. To do this, a multiplexer is added in the signal path. It is controlled by the modulator clock whereby the correct feedback is selected only during the second clock phase. In the first clock phase, the ELD feedback is switched

Fig. 6.7 MATLAB Model of 2nd Order CT $\Delta\Sigma$ Modulator with Noise Coupling

to ground. In the actual system, the multiplexer is switched to the common mode digital signal during the 1st clock phase.

The NC feedback is modelled in a simplified form. This is because the actual charge redistribution SAR ADC capability of residue quantization noise extraction is not modelled. The acquisition of the quantization noise is modelled as simply a difference in the continuous time analog quantizer input and its digitized output. This quantization noise is integrated across the 2nd integrator in a discrete fashion.

In this sense, the 2nd integrator takes the role of both a CT and DT integrator. As with the ELD compensation feedback, the DT integration necessitated the acquired quantization to be discretely differentiated. However, in the actual system, this is not as trivially done as that of the ELD feedback. This is due to the reason that the quantization noise is still represented in the analog domain. Section 6.3.3 describes the DT differentiation via an alternating NC charge storing capacitors. Fig. 6.8a shows the PSD of the ideal second order CT $\Delta\Sigma$ and pseudo third order CT $\Delta\Sigma$ realized via noise coupling modulators at input of -65dBFS. It can be observed that the low amplitude linearity is excellent. The simulations are performed in MATLAB. It can be observed that the NTF in the pseudo third order structure is enhanced due to NC with -60dB/dec noise attenuation. It can also be observed in Fig 6.8b that the harmonic distortions are reduced when NC is turned on, indicating an improvement in the modulator linearity.

6.3.3 Incorporating SAR Quantizer into System

Fig. 6.9a showed the proposed system block level diagram, which includes the NC feedback path. For simplicity, the first integrator with the other feedback paths other than the NC signal route is shown. It can be observed that, in order to avoid the usage

Fig. 6.8a Comparison of PSD Plots of 2nd Order CT $\Delta\Sigma$ modulator when NC is turned ON (Blue) and OFF (Red) with input at -65dBFS

Fig. 6.8b Zoom in of PSD Plots at low frequencies (100Hz $\rightarrow$ 50kHz) when NC is turned ON (Blue) and OFF (Red)

of an additional signal summer; the stored quantization residue is injected to the front of the second integrator. To allow for this, a DT differentiation operation has to be applied to the stored noise on the SAR capacitor array. A simplified system illustration showing the differential capacitor arrays with the noise charge storing capacitors, CR_{1p}/CR_{1n} , CR_{2ap}/CR_{2an} and $CR_{2\beta p}/CR_{2\beta n}$ is given in Fig. 6.9a with its

Fig. 6.9a Proposed NC CT $\Delta\Sigma$ modulator showing 2nd integrator and symbolic SAR quantizer with NC feedback path

Fig. 6.9b Timing diagram of clock signals controlling NC switches for noise injection

corresponding timing diagram in Fig. 6.9b.

From the system's perspective, the insertion of additional charge storing capacitors required an attenuation of the multibit quantizer input. To ensure an equivalent ratio of charge stored and transferred across the second integrator, the capacitor values of CR_{1p}/CR_{1n} , CR_{2ap}/CR_{2an} and CR_{2bp}/CR_{2bn} should be identical to the integrating capacitor C_{int2p}/C_{int2n} . This dictated an important trade off in the architectural design. Should the noise storing capacitors be scaled down, the integrating capacitors have to be scaled down by the same magnitude. This will imply that the integrator resistors be increased to maintain the targeted integration coefficient, hence impacting the noise

performance. Fortunately, there is substantial attenuation when input referred to the modulator front end due to the gain provided by the first integrator stage.

On the other hand, it was observed that the attenuation of the integrator output amplitude had brought about two significant advantages. Firstly, it should be noted that the input to the quantizer possesses the highest signal amplitude. The SAR DAC array has to be charged up to this signal amplitude on every sampling cycle. To maintain signal integrity, boot strapping is required both to provide a fully open, properly-conducting switch as well as to ensure the on-resistance remains unchanged under fluctuating V_{gs} to maintain linearity. This is especially important when the settling time (i.e. determined by the 2nd integrator drivability) is designed to be just sufficient for conserving power consumption. The first integrator output was maintained low by having a feedforward design. Secondly, the attenuation in amplitude means the OTA supporting the integration function can be realised with a decreased gain bandwidth requirement, hence saving power. In addition, the OTA supporting the integration will not be required to work under high slew rates which will place extra power requirements on the other stage.

In this work, an optimal attenuation of two was chosen. This allows the modulator differential peak to peak input to reach a magnitude of 2V even with a voltage supply of 1V. The DT differentiation was made possible by having a pair of additional alternating charge storing capacitors, namely, $CR_{2\alpha p}/CR_{2\alpha n}$ and $CR_{2\beta p}/CR_{2\beta n}$ as shown in Fig. 6.9b with the timing diagram. For each channel, $CR_{2\alpha}$ and $CR_{2\beta}$ take turns to store the residual charge in alternating sampling instances. Subsequently, these charges can be subtracted from the main noise storing capacitors CR_{1p}/CR_{1n} which are active on every sample via cross coupling of the feedback. During operation, the integrator output is sampled directly onto the top plates of the DAC capacitor array

together with the noise storing capacitors. This ensures that no additional charge sharing step is required, which might result in a loss of quantization noise information [10]. With the SAR quantizer embedded in a CT $\Delta\Sigma$ modulator, the strongly correlated integrator and charge storage capacitors renders the charge sharing technique impossible to achieve an optimal sizing.

6.3.4 Digital Differentiation Excess Loop Delay Compensation

This section discusses the digital differentiation ELD technique. Fig. 6.10 shows the implementation of the zero order feedback coefficient giving by K_{ELD} . The total time allocated to this loop is $1T_s$, which is consumed collectively by the multibit quantizer,

Fig. 6.10 Simplified ELD compensation block level diagram illustrating timing allocation for $1T_s$ delay with $0.5T_s$ in SAR and $0.5T_s$ in 2nd Integrator

digital differentiator and the second integrator of the filter. The quantizer takes up $0.5T_s$ and the combined digital differentiator and the second integrator takes the remaining $0.5T_s$. This ensures ample time for the second integrator to accumulate the zero order differential charge feedback to the required voltage at its output for ELD compensation. In [14], two DACs were utilized for the discrete differentiation operation. The feedback from the output of the quantizer is split into 2 paths, delayed

by $0.5T_s$ and T_s , each passed into one DAC respectively. The effectiveness of the differentiation heavily depended on the gain bandwidth of the second integrator. To improve this implementation, the discrete differentiation is moved back into the digital domain. A digital subtractor is utilized for this purpose that ensures an exact difference. By doing this, firstly, the numbers of DACs are reduced from two to one. Additionally, the number of unit current cells for this DAC is greatly reduced since it now only has to handle the difference of the two feedback paths. In this work, we proposed an 8 unit current cell auxiliary DAC for this purpose. The number of current cells required is determined by the rate of change of the modulator output and is hence strongly dependent on the OSR of the modulator. With an OSR of 128, the sampling frequency is 6.4MHz for a maximum input frequency at the bandwidth limit of 25 kHz. This works out to a transient voltage of $dv/dt = (1 * 2\pi * 25000)v/s$ for a 1V differential sinusoidal input signal. At 6.4MHz sampling rate, considering only the signal component, the input to the multibit quantizer will be at a maximum rate of 24.54mV/sample, hence corresponding to around 0.8 LSB. A certain margin is required as a result of the noise coupling feedback which doubled the injected quantization noise mean square value. Hence, even after providing sufficient margin for noise coupling injection, the auxiliary DAC was designed with only 8 LSBs differential unit current cells.

6.4 Circuit Implementation

This section discusses the circuit design implementation, complexities and non-idealities during realization of the system. The circuitries of the major blocks within

the CT $\Delta\Sigma$ modulator are presented in detail for better understanding of the issues that is sensitive to the chosen architecture.

6.4.1 Hybrid SAR System Integration

The charge redistribution SAR structure with 5 bits resolution is chosen as the multibit quantizer. Fig.6.12 shows the simplified system level block diagram for the proposed architecture illustrating all the signal paths. As discussed in section 6.3.3, the unit capacitor values are tagged along with the last integrator filter coefficient. In this design, the unit capacitors are chosen to be 45fF. The residual voltage on the capacitor array at the P^{th} SAR charge redistribution cycle can be expressed mathematically as shown in (6.16) where N represents the resolution of the SAR quantizer.

$$V_P = \frac{2^{N-P} * C_u}{2^N * C_u + C_1 + C_{2\alpha/\beta}} * (V_{refH} - V_{refL}) + V_{P-1} \quad (6.16)$$

The voltages V_{refL} and V_{refH} provide the references for the quantizer for a single ended amplitude of 0 to 1V. Due to the noise charge storage capacitors, C_1 and $C_{2\alpha/\beta}$, the quantizer input is required to swing between 250mV and 750mV. This allows a headroom of 250mV at the driving integrator outputs operating at a supply of 1V. With C_1 and $C_{2\alpha/\beta}$, the DAC capacitor array divides the reference range, $V_{refH} - V_{refL}$ by a factor of 2^{P+1} for each signal channel upon each comparison. The second integrator output drives the top plates of the DAC array. However, this makes the DAC capacitor array sensitive to parasitic capacitance, C_p loading which is predominantly contributed by the offset optimized input transistors of the comparator. The presence of C_p , as shown in Fig. 6.11, can result in a change in the SAR redistribution algorithm as shown in (6.17).

$$V_P = \frac{2^{N-P} * C_u}{2^N * C_u + C_1 + C_{2\alpha/\beta} + C_P} * (V_{refH} - V_{refL}) + V_{P-1} \quad (6.17)$$

If the inputs to the comparator are properly matched, then, the effect of the parasitic capacitance loading will only result in a loss of signal dynamic range. On the other hand, a mismatch in the value of C_p , can cause a wrong decision during the SAR bit comparison. This can be observed under two different scenarios. The first situation that can happen is during the last LSB determination comparator decision. This is less detrimental as this error source will be shaped off by the noise coupling protocol in conjunction with the quantization noise by the modulator NTF. The second occurrence that can happen is during initial SAR bit cycling instance. This will lead to the generation of a grossly erroneous SAR output, which can trigger a vicious cycle that might affect the stability of the modulator. Traditional SAR designs approach this issue by introducing redundancies to detect wrongly made decisions as a result of mismatches. This however reduces the amount of possible allocated time for the loop filter signal integration and DEM shuffling as well as increases the complexities of the system. This work proposes a calibration protocol that minimizes the effect of this non-ideality by making C_1 and $C_{2\alpha/\beta}$ tunable. The effect of a local mismatch between the comparator input transistors can be eliminated by counter-tuning the noise coupling capacitors. For instance, a positive capacitive offset from any source in a signal channel can be resolved by reducing the values of C_1 and $C_{2\alpha/\beta}$ correspondingly. With this, the capacitive ratio in each signal channels can be calibrated to be the same. From another perspective, the mismatch in a channel is therefore consolidated onto the NC capacitors. This creates a differential offset charge injection during the NC phase. To mitigate this error, this work proposes a time staggered chopper stabilization scheme as shown in Fig. 6.12a. The corresponding

Fig. 6.11 Proposed Overall Simplified top level diagram of NC CT $\Delta\Sigma$ modulator showing all feedback paths

timing diagram is illustrated in Fig. 6.12b, whereby C, H and D indicate the charging, holding and discharging phases respectively. The location for feedback into the P or N summing inputs of the second integrator is drawn above each capacitor chopper clock signal. With the prior offset calibration performed, only C_1 and $C_{2\alpha/\beta}$ have to be chopped. As a result of the alternating noise charge feedback, the chopping clock phases for $C_{2\alpha}$ and $C_{2\beta}$ has to be different. Since the subtraction operation is implemented in the differential architecture, the chopper clocks for $C_{2\alpha/\beta}$ are out of phase with the chopper clock for C_1 . The direct approach in designing for noise charge feedback scheme for the differential solution is shown in Fig.6.9a. The responsible noise storage capacitors C_1 and $C_{2\alpha/\beta}$ top plates are connected to the main signal line and the bottom plates to a fixed biasing voltage (i.e. V_{refL} which is 0V in this implementation). Ideally, the common mode voltage of the capacitive DAC top plates should be set at 500mV.

Fig. 6.12a FDCSC Technique with chopper circuitries to mitigate NC capacitors mismatch

Fig. 6.12b Chopper clock for the NC capacitors showing their operations at chopper clock phases

However, it is often slightly displaced as a result of the finite gain in the common mode regulating amplifier at the output of the second integrator. In addition, the common mode voltage at the input of the second integrator might again be different. This contrast in common voltages will cause common mode charge integration across the second integrator. This increases the matching requirements of the second integrator as the common mode charge integration can be manifested into differential noise injection should the Common Mode Rejection Ratio (CMRR) is not designed high enough, causing harmonic distortions. To resolve this, a Floating Differential Charge Storage Capacitor (FDCSC) NC scheme is proposed that adaptively adopts the common mode voltage. To implement this, the bottom plates of CR_{1p}/CR_{1n} , CR_{2ap}/CR_{2an} and $CR_{2\beta p}/CR_{2\beta n}$ capacitor pairs are shorted together instead of connected to a bias voltage. Fig. 6.12a shows the FDCSC scheme and Fig. 6.13 illustrates the charge that would be accumulated by the second integrator with and without

Fig. 6.13 Charge Transfer comparison between conventional and FDCSC Technique

the proposed scheme. In the conventional charge transfer scheme, during the residue collection phase, the NC capacitors are required to store the common mode charges in addition to the differential residue noise charge. In contrast, the FDCSC scheme is only required store the differential residue charge across the DAC array differential lines. This is advantageous when the common mode voltages on the differential DAC array lines and the summing inputs of the second integrator are different as the second integrator will have to recharge the difference in the common mode voltages onto the array every sampling cycle. In addition, during the charge transfer phase, although the differential charge transferred for the conventional is identical to the FDCSC scheme, it should be noted that it is under the assumption that the second integrator is able to perform a perfect integration operation on every cycle. In reality, the second integrator is not ideal and therefore, the actual NC effect is not as promising. On the other hand, the FDCSC scheme only transfers the exact differential NC residue to the input summing nodes of the second integrator. In actual implementation, this scheme also helps to adaptively cope with any common mode fluctuation that might occur during operation, making the system more robust.

6.4.2 System Clock Control

The overall modulator clock control is contained within the SAR quantizer with a modulator sampling clock frequency at 6.4MHz. Overall system operational phases are shown in Fig. 6.14. The three main loops within the system are the Main Feedback Loop (MFL), Excess Loop Delay Feedback Loop (ELDFL) and the Noise Coupling Feedback Loop (NCFL). Each sampling period, T_S , begins at the quantizer sampling instance. The 5 bits SAR quantizer requires 5 SAR comparison loops whereby these cycles should complete within $0.5T_S$.

Fig. 6.14 Diagram showing Overall System Operational Phases

Within the SAR Comparison Phase (SARCP), each comparison cycle is synchronized to a Delay-Line based Timing Control (DLTC) [15]. The DLTC is responsible in generating 5 window pulses that signal the comparator to commence the N^{th} comparison to generate the respective bit output. Fig. 6.15 shows the DLTC block level circuitry. The delay is generated by a biased asymmetrically sized inverter as depicted in the diagram. With a targeted 5 bits resolution, each SAR cycle time is design to be completed within $13.78ns$ with the first sampling window also taken into account. The dynamic comparator used for the SAR quantizer is shown in Fig. 6.16, [15]. When the clk signal ϕ_{CMP} is low, V_p and V_n charges to $0.5 * VDD$ with the comparator outputs V_{outp} and V_{outn} discharging to VSS . This prepares the first comparator first stage as a preamp when ϕ_{CMP} goes high. When this happens, the biasing transistors M_7 - M_8 turns on and the differential input voltage $V_{inp} - V_{inn}$ undergo an amplification across the preamp to the cross coupled latches formed by M_{17} - M_{20} . In this work, the input range varies between 250mV and 750mV, which can only be appropriately handed by a rail to rail input comparator stage. The dynamic comparator of choice have PMOS (M_9 - M_{10}) and NMOS (M_1 - M_2) input differentials to handle the lower and upper input voltage ranges respectively. To provide a higher preamp gain, the input devices are biased in weak inversion for a higher g_m value.

Fig. 6.15 Delay Line Based Timing Control (DLTC) clock pulse generator

M1 M2	4μ/0.4μ	M8	4μ/0.4μ	M15 M16	8μ/0.4μ
M3 M4	4μ/1μ	M9 M10	8μ/0.4μ	M17 M19	1μ/0.4μ
M5 M6	4μ/0.4μ	M11 M12	4μ/0.4μ	M18 M20	8μ/0.4μ
M7	4μ/0.4μ	M13 M14	8μ/0.4μ		

Fig. 6.16 Dynamic Comparator used in SAR quantizer

6.4.3 Excess Loop Delay Compensation

As explained in section 6.3.4, ELD compensation is shifted mostly into the digital domain. Fig. 6.17a depicts the implemented circuit blocks required for the proposed scheme. The first consist of a digital binary subtractor that acts conveniently on the SAR binary current and z^{-1} quantizer outputs.

Fig. 6.17a ELD Feedback simplified Block Level Diagram (Left)
 Fig. 6.17b Digital output representation from Subtractor and Decoder (Right)

Fig.6.17c Digital Subtractor utilized in the ELD Loop

Upon performing a difference, the common mode value of the output is nullified. As shown in Fig. 6.17b, the difference of the various possible subtractor input configurations is tabulated. A binary subtraction will result in a 2's complement output should it be negative. As a result, a decoder is necessary to map the subtractor output to the proper DAC steering digital inputs as illustrated. The binary subtractor and decoder are implemented with asynchronous full adders as shown in Fig. 6.17c and combinational logics respectively whose delays are negligible for consideration. The SAR quantization with the digital subtraction and decoding consume $0.5T_s$, leaving the remaining $0.5T_s$ for integration. Therefore, the DAC should only source the required compensating current for $0.5T_s$ period of time as depicted in Fig. 6.10. This is ensured by the integration synchronizer that timed the DAC output to be valid only for the second $0.5T_s$. With this, the zero order coefficient derived in Section 6.3.4 has to be scaled by a factor of two to achieve the desired compensation.

6.4.4 Main DAC Feedback

The performance of the main DAC is paramount to the system performance. In order to optimized noise performance as well as provide high output impedance to prevent current variation, the current unit transistors are enlarged in size. To curb dominant flicker noise source during device saturation, it can be observed from (6.18) and (6.19) that the W and L of the MOSFETs should be large. The flicker noise power $V^2_T(f)$ is given as:

$$V^2_T(f) = \frac{K_f}{(W * L * C_{ox} * f)} \quad (6.18)$$

Converting into the corresponding noise current, $I^2_T(f)$ is given as:

$$I^2_T(f) = \frac{K_f * g_m}{(W * L * C_{ox} * f)} \quad (6.19)$$

Therefore in this design, the unit current NMOS are sized at $W=1\mu\text{m}$ and $L=2.6\mu\text{m}$. This is a compromise when considerations for low VDD headroom issue are taken into account. Especially so in a low voltage design, good matching between the PMOS sourcing and NMOS DAC current cells is required. Otherwise, the current difference can result in CM voltage fluctuations at the integrator summing node. Such phenomenon can manifest itself into harmonic distortions under the influence of mismatched differential components such as the input resistors or transistors. The integrator summing node impedance is held low with a DC stabilizing amplifier [16] via sinking or sourcing any excess common mode currents to prevent voltage movements. Fig. 6.18a shows the block level diagram of the main DAC with the auxiliary amplifier. The amplifier noise in first order will be rejected by the differential operations. A folded cascode structure is utilized with a pseudo differential

PMOS input stage as illustrated in Fig. 6.18b. The average of the summing nodes is compared with $0.5V_{DD}$, of which the amplifier is configured in a negative feedback that eliminates the error by regulating the PMOS current. The open loop gain of the amplifier is 80dB with a bandwidth of 1.2MHz while consuming $10\mu A$ at 1V V_{DD} .

Fig. 6.18b Pseudo Differential DC regulating opamp

6.4.5 Loop Filter Design Consideration

The feed forward loop filter is realised using capacitive feedforward techniques. This saves energy and area while keeping the implementation complexity down. All forward signals are injected into the summing node of the second integrator, whereby its output drives the SAR capacitor array. Fig. 6.11 shows the overall proposed CT $\Delta\Sigma$ modulator. To reduce the sensitivity to coefficient shifts due to process variation, the overall quantization noise is budgeted below the input resistive thermal noise.

6.4.5.1 First Integrator Design

The first integrator defines the overall modulator noise performance. The noise sources are derived from the input resistors as well as the active opamp, which together with the integrating capacitors constitute the highly linear RC integrator structure. (6.20) shows the overall r.m.s noise where $V_{i,noise}^2$ constitute all the individual input noise powers.

$$V_{Int1}(f) = \sqrt{(\sum_i^N V_{i,noise}^2)} = \sqrt{[V_{Rin,noise}^2 + V_{Ampout,noise}^2 * \frac{1}{|A_{v,int}|}]} \quad (6.20)$$

The input resistor thermal noise $V_{Rin,noise}^2$ is given by $4kTf_{BW}R_{in}$ which resulted in an r.m.s. differential noise voltage of $1.82\mu V/\sqrt{Hz}$ with a resistor of $8k\Omega$. The total input referred active opamp noise power was simulated to be $63.8nV/\sqrt{Hz}$. The total noise contributed by the first integrator (mostly attributed to the resistive thermal noise) limits the modulator SNR to around $106dB$. The first opamp in the modulator needs to maintain the overall linearity. To relax the linearity requirement, the

The input device M1/M2 is primarily optimized for bandwidth and noise requirements with an appropriate transconductance, $g_{m1/2}$, primarily dictated by the W/L ratio and biasing current. The area of M1/M2 devices given by $W * L$ do not have to be sized up for matching because of chopper stabilization, which also reduces requirement for gain, that was simulated to be at $85dB$. The unit gain bandwidth is designed to be at $2.5F_S$. The phase margin is optimally compensated to be at 60° when loaded with the first integrating capacitors C_{int1p}/C_{int1n} with a value of $9.7pF$ each. The two dominant poles contributed by this OTA structure comes from the two gain stages deriving from the folded cascode and the common source output stage respectively. The overall quiescent power consumption under nominal condition is simulated to be at $200\mu A$.

M1 M2	90 μ /1 μ	M8 M9	24 μ /6 μ	M16 M17	6 μ /1 μ
M3	12 μ /2 μ	M10 M11	60 μ /0.72 μ	M18 M19	6 μ /2 μ
M4 M5	6 μ /2 μ	M12 M13	12 μ /6 μ	M20 M21	8 μ /6 μ
M6 M7	2 μ /0.4 μ	M14 M15	6 μ /1 μ	C _{c1} C _{c2}	2.5pF

Fig. 6.19 Fully Differential Opamp with Class A output stage for First Integrator

The two sets of chopper switches are selected to be at the input of the first and second gain stages respectively. This is because the inputs to MOSFETs are of extremely high impedance and hence have negligible gate current flowing. As such, the on resistance of the switches will not be consuming any voltage headroom crucial under low VDD conditions. As such, the switches can be minimally sized to reduce any parasitic loading on the amplifier, which also maximises the switching speed. M14-21 forms the common mode feedback structure for the fully differential OTA. This common mode circuit is chosen as opposed to the conventional resistive sensing implementation because it does not add extra loading to the output of the OTA. The 2 stage OTA consist of a frontend folded cascode structure with a second stage PMOS common source acting as a class A output stage for the small output swing.

For compensation, miller compensation is employed with the insertion of the capacitors, C_{c1} and C_{c2} . Together with the input transconductance of M1/M2, $g_{m1/2}$, the unity gain bandwidth can be derived to be $g_{m1/2}/C_{cc1/2}$.

The common mode circuitry forms a feedback with the output of the OTA and therefore also requires compensation. However, its compensation for stability can be conveniently accomplished with the main OTA with the same miller compensation capacitors since they share the same signal paths. This constituted one of the reasons

why this common mode regulation is chosen too. The common mode feedback senses the output and regulates the OTA output by controlling the biasing current via modulation of the V_{gs} of M8/M9. The open loop AC simulation of the OTA is shown in Fig. 6.20. This simulation included the output loading when configured as an integrator.

Fig. 6.20a AC Open Loop Gain BodePlot for First Opamp (DC Gain: 84.8dB | Bandwidth: 16MHz)
(Top)

Fig. 6.20b AC Open Loop Phase BodePlot for First Opamp (Bottom)

6.4.5.2 Second Integrator Design

The second integrator multitasks both as a CT as well as a DT integrator. Processing the quantization noise and the ELD compensating feedback signals are done in a CT

manner while integration of the noise coupled signal is performed in a DT nature. Unlike the first integrator, the output dynamic range of the second integrator can be as high as peak to peak of $500mV$ single ended. This is already attenuated by a factor of two due to the attenuation noise coupling capacitors, in the SAR ADC as explained in Section 6.4.1. The output of the second integrator is loaded with the SAR DAC array as well as the second integrating capacitors C_{int2p}/C_{int2n} amounting to $7.2pF$ per channel. As such, to provide the drivability, a class AB output stage opamp is chosen as shown in Fig. 6.21, [17].

To keep quiescent power consumption down, a minimum selector M14-23 is included for each channel. During low input signal idling mode, the current biasing the output transistors will be limited to a minimal quiescent current, I_q . With this architecture, the current flowing through the output driving transistors, M24-27 during operation can be simulated as shown in Figure 16. It can be seen that the PMOS sourcing transistors M24/M26 conducts only when output charging is required. On the contrary, during output sinking, M25/M27 will be responsible for conduction. Otherwise, the respective output drivers will only carry the minimal quiescent current, I_q . This allows for optimal power consumption while achieving high slew rate requirements for DT integration. The operation of the minimum selector is as follows. The regulation for minimal quiescent current conduction through the output transistors is done solely via the PMOS drivers M24/M26. M14/15 and M22/23 are the current sensors for the PMOS and NMOS output drivers respectively. M19/M21 is sized to have the same V_{gs} with M14/M15 during idling condition, which causes the current mirrors to have a ratio of 0.5 into the current branch M15/M17/M20.

In other words, the transistors M18/M20 are biased at the corner between linear and saturation operation region during zero load condition. During high sourcing condition, M24/M26 will experience high current flow, increasing its V_{gs} correspondingly. As such, the current mirrors M18-M21 function as per normal since M18/M20 are brought into saturation. With this, current sensing on the idling drivers M25/M27 is done by M22/M23, which through M4-7/M10-13 configured in a negative feedback, regulates M24/M26 to ensure that only I_q is flowing. On the other hand, during high sinking condition, M25/M27 are active and the quiescent current sensing is therefore performed by M14/M15. However, in contrast with high sourcing condition, M18/M20 are now operating in their linear region, acting like resistors due to low current conduction through M24/M26. With this, regulation is achieved by modulation

M1 M2	100 μ /1 μ	M8 M9	24 μ /6 μ	M16 M17	2 μ /6 μ	M24 M26	40 μ /0.4 μ	M32 M33	6 μ /2 μ
M3	36 μ /2 μ	M10 M11	3 μ /2 μ	M18 M20	20 μ /0.4 μ	M25 M27	16 μ /0.4 μ	M34 M35	16 μ /6 μ
M4 M5	2 μ /0.4 μ	M12 M13	3 μ /2 μ	M19 M21	20 μ /0.4 μ	M28 M29	6 μ /1 μ	C_c1 C_c2	2.5pF
M6 M7	2 μ /0.4 μ	M14 M15	20 μ /0.4 μ	M22 M23	8 μ /1 μ	M30 M31	6 μ /1 μ	C_c3 C_c4	2.5pF

Fig. 6.21 Fully Differential Opamp with Class AB output stage for Second Integrator

Fig. 6.22a AC Loop Gain BodePlot for Second Opamp (DC Gain: 82.9dB | Bandwidth: 25.6MHz)
(Top)

Fig. 6.22b AC Open Loop Phase BodePlot for Second Opamp (Bottom)

of the on resistance of M18/M20. The common mode feedback circuitry is similar to OTA1 whereby a feedback from the output is loop back to control the V_{gs} of M8/M9. As discussed for OTA1, the CMFB is frequency stabilized together with the differential mode compensation. This opamp is built onto the first stage opamp, giving a gain of 83dB and a bandwidth of $4F_S$. The opamp consumes $300\mu A$. The phase margin under normal loading conditions is compensated to be 66.4° . The bode plot diagram is plotted in Fig. 6.22 for reference.

6.4.5.3 Dynamic Element Matching (DEM)

The multibit implementation was chosen for desensitization of the system to clock jitter. However, the linearity of the main feedback DAC has to be maintained to prevent harmonic distortions. From the feedback operation timing as shown in Figure 8, $0.5T_S$ is allocated to the DEM block. With this time, a data weighted dynamic element matching block is implemented. This full digital block is asynchronous and is controlled by a pointer that rotates the DAC current cells that is dependent on the quantizer output. This randomizes the current cells, hence translating to the spreading of distortion causing harmonic tones in the frequency domain.

6.5 Experimental Results

The prototype is built in CMOS 65nm process with $V_{DD} = 1V$ and dissipates 0.8mW. The modulator requires only one reference $V_{CM} = 0.5V$. For a SoC operating at 1.2V, the modulator can be supplied by an internal LDO that also serves the reference $V_{DD} = V_{refH} = 1V$ for the SAR. Fig.6.23 shows the measurement result of the 3rd order NC modulator achieving a SNR/SNDR of 100.1dB/95.2dB at -1.6dBFS input revealing an improvement of 10dB as compared to the performance when NC is turned off. The PSD attenuated with a -60dB/dec slope, indicative of enhanced noise shaping. Fig.6.24 shows the PSD of the modulator with a -58dBFS input with the DWA on. The PSD at 1kHz with input amplitude of -1.59dBFS and -59dBFS is plotted in Fig.6.25 and Fig.6.26 respectively. At 1kHz, the SNR/SNDR at -1.59dBFS measured 102.5dB/93.6dB. The tone at 47kHz is due to the chopper inserted at the first integrator opamp. Fig.6.27 shows the comparison of the PSD with (Black) and without (Grey) the chopper turned on. Even with the chopper, it can be observed that there is

still some residual noise at low frequencies attributed to the feedback DAC. The power consumption breakdown in Fig.6.30 revealed the 5b SAR consumed $102\mu\text{A}$ at 6.4MSPs, taking up 13% of total consumption. The DR plot in Fig.6.28 shows an improvement of 10dB across the input magnitudes with NC incorporated. The chip micrograph in Fig.6.30 shows the silicon area occupied of 0.256mm^2 . Table 6.1 shows the comparison of ADCs achieving the similar DR. It can be observed that the DR of 103.1dB achieving a FoMschreier of 177.9dB is comparable to state of the art ADCs.

Fig. 6.23 Measured PSD when NC turned ON (Black) versus NC turned OFF (Grey) at input amplitude of -1.6dBFS at a frequency of 6.25kHz (N=131072)

Fig. 6.24 PSD of 3rd order NC modulator at -58dBFS 6.25kHz input (N=262144) (Top)

Fig. 6.25 PSD of 3rd order NC modulator at -59dBFS 1kHz input (N=262144) (Bottom)

Fig. 6.26 PSD of 3rd order NC modulator at -1.5dBFS 1kHz input (N=262144)

Fig. 6.27 PSD with chopped OTA1 (Black) and PSD with un-chopped OTA1 (Grey) (N=131072)

Fig. 6.28a Measured DR Plots showing difference when NC turned ON versus NC turned OFF (Top)

Fig.6.28b Measured DR plots showing region boxed in Grey (Bottom)

Fig. 6.29 Power consumption contribution of constituting blocks in modulator

Fig. 6.30 Chip Layout (Top Right) Chip Micrograph showing area occupied by individual modules (Bottom)

Parameter	Units	[17]	[18]	[19]	[20]	[21]	This Work
Technology	(nm)	28	65	45	40	40	65
Fs	(MHz)	24	3.072	12	6.5	26	6.4
BW	(kHz)	24	24	20	24	20	25
DR	(dB)	100.6	96.4	91.7	102	NA	103
Peak SNR	(dB)	100.6	NA	78.7	NA	83	100.1
Peak SNDR	(dB)	98.5	95	76.5	90	79	95.2
Power	(μW)	1130	371	1200	500	500	800
Area	(mm ²)	0.022	0.41	0.0895	0.05	0.05	0.256
Order	-	2	2	2	2	2	Pseudo 3rd
FOM ₁	(dB)	171.8	173.1	148.7	178.8	155	178
FOM ₂	(pJ/step)	0.342	0.168	5.49	0.403	1.72	0.340

$$FOM_1 = DR + 10\log(BW/P) \quad FOM_2 = P / 2f_B * 2^{(SNDR-1.76)/6.02}$$

Table 6.1 Table comparing the performance parameters of this work against other modulators developed on advance technologies with feature size equal or smaller than 65nm

6.6 References

- [1] YuQing Yang, et al., “A Single-Die 124 dB Stereo Audio Delta-Sigma ADC With 111 dB THD”, *Solid-State Circuits, IEEE Journal of*, vol.43, Issue 7, pp. 1657-1665, 2008
- [2] Prasad, A., et al., “A 120dB 300mW stereo audio A/D converter with 110 THD+N”, *Solid-State Circuits Conference, ESSCIRC, Proceeding of the 30th European*, pp. 191-194, 2004
- [3] Zangbaghi, R., et al., “An 80-dB DR, 7.2-MHz Bandwidth Single Opamp Biquad Based CT $\Delta\Sigma$ Modulator Dissipating 13.7-mW”, *Solid-State Circuits, IEEE Journal of*, vol.48, Issue 2, pp. 487-501, 2013
- [4] Lee, K., et al., “Noise-coupled $\Delta\Sigma$ ADC’s”, *Electronics Letters*, vol.42, Issue 24, pp. 1381-1382, 2006
- [5] Lee, K., et al., “A Noise-Coupled Time-Interleaved Delta-Sigma ADC With 4.2 MHz Bandwidth, 98 dB THD, and 79 dB SNDR”, *Solid-State Circuits, IEEE Journal of*, vol. 43, Issue 12, pp. 2601-2612, 2008
- [6] Wang, Y., et al., “Noise-coupled continuous-time delta-sigma ADCs”, *Electronic Letters*, vol.45, Issue 6, pp. 302-303, 2009
- [7] Xin Meng, et al., “Low-Distortion Wideband Delta-Sigma ADCs With Shifted Loop Delays”, *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.62, Issue 2, pp. 376-384, 2015
- [8] L. Samid, et. al, “A new kind of low power multibit third order CT $\Delta\Sigma$ Modulator”, *IEEE Int. Symp. On Circuits and Systems*, vol. 3, pp. 293-296, 2002.

- [9] L. Samid, M. Abu-Ghazi, and Y. Manoli, "A Novel Continuous-Time $\Delta\Sigma$ Modulator with a Successive Approximation Multibit Quantizer", *Proc. IEEE Int. Symp. Circuits*, pp. 59-63, 2003.
- [10] Hung-Chieh Tsai, et al., "A 64-fJ/Conv.-Step Continuous-Time $\Sigma\Delta$ Modulator in 40-nm CMOS Using Asynchronous SAR Quantizer and Digital Truncator", *Solid-State Circuits, IEEE Journal of*, vol. 48, Issue 11, pp. 2637-2648
- [11] Ranjbar, M., et al., "A 3.1 mW Continuous-Time $\Delta\Sigma$ Modulator With 5-Bit Successive Approximation Quantizer for WCDMA", *Solid-State Circuits, IEEE Journal of*, vol. 24, Issue 8, pp. 1479-1491, 2010
- [12] Fredenburg, J., et al., "A 90MS/s 11MHz bandwidth 62dB SNDR noise-shaping SAR ADC", *ISSCC Dig. Tech. Papers*, pp. 468-470, 2012
- [13] Mitteregger, G., et al., "A 14b 20mW 640MHz CMOS CT $\Delta\Sigma$ ADC with 20MHz Signal Bandwidth and 12b ENOB", *ISSCC Dig. Tech Papers*, pp. 131-140, 2006
- [14] Tang, H., et al., "A 1.33 μ W 8.02-ENOB 100kS/s Successive Approximation ADC With Supply Reduction Technique for Implantable Retinal Prosthesis", *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 8, Issue 6, pp.844-856, 2014
- [15] Khiem Nguyen, et al., "A 106dB SNR hybrid oversampling ADC for digital audio", *ISSCC Dig. Tech. Papers*, pp. 176-591, 2005
- [16] de Langen, et al., "Compact low-voltage power-efficient operational amplifier cells for VLSI", *Solid-State Circuits, IEEE Journal of*, vol. 33, Issue 10, pp. 1482-1496

- [17] Tze-Chien Wang, et al., “A 0.022mm² 98.5dB SNDR hybrid audio delta-sigma modulator with digital ELD compensation in 28nm CMOS,” *Solid-State Circuits Conference (A-SSCC), IEEE Asian*, pp.317-320, 2014
- [18] Liu, L, et al., “A 95dB SNDR audio $\Delta\Sigma$ modulator in 65nm CMOS”, *Custom Integrated Circuits Conference (CICC), IEEE*, pp. 1-4, 2011
- [19] Dorrer, L, et al., “A Continuous Time $\Delta\Sigma$ ADC for Voice Coding with 92dB DR in 45nm CMOS”, *ISSCC Dig. Tech. Papers*, 2008
- [20] Tien-Yu Lo, “A 102dB dynamic range audio sigma-delta modulator in 40nm CMOS”, *Solid State Circuits Conference (A-SSCC), IEEE Asian*, pp. 257-260, 2011

Chapter 7 Conclusions and Future Works

7.1 Conclusions

The thesis has presented the design of CT $\Delta\Sigma$ modulator from top level system structural selection considerations, high level architectural synthesis methodology down to the circuit implementation and finally the implemented modulator prototype measurement results. High fidelity audio was chosen as the target application for this research. Along the research process, main issues in the implementation, modulator structural shortcomings and possible circuit level improvements had been identified, discussed with analysis and subsequently, proposals made in order to meet the final objectives to realize the optimized high performance CT $\Delta\Sigma$ modulator. Each chapter laid down the major research milestones, explaining in detail the issues encountered and solutions proposed. Equipped with the adequate know-how, two prototypes were developed with the research into two main different structural approach to achieve high dynamic ranges. The first modulator considered high order filter (4th order) with single bit quantizer with a meticulously planned mitigation of predicted issues that surfaced during system level verification and circuit level design.

On the other hand, the second modulator took a major step, exploring the combination of the niche concepts of filter order enhancement with mixed SAR-based multibit quantization while suppressing the heavy sampling kickback issues detrimental in CT domains.

Chapter 1 discussed the motivation for the need to develop high resolution audio bandwidth CT $\Delta\Sigma$ modulator from the perspective of application requirements, design trends and technological advancement reasons. The objectives are laid and achievements are also summarized for the reader's convenience.

Chapter 2 reviewed modulator architectural considerations reported in the literature. The merits and shortcomings for each proposal were discussed as the basis for the development of the modulator prototypes.

Chapter 3 commenced the discussion into system level implementation, whereby the issues in system level verification, block level specification derivation and high level optimizing iterations were identified. In view of these issues, a circuit-based model was proposed in the high level simulation tool MATLAB for rapid prototyping and verification. A 4th order modulator was chosen as an example for demonstrating the feasibility of the model.

Chapter 4 recognized the merits of using multibit quantization within a CT $\Delta\Sigma$ modulator. However, larger occupied area, higher power consumption of contemporary multibit flash quantizers and heavy linearity requirements in the consequential feedback DAC are accompanying issues with such quantizers. Another prominent issue also stems from the loading of the filter output as a result of the large number of comparators for a typical flash topology.

A fast tracking quantizer is proposed by sensing the Active Comparison Region (ACR) where the dormant comparators can be turned off for power savings. If a dynamic reference is utilized, the redundant comparators can be omitted for area savings. Simulation results show that the power efficiency improves by 72.4%. Due to its

speed, the proposed technique benefits not only low bandwidth modulators but can also be easily extended into high speed applications.

Chapter 5 described the realization of the 4th order CT $\Delta\Sigma$ modulator. The purpose was to research into high order single bit architectures for high resolution. Clock Jitter was enhanced with a fixed ‘ON’ time RZ feedback pulse. Process variation tolerance was improved with a proposed circuitry that detects up to 2.08% RC time constant variation. Other than the first stage implemented with an opamp-RC structure, all other stages are realized as gmC integrators. With this, the 4th order filter was compacted with a proposed current feedforward technique that does not require extra feedforward capacitors that load the integrator outputs, hence saving power. For an adder-less feedforward, the quantizer samples directly at the last gmC integrator output. To allow that, the output signal fluctuation optimized for MSA should not cause signal dependent quantizer input capacitance fluctuation. A comparator for this purpose was proposed, which is verified in simulation to possess an input capacitance change of <1fF across the MSA transient. The modulator, implemented in 180nm technology with a supply of 1.5V was fully verified in simulation and achieved an SNR/SNDR of 90.6dB/88.7dB with a reasonable input dynamic range of differential pk-pk of 2V while consuming a current consumption of only 153 μ A.

Chapter 6 proposed the perceived architecture of choice for a high performance audio CT $\Delta\Sigma$ modulator. To allow for high level integration of multi-channel analog signal channels with a heavy DSP codec, an advance 65nm standard CMOS technology was chosen. As such, the first challenge was to develop a high resolution CT $\Delta\Sigma$ modulator with a low supply of 1V. To maximize MSA under such conditions, a 5b quantizer

was chosen with an OSR of 128 for minimization of integrator component size. A SAR-based structure was utilized to minimize the area and power of the 5b quantizer which would otherwise result in 32 power hungry comparators loading the output of the 2nd integrator in the flash topology. To enhance the NTF further, Noise Coupling (NC) was proposed. Due to the sensitivity to kickback noise in CT $\Delta\Sigma$ modulators, the residue acquisition technique using the proposed SAR-based quantizer was the enabling factor for NC implemented in the CT domain. Mismatch in the SAR DAC capacitor array was mitigated with a proposed chopper stabilization method. In addition, CM mismatch between the SAR differential inputs and the integrator summing inputs was resolved by a proposed FDCSC technique that is adaptive to CM differences. The input dynamic range achieved a differential pk-pk voltage of 2V even at the ultra-low supply of 1V considering such a high resolution design target. The modulator achieved a measured DR/SNR/SNDR of 103.1dB/100.1dB/95.2dB while dissipating 0.8mW.

In the overall conclusion, the system level proposals have enabled a more seamless development and verification in the architectural design phase, reducing much of the optimization iterations required.

The research into various modulator non-ideality sensitivities reveals useful information in making structural decisions. The research, design and development of the two modulators discussed various techniques employed to solve issues in order to push the performance required for high fidelity audio applications.

7.2 Research Achievements

In line with the research objectives, the achievements in the research are summarized here. To meet the objectives, both simulation and actual development of the prototypes are carried out. The simulators utilized include MATLAB, Cadence SPECTRE and the prototypes are built in 180nm and 65nm standard CMOS technologies from Global Foundries (GF).

- i. The optimization of the CT $\Delta\Sigma$ modulator can be a tedious process due to the interaction of many parameters such as the active components bandwidth, gain, noise, distortion and not to mention many other system level non-idealities like the jitter and process variations, etc. Since the CT $\Delta\Sigma$ modulator is a non-linear system, it becomes hard to obtain the best trade-offs between performance, power and area. This work proposed a circuit-based model in a high level simulator tool, MATLAB, which models the actual circuit, therefore serving two important objectives. Firstly, it enables quick assessment of the system level performance and sensitivity to a design parameter.

Secondly, the transition to the actual circuit design in Cadence can be expedited since the verification and hence iteration in Cadence can be extremely time-consuming. A 4th order CT $\Delta\Sigma$ modulator with single loop feedback of a Cascaded Integrators Feed Forward (CIFF) architecture is realized for proof of concept.

- ii. This work examines the performance of the CT $\Delta\Sigma$ modulator sensitivity to clock jitter. Extending the results shown in [7] whereby the main feedback DAC jitter is modelled with a Jitter Impulse Response (JIR) that interacts with the filter Loop Transfer Function (LTF), with the model developed; it can be seen that the jitter

performance degrades more rapidly with increased order for a NRZ pulse. This proves that the conventional technique using a fixed ON time on a RZ feedback pulse may become less effective as a result of the uncertainty in sampling at the quantizer.

- iii. It is desirable to reduce the area and power consumption of the flash converter architecture used in multibit design. This is mainly because of the exponential increase in comparator numbers with bit length. This work proposed a fast detect technique by sensing the Active Comparison Region (ACR) along the chain of comparators on the fly which is even applicable for large bandwidth high speed designs. The method detects redundancies in the comparators and quickly disables them to save power. Based on simulations, this technique achieved an improvement in the efficiency of the 4b internal quantizer by 72.4%. The advent of multibit CT $\Delta\Sigma$ modulators in low to moderate bandwidths can also benefit from this work.
- iv. A 4th order single loop, single bit CT $\Delta\Sigma$ modulator with CIFF architecture was developed with the following achievements:
 - The power consumption of moderately high 4th order architecture was evaluated with the inherently linear single bit feedback DAC. The CT $\Delta\Sigma$ modulator achieved a power consumption of only 153 μ A including a jitter immunity enhancement circuitry at a supply of 1.5V. Based on simulations, the maximum SNR/SNDR achieved was 87.1dB/85.4dB with an Oversampling ratio (OSR) of 64. The input dynamic range achieved a peak to peak fully differential voltage of 2V comparable to 5V supply designs.

- A combination of opamp RC and Transconductance-Capacitance-based (gmC) integrators filter structure is proposed with the exploitation of the output versatility of the gmC cell. The opamp-RC integrator is utilized only for the first stage to maintain modulator overall linearity. The consecutive gmC integrators are further shared and optimized for area and power savings. As compared to the well-known capacitive feed forward technique, the proposed gmC-based methodology relaxes the loading on the active integrators that demands power for drivability. This 4th order filter structure consisted of 1 opamp-RC and 3 gmC integrators.
 - A high precision Process Variation Tolerant Enhancement (PVTE) circuitry was proposed and developed to mitigate technological sensitivity of the modulator. The PVTE circuitry only requires a one shot calibration during startup and achieved a process variation detection accuracy of up to 2.08% based on Cadence process corner postlayout simulations.
 - The analysis and development of the single bit comparator for an adder-less transition from the filter output to the quantizer. The comparator input capacitance variation is minimized with a low gain preamp stage that caters to a Maximum Stable Amplitude (MSA) of single ended amplitude of 500mV with capacitance fluctuation of only <1fF to prevent degradation of modulator linearity as a result of signal dependent loading capacitance fluctuation. Hence coefficient variation at the last integrator is avoided.
- v. A high performance pseudo 3rd order, five bit SAR-based noise-enhancing quantizer CT $\Delta\Sigma$ modulator with a single loop CIFF architecture was proposed and developed with the achievement of the following:

- A 5b SAR-based ADC is proposed within the pseudo 3rd order CIFF loop filter as both the internal quantizer while coupling up for quantization noise acquisition. This technique aptly collects its conversion residue stored on the top plates of the capacitive re-distributive DAC of an SAR-based quantizer and injects backwards into the 2nd order filter front end for NTF enhancement by an extra order, hence named as pseudo 3rd order. This enabling methodology allows noise coupling, typically applied only in Discrete Time (DT) applications, to now be possible in a Continuous-Time (CT) modulator. It mitigates the necessity of heavy quantizer input sampling for signal difference and feedback, hence minimizing on kickback noise that is detrimental to modulator linearity. The SAR architecture also relaxes the power requirements in the quantizer as compared to a flash ADC implementation, which would require a total of 32 comparators for a 5b design. The modulator is sampled at an OSR of 128 for a bandwidth of 25kHz. The input dynamic range achieved a differential pk-pk voltage of 2V even at an ultra-low supply of 1V considering such a high resolution design target. The modulator achieved a measured DR/SNR/SNDR of 103.1dB/100.1dB/95.2dB while dissipating 0.8mW.
- The capacitive mismatch of the differential sampling capacitors in the SAR can create erroneous conversion outputs. Such errors could be large if committed during initial MSB determination. A technique for the calibration of the capacitors is proposed. The top plates of the differential are first tuned without the Noise Coupling (NC) protocol. The mismatches are then transferred to the tunable NC feedback capacitors. The deliberate mismatches on the NC capacitors are later averaged off via a chopper stabilization scheme. This

technique mitigates mismatches without resorting to redundancies which requires extra processing time and logics.

- The NC capacitive feedback enables the NTF enhancement scheme. However, due to the common mode voltage mismatches between the SAR differential lines and the 2nd integrator summing node, the performance of the NC protocol can be jeopardized without having a high performance active 2nd integrator. To curb that, an adaptive Floating Differential Charge Storage Capacitor (FDCSC) coupling method is proposed. With this technique, mismatches in the Common Mode (CM) voltage is automatically adapted within the NC capacitors, hence relaxing on Integrator 2 performance requirements.
- This design also achieves minimal reference dependency. Besides the 1V overall modulator supply, only an additional 500mV is required for reference. As such, it fulfills the requirements for a highly integrated SoC audio codec chipset, whereby, CT quiet sampling reduces the channel crosstalk; low supply characteristic enables usage of advance CMOS technologies; efficient and quiet enhancement of NTF pushes SNR towards high fidelity audio specifications and minimal reference dependency relaxes overall system biasing considerations.

7.3 Future Works

Due to constrain of resources, there remains plenty of area for exploration even for audio applications. In addition, it is also interesting for an extension of CT $\Delta\Sigma$ modulator application in DT dominated applications.

- i. In the field of high fidelity audio applications, with technological advancement, supply voltages will inevitably be decreased further. Utilizing high order architecture will become obsolete if condense SoC integration remains the priority of chip developers with the down scaling of product form factors. To achieve high resolution, aggressive increase in OSR and internal quantizer bits will not be efficient. The energy used to decrease noise is spread across a large bandwidth, hence resulting in an increase in power dissipation of supporting active components. However, there still exists a methodology to increase the order of noise shaping without the compromise in stability. It is the use of the MASH architecture.

However, this technique remains an area still to be researched before attaining the maturity level sufficient before achieving the industrial stability required. The main problem remains in the leakage of noise due to the matching between the cascading stages. If possible to resolve these issues, this topology can potentially reach a very high dynamic range at low supplies while remaining stable at a high MSA.

- ii. In the development of microphones for instrumentation application, the change in temperature can affect the tension of the diaphragm. This change in temperature can result in the fluctuation in the microphone sensitivity which may warrant the calibration of the instrument. To enable compensation to temperature changes, it is necessary to incorporate a temperature sensor within the microphone chipset. To do that, it is therefore advantages to have an ADC that can be multiplexed to do temperature sensing. To enable that, the temperature sensor architecture can be researched together with the ADC for a

digital temperature sensing system. In general, state-of-the-art temperature sensors utilize biased BJT for the generation of a linearly varying ΔV_{be} component with temperature as the sensor reference. Conventional temperature sensors still employ DT $\Delta\Sigma$ modulator as their ADC workhorse. For this, the input sampling capacitors acquire a voltage from a PTAT biased BJT in two phases. However, if a CT $\Delta\Sigma$ modulator is used, the PTAT current can be directly passed into the ADC for conversion, hence saving an additional stage of current to voltage conversion.

However, there remain areas for research especially in circuit producing the PTAT current which can be very sensitive to process corner variations. Nevertheless, this can be one area of application where the employment of a CT $\Delta\Sigma$ modulator with a better power efficiency can be deployed for a potential break through.

The research into this topic has resulted in the filing of several patents generally in remote temperature sensing applications [1-3]. In fact, there had been gathering interest to research into CT modulators for its quiet operation to eliminate EMI and cross coupling issues.

7.4 Research Publications

The result of the research has led to the publications of the below journals and conference papers as listed below:

Conference Papers:

1. Yoon Hwee Leow, Fan Zhang, Li Lian Teh, Siek, L. “A circuit based behavioral modeling of Continuous-Time Sigma Delta modulators”, *Integrated Circuits (ISIC), Proceedings of the 12th International, Symposium on, IEEE*, pp.109-112, 2009.
2. Yoon Hwee Leow; Siek, L. “ A high speed tracking quantizer for Continuous-Time multi-bit sigma delta modulators”, *Circuits and Systems (APCCAS), Asia Pacific Conference on, IEEE*, pp.776-779, 2010
3. Seong-Jin Kim; Ng, S.S.Y.; Wee, D.; Yoon Hwee Leow; Fan-Yung Ma; Sie Boo Chiang “High accuracy remote temperature sensor based on BJT devices in 0.13 μ m CMOS”, *Integrated Circuits (ISIC), Proceedings of the 14th International, Symposium on, IEEE*, pp.408-411, 2014.

Journal Papers:

1. Yoon Hwee Leow, Tang Howard, Zhuo Chao Sun, Siek, L. “A 1V 103dB Pseudo 3rd Order Audio Continuous-Time $\Delta\Sigma$ ADC with Enhanced Noise Shaping in 65nm CMOS”, *Solid-State Circuits, IEEE Journal of*, DOI: 10.1109/JSSC.2016.2593777, 2016.

7.5 References

- [1] Yoon Hwee Leow, et al, “Remote Temperature Sensing – Temperature Measurement over diode with Parasitic Cancellation,” U.S. Patent 14/286,482; CN 201510175816.2, Jan 2014
- [2] Yoon Hwee Leow, et al, “Remote Temperature Sensing – Reference Invariant Remote Temperature Sensing Functionality,” U.S 14/321,581, Feb 2014
- [3] Yoon Hwee Leow, et al, “A Pin Conservative, Reference Invariant Multiple Remote Temperature Sensing Technique with Thermistors,” U.S. Patent 201550521, Dec 2014

APPENDIX

Appendix 1

MATLAB Code for Generation of Coefficients for 4th Order CIFF CT $\Delta\Sigma$ modulator

```
%*****
% Global variables
% %*****
**
% This code generates the coefficients for a 4th order CIFF CT Sigma
Delta
% with 1Ts Excess Loop Delay Compensation

fprintf(1, 'Synthesizing NTF....\n');
Fin = input('Fin=');
Amp = input('Input amp=');
order = input('order=');
OSR = input('OSR=');
opt = input('optimize zeros=');
Hinf = input('OOB gain=');

%%%*****%%%
%%%Synthesize NTF%%%
%%%*****%%%

H=synthesizeNTF(order,OSR,opt,Hinf)
plotPZ(H);
f=linspace(0,0.5,100);
z=exp(i*2*pi*f);

figure(2);

bode(H, '-. ');
grid on;
hold on;

%%%*****%%%
%%%Compute LTF    %%%
%%%*****%%%

fprintf(1, 'Calculating L1(z) for HL1....\n\n');
HL1=1/H-1
bode(HL1, '-. ');
hold on;

% Remove 1 CLK Delay

fprintf(1, 'Removing 1 clk delay for HL1_ND....\n\n');
HL1_ND=HL1*(tf([1,0],[1],1,'Variable','z'))
figure(3);
bode(HL1, '-. ');
hold on;
```

```

bode(HL1_ND, '-. ');
grid on;

tfsys=tf(HL1_ND)
[num_HL1ND,den_HL1ND]=tfdata(HL1_ND);
num_HL1ND{1}
den_HL1ND{1}

% Derivation of DIrect Feedback Coefficient for ELD

k=num_HL1ND{1}(1)

num_A=num_HL1ND{1}(1);
num_B=num_HL1ND{1}(2);
num_C=num_HL1ND{1}(3);
num_D=num_HL1ND{1}(4);
num_E=num_HL1ND{1}(5);

den_A=den_HL1ND{1}(1);
den_B=den_HL1ND{1}(2);
den_C=den_HL1ND{1}(3);
den_D=den_HL1ND{1}(4);
den_E=den_HL1ND{1}(5);

num_A_temp=(num_A*(-1)*(den_B))+num_B;
num_B_temp=(num_A*(-1)*(den_C))+num_C;
num_C_temp=(num_A*(-1)*(den_D))+num_D;
num_D_temp=(-1)*num_A;

fprintf(1,'Formulating the transfer function for D2C
transform...\n\n');

HL1ND_D2C=tf([0,num_A_temp,num_B_temp,num_C_temp,num_D_temp],[den_A,d
en_B,den_C,den_D,den_E],1)

[num_D2C,den3_D2C]=tfdata(HL1ND_D2C,'v');
[num_ct_nrz_tmp,den_ct_nrz_tmp]=d2cm(num_D2C,den3_D2C,1)

a1=sym('a1');
a2=sym('a2');
a3=sym('a3');
a4=sym('a4');
c1=sym('c1');
c2=sym('c2');
c3=sym('c3');
c3=sym('c4');
b1=sym('b1');
g1=sym('g1');
g2=sym('g2');

[a1 a2 a3 a4 b1 c1 c2 c3 c4 g1
g2]=solve('b1=1','c1=1','c2=1','c3=1','c4=1','g1=0',...
'a1*c1=num_ct_nrz_tmp(2)','a2*c1*c2=num_ct_nrz_tmp(3)','a1*c1*c4*g2+c
1*c2*c3*a3=num_ct_nrz_tmp(4)',...

```

```
'a2*c1*c2*c4*g2+c1*c2*c3*a4=num_ct_nrz_tmp(5)', 'g2*c4+g1*c2=den_ct_nrz_tmp(3)', 'g1*g2*c2*c4=0')

% Printing out the Calculated Coefficients

k_coeff=[eval(a1),eval(a2),eval(a3),eval(a4),eval(b1),eval(c1),eval(c2),eval(c3),eval(c4),eval(g1),eval(g2)]

a1=k_coeff(1,1);
a2=k_coeff(1,2);
a3=k_coeff(1,3);
a4=k_coeff(1,4);
b1=k_coeff(1,5);
c1=k_coeff(1,6);
c2=k_coeff(1,7);
c3=k_coeff(1,8);
c4=k_coeff(1,9);
g1=k_coeff(1,10);
g2=k_coeff(1,11);
```

Appendix 2

MATLAB Code for Generation of Coefficients for 2nd Order CIFF CT $\Delta\Sigma$ modulator

```
%
*****
***
% Global variables
%
*****
***
% This code generates the coefficients for a 2nd order CIFF CT Sigma
Delta
% with 1Ts Excess Loop Delay Compensation

fprintf(1,'Synthesizing NTF....\n');
order = input('order=');
OSR = input('OSR=');
opt = input('optimize zeros?');
Hinf = input('OOB gain=');

%%%*****%%%
%%%Synthesize NTF%%%
%%%*****%%%

H=synthesizeNTF(order,OSR,opt,Hinf)
plotPZ(H);

%%%*****%%%
%%%Compute LTF    %%%
%%%*****%%%

fprintf(1,'Calculating L1(z) for HL1....\n\n');
HL1=1/H-1;
bode(HL1,'-s');
hold on;

% Remove 1 CLK Delay

fprintf(1,'Removing 1 clk delay for HL1_ND....\n\n');
HL1_ND=HL1*(tf([1,0],[1],1,'Variable','z'))
figure(3);
bode(HL1,'-s');
hold on;
bode(HL1_ND,'-s');
grid on;

tfsys=tf(HL1_ND);
[num_HL1ND,den_HL1ND]=tfdata(HL1_ND);
num_HL1ND{1};
den_HL1ND{1};
```

```

% Derivation of Direct Feedback Coefficient for ELD

k=[num_HL1ND{1}(1)]/[den_HL1ND{1}(1)];

num_A=num_HL1ND{1}(1);
num_B=num_HL1ND{1}(2);
den_A=den_HL1ND{1}(1);
den_B=den_HL1ND{1}(2);
den_C=den_HL1ND{1}(3);

num_A_temp=(num_A*(-1)*(den_B))+num_B;
num_B_temp=(num_A*(-1)*(den_C));

fprintf(1,'Formulating the transfer function for D2C
transform...\n\n');

HL1ND_D2C=tf([0,num_A_temp,num_B_temp],[den_A,den_B,den_C],1);

[num_D2C,den3_D2C]=tfdata(HL1ND_D2C,'v');
[num_ct_nrz_tmp,den_ct_nrz_tmp]=d2cm(num_D2C,den3_D2C,1);

[a1 a2 b1 c1 c2]=solve('b1=1','c1=1','c2=1',...
'a1*c1=num_ct_nrz_tmp(2)','a2*c1*c2=num_ct_nrz_tmp(3)');

k_coeff=[eval(a1),eval(a2),eval(b1),eval(c1),eval(c2)];

% Printing out the Calculated Coefficients

a1=k_coeff(1,1)
a2=k_coeff(1,2)
b1=k_coeff(1,3)
c1=k_coeff(1,4)
c2=k_coeff(1,5)
k

```


Appendix 3

MATLAB Code for Calculation of SNR from a digital bit stream

```
%
*****
***
%   Calculates SNR and PSD of the bit-stream and of the signal
%
*****
***

% Simulation of Modulator Under Test

sim('CT_CIFF_MOD2_Model');

w=hann_pv(N);
f=Fin/Fs;           % Normalized signal frequency
fB=N*(bw/Fs);       % Base-band frequency bins
yy1=xout(1000:999+N);
yy2=yy1';

ptot=zeros(1,N);
[snr,ptot]=calcSNR(yy2,f,1,fB,w,N);
snr
Rbit=(snr-1.76)/6.02;% Equivalent resolution in bits
Rbit
figure(6);
clf;
plot(linspace(0,Fs/2,N/2), ptot(1:N/2), 'r');
grid on;
title('PSD of a 2nd-Order Sigma-Delta Modulator')
xlabel('Frequency [Hz]')
ylabel('PSD [dB]')
axis([0 Fs/2 -200 0]);
```

Appendix 4

MATLAB Code for Parameter Sweep Analysis

```
% This Code Sweeps 4 Parameters within a Model between -20% to 20%

fs=3200000
N=8192;
Ts=1/fs;
bw=25e3;
fb=ceil(N*bw/fs);
f=Fin/fs;
scale2=zeros(20);
SNR_db=zeros(20);
db=0;
sim_no=0;

% Setting up Loop for Sweeping from -20% to 20% of 4 Parameters

for y=linspace(0.8, 1.8, 20)
    param1=y*(200000)
    param2=y*(1000000)
    param3=y*(7.5e-12)
    param4=y*(1000000)
    sim('CT_CIFF_MOD4_test');

    w=hann_pv(N);
    y1=vout(100:999+N);
    y2=y1';

    ptot=zeros(1,20);
    [SNR_db ptot]=calcSNR(y2,f,1,fb,w,N);
    i=db+1;
    db=db+1;
    scale2(i)=SNR_db;
    SNR_db
    sim_no=sim_no+1;

end

Parameter_variation=(linspace(-0.2,0.8,20))*100
plot(Parameter_variation, scale2, 'b');
```