Copper nanowires bonding for three dimensional interconnections

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NANYANG
TECHNOLOGICAL
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**COPPER NANOWIRES BONDING FOR THREE
DIMENSIONAL INTERCONNECTIONS**

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

2016

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partial fulfilment of the requirement for the degree of Doctor of
Philosophy

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Abbreviations

AAO	Anodic Aluminium Oxide
ACF	Anisotropic Conductive Film
BEOL	Back-End-of-Line
CNT	Carbon Nanotubes
EELS	Electron Energy Loss Spectroscopy
FIB	Focused Ion Beam
FPFC	Fine Pitch Flip-Chip
IMC	Intermetallic Compound
NW	Nanowire
SAED	Selected Area Electron Diffraction
SEM	Scanning Electron Microscopy
TC	Texture Coefficient
TCB	Thermocompression Bonding
TEM	Transmission Electron Microscopy
TSV	Through-Silicon Via
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

Abstract

Over the past few decades, the semiconductor industry has been advancing by increasing transistor density on a microchip through continuous device scaling based on the technology roadmap driven by Moore's Law. However, new physical phenomena at scaled dimensions and fundamental limitations in material properties are pushing the limits of existing planar devices. Moreover, interconnect delay, bandwidth and power dissipation are increasingly dominating the integrated circuits' (IC) performance. Hence, a paradigm shift from the present IC architecture is needed to overcome the saturation in chip performance.

Three dimensional (3D) integration has emerged as one of the promising techniques to overcome Moore's Law, by replacing long horizontal wires with short vertical interconnects. This has resulted in smaller form factor, a reduction in RC (resistance-capacitance) delay and allows integration of heterogeneous systems with diverse functionality catering to "More than Moore" technology. However, 3D packaging which involves stacking of devices through the use of solder bumps or solder capped copper (Cu) pillar bumps, is facing challenges due to scaling down and reliability issues. In this work, fabrication of Cu nanowires (NWs) arrays coupled with thermocompression bonding is proposed as an alternative to existing 3D interconnection approaches.

To explore the feasibility of adopting this alternative 3D interconnection, main emphasis is placed on the process development of the Cu NWs arrays on Si substrate and characterization of these bonded NWs arrays. The diameter of Cu NWs can be controlled by varying the anodization voltage, electrolyte type or pore widening duration during the fabrication of the porous alumina template. Growth of Cu NWs with preferred texture can be obtained by manipulating the electrodeposition conditions such as voltage and temperature. The use of different metal interlayers on the substrate influences the NWs density and subsequent processes. Characterization of the Cu NW revealed smooth and continuous morphology with preferred crystal growth orientation in [111] direction.

The second part of the research focuses on the bonding of Cu NWs arrays. At low bond temperature of 200°C, NW-Film and NW-NW bonding exhibit higher average shear strength than that of Film-Film bonding. However, scanning electron microscope (SEM), transmission electron microscope (TEM) and electron energy-loss spectroscopy (EELS) characterizations revealed that the Cu NWs have transformed into Cu oxide nanotubes. Further investigations show that the transformation was a result of Nanoscale Kirkendall Effect due to the low vacuum environment during bonding. Different annealing treatments on the NWs arrays also revealed that multiple voids form initially in the Cu NWs, with further growth through surface diffusion of Cu atoms along the voids' surface which eventually leads to a hollow core.

To overcome Cu oxide nanotube formation, another set of experiments was carried out using a commercial bonder with a high vacuum environment. Experimental results show that Nanoscale Kirkendall Effect can be suppressed. Moreover, increasing bond pressure or bond temperature resulted in a greater average shear strength and lower specific contact resistivity. Given an adequate NW density and bond pressure, the NWs are able to interlock with one another which increases the contact area between the NWs arrays, thus enhancing Cu interdiffusion. NWs bonding at 200°C resulted in a continuous film with indistinguishable bond interface. TEM EELS mapping analysis shows that the bond nature is mainly Cu with small amount of oxygen distributed evenly across the bonded area.

In conclusion, high density Cu NWs arrays on Si substrate can be achieved by optimizing the alumina anodization condition and electrodeposition of the Cu NWs. Using the Cu NWs as a bonding medium, Cu-Cu bonding can be achieved at a low temperature of 200°C, which is desired for compatibility with back-end-of-line (BEOL) processing conditions. Moreover, growth of NWs arrays using anodized alumina template method allows patterning into small columns with flexibility in adjusting the interconnect pitch. Thus, Cu NWs arrays coupled with thermocompression bonding may be an alternative 3D interconnection approach to overcome the challenges in process integration.

Chapter 1

Introduction

Over the past five decades, complementary metal-oxide-semiconductor (CMOS) device scaling has been the primary driver of the microelectronics industry for enhanced system performance and higher productivity in keeping pace with the prediction given by Moore's Law. Moore's Law is coined by Gordon E. Moore who stated that transistor density per chip would double every year in his 1965 paper [1], which was later revised to every two years in 1975 [2]. However, continuous increment in transistor density creates a big challenge in data communication with a microprocessor which has over one billion transistors. As a result, interconnects from the chip to the system have to rapidly grow in number as well and this has become a serious concern in terms of scaling and reliability issues. Moreover, interconnect delay, bandwidth and power dissipation are increasingly dominating the IC performance. Hence, a paradigm shift from the present integrated circuits (IC) architecture is desired to overcome the saturation of chip performance [3].

1.1 Background and Motivation

Three-dimensional (3D) integration has emerged as a potential solution to the challenges faced due to “More Moore” scaling. It also allows heterogeneous system functionality within a package, catering to the needs of “More than Moore” technology. Figure 1.1 shows a schematic diagram of System on Chip (SoC) which demonstrates heterogeneous integration of various functionalities. Stacking of active devices in the vertical direction in addition to the conventional horizontal planar structure enables replacement of long horizontal wires with short vertical interconnects (Figure 1.2). This in turn boosts the device performance through reduced area, power consumption and delay, while achieving smaller form factor.

Figure 1.1 Comparison Schematic diagram of a 3-D SoC [3]

Figure 1.2 Comparison of chip footprint, wire length and distribution between 3-D and 2-D systems [3]

3D integration can be separated into four different categories of interconnection which includes 3D packaging, processed wafer or chip bonding, monolithic stacking and self-assembled devices. Among these categories, 3D packaging is a fairly mature technology which involves wire-bonding or solder bump interconnection. However, increased interconnect density is pushing the limits of scalability of solder bump.

Interconnect which provides power, electrical and mechanical contact between the chip and substrate or interposer is termed as chip-to-substrate (chip-substrate) interconnect. Two common types of chip-substrate interconnect schemes in the current market are wire-bonding and flip-chip solder bumps/micro-bumps (refer to figure 1.3). Due to advantages such as higher feature density and shorter interconnect distance, flip-chip solder bumps (typically lead-free tin-based) has emerged as a widely used off-chip interconnection. However, solder bump poses problems in scalability such as low standoff height and reaching its pitch limitation ($\sim 140\text{ }\mu\text{m}$) [4] (refer to figure 1.4). It also shows incompetency in terms of electrical and reliability performance. For instance, a solder bump of $50\text{ }\mu\text{m}$ in diameter has a current density limit in the order of 10^4 A/cm^2 , with exceeding current density posing a serious reliability problem in terms of electromigration [5]. According to the International Technology Roadmap for Semiconductors (ITRS) [6], a new generation of chip-substrate interconnect is thus necessary to overcome the challenges. It has also been pointed out in ITRS [6] that nanomaterials such as nanowires or nanotubes are required to meet future packaging requirements (refer to figure 1.5).

Figure 1.3 Two common types of chip-substrate interconnects are a) wire-bonding and b) flip-chip solder bumps

Figure 1.4 Schematic diagram of flip-chip solder bumps showing the standoff height and pitch.

Figure 1.5 Schematic diagram of a package with the use of nanomaterials to meet future requirements [6]

As device scaling is pushing the limits of current solder bump technology, alternative interconnects have been introduced from both industries and academic groups. In July 2010, Amkor Technology and Texas Instruments announced that they had qualified and begun production of the industry's first fine pitch copper (Cu) pillar flip-chip packages [4, 7]. By replacing the solder bumps with solder capped Cu pillars, bump pitch has shrunk up to 300% [7]. Solder capped Cu pillars may be a good alternative to solder bump in terms of resolving the scalability issue. However, it has its limits in thermo-mechanical reliability and electrical conductivity. The true capability of Cu pillar is limited by the properties of solder cap as brittle Cu-Sn intermetallics can be formed at the interface. A better solution would be to drive towards a solderless interconnection such as direct Cu-Cu bonding. Table 1.1 shows a comparison among the 3 types of 3D interconnections.

As seen from Table 1.1, Cu-Cu bonding has its advantages of scalability, lower electrical resistivity and superior thermo-mechanical reliability as compared to solder

bump and solder capped Cu pillar. Being a solderless interconnection, brittle intermetallics can be avoided and it has greater electromigration resistance than solder. This improves the quality and reliability of the bond. However, it requires higher bond temperature and bond pressure during the bonding process in order to achieve a high bonding quality. High bond temperature is undesirable as prefabricated devices may be sensitive to high processing temperature. Besides thermal budget limitation, low bond temperature is preferred due to better post-bonding thermo-mechanical stress control and reduction in bond misalignment. As such, Cu nanowires (NWs) arrays bonding is proposed to overcome the relatively high bond temperature of Cu-Cu bonding.

Table 1.1 Advantages and disadvantages of solder bump, solder capped Cu pillar and Cu-Cu bonding

Characteristics	Types of 3D Interconnection					
	Solder bump		Solder capped Cu pillar		Cu-Cu bonding	
Bond Temperature	Low	😊	Low	😊	High	😞
Bond pressure	Low	😊	Low	😊	High	😞
Scalability	Poor	😞	Moderate	😐	Good	😊
Electrical resistivity	High	😞	Moderate	😐	Low	😊
Mechanical reliability	Poor	😞	Poor	😞	Good	😊

Cu NWs arrays coupled with thermocompression bonding (figure 1.6) is proposed as an alternative to replace flip-chip solder bumps or solder capped Cu pillars. In comparison with solder bumps, high aspect ratio NWs are scalable and capable of increasing the standoff height. Cu NWs arrays are also better electromigration resistant and have higher redundancy to fail. Large surface area to volume ratio enables the NWs to have better heat dissipation than bumps. Parallel arrays of NWs allow shunting of current away from higher resistance NWs, thus improving the lifetime. By applying Cu-Cu bonding, solderless interconnection can be achieved which eliminates the formation of brittle copper-tin intermetallics during reflow that can compromise its thermo-mechanical

reliability. Furthermore, high surface area to volume ratio feature enables Cu NWs to undergo pre-melting (or surface melting) at temperatures much lower than its bulk melting point as reported by Tansel Karabacak [8]. As a result, bonding temperature can be reduced which is desirable for compatibility with BEOL processing conditions and reduction in thermal mismatch to ease bond misalignment. Electrical and mechanical study of Cu NWs arrays bonding, which have yet been investigated in detail in the current research field, will also be focused in this thesis.

Figure 1.6 Schematic diagram of proposed Cu NWs arrays interconnect. (a) NWs arrays bonded to film, (b) NWs arrays bonded to NWs arrays.

The proposed chip-substrate Cu NW interconnect structure would need encapsulation such as underfill to prevent Cu oxidation and improve thermo-mechanical reliability. However, underfill needs to be less viscous to fill into the nanosized porous Cu NW bonding structure. This is another important aspect which can be addressed in a separate study. One possible way to reduce the porosity of the Cu NWs bonding is to increase the NW density through interference lithography as discussed in the future work (Chapter 7.2.2).

1.2 Research Objectives and Scope

The overall objective of this research is to demonstrate low temperature Cu-Cu bonding through the use of nanowires for chip-substrate interconnection. To explore the feasibility of adopting this alternative chip-substrate interconnection, the main research scope is as follows:

- Process development on the synthesis of Cu NWs arrays on Si substrate that are compatible with IC fabrication technology, and Cu-Cu thermocompression bonding using these NWs arrays.
- Establish the relationship between the bonding parameters such as temperature, pressure, duration, environment and configuration with the mechanical and electrical properties of the bonded joint.
- Propose the mechanism of Cu NWs bonding under the different conditions.

1.3 Summary of Chapters

The thesis begins with an introduction on the background and motivations which includes the objectives and scope of this work in Chapter 1. This is followed by a concise literature review (Chapter 2) on the chip-substrate interconnect technologies, the theory behind the Anodized Aluminum Oxide (AAO) template formation and various bonding technologies. Chapter 3 highlights the research methodology employed to characterize the experimental results and overall flow of the work. The results and discussion of this research is divided into 3 main chapters. Chapter 4 explores the process development of Cu NWs arrays on Si substrate through discussion on the control of NW diameter, use of different interlayers and electrodeposition conditions. Chapters 5 and 6 investigate on the NWs arrays bonding mechanisms in low vacuum and high vacuum environments, respectively. In both chapters, effects of different bonding conditions that affect the bond shear strength and contact resistivity are studied. The contributions of the thesis and future recommendations are summarized in Chapter 7.

1.4 References

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Chapter 2

Literature Review

From Chapter 1, we understand that an alternative chip-substrate interconnection is required as transistor continues to scale down with a tremendous increase in input/output (I/O) density. In this chapter, various types of chip-substrate interconnect technologies, from existing ones to on-going researched alternatives, will be discussed. As anodic aluminium oxide (AAO) template is used as a mean to fabricate the Cu NWs arrays, a brief introduction on the AAO template and its growth mechanism is presented. In this work, we are using Cu NWs arrays as a replacement of solder bumps between the chip and substrate to form a mechanically strong electrical interconnection via thermocompression bonding. As such, Cu-Cu thermocompression bonding will also be highlighted.

2.1 Chip-Substrate Interconnect Technologies

The main functions of a chip-substrate interconnect is to provide an electrically and mechanically stable contact between the chip and substrate. Wire-bonding has traditionally been adopted to connect the chips to the substrate or package level due to its low cost and simplicity. As I/O density increases and package footprint reduces, flip-chip area array solder ball attachment was introduced. As transistor further scales down, solder bumps can be replaced by solder capped Cu pillars to reduce the high current density and mechanical strain distribution. This will be discussed in more detail in section 2.1.1. Some of the current research on alternative chip-substrate interconnects by other groups will be presented in section 2.1.2.

2.1.1 Review on Existing Chip-Substrate Interconnections

In this section, existing interconnect technologies adopted by the industry will be outlined, especially on the transition from solder bump to solder capped Cu pillar technologies. Figure 2.1 shows an example of the solder capped Cu pillar.

Figure 2.1 Solder capped Cu pillar structure for chip-substrate interconnect. (a) Schematic diagram and (b) SEM image. [1]

2.1.1.1 Flip-Chip Solder Bump Technology

Prior to the introduction of flip-chip technology, wire-bonding was the earliest technique adopted in device assembly [2]. Due to its cost, unreliability and low productivity, flip-chip solder bump interconnection was developed in the early 1960s to overcome the drawbacks of manual wire-bonding [3]. The most prominent type of flip-chip solder bump was invented by IBM in 1960s known as Controlled Collapse Chip Connection (C4) [4]. A schematic diagram of the C4 package configuration is shown in figure 2.2. Flip-chip configuration has several advantages over the conventional wire-bonding technology. It allows self-alignment, higher I/O density, shorter interconnects, better heat dissipation directly through the back of the die and lower height profile. These lead to smaller footprint and thus higher throughput can be attained. Due to the numerous advantages, flip-chip solder bump technology has become one of the most attractive techniques in modern electronic packaging. These include multichip modules (MCM), three dimensional (3D) packaging and fiber optical assemblies. However, increased interconnect density is pushing the limits of scalability of solder bump.

Figure 2.2 Schematic diagram showing the generic configuration of C4 [4]

2.1.1.2 Flip-chip Solder Capped Copper Pillar Technology

Due to limitations in solder bump scaling and reliability issues, the industry is moving towards adopting solder capped Cu pillar technology. In year 2005, wireless device suppliers adopted flip-chip Cu pillar in RF power amplifier and front-end modules via package assembly suppliers such as Amkor Technology [5]. Figure 2.3 shows an

example of flip-chip Cu pillar bump in RF modules. The motivation of this adoption was mainly due to lower cost and better performance in terms of thermal and electrical stability which increased the final test yields [5].

Figure 2.3 Flip-chip Cu pillar bumps in RF module. [6]

In May 2006, Intel reported the adoption of Cu pillar bumps on Si-based CMOS devices [7]. Challenges were faced when integrating Cu pillar bumps into the device with fragile low-k interlayer dielectrics. However, Intel has successfully overcome the challenges and incorporated Cu die-side bumps mated to eutectic tin-lead package-side bumps (figure 2.4) for 65 nm node high volume manufacturing. This is done through numerical modeling where design features that were capable of modulating the amount of stress transferred to the underlying stack were being identified. This information could then be incorporated into the design to reduce transmitted stress to the fragile layers [7]. It was reported that these copper bumps led to improved electromigration resistance and thermal conductivity. Underbump metallization has also been simplified and higher I/O densities were achieved due to the reduction in critical bump dimensions.

Figure 2.4 Cross section SEM image of a Cu die bump mated to eutectic SnPb solder. [7]

Over the past few years, it had been reported that there was an evolution of the Cu pillar bump with solder attach structure on Intel devices. These Intel devices include personal computer chipsets, Atom CPUs and Core i5 32 nm CPU/GPU multichip package structures [8, 9]. In July 2010, Amkor Technology and Texas Instruments announced the delivery of the industry's first fine pitch flip-chip (FPFC) Cu pillar packages to the market [10]. The advantages of the FPFC Cu pillar packages include cost reduction, lead-free bump cap and outstanding electromigration performance. It also allows extreme fine pitch on Si substrates down to 40 μm for through-silicon via (TSV) and chip-to-chip flip-chip stacking. In addition, FPFC on laminate package can be down to 50 μm in line and 40/80 μm staggered bump pitches (figure 2.5).

Figure 2.5 Amkor FPFC Cu pillar package on package structure (left image) and 50 μm in line Cu pillar bump pitch cross section (right image). [10]

In October 2010, Xilinx announced [11] that they were on their way to volume production of the first field programmable gate array (FPGA) with stacked silicon interconnect technology. This involves the use of Amkor Cu pillar technology as microbumps (figure 2.6). All of the above show the rapid transition from conventional solder bumps to solder capped Cu pillar interconnect which is driven by cost and performance.

Figure 2.6 Cross section of 3D package architecture with Si interposer and microbumps (solder capped Cu pillar) by Xilinx. [11]

Although the industry's trend is moving from solder bumps towards fine pitch solder capped Cu pillar technology, there are still challenges ahead to be dealt with. These challenges include the problems associated with the solder cap of the Cu pillar. Solder capped Cu pillar forms brittle intermetallics which weaken the mechanical reliability of the bond.

2.1.2 Current Research on Alternative Interconnections

Besides the solder capped Cu pillar technology which is adopted by the industry, many research groups have been exploring and studying on alternative interconnections. In this section, two of the alternative interconnections using nanostructures will be discussed.

2.1.2.1 Carbon Nanotubes Off-chip Interconnect

The aim of using carbon nanotubes (CNT) is to tackle challenges faced as technology advances. These challenges include high current-carrying capacity, thermal management, I/O density and thermal-mechanical reliability [12]. CNT is chosen as a

potential candidate for off-chip interconnects due to their extraordinary electrical and mechanical properties. Reports have shown that metallic CNTs exhibit ballistic conductivity at room temperature [13, 14]. This enables CNTs to carry remarkable high currents ($> 10^9$ A/cm²) without electromigration failure [15]. It has been reported that the thermal conductivity of a single multi-walled CNT is measured to be more than 3000 W/m.K [16]. This value exceeds the conductivity of diamond (2000 W/m.K). As such, researchers are studying on the integration of CNTs for interconnect applications [17-19].

Three limiting factors towards the integration of CNTs into the off-chip interconnection are high CNT growth temperature (>600 °C), selective positioning of CNT bundles and poor adhesion between CNTs and substrates. Wong's group from Georgia Institute of Technology has come up with "CNT transfer technology" to overcome the above problems [12]. The distinct feature of this technology is to separate the high temperature CNT growth process from the CNT device assembly. Figure 2.7 shows the schematic diagram of the technology process flow. First, the open-ended multi-walled CNTs were grown at high temperature on patterned iron (Fe) catalyst layer. This resulted in well-aligned CNT bundles standing vertically on the substrate (figure 2.8). Second, the CNT bundles are transferred to another Cu substrate with solder paste and under bump metallization (UBM). This is a low temperature process since the solder reflow temperature peaked at 250°C. As these CNTs are open-ended, the adhesion between the CNTs and solders improved through strong capillary force that draws the molten solder paste inside the CNTs during the reflow process. As a result, fine pitch aligned CNT bundles can be achieved during device assembly at low temperature. However, the use of solder limits the electrical and mechanical performance of the interconnect as mentioned in Chapter 1.

Figure 2.7 Schematic diagram illustrating the “CNT transfer technology” process flow for assembling fine-pitch CNT bundles. [12]

Figure 2.8 SEM image showing well-aligned open-ended CNT bundles grown on Si substrate. [12]

2.1.2.2 Anisotropic Conductive Film using Metallic Nanowires

Besides the research on CNTs as off-chip interconnects, metallic NWs are also being explored. As flip-chip I/O pitch continues to scale down, the traditional anisotropic conductive film (ACF) containing micrometer sized conductive particles will face more challenges. As such, Lin *et al.* from ITRI [20, 21] replaced conductive particles with high aspect ratio silver-cobalt NWs. These NWs are highly ordered since they are electroplated through AAO template. With the aid of magnetic field, the NWs are highly directional

during the removal of AAO and polymer filling. As a result, the NWs are kept parallel while embedded inside the polymer film. In this way, the NWs ACF exhibits anisotropic conductance behavior. Figure 2.9 shows a schematic diagram of the process flow of NWs ACF.

Figure 2.9 Schematic diagram showing the process flow of nanowire anisotropic conductive film [21]

In addition to the above technique from ITRI, Stam *et al.* from Tyndall National Institute [22] introduced Cu NWs ACF which they called it as submicron wire ACF (SW-ACF). The process is less complicated as they use the polycarbonate template to electroplate Cu NWs as well as treating it as the final ACF without removal of the template. Heat is applied during the bonding to melt the polycarbonate template slightly to ensure good adhesion between the SW-ACF and substrate (figure 2.10). Figure 2.11 shows the SEM images of the embedded Cu NWs in the polycarbonate template and the final bonded SW-ACF test chip. One of the drawbacks mentioned in the article was the difficulty in removing the gold seed layer after Cu NWs electrodeposition.

Figure 2.10 Schematic diagram showing the bonding of SW-ACF to substrate [22]

Figure 2.11 SEM image (left) showing Cu NWs embedded in polycarbonate template and cross section SEM image (right) showing SW-ACF bonded onto a test chip [22]

2.1.2.3 Patterned Metallic Nanowires for Flip-Chip Interconnects

Sharma *et al.* demonstrated the fabrication of patterned micropads of nickel [23] and copper [24] NWs arrays on silicon substrate through AAO template as a proposed flip-chip interconnect scheme. The micropads were patterned using silicon dioxide (SiO_2) which also acts as an anodization barrier. The advantage of this method is that the synthesis of the NWs arrays is carried out using microfabrication techniques that facilitate easy integration of these nanodevices into standard silicon manufacturing. However, the solder reflow process resulted in the Cu_6Sn_5 intermetallic formation which is brittle and undesirable. All of the above suggest that a solderless interconnection is desired to eliminate the formation of intermetallics which may weaken the mechanical reliability of the bond.

Figure 2.12 Schematic illustrating the proposed interconnect scheme using micropads of metallic NW arrays [24]

2.2 Fabrication of AAO Template

In this section, an introduction to AAO template and its fabrication process is discussed. The nanopore growth mechanism and the principle behind the formation of regular hexagonal pore arrangement are briefly explained. The differences in the fabrication of AAO on a substrate involving additional interlayer are highlighted.

2.2.1 Introduction to AAO Template

AAO template formed by two-step anodization technique [25] is renowned for possessing uniform pore structure with hexagonal (or honeycomb like) arrangement of cylindrical channels (refer to figure 2.13a). The use of different types and concentration of electrolytes [26-28], voltages and anodic oxidation duration allows one to adjust the pore diameter D_p , interpore distance D_{int} and film thicknesses L_f in a wide range [29-31]. Figure 2.13b shows the indication of the various dimensions. In addition, D_p can also be further enlarged through the pore widening process. This tunable nanopore characteristic makes AAO template extremely attractive as a matrix for the synthesis of NWs. Thus, it can be used as a template to synthesize high aspect ratio nanostructures. Besides, incorporation of almost any conductive metallic compound into AAO matrix can be carried out by electrodeposition technique, enabling simple handling over anisotropy of nanostructures.

Figure 2.13 (a) Schematic diagram of ideal AAO structure grown on aluminium [32]. (b) AAO structure denoting the dimensions- D_p , D_{int} and L_f .

2.2.2 Two-Step Anodization

Masuda and Fukuda (1995) [25] reported that a highly ordered nanohole array can be obtained via a two-step anodization of high purity aluminum by applying a constant voltage of 40 V at 0°C in 0.3 M oxalic acid solution. During the initial first-step anodization, cell arrangement at the surface is not very regular. However, nanohole regularity improves with increasing film thickness [29]. Thus, longer period of first-step anodization is carried out to obtain excellent regularity. After first-step anodization, the AAO film is selectively wet etched away by the P-C etch (a mixture of 35 ml/l 85% H_3PO_4 and 20 g/l CrO_3 at 80 °C) established by Schwartz and Platter (1975) [33]. The post-etched aluminum surface leaves behind an ordered array of concave pits, which acts as the sites for deep pore growth during the second-step anodization. As a result, a nanohole array which exhibits excellent regularity is formed after the second-step anodization due to the initial surface created. Figure 2.14 is a schematic diagram of a typical alumina template approach where step A to D shows the sequence of how a two-step anodization is being carried out.

Figure 2.14 Schematic diagram showing two-step anodization of aluminium. [34]

2.2.3 Nanopore Growth Mechanism

In this section, interfacial reactions and the growth of vertical pore channels will be discussed. Nanopore growth mechanism can be described by the process of electrical field assisted dissolution. When the field-enhanced dissolution of the oxide at the electrolyte/oxide interface and the growth of oxide that occurs at the oxide/metal interface are in equilibrium, the pores will grow perpendicular to the surface [35].

According to Uchi *et al.* [36], oxidation occurs at the metal/oxide interface where oxygen containing ions (O^{2-} or OH^-) migrate from the electrolyte as dictated by the following reaction:

Oxide anions move inward to react with aluminum at the metal/oxide interface to form oxide.

At the same time, dissolution of the oxide layer is caused mainly by the hydration reaction of the formed oxide layer [37] as shown:

Al^{3+} ions drift through the oxide layer and are ejected into the solution at the oxide/electrolyte interface. Loss of Al^{3+} ions in the electrolyte has been found to be a prerequisite for porous oxide growth [38]. This contributes to the porous alumina layer.

Barrier oxide growth without pore formation occurs when the Al^{3+} ions reach the oxide/electrolyte interface and react with water to contribute to the oxide formation:

The schematic representation of the ionic migration at the pore bottom under the applied electric field is given in figure 2.15 [39]. The electrons ejected into the electrolyte would combine with hydrogen ions to generate hydrogen gas at the cathode.

Figure 2.15 Pore formation process in AAO. 1. Cell schematic with Al as anode. 2. Localized fields cause initial ordering. 3. Pores form field and temperature enhanced dissolution. 4. Pore growth through equilibrium condition at barrier oxide interface [39].

2.2.4 Self-Organized Formation of AAO

To date, self-organization of AAO has yet been satisfactorily identified. According to Jessensky *et al.* (1998) [40, 41], the atomic density of aluminium in Al_2O_3 is lower than that of metallic aluminium by a factor of two. This leads to volume expansion of Al_2O_3 that is nearly twice than that of the original aluminium metal. The volume expansion which takes place at the metal/oxide interface then leads to a compressive stress during oxide formation. This stress is the origin of the repulsive force that appears between the neighbouring pores which promotes the formation of hexagonally ordered pore arrangements.

On the other hand, Nielsch *et al.* (2002) [42] proposed that self-ordering of porous alumina is possible with any interpore distance if the applied voltage and the pH value of the electrolyte match the 10% porosity rule (figure 2.16). In general, applied voltage influences the interpore distance while pH value of the electrolyte defines the pore radius. Self-ordering of AAO occurs when the combination of voltage and pH conditions results in an AAO with porosity of 10%. The effect of the stress at the aluminum/porous alumina interface would be an essential part of these volume expansion explanations.

Figure 2.16 Transmission electron micrographs of hexagonal self-ordered AAO fabricated at (a) 25 V in 1.7 wt % H_2SO_4 , (b) 40 V in 2.7 wt % $(\text{COOH})_2$ [42].

2.2.5 AAO on Substrate

Shingubara *et al.* [43] was the first to study AAO formed on Si substrate in year 1999. Subsequent studies by Crouse *et al.* [44] and Chu *et al.* [45] found that the profile of the barrier oxide differs from the conventional scallop-shaped barrier oxide formed on Al (figure 2.17). Three types of pore bottom can be identified [46]. First, scallop-shaped barrier oxide is formed on Al foil or substrate (figure 2.18a). Second, inverted barrier oxide that arched at the pore bottom is formed when Al is completely anodized and reached the noble metal substrate (figure 2.18b). The reason for the formation of inverted barrier oxide will be discussed in the following paragraph. Third, oxide of the underlayer or interlayer penetrates the alumina barrier layer at the pore bottom and forms oxide hillocks (figure 2.18c). This oxide penetration phenomenon will also be discussed as below.

Figure 2.17 SEM micrographs of porous alumina nanohole bottom on (a) n-Si (Crouse *et al.*, 2000) [44] and (b) ITO (Chu *et al.*, 2002) [45].

Figure 2.18 Schematic diagrams of AAO formed on different underlayers [46]. (a) Scallop-shaped barrier oxide [47]; b) Inverted barrier oxide with a void at the pore bottom [47]; c) Oxide of the underlayer penetrates the alumina barrier layer at the pore bottom [48].

In the second case (figure 2.18b), oxygen is produced and accumulated at the alumina/substrate interface when the underlayer is inert. This eventually leads to a pressure build up against the pore bottom. As a result, the barrier layer is detached from the interface, leaving some voids beneath it. This accounts for the weak adhesion between the AAO and substrate [45]. In the third case, the underlayer oxide penetrates the alumina barrier oxide and forms oxide hillocks. This can happen when the underlayer metal used can be oxidized under Al anodization conditions and has an oxide with a higher ionic conductivity than alumina [46]. An example of such underlayer metal is tungsten. Figure 2.19 shows the cross section SEM images of the AAO pore channel profile before and after removal of tungsten oxide (WO_3) hillocks [46]. In this work, both inert noble metal (gold) and tungsten are used as the underlayers for AAO fabrication on substrate. Details will be elaborated under chapter 4.

Figure 2.19 SEM image of AAO in the third case. a) WO_3 hillocks form at the pore bottom. b) Selective removal of WO_3 that penetrates the pores. Scale bars correspond to 200 nm. [46]

2.3 Cu-Cu Thermocompression Bonding

There are four major types of bonding technologies in the market; direct oxide bonding, polymer adhesive bonding, solder (eutectic) bonding and copper-to-copper (Cu-Cu) thermocompression bonding [49]. Each of them has its pros and cons. For instance, both direct oxide bonding and polymer adhesive bonding can form good mechanical contacts at relatively low process temperature but they lack of the ability to provide electrical connection. As such, both solder and Cu-Cu thermocompression bonding have emerged as the more popular technologies due to their ability to provide mechanical support and electrical connection [50]. However, solder often leads to reliability problems due to the brittle intermetallic compound (IMC) formed. Thus, we adopt Cu-Cu thermocompression bonding method in this thesis work. One of the drawbacks for this method is the high bonding temperature (above 300°C) required to achieve a good bond [51, 52]. We aim to circumvent this restriction by replacing Cu thin film with Cu NW arrays. Since NW has a high surface area to volume ratio, we believe that it will aid the bonding process and thus lower the bonding temperature required [53].

Thermocompression Cu-Cu bonding for silicon wafer bonding is a promising approach for fabrication of three-dimensional (3D) integrated circuits, which is known to be a potential solution to scaling issues in CMOS circuits. This technology allows stacking of active devices in the vertical direction, which replaces long horizontal wires

with short vertical interconnects. Similarly, we are applying thermocompression bonding to our chip-substrate interconnection using Cu NW arrays.

Thermocompression Cu-Cu bonding (also known as diffusion Cu-to-Cu bonding) uses high pressure to hold two Cu surfaces of the wafers/chips at elevated temperatures. The heat and pressure allow the deformation of microscopic contact between two Cu regions, leading to increase in contact area. Under certain bonding temperatures, Cu atoms with enough thermal energy from the two surfaces can then diffuse into each other to finish the bonding process. The higher the bonding temperatures, the less strict requirements are needed for surface cleanliness and chamber vacuum conditions [54]. However, the bonding temperature has to be compatible with back-end-of-the-line (BEOL) process temperatures in order not to affect the device performance. In addition, low bond temperature is desired for reduction in thermal mismatch to ease bond misalignment. Figure 2.20 shows an example of thermocompression bonding of two Cu surfaces.

Figure 2.20 TEM images of Cu-bonded layers (a) before bonding, (b) after 400°C bonding for 30 min, and (c) after 400°C bonding for 30 min followed by nitrogen anneal at 400°C for 30 min. [55].

2.3.1 Cu-Cu Nanowires Compression Bonding

As mentioned in the previous section 2.3, the high temperature required for effective Cu-Cu thermocompression bonding has been a major drawback of this technique. In recent years, researchers [56-59] have been finding ways to lower the bonding temperature by using Cu NWs.

It has been reported by T. Karabacak *et al.* [53] that Cu nanorods grown by oblique angle sputter deposition exhibit lower melting temperature than its bulk counterpart. It is explained that nanorods experience enhanced surface diffusion as compared to bulk material and thus undergoes pre-melting. Following this work, Wang *et al.* [56, 57] demonstrated that bonding of these Cu nanorods (figure 2.21) achieved dense bonding structure at a lower bonding temperature of 300°C followed by post annealing at 400°C in a reducing environment. These nanorods underwent coalescence readily upon a low bonding temperature of 200°C.

Alternatively, both Q.H. Luan *et al.* (2008) and V.H. Nguyen *et al.* (2009) demonstrated that solderless interconnection can be achieved by Cu NWs thermocompression bonding. Cu NWs which were grown by electroplating through AAO porous template on two different metal surfaces were pressed against each other. This led to permeation and entanglement of the NWs between the two surfaces. As a result, an electrical and mechanical interconnection known as “nano scratch” was formed (figure 2.22) [58]. Process optimization of the Cu NWs bonding was studied to obtain a successful assembly through entanglement of the Cu NWs between the two surfaces. Figure 2.23 shows the SEM images of both bad and successful assembly of the Cu NWs [59].

Though research on the NWs bonding has been emerging in the recent years, the focus is mainly on the demonstration of using Cu NWs as an interconnection. Studies of the bond mechanism and behavior need to be dived in to have a better understanding of this method.

Figure 2.21 Schematic diagram of wafer bonding by Cu nanorod arrays [57].

Figure 2.22 Schematic diagram of “nano scratch” assembly [58].

Figure 2.23 SEM image of bad assembly (left) and successful assembly (right) of the “nano scratch” [59].

2.4 Summary

The tremendous increase in I/O density of IC chips has driven the change in the type of chip-substrate interconnect technologies from wire-bonding to flip-chip array solder ball attachment. In recent years, flip-chip solder capped Cu pillar technology has been introduced to overcome the scaling and reliability issues faced by solder bumps. However, the advantage of using Cu pillar is still limited by the properties of the solder cap. As such, various research groups have been exploring alternative interconnections such as CNT off-chip interconnect, ACF using metallic NWs and patterned micropads of metallic NWs on substrate. Although stress simulation was done by Lin *et al.* [20, 21] to evaluate the peeling stress of the ACF using metallic NWs, the study was primarily focusing on the electrical properties of the interconnect instead of the mechanical property. Similarly, Stam *et al.* [22] focused only on the electrical property of the interconnect which consists of Cu NWs embedded in ACF. In addition, Sharma *et al.* [23, 24] presented the idea of using patterned micropads of metallic NWs arrays through solder reflow process for chip-substrate interconnect. This demonstrates that the fabrication of the metallic NWs enables easy integration of these devices into standard silicon manufacturing.

Nanopore growth mechanism and self-organized formation of AAO template have been widely researched. However, fabrication of AAO on substrate has been less studied, especially on the post processing impact of the interaction between AAO template and the metal underlayer. This will be addressed and discussed in Chapter 4 to develop a robust fabrication method of Cu NWs for subsequent 3D integration.

To overcome the limitation of solder properties, direct Cu-Cu thermocompression bonding using NWs is proposed in this work. T. Karabacak *et al.* demonstrated that nanorods exhibit lower melting temperature than its bulk counterpart due to enhanced surface diffusion. As such, the use of Cu NWs can help to lower the bond temperature which is desirable for low thermal budget process, post-bonding thermo-mechanical stress

control and bond alignment accuracy. However, enhanced surface diffusion may have an adverse effect on electromigration. Greater surface area may lead to more electromigration than in the larger Cu pillar. Nevertheless, Cu NWs array is expected to have better mechanical reliability than solder capped Cu pillar due to the absence of brittle intermetallics formation.

Some of the academic groups have made use of the nanoscale properties of NW to lower the bond temperature. Wang *et al.* [56, 57] had focused on the microstructure analysis of the bonded joint under different bonding temperature and environment. On the other hand, Q.H. Luan *et al.* [58] and V.H. Nguyen *et al.* [59] demonstrated that solderless interconnection can be achieved by Cu NWs thermocompression bonding. However, the relationship between the bonding parameters (such as temperature, pressure, duration and environment) and the electrical and mechanical properties of the NWs joint has not been studied in great detail. Moreover, the mechanism of Cu NWs bonding has not been elaborated yet. Thus, various bonding conditions have been carried out and analyzed in this thesis work to establish the relationship between the electrical and mechanical properties to the bonding parameters, as well as elucidating the bonding mechanism (Chapters 5 and 6).

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Chapter 3

Research Methodology

In this chapter, an overall process flow of the thesis work is presented in section 3.1 and details of each process steps are elaborated in sections 3.2 to 3.7. Various material characterization techniques adopted in this study are highlighted in section 3.8. These include X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), focused ion beam (FIB) and electron energy loss spectroscopy in the transmission electron microscopy (TEM-EELS).

3.1 Process Flow of Nanowires Bonding and Characterization

The experiments involved four main stages (figure 3.1) which include fabrication of the AAO template, electrodeposition of the Cu NWs arrays, thermocompression bonding and bond characterization through electrical and mechanical tests.

Figure 3.1 Experimental flow chart of the research

3.2 Fabrication of AAO template

Two types of AAO template are used in the process development of Cu NW array. These include stand alone AAO template and AAO template grown on Si substrate. The former is used for study on the control of the pore diameters (section 4.3.1), electrodeposition of Cu NWs (section 4.3.3) and characterization of individual Cu NW (section 4.3.4). The latter is used for bonding of Cu NW arrays (Chapter 5 and 6).

3.2.1 Stand Alone AAO Template

The materials and chemicals used in the experiments are summarized and listed in table 3.1. Two types of anodization electrolyte were used to explore the fabrication of different pore diameters of AAO templates.

Table 3.1 Materials and content required for the experiment

Purpose	Material/ Chemical	Content
Anodized sample	Aluminium foil	99.997 % from Alfa Aesar (0.1 mm thick)
Anodization electrolytes	Oxalic acid ((COOH) ₂)	0.3 M
	Sulfuric acid (H ₂ SO ₄)	10 wt%
Alumina etchant	Phosphoric acid (H ₃ PO ₄) and Chromic acid (H ₂ CrO ₄)	6 wt% and 1.8 wt%, respectively
Dissolution of Al film	Mercury Chloride (HgCl ₂)	Saturated
Pore widening	Phosphoric Acid (H ₃ PO ₄)	5 wt%
Copper deposition electrolyte	Copper(II) sulphate pentahydrate (CuSO ₄ ·5H ₂ O) and Sulfuric acid (H ₂ SO ₄)	238 g/L and 21 g/L respectively
Liberation of nanowires	Aqueous sodium hydroxide (NaOH)	1 M

The AAO template fabrication steps described below are based on achieving a nominal pore diameter of 40 nm. The anodizing condition and pore widening time vary for other pore diameters accordingly. AAO templates were prepared in a two-step anodization process, as described in chapter 2.2.2. The equipment set-up is as shown in figure 3.2. Al foil and Pt mesh served as an anode and a cathode, respectively. A Keithley Model 2400 (Keithley Instruments, Inc.) electronic multimeter was connected to both electrodes as a power source. Prior to anodization, Al foil of 99.997% purity is cut into small pieces of dimensions 1 cm by 3 cm (figure 3.3 step 1). To increase the throughput of AAO template fabrication, two pieces of Al foil were anodized at the same time. Anodization was carried out under a constant cell voltage 40 V in a 0.3 M oxalic acid solution at 0°C for 8 h. The formed alumina (step 2) was then removed by an alumina etchant (6 wt% phosphoric acid, H₃PO₄ and 1.8 wt% chromic acid, H₂CrO₄) at room

temperature for 12 hours (step 3), before the Al foil was re-anodized under the same condition as the first step for another 8 hours (step 4). The AAO template was then obtained (step 5) by dissolution of Al using saturated mercury chloride. A subsequent pore widening was carried out in 5 wt% H_3PO_4 solution at room temperature for a range of 20 to 50 min to remove the barrier layer (step 6). Figure 3.4 shows the resulted AAO template (of thickness about $10\ \mu\text{m}$) after pore widening. To investigate on the correlation between pore diameter and pore widening, various pore widening durations were applied and will be discussed in section 4.3.1.2.

Figure 3.2 Schematic diagram of anodization setup (Courtesy of Ng Boon Earn)

Figure 3.3 Schematic diagram illustrating the fabrication process of AAO template using Al foil.

Figure 3.4 Stand alone AAO template after pore widening step.

Further study on the influence of different metal interlayers on AAO anodization was investigated (section 4.3.2) using Al film grown on Si substrate.

3.2.2 AAO Template on Substrate

AAO templates fabricated on Si substrate were studied by using different metal interlayers as shown in figure 3.5. These metal interlayers aim to act as conductive layers for subsequent electrodeposition of Cu NW arrays. Tungsten was chosen as one of the interlayers due to its capability of being oxidized under Al anodization conditions. In addition, its oxide has a higher ionic conductivity than alumina. As mentioned in the literature review (section 2.2.5), these qualities enable the interlayer oxide to penetrate the alumina barrier layer and grow into the alumina pore channels. This will in turn eliminate the step of alumina barrier layer removal before Cu electrodeposition.

Figure 3.5 Schematic diagram illustrating the various layers deposited on Si substrate with (a) Tungsten and (b) Gold as metal interlayers.

Two types of substrate were fabricated. First, titanium (Ti), tungsten (W) interlayer and aluminium (Al) films of thickness 15 nm, 60 nm and 1 μm, respectively were deposited on a thermally oxidized (300 nm) Si substrate. Ti and Al were deposited by e-beam evaporation while W was deposited by sputtering. Second, Ti, gold (Au) interlayer and Al films of thickness 30 nm, 50 nm and 1 μm, respectively were e-beam evaporated sequentially on a thermally oxidized (300 nm) Si substrate without breaking the vacuum. Similarly, the Al substrate was cut into small pieces of dimensions 1 cm by 3 cm. An additional step was applied on Al substrate where the edges were sealed with nail polish to protect the interfaces from being anodized. The anodization setup is similar to figure 3.2 and anodization conditions are the same as described in the previous section 3.2.1. However, a shorter duration was applied on the thin Al film as compared to anodization of Al foil.

The behavior of anodization current against time differs between W and Au interlayer substrates. When Al has fully anodized and reached the metallic interfaces, a decrease or a sudden surge in anodization current was observed for W and Au interlayer substrates, respectively. Anodization was stopped immediately after the surge in current for Au interlayer substrate and extended for an additional 2 to 4 min after the decrease in current for W interlayer substrate. Extended anodization was carried out to allow formation of WO_3 hillocks to penetrate into the alumina barrier layer. Subsequent process steps for the two types of substrate are described in Figure 3.6. Additional steps were required for W interlayer substrate. Pore widening duration of 10 min was first carried out to remove Al_2O_3 flocculation in the pore channels. This was followed by immersion of substrate in the buffer solution (mixture of sodium phosphate, Na_3PO_4 and potassium

phosphate, KPO_4) for removal of WO_3 hillocks. In case of Au interlayer substrate, pore widening duration of 40 min was used to remove the Al_2O_3 barrier layer. In both cases, samples were washed in DI water for 10 min after each process to clean the residues. Nitrogen gas was used to blow dry the sample after each cleaning step.

Figure 3.6 Process flow of tungsten and gold interlayer substrates after anodization.

3.3 Electrodeposition of Copper Nanowires

Electrodeposition occurs when a current passes through an ionic solution. At the cathode, reduction takes place and pure metal (M) forms according to: $\text{M}^{n+} + n e^- \rightarrow \text{M(s)}$. Figure 3.7 illustrates the three-electrode cell set-up used in this experiment. Platinum was used as the anode/counter electrode (CE) and a silver/silver chloride functioned as the reference electrode (RE). AAO template was used as the cathode/working electrode (WE).

Electrolyte composition is provided in table 3.1. Magnetic stirrer was used to ensure homogeneity in the electrolyte and dispersion of bubbles evolved.

Figure 3.7 Schematic diagram of three-electrode cell (Courtesy of Ng Boon Earn)

Prior to electrodeposition of Cu NW arrays, a layer of Au film (about 200 nm thick) was sputtered onto one side of the through-hole AAO template (figure 3.8) to provide electrical contact and serve as the working electrode. Since the Au sputtered AAO template was fragile, it was attached to a steel plate for support. For AAO that was fabricated on substrate, the conductive layer (Au or W) was e-beam evaporated or sputtered as an interlayer during fabrication of the substrate.

For characterization of individual Cu NW, the Au layer was ultrasonically removed from the template embedded with NWs after electrodeposition. Next, the sample was immersed in a small bottle of 1 M NaOH for 4-5 hours to etch away the alumina template completely. After which, the bottle was diluted slowly with de-ionized (DI) water until pH 7 was achieved. The DI water in the bottle was then replaced with isopropanol (IPA) solution and sent for ultrasonic. Finally, free-standing NWs were being liberated and stored in IPA for further TEM characterization.

Figure 3.8 Schematic diagram illustrating the electrodeposition process and liberation of NWs [1]

Electrodeposition of Cu NWs through AAO template on substrate is similar to the procedures as described above. In this case, the steel plate attached with Au sputtered AAO was replaced with the AAO on substrate to serve as the working electrode.

3.4 Dicing

For Cu electrodeposited on Si substrate, the substrates were immersed in acetone to remove the nail polish around the edges prior to dicing. The Cu electrodeposited substrates were then diced into square chips of dimension 1 mm or 2.5 mm. Figure 3.9 shows the diced Cu electrodeposited substrate.

Figure 3.9 Diced substrate with Cu NWs appearing in dark areas.

3.5 Bonding

Two types of bonding (i.e. NW-NW and NW-Film) were carried out in a flip-chip configuration. Figure 3.10 shows the schematic diagram of the process flow for both types of bonding. Two bonding setups were used in this work due to different bonding environment required. Details of the bonding condition will be elaborated in the respective chapters 5 and 6.

Figure 3.10 Schematic diagram of NW-NW and NW-Film bonding.

One of the challenges faced by Cu-to-Cu film bonding is the surface non-planarity which is a result of dishing and erosion during Cu CMP. For Cu NW-Film bonding, NWs should be of a height greater than that of the film recessed region. As NWs are more flexible than the bulk film, it can accommodate better to non-planarity of the film surface through bending and filling up the recessed regions caused by dishing. This increases the contact area between the two chips which is essential for a good bonding.

3.6 Electrical Test

Electrical test (e-test) was carried out on NW-Film bonded samples for bond characterization. The design of the e-test structure is shown in figure 3.11. NW arrays chip (indicated by the small dotted square) was bonded onto the top of the e-test structure (in orange) in a flip-chip configuration. By supplying current and measuring voltage difference at the various locations as indicated in figure 3.11a, a four-point electrical measurement can be achieved. The effective area of resistance (R_a) measurement is indicated by A. The equivalent electrical circuit diagram for figure 3.11a is illustrated in figure 3.12. Similarly, resistance of area B (R_b) and area C (R_c) can be determined by changing the positions of the current and voltage probes.

Figure 3.11 Schematic diagram of the e-test structure. (a) Plan view of four-point electrical test design and (b) cross sectional view of NW arrays bonding.

Figure 3.12 Equivalent electrical circuit diagram for measurement of contact resistance, R_a .

Figure 3.13 SEM image of Cu film e-test structure after shear test: Bonded areas are indicated as A_a , A_b and A_c .

Due to bond misalignment, effective bonded area was measured after shear test using SEM. An example is shown in figure 3.13. The three bonded areas are indicated as A_a , A_b and A_c . The contact resistivity is then calculated using the equation (3.1) below to tabulate the specific contact resistivity of each bonded sample:

$$\frac{R_a A_a + R_b A_b + R_c A_c}{3} = \rho_c \quad (3.1)$$

3.7 Mechanical Shear Test

Shear test was carried out using a Dage series 4000 bond tester. Shear test speed of 20 $\mu\text{m/s}$ at a shear height of 5 μm was applied. The applied force direction is perpendicular to the chip edge and parallel to the test structure plane as illustrated in figure 3.14. In the case of NW-NW bonding, e-test structure will be replaced by NW chip of dimension 2.5 mm by 2.5 mm.

Figure 3.14 Schematic diagram of shear test configuration of the bonded sample.

3.8 Characterization Techniques

3.8.1 X-ray Diffraction

By applying Bragg's law (3.2) [2], XRD technique is used to determine the atomic structure and crystal orientation of the materials. Incident X-ray beams directed towards the sample are diffracted by the atomic planes as illustrated in figure 3.15. These diffracted beams interfere with one another to form constructive interferences when they leave the sample. The constructive interference is governed by the Bragg's condition:

$$n\lambda = 2 d_{hkl} \sin\theta \quad (3.2)$$

where n is an integer, λ is the wavelength of the incident x-ray beam, d_{hkl} is the spacing between parallel lattice planes denoted by Miller indices of (hkl) and θ is the angle between the incident x-ray and atomic lattice planes. By performing a two-theta (2θ) scan, each peak of the collected intensity is extracted from the XRD pattern and matched with the database to obtain the structural information of the scanned sample.

Figure 3.15 Schematic diagram of incident and diffracted beams illustrating Bragg's Law. [3]

In this work, XRD measurements were done to assess the phase structure and crystal orientation of the electrodeposited Cu NWs. Texture analysis of the Cu NWs derived from the XRD pattern is discussed in chapter 4. This is to quantitatively determine the degree of crystalline orientation based on various conditions of electroposition of Cu NWs. The equipment used is Shimadzu XRD-6000 which is located in the Facility for Analysis Characterization Testing and Simulation (FACTS) Laboratory, School of Materials Science and Engineering, NTU. A voltage of 40 kV with current of 40 mA was used to generate the x-rays. Measurements were carried out using θ - 2θ setup with a 2θ scan range between 30° to 90° . The raw data was processed and analyzed using Match! software.

3.8.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) has proven to be a powerful tool for surface analysis due to its sensitivity towards chemical structures on surfaces. The main application of XPS is to detect the chemical bonding state of an element. Additional information such as in-depth distribution can also be extracted due to its dependence of effective escape depth of the photoelectrons [4]. Photoelectrons of kinetic energy (E_k) is generated by a monochromatic x-ray source and correlated to the binding energy (E_B) of the electron by the following equation:

$$E_k = h\nu - E_B - \phi_s \quad (3.3)$$

where h is the Planck constant (6.62×10^{-34} J s), ν is the frequency (Hz) of the radiation and ϕ_s is the analyzer work function. Relating to equation 3.3, figure 3.16 shows the energy band diagram of an electrically conducting sample that is grounded to the spectrometer. For a given x-ray source and electron energy analyzer, E_k can be directly calibrated in E_B . This allows direct identification of elements by referencing from the tabulated E_B values against different electron levels from x-ray fluorescence tables [4].

Figure 3.16 Energy diagram whereby Fermi energies of metal and spectrometer coincide [5].

The chemical nature of Cu oxides formed during the NWs bonding process was identified using XPS located in Institute of Materials Research and Engineering (IMRE). Characterization was carried out in an ultrahigh vacuum (UHV) environment (VG

ESCALAB 220i XL) equipped with a monochromatic Al K (1486.6 eV) source and a concentric hemispherical energy analyzer. Silver paste was applied at the edges to provide additional top grounding of the sample so as to minimize charging. Charging produces a retarding field at the surface that will shift the peaks as E_k of the ejected electrons is reduced. This will lead to inaccurate data measurements. All core-level peaks were referenced by assigning the adventitious carbon peak to 285 eV. XPS was used to determine the change in chemical nature of the Cu NWs annealed at different temperatures. With the combination of TEM EELS mapping analysis, this affirms the Cu oxide nanotube formation during bonding at elevated temperatures in low vacuum system.

3.8.3 Focused Ion Beam

Focused Ion Beam (FIB) system has four basic functions which include milling, deposition, implantation, and imaging. These functions allow cross-sectional imaging, crystal structure analysis, nanofabrication, micro-machining and TEM sample preparation. Figure 3.17 shows the schematic diagram of a dual-beam FIB system which combines both electron beam and ion beam in a single microscope. A stream of high-energy ionized atoms of a relatively massive element is produced via the system and focused onto the sample of interest either for milling or imaging. It can be transformed into a deposition tool by injecting an organometallic gas in the path of the ion beam near the sample surface [6]. The combination of milling and deposition capabilities makes it a useful tool for failure analysis and repair.

Figure 3.17 A schematic diagram showing the configuration of a dual-beam FIB system [6].

In this work, FIB was used to prepare cross sectional samples to characterize the NWs and bond interface of the samples. It was also used for TEM sample preparation. The FIB system used is FEI Nova Nanolab DualBeam™ 600i, located in Microelectronics Reliability Characterization Laboratory, School of Materials Science and Engineering, NTU. Figure 3.18 shows a schematic diagram of the cross sectional sample prepared using FIB. Prior to each cross sectional milling, Pt with thickness of 1-2 μm was deposited on the surface (figure 3.18a) as a protective layer to avoid damages being done to the desired interface during ion-milling. Coarse ion milling using 'Multipass' cutting mode with 6.5 nA current and 30 kV voltage was carried out to expose the cross section of sample interface (figure 3.18b). For improved imaging, 'clean cross section' mode with 0.28 nA current and 30 kV voltage was used to remove surface redeposition of the Pt. Figure 3.19 shows a typical cross sectional image of Cu NWs on substrate.

Figure 3.18 Schematic diagram of the cross sectional sample prepared using FIB. (a) Pt is deposited as a protective layer and (b) Ion milling is carried out to expose the cross section of the sample.

Figure 3.19 Cross sectional image of Cu NWs on substrate prepared using FIB.

3.8.4 Transmission Electron Microscopy- Electron Energy Loss Spectroscopy

With the combination of TEM imaging, electron energy loss spectroscopy (EELS) is an analytical electron microscopy used to study the microstructures of materials [7]. It provides compositional and chemical information by measuring electronic excitations in materials. Though similar to EDX spectrum which relies on electronic excitations, EELS measures the initial excitation of an atom in a material to an ionized state, while EDX measures the X-rays emitted from the decay of this excited state. EELS spectra has a much higher energy resolution than that of EDX. Its energy range is about 0 to 3 keV as compared to X-ray spectra which have a typical range of 1 to 40 keV [7]. Thus, it is can

be used for detection of light elements such as oxygen. In this work, EELS mapping of oxygen was done to locate the different types of oxides at the bonding interface.

By focusing a nearly monochromatic beam of high energy electrons to pass through a material, the spectrometer generates a spectrum showing the number of electrons (scattered intensity) as a function of their loss in kinetic energy [8]. An example of the EELS spectrum of silicon dioxide (SiO_2) is shown in figure 3.20 [9]. Inelastic scatterings of the high energy electron occur during coulombic interactions with the electrons in the material. Due to conservation of energy, the loss of energy is gained by the electrons in the material. Thus, the excitation spectrum of the material can be deduced from the EELS spectrum [7]. As each spectral feature corresponds to a different excitation process, thin samples are recommended so as to achieve a more accurate EELS spectrum. Thick samples have a higher probability of multiple inelastic scatterings for a given transmitted electron. This results in a total energy loss equivalent to the sum of individual losses, which distorts the shape of the energy-loss spectrum.

Figure 3.20 EELS spectrum of silicon dioxide illustrating the intensity of electrons as a function of energy loss. [9]

In this work, TEM-EELS elemental mapping was analyzed to determine the chemical nature of the NW joint interface. TEM sample preparation was done using FIB

system. As described in section 3.8.3, Platinum was deposited on top of the samples to prevent damage during FIB cross section milling. Cross section of the desired interface was cut into a lamella structure and attached to a TEM Cu grid. As TEM-EELS analysis requires very thin sample, thinning of the lamella was carried out until a thickness of around 50 nm or less. This was monitored by the receding of Pt or changing of SEM contrast. The joint interface was then analysed using TEM-EELS (FEI Titan G2 60–300 with Gatan Tridiem imaging filter) in GLOBALFOUNDRIES Singapore Pte. Ltd.

3.9 References

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Chapter 4

Process Development of Copper Nanowires Arrays on Substrate

As device scaling continues to push the limits of solder bump technology, an alternative chip-to-substrate (chip-substrate) interconnection is desired to overcome the scalability and reliability problems. By replacing solder with direct Copper-to-Copper (Cu-Cu) bonding, it prevents formation of brittle intermetallic compound. Due to its nanoscale properties, Cu NWs can lower the bond temperature as compared to bulk Cu film. Hence, thermocompression bonding of Cu NWs arrays is proposed as an alternative approach to the existing chip-substrate interconnection. Prior to the study of nanowires bonding, process development of Cu NWs arrays on Si substrate is being investigated.

4.1 Introduction

Out of the several approaches (such as nanolithography [1], vapour-liquid-solid method [2], hydrothermal synthesis [3], chemical synthesis [4], *etc.*), template-assisted method has emerged as a quick and efficient approach for producing NWs. It is a low cost and high yield technique that is readily scalable to mass production [5]. Among the common templates [6,7], anodized aluminium oxide (AAO) template has been widely used for its favorable characteristics, *i.e.* tunable nanopore diameter and length, high pore density, good mechanical strength, thermal stability [8] and corrosion resistance [9]. This makes it suitable for ultra-scaling and can be integrated within current process conditions. In addition, aluminium is a common material used in the CMOS technology and this compatibility is the key for potential adoption of AAO into the mainstream CMOS manufacturing process. As such, AAO template is used for synthesizing the Cu NWs in this study. Control of the pore diameter and influence of different substrate interlayers are further discussed in section 4.3.1 and 4.3.2, respectively.

Electrodeposition is a promising technique for fabricating continuous NWs in a “bottom-up” fashion. It is efficient in controlling the growth of NWs as it takes place exclusively in the direction normal to the substrate. One great advantage of this method is the ability to create highly conductive NWs. Electrodeposition is based on electron transfer, which is fastest along the highest conductive path. It also enables good control over stoichiometry and can be used to deposit high aspect ratio structures [10] which are needed in chip-substrate interconnection. Hence, electrodeposition via AAO template is adopted to fabricate the NWs in this experiment. Influence of various electrodeposition conditions such as temperature and voltage are discussed in section 4.3.3. This is followed by investigation on the delamination issue for tungsten interlayer sample (section 4.3.4). NWs were also liberated from the template for further material characterizations of individual NW (section 4.3.5).

By adopting electrodeposition via the AAO template method, it is hypothesized that standing Cu NWs arrays on Si substrate could be achieved which provides a potential fabrication method for chip-substrate interconnection.

4.2 Experimental

Standalone AAO templates were used for experiments carried out in sections 4.3.1, 4.3.3 and 4.3.5 while AAO template on substrates were used in sections 4.3.2 and 4.3.4. The anodization setup and experimental details are mentioned in Chapter 3.2. In section 4.3.1.2, the range of pore widening duration applied is 20, 30, 40 and 50 min. The anodization voltage is 40 V and the electrolyte used is 0.3M oxalic acid. Experimental setup and details for electrodeposition and liberation of individual Cu NW are mentioned in Chapter 3.3. The constant voltages (supplied by a potentiostat) and the temperature used in the experiment are tabulated in Table 4.1.

Table 4.1 Electrodeposition condition used in the experiments. Negative voltages were applied because the AAO template at the working electrode was made to be the cathode.

Electrodeposition conditions		
Sample	Copper	
	Voltage (V)	Temperature ($^{\circ}$ C)
Cu 1	-0.01	5
Cu 2	-0.01	R.T
Cu 3	-0.01	60
Cu 4	-0.05	R.T
Cu 5	-0.10	R.T
Cu 6	-1.00	R.T

Removal of AAO template from the substrate was carried out by soaking the sample in acetone to remove the nail polish, followed by immersion in 1M NaOH for 35 min. The sample was then immersed in DI water for another 10 min to clean and remove any residues.

4.3 Results and Discussion

Process development of Cu NW arrays on substrate has been explored and discussed in the subsequent sections. It includes control of the NW diameter through manipulation of the porous template, influence of the metal interlayer, Cu electrodeposition conditions, post annealing of the Cu NW and characterizations of the Cu NW.

4.3.1 Control of Pore Diameters

4.3.1.1 Determination of Anodization Conditions

Jessensky *et al.* [12] have reported that regularly ordered porous structure is formed only within certain anodization voltages that depend upon the particular electrolyte being used. For oxalic acid and sulfuric acid electrolyte, the appropriate range is 30-60 V and below 25 V, respectively. Sulfuric acid electrolyte was used when smaller pore size template was needed to produce smaller diameter nanowires. As such, the anodization conditions chosen for the experiment to obtain templates with a range of pore diameters is summarized in Table 4.2.

Table 4.2 Two-step anodization conditions

Voltage (V)	Electrolyte	Temperature (°C)	Duration (h)	
			1st step	2nd step
20	10wt% Sulphuric acid	0-2	2	2
40	0.3M Oxalic acid	0-2	8	8
60	0.3M Oxalic acid	0-2	1	4

From Table 4.2, a point to note is that long hours of anodization were carried out, especially for 40 V condition. According to Masuda *et al.* [11], longer anodization period improves the regularity of the cell arrangement and produces an almost ideally arranged honeycomb structure. It also helps to reduce the number of defects and dislocations. Defect-free regions appear in large domains, whereas defects are mainly found at the

boundaries of these domains. The size of the domains is dependent on the anodization time, *i.e.* the size of the defect-free region increases with the anodization time. Hence, an anodization period of 8 hours for each step was done at 40 V. This resulted in a template with a thickness of about 10 μm . For both 20 V and 60 V, shorter anodization time was applied due to the resulting higher current density than that of 40 V. The greater current density is a result of different electrolyte and higher voltage used.

Low temperature was maintained during the anodization to ensure more uniform pore diameters throughout the pore channels. It has been reported that due to the thermal enhancement of the chemical dissolution of the oxide by the electrolyte, an increase in the pore diameter towards the oxide surface becomes more pronounced with increasing electrolyte temperature [13].

4.3.1.2 Effects of pore widening time

After anodization and dissolution of Al, a pore widening process was carried out on the remaining AAO to remove the barrier layer and flocs-like Al_2O_3 , which are kept inside the nanopores after anodization. The aim of the pore widening process is to ensure that the bottom of all the pores were fully opened through and at the same time attained templates with a distributed range of pore sizes. Figure 4.1a and b show the SEM images of AAO template with insufficient pore widening and fully opened through pores, respectively. A range of pore widening time was applied on the 40 V anodized AAO template and a relationship between the pore widening time and the resulted pore diameter was established as shown in figure 4.2. The measured pore diameters are displayed in table 4.3.

Figure 4.1 SEM images of the back of AAO template. a) Insufficient pore widening duration and b) sufficient pore widening duration with fully opened through pores.

Figure 4.2 Graph of pore diameter of AAO template against pore widening time.

Table 4.3 Measured pore diameters with respective pore widening time for 0.3 M oxalic acid at 40 V

Pore widening time (min)	Average pore diameter (nm)	Standard deviation (nm)
20	37	±3
30	42	±2
40	46	±4
50	54	±2

From the graph above (figure 4.2), a linear relationship can be established between pore diameter and pore widening time. Generally, when pore widening time is increased,

the pore diameter increases proportionally as observed from the linear graph. This is because a thicker alumina wall has been etched away. With the understanding on the effects of pore widening time, a summary of pore diameters with respect to pore widening time and anodization condition is shown in Table 4.4. Their corresponding SEM images of the templates are shown in Figure 4.3. Hence, the pore diameter of the AAO template can be controlled by manipulating the anodization conditions and pore widening duration.

Table 4.4 Summarized anodization conditions and pore widening time with their corresponding pore diameter

Voltage (V)	Electrolyte	Pore widening time (min)	Average pore diameter (nm)
20	10wt% Sulphuric acid	25	20 ± 1
40	0.3M Oxalic acid	30	42 ± 2
60	0.3M Oxalic acid	55	59 ± 5

Figure 4.3 SEM images of AAO template. (a) 10wt% Sulfuric acid at 20 V; and 0.3M Oxalic acid at (b) 40 V and (c) 60 V, respectively.

4.3.2 Influence of Substrate Interlayer

Following the study on the control of pore diameters through manipulation of anodization conditions and pore widening process, the influence of tungsten (W) and gold (Au) interlayers between the AAO template and Si substrate is investigated. Interlayer functions as the conductive layer for subsequent Cu electrodeposition into the AAO template. As mentioned in section 3.2.2, tungsten was chosen as one of the interlayers due to its capability of being oxidized under Al anodization conditions. Tungsten oxide has a

higher ionic conductivity than alumina, which enables the interlayer oxide to penetrate the alumina (Al_2O_3) barrier layer and grow into the alumina pore channels. As such, removal of alumina barrier layer can be omitted.

4.3.2.1 Anodization on Tungsten and Gold interlayer

Figures 4.4a and 4.4b show the typical current versus time ($I-t$) graphs of Al anodization on substrate with tungsten and gold interlayers, respectively. The average anodization time for W interlayer sample was 42 min. As seen in figure 4.4a, the steady state current (8.1 A) which occurred from 9 to 36.5 min indicates the growth of porous aluminum oxide. When the growth of Al_2O_3 barrier layer reached the W interface, the current started to drop rapidly and followed by a gradual decrease before reaching a steady current (5.1 A) at 40 min, which indicates the growth of tungsten oxide (WO_3). The decrease in current is due to the reduced electric field across the barrier tungsten oxide given a constant applied anodic voltage and increasing thickness of WO_3 . Anodization was extended for another 2 min after the steady current of 5.1 A was reached to allow WO_3 to perforate into the Al_2O_3 barrier layer. With the perforation of Al_2O_3 barrier layer, WO_3 was selectively removed to expose an ohmic contact for subsequent electrodeposition. By using W interlayer substrate, long pore widening process to remove Al_2O_3 barrier layer can be omitted, thus eliminating the increase in pore diameter of the AAO template. Though there are advantages of using W interlayer, the NWs embedded in the AAO template faced delamination from the substrate subsequently. The delamination issue will be further discussed in section 4.3.4.

In contrast to anodization of Al on W interlayer, a surge in current was observed when the Al_2O_3 barrier layer reached the Au interface (figure 4.4b). Due to the sudden surge in current, vigorous evolution of oxygen gas from the reaction may cause delamination of the AAO from substrate. Evolution of oxygen gas occurred when anodization of Al reached the Au interlayer interface and catalyzed the electrolysis of water. This can be represented by equation 4.1. Voids would also form at the Au/AAO interface as a result of vigorous gas evolution. These voids may lead to subsequent

delamination of the AAO template from the substrate. As such, the surge in current needs to be closely monitored to prevent over excessive gas evolution which leads to delamination during anodization.

Figure 4.4 Anodization current against time graphs with a) W interlayer and b) Au interlayer.

4.3.3 Electrodeposition of Copper Nanowires

The ability to fabricate nanowires with preferred growth orientation by adjusting the electrodeposition conditions is an advantage for many applications. For instance, crystallographic orientation along the wire axis is one important parameter that influences the electron transport mechanism in nanowires, which is very important for electronic applications. As such, electrodeposition conditions have been studied to achieve optimized crystalline NWs. According to Jessensky *et al.* [12], anodizing with oxalic acid at 40 V is deemed to have the optimal ordered structure. Thus, AAO template obtained at 40 V was used for the investigation to achieve optimum electrodeposition condition. Many reports have shown that the parameters which affect crystallinity are temperature and voltage [9, 14, 15]. Hence, the plan for achieving highly crystalline nanowires was to find the optimum temperature followed by the optimum voltage. It was however important to understand the growth of the nanowires into the template before proceeding with the rest of the experiments. Thus, an experiment was carried out at a testing stage to

find out the current versus time ($I-t$) profile. Figure 4.5 illustrates the $I-t$ characteristic curve which helped to identify 5 distinct regions.

Figure 4.5 Five regions identified in $I-t$ characteristic curve for electrodeposition of copper into AAO template; Conditions: 0.01 V, room temperature.

The above current-time curve reveals five different regions which is similar to what Riveros *et al.* has reported [10]. Immediately after the potential was applied from open circuit condition, the current exhibited a sharp increase that corresponds to the charge of the electrical double layer. Then, the reduction of copper ions in the vicinity of the cathode surface created a concentration gradient that caused a flux of ions towards the cathode. In this process, the decrease in the current indicates the diffusion layer creation (region (a) in figure 4.5). After that, the current remained nearly constant, corresponding to the growth of the copper nanowires in the pores of the template (region (b)). The current remained constant until the copper nanowires reached the alumina surface (region (c)). Region (d) is the result of rapid growth in the deposition area which occurred when

hemispherical caps started to grow on top of the nanowires. Finally, region (e) is the region of copper overlayer film formation.

As seen from the curve in figure 4.5, when the growth of nanowires reached region (d), they would grow out of the template which is deemed undesirable. Hence, electrodeposition process for the rest of the experiments would be stopped at region (c) or slightly beyond.

4.3.3.1 Temperature Dependence

Based on an applied voltage of -0.01 V, electrodeposition was carried out at 5°C (Cu 1), room temperature (Cu 2) and 65°C (Cu 3) to determine the optimum temperature required. SEM images of the samples were taken after etching in sodium hydroxide (NaOH) for partial removal of AAO template (figure 4.6).

Figure 4.6 SEM images of Cu NW arrays grown at different temperature with applied voltage of -0.01 V. a) Cu 1: 5°C , b) Cu 2: room temperature and c) Cu 3: 65°C .

Cu 1 (figure 4.6a) shows uneven growth of the NWs while Cu 3 (figure 4.6c) shows low density of NWs. One of the possible reasons to account for the low density of NWs in Cu 3 is that vigorous bubbles had evolved during the electrochemical reaction. At high temperature, the reaction rate was enhanced, which resulted in vigorous evolution of hydrogen gas that inhibited uniform electrodeposition of the NWs in the AAO template. Evolution of hydrogen gas is the result of hydrolysis of water at the cathode as shown in equation 4.2.

NWs obtained from all three temperature conditions were considered for further XRD analysis as shown in figure 4.7.

Figure 4.7 X-ray diffraction patterns of Cu NW arrays grown at different temperature with applied voltage of -0.01 V. a) Cu 1: 5 °C and b) Cu 2: room temperature. c) Cu 3: 65 °C.

XRD analysis was done to determine the crystal orientation of the Cu NWs. Figure 4.7 shows the XRD scans for Cu NW arrays embedded in the alumina template electrodeposited at a constant voltage of -0.01 V at 5 °C, room temperature and 65 °C, respectively. Since all the diffraction peaks positions are in agreement with those of Cu JCPDS 04-836 [16], it can be indexed as face-centered cubic (FCC) structure of copper. No diffraction peaks corresponding to the alumina template are observed due to its amorphous structure [17]. However, some Au peaks are present due to the Au conductive layer sputtered at the bottom of the AAO template.

To quantitatively determine the degree of crystalline orientation, texture analysis was done via calculation of texture coefficient (TC) for each sample using equation 4.3 [18]:

$$TC(hkl) = \frac{\frac{I(hkl)}{I_o(hkl)}}{\frac{1}{N} \sum \frac{I(hkl)}{I_o(hkl)}} \quad (4.3)$$

where $TC(hkl)$ is the texture coefficient of (hkl) plane, $I(hkl)$ is the measured relative intensity of (hkl) plane, $I_o(hkl)$ is the relative intensity of (hkl) plane of a standard polycrystalline Cu sample and N is the total number of reflection peaks taken into account. TC of 1 represents randomly oriented crystals in the thin film while TC greater than 1

indicates a preferred orientation perpendicular to the (hkl) plane. The maximum value of TC is N , which implies all the nanowires have the same orientation [10, 19, 20, 21].

Figure 4.8 shows the graph of TC of different planes for Cu 1, Cu 2 and Cu 3. From the analysis of the graph, both Cu 1 and Cu 2 have NWs with preferred orientation ($TC > 1$) along the $[111]$ direction while Cu 3 has a preferred growth orientation in $[220]$ direction. At higher temperature, preferred growth orientation in $[111]$ direction was suppressed ($TC = 0.96$) and $[220]$ direction became the most preferred growth orientation ($TC = 1.25$). Since Cu 2 has a higher TC value of 2.03 than that of Cu 1 ($TC = 1.27$), Cu 2 electrodeposited at room temperature has a stronger texture along the $[111]$ direction. In addition, the highest TC value of Cu 2 (2.03) is much greater than that of Cu 3 (1.25). Electrodeposition at room temperature is thus preferred in terms of a textured Cu (111).

Figure 4.8 Graph of texture coefficient of the Cu NW arrays (calculated with equation 4.3) with respective (hkl) planes for conditions: Cu 1 (5°C), Cu 2 (RT) and Cu 3 (65°C).

4.3.3.2 Voltage Dependence

According to preceding section, electrodeposition of the Cu NWs at room temperature was chosen for the determination of optimum voltage to be used due to its highly preferred crystal orientation in the $[111]$ direction. Hence, electrodeposition of Cu NWs at another 3 different voltages was carried out at room temperature. For low melting

metal like Cu, lower overpotential applied during the deposition would attain single-crystalline nanowires [22]. As such, a small voltage range from -0.01 V to -1 V was considered. The samples were named as Cu 2 (-0.01 V), Cu 4 (-0.05 V), Cu 5 (-0.10 V) and Cu 6 (-1.00 V). The respective SEM images using similar preparation as described in chapter 4.3.3.1 are shown in figure 4.9.

Figure 4.9 SEM images of Cu nanowire arrays with different voltage applied at room temperature. (a) Cu 2: -0.01 V, (b) Cu 4: -0.05 V, (c) Cu 5: -0.1 V and (d) Cu 6: -1 V.

From figure 4.9, we observed that all the conditions were able to synthesize nanowires, and thus they were sent for XRD analysis to check their crystallinity. The XRD patterns obtained are shown in figure 4.10. As seen from the graph (figure 4.10), the preferred orientation of all samples is in the [111] direction as well.

For texture analysis (figure 4.11), we can deduce that Cu 2, 4 and 5 (-0.01 V, -0.05 V and -0.10 V, respectively) have the most preferred crystal growth orientation in the [111] direction with relatively high TC value around 2 as compared to that of Cu 6 (-1.00

V). Hence, with the above analysis, electrodeposition at room temperature with applied voltage in the range of -0.01 V to -0.10 V is the optimized condition in terms of crystallinity.

The reason for preferred orientation growth along [111] direction is that (111) plane has the lowest surface energy for Cu [15]. The mechanism of the growth direction can be explained by using interface energy minimum principle [14]. The interfacial energy between electrolyte and metal substrate is the lowest at the beginning of growth, thus Cu starts to nucleate at the interface in [111] direction. Due to 2D nucleation layer-by-layer growth mode (for soft metal like Cu), orientation growth direction remains the same throughout the filling of pores and this contributed to the highly preferred growth orientation of [111].

Figure 4.10 X-ray diffraction patterns of Cu NW arrays with various constant voltages applied at room temperature. a) Cu 2: -0.01 V b) Cu 4: -0.05 V, c) Cu 5: -0.1 V and d) Cu 6: -1.0 V.

Figure 4.11 Graph of texture coefficient of the Cu NW arrays (calculated with equation 4.3) with respective (hkl) planes for conditions: Cu 2 (-0.01 V), Cu 4 (-0.05 V), Cu 5 (-0.10 V) and Cu 6 (-1.00 V).

4.3.4 Issue on Nanowire Lift off from Tungsten Interlayer Substrate

Despite the advantages of using W interlayer substrate, electrodeposited Cu NW embedded in the AAO template would partially delaminate from the substrate during dicing and removal of AAO template. These issues are further elaborated below.

4.3.4.1 Delamination during Dicing

Region A (dark color) indicated in figure 4.12a represents the Cu NWs embedded in AAO template while region B (light color) represents the delaminated areas after dicing. SEM analysis was done to determine the delaminated interface. Figure 4.12b shows the tilted SEM image of an intersection between A and B. Figures 4.12c and 4.12d are the cross sectional SEM images of regions A and B, respectively. Based on the cross sectional image (figure 4.12c), it is confirmed that region A corresponds to the Cu NWs embedded in AAO template, which are in contact with the substrate. Cross sectional image (figure 4.12d) of region B shows that the AAO template had completely delaminated from the substrate. In addition, SEM images taken from the top and tilted views of region B (figures 4.12e and f) revealed tungsten dimples.

EDX analysis was also done to confirm the delaminated interface. Figure 4.13a and b show the EDX area analysis of the region A and B, respectively. Intense Al peak was observed for region A but absent in region B. This indicates that the AAO template may have delaminated completely from region B. Strong signal of W was observed from region B which corresponds to the exposed W interlayer. Intensity of Cu is relative low for region A as compared to that of region B. This may be due to the EDX taken from the top surface which contained incomplete filling of Cu NWs inside the AAO pores. As such, intensity of Al is relatively much higher than that of Cu. In contrast, strong Cu peak was observed for region B which may correspond to the broken Cu nanowires as seen from the SEM images (figures 4.12e and f). Therefore, it is deduced that delamination had occurred at the interface between the W interlayer and Cu NWs embedded in the AAO template.

Figure 4.12 Delaminated sample after dicing. a) Photo of the diced sample, b) Tilted SEM image showing mixed regions A and B; Cross sectional SEM images of region c) A and d) B; e) SEM top view of region B and f) SEM tilted view of region B.

Figure 4.13 EDX area analysis. a) Region A and b) Region B.

Two possibilities are derived from the above delaminated interface analysis. First, there is poor adhesion between Cu NWs and W layer. Second, there is weak adhesion between AAO and W layer which caused the AAO embedded with NWs to detach during dicing. The reason for poor adhesion between the Cu NWs and W layer could be that the WO_3 barrier layer was not completely removed during the immersion of buffer solution. As such, there is minimal contact between the electrodeposited Cu NWs and W interlayer.

To improve adhesion between Cu NWs and W interlayer, forming gas annealing (FGA) at 450 °C was carried out for 30 min after electrodeposition and before removal of AAO template. Results of the annealed sample revealed enhancement in adhesion between Cu NWs and W layer. Figure 4.14 shows the SEM images of a sample with and without forming gas annealing which experienced N_2 gas blow drying after removal of AAO template. As seen from figures 4.14a and b, density of the as-deposited NWs is much lower than that of the annealed NWs (figure 4.14c) after using N_2 gas blow drying. FGA at high temperature can reduce the oxide at the interface between Cu NWs and W interlayer. Hence, the adhesion between Cu NWs and W interlayer was enhanced after FGA.

Figure 4.14 Top view SEM images of NWs arrays after removal of AAO template and N₂ gas blow drying. a) Without post annealing, b) Higher magnification of a) and c) With post forming gas annealing.

The second possibility of the delamination could be due to the weak force between AAO and W layer which is caused by the formation of WO₃ hillocks. As seen from the literature, formation of WO₃ hillocks reduces the contact between AAO template and the W interlayer. If the growth rate of these hillocks is non-uniform, some regions will have much larger WO₃ hillocks which further reduces the contact between AAO and W interlayer. This is illustrated by the schematic diagram in figure 4.15. Therefore, growth of WO₃ is limited to 2 min to prevent reduction of contact between the AAO and W interlayer.

Figure 4.15 Schematic diagram to illustrate the reduced contact at the interface between AAO and W interlayer due to the growth of WO₃ hillocks.

Despite the above measures, delamination still occurred as water jet was sprayed as well as external mechanical stress was exerted on the sample during dicing. The possible reason for delamination will be discussed in the sections 4.3.4.2. and 4.3.4.3.

4.3.4.2 Delamination during Removal of AAO Template

Though annealed NWs in forming gas proved to have enhancement in adhesion, delamination persisted during dicing and removal of AAO. Diced chip with did not experience delamination was processed with the next step (*i.e.* removal of AAO template). It is observed that the Cu NWs embedded in AAO template was lifted off from the substrate as a whole piece when immersed in 1M NaOH solution. The floated AAO fell back to the substrate when the chip was removed from the NaOH solution. A cross section (figure 4.16a) of this sample was done to investigate the cause of the lifted AAO template. As compared to the cross sectional SEM image (figure 4.16b) of the sample before immersing into NaOH, the thickness of the W interlayer in figure 4.16a has reduced greatly. According to the plot of equilibrium ion concentrations in aqueous solution against pH at room temperature (figure 4.17), both Al_2O_3 and WO_3 are soluble in strong basic solution [23]. Since WO_3 dissolves in basic solution such as NaOH, the delamination may be due to the presence of continuous tungsten oxide layer in between W and AAO. This tungsten oxide layer may be formed during the initial deposition of the substrate. In this work, W and Al were deposited through two different methods. W was deposited by sputtering while Al was deposited by e-beam evaporation. As there is a break in vacuum between the two deposition steps, W may react readily with the surrounding oxygen to form a layer of native WO_3 before e-beam evaporation of Al. The reduction in thickness of W interlayer shown in figure 4.16a also suggests that a layer of native WO_3 may have formed during the fabrication of the substrate.

Figure 4.16 Cross sectional SEM images. a) Delaminated NWs during AAO template removal and b) Sample before immersing into NaOH.

Figure 4.17 Influence of pH on dissolution of Al_2O_3 and WO_3 [24]

4.3.4.3 Cause of Delamination

Figure 4.18 shows a schematic diagram to illustrate the delamination of AAO template due to the native WO_3 . Due to the break in vacuum after W sputtering and before e-beam evaporation of Al, a layer of native WO_3 has formed between W and Al (figure 4.18a). As the AAO barrier oxide reached the top of the native WO_3 layer during anodization, WO_3 hillocks started to form from the W/ WO_3 interface instead of the alumina/W interface. This results in a larger fraction of WO_3 being formed (figure 4.18b). After anodization, WO_3 hillocks were selectively removed by immersing in the buffer solution. Due to isotropic etching, native WO_3 layer was also being etched partially. As a result, the interfacial contact area between AAO and underlying WO_3 was reduced (figure 4.18c). Though the sample withstood the electrodeposition step, delamination occurred during the dicing step. This may be due to the larger force experienced during the dicing step by the reduced interfacial contact and weak force between AAO and WO_3 layer as shown in figure 4.18d.

Figure 4.18 Schematic diagram to illustrate the delamination of AAO template due to the native WO₃. a) Initial substrate with native WO₃ due to break in vacuum, b) Growth of WO₃ hillocks after anodization, c) Removal of WO₃ hillocks, d) Electrodeposition of Cu NWs and e) Immersion in NaOH solution.

As explained in the previous section, WO₃ is soluble in basic solution. Hence, the entire piece of AAO embedded with Cu NWs was lifted off when immersed in NaOH (figure 4.18e). Though there is contact between Cu NWs and the underlying W layer, the fraction of Cu NWs in contact with W is relatively smaller than the rest of the area. AAO pore area has been analyzed using open source software ImageJ (version 1.44 by National Institute of Health). The fraction of pore area against the total sample area is estimated to be around 0.26 (Appendix A). Besides, the pore filling density of Cu NWs may not be 100%. In addition, there could be a possibility that the WO₃ barrier layer was not completely removed during the 10 min immersion in buffer solution. This leads to even a smaller fraction of contact between Cu NWs and W. As such, the bubbles evolved during the dissolution of WO₃ may force the AAO embedded with the Cu NWs to break away.

In conclusion, AAO embedded with Cu NWs was detached from the substrate due to the dissolution of continuous native WO₃ during the immersion of NaOH. Due to the limitation of fabrication of the substrate, formation of native WO₃ on W interlayer

becomes unavoidable. Hence, Au interlayer substrate was used for the rest of the bonding experiments.

4.3.5 Characterization of Individual Copper Nanowire

After the above investigations, Cu NWs were liberated from the AAO template and dispersed in IPA solution for material characterization under TEM. Figure 4.19 shows the TEM image of the liberated Cu NWs which were electrodeposited using -0.1 V at room temperature. Selective area electron diffraction (SAED) and HRTEM images illustrate the single-crystal structure of the Cu NW. Figure 4.19b reveals lattice fringes with an interlayer spacing of 0.208 nm, which corresponds to the characteristic Cu (111) plane and thus confirming that the Cu NW has a face-centered cubic (FCC) structure and is crystalline [25,26].

Figure 4.19 (a) TEM image of single crystal Cu NW and SAED (inset); (b) HRTEM image of (a) showing the interlayer spacing.

4.4 Summary

In this chapter, process development of fabricating Cu NWs arrays on Si substrate has been explored. The diameter of the NW is determined by the pore size of the AAO template. By varying the pore widening duration for a fixed anodized AAO template, a

linear relationship between pore diameter and pore widening time is established. Thus, the diameter of the NW is controllable by adjusting the anodization conditions and pore widening time.

Influence of W and Au interlayer on substrates has been discussed. As WO_3 has a higher ionic conductivity than alumina, WO_3 barrier layer is able to penetrate the alumina barrier layer. Hence, use of W interlayer eliminates the removal of alumina barrier layer process step. For Au interlayer, the surge in current needs to be monitored closely to prevent delamination caused by vigorous gas evolution during anodization.

Growth of Cu NWs with preferred crystal orientation can be obtained by manipulating the electrodeposition conditions. Dependence of the electrodeposition voltage and temperature were analyzed. By using texture coefficient analysis method, electrodeposition at room temperature with applied voltage in the range of -0.01 V to -0.10 V is the optimized condition which yields a preferred growth orientation in [111] direction.

From the investigations on different metal interlayer used, adhesion between Cu NWs and interlayer needs to be considered in order to achieve a high density array of NWs on substrate. The use of W interlayer substrate faces delamination issue during dicing and removal of the AAO template. The possible cause of delamination may be due to the native WO_3 layer grown when there was a break in vacuum after the W interlayer film deposition and before the aluminum film deposition. Due to the limitation of the fabrication method, native WO_3 has formed between Al and W inevitably. Hence, Au interlayer substrate is used for the rest of the bonding experiments.

Finally, TEM analysis shows that crystalline Cu NW with characteristic Cu (111) plane was achieved. In conclusion, standing Cu NWs arrays on Si substrate could be achieved, which makes it a potential approach for 3D interconnections.

4.5 References

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Chapter 5

Nanowires Arrays Bonding in Low Vacuum Environment

A new generation of chip-to-substrate interconnects is necessary to overcome the challenges posed by scaling of solder bump technology. High aspect ratio Cu NWs arrays are scalable and capable of increasing the standoff height. As compared to tin—based solder bump, they are more electromigration resistant and eliminate the formation of brittle copper-tin intermetallics during reflow that can compromise the interconnection's thermo-mechanical reliability. Moreover, Cu provides higher electrical and thermal conductivity than solder. With the NWs arrays configuration, it would also have higher redundancy to fail as compared to single column interconnect. It also has a larger surface area to volume ratio and thus better heat dissipation than a bump or pillar. Parallel arrays of NW allow shunting of current away from higher resistance NWs and thus improve the lifetime. In addition, NWs arrays are more resistant to crack propagation than bump or single column interconnect. Due to its advantages over solder bumps, Cu NWs arrays is proposed to be an alternative chip-substrate interconnection. Process development of Cu NWs arrays on Si substrate has been explored in the previous chapter and standing Cu NWs arrays on substrate has been successfully demonstrated. In this chapter, investigation on joining of Cu NWs arrays through thermocompression bonding method is carried out.

5.1 Introduction

Cu thermocompression bonding is one of the possible technologies for fabrication of three-dimensional (3D) integrated circuits (ICs) and heterogeneous systems. One of the key considerations of this technique is to achieve lower temperature bonding as it is desired for compatibility with back-end-of-line (BEOL) processing conditions and reduction in thermal mismatch to ease bond misalignment. There have been a number of studies on Cu-Cu film bonding for 3D ICs [1-6], but very few studies on the use of Cu NWs as a bonding medium [7-10]. The motivation towards the use of NWs is that nanostructures having high surface area to volume ratio as compared to their bulk materials, they may be able to undergo pre-melting (or surface melting) at temperatures much lower than its bulk melting point as reported by Tansel Karabacak [11]. This in turn lowers the bonding temperature required to have a good Cu-Cu bond between two chips.

5.2 Experimental Methods

Three types of bonding were experimented which include Film to Film (Film-Film), NWs to Film (NW-Film) and NWs to NWs (NW-NW). Each type of bonding was carried out in a face-to-face configuration by flipping over one of the chips. After electrodeposition of Cu NWs through AAO template on substrate, the AAO template was removed by immersing the sample in 1 M sodium hydroxide for about 20 min to expose the standing NWs array. Prior to Film-Film and NW-Film bonding, surface cleaning was done on the electrodeposited Cu film (of 1 μm thickness) by etching in glacial acetic acid for 10 min [12] and blown dry using nitrogen gas.

The bonding condition was set at an applied pressure of 1.3 MPa for 1 hour in low vacuum environment (with a pressure of around 5 mbar) at bond temperature of 200°C and 300°C. A simple bonder (Figure 5.1) was placed in the furnace with a temperature against time profile as shown in Figure 5.2. Metal plates were used to align the two chips together. The nominal bonding area was standardized to 1 mm^2 .

Shear test was carried out using a Dage series 4000 bondtester. Details on shear test condition are provided in Chapter 3.7. For the first part of the experiments, average shear strength was taken based from 5 to 9 samples for each condition. For the second part of the experiments, results were tabulated based on 10 to 11 samples for each condition. A third set of experiments was done to characterize the electrical performance. The bonding condition was similar to the previous ones except that an applied pressure of 3.13 MPa was used with a bond temperature of 200°C. Details of the electrical test can be found in Chapter 3.6. The specific contact resistivity was obtained by taking the average of 9 NW-Film bonded samples.

Figure 5.1 A simple bonder showing the placement of the samples and applied loads before placing in the furnace.

Figure 5.2 Temperature against time graph for the bonding process.

In section 5.3.3, a series of annealing conditions (Table 5.1) were applied to investigate the transformation from NWs into nanotubes. A pressure of around 5 mbar

was in the low vacuum environment while a pressure in the range of 10^{-2} mbar was in the high vacuum system. Forming gas used consists of argon (95%) and hydrogen (5%).

Table 5.1 Experimental matrix to study the effects of different annealing conditions on Cu NWs arrays

Figure No.	Temperature (°C)		Annealing Environment				Annealing duration (min)				
	200	300	Air	Low Vacuum	High Vacuum	Forming gas	0	15	30	60	720
5.10a and b	-	✓	✓	-		-	-	-	-	✓	-
5.10c and d	-	✓	-	✓		-	-	-	-	✓	-
5.10e and f	✓	-	-	✓		-	-	-	-	✓	-
5.10g and h	✓	-	-	-	✓	-	-	-	-	✓	-
5.10i and j	✓	-	-	-		✓	-	-	-	✓	-
5.12a	-	-	-	-		-	✓	-	-	-	-
5.12b	✓	-	-	✓		-	-	✓	-	-	-
5.12c	✓	-	-	✓		-	-	-	✓	-	-
5.12d	✓	-	-	✓		-	-	-	-	✓	-
5.12e	✓	-	-	✓		-	-	-	-	-	✓

Avizo® Fire software from Visualization Sciences Group was used to analyze the voids that had formed inside the NWs annealed at 200°C for 30 min in low vacuum environment. Three dimensional (3D) visualization of the voids was created through stacking of 45 FIB/SEM cross sectional images. The stacked images were aligned to reconstruct the voids that formed inside the NWs.

5.3 Results and discussion

NWs arrays bonding results are discussed in terms of mechanical shear strength and electrical contact resistivity as these are two of the critical parameters that characterize a good Chip-Substrate interconnect. The bonding experiments were carried

out in four parts. First, a comparison among the 3 types of bonding was carried out at a temperature of 200°C. Second, NW-NW samples were bonded at 200°C and 300°C to study the effect of the bond temperature. Third, electrical tests were carried out on NW-Film samples bonded at 200°C. This was followed by investigation on the NW bond mechanism through SEM and TEM-EELS characterizations. A fourth set of experiments focused on the various annealing conditions (*i.e.* temperature, environment and duration) to study the transformation from nanowires into nanotubes.

5.3.1 Nanowires Arrays Bonding Results

5.3.1.1 Mechanical Shear strength

Three types of bonding (Film-Film, NW-Film and NW-NW) are being studied. The bonding temperature was fixed at 200°C which is lower than that used in the reported literature [13] for Cu Film-Film bonding. According to Chen *et al.*, a good Cu-Cu bonding can be achieved at bonding temperatures above 300°C [13]. Figure 5.3 shows the average shear strength of the respective types of bonding. In comparison among the three types of bonding, both NW-Film and NW-NW bonding exhibit higher average shear strength than that of Film-Film bonding. In particular, NW-NW bonding achieved the highest average shear strength. This result suggests that the use of NWs enables a stronger bonding as compared to conventional Film-Film bonding at a lower bonding temperature, which is in line with the requirement of BEOL processing conditions. The shear strength of Film-Film bonding is much lower than those values reported by Borowsky *et al.* [14] and Ang *et al.* [15]. One possible reason for the low shear strength is due to difference in bonding conditions such as temperature, force and bonded area. Borowsky *et al.* reported shear strength values in the range between 5 to 20 MPa. However, the applied bonding conditions followed the usual process parameters for Cu thermocompression bonding which is of higher temperature than 200°C, typically above 400°C. In addition, the bonding was carried out on wafer level as compared to chip-chip bonding in this work. Ang *et al.* reported shear strength value of approximately 95 MPa. However, the applied

bond pressure was 3.28 GPa. This is nearly 1000 times higher than 3.13 MPa which was applied in this work.

Figure 5.3 Comparison of average shear strength among Film-Film, NW-Film and NW-NW samples bonded at 200°C

Although a reasonable bond strength can be achieved with NW-NW bonding at 200°C, further experiments were carried out at 300°C to study the effects of higher bond temperature on NW-NW bonding. The shear test results (Figure 5.4) show that NW-NW bonded at 300°C exhibits higher average shear strength than those bonded at 200°C. This result is in agreement with reports on Cu Film-Film bonding where higher bonding temperature (greater than 300°C) improves the bonding quality [16]. SEM and TEM images were taken on the sheared samples to study the bonding mechanism which is presented in the subsequent section 5.3.2.

Figure 5.4 Comparison of average shear strength between NW-NW bonded at 200°C and 300°C

5.3.1.2 Specific Contact Resistivity

Electrical measurements were carried out on NW-Film bonding by using the electrical test (e-test) structure explained in Chapter 3.6. The specific contact resistivity (ρ_c) for each bonded sample was calculated by using equation 3.1 where A_a , A_b and A_c are bonded areas defined in the SEM image of a sheared sample (an example is as shown in Figure 3.13). R_a , R_b and R_c represent the measured contact resistance for the respective bonded areas on Pad A, B and C. Each contact resistance is derived from the gradient of the voltage against current graph (Figure 5.5). All three contacts displayed an ohmic behavior as deduced from the graph. Using Image J software on the SEM image of the sheared sample, the areas of A_a , A_b and A_c are measured to be $3.811 \times 10^{-7} \text{ m}^2$, $1.363 \times 10^{-7} \text{ m}^2$ and $5.783 \times 10^{-8} \text{ m}^2$, respectively. Using equation 3.1, the specific contact resistivity of the sample bonded at 200°C with bond pressure of 3.13 MPa was $2.158 \times 10^{-7} \Omega \text{ m}^2$. By taking a sampling population of 9 bonded samples, it is deduced that NW-Film samples bonded at 200°C gives an ohmic contact between the 2 chips with an average specific contact resistivity of $2.472 \times 10^{-7} \Omega \text{ m}^2$.

Figure 5.5 Graph of voltage against current obtained from the electrical measurement of a sample bonded at 200°C with bond pressure of 3.13 MPa

5.3.2 Investigation on the Nanowires Bonding Mechanism

Following the shear test of a NW-NW sample bonded at 300°C, cross-sectional SEM and TEM images (Figure 5.6a and 5.6b) of the sheared sample were captured to understand the bonding mechanism. Figure 5.6a and 5.6b is taken from a sheared sample where the shear occurred at the interface between the NW bottom and substrate of the smaller chip. As seen from the SEM and TEM images, the bond interface (indicated by the dotted line) was formed by fusion of NWs arrays from the top and bottom chips. It is also observed that some of the NWs from the opposite chip were not bonded together. One of the possible reasons is due to the imperfect alignment of NWs arrays from the top and bottom chips during bonding. This is expected because the NWs arrays followed the structure of the AAO template, where the pore arrangement was formed randomly and dependent on the initial grain size of the Al film. The observed lateral gaps between neighbouring NWs are due to the initial spacing of the NWs which correspond to the interpore distance of the AAO template. Another possible reason is that during FIB cross sectioning, the sample was not cut at the center of the NWs. An interesting phenomenon was discovered from the top view (Figure 5.6c) and tilted angle (52°) view (Figure 5.6d) of the sheared interface. Both SEM images clearly show that the NWs arrays have been transformed into nanotubes arrays during the bonding process. This suggests a possibility that Kirkendall effect has occurred which led to the formation of voids.

For further investigation, TEM-EELS characterization was done to understand the nanotube formation and the elemental nature of the bond interface. Figure 5.7a shows the cross sectional TEM image of the bond interface between a single pair of NWs from a sample bonded at 300°C. Its corresponding high-resolution TEM (HRTEM) image is shown in Figure 5.7b. The HRTEM image shows that there is good bonding between the pair of nanostructures. The corresponding EELS mapping of oxygen (Figure 5.7c) and Cu (Figure 5.7d) shows that both oxygen and Cu prevailed throughout the joint, including at the joint interface. This signifies that the bond interface is formed by Cu oxide. Moreover, both the oxygen and Cu EELS maps reveal a distinct difference in intensity of electron energy loss between the core and walls of the nanostructures. The intensity of EELS

elemental map of a thin film is proportional to the concentration of atoms present. Therefore, higher intensity of EELS elemental mapping represents thicker material. This suggests that there are different thicknesses throughout the nanostructure. Relatively higher intensity of the mapping is observed at the boundary of the nanostructures. This indicates that the nanostructure is made up of a hollow core with thick walls.

TEM-EELS was also done on NW-Film sample bonded at 200°C. Figure 5.8a shows the TEM image before EELS mapping and its corresponding EELS map of oxygen (Figure 5.8b) and Cu (Figure 5.8c). As seen from the EELS elemental mapping, the presence of oxygen and Cu throughout the NW indicates that Cu has also been oxidized to Cu oxide. Similarly, the distinct difference in intensity of electron energy loss between the core and walls of the NWs suggests that the NW is made up of a hollow core with thick walls. In other words, the NWs have been transformed into nanotubes during the bonding process in both conditions.

In addition to the SEM images of the sheared interface shown in Figure 5.6, TEM-EELS results further affirm that hollow nanostructures were formed during the bonding process which may be a result of Kirkendall effect. Kirkendall effect [17] can occur when Cu atoms in the core have diffused outwards at the Cu/Cu oxide interface and oxidized to form Cu oxide nanotubes. This phenomenon will be further discussed in the next section 5.3.3.

Figure 5.6 SEM images of a) cross-sectional bond interface (indicated by dotted line) between top (Sample A) and bottom (Sample B) chips bonded at 300°C, b) Corresponding TEM image of a), c) Top view and d) tilted view of sheared interface.

Figure 5.7 a) TEM image of a pair of Cu nanowires bonded at 300°C. b) HRTEM image of the interface indicated in a). TEM-EELS mapping of a): c) Oxygen map and d) Copper map.

Figure 5.8 a) TEM image of NW-Film bonded at 200°C. TEM-EELS mapping of a): b) Oxygen map and c) Copper map.

5.3.3 Investigation on the transformation of NW into nanotube

As discussed and concluded from the previous section 5.3.2, the Cu NWs were transformed into Cu oxide nanotubes during the bonding process in a low vacuum

environment. In this section, a series of annealing experiments was conducted on the standing NWs arrays to further understand how Kirkendall effect took place during the bonding. This is studied through analysis on the influence of annealing temperature, environment and duration.

5.3.3.1 Influence of Annealing Temperature and Environment

After removal of AAO template, the exposed standing NWs arrays were annealed in different environment which include air, low vacuum, high vacuum and forming gas. The annealed temperatures were set at 200°C and 300°C for duration of 60 min to study the influence of various annealing conditions. The annealing conditions used are displayed in Table 5.1 under experimental methods.

Generally, it is observed that the transformation from NWs into nanotubes occurred for samples annealed in air (Figure 5.9b) and low vacuum (Figures 5.9d and 5.9f) environment. In particular, void formation at the core of the NWs can be seen from samples annealed in a low vacuum environment (Figures 5.9d and 5.9f). This void formation may be a result of Nanoscale Kirkendall Effect, which transformed the Cu NWs into copper oxide nanotubes [18]. Detailed description on the mechanism is given in the next section 5.3.3.2. As seen from the top view (Figure 5.9a) and cross sectional SEM images (Figure 5.9b), NWs arrays annealed in air resulted in greater fusion between the nanotubes nearer the surface than at the bottom. A possible reason is that a higher concentration of oxygen is present nearer to the surface than at the bottom of the high aspect ratio nanotubes.

In contrast, high vacuum (Figure 5.9h) and forming gas (Figure 5.9j) annealing environment resulted in minimal fusion between the NWs and no void was observed at the core of the NWs arrays. Unlike annealing in air or low vacuum environment (Figures 5.9a, 5.9c and 5.9e), top view SEM images (Figures 5.9g and 5.9i) of high vacuum and forming gas annealed samples show that the NWs did not fuse together. The differences

could be due to the negligible amount of oxygen in the environment such that Cu oxidation is minimal and thus negligible void formation.

In comparison, enhanced fusion among neighboring NWs is observed at higher annealing temperature of 300°C (Figure 5.9c) than at 200°C (Figure 5.9e) in a low vacuum environment. Thus, the enhanced fusion may be the reason that led to a higher average shear strength for NW-NW bonded at 300°C.

Based on the above results, it can be concluded that an appropriate amount of oxygen supply would transform the Cu NWs into Cu oxide nanotubes. Excessive amount of oxygen (i.e. annealing in air) may lead to severe fusion between the Cu oxide nanotubes within the array. In contrast, annealing in an environment with minute oxygen supply (i.e. high vacuum or forming gas) may prevent the transformation from Cu NWs into Cu oxide nanotubes. This finding is in agreement with the bonding results as discussed in the previous section 5.3.2 where transformation from NW into nanotubes was observed in low vacuum bonding.

Figure 5.9 SEM images showing top view of the Cu NWs arrays annealed in various environment and at different temperature for 60 min: (a) Air, 300°C; (c) Low vacuum, 300°C; (e) Low vacuum, 200°C; (g) High vacuum, 200°C; (i) Forming gas, 200°C. (b), (d), (f), (h) and (j) are the cross sectional images (prepared by FIB) of the top view images (a), (c), (e), (g) and (i), respectively.

Characterization on the type of Cu oxide formed at different temperatures was carried out through X-ray photoelectron spectroscopy (XPS) analysis. The samples were taken from the Cu NWs arrays annealed at 200°C and 300°C in low vacuum environment and the as-deposited Cu NWs arrays. XPS scan was performed on the top surface of the as-deposited Cu NWs arrays standing on substrate after removal of AAO and annealed samples. The former serves as a control of the experiments. Figure 5.10a shows the Cu 2p_{3/2} spectrum of the three samples with the metallic Cu peak (Cu⁰⁺) residing at 932.8 eV (indicated by the dotted line I). The as-deposited sample is deduced as mainly metallic due to the lack of any higher binding energy (BE) shoulder peaks which represent chemical shifts due to higher oxidation states [19]. In addition, its background is asymmetric which is expected for metallic structures [20]. However, a slight trace of Cu oxidation was observed from a small peak indicated by the middle dotted line in O 1s spectrum (Fig. 5.10b). This suggests that the Cu NWs array undergo minimal oxidation after exposure to ambient conditions. For the annealed sample at 200°C, an additional small higher BE shoulder peak at 935.2 eV (indicated by the dotted line III) is observed. This signifies that some of the metallic Cu NWs were being oxidized to form higher oxidation states such as Cu(OH)₂ or Cu₂O. In contrast, the annealed sample at 300°C shows a significant change in the spectrum as compared to the previous two samples. The metallic Cu peak has broadened drastically (indicated by the dotted line II) which relates to a sudden increase in oxidation [21]. In addition, formation of satellite peaks is also observed as indicated in Figure 5.10a. Satellite peaks have been reported to be due to CuO electronic states but is not seen for Cu₂O [19,21]. Therefore, it is evident that CuO existed in the 300°C annealed sample while absent in the 200°C annealed sample. From the O 1s spectrum (Figure 5.10b), it is observed that there is a chemical shift towards lower BE (530.2 eV) for the 300°C annealed sample [19]. This shows that 300°C annealed sample has a much higher oxidation state when compared to 200°C annealed sample. Thus, it can be derived that the peak residing at 530.2 eV corresponds to CuO while 530.7 eV corresponds to Cu₂O. With the above XPS analysis, it is deduced that the majority of Cu is oxidized to Cu₂O and CuO at 200°C and 300°C, respectively. This deduction is in agreement with other reports on Cu oxide phase transformation [18].

Figure 5.10 XPS a) Cu 2p_{3/2} and b) O 1s spectra for as-deposited Cu NWs array and arrays annealed at 200°C and 300°C in low vacuum for 60 min.

5.3.3.2 Influence of Annealing Duration

As mentioned in the previous sections, the transformation from Cu NWs into Cu oxide nanotubes may be a result of Kirkendall effect. Kirkendall effect was first demonstrated by Smigelkas and Kirkendall in 1947 [22]. They reported that the formation of voids near the interface is caused by different diffusion rates of the diffusion couple at an elevated temperature. The atomic diffusion occurs through vacancy exchange instead of direct interchange of the atoms. As a result, the net flow of mass in one direction is balanced by a flux of vacancies in the opposite direction. In 2004, this concept was further applied and demonstrated by Yin *et al.* [23] on the synthesis of hollow nanostructures and was named as the Nanoscale Kirkendall Effect. It has been reported that the effect becomes more complex when applied to nanoscale materials. This is due to the dominant nanoscale effects such as large curvature and high interfacial energies [24]. Since then, there have been several studies [25-28] on the fabrication of hollow nanostructures through the Nanoscale Kirkendall Effect.

To understand how Nanoscale Kirkendall Effect takes place during the transformation from Cu NWs into Cu oxide nanotubes, the standing Cu NWs arrays were annealed for a range of duration at a fixed temperature of 200 °C in low vacuum environment. Figure 5.11a shows that the as-deposited NWs array appeared to be smooth and straight with solid core structures. Partial void formation within the core of the Cu NWs can be seen for 15 min (Figure 5.11b) and 30 min (Figure 5.11c) annealed samples. For the 30 min annealed sample, multiple cross sectional SEM images of the nanostructures (cut using focus ion beam (FIB) milling) were stacked using a software to illustrate the three-dimensional (3D) voids that had formed inside the NW core (Figure 5.12). Instead of the planar view of the cross sectional image, this 3D image gives a clearer view of the location and distribution of the voids within a single NW. It shows that voids formed randomly across the NW. The voids look elongated due to the distance given between each stacked image. Complete formation of the nanotube arrays is observed after annealing for 60 min (Figure 5.11d). When the annealing duration is prolonged for 720 min (Figure 5.11e), severe fusion between neighbouring nanotubes is observed.

Figure 5.11f shows a proposed mechanism of the transformation from Cu NW into Cu oxide nanotube with illustrations of two possible pathways. Path I indicates that void growth takes place through a continuous bulk diffusion of Cu atoms at the Cu/Cu oxide interface while Path II suggests that multiple voids growth occurs through surface diffusion of the Cu atoms along the void surface which eventually leads to a hollow core. Observations from the cross sectional images of various annealing durations (Figures 5.11a to 5.11d) clearly suggest that the NWs array adopted the transformation through path II. Possible reason for Path II to be more favorable may be due to the dominance of nanoscale surface effect whereby the diffusion coefficient of surfaces is several orders of magnitude larger than their bulk counterpart [17]. Moreover, void nucleation at the Cu/Cu oxide interface (i.e. path II) is energetically more favorable than in the bulk (i.e. path I). Results of various annealing durations revealed that void nucleation in the NWs is followed by void growth along the void surface, and finally complete transformation of the nanowires into nanotubes when all the Cu at the core has diffused outwards to form

Cu oxide. In addition, Figure 5.13 shows that the final diameter (99 nm) of the formed Cu oxide nanotube is larger than the initial diameter (49 nm) of the Cu NW. Thus, it is evident that there is outward diffusion of Cu atoms from the core of the NW. The above proposed transformation mechanism is in agreement with the concept presented by Fan *et al.* [29] whereby the influence of surface diffusion on the formation of hollow spinel ZnAl_2O_4 nanowires is induced by the Kirkendall Effect. They proposed that the formation of hollow nanostructures involves two main stages. First, small Kirkendall voids are generated at the interface through bulk diffusion and then followed by surface diffusion of core materials along the pore surface.

The volume expansion during the transformation of Cu NW to Cu oxide nanotube has been derived from the experimental results and is calculated to be close to a factor of 3. Theoretical calculations by using the densities of Cu and Cu oxides reveal that the volume expansion is 1.68 and 1.78 for Cu_2O and CuO , respectively. Given that the experimental volume expansion is greater than the theoretical values, the final Cu oxide nanotube would be porous.

Figure 5.11 FIB/SEM cross sectional images of Cu NWs and Cu oxide nanotubes. a) Before annealing. Annealed at 200°C for a range of duration in low vacuum environment: b) 15 min, c) 30 min, d) 60 min and e) 720 min. f) Schematic diagram of proposed transformation from Cu NWs into Cu oxide nanotubes.

Figure 5.12 3D visualization of the voids in the NWs using Avizo® Fire software

Figure 5.13 Cross sectional SEM image of nanotubes array annealed at 200°C for 1 h with outer diameter of 99 nm and inner diameter of 49 nm

5.4 Summary

In this chapter, the experiments were divided into four parts and bonding results are discussed in terms of mechanical shear strength and electrical contact resistivity. First,

a comparison among three types of bonding (Film-Film, NW-Film, NW-NW) bonded at 200°C was presented. Second, NW-NW bonded at 200°C and 300°C were carried out to understand the effect of bond temperature. Third, electrical measurements were carried out on NW-Film bonded at 200°C. Lastly, a series of annealing conditions were applied to study the influence of temperature, environment and duration on the transformation from Cu NW into Cu oxide nanotubes.

Bond temperature of 200°C was chosen because it is of a lower temperature than the reported minimum bond temperature required for a good Cu Film-Film bonding [16]. Both NW-Film and NW-NW bonding exhibit higher average shear strength than Film-Film bonding. In particular, NW-NW bonding achieved the highest average shear strength. This shows that the use of NW enables a stronger bond as compared to conventional Film-Film bonding at low temperatures. This in turn reduces the thermal budget and thermal mismatch. In addition, NW-NW bonded at 300°C exhibits higher average shear strength than those bonded at 200°C. Using the e-test structure, NW-Film bonded at 200°C exhibits an ohmic bond contact with an average specific contact resistivity of $2.472 \times 10^{-7} \Omega \text{ m}^2$.

To investigate the NWs bonding mechanism, SEM and TEM images of the NW-NW bonded sample were taken and it shows that the bond interface was formed by fusion of the NW arrays from the top and bottom chips. However, SEM images taken at the sheared interface suggested that the NWs arrays have been transformed into nanotubes arrays during the bonding process. TEM-EELS results further affirmed the formation of nanotube through the high intensity of EELS mapping along the boundary of the NW. This distinct difference in intensity of electron energy loss between the core and walls of the NWs suggests that the NW is made up of a hollow core with thick walls. From the EELS elemental mapping, the presence of oxygen and Cu throughout the NW indicates that Cu has been oxidized to Cu oxide. TEM-EELS results are similar for NW-Film sample bonded at 200°C.

Investigation on the transformation from Cu NWs into Cu oxide nanotubes was done through a series of annealing conditions. It is revealed that an appropriate amount of oxygen supply would transform the Cu NWs into Cu oxide nanotubes via the Nanoscale Kirkendall Effect. Excessive amount of oxygen or prolonged annealing duration leads to severe fusion between Cu oxide nanotubes within the array. XPS analysis shows that the majority of Cu has been oxidized to Cu_2O and CuO at 200°C and 300°C , respectively. Partial void formation observed in 15 min and 30 min annealed samples supports the concept of Nanoscale Kirkendall Effect. Multiple voids growth occurs through surface diffusion of Cu atoms along the void surface which eventually leads to a hollow core. Increase in width of the final nanotube also supports that there is outward diffusion of Cu atoms from the core of the NW.

Bonding in low vacuum environment resulted in transformation from Cu NWs into Cu oxide nanotubes. Cu oxidation is observed to be a critical effect during the process of NWs bonding than film bonding due to the large surface area to volume ratio of the NW. As a result, Cu NW oxidizes more easily and leads to formation of Cu oxide nanotubes through Nanoscale Kirkendall Effect. To overcome the formation of Cu oxide nanotubes, a new set of experiments involving NW arrays bonding was carried out in a high vacuum environment in the next chapter.

Though the transformation from Cu NWs into Cu oxide nanotubes may seem undesirable in the context of electrical conductive interconnection, it may be useful in other nanotechnology-based applications such as gas sensors [30, 31], solar cells [32] and rechargeable batteries [33-35]. Through bonding of the nanostructures, it allows 3D stacking of devices which may be beneficial for enhancement in sensitivity given the same form factor.

5.5 References

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Chapter 6

Nanowires Arrays Bonding in High Vacuum Environment

In chapter 5, it is concluded that Cu NWs were transformed into Cu oxide nanotubes via the Kirkendall Effect during low vacuum bonding. Cu oxide nanotube is formed in the low vacuum environment where sufficient amount of oxygen is present to react with Cu at elevated temperature. It is hypothesized that NWs bonding in high vacuum environment will prevent the transformation of Cu NWs into Cu oxide nanotubes during the bonding and thus achieves higher shear strength and lower electrical resistance between the chips. As such, Cu NWs arrays bonding experiments were carried out in a commercial bonder instead of the homemade bonder presented in the previous chapter. In addition, bonding conditions such as pressure, temperature, post-bond annealing and pre-bond annealing environment were also explored to understand their influence on the Cu NWs bond quality.

6.1 Introduction

This chapter focuses on Cu NW thermocompression bonding in a high vacuum environment to achieve Cu-Cu joints. Two types of configuration (NW-Film and NW-NW) were used for bonding in a commercial wafer bonder. Investigations on various bonding conditions such as pressure, temperature, post-bond annealing and pre-bond annealing environment were carried out and discussed. Mechanical properties and microstructure characterization were done to understand their effects on the Cu NWs bond quality and mechanism.

6.2 Experimental Methods

The preparation steps of the Cu NWs and Cu film prior to bonding is similar to the experimental methods as described in Chapter 5.2. However, the setup of the bonding equipment differs from the low vacuum bonding. High vacuum bonding is carried out in a wafer bonder (Suss MicroTec ELAN CB6L substrate bonder), which is located in Cleanroom 2 of Nanyang NanoFabrication Centre, NTU. The wafer bonder provides a high vacuum environment with chamber pressure of 1×10^{-4} mbar. Nitrogen is used as the purging gas to minimise Cu oxidation. To reduce non-uniform exertion of bond pressure, the samples were arranged and placed evenly around the peripheral of the wafer bonder as shown in Figure 6.1. Bonding yield was calculated based on the number of successful chip-chip bonding out of the total number of samples per bonding process.

Electrical test was carried out on the NW-Film bonded samples using the e-test structure configuration as described in Chapter 3.6. After completion of electrical test, shear test was carried out using a Dage series 4000 bondtester. Characterization on the microstructure of the NWs arrays bonding is done through cross sectional SEM images and TEM-EELS mapping analysis.

Figure 6.1 Arrangement of NW-Film samples inside a wafer bonder.

6.3 Results and Discussion

The influence of various bonding parameters is analyzed through the electrical and mechanical properties of the bonded joints. To study the electrical performance of the NWs bonding, electrical test (e-test) structure was used in the subsequent experiments to determine the specific contact resistivity of the bonding. Hence, the analysis is focused mainly on NW-Film bonding with the e-test structure consisting of the Cu film (bottom chip) and Cu NW arrays (top chip). The Cu NW arrays chip is flipped on top of the Cu Film in a face-to-face configuration. Lastly, NW-NW bonding was also carried out to study its influence on the bond quality.

Thermocompression bonding (TCB) is a type of solid state diffusion bonding which consists of two stages. The first stage involves plastic deformation of the asperities on each of the uneven surfaces as the pressure is applied. During the deformation process, more metal-to-metal contact is established when relatively brittle oxide thin films are broken locally. This is followed by the second stage of bonding, where thermally activated mechanisms lead to void shrinkage and increase in the bonded areas. As such, two important bonding parameters (pressure and temperature) are studied and discussed in the following sections.

6.3.1 Effects of Bonding Pressure

Various bond pressures (i.e. 110.65 MPa, 204.49 MPa and 251.34 MPa) were applied at a fixed bond temperature of 200°C to the NW-Film samples to study the influence of bond pressure. Bonding yield was calculated based on the number of successful bonding out of the total number of samples. Figure 6.2 shows the bonding yield, with bond pressure of 204.49 MPa and 251.34 MPa achieving 100% yield and bond pressure of 110.65 MPa obtaining a slightly lower successful rate of 87.5 %.

Electrical and mechanical results are presented in Figures 6.3a and 6.3b, respectively. The specific contact resistivity reduces as applied bond pressure increases. In particular, the specific contact resistivity ($2.92 \times 10^{-7} \Omega\text{m}^2$) for bond pressure of 110.65 MPa is an order higher than that of the other two bond pressures. As seen from Figure 6.3b, the shear strength of the bond increases with increasing applied bond pressure. The above results indicate that increase in bond pressure generally gives a stronger bond and lower contact resistivity.

From the cross sectional SEM images (Figure 6.4) of the various samples bonded with different applied bond pressures, enhancement in lateral fusion between NWs arrays can be observed as the bond pressure increases, with lower porosity in the NWs bonded layer. This is due to the larger downward force which caused greater deformation of the NWs. This resulted in the increase in contact between neighbouring NWs and led to greater Cu atoms interdiffusion among the NWs arrays. The increase in lateral fusion may be one of the reasons that contributed to the enhanced bond quality. Besides the lateral fusion between the NWs, there is also an increase in contact at the interface between the NWs and the opposite Cu film due to greater deformation in both Cu NWs and Cu film. This is in agreement with the study by Leong *et al.* where the true contact area, defined as a function of applied load, nominal area and surface roughness parameters, directly affects the bondability of the Cu wafers, as expressed in terms of dicing yield [1].

Figure 6.2 Plot of NW-Film bonding yield against various bond pressures at fixed bond temperature of 200°C.

Figure 6.3 Comparison among various bond pressures with fixed bond temperature of 200°C: a) Specific contact resistivity and b) Shear strength.

Figure 6.4 Cross sectional SEM images of NW-Film bonded at 200°C with bond pressure of a) 110.65 MPa, b) 204.49 MPa and c) 251.34 MPa.

6.3.2 Effects of Bonding Temperature

Temperature is one of the critical parameters of TCB. Three bond temperatures (i.e. room temperature, 100°C and 200°C) with 8 samples each were applied to study the effects of bond temperature on NW-Film bonding. As the previous results have shown that bond pressure of more than 200 MPa will achieve 100% bonding yield, the applied bond pressure is fixed at around 250 MPa with slight variations as indicated in each of the plots. The slight variations were due to bond misalignment. Figure 6.5 shows the bonding yield against various bond temperatures. Both 100°C and 200°C bond temperatures achieved 100% successful rate of bonding while room temperature (RT) has a low bonding yield of 37.5 %. This shows that elevated temperature (higher than RT) is required to achieve a sufficient good bonding between Cu NWs and film.

Electrical tests followed by mechanical tests were carried out to evaluate the influence of the bond temperature. Specific contact resistivity and shear strength are plotted against bond temperature as shown in figure 6.6. Figure 6.6a shows that the average specific contact resistivity of RT and 100°C bondings are $4.27 \times 10^{-7} \Omega\text{m}^2$ and $3.84 \times 10^{-7} \Omega\text{m}^2$, respectively. Their contact resistivities are an order higher than that of 200°C bonding ($1.93 \times 10^{-8} \Omega\text{m}^2$). As shown in figure 6.6b, 100°C bonded samples have an average shear strength of 0.43 MPa which is much lower than that of the 200°C bonded sample (28.91 MPa). No reading was taken for the samples bonded at RT because the bond was weak and delaminated before the shear test was carried out.

Observations from the cross sectional SEM images (figure 6.7) reveal that the contact between the NWs and film increased with increasing bond temperature. There is minimal contact for RT bonding (figure 6.7a), and increases slightly at 100°C (figure 6.7b). A significant increase in contact area is observed for 200°C bonding (figure 6.7c and 6.7d). At an applied bond pressure of 251.34 MPa accompanied with elevated temperature of 200°C, Cu interdiffusion between NWs and film occurred significantly as they merged into a continuous film (Figure 6.7c and d). In addition, the initial Cu film interface is not distinguishable in the 200°C bonded sample (Figure 6.7d) as compared to

that of RT bonding. Unlike the case of TCB between Cu thin films where bond temperature of above 300°C is required to achieve an indistinguishable bond interface [2], Cu NW-Film bonding is able to achieve indistinguishable bond interface at a lower bond temperature of 200°C. This shows that Cu NWs is capable of lowering the bond temperature.

In addition, samples bonded at 200°C using lower bond pressure of 110.65 MPa is compared against these RT and 100°C bonded samples with high applied bond pressures of ~250 MPa. Despite the reduction in bond pressure by more than half, its average specific contact resistivity ($2.96 \times 10^{-8} \mu\Omega\text{m}^2$) is much lower than that of RT and 100°C bonded samples. It has an average shear strength of 4.71 MPa which is higher than that of RT and 100°C bonded samples. This implies that the bond temperature of 200°C has a stronger influence on the bond quality than its bond pressure. Made *et al.* [3] has also reported on the model that relates true contact area as a function of surface topology, applied load, bond temperature and bond duration. It was concluded that power-law creep deformation (equation 6.1) provides a closer fit to experimental results, where the effective diffusivity has an exponential dependency on temperature (equation 6.2). This supports the finding on the greater dependency of temperature. However, the model is based on Cu film bonding and the results may deviate with Cu NWs bonding. Possible factors that could lead to a difference would be the different degree of deformation and higher surface contact area in the case of the NWs which may enhance interdiffusion.

$$\varepsilon = H_c \left(\frac{D_{eff} \mu b}{kT} \right) \left(\frac{\sigma}{\mu} \right)^n \quad (6.1)$$

where ε is the plastic strain rate of deformation, H_c is the Dorn constant, D_{eff} is the effective diffusivity, μ is the shear modulus, b is the Burger's vector, σ is the applied stress, k is Boltzmann's constant, T is the temperature, and n is the stress exponent with a value between 3 and 10.

$$D_{eff} = D_0 \exp\left(\frac{-Q_a}{kT}\right) \quad (6.2)$$

where D_0 is the diffusivity constant and Q_a is the activation energy.

Figure 6.5 Plot of bonding yield against various bond temperatures.

Figure 6.6 Comparison among various bond temperatures of NW-Film bonding: Room temperature, 100°C and 200°C. a) Specific contact resistivity and b) Shear strength.

Figure 6.7 Cross sectional SEM images of NW-Film bonding at different temperatures. a) Room temperature, b) 100°C, c) 200°C and d) Higher magnification of image (c).

TEM-EELS mapping analysis (Figure 6.8) was done on NW-Film sample bonded at 200°C to characterize the bond nature. Both Cu and oxygen maps reveal that the bonded layer consists of a mixture of Cu and Cu oxides. However, the combined Cu and oxygen maps of the NW-Film sample (Figure 6.8b) show that Cu interdiffusion has occurred between the two chips, which is evident from the continuous Cu film in red colour.

In conclusion, a higher bond temperature gives a better bond quality in terms of electrical and mechanical properties. This is attributed to the enhanced Cu atoms interdiffusion between the two chips across the contact area as is evident from the indistinguishable bond interface. At higher bond temperature, diffusivity of Cu is greatly enhanced.

Figure 6.8 TEM-EELS mapping of NW-Film bonded at 200°C: a) Zero electron energy loss, b) combined stacking of Copper and Oxygen maps, c) Copper map and d) Oxygen map.

6.3.3 Influence of Post Bond Annealing

Post-bond annealing was carried out on samples bonded at 100°C to study its influence in the enhancement of bond quality. The bonded samples were annealed at 400°C for 3 hours in N₂ environment. Bond characterization reveals that there is an enhancement in bond strength and reduction in specific contact resistivity after post-bond annealing. The average shear strength (3.39 MPa) of the bonded samples with post-bond annealing is about 8 times higher than that of the bonded samples without post bond annealing (0.43 MPa) (figure 6.9a). The average specific contact resistivity is also reduced from 3.84 Ωm^2 to 2.66 Ωm^2 after post-bond annealing (figure 6.9b). To study on the bond quality enhancement, cross sectional SEM images were taken. Figure 6.10a shows the NW-Film bonded at 100°C. After post-bond annealing at 400°C, the contact between the Cu NWs and Cu Film increased significantly as shown in figure 6.10b. In addition, there

is also enhanced lateral fusion among the NWs arrays. This may be the reason for the enhancement in the bond quality.

Though post-bond annealing leads to an improvement in the bond quality, its bond properties are still poorer than that of samples bonded at 200°C without post-bond annealing (figure 6.9). The 200°C bonded sample has the highest average shear strength and lowest average specific contact resistivity among the three samples. Hence, post-bond annealing is not as effective as the initial bond temperature in the determination of bond quality.

The reason that post-bond annealing even at a much higher temperature of 400°C and longer duration is not as effective in improving the bond quality as compared to using a higher bond temperature initially could be due to the lower driving force for fusion between the coalesced Cu NWs and film. After the initial bonding at 100°C, some of the NWs have made contact to the film, which would reduce its surface area to volume ratio. Moreover, during post-bond annealing, no load was applied on the samples and thus further lateral fusion between NWs would not be possible if they were not in contact already. Hence, a good bonding is attributed to the initial bonding temperature rather than the post-bond annealing temperature. Furthermore, it has been reported that post-bond annealing is undesirable for IC fabrication due to the promotion of Cu (220) grain growth, which has a shorter electromigration lifetime than Cu with preferred (111) orientation [4].

Figure 6.9 Comparison among 100°C bonded, post-bond annealing and 200°C bonded samples. a) Shear strength and b) Specific contact resistivity.

Figure 6.10 Cross sectional SEM images. a) NW-Film bonded at 100°C and b) NW-Film bonded at 100°C with 400°C post-bond annealing.

6.3.4 Nanowires-to-Nanowires Bond mechanism

To understand the NWs bonding mechanism, a comparison between NW-Film and NW-NW bonding was done to study the differences. As concluded from the previous sections, bond temperature has a stronger influence in the enhancement of the bond quality than bond pressure. Hence, NW-NW samples were bonded at room temperature and 200°C to study the influence of bond temperature. Bond characterizations through SEM and TEM-EELS map analysis were used to study the structure and elemental distribution of the bonds for both NW-Film and NW-NW types of bonding.

6.3.4.1 Comparison between NW-Film and NW-NW bonding

Cross sectional SEM images of NW-Film and NW-NW bonded at RT with bond pressure of 254.14 MPa (Figures 6.11a and 6.11c) and 264.66 MPa (Figures 6.11b and 6.11d), respectively, were captured through FIB milling of the sheared samples. As there is a slight difference in the applied bond pressures, the comparison focuses on the microstructure of the bonds instead of the mechanical performance of each sample. For RT bonding, the contact between NWs and Cu film is minimal and is dependent on the plasticity of the Cu NWs at the contact area. As compared to NW-Film bonding, the contact area between the two NWs arrays chips is increased due to the flexibility of the

NWs and their spacing. With an appropriate density of NWs on the chip and applied bond pressure, the NWs from both chips were able to interlock with one another and thus increased the contact area which led to enhanced Cu diffusion. This can be observed from the NWs in the cross sectional images of the NW-NW bonded sample (Figures 6.11b and 6.11d). As such, the interlocking of NWs can be one of the advantages of using NWs instead of thin film.

Figure 6.11 Cross sectional SEM images of NW-Film and NW-NW bonded at RT with bond pressure of a) 254.14 MPa and b) 264.66 MPa. c) and d) are the magnified images of a) and b), respectively.

Smaller grain size of NWs as compared to the film may be another factor that contributes to the enhancement in bond quality. Nguyen *et. al.* reported that smaller Cu grain size results in a lower void density at the Cu bonded interface [5]. This is because smaller Cu grains are energetically more favorable to grow and form larger grains. As such, substantial interdiffusion and higher growth rate of Cu grain across the interface would occur during TCB. This leads to enhancement in the Cu-Cu bond quality.

TEM-EELS mapping analysis was carried out on the NW-NW sample bonded at RT. As observed from the Cu and oxygen maps (Figure 6.12), the bond consists of mainly

Cu with thin Cu oxides surrounding the surface of the NWs arrays. The formation of thin Cu oxides is inevitable once the AAO template is removed and Cu NWs arrays are exposed to ambient.

Figure 6.12 TEM-EELS mapping (Left to right) of NW-NW bonded at RT: Zero electron energy loss, Copper map and Oxygen map.

6.3.4.2 Effects of bond temperature on NW-NW bonding

For further investigation, NW-NW bonding was carried out at 200°C with an applied bond pressure of 507.6 MPa to study the effects of the elevated bond temperature. As compared to NW-NW bonded at RT, fusion between the two NWs array chips could be observed from the cross sectional SEM image (Figure 6.13a). In addition, the NWs interface is not distinguishable as seen from the TEM image (Figure 6.13b). High resolution TEM image (Figure 6.13c) taken at the center of the bonded sample shows good bonding between the two NW chips with polycrystalline microstructure. The top right inset of figure 6.13c shows the enlarged image of region A. It reveals an interlayer spacing of 0.301 nm, which corresponds to the Cu₂O (110) plane. This finding coincides with the previous XPS analysis which shows that Cu is oxidized to Cu₂O at 200°C. TEM-EELS elemental mapping analysis was done on the 200°C bonded NW-NW sample to determine the bond nature. Figure 6.14 shows that the bond is mainly Cu with slight oxidation distributed evenly across the bonded area. As mentioned in the previous section, formation of thin Cu oxides is inevitable when Cu NWs arrays are exposed to ambient after removal of AAO. Therefore, mild Cu oxidation continues during the bonding

process at elevated temperature, even in a high vacuum environment. This explains the mixture of Cu and Cu oxide bonds observed for both NW-NW and NW-Film samples bonded at 200°C. With the combined analysis from HRTEM and TEM-EELS, Cu NW-NW bonded joint at 200°C consists of both Cu and Cu₂O.

Figure 6.13 NW-NW bonded at 200°C with bond pressure of 507.6 MPa: a) Cross sectional SEM image, b) TEM image and c) HRTEM image.

Figure 6.14 TEM-EELS mapping (Left to right) of NW-NW bonded at 200°C with bond pressure of 507.6 MPa: Zero electron energy loss, Copper map and Oxygen map.

As the above TEM-EELS mapping analysis shows that the bonded samples consist of a mixture of Cu and Cu oxides, NW-NW samples bonded at 200°C with pre-bond forming gas annealing (FGA) were carried out to reduce the Cu oxides. This is to investigate the impact of Cu oxide reduction on the NW-NW bond. Pre-bond FGA is set at 200°C for 60 min. With an applied bond pressure of 264.4 MPa, Cu NWs arrays between the two chips were fused together to form a homogeneous film (Figure 6.15). This is possible due to the NWs interlocking behavior as explained earlier. Cu oxide reduction on the NWs surface resulted in enhancement of Cu interdiffusion between the two chips. The result is similar with previous findings reported by Wang *et. al.* on low temperature wafer bonding using Cu nanorods grown by oblique angle deposition. Wang *et. al.* reported that Cu nanorods arrays with diameter of 10 to 50 nm underwent coalescence when subjected to a bonding temperature of 200°C combined with an external bond pressure [6,7].

Figure 6.15 Cross sectional SEM image of NW-NW bonded at 200°C with pre-bond FGA.

6.3.5 Effects of Pre-bond Annealing Environment

Previous result shows that pre-bond FGA improves the bond interface as a homogeneous film can be obtained. Hence, further experiments were carried out to study the influence of pre-bond annealing environment on the bond quality in terms of mechanical and electrical performance. Prior to the exertion of bond pressure on NW-Film samples, two different pre-bond annealing environments (i.e. FGA and high vacuum)

were carried out on different experiment splits. It has been reported that FGA can reduce Cu oxides and thus enhances Cu film to film bonding [8]. Therefore, forming gas annealing at 200°C for 60 min was applied on the NWs and Film prior to the application of pressure. Pre-bond annealing in vacuum environment was carried out at the same temperature and duration to serve as a control experiment. Due to slight differences in the effective bonded area, the bond pressure varied slightly given a fixed force being applied. The calculated bond pressures are 263.29 MPa and 251.34 MPa for forming gas and vacuum environment, respectively. The yield rate of bonding for pre-bond FGA samples is 87.5% while all samples were successfully bonded for pre-bond vacuum annealed samples (Figure 6.16). Since the bond pressure of FGA experiment is slightly higher than that of vacuum experiment, the lower yield rate of FGA bonding is not attributed to the reduction in bond pressure. Further analysis is required to determine the cause of the lower yield rate of bonding.

Electrical and mechanical tests were carried out on these successfully bonded samples to study the influence of pre-bond annealing environment on the bond quality. Both electrical and mechanical results are presented in Figures 6.17a and 6.17b, respectively. The average specific contact resistivity of samples annealed in vacuum environment prior to bonding is $1.93 \times 10^{-8} \Omega\text{m}^2$. This is lower than that of the pre-bond FGA samples ($3.148 \times 10^{-8} \Omega\text{m}^2$). In addition, the former has an average shear strength of 28.9 MPa, which is higher than that of the latter (12.06 MPa). Both results show that pre-bond annealing in vacuum environment leads to better mechanical and electrical properties of the NW-Film bonded samples.

Figure 6.16 Plot of successful rate of NW-Film bonding against pre-annealing environment.

Figure 6.17 Comparison between pre-bond annealing environment in forming gas and vacuum.

a) Specific contact resistivity and b) Shear strength.

Characterization on the microstructure of the bond interface was done to investigate the difference in mechanical and electrical properties between the two pre-bond annealing environments. Cross sectional SEM images (Figure 6.19a and 6.19b) show that both pre-bond annealing environments resulted in good bonding between NWs arrays and Cu Film as the bond interface between the NWs and film could not be distinguished clearly. Some regions have Cu interdiffusion between the top and bottom chips and appear as a continuous Cu film. For the pre-bond FGA sample, lateral fusion

between the NWs could be observed. This may be due to the surface Cu oxide of the NWs being reduced to Cu during the pre-bond FGA process. As such, Cu interdiffusion between neighbouring NWs could occur when in contact with one another during the exertion of bond pressure.

After the shear test, failure locations of the samples were identified and categorized into interfaces A, B, C or D (Figure 6.18). A and B represent the failure interfaces at the NW chip where A is at the interface between the bottom of the NWs and substrate, and B is the interface between silicon dioxide and Ti interlayer of the NW chip. C represents the failure that occurred at the interface between silicon dioxide and Ta adhesion layer of the Cu film chip. D is the failure interface between Cu NW and film which can be observed from both types of the bonding. For both types of bonding, the bond between NWs arrays and Film was relatively strong such that most of the failures occurred at interfaces A, B and C. It was observed that the failure occurred mainly at interface A for samples with pre-bond FGA. On the other hand, the failure interface was a mixture of A, B, C and D for samples with pre-bond vacuum annealing. This is clearly shown in the TEM images indicated by the red circles (Figure 6.19c and 6.19d). One possible reason could be due to the weak contact between the bottom of the NWs and substrate. During FGA, Cu oxide at the bottom of the NWs was reduced and thus led to a reduction in contact area between the bottom of the NWs and substrate. This can be seen from Figure 5.9j in the previous chapter which shows the cross sectional SEM image of NWs arrays annealed in forming gas. As such, the failure occurred at the weak interconnection between the bottom of Cu NWs and substrate, which explains the results of a weaker shear strength and higher specific contact resistivity of pre-bond FGA samples.

Figure 6.18 Schematic diagram of a NW-Film bonding with indication of four failure interfaces A, B, C and D.

Figure 6.19 Cross sectional SEM images of a) pre-bond FGA and b) pre-bond vacuum annealing. c) and d) are TEM images of a) and b) , respectively.

6.4 Summary

In the previous chapter, Cu NWs bonding in low vacuum environment revealed that the Cu NWs have been transformed into Cu oxide nanotubes via the Nanoscale Kirkendall Effect during the bonding process. Hence, both NW-Film and NW-NW bonding were carried out in a high vacuum environment to obtain Cu-Cu joints after bonding using NWs. Investigation on the effects of various bond parameters such as bond pressure, bond temperature, post-bond annealing and pre-bond annealing environment are focused in this chapter. The NW-NW bonding mechanism is studied through comparison with NW-Film bonding, microstructure characterization and elemental mapping analysis.

Various bond pressures were applied on the NW-Film bonding to study its influence on the enhancement of bond quality. Increasing bond pressure results in greater average shear strength and smaller specific contact resistivity. From the cross sectional SEM images, greater deformation between the Cu NWs and Cu film was observed as the applied bond pressure was increased. As a result, there is an increase in contact between the Cu NWs and Cu film, which led to enhanced Cu interdiffusion and thus improves the bond quality.

Various bond temperatures were also used in a series of experiments to study its influence on the NW-Film bond quality. NW-Film bonding at RT achieved a low yield of bonding whereas bond temperature of 100°C and 200°C achieved 100% successful rate of bonding. This shows that bond temperature higher than RT is required to achieve a sufficient good bonding even with the usage of NWs. A great enhancement in bond quality in terms of mechanical shear strength and specific contact resistivity is observed when the bond temperature is increased to 200°C. In addition, cross sectional SEM and TEM images reveal that the 200°C bond temperature produced an indistinguishable bond interface between the NWs and film. A continuous Cu film is observed as Cu interdiffusion occurred between the top and bottom chips. This temperature is lower than the reported bond temperature of 300°C where Cu thin film bonding is capable of achieving an indistinguishable bond interface [2]. In addition, samples bonded at 200°C with reduced bond pressure revealed a much better bond quality than that of RT and

100°C bonded samples. This shows that the bond temperature of 200°C has a stronger influence on the bond quality as compared to its bond pressure.

Further results show that post-bond annealing at 400°C on a NW-Film sample bonded at 100°C led to enhancement of the bond quality in terms of average shear strength and specific contact resistivity. This is due to the increased in contact area between the Cu NWs arrays and Cu film during the annealing process. Besides, lateral fusion between NWs was also observed. However, its mechanical and electrical properties were still poorer than that of NW-Film samples bonded at 200°C. The driving force for fusion of the coalesced Cu NWs is smaller than the initial Cu NWs bonding process. Hence, post-bond annealing is not an effective approach in the enhancement of bond quality. A good bonding interface is attributed to its initial bond temperature instead of the post-bond annealing temperature.

As compared to NW-Film bonding, the contact area between two NWs arrays chips is increased due to the high surface to volume ratio of NWs. Given an appropriate density of NWs arrays and bond pressure, the NWs from both chips are able to interlock with one another as is evident from the cross sectional SEM images. This increased the contact area which led to enhanced Cu diffusion. This facilitates the shrinkage of voids and thus increases the bonded area. Smaller grain size of NWs as compared to film may be another factor that contributes to the enhancement of bond quality. This is because smaller Cu grains are energetically more favorable to grow and form larger grains. As a result, substantial interdiffusion and higher growth rate of Cu grain across the interface would occur during the bonding process.

TEM-EELS results reveal that both NW-Film and NW-NW samples bonded at elevated temperature in high vacuum environment consist of a mixture of Cu and Cu oxide. Thin Cu oxide surrounding the Cu NW was formed after removal of AAO template and exposed to ambient air. During the process of bonding at elevated temperature, Cu oxidation is minimal but inevitable, especially on the surface walls of the NWs where oxygen can diffuse through the empty spaces between neighbouring NWs. At high enough

applied force, the thin Cu oxide between the two chips can be partially broken mainly because of the deformation of surface asperities at the contact points. Thus, direct Cu to Cu interconnections were formed at those positions.

By applying pre-bond FGA to NW-NW bonding at 200°C, Cu oxide on the NW surface was reduced. This resulted in enhancement of Cu interdiffusion between the two chips and a continuous film was formed. However, experimental results show that pre-bond FGA environment led to weaker average shear strength and higher specific contact resistivity than pre-bond annealing in vacuum environment. The poorer mechanical and electrical performance may be attributed to the smaller contact area between the bottom of the NWs and substrate after reduction of the Cu oxide as observed from the failure interfaces through SEM and TEM images. Hence, it is not a good indication of the actual NW-Film bond quality. Nevertheless, pre-bond vacuum environment was used to eliminate the possibility of poor mechanical performance contributed by the weak interconnection between the NWs and substrate.

In conclusion, the change in bonding environment from low vacuum to high vacuum has prevented the formation of Cu oxide nanotubes as originally planned. This is because the amount of oxygen in the environment is insufficient to allow transformation of Cu NWs into Cu oxide nanotubes via the Kirkendall effect (as described in Chapter 5). In addition, the relationship between the bonding parameters and their electrical and mechanical properties has been established. The bonding mechanism has also been analyzed through various characterization techniques.

6.5 References

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Chapter 7

Conclusions and Recommendations

Three dimensional (3D) integration is one of the potential solutions to the challenges faced due to “More Moore” scaling. It replaces long horizontal wires with short vertical interconnects which reaps benefits of achieving smaller form factor and reduction in RC delay. It also allows integration of heterogeneous system functionality catering to “More than Moore” technology. However, further scaling poses challenges to Cu pillar fine pitch flip-chip technology. In this work, Cu nanowires arrays coupled with thermocompression bonding is proposed as an alternative to replace flip-chip solder bumps or solder capped Cu pillars. This forms a solderless interconnection which overcomes the scalability and reliability issues of solder.

7.1 Conclusions

The feasibility of adopting this alternative chip-substrate interconnection is explored and discussed in terms of the process development of Cu NWs arrays on Si substrate and NWs arrays bonding.

While extensive research has been done on the synthesis of nanostructures, integration of standing NWs on substrate is less explored. Therefore, the first part of the thesis is focused on the exploration of achieving standing Cu NWs arrays on substrate. The NW diameter is determined by the pore size of the Anodized Aluminium Oxide (AAO) template. Experimental results show that the diameter of the NW is controllable by adjusting the anodization conditions and pore widening time of the porous template. The choice of the metal interlayer used for the substrate influences the subsequent fabrication process. Tungsten interlayer eliminates the removal of alumina barrier layer process step due to the ability of tungsten oxide barrier layer to penetrate the alumina barrier layer during anodization. In contrast, the use of gold interlayer is prone to delamination which is caused by vigorous gas evolution during anodization. Though tungsten interlayer gives a higher yield of AAO template during anodization process, it may encounter delamination issue during dicing and removal of AAO template after Cu NWs deposition. Possible cause of delamination may be due to the native tungsten oxide formed when there was a break in vacuum during the substrate fabrication. In addition, adhesion between Cu NWs and interlayer needs to be considered in order to achieve a high density arrays on substrate.

Growth of Cu NWs with preferred crystal orientation can be obtained by manipulating the electrodeposition conditions such as voltage and temperature. By using texture coefficient analysis method, electrodeposition at room temperature with applied voltage in the range of -0.01 V to -0.10 V was found to be the optimized condition which yields a preferred growth orientation in [111] direction.

The second part of the research involves NWs arrays bonding which has not been explored extensively. Both NW-Film and NW-NW bonding exhibit higher average shear strength than Film-Film bonding at a low bond temperature of 200°C. However, SEM and TEM-EELS results of the sheared sample revealed that Cu oxide nanotubes had formed during the bonding process in a low vacuum environment. Investigation on the transformation from Cu NWs into Cu oxide nanotubes was done through a series of annealing conditions. It was revealed that an appropriate amount of oxygen supply is required to transform the Cu NWs into Cu oxide nanotubes via the Nanoscale Kirkendall Effect. Excessive amount of oxygen and prolonged annealing duration leads to severe fusion between Cu oxide nanotubes within the array. Through XPS analysis, the majority of Cu was oxidized to Cu₂O and CuO at 200°C and 300°C, respectively. The concept of Nanoscale Kirkendall Effect is supported by partial void formation observed in 15 min and 30 min annealed samples. Multiple voids growth occurs through surface diffusion of Cu atoms along the void surface which eventually leads to a hollow core. Increase in width of the final nanotube also supports that there is outward diffusion of Cu atoms from the core of the NW.

From the investigation, it was concluded that bonding in a low vacuum environment resulted in transformation from Cu NWs into Cu oxide nanotubes. Cu oxidation is observed to be more prevalent in the process of NWs bonding than film bonding due to the large surface to volume ratio of the NW. As a result, Cu NW oxidizes more easily and leads to formation of Cu oxide nanotubes through Nanoscale Kirkendall Effect.

It is hypothesized that NW bonding in a high vacuum environment could prevent Cu oxide nanotubes formation. A second set of experiments involving NWs arrays bonding was carried out in a high vacuum environment to prove the hypothesis. Experimental results show that increasing bond pressure and temperature resulted in greater average shear strength and reduced specific contact resistivity. Given an adequate NW density and bond pressure, NWs are able to interlock with one another which increases the contact area between the NWs arrays and thus enhances Cu interdiffusion. A

continuous film with indistinguishable bond interface can be achieved through Cu NWs bonding at 200°C. This temperature is lower than the reported Cu thin film bonding where bond temperature of above 300°C is required to achieve an indistinguishable bond interface. TEM-EELS mapping analysis shows that the bond nature is mainly Cu with slight oxidation distributed evenly across the bonded area. By applying pre-bond FGA prior to NW-NW bonding at 200°C, Cu oxide on the NW surface is further reduced. This led to enhanced Cu interdiffusion and a void free homogeneous bond interface was achieved. However, the mechanical performance did not improve as expected which may be due to the weak interconnection between the bottom of the NW and substrate. Nevertheless, it has demonstrated that low temperature Cu-Cu bonding can be achieved with Cu NWs in an optimized bonding condition.

In conclusion, this research explores the development of Cu NWs for chip-substrate interconnection through thermocompression bonding. The main achievements of this work are:

- High density of Cu NWs arrays can be grown directly on Si substrate and bonded at a low temperature of 200°C, which is desired for compatibility with back-end-of-line (BEOL) processing conditions. This temperature is lower than the 300°C reported in literature, which is the temperature required to achieve a good Cu-Cu bonding [54]. Growth of NWs arrays using AAO template method allows patterning them into small columns which makes it scalable to finer pitch dimension.
- The relationship between the bonding parameters (such as temperature, pressure, duration, environment) and the electrical and mechanical properties of the NWs joint has been established, which previously has not been studied for Cu NWs arrays bonding.
- The Cu NW-NW bonding mechanism has been established through various characterization techniques. Interlocking of NWs between two chips increases the contact area between the NWs arrays and thus enhances Cu interdiffusion. However, Cu NWs oxidize more easily due to the large surface to volume ratio of the NWs. Subjecting the chips to forming gas annealing prior to NW-NW bonding

is able to reduce the Cu oxide on the NW surface, which leads to enhanced Cu interdiffusion. Thus, a void free homogeneous bond interface can be achieved.

- The mechanism for the transformation of Cu NWs into Cu oxide nanotubes during bonding was established through the Nanoscale Kirkendall Effect. This shows that the bonding environment is crucial for Cu NWs arrays bonding as excessive amount of oxygen will lead to Cu oxide nanotubes formation at elevated bonding temperature.

The motivation of this work is to overcome the challenges faced by solder bump technology. Solder bump has its limitations in terms of scalability and reliability. Therefore, solder capped Cu pillar technology has been adopted by the industries to meet the tremendous increase in I/O density through scaling down the pitch. However, solder capped Cu pillar is susceptible to the formation of brittle intermetallic compound. Thus, Cu-Cu bonding can be a good alternative to 3D interconnection as it omits the use of solder. One of the disadvantages of Cu-Cu bonding is that it requires higher bond temperature than solder. Hence, this work has demonstrated that the replacement of Cu Film-Film bonding with Cu NW-NW bonding can lower the bond temperature.

7.2 Future Recommendations

In summary, this thesis has investigated on the NWs arrays bonding characterization and mechanism in the development of an alternative chip-chip/substrate interconnection for 3D integration. Further exploration needs to be done for optimization of NWs arrays bonding to achieve better bond quality and reliability. Some of the future works are suggested in the following sections.

7.2.1 Effect of Crystallinity on Bond Strength

Through molecular dynamics (MDs) simulation, Gao *et. al.* reported that crystallographic orientations and temperatures affect the mechanical deformation behavior of copper NWs [1]. In addition, experiments demonstrated by other researchers [2-5] revealed that metal NWs show highly distinct plastic deformation and fracture modes that

are strongly dependent on crystallographic orientation. Recent studies by Liu *et al.* reported that low temperature direct Cu-Cu bonding could be achieved by creep on (111) textured surface of Cu film [6,7]. The findings from Chapter 4 concluded that NWs of different preferred crystal orientation can be synthesized by applying certain electrodeposition condition. Thus, it will be of value to study the effect of crystallographic orientation on the bond strength by synthesizing NWs arrays of different preferred crystal orientation.

7.2.2 Diameter and Density Dependence of Nanowires in Bond Quality Enhancement

The bonding characterizations discussed in chapters 5 and 6 relate various bonding conditions to the NWs bonding behavior. These analyses are based on a fixed nominal bonding area with NW diameter of ~50 nm. However, in the case of a fixed nominal bonding area, shrinking the NW diameter will increase the number of NWs involved in the bonding as illustrated in Figure 7.1. This may in turn influence the bond strength, contact resistivity or other properties. For instance, specific contact resistivity may increase due to shrinkage in NW diameter or reduce due to bond quality enhancement. As mentioned in chapter 6, we concluded that the enhancement in bond shear strength may be due to increase in NW surface area to volume ratio. This implies that an increase in NWs density may contribute to bond enhancement since the NW contact surface area increases. In addition, an increase in the NWs density can also help in reducing the voids caused by large interpore spacing of the AAO template. It is therefore clear that there are multiple factors influencing the bond quality. As such, there is a need to investigate if the bonding characterization results obtained are dependent on the effect of reduced NW diameter and change in NW density. This can be done by fixing one variable and investigate on the other. Figure 7.2a and b shows a comparison by fixing the quantity and varying the NW diameter. Figure 7.2b and c shows the vice versa. Lastly, Figure 7.2a and c shows a comparison on varying both NW diameter and quantity while fixing the NW contact area. A systematic study on the dependence of the NW diameter and density of NW could give additional insight to properties relating to the bonding mechanism reported.

One of the techniques to vary the interpore spacing and achieve high density of the NWs arrays is to use interference lithography [8]. It creates a regular pattern on the imprint stamp follow by replicating the pattern to Al film. The cavities generated on the Al surface act as pore nucleation sites during the first step of anodization. As such, high density regular pore arrangement can be achieved.

Figure 7.1 Schematic diagram (top view) of NW arrays (represented in red dots) for a given fixed nominal bonding area. (a) Large NW diameter with lesser quantity and (b) small NW diameter with larger quantity.

Figure 7.2 Schematic diagram (top view) of NW arrays (represented in red dots) for a given fixed nominal bonding area. (a) and (b) have the same quantity of NWs but different diameter; (b)

and (c) have the same diameter but different quantity of NWs; (a) and (c) have the same NW contact area but different NW diameter and quantity.

7.2.3 Reliability of Cu NWs bonding

To apply chip-substrate Cu NW interconnect structure to 3D IC integration, it is essential to have good electrical, mechanical and thermal properties of the bonding interface for robustness and long term reliability. Nanoscale properties may affect the bulk mechanism of interconnect failure. For instance, EM behaviour of NW may differ from bulk since surface to volume is larger. Greater surface area may lead to more surface electromigration of Cu. Therefore, studies on electromigration (EM) and thermal cycling of the Cu NWs bonding are suggested as part of the future work to evaluate the reliability of Cu NWs bonding.

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List of Publications

Journal

S. R. Chun, W. A. Sasangka, M. Z. Ng, Q. Liu, A. Du, J. Zhu, C. M. Ng, Z. Q. Liu, S. Y. Chiam, and C. L. Gan, "Nanotube Arrays: Joining Copper Oxide Nanotube Arrays Driven by the Nanoscale Kirkendall Effect (Small 15/2013)," *Small*, vol. 9, pp. 2545-2545, 2013.

Conferences

S. R. Chun, C. L. Gan, W. A. Sasangka, A. Du, Q. Liu, C. M. Ng, K. C. Leong: Investigation on Low Vacuum and Low Temperature Copper Nanowires Bonding Mechanism for 3D ICs, in 3D TSV Process and Design Challenges, International Conference on Materials for Advanced Technologies (ICMAT) 2011, Singapore, Jun. 26-Jul. 1, 2011.

S. R. Chun, C. L. Gan, A. Du, Q. Liu, C. M. Ng: Investigation of Copper Oxide Nanotube Formation from Copper Nanowires Arrays Fabricated by Electrodeposition Through AAO Template , in Nanodevices and Nanofabrication, International Conference on Materials for Advanced Technologies (ICMAT) 2011, Singapore, Jun. 26- Jul. 1, 2011.
[**Best Poster Award**]

S. R. Chun, W. A. Sasangka, C. L. Gan, H. Cai, C. M. Ng: Low Temperature Bonding via Copper Nanowires for 3D Integrated Circuits, in Advanced Interconnects and Chemical Mechanical Planarization as a Semiconductor Technology Enabler, Mater. Res. Soc. Symp. Proc. **Volume 1249**, Warrendale, PA, 2010, 1249-F04-21