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Sheik Fareed Muhammad Musthafa Roomi

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SHEIK FAREED MUHAMMAD MUSTHAFA ROOMI

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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Sheik Fareed Muhammad Musthafa Roomi

School of Electrical and Electronic Engineering

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Abstract

Global electrical power demands has seen a dramatic spike recently. Along with demands, deterrents like the shortage in electricity, spikes in electricity price, and power quality problems force many utility customers to examine alternative means of power generation. One of the best alternatives that can improve the traditional power grid is the Distributed Energy Resources (DER). These are small-scale power generation sources with high quality and reliable electricity, and are usually located onsite. All types of distributed energy sources require specific energy regulators, which enables direct connections of the energy source to the utility.

Usually high performance voltage and current source inverters are used for dc-ac conversion. However, these traditional inverters support only the voltage buck operation. Due to their narrow obtainable output voltage property, these inverters cannot be interfaced solely for exploiting energy from renewable sources. These drawbacks can be overcome by designing inverters with voltage buck and boost capabilities. The traditional rule to achieve the voltage buck-boost conversion is by employing a dc-dc boost converter as a front end to the dc-ac inverter. As this conversion involves two converters being connected in series, drawbacks like cost, control and two-stage energy conversion motivate the need to look for an alternative. Therefore, as a solution, the Z-Source inverter (ZSI) was introduced in 2002. ZSI consists of an impedance network and performs single-stage energy conversion. ZSI has been widely preferred in research fields including this research due to advantages like wider obtainable output voltage, higher reliability and higher efficiency.

Medium/high power applications are trending towards incorporating multilevel inverters due to a better output waveform quality and low electromagnetic interference (EMI) while employing devices of smaller voltage rating. In recent years, multilevel inverters that can provide both voltage buck and voltage boost has been the focus for many research studies as it greatly reduces the need for additional dc-dc converters. Therefore, this research also focusses on the multilevel ZSI. Furthermore, the topological design and control schemes for multilevel ZSI's are investigated.

Three-level ZSI topology is configured with two X-shaped LC impedance networks and is merged with the existing NPC inverter topology. The neutral point is formed between the two Z-Source networks. Even though modified modulation methods for controlling the inverter operation have been proposed, this research proposes a new modulation scheme (Reference Disposition Level Shifted Pulse Width Modulation) for three-level ZSI, which provides flexibility for easier implementation with reasonable voltage boosting, low harmonic and less

switching loss across semiconductor devices. As the two impedance networks are supplied by two isolated dc sources, any voltage variability will lead to unbalanced voltage boosting. The main challenge lies in inserting the shoot through without introducing volt-sec error to the three-phase inverter output. Therefore, the proposed topology is designed based on the afore-mentioned aspects.

Dual Z-Source Network Neutral Point Clamped inverter are investigated for ideal and non-ideal conditions with the proposed modulation method as the control scheme. The mathematical analysis for the system is modeled through the simulation and is determined to support the analysis. The experimental setup is assembled and the results are compared to prove the potency of the proposed modulation scheme.

In addition, a two-level inverter topology and its various modulation schemes, that produce the unique shoot through states has been investigated. In addition to the traditional active and zero states, this unique shoot through states provide the voltage boost capability for the inverter. The different modulation methods for controlling the inverter are compared. Maximum Boost Control method is chosen for this research given that it provides wide operating range with maximum voltage gain. As a part of DER application, Proton Exchange Membrane Fuel Cell (PEMFC) stack, which is operated at nominal pressure and temperature, is designed. The design provides the flexibility of controlling the fuel flow rate using a fuel flow regulator. The designed fuel cell stack is then integrated with the conventional and the ZSI energy converters. The performance of both the converters is investigated under sustained and variable fuel flow rate.

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List of Acronyms

AC	Alternating Current
AFC	Alkaline Fuel Cell
APOD	Alternative Phase Opposition Disposition
CHP	Combined Heat and Power
CSI	Current Source Inverter
DC	Direct Current
DER	Distributed Energy Resources
DG	Distribute Generation
DMFC	Direct Methanol Fuel Cell
DZSN	Dual Z-Source Network
EMI	Electromagnetic interference
EZSI	Embedded Z-Source Inverter
FST	Full Shoot Through
IGBT	Insulated-gate bipolar transistor
IPD-LSPWM	In-Phase Disposition Level Shifted Pulse Width Modulation
LST	Lower Shoot Through
LV	Low Voltage
MBC	Maximum Boost Control
MCBC	Maximum Constant Boost Control
MCFC	Molten Carbonate Fuel Cell
MLI	Multilevel Inverter
MV	Medium Voltage
NPC	Neutral Point Clamped

NST	Non-Shoot Through
PAFC	Phosphoric Acid Fuel Cell
PD	Phase Disposition
PEMFC	Proton Exchange Membrane Fuel Cell
POD-LSPWM	Phase Opposition Disposition Level Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
QZSI	Quasi Z-Source Inverter
RD-LSPWM	Reference Disposition Level Shifted Pulse Width Modulation
RES	Renewable Energy Sources
SBC	Simple Boost Control
SOFC	Solid Oxide Fuel Cell
ST	Shoot Through
SZSN	Single Z-Source Network
THD	Total Harmonic Distortion
TSI	T-source Inverter
UST	Upper Shoot Through
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

List of Symbols

B	Boost factor of Z-Source inverter
C	Capacitor
D	Diode
D_x ($x=1$ or 2)	Input diodes for dual Z-Source network
D_x, D_x' ($x=a, b$ or c)	Clamping diodes
i_C	Capacitor current
i_L	Inductor current
L	Inductor
M	Modulation index
N	Neutral point
S_z, S_z' ($z=a, b$ or c)	Switches in the inverter circuit
T	Switching period
T_0	Shoot through period
T_1	Non-shoot through period
V_C	Capacitor voltage
V_i, V_{iU}, V_{iL}	Input dc sources
$\widetilde{v}_0$	Peak dc-link voltage in Z-Source inverter
V_o, V_{oU}, V_{oL}	dc-link voltages
v_L	Inductor voltage
V_x ($x=ab, bc$ or ca)	Output line voltages of the inverter
V_{xN} ($x=a, b$ or c)	Normalized inverter phase voltage

Chapter 1 Introduction

1.1. Background and Motivation

1.1.1. Background

Global energy demand has tremendously increased over the past few decades stressing the availability and sustainable extraction of the conventional energy sources (natural gas, coal, etc.). With the depletion rate of fossil fuel consumption to meet the increasing energy demands of our expanding global economy and population, the fossil fuels would exhaust by the end of this century. Even though fossil fuels are the primary source of energy, the method of processing the fossil fuels and generating electricity are causing tremendous impact on the environment. Depending on the type of fossil fuel and the method of combustion, the impact varies. Some of the major impacts being the greenhouse gas emissions, resultant global warming, acid rain and pollution. The major drawback of these fossil fuels being the carbon dioxide emission, the global carbon-dioxide emission continue to rise with increasing demand, and is illustrated in Figure 1.1 [1]. It is reported that the total emissions due to combustion of fossil fuel and industrial processes exceeded 35.7 billion tonnes of carbon dioxide in 2014 [2]. Faster depletion rate of fossil fuels, increasing emissions of greenhouse gases and increase of fuel cost has spurred research into alternatives.

Figure 1.1 Carbon Dioxide Emissions all over the world by countries

The deregulation of energy markets, environmental concerns, energy supply security and emerging new technologies are the driving factors to switch from a centralised to a de-centralised power generation, frequently with small-scale co-generation. Conventional means of power generation are generally centralised and often require power transmission over long distances whereas, new emerging Distributed Energy Resources (DER) systems are de-centralised and therefore preferably installed near the loads they serve, as depicted in Figure 1.2.

Figure 1.2 Centralized Power Generation vs. De-centralized (localized) Power Generation

Distributed Energy Resources system are small, modular and typically placed on-site unlike the traditional large-scale central generation. With the increase in initiatives worldwide to de-carbonise energy supply, a wide variety of generating plant technologies are being connected to the Distributed Generation (DG) networks. These include the established Combined Heat and Power (CHP), wind turbines and photovoltaic cells. In addition to these common de-centralised technologies, there are nascent and emerging technologies including, fuel cells, solar thermal, micro-CHP, marine renewable technologies, etc. which are at various developmental stages to demonstrate their commercial viability [3, 4]. Power generation using DER systems is used as an alternative or an enhancement to the traditional means of power generation. DER systems are increasingly adopted in various countries that aim to reduce the carbon footprint of their energy generation. Moreover, the trend of the electricity transmission is increasingly skewing towards micro-grids. This provides an increased

impetus for the development of the current DER system application for different loads and various renewable energy sources worldwide.

1.1.2. Motivation

Irrespective of the types of distributed generation sources considered for power generation, some form of energy regulation system is required to convert the power generated into useful power that can be directly connected to the load. The need for energy regulation is primarily due to the impact of environmental conditions on the energy harvested from these sources. Therefore, even though the output energy from these sources are electrical, connecting it directly to the utility mains or the utility grid is not advisable. The energy regulation system consists of a power controller and a power converter interfaced by sensors and semiconductor driving circuits. The power controller performs operations including maximum power point trackers, grid synchronization and fast dynamics to the system. Then the power converter receives the signal and performs the conversion of magnitude, frequency and phase of the electrical quantities before smooth grid connection is affected. Figure 1.3 depicts a typical structure of the load integrated to various DER system.

Figure 1.3 DER Electricity Paradigm

Generally, the dc-ac power conversion illustrated in Figure 1.3 involves a dc-dc boost converter and a dc-ac voltage buck inverter. Such series connection of two electronic converters gives rise to a two-stage power conversion. This might result in using more components than necessary, thus, incurring a high system cost. Therefore, to reduce the required number of components several single-stage conversion strategies were proposed. One such proposed method for single-stage power conversion is Z-Source inverter. Therefore, the

main motive of this research is to eliminate the dc-dc-ac stages of power conversion. This entails further investigation into dc-ac power conversion.

1.2. Objectives and Contribution

With the motive of integrating DER systems to the recently popular Z-Source inverter, the following contributions were achieved:

- *Exploring various modulation strategies for ZSI:* This research focus on both the two-level and three-level Z-Source inverters. Hence, proper modulation techniques need to be implemented to ensure that shoot through states are inserted properly. Therefore, to understand the performance of modulation techniques, comparisons between techniques are essential. Furthermore, the reasons for choosing certain modulation methods are detailed in the subsequent chapters.
- *Analysing the possibility of integrating the Z-Source topology to basic NPC:* The topology consists of two Z-Source networks connected to different dc sources and an inverter circuit. The two Z-Source networks provide voltage boost through proper pulse width modulated algorithm. The existing topology is reconfigured to a novel non-ideal topology, to consider the voltage drop across circuits. Mathematical analysis needs to be performed subsequent to every reconfiguration.
- *Propose a new modulation method for Dual Z-Source NPC:* A new modulation method based on the carrier comparison scheme is proposed for controlling the shoot through states of the inverter. The proposed method has to be tested for both the ideal and non-ideal circuits of the Z-Source inverter.
- *Investigate the performance of fuel cell coupled with inverters:* Despite low output power, fuel cells are preferred for power generation. As the research application is mainly DER oriented, a suitable fuel cell stack is designed. The fuel cell is subsequently connected to a traditional dc-dc boost converter followed by voltage source inverter, and a Z-Source inverter. The performances of both the converters are evaluated and presented in this thesis.

1.3. Organisation of the thesis

The thesis is organised into seven chapters and a brief description of each chapter is presented below to render an overview of the thesis.

Chapter 1, reports the background and motivation for this research. A brief introduction on the necessity of the DER systems. The subsequent research objectives focus on some of the components typically utilised when designing a DER system. Following that, the contribution and organisation of the thesis are elaborated to provide an overview of the research.

Chapter 2 reviews on the various two-level voltage buck-boost converters topologies, the existing multilevel inverter topologies, and their respective modulation methods. Therefore, further analysis would yield insights in integrating the conventional two-level and multilevel topologies to the Z-Source inverter. This is underscored by the renewed focus on the researching the Z-Source inverter recently. Additionally, the classifications of the DER systems and the renewable energy sources are presented. As fuel cell is one of the principal components of this research, a review on the ideology of the fuel cell system is presented to provide information on the general concepts of fuel cells.

As Z-Source is the focus of the research, Chapter 3 provides details about the classification of two-level inverters. Along with the classification, comprehensive comparisons of various modulation methods for two-level inverter are discussed to choose a proper modulation method to control the switching sequence of a two-level ZSI with fuel cell. In addition, this chapter provides topological development and modulation methods of a three-level Z-Source neutral point clamped inverter.

In Chapter 4, Z-Source multilevel inverter designed by connecting two Z-Source networks between two isolated dc sources and the inverter circuitry is represented. A new modulation method is proposed for Dual Z-Source network to provide easier implementation and required voltage boosting. The concept of the modulation method is explained and the theoretical findings are compared with the key results.

Chapter 5 provides the reconfigured topology of the Dual Z-Source network NPC inverter. This topology is designed considering the non-ideal circuit i.e. voltage drops across the circuit are taken into account. The mathematical analysis of the reconfigured topology is also presented. The proposed modulation method in Chapter 4 is implemented to the non-ideal circuit and the simulation and experimental findings are reported.

As a part of DER system, the two-level Z-Source inverter is integrated to a fuel cell, which is designed based on available industrial data. Chapter 6 reports the performance analysis of the traditional boost converter and two-level Z-Source inverter integrated to the PEMFC stack. Different case studies wherein variation of variables including, constant fuel flow rate and variable fuel flow rate are analysed and the effect of these converters on

the fuel cell output are studied. Furthermore, the simulation results for all the analysis provide further information on the performance of this framework.

Lastly, Chapter 7 presents the conclusion of the thesis, and suggestions on possible future research are discussed.

Figure 1.4 Structure of the Thesis

The overall structure of the thesis is shown in Figure 1.5

Chapter 2 Literature Review

2.1. Voltage Buck-Boost Concepts

Voltage buck-boost energy conversions are achieved either by two-stage or single-stage conversion methods. The two-stage energy conversion topology includes a dc-dc boost converter added to the front end of a dc-ac voltage source inverter or a dc-dc buck converter to the front end of a dc-ac current source inverter. Single-stage conversion uses lesser number of active or passive components unlike the two-stage energy conversion [5-14]. Some of the widely used converters includes the step down or buck converter, step up or boost converter, Cuk, SEPIC and Z-Source converters. In this section, multiple voltage buck-boost inverters are reviewed.

2.1.1. Boost Converter

Figure 2.1 provides the foundation for the two-stage topology, wherein two fundamental converter modules are merged for energy conversion. The advantages of this converter is the simplicity, and independent control. It also includes a decoupling capacitor in the dc-link for buffering the converter modules. Adding a line frequency to the ac terminals enables to achieve a higher gain. This may also be achieved by adding a dc-dc boost converter to the dc-link terminals [15]. When compared to the normal six-switch converter, boost converter has one additional switch. Inclusion of this additional switch, its corresponding driving circuits and other passive components have rendered the boost converter with multiple components. To redress some of these issues, single-stage buck-boost converters that use lesser components were developed.

Figure 2.1 Two-stage energy conversion with a front end dc-dc boost converter

2.1.2. Cuk-derived Buck-Boost Converter

As mentioned earlier, in order to create solutions for the two-stage energy conversion, single-stage buck-boost converters like Cuk and SEPIC converters were introduced. These converters can be placed in between the source and the six-switch inverters to provide single-stage conversion [16]. The topology of the Cuk converter is illustrated in Figure 2.2(a). The converter includes a six-switch inverter, an inductor, a capacitor and an additional switch. When compared with the two-stage converters, these single-stage converters possess fewer passive components, and therefore are compact with good boosting ability. In addition, variants like diode-assisted Cuk converter are derived using the same operating principles [17]. An overview of the operating principle of the Cuk buck-boost converter is discussed to demonstrate the process of achieving voltage boost. The Cuk converter operates in two different states: Non-Shoot Through state (NST) when the switch (S_{CUK}) is turned 'on' and Shoot Through (ST) state when the switch (S_{CUK}) is turned 'off'.

Figure 2.2 Cuk-derived buck-boost converter (a) topology (b) equivalent circuit when switch is 'on'
 (c) equivalent circuit when switch is 'off'

a) Non-Shoot Through State

The equivalent circuit of the NST state is depicted in Figure 2.2(b). During this state, the switch (S_{CUK}) is turned 'on'. The inductor current I_L flows through the switch and the dc source V_{dc} charges the inductor at the rate of V_{dc}/L . During this state, the dc-link of the inverter will be in either an active state or a zero state. There

are six active states and two zero states in the NST state in the inverter. For active state, energy from capacitor C will be discharged to the external ac load.

b) Shoot Through State

For this state, the switch (S_{CUK}) turns 'off' as illustrated in Figure 2.2(c). The inductor current I_L now discharges through the dc source, capacitor C (charging it), and all the anti-parallel diodes of the inverter at the rate of $(V_{dc} - V_C) / L$, where V_C represents the voltage across the capacitor. During this state, the dc-link of the inverter is 'shorted', resulting in non-transference of energy to the ac load. This is similar to the operation of the inverter when it functions in either one of the two zero states.

2.1.3. SEPIC-derived Buck-Boost Converter:

SEPIC converter is also placed in front of the six-switch inverter to provide single-stage buck-boost conversion. Therefore, Cuk and SEPIC converter share similar circuit [16]. The topology of the SEPIC derived buck-boost converter is illustrated in Figure 2.3(a). Cuk and SEPIC converters possess the same number of components, differing in their arrangement in the circuit. Like Cuk converter, SEPIC-derived buck-boost converter also has two distinct operating states.

Figure 2.3 SEPIC-derived buck-boost converter (a) topology (b) equivalent circuit when switch is 'on' (c) equivalent circuit when switch is 'off'

a) Non-Shoot Through State

The equivalent circuit of the SEPIC-derived buck-boost converter during this state is depicted in Figure 2.3(b), which shows the switch (S_{SPC}) is 'on' and hence the inductor current flows through the dc source and the switch at the rate of V_{dc}/L . The dc voltage and capacitor voltage serves the ac load and voltage across the load will be $(V_{dc} + V_C)$, if the inverter is in any one of the six active states.

b) Shoot Through State

This state is introduced by turning 'off' the switch (S_{SPC}) as portrayed in Figure 2.3(c). During this state, the dc voltage source is isolated from the inverter bridge. The inductor current then flows through the capacitor C and all the anti-parallel diodes of the inverter. The inductor current discharges at a rate of $-V_C/L$. The dc-link of the VSI bridge is shorted and subsequently the ac output voltages are zero. The time duration of the NST zero states can be adjusted to vary the voltage gain.

2.1.4. Z-Source Buck-Boost Inverter

An impedance power converter following a single-stage energy conversion has been introduced [18]. A simple representation of the Z-Source inverter is illustrated in Figure 2.4. As Z-Source inverter (ZSI) is the main objective of the research, a detailed description of the inverter is explained in the next chapter.

Figure 2.4 General representation of ZSI connecting source to load

Comparisons of the Z-Source inverter with the other buck-boost converters are tabulated in Table 2.1.

Table 2.1 Comparison of ZSI with dc/dc/ac and dc/ac converters

	DC/AC/DC converter		Cuk-derived	SEPIC-derived	Z-Source
	DC/DC converter	VSI			
Input Voltage	DC	DC	DC	DC	DC
Output Voltage	DC	AC	AC	AC	AC
Voltage Gain	Boost	Buck	Boost/Buck	Boost/Buck	Boost/Buck
Number of Inductors	1	0	1	1	2
Number of Capacitors	1	0	1	1	2
Number of Diodes	1	0	1	1	1
Number of Switches	1	6	7	7	6

The single-stage topology to achieve voltage boost/buck abilities and fewer high-frequency switching devices provides the ZSI with substantial advantages over the traditional boost or VSI. Furthermore, ZSI protects the devices from damage when the upper and lower switches of a leg are simultaneous switched 'on'. Another significant advantage of the ZSI topology is that a single controller is sufficient to perform inverter switching. Therefore, the complexity of the circuit is substantially reduced. Unlike Cuk and SEPIC-derived inverters, dc-link current of the inverter does not flow through the anti-parallel diode during the ST state. Instead, the current flows through the switches that are shorted. The dc-inductors limits the current through the shorted switches, thereby preventing any damages to the switches. Therefore, ZSI exhibits lesser electromagnetic noise when compared to other single-stage converters. Due to these advantages, ZSI is considered as a safer topology and dead-time protection is rendered redundant. In addition, from Table 2.1 it can be surmised that ZSI needs more passive components when compared to other converters, which may result in greater conduction losses. However, the parasitic resistors are usually small, that the effects may be neglected.

2.2. ZSI developed topologies

Even though ZSI is advantageous over other voltage buck-boost topologies, there are few drawbacks associated with the Z-Source inverter. The principle drawbacks are,

- Discontinuity in the input current during boost mode

- Difficulties in suppressing the inrush current caused by the impedance network at start-up

The topological configuration of the ZSI has been changed in order to ameliorate one or more drawbacks. Some of the developed topologies are reviewed in the following sub-sections.

2.2.1. Quasi ZSI

The voltage fed QZSI (Quasi ZSI), identified as the improved version of the traditional ZSI, was proposed in [19]. The improvements of QZSI over ZSI are the changes in: position, connection of capacitors and inductors of the impedance network. In addition to the aforementioned improvements, QZSI lowers DC voltage with continuous input current on capacitor C_1 , and depicted in Figure 2.5.

Figure 2.5 Topology of Quasi ZSI with continuous input current

Figure 2.6 Topology of Quasi ZSI with discontinuous input current

The QZSI may also be fitted with a lower DC voltage and discontinuous current on capacitors C_1 and C_2 , and depicted in Figure 2.6. It is determined that the components used in QZSI are identical to the traditional ZSI, with few modifications as discussed above. The topologies illustrated in Figures 2.5 and 2.6, features a common DC rail and can be rendered bidirectional by replacing the diode D1 with a bidirectional switch.

2.2.2. Embedded ZSI

Unlike the traditional ZSI, EZSI (Embedded ZSI) has a second order LC filter placed before the input diode. Though addition of filter increases the cost of the inverter, L. Poh Chiang et al., [20] claims to have designed EZSI primarily to avoid high-frequency current ripple flowing into the DC source under load. This would ultimately reduce the dynamics of the power source. The ZSI is termed as embedded ZSI because it embeds the existing inductors and capacitors to form the LC filter as depicted in Figure 2.7. The developed prototype possess an advantage wherein the capacitor size (voltage rating) can be reduced significantly, without affecting the voltage boost. However, the prototype has a disadvantage that it requires two input dc sources.

Figure 2.7 Topology of Embedded ZSI

2.2.3. Improved ZSI

Improved ZSI (IZSI) proposed in [21], addresses the following two problems found in the traditional ZSI:

- Z-Source capacitors imposes voltage stresses similar to the DC source, therefore, increasing the need for high-voltage capacitors, which results in higher cost of the system
- The voltage and current surge caused by the capacitors and inductors of the impedance network cannot be suppressed and may destroy the device

Thus, to overcome these drawbacks, the prototype depicted in Figure 2.8 was designed. The changes to the traditional ZSI to obtain Improved ZSI are:

- 1) The change in position of the impedance network to the back end of the inverter
- 2) The change in position and connection direction of the input diode

Figure 2.8 Topology of Improved ZSI

2.2.4. T-Source Inverter

The above mentioned three types of topologies were aimed at maintaining the number of elements, but changing the positions of the same to eliminate the drawbacks of the existing ZSI. Therefore, TSI (T- Source Inverter) [22] is modeled in order to reduce the number of elements used in the traditional ZSI. In Figure 2.9, the traditional impedance network is replaced with a modified network, which is a low leakage inductance transformer and one capacitor. Similarly, the impedance network may also be replaced using the other passive elements in [22]. Notably, the output voltage of the device can be manipulated by using a transformer at any transformer ratio besides 1:1.

Figure 2.9 Topology of low-leakage-inductance-transformer-based TSI

2.3. Pulse Width Modulation methods for Z-Source inverters

Numerous pulse width modulation techniques have been developed for the voltage source inverter. This inverter has six active states when the load is connected to the dc voltage and two zero states when the load is shorted through the upper or lower switches of any leg. The traditional control of the inverter is simple. It involves the comparison of the output signal and the reference signal. The outcome provides the gating signal for the switching devices. Through the traditional control, low switching losses can be achieved easily because there are only six switching for a single fundamental frequency cycle. As the inverter uses electronic switches, the output voltage can be controlled. The harmonics can be optimised by doing multiple switching within the inverter. The basic PWM principle to control the output voltage based on a triangular carrier method is illustrated in Figure 2.10.

Figure 2.10 Traditional carrier based PWM without ST zero states

From Figure 2.10, it can be observed that in a traditional PWM control, every switching cycle consists of two non-zero states and two active states; thereby achieving the desired voltage. The traditional PWM technique is highly used in cases where the dc voltage is sufficiently high to generate the desired ac voltage. However, when the ac voltage is large, additional modification is required to boost the dc voltage to equalise the ac output voltage. The modification includes the insertion of ST state in the PWM control as demonstrated in Figure 2.11. Inserting this new state does not cause any difference in the operation of the traditional inverter. Each phase legs' devices gates are switched 'on' and 'off' per switching cycle. The active states of the traditional inverter remain unchanged. The ST zero states are evenly inserted into the NST state at each phase without actually changing the time interval. This additional inserted state provides the boosting capability to the inverter. In addition, the switching frequency of the Z-Source inverter is six times the switching frequency of the traditional inverter. This greatly reduces the inductance required in the impedance network.

Figure 2.11 Modified carrier-based PWM with ST zero state evenly distributed

The ST state is the additional state of the Z-Source inverter. Inserting the ST state in the PWM control method for ZSI is a significant challenge. After the development of Z-Source inverter, few methods have been proposed for the insertion of ST states in the inverter.

The various proposed modulation methods for inserting ST states are

- Simple Boost Control
- Maximum Boost Control
- Maximum Constant Boost Control
- Modified Space Vector Modulation Boost Control

2.3.1. Simple Boost Control method

The Simple Boost Control method (SBC) was developed by [18]. This method involves the comparison of two straight lines with the triangular wave as shown in Figure 2.12. The two straight lines, which should be greater than or equal to the peak value of the three-phase references, are used to insert ST states in the modulation.

These lines are compared with the triangular waveform. When the waveform goes above the upper line or goes below the bottom line, the additional state is introduced and the circuit enters into ST mode. Even though this method is simple, it causes additional voltage stress on the switches. This stress is attributed to the fact that some traditional zero states are not utilised.

Figure 2.12 Simple Boost Control method

2.3.2. Maximum Boost Control method

As the SBC method imposes voltage stress on the switches, it is necessary to minimise the stress but also to maintain the voltage gain. This can be achieved by increasing the ST duty ratio. This maximization technique makes sure that all the traditional zero states are utilised thereby changing every zero states to the ST state [23]. Unlike the SBC method, the Maximum Boost Control (MBC) method does not possess two lines. Instead, the triangle waveform is directly compared with the three-phase sinusoidal waveforms as illustrated in Figure 2.13. When the triangular wave is either greater than the maximum reference sinusoidal curve or smaller than the minimum of the reference wave, the circuit enters into a ST state. In this method, the duty ratio is increased to the maximum possible value. Therefore, it varies almost six times the output frequency, which results in the injection of high ripple in the inductor current and the capacitor voltage.

Figure 2.13 Maximum Boost Control method

2.3.3. Maximum Constant Boost Control method

The important task lies in reducing the ripple current and voltage in the circuit during the ST. Also if the volume and the cost have to be reduced then it is necessary to maintain a constant ST duty ratio. With that said, in order to reduce voltage stress, the ST duty ratio must be as high as possible thereby providing maximum boost control. All these drawbacks of the constant and maximum ST method are overcome by the Maximum Constant Boost Control (MCBC) method [24]. This method reduces the ripples in the inductor current and the capacitor voltage without increasing the inductances and capacitances. Additionally, this provides the maximum boosting capability while maintaining a constant duty ratio. This is achieved by using modified reference lines as illustrated in Figure 2.14, which maintains a constant interval between them thereby providing a constant boost ratio. These modified reference lines are similar to the peak three-phase AC voltages. These are compared with the triangular wave. When the triangular wave is greater or lesser than the modified reference lines, the inverter enters into the ST mode of operation.

Figure 2.14 Maximum Constant boost control

2.3.4. Modified Space Vector Pulse Width Modulation

The traditional space vector pulse width modulation is considered as the most suitable best among all the available modulation techniques for the inverter. This modulation technique is widely used for variable-frequency drive applications. For a conventional three-phase bridge inverter, there are 8 permissible switching states.

Table

2.2 gives an overall idea of the switching states and the corresponding phase voltages of the conventional inverter.

Table 2.2 Summary of Inverter Switching States

State	v_{an}	v_{bn}	v_{cn}
000	0	0	0
001	$-V_d/3$	$-V_d/3$	$2V_d/3$
010	$-V_d/3$	$2V_d/3$	$-V_d/3$
011	$-2V_d/3$	$V_d/3$	$V_d/3$
100	$2V_d/3$	$-V_d/3$	$-V_d/3$
101	$V_d/3$	$-2V_d/3$	$V_d/3$
110	$V_d/3$	$V_d/3$	$-2V_d/3$
111	0	0	0

As described previously in this section, the space vector PWM is the most common technique and is widely utilised in current-regulated pulse width modulation inverters due to its relatively low current harmonics [25-27] and higher modulation index. In-order to use this pulse width modulation scheme for Z-Source inverter, the

conventional space vector PWM needs to be modified. There are 8 vectors $V_0 - V_7$ utilised in a conventional space vector PWM. Among the available vectors two vectors V_0, V_7 are assigned as zero vectors and $V_1 - V_6$ are active vectors. Each vector is assigned to a state and the eight permissible states of the inverter and the corresponding phase voltages are listed in Table 2.2. Figure 2.15 introduces the switching patterns of the traditional and modified space vector PWM [28]. This figure is plotted under the assumption that the vectors V_1 and V_2 are applied for a time interval of T_1 and T_2 respectively and the zero vector is applied at time T_0 for a sampling period of T_s . In the figure, a new time duration T is added to the already existing time periods T_1, T_2 and T_0 . This additional time T added to the conventional space vector PWM result in the boosting of the dc-link

Figure 2.15 Switching pattern for the PWM

- (a) Switching pattern for traditional SVPWM
- (b) Switching pattern for MSVPWM

voltage of the Z-Source inverter thereby, producing the desired ac output voltage.

2.4. Multilevel Inverter Topologies and Modulation Schemes

Power converters with two-level and multi-level configuration have been applied widely for dc-ac energy conversion. They are, ac motor drives [29-32], uninterruptable power sources [33-36], interfacing renewable or distributed power systems [37-40], and electric vehicles [41-43]. In general, most of the applications involve two-level inverters. However, many industrial applications require high power, however, some appliances requires medium or low power for their operation. The multilevel inverter was introduced in 1975 and the main motive is to deliver a high output power from a medium voltage source. Sources like batteries, super-capacitors,

solar panel, fuel cells are some of the medium voltage sources. Among the voltage source and current source inverters, VSI has the advantages like high switching speed and faster transient response. CSI, when used as switching devices, involves complex gate circuitry and limited switching frequency, thereby contributing to more losses than VSI [44-45]. Therefore, in the following section, some of the voltage source inverter topologies are reviewed.

2.4.1. Traditional 2-L Inverter

The topology of the traditional 2-level voltage source inverter is presented in Figure 2.16. These inverters are the highly preferred for the induction motor drive applications given its fast switching characteristics. In order to eliminate low order harmonic component, two-level inverter needs to be operated at high switching frequency [46]. Operating at high switching frequency can reduce the filter size. However, it causes high dv/dt across the switches. As a result, these semiconductor switches experience voltage spikes which are higher than the dc voltage. Therefore, to increase the voltage rating of two-level voltage source inverters for high power applications, additional semiconductor switches are needed. This may also cause voltage distortion when the switches are not operated instantly.

Figure 2.16 Traditional Two-Level Inverter Topology

2.4.2. Multilevel inverters

To overcome drawbacks such as the increase in the power and switching range of the two-level inverters, multilevel inverters are developed [49-59]. Some of the advantages of the multilevel inverters are:

- MLI can be operated at both higher switching frequencies and lower switching frequencies

- Lower switching frequency means lower switching losses as the number of levels in output voltage increases
- THD is reduced as the number of output voltage levels is increased
- MLI can draw input current with low distortion
- Selective harmonic elimination technique along with multilevel inverter topology results in low total harmonic distortion in the output waveform without using any filter circuit
- Due to low conduction loss, lower rating semiconductor devices can be used for low and high power inverter applications

Due to the aforementioned advantages, multilevel inverters can be used for high power applications and the output voltage waveform of these inverters is obtained from a strata of individual voltage levels [60-76]. Among all the discussed multilevel inverters so far, diode-clamped inverter, flying capacitor inverter and H-bridge inverter. As this research includes integration of Z-Source with multilevel inverter, the following section presents an overview of the most commonly adopted inverters.

a) Multilevel Diode-Clamped Inverter

The topology of the three-level diode-clamped inverter, commonly known as neutral-point-clamped (NPC) is highlighted in Figure 2.17. This inverter uses diodes to provide the multiple voltage levels through the different phases to the capacitor bank that are connected in series. The clamping diodes transfer the dc-link voltage stress evenly among the semiconductor switches [77-80]. The significant drawbacks of diode-clamped inverter are twofold: maximum output voltage of the inverter is half the input dc voltage and dc-link capacitor voltage imbalance. The former can be improved by increasing the number of switches, diodes and capacitors. The dc-link capacitor voltage imbalance can cause low-order harmonic distortion and additional voltage stress across the capacitors and switches. To address this drawback, various neutral point balancing techniques have been proposed. Despite these serious drawbacks, this type of inverter exhibits high efficiency. This is attributable to the fundamental frequency that is utilised for all switching devices. These inverters are widely used in applications like high voltage ac and dc transmission lines, static var compensation, high voltage system interconnections and variable speed motor drives.

Figure 2.17 Multilevel diode-clamped inverter

b) Multilevel Flying Capacitor Inverter

Similar to multilevel diode-clamped inverter, multilevel flying capacitor inverter has been the focus for many research studies [81-87]. The topology of the multilevel flying capacitor inverter for a three-level is illustrated in Figure 2.18. The configuration includes a series connection of capacitors, which transfers limited amount of voltage to the semiconductor switches. The output voltage of the inverter is half the dc-link voltage and the inverter produces three distinct voltage levels. The voltage levels are positive half dc-link voltage, zero and negative half dc-link voltage. In order to achieve higher output voltage levels more number of capacitors are needed, which results in an unwieldy system size. Even though the number of capacitors increases, with proper modulation scheme, capacitor balancing can be achieved without any constraint. Induction motor control using direct torque control circuit, static var generation, converters with harmonic distortion capability, and sinusoidal current rectifiers are some of the applications incorporating the multilevel flying capacitor inverter topology.

Figure 2.18 Multilevel flying capacitor inverter

c) Cascaded H-bridge Multilevel Inverter

The cascaded H-bridge multilevel inverter consists of series of power conversion cells in series [88-91] and uses fewer number of components in each level compared to diode-clamped and flying capacitor multilevel inverter topologies. The topology of a multilevel H-bridge inverter is shown in Figure 2.19. The capacitors and the switches together form an H-bridge and each bridge is supplied by individual DC supply. Each H-bridge cell produces three voltage levels: positive dc, zero and negative dc. Multilevel cascade inverters are used to eliminate the bulky transformer required in case of the conventional multiphase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. However, these require large number of isolated voltages to supply each cell. Main application includes motor drives, active filters, electric vehicle drives, dc power source utilisation, power factor compensators, back-to-back frequency link systems and interfacing with renewable sources.

Figure 2.19 Cascaded H-bridge inverter

2.5. Pulse Width Modulation methods for MLI

Among several pulse width modulation techniques that had been proposed so far, the preferred and the most common method is the carrier-based Sinusoidal Pulse Width Modulation (SPWM) method. This basic technique provides an easy way to control the amplitude and frequency. It can suppress the harmonics present in the quasi-square wave. Besides that, to improve the overall performance of the inverter, many improvements were suggested to the SPWM method. One such proposed suggestion was the addition of an appropriate harmonic offset to the sinusoidal references, to raise the inverter modulation index to 1.15.

For NPC multilevel inverters, most carrier based modulation method are derived based on disposition techniques, where for a n -level inverter, $n-1$ carriers of identical frequency and amplitude are used to provide switching. The developed multicarrier techniques for controlling the multilevel inverters demonstrate the advantages of an optimized harmonic performance and a reduced common-mode voltage. Among the multicarrier techniques, the most widely used technique for controlling the NPC inverter is shown in Figure 2.20. From Figure 2.20, it can be surmised that two carrier signals used for modulation. Based on the arrangements of the carriers, they are the Phase Disposition (PD) scheme and Alternative Phase Opposition Disposition (APOD) scheme.

(a)

(b)

Figure 2.20 Carrier arrangements (a) PD scheme (b) APOD scheme

In Figure 2.20(a), the phase shift between the two carriers is zero, hence named as Phase Disposition scheme. This scheme has been proved to produce a better output waveform quality when compared with other carrier-based schemes [92]. Similarly, the phase shift between the carriers is 180° in Figure 2.20(b), thereby known as Alternative Phase Opposition Disposition [93]. Even though the APOD scheme produces poorer output waveform quality, it generates lower common mode voltage when compared to PD scheme. This property of APOD makes it more preferable for variable speed ac drives in industries, where large common-mode voltage tend to cause premature failure and induced leakage current to ground [94-95].

For cascaded inverters, the most common modulation technique requires continuous three-level PWM within individual cell and with phase shifter carriers between the cascaded inverters of each phase leg to achieve optimum harmonic cancellation within the phase leg. This modulation technique achieves the same spectral performance similar to the Alternative Phase Opposition Disposition for NPC inverters when the switching frequencies are normalized so that overall number of switching transitions per fundamental cycle would be the same.

As discussed previously, the main concentration in designing the modulation techniques is related to common-mode voltage. Therefore, along with carrier-based modulation techniques, researchers have proposed multiple modulation techniques that can further reduce the common-mode voltage [96]. Using these techniques, the reduction in the common-mode voltage is achieved by modifying the switching state patterns of pulse width modulation, and any additional hardware equipment is not required [97-98]. Therefore, the cost is relatively low, making this modification approach to be highly preferred when compared to other solution involving external hardware. Still one drawback associated with the modified approach is that the common-mode voltage produced by the inverter cannot be completely eliminated during the dead-time protection intervals. This results in the introduction of common-mode spikes to the inverter output voltage waveform by the dead-time effect. Until the dead-time protection is implemented, complete elimination of common-mode voltage is not possible with PWM modification approach. Alternatively, space vector modulation concepts are introduced to achieve operational functions, which are not feasible with carrier-based modulation. Even though space vector is flexible to modify the operational characteristics of the inverter, it needs huge memory and complex computation.

2.6. Distributed Generation Networks

2.6.1. Distributed Energy Resource Technologies

Generally, DER refers to those energy resources in which the power generation is directly connected to the medium voltage (MV) and low voltage (LV) distribution systems rather than bulk transmission systems [99]. DER systems include generation units like fuel cell, micro-turbines, photovoltaics, etc. Besides the aforementioned components, DER systems typical comprise of other devices including, storage units like batteries, flywheels, superconducting magnetic energy storage, etc. Figure 2.21 illustrates a schematic representation of the technologies that supports DER systems.

Figure 2.21 Technologies supporting DER systems

DER systems possess many advantages and disadvantages.

Advantages:

- Transmission and distribution losses are greatly reduced, enabling significant savings in energy procurement costs, capital costs and maintenance
- Reliability: Distributed Generation systems can ameliorate the impact of failures due to unexpected calamities
- Modular design provides inherent flexibility and upgradability, enabling the system to match the seasonal and diurnal variations in energy demand
- Diversity: Variety of power generating technologies can be used, thereby granting immunity from price shock and resource crunch
- Efficiency is greatly increased in on-site power generation by using waste heat for existing thermal process while using CHP (co-generation)
- Requires low capital costs, providing flexibility in financing and commissioning DER systems
- Locally available alternative and renewable energy sources can be used to generate power, reducing the need to import fossil fuels

Chapter 2 Literature Review

- Shorter planning, erection, commissioning and maintenance phases, enable quicker response to changes in the load
- When fully adopted, SO_x/NO_x emissions can be substantially reduced; hence, reducing smog causing Peroxy Acetyl Nitrate (PAN)
- Aids in easy transmission of energy to different sites

Disadvantages:

- High cost of the kWh for some fuels
- Electrical quality issues in terms of voltage and frequency control
- Reactive power issues
- Reliability – Solar or wind (seasonal variations)

The common types of distributed energy generation technologies are:

a) Micro-turbines

- An emerging technology that has been made commercially available, where the turbine, compressor and generator are on the same shaft which spins at high speed
- The output power ranges from 25kW to 500kW
- Net electrical efficiency is around 25% and if the waste heat is exploited then the overall efficiency can be increased up to 80%
- These turbines are fuelled by natural gas, propane, diesel or kerosene

b) Diesel Gen-sets

- Combination of diesel engine and electrical generator to produce electricity
- Commonly used for emergency back-up and also as peaking or load base units
- Power ranges from 50kW to 6MW
- Efficiency is around 33% to 40%

c) Gas Turbines

- Output power ranges from 1MW to 100MW
- Efficiency ranges from 30% to 40%
- Commonly used in industrial applications for powering CHP or as peaking units by utilities
- Fuel being used by these turbines are natural gas, distillate and methane

d) Internal Combustion Engines

- These engines convert the energy in the fuel to mechanical energy, which is used to turn a shaft in the engine
- This rotational motion is converted to electrical power by the generator
- Power ranges from 5kW (residential back up) to 7MW (large generators)
- Thermal efficiency ranges between 26% for a low compression engine and 34% for a highly modified engine
- Reciprocating engines use fuels like gasoline, natural gas, diesel fuel and other petroleum distillates

e) Fuel Cells

- These are quiet, clean and highly efficient on-site electrical generators, which utilise chemical reaction to produce electricity
- In addition to electrical power, fuel cell can also act as thermal energy source for water and space heating, or absorption cooling
- When compared to energy service costs for conventional sources, fuel cells can reduce the service costs by 20% - 40%
- Ideal fuel for fuel cells is hydrogen but some types use gaseous fuels
- Operating temperatures can vary between 80 and 1000 °C
- Depending on the electrolyte used, fuel cells can be classified into different types

Table 2.3 tabulates the different types of fuel cell technologies and its characteristics.

Table 2.3 Comparison Chart of fuel cell technologies

Types	Operating Temperature	Power Range	Electrical Efficiency	Applications
Proton Exchange Membrane Fuel Cell (PEMFC)	50 – 100 °C	3kW – 250 kW	53-58% (transportation) 25-25% (stationary)	Backup power, Transportation, DG
Alkaline Fuel Cell (AFC)	90 – 100 °C	10kW – 100kW	60%	Military, Space
Phosphoric Acid Fuel Cell (PAFC)	150 – 200 °C	200kW	>40%	DG
Molten Carbonate Fuel Cell (MCFC)	600 – 700 °C	250kW – 2MW	45-47%	Electric Utility, LDG
Solid Oxide Fuel Cell (SOFC)	600 - 1000 °C	225kW – 2MW	35-43%	Auxiliary power, LDG, Electric utility

2.6.2. Renewable Energy Source Technologies

Renewable Energy Source (RES) technologies can work in a grid-connected mode or as a stand-alone system in combination with an energy storage device like batteries. Some of the common technologies that are an alternative or an enhancement to the conventional power generation are:

a) Wind Turbines

- When the turbine with fan blades at the top of tower rotates due to the wind, a generator produces electrical power
- Power range for a single wind turbine vary from a few kW to 5MW
- This commercially available technology provides zero emissions in utility implementation; thereby allowing green power price premium
- As energy output varies with wind speed, this technology is not suitable for back-up or off-grid applications

b) Photovoltaic

- Solar cells convert light into electricity with no moving parts
- PV does not generate noise and is favored for residential application
- Compared to other technologies, PV has high installation costs and requires large space
- This technology can be used for peak shaving and are highly reliable
- When accompanied with energy storage, solar cells are well suitable for back up
- Power range predominantly depends on the availability of area for installation

c) Small Hydro

- A mature technology that can be well integrated at the distribution level
- Power ranges from a few kW to hundreds of kW's

d) Biomass

- Modern biomass energy converts organic waste from forestry and agriculture into fuel for producing electricity
- Using biomass generated fuels in cars results in less pollution compared to gasoline

The extraction of useful energy from these sources are dependent on the attributes of their availability and the demand for the extracted energy. For example, the availability of wind energy is highly variable and depends on the topography and the weather conditions of the location of the source. DER systems that incorporate multiple renewable sources of energy for power generation require reassessment of system operation. Implementation of such DER systems typically suffer from issues in their reliability, stability and power quality.

2.7. Fuel Cell

Distributed Energy Resources system uses various renewable sources like solar, wind, tidal farms, bio-fuels, solar thermal collectors, hydro power, etc., and play a vital role in the electric power generation and distribution system. Inherently, these are non-polluting and abundantly available. Additionally, the outputs from these sources are usually electrical. Therefore, the transmission and distribution of energy over long distance in an efficient way is can be achieved with relative ease. Currently, the most commonly used renewable energy

sources are solar and wind energy sources. These sources are available abundantly, but have limited efficiency. With the implementation of semiconductor devices, these problems are ameliorated. A similar technology that is increasingly adopted regardless of the low power generation is the hydrogen technology. Hydrogen is one of the elements that are available abundantly on earth. Moreover, hydrogen can be used for energy conversion with high efficiency. With these advantages, hydrogen is being used for utility power generation and vehicular application recently. Fuels cells are a class of electricity generators that uses hydrogen as a fuel and converts energy from hydrogen into electricity. Fuel cell is an electro chemical converter that generate power based on chemical reactions. The result of the chemical reactions is the production of electricity in the external circuit connected to it. Fuel cells are classified into many types based on the type of fuel used, electrodes and the construction. Some of the more commonly used fuel cells [100] are Proton Exchange Membrane Fuel Cell (PEMFC), Solid Oxide Fuel Cell (SOFC), Phosphoric Acid Fuel Cell (PAFC), Molten Carbonate Fuel Cell (MCFC), Direct Methanol Fuel Cell (DMFC). Of these types, PEMFC is chosen for further research; because these fuel cells can operate at relatively lower temperature, possess high power density. The most important feature of PEMFC is the output of these fuel cells can be changed quickly to meet the shifts in the load demand. The output range of a single PEM unit varies from several watts to several kilowatts. Thereby, allowing this fuel cell to be used in large scale applications. In recent years PEM systems are available to provide applications with primary and backup power, to power forklifts, many material handling vehicles and portable consumer electronics [101].

PEMFC demonstrates superior performance when used as Distributed Generation (DG) sources. When compared with other distributed generation sources like solar, and wind energy sources; fuel cell do not circumscribe to any geographic limitations. Therefore, it can be transferred and installed at any site required. One of the applications where the PEM fuel cell plays a vital role is the electric vehicle. Larger fascination towards these vehicles and low carbon emissions make PEM fuel cell attractive for vehicular applications. The main feature of PEM fuel cell is that it aids quick start, which makes it best suitable for electric vehicles. These fuel cells are considered as a good source of energy that provide reliable power at steady state. Nevertheless, these are not effective in responding to the load transients promptly. This is attributed to the slow internal processes. Therefore, to make a fuel cell operate effectively its transient properties should be analysed for different applications. Some research studies have been reported on the steady-state [102-108] and dynamic [109-113] fuel cell modeling. As these works usually focus on the electrochemical reactions, various researches

have been conducted to analyse the dynamic characteristics of the fuel cell, focusing mainly on the electrical characteristics of the fuel cell [114-117].

2.7.1. Fuel cell characterization

In PEMFC, the main fuel utilized is hydrogen, which is oxidized at the anode and oxygen is reduced at the cathode. Figure 2.21 illustrates the simplified representation of a PEMFC along with the corresponding internal voltage drops. Equations (2.1), (2.2) and (2.3), respectively, gives the anode, cathode and the total reactions occurring within the fuel cell:

Figure 2.22 Simplified representation of a PEMFC with its internal voltage drops

The fuel cell output voltage is a combination of reversible and irreversible voltage. The irreversible voltage represents the losses in the fuel cell. The main losses in the output voltage of the fuel cell are activation losses, ohmic losses and concentration losses. The output of the fuel cell is given by Equation (2.4) [100]:

$$V = E_{rev} + E_{loss} = E_{rev} + V_{act} + V_{ohmic} + V_{conc} \quad (2.4)$$

where,

E_{rev} –reversible cell potential.

$E_{loss} = V_{act} + V_{ohmic} + V_{conc}$ –irreversible cell potential or losses in the cell (V).

a) Activation losses

These losses are dependent on the rates of the chemical reaction that happens on the surface of the electrode. A portion of the generated voltage will be lost due to the chemical reaction. These losses are directly proportional to the cell current. The chemical reaction occurs rapidly resulting in fewer activation losses when the fuel cells are operated at high temperatures. However, as PEMFC operates at low temperatures, these losses are considerable. The voltage drop due to the activation losses can be characterized by:

$$V_{act} = A. \ln \left(\frac{i}{i_0} \right) \quad (2.5)$$

Practically in fuel cells, some fuel will diffuse from the anode directly through the electrolyte to the cathode leading to fuel cross-over. This reaction does not contribute to the generation of current. Even though the electrolyte is meant for transporting ions, in few instances it transports electrons, thereby producing internal current. The fuel cross-over and internal currents are challenging to measure, yet the voltage drop due to the losses is considered by adding an additional constant current i_n to the previous equation. The following equation provides the voltage drop:

$$V_{act} = A. \ln \left(\frac{i + i_n}{i_0} \right) \quad (2.6)$$

where

A Tafel equation constant

i Current density (mA/cm²)

i_0 Exchange current density

i_n Internal current density

b) Ohmic losses

The ohmic losses are contributed by the electrical resistance of the electrodes, resistance to the ions movement in the electrolyte, and the resistance of the cell interconnects. The voltage drop due to the ohmic losses is directly proportional to the current density. Therefore these losses are characterized by:

$$V_{ohm} = i \cdot r \quad (2.7)$$

where

r Area specific resistance ($k\Omega cm^2$)

c) Concentration losses

These losses occur when a change in the concentration of the reactants occurs (in PEMFC - hydrogen and oxygen). During the operation of the fuel cell, there will be a reduction in hydrogen concentration as more hydrogen is consumed with increase in the current drawn from the fuel cell. Similarly, in the cathode, reduction of the oxygen concentration occurs while current is drawn from the cell. These losses become more significant at higher current rates as more hydrogen and oxygen will be involved in the process. The concentration loss is characterized by:

$$V_{conc} = m \cdot \exp(-ni) \quad (2.8)$$

where

m, n constants of the concentration loss parameters

The electrical characteristics of a fuel cell can be explained by the polarization curve which depicts the change in the fuel cell output voltage with respect to the current density. The typical polarization curve for a fuel cell is depicted in Figure 2.22, which explains the chemical and electrical phenomenon within the active region of the fuel cell. The three different losses contributing to the voltage drop in the fuel cell that occurs during current densities less than $50 mA/cm^2$ are activation losses, current densities in the range of $50-900 mA/cm^2$ are ohmic losses and current densities above $900 mA/cm^2$ are concentration or mass transport losses.

Figure 2.23 Polarization curve of a PEM fuel cell

2.8. Summary

This chapter begins with a brief review about the voltage buck-boost concepts, in which the two-stage power conversion and single-stage power conversion methods are described. The two-stage power conversion involves a dc-dc buck/boost converter as a front end to the traditional voltage source inverter. To overcome the drawbacks of two-stage energy conversion, single-stage buck-boost methods like Cuk, SEPIC and Z-Source inverters are introduced. A review on the operational characteristics of the inverters are presented. As Z-Source is the main course of study, a brief description of the various topologies and modulation techniques of Z-Source is reported and the detailed description of the inverter are presented in the next chapter.

The literature review continues with a review on the popular multilevel inverter topologies and the modulation methods for controlling them. The multilevel inverters are the prior choice for high or medium power applications. However, the multilevel inverter as a stand-alone system cannot perform voltage-boost operation. To incorporate the boost-capability to the inverter basics, the multilevel inverters should be integrated with the voltage buck-boost topologies. One such integration is carried out between NPC inverter and Z-Source buck-boost topology. The operational characteristics and the proposed modulation method for NPC are explained in the upcoming chapters of the thesis.

Chapter 2 Literature Review

Following the literature review on popular two-level and three-level voltage buck-boost topologies, this chapter proceeds with a basic explanation of the fuel cell. In the latter part of the research, a fuel cell stack is designed based on industrial parameters and integrated with the boost converter and two-level Z-Source inverter. The performance of the stack and the converters are simulated and the results are discussed.

Chapter 3 Z-Source Inverter

3.1. Introduction

As the focus of this research deals with renewable energy systems, inverters with both voltage buck and boost capabilities are needed due to the unexpected voltage fluctuation caused by environmental, climatic and geographical changes. The two traditional converters: Voltage Source Inverters (VSI) and Current Source Inverters (CSI) are classified based on the directions of power flow. In a typical Voltage Source Inverter, the dc voltage source is supported by a large capacitor. This inverter comprises of six switches and each switch has an antiparallel diode to provide current flow in both the directions and unidirectional voltage blocking capacity. Although these inverters are frequently employed, there are some limitations, wherein the dc input voltage has to be greater than ac output voltage. Therefore this inverter operates as either buck or boost based on the type of conversion required. In some applications where the dc input voltage is limited, an additional boost converter needs to be incorporated which increases cost and lowers efficiency. In addition, in this traditional VSI, the switches in the upper and lower phase of the same leg cannot be turned 'on' simultaneously. This results in a ST which would eventually destroy the devices. Additionally, an LC filter should be used to achieve sinusoidal voltage output. In CSI, the dc current source is a relatively large inductor, which is fed by some dc voltage sources. This inverter consists of six switches with a diode connected in series, permitting current flow in one direction while blocking voltage in both directions. Similar to the VSI, CSI requires additional converters for boosting or bucking operation that may increase cost and lower efficiency. A limitation of CSI is that the ac voltage to be greater than that of the dc input voltage. To achieve this operation the CSI acts as a boost or a buck converter based on the application but its operation is contrary to the operation of VSI. Another major drawback of this inverter is that any one of the switches in upper and lower legs has to be maintained in 'on' position at all times. If not maintained, then an open circuit of the inductor ensues and destroys the device. Mostly these traditional inverters operate as either a boost or a buck converter at a given point. In addition, they are sensitive to EMI noises.

The above-mentioned problems are overcome by using the Z-Source inverter proposed in [18]. Figure 2.6 in Chapter 2 shows the Z-Source inverter connected in general to the load. Unlike the traditional VSI and CSI, which uses a capacitor and an inductor respectively, this inverter consists of a unique impedance network that connects the source and the load or another converter. Z-Source inverter consists of two inductors L_1 and L_2 and

two capacitors C_1 and C_2 . The inductors and capacitors are connected in X-shaped thereby forming the impedance network that connects the source with the load or another converter. The source used for this converter may be a dc voltage source or a dc current source. The sources can be a fuel cell, an inductor, a capacitor, a battery, a rectifier or a combination of these sources. The switches used in the Z-Source inverter can either be a: combination of semiconductor devices and anti-parallel diode same as in voltage source; or be a series combination of switching devices and the diode as in current source inverter. Thereby, the drawback of VSI and CSI main circuits are interchangeable and is overcome by impedance inverter. The inductors used to form the impedance network can be a split inductor or two different inductors. The added advantage of this inverter is that it can be used for all kinds of ac-to-dc, dc-to-ac, ac-to-ac and dc-to-dc conversions.

Z source inverter is an attractive option for the power conversion given that the theoretical output voltage can be of any value regardless of the input. This feature ensures that the Z-Source inverter to outperform the traditional voltage and current source inverters. Also, traditional converters have only eight switching states (six active states when the dc voltage source is connected to the load and two zero states when the load is shorted by either the upper or lower switches in the three legs). The Z-Source inverter provides an additional state when the load is shorted, enabling this inverter to possess nine switching states. The additional state, which is named as the ST state, can be obtained by seven ways:

- Shoot through by shorting switches in any one phase leg
- Shorting the switches in any two phase legs
- Shorting all the devices in the three-phase leg

This additional state provides the Z-Source inverter with its unique buck-boost characteristic.

3.2. Two-Level ZSI

ZSI can be configured into VSI and CSI. The network structure is identical for both the configurations, with the impedance network connected between the source and the traditional VSI Bridge. This impedance network will provide the required voltage boost capability, while at the same time performing the voltage buck operation based on the requirement. The topologies of both the voltage-type and the current-type inverters and their operations are discussed below.

3.2.1. Voltage Type Z-Source Inverter

Even though both the voltage and current type converters are introduced at the same time, the voltage-type Z-Source inverters are increasingly preferred when compared with the current-type Z-Source inverter. Therefore, the modulation techniques, dynamics and sizing of voltage-type inverter have been thoroughly investigated recently. This inverter is commonly utilised in applications like motor drives, solar techniques, fuel cell and electric vehicle concepts. The operation of the inverter is unchanged despite the objective of the investigation. The operation involves the charging of the two inductors, which results in voltage boosting. The advantage of Z-Source over traditional two-stage inverter is that it can perform the boosting operation without an additional switch. The function of the additional switch is compensated by an extra state in the Z-Source inverter, at which both the switches in a single leg are turned 'on'.

Figure 3.1 Voltage type Z-Source inverter topology

The topology of the voltage type Z-Source inverter is illustrated in Figure 3.1. In traditional two-stage inverters, the shorting of the two switches in the same leg cause damages to the circuit. However, in the Z-Source inverter these damages are prevented due to the restricting action by the inductors. In the normal and the traditional converters, a dead time protection is needed to make sure the active switched are all turned 'off' before any other switch is turned 'on'. This happens for a few microseconds. During this period, a fly-back or fly-wheel diode is connected anti-parallel to every switch and provides a path for the current. In the Z-Source inverter, turning switches 'on' or 'off' in the same leg does not affect the circuit. Therefore, inverters may be operated without the encumbrances of dead time protection. Therefore, inverters are generally less sensitive to electromagnetic noises. Z-Source inverter operates in two modes: ST state and NST state. The operations of voltage-type Z-Source inverter in these two states are explained below.

The analysis of the Z-Source inverter is based on the assumption that the inductors L_1 and L_2 and the capacitors C_1 and C_2 possess the same value. If both the inductance and capacitance values are same, the impedance network attains symmetry. Therefore with a symmetrical structure (illustrated in Figure 3.1), the voltage across the inductors and capacitors are:

$$v_{L1} = v_{L2} = v_L \quad (3.1)$$

$$V_{C1} = V_{C2} = V_C \quad (3.2)$$

a) Shoot Through State

During this state, both the switches in any one of the three-phase legs is turned 'on'. The equivalent circuit of the inverter in this state is shown in Figure 3.2. During this state, the diode is reverse biased (open circuit) and a short circuit represents the inverter bridge.

Figure 3.2 Equivalent circuit of voltage-type Z-Source inverter during ST state

For a switching cycle T ,

The inverter operates in ST mode for a period of T_0 .

From the equivalent circuit shown in Figure 3.2, it is given that:

$$v_L = V_C \quad (3.3)$$

$$v_d = 2V_c \quad (3.41)$$

$$v_0 = 0 \quad (3.5)$$

b) Non-shoot through State

This operation of Z-Source inverter during this state is similar to the operation of the traditional inverters. This state represents any one of the six active states or the two null states of the inverter bridge. Figure 3.3 portrays the equivalent circuit of this state. During this state, the diode is forward biased and conducting and the inverter bridge operate in any one of the traditional eight states.

Figure 3.3 Equivalent circuit of voltage-type Z-Source inverter during NST state

The inverter operates in NST mode for a period of T_l .

Thereby, from the equivalent circuit of this mode as shown in Figure 3.3, it is given that:

$$v_L = V_i - V_c \quad (3.6)$$

$$v_d = V_i \quad (3.7)$$

$$v_0 = V_c - v_L = 2V_c - V_i \quad (3.8)$$

where,

v_L – voltage across the inductor

V_C – voltage across the capacitor

V_i –dc voltage source

$$T = T_1 + T_0.$$

For a time period T , the average value of the inductor is given by:

$$V_L = \overline{v_L} = \frac{T_0 \cdot V_C + T_1(V_i - V_C)}{T} \quad (3.9)$$

In a steady state, the average value of the inductor is zero. Therefore:

$$V_L = \frac{T_0 \cdot V_C + T_1(V_i - V_C)}{T} = 0 \quad (3.10)$$

Hence,

$$\frac{V_C}{V_i} = \frac{T_1}{T_1 - T_0} \quad (3.11)$$

Similarly, the average value of the dc-link voltage can be given by:

$$V_0 = \frac{T_1}{T_1 - T_0} V_i = V_C \quad (3.12)$$

From Equation (3.8), the peak value of the dc-link voltage can be modified as:

$$\widehat{v_0} = 2V_C - V_i = \frac{T}{T_1 - T_0} V_i = B \cdot V_i \quad (3.13)$$

where,

B –boost factor obtained from ST state.

$$B = \frac{T}{T_1 - T_0} \geq 1.$$

$\widehat{v_0}$ –peak value of the dc-link voltage.

By multiplying modulation index with half the peak value of the dc-link voltage generates the peak value of the ac output voltage. The peak value is given by Equation (3.14):

$$\widehat{v_{ac}} = M \cdot \frac{\widehat{v_0}}{2} \quad (3.14)$$

where M is the modulation index.

By substituting the value of $\widehat{v_0}$, Equation (3.14) becomes:

$$\widehat{v_{ac}} = M \cdot \frac{B \cdot V_i}{2} \quad (3.15)$$

From Equation (3.15), it is determined that the ac output voltage can be stepped up by adjusting the boost factor, which is evidently absent in the traditional voltage source inverters. The product of the modulation index and the boost factor determines the buck-boost factor.

$$B_B = M \cdot B \quad (3.16)$$

The boost factor B is determined by the modulation index M and can be controlled by the ST duty cycle of the zero state over the NST duty cycle of the active states of the pulse width modulation inverters. As the load terminal of the inverter is subjected to the same zero voltage during the ST state, this ST state does not disrupt the switching control of the inverter.

3.2.2. Current-Type Z-Source Inverter

The other topology of the Z-Source inverter, which is the current-type Z-Source inverter, is depicted in Figure 3.4. The current-type Z-Source inverter provides an additional operation with respect to the voltage type Z-Source inverter. In this inverter type, in addition to the (six active and two zero) NST states and ST state, the impedance network interrupts the current flowing through the current source inverter bridge which is achieved by turning ‘off’ all the switches. An advantage of the Z-Source inverter is that overvoltage does not occur during any interruption. Turning ‘off’ all switches leads to an open circuit, which introduces voltage-buck or current-boost functionality rather than the traditional voltage-boost or current-buck current source inverter; hence providing flexibility in control.

Figure 3.4 Current type Z-Source inverter topology

The current-type Z-Source inverters are not widely used when compared to that of voltage-type. However, this inverter has been investigated for its operation with some solar energy harvesting. Therefore, this inverter is also one of the considerations for renewable operation. The operating principle of the current-type Z-Source inverter is reviewed below.

a) Open Circuit State

As mentioned earlier, the distinctive characteristic of this inverter is its capability to prevent overvoltage during the open circuit state caused by the turning ‘off’ all switches. This characteristic is the reason for the boosting of the current during this state, which is accompanied with the usual current buck operation by the inverter bridge. The equivalent circuit of the open circuit state of the current-type Z-Source inverter is exemplified in Figure 3.5.

As observed from the figure, during the open circuit state, the diode is short circuited and the inverter bridge is open circuited. With this, the corresponding current expressions are given by:

$$I_{L1} = I_{L2} = I_L = i_{C1} = i_{C2} = i_c \quad (3.17)$$

$$i_d = I_L + i_c \quad (3.18)$$

$$i_o = 0 \quad (3.19)$$

Figure 3.5 Equivalent circuit of current-type Z-Source inverter during open circuit state

b) Non-Open Circuit State

This state occurs when the inverter operates in any one of the six active states or the three null states. During this state, the diode becomes reverse biased and blocks. This can be observed in Figure 3.6. Now the current relations are given by:

Figure 3.6 Equivalent circuit of current-type Z-Source inverter during non-open circuit state

$$i_d = I_i \quad (3.20)$$

$$i_c = I_i - I_L \quad (3.21)$$

$$i_o = I_L - i_c = 2I_L - I_{dc} \quad (3.22)$$

3.3. Implemented Modulation Methods for Two-Level Z-Source Inverter

The overview of the different pulse width modulation methods for the Z-Source inverter is explained in Chapter 2. In this thesis, the research focuses on instrumentation of the modulation methods for examining the working of the NPC Z-Source inverter. Based on the review of modulation scheme for multilevel inverters in Chapter 2, carrier-based modulation scheme is chosen. A new modulation method implementing the maximum constant boost control (MCBC) for inserting ST state has been proposed. Furthermore, the operation of fuel cell with boost converter and two-level Z-Source inverter were studied. So for this purpose, the inverter modulation is achieved by using maximum boost control method whose operating region is high compared to SBC method. Therefore Section 3.3 presents the theoretical relationships of multiple factors including, ST duty ratio, modulation index, boost factor, voltage gain and voltage stress, etc. that needs to be taken into consideration when choosing MBC or MCBC method for two-level or three-level Z-Source inverter, respectively.

3.3.1. Principle of Maximum Boost Control method

The ST state insertion for the maximum boost control method is depicted in Figure 3.7. As observed from Figure 3.7, the circuit enters the ST state whenever the triangular carrier wave is greater than or lesser than the maximum or minimum value of the reference curves (V_a , V_b , and V_c), respectively.

From the evaluation performed in [18], the SBC method is limited because the ST duty ratio obtained decreases with increase in modulation index. This in turn causes high voltage stress across the inverter switches. MBC method was proposed by [23] aiming to reduce the voltage stress across the semiconductor devices and to achieve high voltage boost for any given voltage gain caused by the SBC method. This method uses all zero states to boost the voltage with the active states remaining unchanged. Therefore, maximum boost and ST duty ratio for any given modulation index is now achieved. The sketch map of the maximum ST time interval is highlighted in Figure 3.8

Figure 3.7 Switching pattern for Maximum Boost Control method

Figure 3.8 Maximum boost control ST time interval

From Figure 3.8, it is observed that the ST time interval repeats every $\pi/3$. If the switching frequency is higher than the modulation frequency, the ST duty ratio over a switching cycle for the interval $(\pi/6, \pi/2)$ is given by:

$$D_0 = \frac{2 - (M \sin \theta - M \sin(\theta - \frac{2\pi}{3}))}{2} \quad (3.23)$$

In-order to obtain the voltage gain, the average value of the ST of the duty ratio can be expressed by simplifying the above equation within the limits $(\pi/6, \pi/2)$ and with respect to θ .

On simplification, Equation (3.24) is:

$$D_0(\theta) = 1 - \frac{\sqrt{3}}{2} M \cos\left(\theta - \frac{\pi}{3}\right) \quad (3.24)$$

From which, the boost factor is obtained as:

$$B = \frac{1}{1 - 2D_0} = \frac{\pi}{3\sqrt{3}M - \pi} \quad (3.25)$$

With the MBC method, the voltage gain can be obtained by using the modulation index M .

$$G = \frac{\widehat{v}_{ac}}{V_{i/2}} = MB = \frac{\pi M}{3\sqrt{3}M - \pi} \quad (3.26)$$

From the voltage gain equation (3.26) and voltage gain equation (3.15) of the SBC method, the maximum modulation index for a given voltage gain G is:

$$M = \frac{\pi G}{3\sqrt{3}G - \pi} \quad (3.27)$$

From Equation (3.27), the output voltage grows to infinity when modulation index reaches $\pi/3\sqrt{3}$. Figure 3.9 plots the graph wherein the relationship between the voltage gain and modulation index is detailed. The area under the curve represents the operating region of ZSI implementing MBC method.

Figure 3.9 Operating region of MBC

The voltage stress versus the voltage gain is illustrated in Figure 3.10. From Figure 3.10, for any given voltage gain higher values of modulation index can be used, which leads to minimum stress across the switches. Thereby, the voltage stress (V_s) across the switches for MBC is given by:

$$V_s = B.V_i = \frac{\pi V_i}{3\sqrt{3}M - \pi} \quad (3.28)$$

Figure 3.10 Voltage stress vs Voltage gain

3.3.2. Principle of Maximum Constant Boost Control method

During low frequency, the MBC method introduces ripples in inductor current, which may result in increased inductor size. If the ripples were eliminated (by maintaining a constant ST duty ratio), the volume and cost of the inverter can be reduced. From [24], MCBC relatively reduces stress on the semiconductor devices when compared with earlier methods. Moreover, for any modulation index value, greater voltage boost can be obtained. As illustrated in Figure 3.11, this method provides high voltage gain while the ST duty ratio is maintained constant always. This method consists of five modulation signals: three reference signals V_a , V_b and V_c and two signals (upper and lower) for providing ST V_p and V_n . As observed in other methods, when the triangular wave is greater or lesser than the ST signals, the circuit will enter into ST mode. Otherwise, the inverter switching is observed to follow the traditional PWM technique.

Figure 3.11 Switching pattern for Maximum Constant Boost Control method

In this control method, the boost factor should remain the same for every switching cycle in-order to maintain a constant boost. The challenge in this method is to achieve the maximum boost factor while maintaining it constant always. To calculate the boost factor, the entire cycle is assumed to be divided into two half periods:

$$\left(0, \frac{\pi}{3}\right) \text{ and } \left(\frac{\pi}{3}, \frac{2\pi}{3}\right).$$

For the first half period $\left(0, \frac{\pi}{3}\right)$, the upper and lower ST signals are expressed as:

$$V_{p1} = \sqrt{3}M + \sin\left(\theta - \frac{2\pi}{3}\right)M, \text{ for } 0 < \theta < \frac{\pi}{3} \quad (3.29)$$

$$V_{n1} = \sin\left(\theta - \frac{2\pi}{3}\right)M, \text{ for } 0 < \theta < \frac{\pi}{3} \quad (3.30)$$

During the second half period $\left(\frac{\pi}{3}, \frac{2\pi}{3}\right)$, the upper and lower signals are given by:

$$V_{p2} = \sin(\theta)M, \text{ for } \frac{\pi}{3} < \theta < \frac{2\pi}{3} \quad (3.31)$$

$$V_{n2} = \sin(\theta)M - \sqrt{3}M, \text{ for } \frac{\pi}{3} < \theta < \frac{2\pi}{3} \quad (3.32)$$

With the above-derived expression, the distance between the upper and lower envelope curves that determines the ST duty ratio for any given modulation index is always constant. Therefore maintaining a constant ST duty ratio to be constant. Ratio is expressed as:

$$\frac{T_0}{T} = \frac{2 - \sqrt{3}M}{2} = 1 - \frac{\sqrt{3}M}{2} \quad (3.33)$$

The boost factor B and the voltage gain G for the maximum constant boost control are computed using the expressions below:

$$B = \frac{1}{1 - 2\frac{T_0}{T}} = \frac{1}{\sqrt{3}M - 1} \quad (3.34)$$

$$G = MB = \frac{M}{\sqrt{3}M - 1} \quad (3.35)$$

The graph of modulation index versus voltage gain is plotted in Figure 3.12. From (40), the voltage gain reaches infinity when modulation index reaches $\sqrt{3}/3$.

Figure 3.12 Operating region of MCBC

The voltage stress for this method is given by:

$$V_s = B \cdot V_i = \sqrt{3} - \frac{1}{G} \quad (3.36)$$

Figure 3.13 Voltage stress vs Voltage gain

The voltage stress versus voltage gain graph for the maximum constant boost control is illustrated in Figure 3.13.

3.3.3. Comparison of the control methods for the two-level ZSI

The summary of all relations for the different ST control methods is tabularised in Table 3.1, in which D_0 represents ST duty ratio, M represents modulation index, B boost factor, G voltage gain and V_s represents the stress across the switches.

Table 3.1 Summary of different control methods expressions

Control Method	SBC	MBC	MCBC
D_0	$1 - M$	$\frac{2\pi - 3\sqrt{3}M}{2\pi}$	$1 - \frac{\sqrt{3}M}{2}$
B	$\frac{1}{2M - 1}$	$\frac{\pi}{3\sqrt{3}M - \pi}$	$\frac{1}{\sqrt{3}M - 1}$
G	$\frac{M}{2M - 1}$	$\frac{\pi M}{3\sqrt{3}M - \pi}$	$\frac{M}{\sqrt{3}M - 1}$
V_s	$(2G - 1)V_0$	$\frac{3\sqrt{3}G - \pi}{\pi}V_0$	$\sqrt{3} - \frac{1}{G}$

The operating region and the voltage stress of the SBC method is compared with MBC and MCBC methods and

Figure 3.14 Comparison of operating region of the different control methods

Figure 3.15 Comparison of voltage stress on switches by the different control methods

are the results are demonstrated in Figures 3.14 and 3.15, respectively.

3.4. Three-level Z-Source NPC Inverter

Three-level NPC inverters possess notable advantages like higher output waveform quality, lower voltage stress, lower common mode voltage, lower semiconductor losses and the power semiconductor devices needs to block half of dc-link voltage, when compared to a two-level inverter. Similar advantages apply to the Z-Source NPC inverter. The principle of boosting the voltage in the three-level Z-Source NPC inverter is achieved by utilizing the ST states, in which the upper two switches and lower two switches are gated 'on'. However, the main challenge is to connect the neutral point of the inverter. In order to achieve that, various topologies has been

proposed. Some of these topologies are the Single Z-Source Network Neutral Point Clamped (SZSN-NPC) inverter and Dual Z-Source Network Neutral Point Clamped (DZSN-NPC) inverter. Figures 3.16 and 3.17 depict the different topologies of Single Z-Source network NPC inverter. Figure 3.16 is the traditional way of creating the neutral point using split capacitor bank [120]; whereas Figure 3.17 indicates that, the neutral point is created between the split input-dc sources [122-123]. The operation of the circuits at active and zero states, and the corresponding voltage representation are discussed below.

Figure 3.16 Topology of Single Z-Source network with neutral point connected to split capacitor bank

Figure 3.17 Topology of Single Z-Source network with neutral point connected to split input dc sources

3.4.1. Split capacitor Single Z-Source Network NPC Inverter

The equivalent circuit of the SZSN-NPC inverter using split capacitor banks is illustrated in Figure 3.18, wherein the current source represents the inverter circuit and the load. In two-level inverter, there is only one ST

state. However, for three-level inverters, there are three ST states. Full shoot through (FST) where all the switches (e.g. S_{a1} , S_{a2} , $S_{a1'}$, $S_{a2'}$) in a single leg are turned 'on', upper shoot through state (UST) where the upper three switches are turned 'on' and lower shoot through state (LST) where the lower three switches are turned 'on'. The analysis of the Z-Source inverter is based on the assumption that the inductors L_1 and L_2 and the capacitors C_1 and C_2 possess the same values, represented as L and C , respectively. This assumption ensures the symmetry of the impedance network, which is explained by Equations (3.1) and (3.2). The dc-link voltage levels are represented by $V_{(+)}$, V_N and $V_{(-)}$. The equivalent circuits and the mode of operation for different states are explained below.

a) Non-Shoot Through state

The dc-link capacitors are represented as V_{d1} and V_{d2} , respectively. Figure 3.18 portrays the simplified representation of three-level Z-Source inverter during a NST state.

Figure 3.18 Three-level Z-Source NPC NST state (D_1 and D_2 are conducting)

During NST, the diodes D_1 and D_2 are conducting and $V_{d1} = V_{d2} = v_d$. Therefore, the voltage expressions for this state are given as:

$$v_L = 2v_d - V_C \quad (3.37)$$

$$V_{(+)} = +\frac{V_0}{2} \quad (3.38)$$

$$V_N = 0V \quad (3.39)$$

$$V_{(-)} = -\frac{V_0}{2} \quad (3.40)$$

$$V_0 = 2(V_C - v_d) \quad (3.41)$$

b) Full shoot through state

The simplified representation of three-level Z-Source inverter during a NST state is illustrated in Figure 3.19. The FST state is initiated by turning ‘on’ all the switches in a single leg. During this state, the diodes D_1 and D_2 are reverse biased. Therefore, the corresponding expressions can be given by:

Figure 3.19 Three-level Z-Source NPC during FST state (D_1 and D_2 are blocking)

$$v_L = V_C \quad (3.42)$$

$$V_{(+)} = V_N = V_{(-)} = 0V \quad (3.43)$$

c) Upper shoot through state

The three-level NPC inverters possess additional two ST states because of the presence of neutral point. In FST state, both the diodes are reverse biased. However, in additional states, one of the diodes is blocking while

another is conducting. One of the two additional state is the UST state which is achieved by shorting the upper three switches of the inverter. In this state, the diode D_2 is reverse biased and the diode D_1 is conducting. The equivalent circuit of the state is shown in Figure 3.20.

Figure 3.20 Three-level Z-Source NPC during UST state (D_1 conducting and D_2 blocking)

During this state, the mathematical expressions are given by:

$$v_{L1} = V_{d1} \quad (3.44)$$

$$V_{(+)} = 0, V_N = 0 \quad (3.45)$$

$$V_{(-)} = V_{d1} - V_{C1} \quad (3.46)$$

d) Lower shoot through state

Another additional state is the LST state, wherein the lower three switches are shorted, to provide the voltage boost. In this state the diode D_1 is reverse biased while diode D_2 is conducting, which can be deduced from the equivalent circuit depicted in Figure 3.21.

Figure 3.21 Three-level Z-Source NPC during LST (D_2 conducting and D_1 blocking)

During this state, the voltage expressions are:

$$v_{L2} = V_{d2} \quad (3.47)$$

$$V_{(+)} = -V_{d2} + V_{C2} \quad (3.48)$$

$$V_{(-)} = 0, \quad V_N = 0 \quad (3.48)$$

If the UST, LST and NST are chosen for the inverter operation, the averaged inductor voltage for a period of T is given by:

$$V_c = \frac{2v_d * (1 - T_0/2T)}{1 - T_0/T} \quad (3.49)$$

where,

T_0 – common shoot through period for both UST and LST states.

Using Equation (3.49), the peak dc-link voltage is given by:

$$\hat{v}_0 = V_c - v_L = \frac{2v_d}{1 - T_0/T} \quad (3.50)$$

Therefore, the peak ac output voltage is derived as:

$$\widehat{v}_{ac} = M \cdot \frac{\widehat{v}_0}{2} \quad (3.51)$$

3.4.2. Split dc-source Single Z-Source Network NPC Inverter

The split dc-source SZSN-NPC inverter is similar to the split-capacitor bank except for the neutral point that is formed between the two input dc sources (V_{iU} and V_{iL}) as depicted in Figure 3.17. The mode of operation includes NST, FST, UST and LST states. To achieve voltage boosting, the inverter can be operated in two combinations: 1) NST state with FST state 2) NST state with UST and LST states.

a) Non-Shoot Through state

The simplified representation of three-level Z-Source inverter during a NST state is illustrated in Figure 3.22.

Figure 3.22 Three-level Z-Source NPC during NST state (D_1 and D_2 are conducting)

Considering $V_{iU} = V_{iL} = V_i$ and during NST, the diodes D_1 and D_2 are conducting. Therefore, the voltage expressions for this state are given as:

$$v_L = 2V_i - V_c \quad (3.52)$$

$$V_{(+)} = +\frac{V_0}{2} \quad (3.53)$$

$$V_N = 0V \quad (3.54)$$

$$V_{(-)} = -\frac{V_0}{2} \quad (3.55)$$

$$V_0 = 2(V_c - V_i) \quad (3.56)$$

b) Full Shoot Through state

The simplified representation of three-level Z-Source inverter during a NST state is shown in Figure 3.23. The FST state is initiated by turning ‘on’ all the switches in a single leg. During this state, the diodes D_1 and D_2 are reverse biased. Therefore, the corresponding expressions can be given by:

Figure 3.23 Three-level Z-Source NPC during FST state (D_1 and D_2 are reverse biased)

$$v_L = V_c \quad (3.57)$$

$$V_{(+)} = V_N = V_{(-)} = 0V \quad (3.58)$$

c) Upper Shoot Through state

The three-level NPC inverters possess additional two ST states due to the presence of neutral point. In FST state, both the diodes are reverse biased. However, in additional states, one of the diode is blocking while another is conducting. One of the two additional state is the UST state, which is achieved by shorting the upper

three switches of the inverter. In this state, the diode D_2 is reverse biased and the diode D_1 is conducting. The equivalent circuit of the state is portrayed in Figure 3.24.

Figure 3.24 Three-level Z-Source NPC during UST state (D_1 forward and D_2 reverse biased)

During this state the mathematical expressions are given by:

$$v_{L1} = V_{iU} \quad (3.59)$$

$$V_{(+)} = 0, \quad V_N = 0 \quad (3.60)$$

$$V_{(-)} = V_{iU} - V_{C1} \quad (3.61)$$

d) Lower Shoot Through state

One of the other additional ST state is the LST state, in which the lower three switches are shorted, to provide the voltage boost. In this state the diode D_1 is reverse biased and diode D_2 is conducting, which can be determined from the equivalent circuit represented by Figure 3.25.

Figure 3.25 Three-level Z-Source NPC during LST (D_2 forward and D_1 reverse biased)

During this state, the voltage expressions are:

$$v_{L2} = V_{iL} \quad (3.62)$$

$$V_{(+)} = -V_{iL} + V_{C2} \quad (3.63)$$

$$V_{(-)} = 0, \quad V_N = 0 \quad (3.64)$$

If the FST and NST are chosen for the inverter operation, then averaging the inductor voltage for a period of T yields:

$$V_C = \frac{2V_i \cdot (1 - T_0/T)}{1 - 2T_0/T} \quad (3.65)$$

where,

T_0 – shoot through period for the FST state.

From Equation (3.65), the peak dc-link voltage can be calculated as:

$$\hat{v}_0 = 2V_C - 2V_i = \frac{2V_i}{1 - 2T_0/T} \quad (3.66)$$

Therefore, the output peak phase voltage is derived as:

$$\widehat{v}_{ac} = M \cdot \frac{\widehat{v}_0}{2} = M \cdot \frac{V_i}{1-2T_0/T} = M \cdot B \cdot V_i \quad (3.67)$$

where,

M – modulation index

$B = 1/(1 - 2T_0/T)$ – boost factor. B should be greater than one for boost operation.

3.4.3. Dual Z-Source Network NPC Inverter

The most common topology for designing a Z-Source NPC is by connecting two Z-Source networks instead of the capacitor banks in traditional NPC inverters. Figure 3.26 shows a Dual Z-Source Network Neutral Point Clamped inverter (DZSN-NPC) with two Z-Source networks (upper and lower) connected to a dc-link. The two Z-Source networks are supplied by two isolated dc sources. The negative dc terminal of the upper Z-Source network is connected to the positive dc terminal of the lower Z-Source network. The inverter dc-link is attached to the middle point of the upper and lower networks, represented by point N in Figure 3.26, thus forming a neutral point with a potential of 0V. The impedance network employed results in voltage buck-boost and exhibits greater reliability. This is attributed to the insertion of ST state and would not cause any semiconductor to fail. In addition, as the ST allows the inverter to be operated without any dead-time protection, the quality of the output is better. The only limitation of the DZSN-NPC inverter is its cost, as it requires two passive Z-Source networks.

Figure 3.26 Topology of Three-level Z-Source Dual Z-Source NPC inverter

With the neutral point formed between the upper and lower Z-Source networks, the voltage boosting of both the networks needs to be simultaneous. For the upper Z-Source network the dc-link voltage boosting can be achieved by turning ‘on’ the upper three switches of any phase leg (e.g. S_{a1} , S_{a2} and $S_{a1'}$) with the diodes D_1 , D_a being forward biased and D_2 reverse biased. Similarly the voltage boosting for the lower Z-Source network is stimulated by turning ‘on’ the lower three switches of any phase leg (e.g. S_{a2} , $S_{a1'}$ and $S_{a2'}$) with diodes D_2 , D_a being in conducting mode and D_1 in blocking mode. While performing the dc-link voltage boosting, the important factor to be considered is that both the Z-Source networks should not be boosted simultaneously. When boosted simultaneously, it short circuits the full dc-link which can degrade the performance of the harmonics. Therefore, the boosting must be performed at equal time intervals so that the dc-link voltage unbalancing can also be avoided. Therefore, while implementing the modulation method for dual Z-Source network, FST state (achieved by turning ‘on’ all switches in a single-phase leg) should be avoided. The later section deals with the different modulation methods for the Z-Source NPC inverters.

3.5. Modulation methods for Three-Level Z-Source Neutral point clamped inverter

Among the three topologies, the single Z-Source network with split-dc source NPC inverter and dual Z-Source NPC inverter are highly preferred. Voltage boosting in the Z-Source NPC inverter is achieved by utilizing the zero states found in the traditional inverter as ST states, similar to the two-level inverter topology. These ST states should be carefully inserted using proper modulation method. In traditional two-level inverters, full dc-link is shorted to provide voltage boosting. As discussed in the previous section, for three-level NPC inverters, the voltage boosting is achieved by changing the zero states into FST state (all switches are turned ‘on’), UST state (top three switches in any leg is turned ‘on’) and LST states (bottom three switches in any leg is turned ‘on’). The different operating states of the inverter and the corresponding switches and diodes that are turned ‘on’ during these operating states for a single phase (phase a) are listed in Table 3.2.

For traditional NPC inverters, the most common pulse width modulation methods were reviewed in Chapter 2. The two most common carrier based modulation methods are Phase Opposition Disposition Level Shifted Pulse Width Modulation (POD-LSPWM) and In-Phase Disposition Level Shifted Pulse Width Modulation (IPD-LSPWM). These carrier comparison methods are further used for the three-level Z-Source inverter with the ST state inserted by performing additional comparison. Nonetheless, sufficient care should be taken to ensure that

normalized volt-sec average is maintained at all times, no matter if FST state or combination of UST and LST state are used for dc-link voltage boosting.

Table 3.2 Switching states of a three-level ZSI

Operating States	Turned 'on' Switches	Turned 'on' diodes	Output Voltage
Non-shoot through (NST)	S_{a1}, S_{a2}	D_1, D_2	$+v_i/2$
Non-shoot through (NST)	$S_{a2}, S_{a1'}$	$D_1, D_2 (D_a \text{ or } D_{a'})$	0
Non-shoot through (NST)	$S_{a1'}, S_{a2'}$	D_1, D_2	$-v_i/2$
Full shoot through (FST)	$S_{a1}, S_{a2}, S_{a1'}, S_{a2'}$	---	0
Full shoot through (FST)	$S_{a1}, S_{a2}, S_{a1'}, S_{c2}, S_{c1'}, S_{c2'}$	$D_{a'}, D_c$	0
Upper shoot through (UST)	$S_{a1}, S_{a2}, S_{a1'}$	$D_{a'}, D_1$	---
Lower shoot through (LST)	$S_{a2}, S_{a1'}, S_{a2'}$	D_a, D_2	---

3.5.1. Phase Opposition Disposition Modulation method

In this method the three-phase sinusoidal reference waves (V_a^* , V_b^* and V_c^*) are compared with two triangular carrier waves ($V_{\text{carr}+}$ and $V_{\text{carr}-}$), which are phase shifted by 180° as depicted in Figure 3.27. This comparison produces two individual gate signals for the upper two switches in each phase and their corresponding NOT signals is given to the lower two switches. This modulation method used for the traditional three-level inverters can be extended to the three-level Z-Source because the rear end of both the configuration is a NPC circuit. However if no modification is made to the traditional switching sequence, this modulation method leads to voltage buck operation when used with Z-Source inverter.

Figure 3.27 POD-LSPWM switching sequence for traditional NPC

So in order to boost the voltage using Z-Source inverter, insertion of ST states has to be carried out without causing any modification to the normalized volt-sec average appearing across the load. Therefore, two additional signals: UST line and LST line as represented in Figure 3.28 is utilized. The UST line is compared to one of the triangular carriers (V_{carr+}) and the LST line is compared to the other triangular carrier (V_{carr-}) to determine the insertions of ST states. From Figure 3.28 it can be deduced that all switches are turned 'on' during the ST state leading to a FST state in place of a combination of UST and LST states. This is attributable to the fact that the ST due to the two ST lines occurs at the same period. From Table 3.2 it can be noted that the FST state are inserted either by turning 'on' all the switches in a single phase leg, or by turning 'on' a combination of switches from two phase legs.

Figure 3.28 POD-LSPWM switching sequence for three-level Z-Source NPC

3.5.2. In-Phase Disposition Modulation method:

Similar to POD modulation method, another method was developed based on carrier comparison. The In-phase Disposition Modulation method is known to produce less harmonic content. In this method, two triangular waves that are in phase with each other are compared with three reference sinusoidal waves to produce the switching sequence to the inverter. From Figure 3.29, it can be inferred that at no point of time all switches in a single phase leg are turned 'on'. Therefore, FST state is not available for maintaining the normalized volt-sec average across the externally connected load. Therefore, in order to use the In-phase Disposition Modulation method for Z-Source inverter, the only choice left to insert the ST state by the combination of the UST and LST states as shown in Table 3.2.

Figure 3.29 IPD-LSPWM switching sequence for three-level traditional NPC

Incorporating all the above said reasons, a modified switching sequence is developed for using with three-level Z-Source NPC. The modified method consists of two additional ST lines similar to that of the Phase Opposition Disposition method, which is compared with both the carrier waves to produce the ST state. As shown in Figure 3.30, the UST line is compared with the carrier signal (V_{carr}^+) and the inverter enters into UST state; the LST line is compared with the carrier signal (V_{carr}^-) and the inverter operates in LST state. During these switching states, the control signal for a single phase leg is 1110 for UST and 0111 for LST state. Care should be taken to ensure a balanced insertion, which is required for undistorted voltage boosting.

Figure 3.30 IPD-LSPWM switching sequence for three-level Z-Source NPC

3.6. Summary

This chapter commences with the explanation and the operating modes of a two-level Z-Source inverter. The overviews of the different ST control schemes for Z-Source inverter that are implemented in this thesis are explained. A comparison table is presented on parameters including, ST duty ratio, modulation index, boost factor, voltage gain and voltage stress, etc. These factors have to be considered when choosing a particular method of PWM technique for an application. Due to the wide operating region, the MBC method is used in this research for a two-level operation of ZSI. The key findings of MBC modulated two-level ZSI, when compared with boost converter, are presented in Chapter 6.

Then the chapter discusses the topologies of three-level Z-Source NPC. The topologies are distinguished by the method used for connecting the neutral point. In the first topology a split capacitor bank, in the second topology

a split dc source and in the third topology two individual Z-Source networks are used. Among the three topologies, the latter two are the most common topologies for the three-level Z-Source NPC. The operation of these individual topologies during the ST and NST states are explained. Furthermore, this section includes the modulation strategies for careful insertion of the FST or UST and LST to the inverter circuitry. Two carrier based modulation methods, phase opposition disposition modulation, and in-phase disposition modulation, are used to achieve voltage boosting capability of the inverter by using the minimum number of device commutations per half-switching cycle. From the analysis, it is deduced that NPC has three ST states when compared to a single ST state in two-level Z-Source. With this feature, different combinations of ST and NST states can be achieved in three-level Z-Source NPC. Compared to other modulation methods for ZSI, MCBC maintains a constant ST duty ratio to achieve maximum voltage gain. Therefore, the MCBC method explained for two-level inverter is modified to be integrated with the carrier based disposition modulation methods, thereby resulting in insertion of ST states and achieving voltage boosting in three-level Z-Source NPC.

Chapter 4 Dual Z-Source Network with Proposed Modulation Method

4.1. Dual Z-Source Network Neutral Point Clamped Inverter

Subsequent to the discussion on the topologies and modulation methods for three-level Z-Source Neutral Point Clamped (NPC) inverter in Chapter 3, this chapter presents a thorough integration of the proposed modulation method for Dual Z-Source Network Neutral Point Clamped (DZSN-NPC). The highly preferred DZSN-NPC inverter uses two isolated dc sources integrated to two different Z-Source networks to power the inverter. The topology is presented in Figure 4.1 for reference. With many modulation methods previously proposed, the aim of this research is to introduce a new modulation method that uses carrier comparison technique. However, in this proposed method, a single carrier is used instead of conventional two carriers. An important factor when designing this modulation method is to avoid the FST state caused by shorting of all switches in a single leg. As mentioned earlier, this FST state needs to be avoided to eliminate the volt-sec error. Therefore, the proposed method uses the UST and LST states to provide dc-link voltage boosting.

Figure 4.1 Dual Z-Source network NPC with two individual DC sources

4.2. Reference Disposition Level Shifted Pulse Width Modulation

The new modulation method uses two reference signals and one carrier signal, in contrary with the conventional carrier based techniques. The two reference signals are level shifted with respect to each other, which when compared to the single carrier signal provides switching sequence to the inverter. Figure 4.2 illustrates the Reference Disposition Level Shifted Pulse Width Modulation (RD-LSPWM) method to produce PWM switching without ST. As exemplified by Figure 4.2, the two reference waves are compared with the triangular carrier wave to provide signals to the switches. Equations (4.1) and (4.2) expresses the reference waves V_{a1} and V_{a2} respectively, where $\theta = \omega t$ and M is the modulation ratio.

Figure 4.2 Proposed RD-LSPWM modulation method without ST signals

$$\left. \begin{aligned} V_{a1} &= \sin(\theta) \cdot M \\ V_{b1} &= \sin\left(\theta - \frac{2}{3}\pi\right) \cdot M \\ V_{c1} &= \sin\left(\theta - \frac{4}{3}\pi\right) \cdot M \end{aligned} \right\} \quad (4.1)$$

$$\left. \begin{aligned} V_{a2} &= 1 + [\sin(\theta) \cdot M] \\ V_{b2} &= 1 + [\sin\left(\theta - \frac{2}{3}\pi\right) \cdot M] \\ V_{c2} &= 1 + [\sin\left(\theta - \frac{4}{3}\pi\right) \cdot M] \end{aligned} \right\} \quad (4.2)$$

To achieve insertion of ST for the Z-Source inverter, traditional PWM strategies should be modified. Several modified PWM methods for Z-Source inverter based on traditional control methods were presented in Chapter 3. A simple boost uses two lines to control the ST states. In maximum boost, ST state happens when the carrier is greater than the reference waves. However, drawbacks like low frequency ripples, voltage stress on switches and operating range of these techniques resulted in an improved MCBC method, where two modified curves greater than or equal to the amplitude of the reference waves is compared with the triangular wave to control the ST. In this method by maintaining the ST duty ratio constant, low frequency current ripple can be eliminated thereby reducing the volume and cost of the network. Furthermore, to reduce stress across the semiconductor switches, a greater voltage boost is required for any modulation index. In addition to constant duty ratio and voltage stress, neutral voltage balancing needs to be considered. Considering these requirements, Reference Disposition Level Shifted PWM (RD-LSPWM) is implemented to achieve maximum voltage gain using MCBC method as illustrated in Figure 4.3.

The sketch map of RD-LSPWM depicted in Figure 4.3, comprise of eight modulation signals: two sets of three reference signals V_{a1} , V_{b1} , V_{c1} & V_{a2} , V_{b2} , V_{c2} and two ST signals V_u and V_l . The first set of reference signals (V_{a1} , V_{b1} , V_{c1}) corresponds to the switches S_{x1} and $S_{x1'}$, where $x = a, b, c$ and the second set of reference signals (V_{a2} , V_{b2} , V_{c2}) corresponds to the switches S_{x2} and $S_{x2'}$, where $x = a, b, c$. The circuit enters into UST state when the upper modified signal V_u (which is equal to or greater than the peak value of the first set of reference signals) is lower than the carrier signal. Similarly, the circuit enters into LST state when the lower modified signal V_l (which is equal to the lower peak value of the second set of reference signals) is greater than the carrier signal. As discussed earlier, during the NST states, switching follows a pattern identical to that of the traditional carrier based PWM, with the exception that the two reference signals and the carrier signal are compared.

Figure 4.3 Proposed RD-LSPWM with ST signals

The UST and LST signals are periodical and there are two half periods $[0, \pi/3]$ and $[\pi/3, 2\pi/3]$ in a single switching cycle. During the first half period of the switching cycle, the modified curves are given by:

UST curve:

$$V_u = M \left(\sqrt{3} + \sin \left(\theta - \frac{2}{3}\pi \right) \right) \text{ where } \theta \in [0, \pi/3] \quad (4.3)$$

LST curve:

$$V_l = M \left(\left(\frac{1}{M} \right) + \sin \left(\theta - \frac{2}{3}\pi \right) \right) \text{ where } \theta \in [0, \pi/3] \quad (4.4)$$

During the second half period of the switching cycle, the modified signals are given as:

UST curve:

$$V_u = M (\sin(\theta)) \text{ where } \theta \in [\pi/3, 2\pi/3] \quad (4.5)$$

LST curve:

$$V_l = M \left(\left(\frac{1}{M} \right) + \sin(\theta) - \sqrt{3} \right) \text{ where } \theta \in \left[\frac{\pi}{3}, \frac{2\pi}{3} \right] \quad (4.6)$$

The ST duty ratio for any modulation index is the distance between the upper and lower envelope curves. Equations (4.3) – (4.5) indicate that this distance is always constant. This implies that ST duty ratio (D_o) is constant. For the single Z-Source inverter, the boost factor can be determined from D_o and is given by [123]:

$$B = \frac{1}{1-2D_o} \text{ where } D_o = \frac{T_o}{T} \quad (4.7)$$

Now, the DZSN-NPC which is supplied through two individual dc sources, includes two Z-Source networks between the source and the NPC inverter circuit. Therefore, two boost factors for the DZSN-NPC are defined by the following expressions:

$$B_{up} = \frac{1}{1 - \frac{2(T_{ou})}{T}} \quad (4.8)$$

$$B_{low} = \frac{1}{1 - \frac{2(T_{oL})}{T}} \quad (4.9)$$

where, B_{up} and B_{low} are the boost factors of the upper and lower Z-Source networks respectively and T_{ou}/T , T_{oL}/T defines the ratio of ST duration for the upper network and the lower network, respectively. From Equations (4.8) and (4.9), the upper and lower dc-link voltages are given by Equations (4.10) and (4.11), respectively:

$$V_{ou} = V_{iu} \cdot B_{up} = \frac{V_{iu}}{1 - \frac{2(T_{ou})}{T}} \quad (4.10)$$

$$V_{oL} = V_{iL} \cdot B_{low} = \frac{V_{iL}}{1 - \frac{2(T_{oL})}{T}} \quad (4.11)$$

At certain instances wherein the voltage levels are different, the neutral point balancing will be affected. Hence to achieve balancing, some modifications to the ST duty duration for both the upper and lower Z-Source networks is required and shown in Equations (4.12) and (4.13):

$$V_{oU} = V_{iU} \cdot B_{up} = \frac{V_{iU}}{1 - \frac{2(T_{oU} + T_T)}{T}} \quad (4.12)$$

$$V_{oL} = V_{iL} \cdot B_{low} = \frac{V_{iL}}{1 - \frac{2(T_{oL} + T_T)}{T}} \quad (4.13)$$

where, V_{iU} and V_{iL} are the individual dc sources connected to the upper and lower Z-Source networks. V_{oU} and V_{oL} are the corresponding output dc-link voltages and T_T is the common ST duration for both the upper and lower Z-Source networks. Ideally, both the dc-link sources are maintained at the same voltage levels. The boost factors determine the output voltage of the dc-links, which should be of identical magnitude to achieve low output THD. Thereby, the peak ac voltage for dual network can be expressed by Equation (4.14) in which V_i represents the value of the dc sources:

$$\widehat{v_{ac}} = M \cdot B \cdot V_i \quad (4.14)$$

4.3. Switching States of DZSN-NPC using RD-LSPWM

From the topology portrayed by Figure 4.1, the two Z-Source networks draw power from individual dc power sources. The negative dc line of the upper Z-Source network is connected to the positive dc line of the lower Z-Source network. The midpoint of these lines is connected to the dc-link of the inverter, thus forming a neutral point with a potential of 0V. Furthermore, Z-Source inverter has several unique ST states in addition to the active and zero states of the conventional inverters. As the Z-Source NPC inverter boosts the dc-link voltage during these ST states, the ST interval needs to be generated carefully to equally distribute the boosted inductive energy into the Z-Source network. Table 4.1 summarizes the switching states of the inverter during the two operating modes: ST and NST states.

From Table 4.1, it can be surmised that Z-Source NPC inverter possesses three ST states, namely FST, UST and LST. FST occurs when all the switches of the single leg or any two legs or all three legs are shorted. UST represents that the upper three switches (S_{x1} , S_{x2} , $S_{x1'}$, where $x = a, b, c$) in a leg are turned 'on' with D_a forward biased and similarly LST implies that the bottom three switches (S_{x2} , $S_{x1'}$, $S_{x2'}$, where $x = a, b, c$) in a leg are turned 'on' with D_a forward biased.

Table 4.1 Switching States of the DZSN-NPC inverter, illustrated in Figure 4.1 (ST $\equiv$ Shoot Through)

Phase	Switching States	Switches (ON)	Diodes (ON)	Output
a	Non-ST	S_{a1}, S_{a2}	D_1, D_2	$+V_i$
a	Non-ST	$S_{a2}, S_{a1'}$	$D_1, D_2, D_a(\text{or } D_{a'})$	0
a	Non-ST	$S_{a1'}, S_{a2'}$	D_1, D_2	$-V_i$
a	Upper-ST	$S_{a1}, S_{a2}, S_{a1'}$	-	0
a	Lower-ST	$S_{a2}, S_{a1'}, S_{a2'}$	-	0
a	Full-ST	$S_{a1}, S_{a2}, S_{a1'}, S_{a2'}$	-	0
b	Non-ST	S_{b1}, S_{b2}	D_1, D_2	$+V_i$
b	Non-ST	$S_{b2}, S_{b1'}$	$D_1, D_2, D_b(\text{or } D_{b'})$	0
b	Non-ST	$S_{b1'}, S_{b2'}$	D_1, D_2	$-V_i$
b	Upper-ST	$S_{b1}, S_{b2}, S_{b1'}$	-	0
b	Lower-ST	$S_{b2}, S_{b1'}, S_{b2'}$	-	0
b	Full-ST	$S_{b1}, S_{b2}, S_{b1'}, S_{b2'}$	-	0
c	Non-ST	S_{c1}, S_{c2}	D_1, D_2	$+V_i$
c	Non-ST	$S_{c2}, S_{c1'}$	$D_1, D_2, D_c(\text{or } D_{c'})$	0
c	Non-ST	$S_{c1'}, S_{c2'}$	D_1, D_2	$-V_i$
c	Upper-ST	$S_{c1}, S_{c2}, S_{c1'}$	-	0
c	Lower-ST	$S_{c2}, S_{c1'}, S_{c2'}$	-	0
c	Full-ST	$S_{c1}, S_{c2}, S_{c1'}, S_{c2'}$	-	0
x,y = combination of any two legs	Full-ST	$S_{x1}, S_{x2}, S_{x1'}, S_{y2}, S_{y1'}, S_{y2'}$	D_{x2}, D_{y1}	0
A,B,C	Full-ST	$S_{a1}, S_{a2}, S_{a1'}, S_{a2'}, S_{b1}, S_{b2}, S_{b1'}, S_{b2'}, S_{c1}, S_{c2}, S_{c1'}, S_{c2'}$	-	-

During these ST states, the output voltage of the inverter is boosted. However, care should be taken that the boosting time period of the upper and lower networks should be identical. This ensures that shorting of full dc-link will be avoided. This also ensures that the voltage boosting is balanced. As discussed earlier, by turning ‘on’ all switches in three legs, the circuit enters into FST mode, which also aids in voltage boosting. Nevertheless, turning ‘on’ all inverter switches leads to ‘volt-sec error’ [123] in the inverter output. Therefore, this research uses UST and LST states to achieve voltage boosting. The diodes (D_1 and D_2) in Figure 4.1 connected to the Z-Source networks ensures the unidirectional operation. If the diodes were replaced with switches, then the appropriate switches must be turned ‘off’ to disconnect the source during voltage boosting. In the chosen experimental setup, the diodes will reverse bias depending on the shorted Z-Source network.

During the ST states the inverter terminals are shorted changing the output voltage of the inverter to 0V. The inductive energy stored during ST is delivered to the ac load during any of the NST states mentioned in Table 4.1, where the switches are assembled in two complementary pairs for each phase. From the table, the output voltages of the inverter during the NST states are determined to be $+V_i$, 0V, $-V_i$.

4.4. Key Results

4.4.1. Identical dc sources

For evaluating the performance of the RD-LSPWM method for the Dual Z-Source network, simulations were performed using PSIM with Matlab/Simulink coupler. The individual dc voltage sources V_{iU} and V_{iL} supplying the upper and lower Z-Source networks are maintained at 100 V, based on the analysis from prior research studies [25], [28]. Similarly, the Z-Source network parameters for both networks are $L = 2$ mH and $mH1000 \mu F$ with a switching frequency of 10 kHz. The passive components of the impedance network are determined based on [121]. A three-phase RL circuit serves as the load of the Z-Source inverter.

In this section, the theoretical calculations of the dual Z-Source network implementing the reference disposition method are compared with the simulation outputs and the results are discussed. For the evaluation, the modulation index was set to $M = 0.85$, with which the boost factor of the Z-Source in the maximum constant boost control method is calculated using the equation $B = 1/(\sqrt{3}M - 1)$. The value of boost factor was determined as 2.1. Thereby the ST duty cycle is set at $T_0/T = 0.26$. The output of the upper dc voltage is induced by the Z-Source capacitors in the upper network. In reference to the circuit configuration given in Figure 4.1, key waveforms for the configuration are presented from Figure 4.4. Figures 4.4 and 4.5 depicts the voltage

across the upper capacitor and upper dc-link respectively. From Figure 4.5, the simulated average value of the upper dc-link voltage is computed to be 200 V. The computed value is similar to the theoretically calculated value of the upper dc-link, and shown in Equation (4.15):

$$V_{oU} = V_{iU} \cdot B_{up} = 100 \cdot 2.1 = 210 \text{ V} \quad (4.15)$$

Figure 4.4 Capacitor voltage of the upper Z-Source network with $M=0.85$ and $B=2.1$ (refer to Figure 4.1)

Figure 4.5 Voltage across the upper dc link with $M=0.85$ and $B=2.1$ (refer to Figure 4.1)

Similarly, for the lower Z-Source network, which is fed by 100 V dc source, capacitor voltage and the dc-link voltage, are illustrated in Figures 4.6 and 4.7. The average value of the lower dc-link voltage through simulation

in Figure 4.7 is computed as 202 V, which is similar when compared to the expected theoretical value of 210 V calculated using Equation (4.11):

$$V_{oL} = V_{iL} \cdot B_{low} = 100 \cdot 2.1 = 210 \text{ V} \quad (4.16)$$

Figure 4.6 Capacitor voltage of the lower Z-Source network with $M=0.85$ and $B=2.1$ (refer to Figure 4.1)

Figure 4.7 Voltage across the lower dc link with $M=0.85$ and $B=2.1$ (refer to Figure 4.1)

The waveforms shown in Figures 4.5 and 4.7 confirms the upper and lower dc-link voltages are almost identical. Furthermore, the capacitor voltages are balanced by the proper insertion of the ST states by this method,

therefore, neutral point potential is balanced. Figure 4.8 illustrates the output phase voltage of the inverter. The total harmonic distortion of the output phase voltage is depicted in Figure 4.9.

Figure 4.8 Output phase voltage (V_{ph}) of the inverter (refer to Figure 4.1)

Figure 4.9 THD of Output Phase voltage of the inverter (refer to Figure 4.1)

Figures 4.10 and 4.11 provide the output line-to-line voltage and its harmonic distortion waveforms, respectively. The total harmonic distortion of the output line voltage incorporating reference disposition is

47.69%. The output line currents of the inverter, whose ripple can be eliminated using a proper filter, for the reference disposition method is illustrated in Figure 4.12.

Figure 4.10 Output line-to-line voltage (V_{ab}) of the inverter (refer to Figure 4.1)

Figure 4.11 THD of output line-to-line voltage of the inverter (refer to Figure 4.1)

Figure 4.12 Output line currents of the inverter (refer to Figure 4.1)

4.4.2. Non-identical dc sources

Generally, the upper and lower Z-Source networks are supplied by identical dc sources. However, when applied for a DER system, the dc sources would not be identical. This section analyses the performance of the proposed method when the dc sources are not identical. The major problem that occurs when the supplies are unbalanced is the neutral point balancing problem. To achieve balancing during that non-identical condition, the adjustments in the ST duration of both the upper and lower Z-Source networks are incorporated and explained by Equations (4.12) and (4.13), respectively. The boost factor also changes correspondingly as it is a function of ST period, observed from Equation (4.7). The key results for the system under non-identical dc sources is presented in this section. The upper (V_{cu}) and lower (V_{cl}) capacitor voltages when supplied by different voltage dc sources are shown in Figure 4.13. From this figure, it is inferred that the upper capacitor voltage is significantly greater than the lower capacitor voltage. For this output, no modification in the ST duration is introduced. With the modification, the output of the capacitor voltages is shown in Figure 4.14. From the figure it can be verified that both the capacitors are balanced, thereby providing neutral point balancing.

Figure 4.13 Upper and Lower capacitor output voltages supplied by non-identical dc sources (without modification in ST duration) (refer to Figure 4.1)

Figure 4.14 Upper and Lower capacitor output voltages supplied by non-identical dc sources (with modification in ST duration) (refer to Figure 4.1)

With the capacitor voltages of the upper and lower Z-Source network being balanced, the upper and lower dc-link voltages are portrayed in Figures 4.15 and 4.16, respectively. It is observed that the magnitudes of the upper and the lower dc-link voltage are identical. From the simulation results the average value of upper and lower dc-link voltages are computed as 191 V and 189 V, respectively. Therefore, the neutral point potential balance is achieved by this proposed modulation method.

Figure 4.15 Upper dc link voltage supplied by non-identical dc sources (refer to Figure 4.1)

Figure 4.16 Lower dc link voltage supplied by non-identical dc sources (refer to Figure 4.1)

In this method, the two individual dc sources are non-identical. However from Figure 4.14, it is determined that the capacitors in both the networks are balanced. Therefore, the output phase voltage of the inverter is non-distorted as observed from Figure 4.17.

The output voltage of the non-identical dc sources is obtained and plotted in Figure 4.17. The peak value of the output voltage for the non-identical dc source was determined as slightly lower than the case wherein identical dc sources were considered. The adjustment in the ST duration impacts the boost factor. This is the primary reason for the variation of magnitudes between the identical and non-identical conditions. The total harmonic distortion of the output phase voltage is illustrated in Figure 4.18.

Figure 4.17 Output phase voltage (V_{ph}) of the inverter during non-identical condition (refer to Figure 4.1)

Figure 4.18 FFT of the output phase voltage during non-identical condition (refer to Figure 4.1)

Figures 4.19 and 4.20 provides the output line-to-line voltage and its harmonic distortion waveforms, respectively. The total harmonic distortion of the output line voltage incorporating reference disposition is 47.32%. The harmonic analysis for both the cases are almost identical. Figure 4.21 depicts the three-phase

output currents of the Z-Source inverter. There are small spikes that are visible but these are absent during the identical condition. These can be eliminated by either modifying the modulation index or by using a proper filter.

Figure 4.19 Output line-to-line voltage (V_{line}) of the inverter during non-identical condition (refer to Figure 4.1)

Figure 4.20 FFT of output line-to-line voltage during non-identical condition (refer to Figure 4.1)

Figure 4.21 Three-phase output line currents during non-identical condition (refer to Figure 4.1)

4.5. Summary

This chapter discusses the newly proposed modulation method for the Z-Source NPC inverters. The proposed modulation method utilises two sets of reference signals, two ST signals and one carrier signal to provide switching sequences to the inverter. While inserting the ST states, steps are taken to avoid drawbacks like volt-sec error. The switching devices at various switching states are tabulated in Table 4.1. As the dual Z-Source network is supplied by two individual sources, two different conditions were analysed with the proposed modulation methods.

In general, two dc sources with same voltage rating are connected to perform with dual Z-Source inverter. This yields the two conditions of identical and non-identical dc sources. The initial part of the results (under the identical dc sources) describe the performance evaluation of the proposed reference disposition level shifted PWM. The performance is verified for an ideal circuit. The verification process requires that the upper and lower capacitor voltages are balanced. This balance is confirmed by carrying out simulations in Matlab/Simulink and PSIM environment. The results are illustrated in Figures 4.4 and 4.6. As the capacitors are determined to be balanced, neutral point balancing is achieved. The results obtained from simulation agrees with the theoretical results, validating the proposed modulation method for identical dc voltage sources.

The need for examining the performance of non-identical dc sources for this modulation method given that most natural scenarios do not incorporate identical dc sources. Therefore, for non-identical conditions, achieving the neutral point balance is an important progression in the analysis of the modulation method. Modification of the ST duty ratio of the upper and lower Z-Source inverters is necessary to achieve this. The results for the non-

identical dc sources are presented in the latter part of the results section. In both cases, the implemented modulation scheme achieves maximum voltage boost, low semiconductor stress, low THD and better output waveform quality with easier implementation. Furthermore, the proposed modulation method can achieve neutral point balancing for identical and non-identical dc sources.

Chapter 5 Reference Disposition Level Shifted Pulse Width Modulation for non-ideal Dual Z-Source Network NPC

5.1. Non-ideal Dual Z-Source network NPC

From the review on multilevel inverters in Chapter 3, it can be concluded that several stages of dc voltages may be used to deliver a desired output voltage. Implementing multiple dc voltages helps to achieve a near sinusoidal output voltage with the multi-level inverter while adopting fundamental frequency switching. One of the most common multilevel topology that is widely used is the diode clamped inverter, mostly known as Neutral Point Clamped (NPC) inverter. In Chapter 4, the NPC inverter was used along with a Z-Source inverter. To form the neutral point for the inverter, two different Z-Source networks were implemented in the circuit, thereby forming the ‘Dual’ Z-Source Network Neutral Point Clamped (DZSN-NPC). A new carrier based modulation method has been proposed for the aforementioned topology. Notably, the inverter was operated under ideal condition in DZSN-NPC i.e. no losses in the circuit were considered. In practice, there would occur a voltage drop across the components. Due to this phenomenon, it is vital to examine the performance of the proposed modulation method for DZSN-NPC in real scenarios. Therefore, this chapter deals with the study of the non-ideal DZSN, where the circuit resistance and their respective voltage drop are considered. The real time voltage drops are introduced in the simulation study by connecting a resistance to the existing topology (shown in Figure 4.1). Figure 5.1 illustrates the circuit that incorporates these modifications. A detailed circuit analysis is presented in the this section. The ST to the inverter is inserted through the new modulation method (RD-LSPWM), described in Chapter 4.

Figure 5.1 Non-Ideal circuit of DZSN-NPC with two individual dc sources

5.2. Non-ideal DZSN circuit analysis

As two symmetrical single Z-Source networks form DZSN, the circuit analysis is performed for one of the networks. As observed from Figure 5.1, the upper Z-source network possess two capacitors and inductors. By assuming that the inductors and the capacitors have the same value of inductance and capacitance, makes the network symmetrical. In this case, the voltage across both the capacitors and inductors is represented as V_C and v_L respectively and the voltage drop across the resistance as V_R . Therefore, the operation of the inverter for a switching period of T (ST state for a period of T_θ and NST states for a period of T_l) are expressed by the following series of equations.

A symmetrical network is assumed wherein the inductors L_1 and L_2 and the capacitors C_1 and C_2 possess the same inductance and capacitance values, respectively:

$$v_{L1} = v_{L2} = v_L \quad (5.1)$$

$$V_{C1} = V_{C2} = V_C \quad (5.2)$$

For a switching cycle T ,

During ST zero state for a period of T_0 , the voltages are:

$$v_L = V_C - V_R \quad (5.3)$$

$$V_{oU} = 0 \quad (5.4)$$

During one of the eight NST states for a period of T_I , the voltages are:

$$v_L = V_{iU} - V_C - V_R \quad (5.5)$$

$$V_{oU} = V_C - v_L = 2V_C - V_{iU} + V_R \quad (5.6)$$

where,

v_L – voltage across the inductor

V_C – voltage across the capacitor

V_R – voltage drop across the resistance

V_{iU} –upper dc voltage source

V_{oU} –upper dc-link voltage

$$T = T_I + T_0$$

Averaging inductor over a time period T :

$$V_L = \overline{v_L} = \frac{T_0(V_C - V_R) + T_1(V_{iU} - V_C - V_R)}{T} \quad (5.7)$$

Under steady state condition, Equation (6.7) equals to zero. Thereby:

$$V_L = \frac{T_0(V_C - V_R) + T_1(V_{iU} - V_C - V_R)}{T} = 0 \quad (5.8)$$

Further solving yields the following:

$$V_C = \frac{TV_R - T_1V_{iU}}{T_0 - T_1} \quad (5.9)$$

Similarly, the average upper dc-link voltage of the inverter is,

$$V_{oU} = \overline{v_{oU}} = \frac{T_0 \cdot 0 + T_1(2V_C - V_{iU} + V_R)}{T} \quad (5.10)$$

Hence:

$$\overline{v_{oU}} = \frac{T_1}{T} (2V_C - V_{iU} + V_R) \quad (5.11)$$

The peak dc-link voltage is determined as,

$$V_{oU(peak)} = \frac{1}{1 - \frac{2(T_0)}{T}} (V_{iU} - 2V_R) \quad (5.12)$$

where,

T_0 – ST duration.

Equations (5.11) and (5.12) provides the mathematical expression for the average and peak value of the dc-link voltage, which are used to evaluate the performance of the proposed Reference Disposition PWM for DZSN.

5.3. Switching states of the inverter using RD-LSPWM

As observed from Figure 5.1, each of the two Z-Source networks have individual dc power supply. One dc output terminal (negative) of the upper Z-Source network is connected to one dc output terminal (positive) of the lower Z-Source network. The dc-link of the inverter is connected to the mid point of the upper and the lower networks, represented by the point N in Figure 5.1. N is the neutral point with a potential of 0 V. In addition, Z-Source inverter has several unique ST states, in addition to the active and zero states of the conventional inverters. As the Z-Source NPC inverter utilises these ST states to boost the dc bus voltage, the ST interval has to be generated with precision. This ensures that the boosted inductive energy is equally distributed into the Z-Source network. The modulation scheme is explained in detail in the previous chapter. Figure 5.2 shows the control logic of a single phase for DZSN-NPC inverter. One of the regular three-phase reference signals (V_{a1}) and the level shifted reference signal (V_{a2}) are compared with the carrier signals, making the inverter operation similar to the carrier comparison PWM implemented in VSI. Additionally, V_u and V_l determines the UST and LST duty cycles. Moreover, comparisons depicted in Figure 5.2, generates the switching signals to the inverter.

Figure 5.2 ST control logic for phase 'a' using RD-LSPWM

Table 5.1 summarizes the switching states of the inverter during the ST and NST states. From Table 5.1, it can be determined that the Z-Source NPC inverter possess three ST states, namely FST, UST and LST. Even though three ST states are feasible, from Figure 5.2, it is evident that the voltage boosting of the dual Z-Source network is achieved by using the UST and LST states.

Table 5.1 Simplified Switching representation for a non-ideal three-level ZSI ($z = a, b, \text{ or } c$)

Switching States	Switches (ON)	Diodes (ON)	Output
Non-ST	S_{z1}, S_{z2}	D_1, D_2	$+V_i$
Non-ST	$S_{z2}, S_{z1'}$	$D_1, D_2, D_z (\text{or } D_{z'})$	0
Non-ST	$S_{z1'}, S_{z2'}$	D_1, D_2	$-V_i$
Upper-ST	$S_{z1}, S_{z2}, S_{z1'}$	$D_1, D_{z'}$	0
Lower-ST	$S_{z2}, S_{z1'}, S_{z2'}$	D_2, D_z	0
Full-ST (preferred but not included)	$S_{z1}, S_{z2}, S_{z1'}, S_{z2'}$	-	0
Full-ST (not preferred)	$S_{a1}, S_{a2}, S_{a1'}, S_{a2'}, S_{b1}, S_{b2}, S_{b1'}, S_{b2'}, S_{c1}, S_{c2}, S_{c1'}, S_{c2'}$	-	-

5.4. Key Results

Reference Disposition level shifted pulse width modulation method is used for providing the switching signals to the inverter. Similar to ideal network, the performance evaluation of non-ideal dual Z-Source network incorporating the proposed method is performed using PSIM with Matlab/Simulink coupler. The simulation results are discussed in the following part of this section, followed by the experimental verification of the setup in Section 5.4.2

5.4.1. Simulation verification

For evaluating the performance of RD-LSPWM modulation method for the non-ideal Dual Z-Source network, the two individual dc voltage sources V_{iU} and V_{iL} supplying the upper and lower Z-Source networks are maintained at 40 V each. The parameters for both the upper and lower Z-Source networks are $L = 5$ mH and $C = 1000$ μ F with a switching frequency of 1 kHz. Similar to the ideal case, the parameters of the impedance network are determined based on [121]. Due to the limitation in the laboratory equipment, the experiment can be done only at low switching frequency. A three-phase RL circuit serves as the load of the Z-Source inverter.

For the designed impedance values, the modulation index is set to $M = 0.85$ in order to achieve maximum voltage boosting. Setting the M value, the ST duty cycle is calculated to $T_o/T = 0.26$ and the simulated results are discussed subsequently. The output of the upper dc-link voltage is induced by the Z-Source capacitors in the upper network. Figures 5.3 and 5.4 depicts the voltage across the upper capacitor and the upper dc-link voltage, respectively.

From Figure 5.4, the simulated average value of the upper dc-link voltage is determined to be 53.1 V, which is similar to the theoretical value, which is 54. The theoretical value is calculated using the mathematical expression given in Equation (5.11).

Figure 5.3 Capacitor voltage of the upper Z-Source network with $M=0.85$ (refer to Figure 5.1)

Figure 5.4 Voltage across the upper dc link with $M=0.85$ (refer to Figure 5.1)

Similarly, for the lower Z-Source network, which is fed by another 40 V dc source, the capacitor voltage and the dc-link voltage are illustrated in Figures 5.5 and 5.6. The average value of the lower dc-link voltage through the simulation is observed to be 53.2 V as available in Figure 5.6. This is identical to the expected theoretical value of 54 V calculated using Equation (5.11).

Figure 5.5 Capacitor voltage of the lower Z-Source network with $M=0.85$ (refer to Figure 5.1)

Figure 5.6 Voltage across the lower dc link with $M=0.85$ (refer to Figure 5.1)

The waveforms illustrated in Figures 5.4 and 5.6 demonstrates that the upper and lower dc-link voltages are almost the same, balancing the neutral point potential. Under ideal conditions, the circuit resistance is not considered. Then, the boost factor of the Z-Source in the MCBC method is calculated using the equation $B = 1/(\sqrt{3}M - 1)$ and is computed as 2.1. From the simulation results depicted in Figures 5.4 and 5.6, the peak value of the dc-link voltage is 80 V that matches with Equation 5.12. The obtained peak value by incorporating MCBC method in the proposed modulation method proves that the boosting of the dc link voltage matches the ‘boost factor’ value (Equation 5.12) claimed in [44]. Figure 5.7 illustrates the output phase voltage (V_{aN}) of the inverter. From the waveform it is established that the peak value of the voltage is 85 V, and is agreeable with the theoretical calculation of 88 V, calculated using $\widehat{v_{ac}} = M.B.V_i$. The total harmonic distortion of the output phase voltage is depicted in Figure 5.8.

Figure 5.7 Output line to neutral voltage (V_{aN}) of the inverter (refer to Figure 5.1)

Figure 5.8 THD of Output Phase voltage (refer to Figure 5.1)

Figure 5.9 provides the output phase to load neutral voltage. Figures 5.10 and 5.11 show the output line-to-line voltage and its harmonic distortion waveforms respectively. The total harmonic distortion of the output line voltage incorporating the proposed reference disposition modulation technique is 41.09%. The output line currents of the inverter, whose ripple can be eliminated using a proper filter, for the RD-LSPWM is shown in Figure 5.12.

Figure 5.9 Output voltage (line to load neutral) of the inverter (refer to Figure 5.1)

Figure 5.10 Output line-to-line voltage (V_{ab}) of the inverter (refer to Figure 5.1)

Figure 5.11 THD of output line-to-line voltage (refer to Figure 5.1)

Figure 5.12 Output line currents of the inverter (refer to Figure 5.1)

5.4.2. Experimental verification

A hardware prototype of the Dual Z-Source network implementing the proposed Reference Disposition modulation with the help of dSpace RT1103 is built for this research. The hardware prototype is designed and implemented to verify the simulation results discussed in Section 5.4.1 and is illustrated in Figure 5.13. All the results presented in this chapter are implemented using the parameters tabulated in Table 5.2. The experimental results obtained matches the theoretical calculation and simulation results, verifying the applicability of the proposed modulation control even under a low switching frequency of 1 kHz.

Table 5.2 System parameters for both simulation and experimental prototypes

Parameter	Specification
DC supply (V)	40
Z-Source Inductor (mH)	5
Z-Source Capacitor (μ F)	1000
Switching frequency (kHz)	1
Load Resistance (Ω)	30
Load Inductor (mH)	6
Fundamental frequency (Hz)	50

Figure 5.13 Experimental set-up of Dual Z-Source Network (DZSN) implementing RD-LSPWM

Figure 5.14 Experimental Upper Capacitor voltage with $M=0.85$ (10V/div)

Figures 5.14 and 5.15 illustrates the experimental value of the upper link capacitor and dc-link voltage, respectively. From Figure 5.15, the average value of the dc-link is determined as 54.6 V, which is quite similar to the theoretical calculation of 54 V. The upper link capacitors and the dc-link voltage are similar to the values obtained in the simulation results.

Figure 5.15 Experimental upper dc link voltage with $M = 0.85$ (20V/div)

Figure 5.16 Experimental Lower Capacitor voltage with $M=0.85$ (10V/div)

Figure 5.17 Experimental lower dc link voltage with $M = 0.85$ (20V/div)

Figure 5.18 Experimental phase voltages (V_{aN} , V_{bN} , V_{cN}) (75V/div) and their respective FFT spectrum (20V/div)

Figure 5.19 Experimental voltage (line to load neutral) (50V/div) for phases a, b & c and their respective FFT spectrum (15V/div)

Figure 5.20 Experimental three-phase line-to-line voltage (V_{AB}) (150V/div) and its FFT spectrum (20V/div)

Figure 5.21 Experimental three-phase output currents (I_a, I_b, I_c) with RL load (500mA/div)

Similarly, the lower network capacitor and dc-link experimental results are illustrated in Figures 5.16 and 5.17 respectively, which indicates agreement between the theoretical and simulation results. From the dc-link voltage waveforms, it is evident that the output of Z-Source network is not constant anymore unlike the traditional voltage source inverter. The voltage goes to zero when the circuit enters the ST state and is verified in the simulation and experiments.

The experimental results of the phase voltages (V_{aN} , V_{bN} & V_{cN}) and line to the load neutral voltages for all the three-phases of the inverter are illustrated in Figures 5.18 and 5.19, respectively. Furthermore, the corresponding FFT spectrum of both the voltages are given in the same figures. The line-to-line voltage (V_{AB}) is portrayed in Figure 5.20 and the corresponding FFT spectrum is presented. The harmonics at the operating switching frequency 1 kHz is eliminated in the line-to-line voltage. The three-phase output currents are depicted in Figure

5.21. A comparison of the theoretical, simulation and the experimental values obtained are illustrated in Table 5.3.

Table 5.3 Overview of Results

Parameter	Theoretical	Simulation	Experiment
Upper Capacitor (V)	52.2	53.2	58
Upper dc-link (average) (V)	54	53.1	54.6
Lower Capacitor (V)	52.2	53.1	55
Lower dc-link (average) (V)	54	53.2	56.3
AC voltage (peak) (V)	88	85	82

5.5. Summary

This chapter evaluates the performance of the proposed novel modulation method for careful ST of two individual dc sources supplying the dual Z-Source inverters whose output ac voltage can be stepped up or down. Evaluation of the simulation and experimental results are performed and the findings of the research are presented, for the proposed modulation method wherein practical cases considering the losses. To implement this modulation method for practical cases, the dual Z-Source network is non-ideal i.e., the voltage drops across the circuits are considered. The ST duty ratio and the modulation index for the ST duty ratio are analysed based on the MCBC method. The proposed modulation method uses two-level shifted reference waves that are compared with the carrier to provide the switching. Furthermore, two modified signals are used to control the UST and LST states of the inverter. The full ST state of the inverter is rejected to avoid the volt-sec error. This novel method achieves neutral point balancing which eliminates additional voltage stress on the switches. As this method incorporated phase disposition scheme, it aids in easier implementation when compared to the space vector for DZSN. The simulation results are presented to validate the performance of the modulation method in a dual impedance network and are subsequently verified with the experimental results. From the results, it can be concluded that the dc-link voltages are balanced even during non-ideal condition. Furthermore, the output line voltage harmonic distortion for the reference disposition based modulation method is determined as 41.09%, which is recommended for a three-level operation in industrial and in Distributed Energy Resources

(DER) applications with one of the power sources being a fuel cell. Another important advantage of the proposed modulation is its operability at relatively low switching frequency without losing the ability to provide optimal waveforms. The validity of the RD-LSPWM is indicated by the agreement of the calculated boost factor value in this modulation method with [44]. Furthermore, it is evident that boost factor remains unaffected despite the voltage drop across the resistances. Examining the attributes of the proposed modulation method performance indicates the utility of Reference Disposition Level Shifted Pulse Width Modulation method in industrial and DER applications.

Chapter 6 Evaluation of PEMFC with Traditional and Two-Level Z-Source Inverters

6.1. Modeling of PEMFC

A simple model for the Proton Exchange Membrane Fuel Cell (PEMFC) based on [119] is used for this research and is illustrated in Figure 6.1. The model consists of a fuel cell stack represented by a voltage source and a resistance connected in series with it. E and E_{OC} represent the effective voltage and the open circuit voltage of the fuel cell respectively. The output voltage of the fuel cell is:

$$V_{fc} = E - R \cdot i_{fc} \quad (6.1)$$

In general, the controlled voltage of the fuel cell is given by the following equation:

$$E = E_{OC} - N \cdot A \cdot \ln \frac{i_{fc}}{i_0} \quad (6.2)$$

where,

E_{OC} – open circuit voltage (V)

N – number of cells

A – Tafel slope (V)

i_0 – exchange current (A)

R – internal resistance (Ω)

i_{fc} – fuel cell current (A)

V_{fc} – fuel cell voltage (V)

The controlled voltage is obtained from [1] and the electrical model of the losses, primarily the activation loss, is included by connecting a RC branch in parallel. The output of the fuel cell voltage will observe a delay which is approximated as twice the time constant ($\tau = RC$), when there is a sudden change in the fuel cell current. The

effect of the delay is represented in the controlled voltage of the fuel cell with a first order transfer function.

Therefore, the changes in the controlled voltage of the fuel cell is:

$$E = E_{oc} - N.A.ln \frac{i_{fc}}{i_0} \cdot \frac{1}{s \cdot \frac{T_d}{3} + 1} \quad (6.3)$$

where,

T_d – Response time (sec)

The fuel cell stack used in this research is designed considering the temperature and pressure of the fuel cell. Also, the flow rate of the fuel and air are varied to analyse the performance of the inverters. These variations affect the Tafel slope, exchange current, and the open circuit of the voltage. A typical description of the system is depicted in Figure 6.1. The Nernst voltage and the exchange current are represented by E_n and i_0 respectively, which are functions of the utilisation of hydrogen (H_2) and oxygen (O_2) as shown in Equation (6.4).

$$E_n, i_0 = f(U_{H_2}, U_{O_2}) \quad (6.4)$$

Figure 6.1 Schematic representation of fuel cell stack model

The utilisation of fuel and air are given by the following equations:

$$U_{H_2} = \frac{60000 \cdot R \cdot T \cdot i_{fc}}{z \cdot F \cdot P_{fuel} \cdot V_{fuel} \cdot x\%} \quad (6.5)$$

$$U_{O_2} = \frac{60000 \cdot R \cdot T \cdot i_{fc}}{2 \cdot z \cdot F \cdot P_{fuel} \cdot V_{fuel} \cdot y\%} \quad (6.6)$$

where,

P_{fuel} = absolute supply pressure of fuel (atm)

P_{air} = absolute supply pressure of air (atm)

V_{fuel} = fuel flow rate (l/min)

V_{air} = air flow rate (l/min)

x = percentage of hydrogen in the fuel (%)

y = percentage of oxygen in the oxidant (%)

So the open circuit voltage, exchange current and Tafel slope are given by the updated series of equations as in [7], [118]:

$$E_{OC} = x \cdot E_n \quad (6.6)$$

$$i_0 = \frac{z \cdot F \cdot k (P_{H_2} + P_{O_2})}{R \cdot h} \cdot \exp\left(\frac{-\Delta G}{RT}\right) \quad (6.7)$$

$$A = RT/z\alpha F \quad (6.8)$$

where,

E_n – Nernst voltage (V)

x – voltage constant at nominal condition of operation

z – number of moving electrons ($z=2$)

k – Boltzmann's constant (1.38×10^{-23} J/K)

F – 96485 A s/mol

P_{H_2} – partial pressure of hydrogen inside the stack (atm)

R – 8.3145 J/(mol K)

P_{O_2} – partial pressure of oxygen inside the stack (atm)

α – charge transfer coefficient

h – Planck's constant (6.626×10^{-34} J s)

T – operating temperature (K)

ΔG – activation energy barrier (J)

Based on the above equations, the fuel cell is modeled and the diode is included in the circuit as illustrated in Figure 6.1 to prevent any negative current flowing into the stack. Furthermore, a flow rate regulator is also incorporated to regulate the fuel flow rate based on the fuel cell output current of the fuel cell. while the air flow is being maintained at a constant rate of 401 litres per minute. Under this operating condition, the fuel can be utilised efficiently at more than 99%. This model will be incorporated with the converters and their performance will be evaluated.

6.2. Key Results

The PEMFC stack modeled described in the previous section is used with the traditional and Z-Source. The MBC method is chosen in this part of the study for two-level inverters, given its wide operating region as determined in Figure 3.14. The performance of the fuel cell with the boost converter and the Z-Source inverter implementing the MBC method is studied and the corresponding simulation results are analysed. The block diagrams of the system are depicted in Figures 6.2 and 6.3, respectively. The system consists of a fuel cell stack, a fuel regulator, a boost converter or a three-phase Z-Source inverter controlled by SPWM and a corresponding RL load. The initial cases in this chapter present the results of the PEMFC connected to the load via boost converter followed by connecting the fuel to the load via Z-Source. The changes in fuel flow rate, the fuel utilisation, stack consumption and the stack efficiency are studied. The output voltage and the output current of the fuel cell, dc-link voltage and the three-phase output current and voltage are evaluated using MATLAB and Simulink. The analysis is performed for the following paradigms:

- constant fuel flow rate with balanced and unbalanced load condition for boost converter
- constant fuel flow rate with balanced and unbalanced load condition for Z-Source inverter
- variable fuel flow rate with boost and Z-inverters

In this study, PEMFC has a nominal operating power of 6kW. Table 6.1 tabulates the PEMFC stack and the operating parameters used in this research.

Table 6.1 Operating parameters of the system

Parameters	Value
Nominal power (W)	6000
Nominal voltage (V)	45
Nominal current (A)	133.3
Maximal power (W)	8325
Nernst voltage of a single cell (V)	1.1288
Exchange current, i_o (A)	0.0160
Number of cells, N	65
Internal resistance of the PEMFC stack, R_{fc} (Ω)	0.0757
Nominal operating temperature (K)	338
Absolute supply pressure of fuel (atm)	1.5
Absolute supply pressure of air (atm)	1
Amount of hydrogen (%)	99.95
Amount of oxygen (%)	21
Z-Source Inductor (mH)	2
Z-Source Capacitor (μ F)	1000
Switching Frequency (kHz)	1
Load Inductor (mH)	15
Load Resistance (Ω)	2
Fundamental frequency (Hz)	50

Figure 6.2 Block diagram of fuel cell stack model with traditional boost converter and VSI

Figure 6.3 Block diagram of fuel cell stack model with traditional boost converter and VSI

6.3. Case 1: Constant fuel flow rate

In Case 1, the fuel cell stack is operated with a constant fuel rate of 5lpm. The hydrogen flow rate is maintained at a constant rate throughout the operation. For this condition, the operation of the fuel cell stack is studied with the boost converter and the Z-Source inverter. Furthermore, with a constant fuel flow rate, the fuel cell is operated for two different load conditions and the performances have been analysed. The simulation results are presented below for the balanced and the unbalanced load conditions.

6.3.1. Operation of fuel cell stack with boost converter under balanced load

The schematic diagram of the fuel cell integrated with the boost converter is determined in Figure 6.4. Figure 6.5 determined the simulation results of the fuel cell stack when operated with the boost converter. The fuel flow rate, which is expressed in litres per minute (lpm), is maintained constant during the experiment. Even though the fuel flow is maintained constant, a fuel flow regulator is used to regulate the flow of hydrogen gas into PEMFC. The corresponding oxygen and hydrogen utilisation rates are presented in the figure. After the commencement of the experiment, a drop in the utilisation rate occurs. The initial change occurs due to the

Figure 6.4 Schematic representation of the fuel cell integrated to the boost converter

Figure 6.5 Stack Characteristics under balanced load condition

transient state of the voltage regulator. After that instant, the utilisation reverts to normal operation and consumption rate of the hydrogen and oxygen fuels. These details are plotted in the Figure 6.5 (d) and (e) respectively. The efficiency of the fuel cell system illustrated in Figure 6.5(f) is determined as 25%, which is within the range of the theoretical efficiency of PEMFC.

Figure 6.6 illustrates the fuel cell output voltage, current and the dc-link voltage. At $t = 0$, when the fuel cell voltage is low, the current is at its maximum value. When the voltage increases with time, the current decreases simultaneously, proving the concept of a fuel cell. The boost converter boosts the voltage to 100 V, and is observable from Figure 6.6. The peak at the beginning of the dc-link voltage is due to the transient effect of the fuel flow regulator. The corresponding three-phase ac output voltage and current are illustrated in Figures 6.7 and 6.8, respectively. Under balanced load condition the three-phase output currents of the inverter must possess identical magnitude, and is observable in Figure 6.8.

Figure 6.6 Output Waveforms of fuel cell and dc link under balanced load condition

Figure 6.8 Three phase Output currents of the inverter under balanced load condition

Figure 6.9 Current FFT of the inverter under balanced load condition

Figure 6.8 shows the three-phase output phase current and its corresponding FFT has been shown in Figure 6.9. From the Figure 6.9, it can be observed the fundamental frequency at 50 Hz has a magnitude of 8.096 A and a total harmonic distortion of 3.36% for the balanced load condition. With the operation of fuel cell stack examined for boost converter, the analysis is with Z-Source inverter is discussed in the following section.

6.3.2. Operation of fuel cell stack with Z-Source inverter under balanced load

The schematic diagram of the fuel cell integrated with the Z-Source inverter is illustrated in Figure 6.10. The parameters that control the output voltage of the fuel cell is depicted in Figure 6.1. The schematic diagram shows the fuel cell stack represented as E . In this section the operation of the fuel cell stack with constant fuel flow rate with the Z-Source implementing the maximum boost control method is investigated. The corresponding changes in the fuel cell stack including, the consumption of fuel and air, output voltage of stack, output current of stack and the stack efficiency are plotted.

Figure 6.10 Schematic representation of the fuel cell integrated to the Z-Source inverter

With the operation of the fuel with boost converter been investigated, similarly, the operation of fuel cell with the Z-Source inverter is investigated. The results are presented in the following section. All the simulation studies carried out for boost converter, have been performed for Z-Source. The fuel flow rate is maintained constant. Unlike boost converter, the utilisation rate of oxygen is maintained constant. The fuel consumed by the Z-Source inverter is lesser than the fuel consumption of the boost converter. The consumption is reduced and can be observed in Figures 6.11 (b), (c), (d) and (f). The efficiency of the stack is determined as 20%. When compared to the efficiency of the fuel cell with boost converter, the efficiency of fuel cell with Z-Source decreases and can be deduced from Figure 6.11. Even though there is a drop in efficiency, the output voltage of the fuel cell remains constant. Also, the Z-Source inverter performs the boost operation and the dc-link voltage is 95 V, and is considered reasonable, given that the boost converter is 100 V. Even with lesser amount of fuel utilised, the dc-link voltage is boosted to a value similar to the boost converter.

Figure 6.11 Stack Characteristics under balanced load condition

Figure 6.12 Output Waveforms of fuel cell and dc-link under balanced load condition

The fuel cell output voltage, output current and the dc-link output voltage are depicted in Figure 6.12. The dc-link voltage is maintained at a desirable value to meet the load demand. From the dc-link voltage in Figure 6.12, no peak is observed at the beginning of the experiment. This proves that the Z-Source inverter eliminates the effect of the voltage regulator. The dc-link voltage can be further boosted by controlling the ST states in the inverter. The three-phase ac output voltage and the current of the fuel cell system with Z-Source inverter are illustrated in Figures 6.13 and 6.14, respectively. From Figure 6.14, it is surmised that the output current is almost sinusoidal and the three-phase currents are identical. This serves as the confirmation that the system operates in a balanced load condition.

Figure 6.13 Output phase voltages of the inverter under balanced load condition

Figure 6.14 Three-phase AC output currents of the inverter under balanced load condition

Figure 6.15 Current FFT of the inverter under balanced load condition

Figure 6.15 illustrates the current FFT of the Z-Source inverter with a balanced load condition and a constant fuel rate. For the balanced load condition, from the Figure 6.15, it can be observed that the fundamental component at the frequency 50 Hz has a magnitude of 6.073 A and total harmonic distortion of 2.31%. When compared to the current FFT waveform of the boost converter shown in Figure 6.9, the total harmonic distortion of the Z-Source inverter is low. This ensures that the operation of the Z-Source inverter is improved when compared to the boost converter.

The performance of the fuel cell stack with both the boost converter and the Z-Source inverter are evaluated. As mentioned earlier, the fuel flow rate is constant and the input variables of the fuel cell, the output of the fuel cell, dc-link voltage and the ac output voltage and current for both the converters are plotted. The utilisation of the fuel is shown in Figures 6.5 and 6.11 for boost and Z-Source inverters respectively. From the results the output of the fuel cell can be studied. Changes in the utilisation of the fuels is observed when the stack is used with Z-Source inverter unlike the boost converter. Regardless of the decrease in the fuel utilisation, Z-Source provided the required amount of dc-link voltage. As utilisation influences the efficiency of the fuel cell stack, the variation causes the efficiency of the stack to drop. The reason for the decrease in the utilisation is under investigation. When the utilisation is corrected, the efficiency is expected to increase. In this report, the Z-Source inverter is utilised with a modulation index of 0.7. In addition, the output of the boost converter is static. However, the output of the dc-link voltage of the Z-source inverter can be further increased by adjusting the ST duty ratio to a higher value. Thus, Z-Source inverter can be used for an energy neutral building in situations where boost converters are implemented.

6.3.3. Operation of fuel cell stack with boost converter under unbalanced load

Figure 6.4 presents the schematic diagram of the fuel cell stack with the boost converter. The previous section discussed the performance of the fuel cell stack under balanced load condition. In this case, the load is varied but the constant fuel flow rate is maintained. The load changes will cause a change in the output current, thereby, affecting the efficiency of the fuel cell. There would be changes in the utilisation and the consumption of the fuel cell. Therefore, the performance of the fuel cell stack integrated with a boost converter under unbalanced load condition is studied using Matlab/Simulink and the simulation results are presented.

Figure 6.16 Stack Characteristics under unbalanced load condition

The performance of the fuel cell stack for the unbalanced load condition is depicted in Figure 6.16. The oxygen utilisation is maintained constant, similar to the balanced load condition. The percentage of hydrogen utilisation changes and can be inferred from Figure 6.16(c). It undergoes slight reduction when compared to the balanced load utilisation, shown in Figure 6.5(c). There are some drops at the initial stages of the utilisation, which is primarily attributable to the transient state of the voltage regulator. The drops are substantial when compared to

the balanced load condition. After few seconds, the fuel cell utilisation is reverts to a normal operation. The consumption of air and fuel in litres per minute is illustrated in Figures 6.16(d) and (e) respectively. The efficiency of the fuel cell is computed as 25% during unbalanced load as illustrated in Figure 6.16(f).

Figure 6.17 Output Waveforms of fuel cell and dc-link under unbalanced load condition

Figure 6.17 illustrates the fuel cell output voltage, output current and the dc-link voltage. The fuel cell output waveform drops to zero once there is no utilisation. The dc-link voltage rises to 125 V peak due to the transient effect of the regulator. Even with the change in load, the boost converter is designed to provide 100 V at the output which is exemplified by Figure 6.17. Figures 6.18 and 6.19 indicate the ac output line voltages and ac output current waveforms, respectively. From Figure 6.19 it can be observed that the magnitudes of the three-phase ac currents are dissimilar, indicating that the system is operating under unbalanced load condition.

Figure 6.18 Output phase voltages of the inverter under unbalanced load condition

Figure 6.19 Three-phase output current of the inverter under unbalanced load condition

Figure 6.20 Current FFT of the inverter under unbalanced load condition

The current FFT for the three-phase ac current obtained from integrating the fuel cell stack with the boost converter under unbalanced load condition is illustrated in Figure 6.20. This figure indicates that the fundamental component at 50 Hz is 8.905 A and the total harmonic distortion is 3.80%, which is higher than 3.36% total harmonic distortion obtained during the balanced load condition. The small variation in total harmonic distortion and the fundamental component is attributed to unbalance in the three-phase current.

6.3.4. Operation of fuel cell stack with Z-Source inverter under unbalanced load

Figure 6.10 presents the schematic diagram of the fuel cell stack with the Z-Source inverter. With the performance analysis of the fuel cell stack with boost converter implementing the maximum boost modulation method completed, the performance of the fuel cell stack with Z-Source is investigated under unbalanced load condition. The input fuel flow rate is maintained constant throughout. The load changes would result in changes to the output current, utilisation and consumption. This would impact the efficiency of the fuel cell. Hence, the performance of the fuel cell stack integrated to a Z-Source inverter under unbalanced load condition is examined and the simulation results are presented using Simulink.

Figure 6.21 Stack Characteristics under unbalanced load condition

The simulation results of the fuel cell stack with the Z-Source inverter under unbalanced load condition is illustrated in Figure 6.21. The utilisation rate of oxygen is maintained at identical magnitudes for the balanced and the unbalanced conditions which is observed from Figures 6.11(b) and 6.21(b). Notably, the utilisation rate does not decline to zero at any instance. There is a change in the percentage of hydrogen utilised as observed from Figure 6.21(c), which remains lesser than the boost converter. The consumption of air and fuel solely depends on the load requirements and depicted in Figure 6.21(d) and (e), respectively. The efficiency of the fuel cell stack during the unbalanced load is 20%. This is lesser than the boost converter, when the latter operated

under the unbalanced load condition. Notably, the Z-Source inverter managed to give around 95 V output voltage even though the efficiency underwent reduction.

Figure 6.22 Output Waveforms of fuel cell and dc-link under unbalanced load condition

The fuel cell output voltage, fuel cell output current and dc-link voltage are shown at the top, middle and bottom of Figure 6.22, respectively. As explained earlier, the dc-link voltage can be further increased by adjusting the ST duty ratio of the Z-Source inverter. Z-Source inverter again eliminates the peak at the beginning of the dc-link voltage during unbalanced condition. The dc-link voltage is boosted to the desired value despite with lesser usage of fuel. Figures 6.23 and 6.24 respectively portray the three-phase output voltage and current waveforms. From Figure 6.24, it can be observed that the magnitudes of the three-phase currents are dissimilar, thereby, demonstrating the performance of the fuel cell stack for the unbalanced load condition.

Figure 6.23 Output phase voltages of the inverter under unbalanced load condition

Figure 6.24 Three-phase output current of the inverter under unbalanced load condition

Figure 6.25 Current FFT for phase a of the inverter under unbalanced load condition

Figure 6.25 portrays the current FFT for the unbalanced load condition for Z-Source inverter that is integrated with the fuel cell stack. The fundamental component has a magnitude of 6.957 A and total harmonic distortion

of 2.26%. By comparing the results in Figure 6.25 with Figure 6.20, the Z-Source inverter provides lesser harmonic distortion than boost converter even under unbalanced load condition. With the results for the performance of the converters under constant fuel flow rate discussed, the performances under variable fuel flow rate for both the converters are investigated in the Section 6.4.

6.4. Case 2: Variable fuel flow rate

The schematic diagram of the system are depicted in Figures 6.4 and 6.10 for the boost converter and Z-Source inverter, respectively. This case is analysed by introducing a small change in the input i.e. fuel flow rate. In this case, the hydrogen flow rate to the fuel cell stack is varied after a particular interval of time. With the varying flow rates, the performance of the fuel cell stack with the boost converter and the Z-Source are investigated. Furthermore, the changes in the output of the fuel cell and dc-link voltage are quantified. The corresponding waveforms are presented in Sections 6.4.1 and 6.4.2.

6.4.1. Operation of fuel cell with boost converter

In this section, the performance of the system with variable fuel rate is analysed. A fuel flow regulator is used to maintain the fuel (hydrogen) utilisation at a value of 99.56% for the first 1 sec. By bypassing the fuel flow rate after 1 sec, the rate of the fuel utilisation is allowed to vary and is shown in Figure 6.26(a). Now, the fuel flow rate is increased to 10lpm. Subsequently, the changes in the voltage of the stack are observed. The changes in the utilisation of fuel would definitely impact on the amounts of fuel and oxygen consumed and the efficiency of the fuel cell stack. With increase in the fuel flow rate, the hydrogen utilisation is commensurately reduced. This causes an increase in the Nernst voltage, decreasing the output current of the fuel cell. Hence, the fuel consumption by the fuel cell stack and the efficiency of the fuel cell stack decrease. The changes in utilisation, consumption and efficiency of the fuel cell stack for different flow rates are shown in Figure 6.26 (b)&(c), (d)&(e) and (f), respectively. The change in the fuel flow rate impacts the fuel cell stack output. The output voltage, output current of the fuel cell and the dc-link voltage are illustrated in Figure 6.27. From Figure 6.27, it can be observed that the dc-link voltage is maintained at 100 V by the boost converter. Therefore, the required power for meeting the demand is delivered.

Figure 6.26 Stack Characteristics under variable fuel flow rate condition

Figure 6.27 Output Waveforms of fuel cell and dc-link under variable fuel flow rate condition

6.4.2. Operation of fuel cell with Z-Source inverter

As discussed previously, the performance of the fuel cell stack and Z-Source inverter with variable fuel flow rate is analysed. As inferred from Figure 6.28, fuel rate is shifted from 5lpm to 10lpm after the first second of the simulation. This results in a change in the stack efficiency and percentage of H_2 being utilised decreases. As the load demand does not change, the consumption of fuel remains stable. Therefore, for any given load demand, if the fuel flow rate can be controlled optimally, the fuel cell can be utilised efficiently. The results for the changes in utilisation, consumption and efficiency of the fuel cell stack for different flow rates are depicted in Figure 6.28 (b)&(c), (d)&(e) and (f), respectively. Changes in the fuel flow rate impacts only the fuel cell stack output. The output voltage, output current of the fuel cell and the dc-link voltage are illustrated in Figure 6.29 It can be observed that the dc-link voltage is maintained around 95 V by the Z-Source inverter. This ensures the deliverance of the required power to meet the demand.

Figure 6.28 Stack Characteristics under variable fuel flow rate condition

Figure 6.29 Output Waveforms of fuel cell and dc-link under variable fuel flow rate condition

The performance results of the PEMFC stack with boost converter and Z-Source inverter under variable fuel flow condition is depicted in Figures 6.26, 6.27, 6.28 and 6.29. The fuel flow rate is increased from 5lpm to 10lpm as observed from Figure 6.26(a). The percentage of oxygen utilised in this research is maintained constant and the utilisation of the hydrogen is the sole variable. The utilisation rate of hydrogen in Figure 6.26(c) decreases when the fuel flow rate is increased. The efficiency of the fuel cell stack is calculated based on the utilisation of the fuels for the chemical reaction that generates power. An important conclusion of this research is that the hydrogen consumption and utilisation rate affects the efficiency in fuel cell stack for both conditions of constant and variable fuel flow rates. From Figures 6.27 and 6.29 it can be established that the output voltage of the fuel cell and the dc-link voltage remain unaffected. The three-phase output voltages and currents are unaffected with variations in fuel rate, as the converters maintain the dc-link voltage. The waveforms are not presented in the section.

6.5. Summary

Fuel cell is an important energy source, and is a part of the promising and emerging technology for a DER application. Given the importance of this technology, this research uses fuel cell as the dc source. The initial part of this chapter deals with the modeling of the fuel cell. The modeled fuel cell is then integrated to either boost converter or ZSI and their performances are evaluated. The utilisation, consumption of fuel and air are monitored to track changes in fuel flow and efficiency. The fuel flow regulator performs the important task of maintaining the fuel flow at a sufficient rate to evaluate the operation of the fuel cell. Therefore, fuel flow regulator plays the primary role in altering the fuel rate based on demand. From the results of the balanced and unbalanced load conditions, the transient effect of the regulator is more prominent (dc-link peak voltage of $125V_0$) in the results of boost converter. Importantly, this effect is completely eliminated by Z-Source inverter. The ZSI also provides a smooth transition due to the capacitor network. Another point to be noted from the results is that ZSI uses less fuel when compared to boost converter and the output of both are more or less the same. The Z-Source inverter deliver the desired voltage irrespective of the change in the fuel flow rate, providing an impetus for the usage of ZSI. The major concern about the traditional boost converters is the static output voltage. However, in ZSI, the output can be boosted by adjusting the ST duty cycle. Therefore, Z-Source inverter is a viable and an improved alternative to the traditional boost converter in distributed energy resources application.

Chapter 7 Conclusions and Recommendations for Future Research

7.1. Conclusions

Recently, Z-Source inverter, a single-stage energy conversion technology, has gained attention in Renewable energy conversion. This research concentrates on the topological and modulation designs of two-level and three-level Z-Source inverters. With a motive to integrate Z-Source inverter with the DER systems, Chapter 1 in this thesis expounds the need for a substitute or an enrichment to the traditional means of power generation. DER acts as a quicker and an economical recourse to the establishment of huge, centralised power plants and high-voltage transmission lines. Therefore, DER systems offer consumers with a more reliable service, greater energy efficiency, good power quality, possibilities for lower cost, and energy independence.

Even though the output of the distributed energy sources is electrical, power regulators are needed to avoid problems that arise due to unexpected fluctuations. Therefore, in Chapter 2, the existing means of two-stage and single-stage energy conversion are explained. The reasons for preferring single-stage power conversion to traditional two-staged power conversion are analysed. As this research in topologies that extends from two-level to multilevel inverters, a review on the most commonly preferred multilevel topologies is presented. To operate any power inverters with high efficiency and low switching loss, proper modulation method should be implemented. This chapter also reviews some of the Pulse Width Modulation schemes for multilevel inverters. The renewable Distributed Energy Resources (DER) technologies such as photovoltaic, wind system, biomass, fuel cell or hydroelectric power provide momentous benefits to the environment are reviewed in this chapter. Fuel cell shows improved performance when connected as a part of a DER system, and therefore was one of the principal components opted for this research. Hence, an objective of this research is to evaluate the performance of fuel cell, by connecting the fuel cell as a dc source with the Two-Level inverters.

As Z-Source inverters are the focus of this research, the work is primarily divided into two sections. The first section investigates the performance of a new modulation method for three-level Z-Source inverter and the second section evaluates the two-level Z-Source inverter with the fuel cell. In Chapter 3, the mathematical analysis of the modulation methods used for the ZSI operation is presented. From the analysis the method with a wide operating range, is chosen for controlling the two-level inverter operation whereas, the method with

constant boost is chosen for three-level inverter operation. The overview of the multilevel ZSI is also presented in this chapter.

In Chapter 4, the NPC topology is integrated with the Z-Source topology to provide voltage buck and boost capabilities. The Z-Source NPC is designed by connecting two Z-Source networks (supplied by two individual dc sources) and the operating principles are presented. The main challenge is the insertion of the ST states for the three-level operation. In this chapter, a new modulation method (Reference Disposition Level Shifted Pulse Width Modulation) is proposed, which is based on the basic carrier comparison method. When designing this modulation method, substantial care is taken to insert the ST states aptly to ensure that the modulation scheme operates with a maximum of six operating devices per half switching cycle. This prevents drawbacks like the introduction of volt-sec error to the inverter output. After the theoretical analysis, the proposed control method is tested by simulation and the results obtained is in agreement with the analysis. As two individual dc sources are used to supply power to the Z-Source networks, it is possible that the voltage output of the dc sources will vary. In this case, the neutral point balancing can be affected. Considering these limitations, the ST duration is adjusted for the upper and lower Z-Source networks. As the output of the dc-links primarily depends on the capacitors in the impedance networks, the capacitor voltages are considered the primary factor when modifying the ST duration. With proper adjustment to the ST period, neutral point balancing can be achieved. This process is demonstrated with illustrated results in this chapter and subsequently, the results are verified using simulation.

The Dual Z-Source network considered is based on ideal condition. In real cases, there are voltage drops across the circuit. With the motive of implementing the proposed modulation method for real time applications, the topology of the dual Z-Source network is reconfigured. The new topology considers the voltage drop by connecting resistance in series with the dc sources, thereby rendering it non-ideal. The mathematical analysis was performed again after the addition of resistance. This was proved by conducting experiments and the results are verified using simulation. In continuation, the performance of the proposed control method is tested using simulation. The results obtained from the simulation are similar to the mathematical analysis. As the principle objective is the implementation of the control method in real time, an experimental setup was built and the control method was tested. From the results, the control method can provide neutral point balancing even during non-ideal condition. The results obtained through experimentation demonstrate substantial agreement with the theoretical and simulation results. The only limitation is that the boost factor is lower when compared to that of the ideal condition. However, the proposed reference disposition level shifted PWM for Z-Source NPC operates with less switching loss, low THD, and more over provides the flexibility of easier implementation.

Another principle objective is the successful integration of the Z-Source with DER system. Therefore, this research investigates the performance of two-level inverters with the PEMFC. The fuel cell was sized to operate with a nominal power of 6kW. The parameters of the fuel cell stack used in this research are explained in Chapter 6. The calculations of these parameters were done based on [24]. With the design of the PEMFC, the stack was connected to the traditional boost converter with VSI and maximum boost modulated ZSI. The performance of both the converter were analysed under two different sets of conditions. The fuel flow rate was the varying parameter and its impact on utilisation, consumption and efficiency was analysed. In case 1 (constant fuel flow rate), the fuel flow rate was maintained at a nominal value or constant and the performance of the stack with the both converters were observed using simulations. Even though the efficiency was marginally compensated, which was mainly due to the change in the utilisation of the fuels, the output of the stack and dc-link voltage was always maintained, and the load demand was met. In case 2 (variable fuel flow rate), during the first second, the utilisation of hydrogen was maintained at a nominal value using the fuel flow regulator. After this sec, by bypassing the fuel flow regulator, the fuel rate was increased. This caused a variation in the stack voltage and changed the efficiency of the system. The boost and the Z-Source inverter regulate the dc-link voltage, irrespective of the fuel flow rate.

From the results obtained, it can be observed that Z-Source utilises lesser fuel when compared to boost converter even when boosting by both converters remained identical. For a fuel cell to be used as a source, regulators play a vital role. However, sufficient analysis needs to be conducted to prevent any impact on the dc-link output by the regulators. Results showed a surge at the beginning of boost converter dc output which was subsequently eliminated in the Z-Source operation. Moreover, the output of the boost converter is fixed unlike the Z-Source inverter wherein the ST state decides the amount of boosting performed by the Z-Source inverter. By adjusting the ST state, the Z-Source inverter output can be further boosted. In addition, the L and C network in the Z-Source may cut the need for low pass filters. Therefore, with this conclusion, the research aims to implement the same analysis for a three-level Z-Source operation in future.

7.2. Recommendations for future work

Following research into the previous ZSI frameworks, a few extensions of the two-level and three-level ZSI would further the understanding of ZSI principles.

This thesis mainly concentrates on the fuel cell as the input source for two-level operation with the focus on the DER systems. Even though fuel cell is increasingly preferred, its performance is improved when connected as a

distributed generation sources. For future applications, fuel cell with Z-Source can be integrated to variable distributed generation sources to increase the productivity.

In the DER applications energy storage systems like battery and ultra-capacitors are widely used along with the fuel cell to meet the demand when the output from the fuel cell is insufficient. In-order to integrate battery with the fuel cell that subscribes to the traditional PWM technique, an additional DC-DC boost converter is required. This increases the complexity, volume and cost of the system. This drawback can be overcome by using the Z-Source inverter with a slight modification to the topology, by replacing one of the capacitors with battery in the impedance LC network, the Z-Source inverter. Hence, the additional DC-DC converter is eliminated and the same impedance network can be used to connect the main inverter circuit to any dc power source. More advantages include the ability to control the input power, the output power and the state of charge of the battery by adjusting the ST duty ratio. A potential research topic is the study on the state of charge of battery to find a possible method to integrate within the Z-Source network.

With substantial increases in the demand for power, multi-level inverters have emerged as a satisfactory solution. These inverters possess an array of power semiconductor and capacitor voltage sources and the output voltage generated by these inverters are in stepped waveforms. One such multilevel inverter is presented in this thesis. Usually, the research focuses solely on the NPC inverters. Further studies investigating the procedure to integrate the Z-Source inverter with flying capacitor topology is another potential field of interest.

Traditionally voltage source converters are universally preferred. Therefore, the topologies investigated in the research are mostly voltage fed. Even though current-fed inverters are less popular when compared to voltage-fed, there exist applications where current-fed inverters are preferred. Future research could investigate the operation of the current-fed Z-Source inverters.

In addition, for three-level operations the two individual dc sources are considered as ideal dc sources. However, the principal aim is to use the inverters for DER applications. The ideal dc sources can be replaced with PV, wind or other renewable sources. In this research, the design of the fuel cell enables its usage in two-level and three-level inverters. Investigating the performance of the fuel cell as one of the dc source in Dual Z-Source network NPC inverter is a potential research focus.

Practically, the values of the inductors and the capacitors would be dissimilar due to tolerances. Hence, studying the effect of such imbalances is an important objective for further research.

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Appendix

Matlab/Simulink c

Matlab/Simu

PSIM circuit of

PSIM circuit of three.

Matlab/Simulink contro