Adaptive efficiency optimized power regulator for portable devices

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**NANYANG
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**ADPTIVE EFFICIENCY OPTIMIZED POWER
REGULATOR FOR PORTABLE DEVICES**

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2016

ADAPTIVE EFFICIENCY OPTIMIZED POWER REGULATOR FOR PORTABLE DEVICES

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Abstract

An adaptive efficiency optimized power regulator that can work at load current ranging from mille-ampere to ampere is developed for portable devices. Based on the proposed efficiency tracking method, the power regulator can adjust its efficiency to the highest as the load current or supply voltage varies.

An internal 10- μ A, trim-free, low temperature coefficient, supply independent current reference with process compensation feature is proposed to ensure that the system remains stable over PVT variations. Without using high gain amplifier, a 130 ppm/ $^{\circ}$ C temperature coefficient current reference across -40 $^{\circ}$ C to 80 $^{\circ}$ C temperature range is achieved. The proposed circuit can work at supply voltage varying from 2.4V to 3.2 V, with only 30-nA current drift at room temperature.

To reduce the line regulation of output voltage and clock, an internal merged structure bandgap voltage reference and a temperature independent current reference (BGVCR) is proposed. The bandgap voltage reference segment of the BGVGR is designed to serve as a reference voltage for the power regulator, while the current reference segment function as a reference current for the clock generator to produce a stable clock. The proposed proportional to absolute temperature (PTAT) current sharing approach proposed in this thesis allows amalgamation of the bandgap voltage and current reference in the same structure without them affecting each other's performance. PTAT sharing helps to compensate process variation in the proposed circuit, thus doing away with the trimming resistor array. A local feedback loop together with parasitic capacitor is deployed to achieve self-start-up. The gain of the voltage tracking loop for generating the PTAT current is also boosted. The proposed compact BGVCR attained 5 ppm/ $^{\circ}$ C temperature coefficient for bandgap voltage reference and 150 ppm/ $^{\circ}$ C temperature coefficient for the current reference across -40 $^{\circ}$ C to 80 $^{\circ}$ C temperature range at 1.8-V internal supply voltage.

Using the proposed methodology, the efficiency of the power regulator can be easily tracked using its input current. An enhanced full range current sensor based on self-bias structure for buck regulator is proposed in this thesis to sense the input current of the power regulator. The proposed full range current sensor can sense current from both the high side and low side switches of the power regulator within the same switching cycle. It has higher than 95% sensing accuracy while consuming less than 1% of the total input power. The current sensor is implemented in the power regulator with less than 1% area of the power transistor array.

The dead-time of the power regulator must be carefully controlled to achieve best efficiency. Instead of using high gain amplifier for body diode conduction sensing, or zero voltage detecting, a sensor-less adaptive dead-time control driver utilizing predictive idea for dead-time control is proposed. Unlike the conventional predictive method that requires self-adjusting or tuning during testing, a threshold voltage is used as the predictive information for dead-time control. The delay in body-diode conduction sensor or zero voltage detector is totally eliminated from the power regulator. Not only the power consumption of the system is greatly reduced, the control accuracy of the dead-time is also enhanced. With the proposed prediction circuit, less than 3-ns body-diode conduction time is obtained, while the switching loss is minimized which helps the power regulator to achieve more than 95% peak efficiency at 450-mA load with 2.4-V supply voltage.

Lastly, a complete power regulator system that includes all the building blocks described above are fabricated in 0.18- μm CMOS process, occupying a silicon area of 2 mm x 2 mm. Based on the proposed efficiency optimized method and embedded building blocks, more than 95% peak efficiency and higher than 84% overall efficiency is achieved at 2.4-V supply voltage across 70-mA to 1.1-A load range with 30 mV/A load regulation. When supply voltage is increased to 3.2 V, the efficiency drop on the converter is less than 3% and the line regulation is less than 1%/V.

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Chapter 1 Introduction

1.1 Background

In modern consumer electronic market, battery operated electronic devices such as smartphone and tablet are of great demand. However, these electronic devices consume a large amount of power ranging from several tens of mW to 1W of power [1]. This is attributed to the fact that smartphone has many different power consuming blocks such as the Global System for Mobile Communications (GSM) block, the third generation mobile telecommunications technology (3G) block, the fourth generation mobile phone mobile communication technology (4G) block, the wireless local area network (WiFi) block, Bluetooth block, display block, central processor unit (CPU), Global Positioning System (GPS) block, etc. The respective power consumption of these blocks is shown in Table 1-1.

Table 1-1 Power consumption in different blocks of a smartphone [1]

Work mode	Power consumption (mW)									
	Free runner block power consumption (mW)									Google Nexus One
	GSM	CPU	RAM	WiFi	Graphics	Audio	LCD	Others	Total	
Suspend	31	12	2	7	9	4	3	0.6	68.6	24.9
Idle	58	37	7	8	82	28	48	65.7	333.7	333.9
Network (WiFi)	80	90	50	720	-	-	-	113.7	1053.7	884.1
Network (GSM)	630	40	20	10	-	-	-	209.7	929.7	825.9
Video	60	120	40	-	110	-	60	168.8	558.8	526.3
Audio	55	60	23	-	91	32	48	110	419	322.4
GSM phone call	870	40	10	-	70	-	60	85.4	1135.4	746.8

The free runner listed in Table 1-1 is a test bench designed in [1], where it consists merely of testing blocks without any operating system. The suspend mode is a work mode where all the devices are in sleep mode and are waiting for SMS, phone call or other activities. The idle mode is when all devices are awakened but without any operation. As seen in Table 1-1, the power consumption of different blocks varies, ranging from several tens mW to nearly

1 W. At times, more than one block may be operating together; for example, when watching on-line videos, use of WiFi, graphics and display blocks being active, etc., causing the power consumption to be nearly 1.2 W.

This power is usually supported by LiCoO_4 battery that can support output voltage of 3.7 V. The popular CMOS processes such as 65nm and 40 nm CMOS technologies are usually thin oxide devices which need 1.2-V or 1.1-V supply voltage, or thick oxide devices that can only tolerate 3.3-V supply voltage. Thus, additional special process device is needed to convert the 3.7-V battery output voltage to 3.3-V on-chip voltage for the CMOS devices. This kind of high voltage process usually consumes large area and its cost is high. It also needs one more chip for power supply. This will increase the cost of the portable device and reduce the integratable level of the system.

The recent developed LiFePO_4 battery is becoming more and more popular. It has a 3.2-V output voltage and 95% energy efficiency [2-7]. A comparison table on various li-ion batteries, both conventional and recent Li-ion batteries are summarized in Table 1-2.

Table 1-2 Caparison of different kind of Lion battery.

Type	LiCoO_2	LiMn_2O_4	LiFePO_4
Normal operating voltage (V)	3.7	3.7	3.2
safety	bad	middle	good
Environmental friendly	Yes	Yes	Yes
Memory effect	No	No	No
Energy efficiency (%)	90	90	95
Cycle life	>500	>500	>2000
Charge time (hours)	2-4	2-4	<2
Self-discharge (%/month)	10	10	8

It can be seen in Table 1-2 that the LiFePO_4 battery has much better performance than the other two batteries. It is safer, has higher efficiency, longer life time as well as small self-discharging and fast charging time feature. In future, wireless charging will replace today's line based charging method. This calls for the battery to be able to charge quickly and safely. To embed the power management circuit in the SOC using commercial CMOS, the output

voltage of the battery needs to be lower than 3.3 V. Thus, the LiFePO_4 is the best choice by far.

The output voltage of LiFePO_4 battery is between 2.4 V to 3.2 V. And the core supply voltage of the SOC is usually 1.2 V or lower. Thus, a CMOS based power regulator for buck the battery voltage to 1.2 V across a wide load range is necessary.

In CMOS power regulator, the power transistor is to be carefully optimized as it usually dominate the total loss of the power regulator which includes five types of losses: (1) switching loss, (2) power transistor conduction loss, (3) shoot through current loss, (4) body diode conduction loss and (5) reverse current loss [8, 9]. The switching loss and power transistor conduction loss are determined by both the size of the power transistor and the switching frequency of the power regulator [10], and will be discussed in section 6.1. The size of the power transistor has to be optimized according to the load requirement, supply voltage and output voltage. Hence, an adaptive sizing approach for the power transistor was adopted to cater a wide load range for the power regulator [11]. The conventional method for sizing power transistor relies on the load current to do adjustment, and it cannot function well when the supply voltage varies. In battery powered electronic system, the supply voltage is always changing from 2.4 V to 3.2 V and the load current varying from several tens of mA to 1 A. The conventional load current based power transistor size selection method is therefore not the best choice. An adaptive efficiency optimized control method to adjust the power transistor size adjusting based on a best efficiency point instead of relying solely on the load current is mandate in power regulator control, and this will be the main focus of this thesis. To guarantee the performance of the transceiver, amplifier, ADC, etc. in the portable devices, the power regulator should have small line regulation, load regulation and ripple. In order to realize all these features, the system must be optimized from top to bottom. Thus, a current reference which can set the quiescent condition for error amplifier, comparator and clock generator is required. A bandgap voltage reference is also needed to guarantee the line and load regulation of the power regulator. The efficiency tracking module should rely on the input power and

output power, which needs high performance current sensor to track the input power.

The shoot through and body diode conduction loss must be carefully controlled, otherwise it will bring about large degradation in efficiency. In worse case scenarios, it may even cause severe damage to the power transistor. Thus, the dead-time between the two power transistors should be appropriately and carefully controlled to avoid any low impedance path between the supply and ground. Since the dead-time is always changing with the supply voltage or load current, the adaptive dead-time approach is thus widely adopted. The conventional adaptive dead-time control techniques involve detecting switching node voltage, inductor current or body diode conduction. The control logic is normally very complex and it demands for high gain amplifier which consumes a substantial amount of power if it has to control the dead-time with good accuracy. Hence, details on how to optimize the dead-time will also be provided in this thesis.

Suggestions for future work: the detrimental effects of the reverse inductor current phenomenon will be explored in the future work.

1.2 Objective

In this research, an adaptive efficiency power regulator with all the building blocks embedded for portable device is designed and implemented. As mentioned in the above, the proposed adaptive efficiency power regulator need to work at 1.2V output voltage with up to 1A load current. Additionally, several critical building blocks have to be optimized to guarantee system performance. These blocks include the below:

- (1) A Current reference which is an important building block, can set the quiescent condition for the error amplifier, comparator and clock generator. To guarantee that all the circuits work well across PVT variation, a current reference with low current drift across 2.4-V and 3.2-V supply voltage, low temperature coefficient (TC) across -40°C to

80°C temperature range and can compensate process variation is necessary. In order to save area and the number of control pins, the current reference should have trim-free feature.

- (2) The power regulator should have a stable output voltage that depends on the bandgap voltage reference generator. The bandgap voltage reference must have low TC across -40°C to 80°. It also should be a trim-free structure for saving in area.
- (3) To help the efficiency tracking method to function well, the input power should be tracked through high performance current sensor to monitor the input current across the 70-mA to 1-A load range as the supply voltage varies from 2.4 V to 3.2 V is needed.
- (4) The power transistor is the main contributor of power loss in the regulator. Its size and layout should all be carefully designed, for several tens of mA to 1-A load range, and across 2.4-V to 3.2-V supply voltage.
- (5) In order to eliminate shoot-through or body diode conduction of the power transistors, the dead-time between the two power transistors should be appropriately and carefully controlled to avoid any low impedance path between the supply and ground. In order to save power and area, a sensor less way of dead-time control is necessary to guarantee dead-time control accuracy over the 1-A load range, across the 2.4-V to 3.2-V supply voltage.

1.3 Contributions

This research aims to design an efficiency optimized power regulator, with focuses on the following aspects:

1. To generate a PVT compensated bias current for analogue blocks in power regulator. A 10- μ A trim-free current reference is proposed to generate the low accuracy bias for internal low dropout regulator (LDO). It has a less than 130 ppm/°C temperature coefficient (TC) across -40°C to 80°C temperature range. With supply voltage varying from 2.4 V to 3.2 V, the reference output current has a line regulation of less than 0.5%/V at room

temperature. Based on the proposed structure, the process variation was compensated, where silicon area was also reduced due to the absent of trimming resistor array. This allows the proposed structure to fit easily in commercial products.

To increase the line regulation on output voltage and clock frequency, a merged structure bandgap voltage reference and current reference (BGVCR) is proposed to guarantee the power regulator output voltage to be stable, and to give the clock generator a more accurate reference. Based on the proposed structure, the reference generator can function without requiring a start-up circuit and a trimming resistor array to save large amount of silicon area. Using a 1.8-V supply voltage that is derived from an internal low dropout regulator (LDO), the proposed BGVCR can generate a 1.1-V reference voltage with 5-ppm/°C TC and 9.8-μA reference current, with 150-ppm/°C TC across the -40°C to 80°C temperature range. Based on the proposed PTAT current sharing concept, the proposed BGVCR can adequately compensate for process variations to yield good performances without the trimming resistor array.

2. To attain the input current information for efficiency tracking, a full range enhanced self-bias current sensor can sense current at both the high side and low side switches within one switching cycle of the buck converter is proposed in this thesis. A better than 95% sensing accuracy is obtained. Its power consumption is less than 1% of the total input power for the entire power regulator.
3. The aspect ratio of the driver buffer has been optimized and a novel sensor-less threshold voltage prediction idea for adaptive dead-time control of the power transistor in power regulator is proposed in this thesis. Based on the proposed idea, the system has nearly no body-diode conduction at light load and a less than 3-ns body-diode conduction time at 1.1-A load. Without bringing in shoot-through current while minimizing switching loss, the adaptive dead-time control driver helps the system to achieve higher than 95% peak efficiency.

4. An adaptive efficiency optimized control method is proposed to adjust the size of the power transistor based on best efficiency. By implementing all the above mentioned control methods and building blocks, the proposed adaptive efficiency optimized power regulator (AEOPR) is able to attain optimized performance. Using the internal PVT compensated bias circuit, the AEOPR can compensate the PVT variation. With the help of the proposed adaptive dead-time control circuit, less than 5% of the power transistor area is used for the dead-time driver and less than 1% of total power is consumed by the adaptive dead-time driver to achieve a less than 3-ns body diode conduction which helps the AEOPR to attain a more than 95% peak efficiency. With internal bandgap voltage reference as error amplifier reference input, the system can achieve 1.2-V output voltage with less than 30 mV/A load regulation as the load current varies from 70 mA to 1.1 A. Also, the buck regulator has less than 1%/V line regulation across supply voltage varying from 2.4 V to 3.2 V. By adjusting the power transistor size according to the best efficiency point, more than 84% conversion efficiency is achieved over load range varying from 70 mA to 1.1 A at 2.4-V to 3.2-V supply voltage.

1.4 Organization of Thesis

This thesis consists of eight chapters and they are organized as follows: Chapter 2 reviews the bandgap voltage reference, current reference, current sensor, power MOS design, dead-time control technology, pulse width modulator (PWM), error amplifier design and compensation network design and wide load range efficiency power regulator; Chapter 3 overviews the system structure of the proposed adaptive efficiency optimized power regulator and also discussed the adopted conventional LDO for internal supply voltage and PWM generator; Chapter 4 describes the proposed bandgap voltage and current reference; Chapter 5 presents the design of the enhanced full range current sensor; Chapter 6 discusses the power MOS design and the new dead-time control driver design; Chapter 7 shows the efficiency tracker design and measurement result of the proposed adaptive efficiency optimized power regulator; Chapter 8 concludes this research and highlights some of the future work.

Chapter 2 Literature Review

Many methods have been proposed for wide load range DC-DC buck regulator. However, regardless of the types of the power regulator, their basic structure remains as depicted in Figure 2-1.

Figure 2-1 Conventional DC-DC buck regulator structure.

As seen in Figure 2-1, there are many building blocks in the buck power regulator: the bandgap reference (BGR), which is a reference generator to produce a PVT independent reference for the power regulator to attain stable output; the inductor L and capacitor C are for energy storage and usually external components due to their large size; the power transistors (M_P and M_N) are pass on transistors which contribute most in the power loss of the buck regulator; dead-time controller and driving buffers are used to generate control signal for the power regulator to control the power transistors avoiding shoot through, minimizing switching loss and body diode conduction loss; the R-S latch represents the control logic which controls the power regulator to do mode selection and power transistor size selection; the comparator (CMP) and the error amplifier (EA) combined to feedback the output voltage information to the input, and together with saw tooth generator generating a PWM signal for system controlling. Additionally, current sensor is usually needed to do adaptive efficiency control for the power regulator. The buck regulator system

will be based on the above blocks, optimizations and system control methods to achieve high efficiency and small ripple over wide load range. The literature review to be presented in this chapter will start from blocks level before discussing on the buck power regulator at system level.

2.1 Bandgap Voltage and Current Reference

2.1.1 Bandgap Voltage Reference

Bandgap reference (BGR) is one of the most critical building blocks in analogue and mixed-signal circuits such as the DC-DC converter, ADC, linear regulator and life-assist medical devices. The BGR's performance and power consumption can certainly have a huge impact on the performance of these circuits. To achieve low power consumption and wide temperature range, the availability of a low temperature coefficient BGR is crucial. Although several BGRs have been developed, most of them focused only on one aspect, which is to achieve low temperature coefficient or low power consumption or a wide temperature range. However, low temperature coefficient BGRs usually have large power consumption [12-17], and the low power consumption BGRs typically have poor temperature coefficient [18, 19] or small temperature range [14, 15, 18, 20].

A conventional amplifier based BGR is shown in Figure. 2-2(a). It includes both the PTAT and CTAT voltage generators. The PTAT voltage is defined as:

$$V_{PTAT} = \frac{R_2}{R_1} V_T \ln(N) \quad (2.1)$$

where N is the ratio between Q_1 and Q_2 , usually chosen to be 8; and V_T is the thermal voltage. The CTAT voltage is expressed as:

$$V_{CTAT} = V_{BE} \quad (2.2)$$

where V_{BE} is the base emitter voltage of the vertical BJT in standard CMOS process. Thus, the BGR output voltage is

$$V_{BGR} = \frac{R_2}{R_1} V_T \ln(N) + V_{BE} \quad (2.3)$$

Figure 1 consists of two circuit diagrams, (a) and (b), illustrating the proposed current mirror. Both circuits are powered by V_{DD} and have a reference voltage V_{BGR} . The input current is $PTAT$ and the output current is $CTAT$.

(a) This circuit includes an op-amp A_1 and a resistor R_1 . The input current $PTAT$ flows into the source of MP_1 . The gate of MP_1 is connected to V_{DD} . The source of MP_1 is connected to the non-inverting input of A_1 . The gate of MP_2 is connected to V_{DD} . The source of MP_2 is connected to the inverting input of A_1 . The output of A_1 is connected to the gate of MP_3 . The source of MP_3 is connected to V_{DD} . The drain of MP_3 is connected to V_{BGR} . The resistor R_1 is connected between the source of MP_1 and the source of Q_1 . The source of Q_1 is connected to ground. The gate of Q_1 is connected to the gate of Q_2 . The source of Q_2 is connected to ground. The drain of Q_2 is connected to $CTAT$.

(b) This circuit includes two NMOS transistors MN_1 and MN_2 and a resistor R_1 . The input current $PTAT$ flows into the source of MP_1 . The gate of MP_1 is connected to V_{DD} . The source of MP_1 is connected to the gate of MN_1 . The gate of MN_2 is connected to V_{DD} . The source of MN_2 is connected to the gate of MP_2 . The output of A_1 is connected to the gate of MP_3 . The source of MP_3 is connected to V_{DD} . The drain of MP_3 is connected to V_{BGR} . The resistor R_1 is connected between the source of MP_1 and the source of Q_1 . The source of Q_1 is connected to ground. The gate of Q_1 is connected to the gate of Q_2 . The source of Q_2 is connected to ground. The drain of Q_2 is connected to $CTAT$.

Thereafter, the high gain amplifier can be replaced by other structure. A novel structure that shaped the BGR without needing the high gain amplifier, i.e. the 4T BGR shown in Figure. 2-2(b), was reported in [20]. This BGR can save a huge amount of power by removing the high gain amplifier. However, its temperature coefficient is poor due to the limited gain of the 4T stage, causing the error between V_X and V_Y to be large. Ultimately, the generated PTAT current is not truly proportional to temperature.

Current reference is one of the most important building blocks for analogue circuits and mixed signal circuits such as ADC, power regulator and life-assist devices. As the current reference is providing bias condition for other analogue

circuits, it should have low temperature coefficient (TC) [21, 22], supply independent [23, 24] and process compensation properties [25, 26]. In order to save area and easy to be used, it should be trim-free [21]. However, it is difficult to have all these features in one single design. This is because most of the existing design are based on the two conventional current reference structures as shown in Figure 2-3.

Figure 2-3(a) shows a voltage to current topology. The compensation voltage generator was usually supplied by bandgap voltage reference, which is used to cancel the temperature coefficient of resistor R at the output current. This topology has two drawbacks: First, it needs high accuracy voltage reference, or else will suffer from supply variation; Second, this topology needs high gain amplifier which itself needs bias current. Thus, a current source must be designed first to bias the amplifier, which also can be affected by supply variation, temperature variation and process variation.

Figure 2-3(b) shows another topology for current reference generating. Conventionally, the proportional to absolute temperature (PTAT) current and complementary proportional to absolute temperature (CTAT) current are generated from different current sources, which usually suffers from process variation [21]. Thus, this kind of topology usually needs large amounts of trimming resistor to get zero TC point moving to the targeted value.

Figure 2-3 Conventional current reference: (a) voltage to current reference; (b) direct current reference.

Hence, a low TC, supply independent current source with process compensation feature is proposed in this thesis. Enhanced from the structure of Figure 2-3(b), this research presents a novel structure to generate the CTAT current and PTAT current from one current source, which thus compensates process variation. Hence, the proposed current reference can get targeted zero TC point without having the trimming resistor array.

2.2 Current Sensors

2.2.1 Types of Current Sensor

To ensure adaptive efficiency over a wide load range, the current information is very important for the power regulator so as to perform adaptive sizing or the control mode selection [27]. Different kinds of current sensing techniques have been proposed and they can be divided into four general categories: power MOS resistance [28], load current [29], inductor current [30, 31] and power MOS transistor [27, 32-37]. A brief overview for each of these methods are detailed as follows.

(1) The power MOS resistance sensing topology is realized by sensing the resistance of the power MOS that operates in the triode region and is assumed as a voltage-controlled switch. Its turn-on resistance can be approximated as follows:

$$R_{DS} = \frac{L}{W\mu C_{ox}(V_{GS} - V_{TH})} \quad (2.4)$$

where W and L are the channel width and length of the power MOS transistor, respectively; C_{ox} is the oxide capacitance for the gate-channel interface; V_{GS} is the voltage across the gate-source terminal of the transistor; V_{TH} is threshold voltage of the MOS transistor; and μ is the electron or hole mobility. This sensing topology is shown in Figure 2-4.

Figure 2-4 Power MOS R_{DS} sensing topology.

The merit of this topology is its distinctive lossless feature. However, its accuracy is not good. The sensing output can be calculated using the following equation:

$$V_{SENSE} = I_P R_{DS} \quad (2.5)$$

The selection of R_{DS} for the power transistor is determined by W , L , μ , C_{OX} and V_{TH} , whereas I_P is decided by the load. Therefore V_{SENSE} is affected by variations in W , L , μ , C_{OX} and V_{TH} , which are attributed to the process and temperature variation for up to 49% [28].

(2) The load current sensing topology requires a series resistor to be inserted between the load and inductor, whereby its structure is presented in Figure 2-5.

Figure 2-5 Load current sensing topology.

This topology will no doubt dissipate large amount of power if good accuracy is required. The sensing voltage can be calculated using the following equation:

$$V_{SENSE} = I_{SEN} R_{SENSE} \quad (2.6)$$

For this sensing topology, R_{SENSE} is to be determined and the value of I_{SEN} should be made equal to I_{LOAD} . R_{SENSE} is usually an external resistor with good accuracy and minimal temperature variation. Thus, this sensing topology should be much better as compared to the R_{DS} sensing topology. This topology however has one prominent drawback, that is, a good accuracy will bring about a large voltage drop across the sensing resistor. At the same time, a heavy load current will also result in a large voltage drop across the sensing resistor to ultimately degrade the power regulator efficiency.

(3) The Inductor current sensing topology shown in Figure 2-6 engages novel integrated circuit design techniques to sense the inductor current.

Figure 2-6 Inductor current sensing topology.

The equation for the sensing voltage can be expressed as:

$$V_{SENSE} = \frac{(R_L + sL)}{1 + sR_F C_F} R_L I_L \quad (2.7)$$

where R_L is resistance of inductor, I_L is inductor current, L is the inductance of the inductor, R_F is the resistance of the sensing resistor, and C_F is capacitance of the sensing capacitor. R_L is typically very small and unknown to the circuit designer. Hence, its sensing accuracy depends on the tolerance of the inductor value and the tuning accuracy of the filter. This topology is affected by temperature, and also the inductor manufacturing process, which may yield a

total tolerance change of 28% [29, 30]. Due to these drawbacks, an innovative self-learning idea was proposed in [31], which requires a large G_m -C filter that increases the silicon area overhead (nearly half of the chip area).

(4) The MOS current sensing topology make use of the current mirror to sense the current through the power MOS transistor. Its circuit is given in Figure 2-7.

Figure 2-7 Power MOS current sensing topology.

The power MOS transistor operates in the triode region and its current-voltage relation is simply the standard MOS transistor current equations:

$$I_P = \mu_p C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \quad (2.8)$$

where, W and L are the channel width and length of the power MOS transistor, respectively; C_{ox} is the oxide capacitance for the gate-channel interface; V_{GS} is the voltage across the gate-source terminal of the transistor; V_{TH} is threshold voltage of the MOS transistor; μ_p is the hole mobility and V_{DS} is drain to source voltage of the MOS transistor. In order for this topology to operate, a tracking loop should be added between the drain of power MOS transistor and the drain of the sensing MOS transistor, so as to force V_B to be equal to V_A . If the same channel length is used for the power and sensing MOS transistor, the current flowing through the power and sensing MOS transistor will obey the below current and transistor channel width relation:

$$\frac{I_P}{I_{PS}} = \frac{W_P}{W_{PS}} \quad (2.9)$$

I_P and I_{PS} are the current through the power and sensing MOS transistor, respectively; W_P and W_{PS} are the channel width of the power MOS M_P and the sensing MOS transistor, M_{PS} , respectively. This topology is lossless and yields good accuracy. Usually, the ratio of W_P/W_{PS} gives a large value of several thousand hence the current going through the sensing MOS transistor is minimal. Thus, the sensing voltage V_{SENSE} can be expressed as:

$$V_{SENSE} = I_P \frac{W_{PS}}{W_P} R_{SENSE} \quad (2.10)$$

Here, R_{SENSE} is the resistance of the sensing resistor. The accuracy of this sensing topology will not be affected by the process variation of the circuit and will only depend on the tolerance of the resistor, which can be as good as a 5% tolerance. Therefore, this topology offers both high accuracy and conversion efficiency. A summary on the different sensing topologies discussed is tabulated in Table 2-1.

Table 2-1 Comparison of different current sensing topologies

Sensing Topology	Accuracy tolerance	Δ Efficiency	Advantage	Disadvantage
MOS Resistance [28]	49%	<1%	Area Efficient, Lossless	Poor Accuracy
Load Current [29]	5-10%	4%	High Accuracy	Poor Power Efficient
Inductor Current [30, 31]	28%	Depend on topology	Lossless	Poor Accuracy & Large Silicon Area Overhead
MOS Current [27, 33-37]	5-10%	<1%	Area Efficient, Lossless, Good accuracy & Power Efficient	High Gain Amplifier Required

From Table 2-1, it can be deduced that the MOS sensing topology can achieve both high accuracy and best the efficiency. Thereafter, the current sensor to be designed in this research is based on the MOS current sensing topology.

2.2.2 Analysis of Existing Power MOS Current Sensor

Different on-chip MOS current sensors have been reported for the switching-mode power regulators. However, these on-chip current sensors cannot simultaneously achieve excellent sensing accuracy and concurrently allow the switching-mode power converters to operate at high frequency while consuming a very low amount of quiescent current. A Bi-CMOS is implemented in [32], whereby the accuracy of the current sensor depends solely on the voltage mirror realized by bipolar transistors. As Bi-CMOS technology is much more costly than normal CMOS process, it is not a cost-efficient power regulator design.

2.2.2.1 Power PMOS current sensor

A fully CMOS based power PMOS current sensor is proposed in [27] and its schematic is provided in Figure 2-8.

Figure 2-8 A high gain amplifier based current sensor [27].

A high gain amplifier is applied to nodes V_A and V_B , to create a negative feedback loop, forcing V_B to be equal to V_A . The two biasing currents I_1 and I_2 are very small. Thus, its effect on accuracy can be ignored. However, during light load condition, for example, if the load current is 50 mA, assuming that the sensing ratio N is 1000, bias current is 10 μ A, there will be an estimated

error of 20%. Therefore, this current sensor yields poor accuracy during light load condition. If the biasing current is not large, M_{B2} may not operate in the saturation region causing the load resistance of the feed-back loop to be not as high. As a result, the overall loop gain will reduce leading to errors in the current sensor network. Additionally, there are two V_{GS} voltage drops for M_{RS} and M_2 to work in the saturation region. Thus, the output swing of the high gain amplifier must be designed with due consideration to allow it to handle the two V_{GS} head room voltages. A two stage cascaded class AB amplifier is employed here, which will limit the supply voltage for this sensing technology. Therefore, it is unsuitable for modern low supply voltage applications which are the niche in many of the recent published research works.

Figure 2-9 A 1.2-V supply voltage current sensor [33].

A modified version is proposed in [33], whereby its corresponding schematic is shown in Figure 2-9. This circuit version has almost the same structure shown in [27]. Three NMOS transistors (M_1 , M_2 and M_{PS}) have been replaced by a single PMOS transistor. The amplifier and sensing output PMOS transistor form a negative feedback loop to force V_B to be equal to V_A . Thus, the current going through M_P and M_{PS} is $I_P/I_{PS} = N$ which resembles the former version

shown in [27]. By replacing the current sensor output stage from NMOS to PMOS and modifying the amplifier cascode structure, a 1.2-V supply voltage can be employed in this topology. However, the sensing accuracy and tracking speed for this topology have no doubt been sacrificed since the gain of the amplifier is greatly reduced. Also, the biasing current will have a great impact on the sensing accuracy which resembles closely to the former circuit version.

Figure 2-10 A 1-V supply voltage current sensor [34].

2.2.2.2 Power NMOS current sensor

Instead of PMOS current sensing, a NMOS current sensor is proposed in [34]. The circuit, as is depicted in Figure 2-10, has similar structure as that of Figure 2-9 [33], where it only modifies the circuit from PMOS to NMOS transistor sensing. In order to eliminate the undesirable effect of the large sensing resistance in relative to the turn on resistance of the MOS switch in the loop gain, an additional sensing resistor M_{RS2} is added to the output of the amplifier. This structure has an obvious drawback: the speed is limited by the unity-gain bandwidth (GBW) of the amplifier which will in turn be limited by the bias current. As a consequence, this will reduce the sensing accuracy to a large extent. This is because the design of a high speed amplifier requires a large amount of biasing current but this will result in more errors from the current sensor. Furthermore, large biasing current causes an increase in the overall quiescent power consumption especially for light load, which then degrade its efficiency drastically. Hence, a trade-off between speed, accuracy and power

consumption is inevitable. This creates a design bottleneck whereby the speed of this topology cannot be too high while concurrently achieving high accuracy.

To sense the full range current of the power regulator and to reduce the bias current affect, the bias current cancellation approach of Figure 2-11 is proposed in [35]. This current sensor employs a current cancellation transistor to compensate the quiescent biasing current. Although the bias current will flow through transistor M_{RS2} , it will be compensated by the current flowing through M_C which is the same amount as the biasing current, I_1 and I_2 . Hence the current through sensing resistor R_{SENSE} will be $1/N$ of the power MOS, without being affected by the error brought about by the biasing current. In this way, the speed of the current sensor is only limited by the biasing current and not affected by its sensing accuracy. In addition, this current sensor can sense the full range of inductor current. Both the PMOS and NMOS power transistors current sensors share the same current sensing core which do away with large number of transistors needed for full range current sensing. This topology creates a new milestone for sensing a full range of current. Although this current sensor is designed for boost converter, after modification, it can be applied to other converter topologies. The only limitation is that it requires a

biasing current that can achieve high speed during heavy load. But this proves to be power inefficient during light load as the biasing current will always consumes power.

Figure 2-12 A shunt feedback based current sensor [36].

A shunt feedback idea is proposed in [36], as is shown in Figure 2-12, which adds a shunt feedback to increase its speed and accuracy. For the PMOS current sensor, M_{SHP1-7} form a shunt feed-back loop between the drain of M_1 and M_2 which forces the drain voltage of M_{BP1} and M_{BP2} to be equal. Under these circumstances, even if the overall biasing current is very low, I_{BP1} and I_{BP2} can still be guaranteed to be equal. Hence, V_{PB} can track V_{PA} very closely. In this case, the accuracy of the current sensor will be increased to a great extent. For current sensing of power NMOS transistor, M_{SHN1-7} is used to form the shunt feed-back loop to force the drain voltages of M_{BN1} and M_{BN2} to be the same. This is similar to the operation of the current sensor for power PMOS transistor.

In addition, a duty ratio detector that can choose alternatively whether to sense the current in the PMOS or NMOS power transistor is engaged. This is because current sensor usually needs a longer time to be stable. The PMOS and NMOS current sensor are selected from a MUX which is to be decided by the duty ratio detector. This may give rise to other problems. Its power PMOS and NMOS current sensor are a simple combination of two different sensors. Therefore, many transistors are being used, which will occupy a larger silicon chip area. Two biasing current and one bias voltage are required in this design, which is again a lead to significant silicon area overhead.

Figure 2-13 A self-bias current sensor [37].

In order to achieve high speed during heavy load and also high efficiency during light load, the self-biased current sensor was proposed in [37]. The circuit, as illustrated in Figure 2-13 can sense a full range of inductor current in merely one switching cycle and can adjust its biasing current with a transiting from heavy to light load. However, this is only applicable to buck-boost converter, which merely requires it to sense the current in the power NMOS transistor to obtain the full range inductor current information, and it cannot be used directly for sensing the full range inductor current of a buck converter. The rationale here is that for a full range inductor current sensing of a buck converter, it is required to sense the current going through both power PMOS and NMOS transistor in the same cycle. Thus, an enhanced full range current sensor has been proposed in this thesis based on this topology for the buck regulator.

2.3 Power MOSFET

Power transistors are most important building blocks in the design of a power regulator. Its aspect ratio has large effect on turn on resistance and parasitic capacitance of power transistor which has very large impact on the power efficiency of the regulator. This is because power MOS transistor usually has a very large size in order to yield lower turn on resistance (R_{DS_ON}) which is shown in the below equations [38]:

$$R_{DS_ON_P} = \frac{1}{\mu_p C_{OX} \frac{W_P}{L} (|V_{GS_P}| - |V_{TH_P}|)} \quad (2.11)$$

$$R_{DS_ON_N} = \frac{1}{\mu_n C_{OX} \frac{W_N}{L} (V_{GS_N} - V_{TH_N})} \quad (2.12)$$

where $R_{DS_ON_P}$ and $R_{DS_ON_N}$ are the turn on resistance of power PMOS (M_P) and NMOS (M_N) transistors respectively, L is channel length for the power MOS transistor, μ_n and μ_p are the electron and hole mobility respectively. W_P and W_N are the channel width for M_P and M_N respectively, V_{GS_P} and V_{GS_N} are the gate control voltage for M_P and M_N respectively. V_{TH_P} and V_{TH_N} are the threshold voltage for M_P and M_N respectively. C_{OX} is the oxide capacitance per unit area. Thus, there will be power loss due to this turn on resistance which is widely known as conduction loss (P_{COND}) [39, 40]. Its equation is shown below:

$$P_{COND} = I_{LOAD}^2 (D \cdot R_{DS_ON_P} + (1-D)R_{DS_ON_N}) \quad (2.13)$$

where I_{LOAD} is the load current and D is switching duty cycle for the power regulator. As seen in the above equation (2.13), P_{COND} is dependent on the duty cycle of the control signal, load current, resistance of $R_{DS_ON_P}$ and $R_{DS_ON_N}$. The duty cycle of the control signal is decided by the output voltage to input voltage ratio which will vary with load changing. It can be seen from equation (2.11) and (2.12) that $R_{DS_ON_P}$ and $R_{DS_ON_N}$ are reduced with large aspect ratio by consume large silicon area. Also, M_P and M_N have different mobility, which means same turn on resistance for M_P and M_N will result in different chip areas. Thus, an optimization has to be done for all these considerations for the conduction loss. Furthermore, large aspect ratio of the power MOS will bring about large parasitic capacitance and significant charging and discharging loss

during the interval when the power MOS turns on, i.e. switching loss [41, 42] as expressed:

$$P_{SW} = (C_{GP} + C_{GN})V_{DD}^2 f \quad (2.14)$$

C_{GP} is gate capacitance of M_P , which can be calculated by $C_{GP} = C_{OX}W_PL$. C_{GN} is gate capacitance of M_N which can be calculated by $C_{GN} = C_{OX}W_NL$. and f refers to the switching frequency of M_P and M_N transistor [41].

Thus, both conduction and switching loss should be taken into consideration for the total loss, which can be simply expressed as:

$$P_{TOTAL} = P_{COND} + P_{SW} \quad (2.15)$$

According to equations (2.11) to (2.15), channel length should be small regardless of attempting to reduce conduction or switching loss. Hence, the minimized channel length for the process is chosen for the power MOS. Thereby, $0.18 \mu m$ is chosen as the channel length of the power MOS transistor in the $0.18 \mu m$ CMOS process.

However, channel width has different effect on P_{COND} and P_{SW} , and load current switching frequency must be taken into consideration, which is not easy to decide. Thus, load condition and switching frequency is fixed first, the relationship between channel width and power loss is shown in Figure 2-14.

Figure 2-14 Effect of power MOS channel width for conduction loss and switching loss.

With reference of Figure 2-14, the channel width for the power MOS can be optimized for a fixed load switching frequency. W_{OPT} in Figure 2-14 is the optimized power MOS channel width for such load condition. However, different load may have different optimized channel width. Hence, adaptive size is usually adopted for a wide load range power regulator application [39-41, 43]. Once the channel width is fixed, it can only have a single peak efficiency for a particular load [39] which can be observed in Figure 2-15.

Figure 2-15 Efficiency curves versus channel width.

With reference of Figure 2-15, conduction loss contributes more for heavy load whereas switching loss contributes more for light load. Thus, the channel width of power MOS should be carefully chosen according to load current and duty cycle of the control signal.

2.4 Dead-Time Control

Switching loss and power MOS conduction loss have been discussed in 2.3, However, the shoot through loss and body diode conduction loss must be carefully controlled, or else will bring large efficiency drop or even damage the power MOS. Hence, a dead time should be added during power MOS switching, which is shown in Figure 2-16.

Figure 2-16 Dead-time control diagram.

In Figure 2-16, V_{P_DRIVE} is the gate control signal for M_P ; V_{N_DRIVE} is gate control signal for M_N ; T_{DLY} is delay time between gate control signal for M_N and M_P which is the so called dead time. T_{DLY} must be optimized, if T_{DLY} is too small, M_P and M_N will turn on at the same time, a large shoot through current will be injected from power supply, which goes through M_P and M_N to ground. Such a large shoot through current will cause the efficiency of the power regulator to degrade tremendously or even damage M_P and M_N . However, if T_{DLY} is too large, body diode of M_N will conducting, which also waste large amount of power. Thus, the dead time should be optimized.

Many adaptive methods have been proposed to control the dead time. Most of them require very fast body diode conduction sensor to achieve fast respond time [44-46]. Some need high gain amplifier to get accurate dead time control, in order to get 1 ns resolution for the dead time control, the adaptive control circuit should have less than 1ns respond time, which is not easy to achieve [47-50]. In order to decrease these effects, a sampling and holding idea is proposed in [8], this idea can use low speed circuit to do fast speed control. furthermore, a sensor less idea is also proposed in [51], which can eliminate the high speed body diode conduction sensor, however, its control resolution is 20ns which is not. In order to get a finer control resolution, these adaptive control methods require small tapering factor to decrease additional delay caused by the inverter driver chain. The tapering factor should be as small as 3-30 to get aimed output rise time and fall time for the driver [52, 53]. Such large ratio will result in large area consumption for the driver, and number of driver stage should be large enough to drive large power MOS. In addition, the increased number of driver stages will cause large shoot-through power loss.

2.5 Pulse Width Modulation Control Signal

Pulse width modulation (PWM) control signal is commonly used in continuous conduction buck regulator for heavy load application [54-61]. This is because the PWM control method can help the CCM mode buck regulator to achieve high efficiency at heavy load. The PWM theory is illustrated in Figure 2-17.

Figure 2-17 PWM generator.

In addition to the input signal, a conventional PWM generator requires a saw-tooth signal as the other input for the comparator to generate a PWM control signal. The PWM control circuit comprises three parts: a ramp generator, an error amplifier and a compensation network. Each of these blocks are briefly described in the following sections.

2.5.1 Ramp Generator

A conventional ramp generator is shown in Figure 2-18 [27].

Figure 2-18 Ramp clock generator.

Here, the reference current and the capacitor value decide the slope of the rising speed of the ramp signal; V_H and V_L set the high side and low side of the ramp signal output, respectively; and the shorting switch M_{N1} defines the falling speed of the ramp signal. The negative SR latch output is the pulse clock that can be used as a PWM generator reset signal which will be discussed in the later chapter.

2.5.2 Error Amplifier

The error amplifier is one of the most important building blocks in switched mode power regulator, where its output signal will controls the duty cycle of the PWM output signal. Many high gain amplifier structure have been proposed [62-66]. Among these structure, the folded cascode is most favorable due to its high gain and without the need for stability compensation. A conventional folded cascode single ended amplifier is shown in Figure 2-19 [66].

Figure 2-19 Conventional folded cascode amplifier [66].

The folded cascode structure in [67] offers high gain, wide band width and low power consumption features. The downside of this structure is the high supply voltage required for a metric of the cascode load stage. Thus, the high swing cascode stage is usually applied for load stage as illustrated in Figure 2-20.

Figure 2-20 High swing cascode amplifier.

Both the input and output swings for this kind of cascode amplifier structure is increased. The challenge is about the four bias voltages design to ensure the amplifier works in active region. A new bias structure is therefore proposed in this thesis which will be shown in later chapter.

2.5.3 Compensation Network Design

The DC-DC buck regulator is a second order low pass filter system. The phase margin for the system must be compensated or else the error amplifier output will not be stable which will force the PWM block to generate variable duty cycle signal at a fast speed causing the system oscillate. Thus, some form of compensation is required. Several compensated methods have been proposed [67-69]. The most commonly adopted compensator is the type II (proportional-plus-integral—PI) and type III (proportional-integral-derivative—PID) compensator as described below.

2.5.3.1 Type II compensator

An ideal type II compensator is the invert zero system with the following transfer function:

$$H(s) = G_{\infty} \left(1 + \frac{\omega_L}{s}\right) \quad (2.16)$$

here, G_∞ is gain at high frequency and ω_L is corner frequency. The frequency response of the compensator is shown in Figure 2-21.

Figure 2-21 Frequency response of type II compensator: (a) gain response; (b) phase response.

As shown in Figure 2-21, the compensator increases the dc gain of the system, which helps the dc error approaches zero. However, the inverted zero is difficult to be accomplished in real application. In actual system, one more pole will be added in the system as shown in the circuit of Figure 2-22 .

Figure 2-22 Circuit for type II compensator.

The transfer function of the type II compensator shown in Figure 2-22 is given:

$$H(s) = \frac{s + \frac{1}{R_{C1}C_{C1}}}{R_{F1}C_{C2}s(s + \frac{1}{R_{C1}\frac{C_{C1}C_{C2}}{C_{C1} + C_{C2}}})} \quad (2.17)$$

From (2.17), it can be seen that there are two poles and one zero. This is a little different from the ideal type II compensator transfer function shown in (2.16). The frequency response of the circuit shown in Figure 2-22 is given in Figure 2-22.

Figure 2-23 Frequency response of real type II compensator: (a) gain response; (b) phase response.

Here, f_{P2} can be used to reduce the noise at the switching frequency of the power regulator. However, this kind of compensator is unable to increase the phase margin of the system. Hence, if the system phase margin is not high enough the type II compensator cannot fulfil the requirement. Thus, further enhancement must be incorporate to increase phase margin of the system.

2.5.3.2 Type III compensator

As discussed above, the type II compensator cannot fulfil the task of controlling the DC noise and improving the phase margin of the power regulator system. The type II compensator is therefore enhanced to type III compensator which is the PID compensator. Its transfer function is defined as:

$$H(s) = G_{CM} \frac{(1 + \frac{\omega_L}{s})(1 + \frac{s}{\omega_Z})}{(1 + \frac{\omega_{P1}}{s})(1 + \frac{\omega_{P2}}{s})} \quad (2.18)$$

As compared to (2.17), one zero is added to increase phase margin and one additional pole is also added to reduce the high frequency noise. A better appreciation can be inferred from Figure 2-24.

Figure 2-24 Frequency response of type III compensator: (a) gain response; (b) phase response.

The inverted zero at f_L provides the same function as the type II compensator, the added zero at f_Z provides a phase lead to increase phase margin, while the two poles at frequency f_{P1} and f_{P2} cause the gain to roll off at high frequency

and prevent the switching ripple from disrupting the operation of the pulse width modulator.

2.6 Wide Load Range Power Regulator

To fulfill the requirement discussed in Chapter 1, an adaptive efficiency method is needed for the wide load range application. As the power transistor is the dominator of the total loss in the power regulator, many methods had been proposed to control such loss of power in the power transistor.

The multimode control technology is one of the most useful control method to achieve adaptive efficiency over a wide load range [43, 70-72].

2.6.1 PFM Modulation

The pulse frequency modulation as described in Figure 2-25 is one the most important control method in power regulator design [73-79].

Figure 2-25 PFM mode control theory.

Similar to PWM control method, the PFM control method converts the control voltage to a switching frequency that is proportional to load current. The PFM control method can greatly improve the power efficiency at light load condition especially for a less than 1-mA load. This is for the reason that at light load condition, switching loss dominants the power loss in the power regulator. The PFM control method can control the switching frequency of the power regulator according to load current. At light load condition, the switching frequency of the power regulator will be lowered down, thereafter, the switching loss will be reduced as mentioned in section 2.3.

2.6.2 PWM/PFM Combine Mode Control

The pulse width modulation (PWM) exhibits good efficiency for heavy load but has poor efficiency for light load. This is due to the fact that the PWM control mode usually comes with excessive switching, gate drive, and quiescent current losses. Thus the combine mode control method is usually used for wide load range application. Thus, a PWM/PFM combined mode power regulator [80] has been proposed to achieve high efficiency over wide load range. The structure is shown in Figure 2-26.

Figure 2-26 PFM/PWM dual mode control method.

This design utilized the PFM mode to achieve high efficiency at light load and PWM mode to achieve high efficiency at heavy load, as illustrated in Figure 2-27.

Figure 2-27 Measured efficiency of the dual mode control method.

Other than operating in PFM mode, this design switches off all the unnecessary blocks to reduce power consumption. Thus, this design can achieve good efficiency at less than 200-mA load range. However, at higher than 200-mA load range the efficiency of the power regulator drops heavily and this may be attributed to the power transistor not being optimized and hence not being able to work well under heavy load condition. It can be seen from Figure 2-27 that there has an overlap region between 60 mA to 200 mA. The key is therefore to decide on the right mode transition at suitable juncture.

To increase the heavy load efficiency of the power regulator, a multi-phase combined with PWM/PFM dual mode controller is proposed in [81], as is shown in Figure 2-28.

Figure 2-28 A multi-phase multi-mode combined control method.

By applying the PFM mode at light load and multi-phase PWM controller at heavy load, this design can achieve nearly 90% efficiency at about 1-A load, as shown in Figure 2-29.

Figure 2-29 Measured efficiency of the multi-phase multi-mode combined control method.

From Figure 2-29 it can be seen that the power regulator can achieve high efficiency at load current larger than 1-A load, but it has only 91% peak efficiency implying the overall efficiency is a bit low. This is because of the many blocks in the multi-phase controller, which consume a lot of power. The multi-phase control scheme also increases the design complexity which calls for more attention on the stability of the system.

As discussed above, the pulse frequency modulation (PFM) control mode is more suitable for light load condition [82]; but it requires variable frequency which may post difficulties in designing the input filter for the following regulator as it needs sufficient attenuation over wider frequency range. Thus, the pulse skipping modulation was adopted to replace PFM in some cases [83].

In Figure 2-30, PFM (PSM) (region I) and PWM (region III) each yields high efficiency in the case of light load and heavy load, respectively. Hence, there exists an efficiency drop region (region II) between the two (see Figure 2-30), thereafter a third mode is needed to compensate the efficiency drop at the gap.

Figure 2-30 Different control mode comparison.

The digital off-time modulation (DOTM) control method is proposed in [84]. The DOTM is devised to increase the efficiency between the PFM mode and the PWM mode which structure is illustrated in Figure 2-31.

Figure 2-31 A DOTM based tri-mode control method.

This design combines the PFM, DOTM, PWM control methods to achieve high efficiency over a wide load range, and its efficiency is presented in Figure 2-32.

Figure 2-32 Measured efficiency of the tri-mode control method.

It can be seen from Figure 2-32 that quite a good efficiency has been achieved at light load condition. But at load current higher than 400 mA (which is important region for portable devices application) the efficiency is low. Also, this design requires a digital processor to achieve the control method which is not applicable in most commercial power regulator.

As discussed above, the multimode control method plays an important role in wide load range power regulator. However, it only performs well for application with load current at several mA or less than 1 mA. If the load current is higher than 100 mA, only PWM is necessary (see Figure 2-27, Figure 2-29, Figure 2-32). Furthermore, the multi-mode control method has one obvious drawback that is, the noise contribution of the power regulator will be large. This will increase the PSRR requirement for other circuits like the ADC, TDC, PLL, etc. in portable devices. Thus, based on the review above, the multimode control method is not a good choice for the intended portable devices application where the load demands for nearly 100 mA to 1A.

2.6.3 Adaptive Power Transistor Size Control Method

The multimode control method solves the switching loss by reducing the switching frequency, which can also be achieved by lowering the parasitic capacitance of the power transistor. Using fixed frequency, the adaptive power transistor size control method provides a better solution. As discussed in section 2.3 different load requires different power transistor size. At heavy load, larger transistor size is necessary to reduce the conduction loss, while at light load, small power transistor size is to be adopted to reduce the switching loss of the power transistor. If the power transistor is properly sized, even with fixed switching frequency is sufficient to attain good efficiency over a wide load range. Thus, the PWM control mode based adaptive power transistor size shown in Figure 2-33 is also widely adopted in wide load range application.

Figure 2-33 Adaptive power transistor control methodology.

As shown in Figure 2-33, the power transistor controller will adjust the power transistor size according to load requirement to achieve high efficiency over wide load range.

A V_{DS} sensing method is proposed in [85] to control the conduction loss with sensing structure is shown in Figure 2-34.

Figure 2-34 The V_{DS} based adaptive power transistor control method.

This design controls the segmented power transistor by comparing the V_{DS} voltage of the power transistor to a reference voltage; if V_{DS} is larger than the reference voltage, more transistors will be turned on. This design utilizes a sample sensing technology to control the power transistor according to the conduction loss. The efficiency of this design is shown in Figure 2-35.

Figure 2-35 Measured efficiency of the V_{DS} based adaptive power transistor control method.

It can be seen in Figure 2-35, that the efficiency is improved especially for heavy load. However, this idea does not consider the switching loss. The power transistor is also not optimized. It is thereafter a rough control approach and so,

the efficiency it achieved is not high. It is less than 90% as illustrated in Figure 2-35.

A more accurate control technology that can adjust the power transistor size by detecting the load current is widely used in [86, 87], which adjusts the power regulator size based on load current. As the structure is similar to above of the V_{DS} sensing technology, and their efficiency is not high, they will not be listed in detail here. [43] is a multi-mode adaptive power transistor size control which provides power transistor size adjusting combined with multi-mode control PFM, (dithering skip modulation) DSM, PWM, combined mode control. The topology of such structure is presented in Figure 2-36.

Figure 2-36 A multi-mode adaptive power transistor combined control method.

This design establish a linear relationship between the load current and the power transistor size with control code as described in Figure 2-37.

Figure 2-37 The linear relationship between power transistor size and load current.

As can be seen from Figure 2-37, the digital control word for the power transistor sizing is proportional to load current. This design is however, suitable only for fixed input voltage (3.3V) and output voltage (1.65V) application as the power transistor size is not really proportional to the load current while it is also affected by the supply voltage and output voltage. The multi-mode control method is only able to improve the efficiency at less than 100 mA load condition as can be seen in Figure 2-38.

Figure 2-38 Measured efficiency of the multi-mode adaptive power transistor combined control method.

It can be seen from the efficiency curve that this design achieves higher than 90% efficiency at light load condition by applying the combined mode control method. But when the load current is higher than 500mA, the efficiency drops heavily which proves that the linear relationship established by this design is not suitable for heavy load. And furthermore, this design only converts 3.3 V voltage to 1.65 V which is not suitable for most applications. The dithering skip method also generate dithering noise to the converter output, which makes the noise even more difficult to be controlled.

Thereafter, a look up table idea is proposed in [88-90], where the transistor size is calculated based on an assumed load condition. This idea enables the power transistor to be optimized for the load current, however, during fabrication, the process variation will cause the power transistor to be unsuitable for the assumed load condition. Also when the supply voltage changes, such kind of idea also cannot predict the best power transistor size. Thus, an adaptive efficiency control method that can size the power transistor based on best efficiency point which suitable for the varied supply voltage wide load current application of portable devices is proposed in this thesis.

Chapter 3 System Structure Overview of The Proposed Power Regulator

As discussed in Chapter 2, the adaptive size PWM mode power regulator is the best choice for reducing the switching loss and conduction loss while controlling the noise spectrum in fixed frequency range. In conventional adaptive power MOS size control method, only the load current is used as the control information for deciding the power MOS size. This kind of control methodology only functions well for fixed supply voltage. When the supply voltage is varying, the best efficiency point will no longer depend solely on load current. In battery operated system, the supply voltage is always not fixed. Hence, the conventional load current based control method is not suitable for such application. An adaptive efficiency optimized power regulator (AEOPR) is hence presented in this chapter. Based on the proposed efficiency tracking method, the power regulator will adjust its power MOS size based on the efficiency of the power regulator instead of relying on the load current. The power MOS size will be selected based on the best efficiency point for different load and supply voltage. The proposed AEOPR which includes all the building blocks, is fabricated in standard 0.18- μm CMOS process, occupying an area of 2 mm x 2 mm. With a supply ranging from 2.4 V to 3.2 V, the presented AEOPR can work with load current varying from 70 mA to 1.1 A at 1.2-V output voltage, achieving more than 95% peak efficiency. The proposed AEOPR is a PWM controlled buck regulator, and its system structure is shown in Figure 3-1.

Figure 3-1 System structure of proposed AEOPR.

In order to save power, and guarantee the performance of the system, the optimized efficiency power regulator must be optimized from system level down to every individual building block. All the critical building blocks are work at 1.8-V internal supply voltage that is generated by a conventional LDO and will be discussed in section 3.1. To guarantee the stability of the power regulator, the PID compensation was added to the PWM control loop to assist the system in achieving more than 50° phase margin which will be analyzed 3.2.

The BGR block and the bias current generator will be discussed in Chapter 4. The current sensor which is used to track the input power for the efficiency optimize control will be analyzed in Chapter 5. The M_{N1-M} and M_{P1-M} are power NMOS and PMOS transistor arrays, respectively, whereby the design considerations will be discussed in section 6.1. The dead-time control driver has been analyzed in sub-section 6.2.2. The efficiency tracker which utilizes the current sensor input information, to control the size of the power transistor, allow it to work at the best efficiency point will be discussed in Chapter 7. The system experimental results will also be provided in Chapter 7, to substantiate the performance of the proposed AEOPR.

3.1 LDO Design

The input voltage for the AEOPR ranges from 2.4 V to 3.2 V. This variable supply voltage is not suitable for the internal error amplifier, comparator and some digital blocks. Since most of these circuits deploy the 1.8-V transistor, and so a supply voltage of 1.8 V will be more appropriate. With that, a low dropout regulator (LDO) is needed to convert the input voltage to 1.8-V serving as the internal supply voltage. A conventional LDO is engaged in this proposed structure as shown in Figure 3-2.

Figure 3-2 The utilized LDO structure.

Here, M_P utilized the power transistor which will be discussed in section 6.1. The error amplifier, resistors, R_{F1} and R_{F2} , together with transistor M_P forms a negative feedback loop providing an output voltage of:

$$V_{LOAD} = \frac{R_{F1} + R_{F2}}{R_{F1}} V_{REF} \quad (3.1)$$

here, V_{LOAD} is output voltage and V_{REF} is the reference voltage derived from the BGR discussed in Chapter 4. The simulation results of the LDO output is given in Figure 3-3.

Figure 3-3 LDO output voltage vs load current.

As illustrated in Figure 3-3, the LDO output voltage is independent of the load current. It is proportional to the supply voltage, with a line regulation at about 2%/V. The testing result of LDO is shown in Figure 3-4.

Figure 3-4 LDO measurement results.

It can be seen in Figure 3-4 that the line regulation of the LDO is 2%/V, and the variation between simulation and testing result is less than 3%, which is stable enough for internal circuit to function well when supply voltage varied from 2.4 V to 3.

3.2 PWM Generator

The pulse width modulation (PWM) control method is important in switch mode power regulator. As shown in Figure 3-1, the output sensing resistor,

BGR, error amplifier (EA), comparator, RS latch and ramp clock generator, form the PWM generator.

Here, the ramp signal and clock pulse clock signal are both generated from the same ramp clock generator to ensure the same switching frequency. The RS latch is a standard cell and the BGR generator will be discussed in Chapter 4. The following subsections describes the PWM control circuit in three separate blocks: Ramp clock generator, error amplifier and the compensation network design.

3.2.1 Ramp Clock Generator

The ramp generator controls the switching frequency of the power regulator, and so having a stable frequency is very important, as depicted in 2.5.1. The fully integrated ramp clock generator of Figure 3-5 is utilized as clock generator for the buck power regulator.

Figure 3-5 Ramp generator with real bias.

The bias current of the ramp generator is mirrored from the current reference proposed in section 4.2. On-chip MIM capacitor is engaged in this design, where the capacitance is proportional to its area. In order to conserve area for the capacitor, the bias current of the ramp clock generator is set to $1\mu\text{A}$. The simulation result of the ramp clock generator is shown in Figure 3-6.

Figure 3-6 Ramp clock generator simulation result.

It can be seen in Figure 3-6 that a 1.2-MHz clock is generated and the ramp signal has a 1.1-V peak value.

3.2.2 Error Amplifier Design

Error amplifier is one the most important circuit blocks in power regulator design. Its performance affects the power regulator through the PWM control signal in the power regulator. Thus, high gain high band width error amplifier is usually needed to assist the power regulator in achieving the required performance. As discussed in sub-section 2.5.2, the folded cascode amplifier is adopted as the error amplifier. As the supply voltage for the error amplifier is 1.8 V, high swing cascode structure must be applied to guarantee the folded cascode amplifier performs well in such low supply voltage. Designing a bias circuit for the high swing cascode amplifier is a challenge. The conventional approach uses a two-branch high swing cascode structure which brings more offset error and consumes more power. A new bias circuit structure is hence proposed to bias the high gain folded cascode error amplifier as shown in Figure 3-7.

Figure 3-7 Proposed high swing cascode amplifier.

The I_{BIAS} shown in Figure 3-7 is generated from the 10- μ A current reference as illustrated in sub-section 4.2.2. The transistors MP_A and MP_B form the input stage of the folded cascode amplifier; MP_{8-11} and MN_{8-11} form the folded cascode load stage; MP_{1-5} and MN_{1-7} serve as the bias stage while MP_{6-7} provides the tail current of the amplifier. Unlike the conventional way in generating the bias voltage for the high swing cascode structure, a new complementary bias structure is proposed in this sub-section. The transistor MP_2 works in the saturation region to provide two over-drive voltage (V_{ov}) plus a threshold voltage for transistor MN_2 to be biased in the saturation region. In order to guarantee MN_2 functions in the deep saturation region, the W/L for MP_2 is usually chosen small value to generate more voltage drop. Transistor MN_1 and MP_1 are for process compensation. In normal condition, MN_1 turns off and MP_1 is forced to saturation region which voltage drop is usually small. But, in a PMOS slow, NMOS fast condition, PMOS transistor threshold voltage is increased. Thus, the voltage drop across MP_1 and MP_2 will be larger than threshold voltage of MN_1 to turn on MN_1 . Both MP_1 and MP_2 will be forced to triode region where both will function as resistors to cause transistor MN_2 be biased in the saturation region. For transistor MN_{4-5} and MP_5 , similar analysis can be amend out to demonstrate that they provide the bias voltage for transistor MP_4 .

Based on the proposed complementary bias circuit for the high swing folded cascode amplifier, the bias input current is conserved by 20 %, and the performance of the amplifier was also enhanced, as illustrated in Figure 3-8.

Figure 3-8 Frequency response of the folded cascode amplifier.

It can be seen that with a 10- μ A bias current, more than 90 dB dc gain has been achieved and the unit gain band width is about 2.6 MHz, with a 86 degree phase margin. This fulfil the requirement of the error amplifier for buck power regulator with high gain and low power features.

3.2.3 Compensation Network Design

The compensation network affects the stability of the power regulator through the PWM generator control signal as illustrated in sub-section 2.5.3. The buck power regulator shown in Figure 2-1 is a second order system, which transfer function :

$$H(s) = \frac{1}{1 + s\frac{R}{L} + s^2LC} \quad (3.2)$$

where, R is load resistance, L is inductor and C is load capacitor. After rearranging:

$$H(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \quad (3.3)$$

here, $Q = R\sqrt{\frac{C}{L}}$ is the quality factor, $\omega_0 = \frac{1}{\sqrt{LC}}$ is defined as the corner frequency of the second order system. When Q is larger than 0.5, it will become a complex pole system, with frequency response as shown in Figure 3-9.

Figure 3-9 Frequency response of the buck regulator: (a) gain response; (b) phase response.

Here, $f_0 = \frac{\omega_0}{2\pi}$ is the buck regulator corner frequency. The phase shift speed is proportional to Q . This means that the higher Q factor, the smaller phase margin the system will have. The frequency response for the LC low pass filter is depicted in Figure 3-10.

Figure 3-10 Frequency response of the LC low pass filter.

As can be seen in Figure 3-10, the phase shift at corner frequency is 180° , which will cause the system to oscillate. At the switching frequency of the power regulator, there exists a non-dominant zero, which is generated from the equivalent series resistance of the load capacitor. This high frequency zero will lower the gain to decrease the circuit speed. This increases circuit noise at the switching frequency of the power regulator. Thus, a type III compensator is needed to increase the phase margin when lowering the DC and switching frequency noise. The circuit structure is given in Figure 3-11.

Figure 3-11 Adopted type III compensator.

In Figure 3-11, R_{C1} , C_{C1} forms the dominant zero Z_1 ; R_{F1} , R_{C2} , C_{C2} constitute the second zero Z_2 ; R_{C2} , C_{C2} forms the first non-zero pole P_1 and R_{C1} , C_{C1} , C_{C3} forms the second non-zero value pole P_2 . Thus, the transfer function of the adopted compensator is:

$$H(s) = \frac{R_{C2} + R_{F1}}{R_{C2}R_{F1}C_{C3}} \frac{(s + \frac{1}{R_{C1}C_{C1}})(s + \frac{1}{(R_{C2} + R_{F1})C_{C2}})}{s(s + \frac{1}{R_{C1}\frac{C_{C1}C_{C3}}{C_{C1} + C_{C3}}})(s + \frac{1}{R_{C2}C_{C2}})} \quad (3.4)$$

As discussed in sub-section 2.5.3.2, the dominant zero Z_1 is inserted at $\frac{1}{2}f_0$ and the second zero Z_2 is inserted at f_0 . The non-zero pole P_1 is inserted at half switching frequency of the power regulator, and non-zero pole P_2 is inserted at the frequency of zero generated by the parasitic resistor (f_{ESR}). The frequency response of the compensator is given in Figure 3-12.

Figure 3-12 Frequency response of the adopted compensation network.

From Figure 3-12 one can notice a 230° phase shift is realized by the compensation network at the corner frequency of f_0 . Thus, the -180° phase shift at the corner frequency will be changed to 50° as shown in Figure 3-13.

Figure 3-13 Frequency response of the power regulator system after compensation.

As seen in Figure 3-13, the phase shift of the LC low pass filter is boosted to 140° at the corner frequency, and at unit gain frequency point, the phase shift is 50° , which means the system has now attained a 50° phase margin. At the switching frequency, the gain decreases at 40 dB/decade, and the gain at the switching frequency is about -60 dB which is sufficiently strong to suppress the noise at switching frequency.

Chapter 4 Bandgap Voltage and Current reference

Bandgap voltage current reference and current reference are important building blocks that set the DC operating point of the power regulator. A Low TC current reference, a bandgap voltage current reference and a low power bandgap voltage reference are proposed and described in this chapter.

4.1 Temperature Independent Current Reference

To guarantee the analog blocks of the regulator system to have stable performance, a PVT independent current reference is necessary for bias current generating. This sub-chapter presents a 10- μ A, trim-free, low temperature coefficient, supply independent current reference with process compensation feature. Based on the proposed structure, a 130 ppm/ $^{\circ}$ C temperature coefficient current reference across -40° C to 80° C temperature range is achieved. The proposed circuit can work at supply voltage varying from 2.4 to 3.2 V, while only has 30-nA drift at room temperature. The proposed current reference is implemented in the proposed AEOPR occupying an area of 0.005 mm².

4.1.1 Circuit Design

The proposed current reference is based on the self-biased current source structure[66]. This self-biased structure does not need high gain amplifier to generate the current source. It therefore consumes a smaller area and power compared to amplifier based current source. However, this current source is thermal voltage based, which is proportional to temperature. In fact this is only a PTAT current source. In order to get zero TC current reference, A CTAT current generator is needed to compensate the temperature coefficient of thermal voltage. Usually, base-emitter voltage (V_{BE}) is used as CTAT voltage source to generate the CTAT current to compensate the temperature coefficient of the thermal voltage. However, as discussed above, if additional V_{BE} based CTAT voltage generator is added to generate the CTAT voltage, process variation will affect the current reference output. But, in fact, the PTAT current source includes CTAT voltage source already. If this CTAT voltage is utilized, process variation will be eliminated, because the PTAT voltage and CTAT

voltage are generated from the same source. Thus, a novel structure is proposed in this paper as shown in Figure 4-1 (start-up is not shown).

Figure 4-1 Proposed current reference.

Here, MP_{1-6} , MN_{1-2} , Q_{1-2} and R_1 forms the PTAT current generator as illustrated in Figure 4-2, which is generated from a PTAT voltage divided by a resistor. MP_{1-4} and MN_{1-2} forms a negative feed-back loop to force voltage V_X to track voltage V_Y . In order to let voltage V_X equal to V_Y , the same W/L is chosen for MP_{1-4} , and the same is applied to MN_{1-2} .

Figure 4-2 Equivalent PTAT current generator.

Thus, the PTAT voltage is generated from the difference of V_{BE2} and V_{BE1} , which is

$$V_{PTAT} = \Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln(N) \quad (4.1)$$

where, V_{BE2} and V_{BE1} are base emitter voltage of the parasitic BJT transistor Q_2 and Q_1 , N is the size ratio between Q_2 and Q_1 and V_T is the thermal voltage. Hence, the PTAT current is:

$$I_{PTAT} = \frac{V_{PTAT}}{R_1} = \frac{V_T \ln(N)}{R_1} \quad (4.2)$$

MP_{3-4} , MP_{7-10} , MN_{2-3} , and R_2 forms the CTAT current generator as shown in Figure 4-3. Here, MP_3 and MP_9 are in the same bias condition, while MP_4 and MP_{10} in the same bias condition. Gates of MN_2 and MN_3 are connected together. If we choose the same W/L for MP_{3-4} , MP_{9-10} and MN_{2-3} respectively, voltage V_Z will equal to V_Y . Thus, the CTAT voltage V_{BE2} will be mirrored to resistor R_2 , and hence the CTAT current is:

$$I_{CTAT} = \frac{V_{CTAT}}{R_2} = \frac{V_{BE2}}{R_2} \quad (4.3)$$

The PTAT current and CTAT current are mirrored by MP₅₋₆ and MP₇₋₈ separately and are summed as I_{REF} , which is:

$$I_{REF} = I_{PTAT} + I_{CTAT} = \frac{V_T \ln(N)}{R_1} + \frac{V_{BE2}}{R_2} \quad (4.4)$$

Figure 4-3 Equivalent CTAT current generator.

The temperature coefficient for the reference current is:

$$TC = \frac{\partial I_{REF}}{\partial T} = \frac{\partial(\frac{V_T \ln(N)}{R_1})}{\partial T} + \frac{\partial(\frac{V_{BE2}}{R_2})}{\partial T} \quad (4.5)$$

The zero TC point is decided by:

$$\frac{\partial(\frac{V_T \ln(N)}{R_1})}{\partial T} + \frac{\partial(\frac{V_{BE2}}{R_2})}{\partial T} = 0 \quad (4.6)$$

In conventional way, when there has process variation, the zero TC point will be varied, which usually needs trimming resistor array to do compensation. However, in the proposed current reference structure, the process variation has been compensated internally. As shown in Figure 4-1, the PTAT and CTAT current are generated from the same current source. Assuming there has process

variation of α for BJT transistor, and β for resistor, the PTAT current will be changed to:

$$I_{PTAT1} = \frac{(1+\alpha)(V_{BE2} - V_{BE1})}{(1+\beta)R_1} = \frac{(1+\alpha)V_T \ln(N)}{(1+\beta)R_1} \quad (4.7)$$

the CTAT current will be changed to:

$$I_{CTAT} = \frac{V_{CTAT}}{R_2} = \frac{(1+\alpha)V_{BE2}}{(1+\beta)R_2} \quad (4.8)$$

the current reference output will be:

$$I_{REF} = I_{PTAT} + I_{CTAT} = \left(\frac{1+\alpha}{1+\beta}\right) \left(\frac{V_T \ln(N)}{R_1} + \frac{V_{BE2}}{R_2}\right) \quad (4.9)$$

the temperature coefficient will be:

$$TC1 = \frac{\partial I_{REF1}}{\partial T} = \left(\frac{1+\alpha}{1+\beta}\right) \left(\frac{\partial(\frac{V_T \ln(N)}{R_1})}{\partial T} + \frac{\partial(\frac{V_{BE2}}{R_2})}{\partial T}\right) \quad (4.10)$$

the zero TC is thus decided by

$$\frac{\partial I_{REF1}}{\partial T} = \left(\frac{1+\alpha}{1+\beta}\right) \left(\frac{\partial(\frac{V_T \ln(N)}{R_1})}{\partial T} + \frac{\partial(\frac{V_{BE2}}{R_2})}{\partial T}\right) = 0 \quad (4.11)$$

See from (4.7) – (4.11), it is easy to understand that the process variation will only affects the current value, but not the zero TC point. Thereafter, the proposed current reference is trim-free which can save large area for the trimming resistor. Also, this helps the proposed design more flexible to be applied in commercial electronics circuit design.

Furthermore, as shown in (4.4), the proposed current reference is decided by V_T and V_{BE} voltage, which is thus supply independent.

4.1.2 Experimental Results

The proposed structure was implemented in the proposed power regulator as bias current generator, which takes an area of $100 \mu\text{m} \times 50 \mu\text{m}$. The micrograph for the proposed current reference is shown in Figure 4-4.

Figure 4-4 Micrograph of the proposed current reference.

In order to guarantee the performance of the proposed current reference, the effect of mismatch was studied through Monte-Carlo simulation with 200 runs. The supply voltage was set at 2.4 V and 3.2 V and the simulation results are presented in Figure 4-5.

(a)

(b)

Figure 4-5 Monte-Carlo simulation of the proposed current source: (a) simulation results at 2.4V supply voltage; (b) simulation results at 3.2-V supply voltage.

As shown in the Monte-Carlo simulation results, the 3σ variation of the current reference is about $0.6 \mu\text{A}$, which is about 6% variation of the $10 \mu\text{A}$ current reference output. The circuit biased by the current reference is designed to have 20% tolerance of the bias current, which means the proposed current reference can have 14% margin even with the 3σ variation of mismatch.

The 2.4-V to 3.2-V supply voltage is applied to the testing chip, with temperature varying from -40°C to 80°C . The measurement results are given in Figure 4-6.

Figure 4-6 Measurement results of the proposed current source.

Seen as in Figure 4-6, the proposed current reference is able to generate 10 μA current reference with less than 4% error and less than 130 ppm/ $^{\circ}\text{C}$ across a temperature range of -40°C to 80°C without trimming at 3.2-V supply voltage. This proves that the proposed process compensation method can absorb the process variation to maintain the zero TC point.

With supply voltage varying from 2.4 V to 3.2 V, the proposed current reference exhibits a less than 0.5%/V line regulation at room temperature, and has less than 1%/V line regulation across -20°C to 80°C temperature range as illustrated in Figure 4-6. At -40°C , the proposed current reference does not function well. This is because at low temperature, the threshold voltage of the MOS transistor is increased by about 20%. At 2.4-V supply voltage, transistor MP_{1-10} was pushed to the boundary at between the saturation and triode regions. Even though, the error of the current reference is 12% which can still be tolerated in providing the bias current for most cases as most circuits are designed to tolerate 20% bias variation.

As can be seen from both the Monte-Carlo simulation and measurement results, the current reference can work without a bias trimming circuit, where it is able to maintain the variation of less than 6 %. This is much lower than the variation tolerance of the circuit that is biased by the proposed current reference.

A comparison between the proposed current reference and some existing design is shown in Table1. It shows that the proposed current reference can work at wide temperature range, have low temperature coefficient, can compensate process variation without trimming resistor array and is also supply independent.

Table 4-1 Summary of some existing design

	[21]	[25]	[23]	[26]	[24]	This Work
CMOS Technology (μm)	0.18	0.18	0.5	0.35	0.35	0.18
Supply Voltage (V)	1 – 1.2	1	2.3 – 3.3	5	1.8-3.0	2.4-3.0
Output Current (μA)	$7.81 \pm 4.5\%$	$144 \pm 7\%$	16-53	$0.001 - 0.05$	0.1	$10 \pm 1.4\%$
Temperature Range ($^{\circ}\text{C}$)	0 – 100	0 – 100	0 – 80	0 – 80	0 – 80	-40 – 80
TC (ppm/ $^{\circ}\text{C}$)	24.9	185	132	250	600	130
Normalized Current Consumption ^a	0.12 X	0.5 X	2 X	225 X	5 X	2 X
Line Regulation (%/V)	100	N.A.	1	N.A.	0.2	0.5
Area (mm^2)	0.023	0.07	0.06	0.006^b	0.015	0.005
Trimming	No	Multi-temp.	Multi-temp.	Multi-temp.	No	No

^a Normalized current consumption is the current consumption divided by the reference output current .

^b Bias was gotten from outside of the chip.

4.1.3 Summary

The proposed current reference can generate a $10\text{-}\mu\text{A}$ reference current, with 4% accuracy. With supply voltage varying from 2.4 V to 3.2 V, the reference output current has a line regulation of less than $0.5\%/V$ at room temperature. Based on the proposed structure, process variation was compensated, which saves large area for trimming resistor array and this helps the proposed structure easy to be fitted in commercial products. And less than $130\text{ ppm}/^{\circ}\text{C}$ TC has been achieved across $-40^{\circ}\text{C} - 80^{\circ}\text{C}$ temperature range at 3.2-V supply voltage.

4.2 Start-Up Free Merged Bandgap Voltage Current Reference

To guarantee a stable output voltage of the power regulator, a stable BGR and current reference for the clock generator is necessary. This section presents a novel merged structure to function both as a BGR and a temperature independent current reference. The proportional to absolute temperature (PTAT)

current sharing approach we proposed allows amalgamation of the bandgap voltage and current reference in the same structure without them affecting each other's performance. PTAT sharing helps to compensate the process variation in the proposed circuit, thus doing away with the trimming resistor array. The proposed structure deployed a local feedback loop together with parasitic capacitor to achieve self-start-up thereby eliminating the need for a start-up circuit. The gain of the voltage tracking loop for generating the proportional to absolute temperature current is also boosted. The proposed compact voltage current reference attained 5 ppm/°C temperature coefficient for bandgap voltage reference and 150 ppm/°C temperature coefficient for the current reference across -40°C to 80°C temperature range at 1.8-V supply voltage. The proposed design is implemented in the proposed AEOPR with a chip area of 0.006 mm².

The proposed BGVCR depicted in Figure 4-7 is a dual structure for bandgap voltage and current reference circuit. The voltage reference and current reference share the same PTAT current generator. The analysis of the proposed BGVCR can be divided into four parts: current reference generating, bandgap voltage reference generating, start-up free approach and self-bias method.

Figure 4-7 Proposed start-up free bandgap voltage current reference.

In order to generate a temperature independent current reference, both PTAT current source and CTAT current source are needed to perform temperature compensation for the current reference output. The equivalent circuit for generating the current reference is shown in Figure 4-8.

Figure 4-8 Equivalent circuit for generating current reference.

Here, MP₅₋₁₀, MN₂₋₃, R₂ and Q₁₋₂ form the PTAT current generator. MP₇₋₁₀ and MN₁₋₂ create a negative feed-back loop to force voltage V_Y equal to V_X. Thereafter, a PTAT voltage (V_{PTAT}) is generated from the voltage difference between the base-emitter voltage of Q₁ and Q₂, i.e.

$$V_{PTAT} = \Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln(N) \quad (4.12)$$

where V_{BE1} and V_{BE2} are the base-emitter voltages of parasitic BJT transistors, Q_1 and Q_2 , N is the size ratio between Q_2 and Q_1 , and V_T is the thermal voltage. Thus, the PTAT current (I_{PTAT}) is

$$I_{PTAT} = \frac{V_{PTAT}}{R_\gamma} = \frac{V_T \ln(N)}{R_\gamma} \quad (4.13)$$

MP₁₋₄, MP₉₋₁₀, MN₁, MN₃ and R₁ form the CTAT current generator. MP₁₋₂ and MP₇₋₁₀ are chosen to have the same W/L to guarantee the same bias condition for MP₁ and MP₉ as well as for MP₂ and MP₁₀. MN₁ and MN₃ are connected together. If the two transistors have the same W/L , V_Z and V_Y will have the

same voltage, which allow the CTAT voltage generated from the base-emitter of Q_2 to be mirrored to resistor R_1 , and thus be converted to the CTAT current I_{CTAT} , where

$$I_{CTAT} = \frac{V_{CTAT}}{R_1} = \frac{V_{BE2}}{R_1} \quad (4.14)$$

The PTAT and CTAT currents are mirrored by MP₅₋₆ and MP₃₋₄, respectively. They are added as current reference output I_{REF}

$$I_{REF} = I_{PTAT} + I_{CTAT} = \frac{V_T \ln(N)}{R_2} + \frac{V_{BE2}}{R_1} \quad (4.15)$$

The PTAT and CTAT current sources share the same CTAT voltage source. The zero TC point is therefore not affected by process variation; only the output current value will be affected. As shown in (4.15) the output current is decided by V_T , V_{BE2} , R_1 and R_2 , and hence independent of the supply voltage.

4.2.3 Bandgap Voltage Reference

The bandgap voltage reference is a summation of the PTAT voltage and CTAT voltage to compensate temperature variation as shown in Figure 4-9.

Figure 4-9 Equivalent circuit for generating voltage reference.

The PTAT voltage is generated from a PTAT current times the resistor that shares the PTAT current source with the current reference. The PTAT current is mirrored by MP₁₁₋₁₂ and flows through R₃ to generate the PTAT voltage (V_{PTAT2})

$$V_{PTAT2} = I_{PTAT} R_3 = \frac{R_3 V_T \ln(N)}{R_2} \quad (4.16)$$

The CTAT voltage is generated from a parasitic BJT transistor Q₃, i.e., V_{BE3} . Thus, the bandgap voltage reference output (V_{REF}) is

$$V_{REF} = V_{PTAT2} + V_{BE3} = \frac{R_3 V_T \ln(N)}{R_2} + V_{BE3} \quad (4.17)$$

It can be seen from (4.17) that the bandgap voltage reference only relates to the ratio of resistor R₃ to R₂ and the base-emitter voltage of the parasitic BJT transistor Q₃. This means that resistor drift due to process variation can be eliminated from the bandgap voltage reference output. When process variation happens, all the BJT transistors will be affected in the same manner but the zero TC point will not be affected. The change is only on the reference output value. The current reference and bandgap reference voltage share the same PTAT current generator, which saves both silicon area and power consumption in the proposed merged structure BGVCr. Conversion from one to another is also not required as the two are separately generated. Thus, they will not affect each other's performance like the conventional design.

4.2.4 Start-Up Free Approach

Start-up circuits are usually required in conventional bandgap voltage and current reference circuit, causing large silicon area and power consumption. Our proposed BGVCr resolves these concerns by being able to self-start-up. In Figure 4-10(a), the parasitic capacitances involved during BGVCr start-up are analyzed. C_{GS1}, C_{DS1}, C_{GS2}, C_{DS2}, C_{GS3}, C_{DS3} are the parasitic capacitances of transistor MP₇, MP₈ and MN₂, respectively. During the start-up phase, all the MOS transistors have yet to turn on. The parasitic BJT transistors can be assumed as diodes. Thus, only the parasitic capacitors are being charged during this phase. The equivalent circuit is shown in Figure 4-10(b). Once the circuit is fed with a supply voltage, all the parasitic capacitors will begin to charge up. When the gate source voltage of MP₇ (V_{ab}) is larger than the threshold voltage

of the PMOS transistor, i.e., V_{TH_P} , both MP_7 and MP_9 turn on. As node d is connected to ground through diode Q_1 , MP_8 and MP_{10} are guaranteed to turn on after MP_7 and MP_9 turned on. Thereafter, node e is connected to VDD through MP_{9-10} . Hence, MN_2 and MN_3 are both turned on and the circuit is triggered, so that the negative feed-back loop will drive all transistors to their steady state regions.

Figure 4-10 Equivalent circuit for start-up: (a) PTAT current source start-up, (b) equivalent node voltage analysis.

There are some boundary conditions to be considered in guaranteeing the circuit to start-up. The crucial factor is whether MP_7 and MP_9 can both be turned on. This is controlled by voltage V_{ab} , which must be larger than V_{TH_P} to turn on MP_7 and MP_9 . Assuming that the circuit cannot start-up, all the MOS transistors are turned off as the parasitic capacitors are being charged. MP_{7-10} have the same W/L , and so the value of the parasitic capacitors C_{GS1} , C_{GS2} , C_{DS1} , C_{DS2} can be assumed to be the same when the transistors are turned off. In the worst case, we do not consider the parasitic capacitance of MN_2 , which is usually smaller than the parasitic capacitance of the PMOS transistor. As

illustrated in Figure 4-10(b), C_{DS1} is in series with C_{GS2} and the two are paralleled with C_{DS2} , such that the total capacitance is 3/2 times that of C_{GS1} . Thus, the supply voltage across the equivalent circuit can be split into four parts: voltage V_{ab} , V_{bd} , resistor voltage drop V_{df} and diode forward voltage drop V_{fg} . The charging current is of the largest when the supply is first added and most voltage drop will occur across the resistor. Thereafter, the charging current decreases to zero until all the parasitic capacitors are fully charged, and the voltage across the resistor will become zero. Hence, the supply voltage can now be viewed as three parts: voltage V_{fg} is still the same diode forward voltage drop, the voltage across V_{ab} and V_{bd} will be inversely proportional to their capacitance, and thus, V_{ab} is 3/2 times of V_{bd} , which is

$$V_{ab} = \frac{3(V_{DD} - 0.7)}{5} \quad (4.18)$$

where 0.7 V is the diode forward voltage drop of the diode connected transistor Q_1 . By assuming that V_{TH_P} is 0.6 V, the supply voltage limitation becomes 1.7 V. If the parasitic capacitor C_{GS3} and C_{DS3} are into consideration, V_{ab} will be larger than the limitation value illustrated in (4.18). Thus, with a 1.8-V supply voltage, the internal start-up function can be guaranteed.

In order to identify the start-up function, a square-wave is applied as the supply voltage for the proposed BGVCR, which is shown in Figure 4-11. As can be seen, there is a start-up process for node b, d and e at the start of every rising edge. And after the start-up phase, the node voltages fall into their respective steady state regions.

Figure 4-11 Simulation results with square wave as supply voltage.

Here, only the PTAT current source start-up is analyzed. This is because after the PTAT current source is started-up, the whole circuit will be pushed into a steady state region. As demonstrated in Figure 4-8, when PTAT current source is triggered, MN_1 will be turned on, causing MP_1 and MP_2 to turn on with the same procedures as the PTAT current source being started-up. MP_{11} and MP_{12} in Figure 4-9 are simply the current mirror that replicate the PTAT current to the bandgap voltage branch. Hence, when the PTAT current source is initiated, the whole BGVCR will start-up.

4.2.5 Experimental Result

The proposed structure is implemented in a standard 0.18- μm CMOS process, and occupies an area of 0.006 mm^2 . The micrograph of the fabricated chip is given in Figure 4-12. The chip is tested at 1.8-V supply voltage with temperature varying from -40°C to 80°C .

Figure 4-12 Micrograph of the fabricated BGVCR chip.

To guarantee the trim-free feature of the proposed BGVCR, the Monte-Carlo simulation was carried out as illustrated in Figure 4-13.

(a)

(b)

Figure 4-13 Monte-Carlo simulation of the proposed BGVCR: (a) voltage reference output; (b) current reference output.

As seen from the Monte-Carlo simulation, the 3σ variation of the voltage reference and current reference is 60 mV and 0.6 μ A, respectively. The voltage reference variation is 5% and the current reference variation is 6% of the output. Both of them are much less than the 20% variation tolerance. Thus, a trimming resistor array is not necessary for the proposed BGVCR. A comparison between the simulation and testing results for the bandgap voltage reference output is provided in Figure 4-14. The simulation results of Figure 4-14(a) proves that the proposed BGVCR can generate bandgap voltage reference with 5 ppm/ $^{\circ}$ C TC across -40° C to 80° C temperature range at 1.8-V supply voltage. The testing results of Figure 4-14(b) shows that the TC is 50 ppm/ $^{\circ}$ C, which is much higher than the simulation result. This is due to the finite load impedance of the multi-meter, which brings a parallel resistance to the bandgap voltage reference output impedance during testing. Thus, the zero-TC point was moved to a lower temperature region, which results in the poorer measured performance than in simulation. Furthermore, the process variation for the BJT transistors has brought about a 30-mV voltage difference between the testing and simulation results. However, in real application, the bandgap voltage reference is usually used to provide the input to a buffer, which can be assumed a capacitive load. Hence, the load impedance is much higher than the impedance of the multi-meter, where the later will have a much lower effect on the bandgap voltage reference output.

Figure 4-14 Voltage reference output: (a) simulation result; (b) testing results.

The current reference output is shown in Figure 4-15. The target value of the current reference is $10\ \mu\text{A}$. However, for layout matching consideration of the poly resistor, we had chosen an even ratio for R_1 and R_2 , leading to a $9.8\text{-}\mu\text{A}$ zero TC current, which constitutes a 2% error when compared to the targeted $10\text{-}\mu\text{A}$ reference current. Fortunately, this can be tolerated in most application. As seen in Figure 4-15(a), the simulation result of the proposed BGVCR can generate $150\ \text{ppm}/^\circ\text{C}$ current reference across -40°C to 80°C temperature range while the measurement result shown in Figure 4-15(b) exhibits a $180\text{-ppm}/^\circ\text{C}$ TC with similar zero-TC point as the simulation result. This proves that the proposed BGVCR can eliminate the process variation through the proposed PTAT current sharing approach.

Figure 4-15 Current reference output: (a) simulation result; (b) testing result.

The self-start-up function is difficult to be tested as the time interval is too short to be snapshotted. However, during the temperature sweeping tests, the chip functions very well when the supply voltage was added and removed frequently. This proves that the proposed start-up-free idea can function well even with temperature variation.

A comparison between the proposed BGVCR voltage reference output and some existing designs is tabulated in Table 4-2 Table I, and the assessment between the proposed BGVCR current reference output and some existing current reference designs is summarized in Table 4-3.

Table 4-2 Summary of bandgap voltage reference design

Parameters	[12]	[16]	[19]	[15]	This work
CMOS Technology (μm)	0.35	0.16	0.18	0.35	0.18
Supply voltage (V)	2.5	1.8 $\pm$ 10%	1.2–1.8	1.8–4.5	1.8 $\pm$ 5%
V_{REF} (V)	0.617	1.08	1.09	0.9	1.1
TC (ppm/ $^{\circ}\text{C}$)	13.7	12	147	14.8	5/sim 50/test
Min. temp. ($^{\circ}\text{C}$)	-50	-40	-40	0	-40
Max. temp. ($^{\circ}\text{C}$)	150	125	120	100	80
Area (mm^2)	0.1	0.12	0.03	0.01	0.006
Need bias current source	Yes	Yes	Yes	Yes	No
Need start-up	Yes	Yes	Yes	Yes	No
Need trimming	Yes	Yes	No	Yes	No

Table 4-3 Summary of existing current reference design

Parameters	[21]	[91]	[92]	[93]	This work
CMOS Technology (μm)	0.18	0.35	0.18	0.35	0.18
Supply voltage (V)	1–1.2	1.8–3.0	1	5	1.8 $\pm$ 5%
I_{REF} (μA)	7.8 $\pm$ 4%	0.096 $\pm$ 2%	144 $\pm$ 7%	0.001–0.05	9.7 $\pm$ 2%
TC (ppm/ $^{\circ}\text{C}$)	24.9	520	185	250	150/sim 180/test
Min. temp. ($^{\circ}\text{C}$)	0	0	0	0	-40
Max. temp. ($^{\circ}\text{C}$)	100	80	100	80	80
Area (mm^2)	0.023 ^a	0.015	0.07	0.006 ^b	0.006
Need BGR	Yes	No	No	Yes	No
Need bias current source	Yes	Yes	Yes	Yes	No
Need start-up	Yes	Yes	Yes	Yes	No
Need trimming	No	No	Yes	Yes	No

^aThis area is without BGR, if add BGR, the area will be 0.123 mm^2 .

4.2.6 Summary

We have proposed a merged structure to generate bandgap voltage reference and current reference without requiring a start-up circuit or a trimming resistor array. With comparable performance to the conventional design, the proposed BGVCR has the most compact structure, occupying only 0.006 mm^2 of silicon area. At 1.8-V supply voltage, the proposed BGVCR can generate 1.1-V reference voltage with 5-ppm/ $^{\circ}\text{C}$ TC and 9.8- μA reference current, with 150-ppm/ $^{\circ}\text{C}$ TC across the -40°C to 80°C temperature range. Based on the proposed

PTAT current sharing concept, the proposed BGVCR can adequately compensate the process variations to yield good performances.

4.3 Bandgap Voltage Reference

The battery operated device may sometimes enter into low power mode when the supply voltage is lower than 2.4-V. During such condition, an ultra-low power BGR is needed to provide a low accuracy reference when the system transit to a standby mode. This is for the system to do fast recovery from the standby mode when supply voltage is higher than 2.4-V. A low power cross-coupled BGR is thus proposed in this section. Based on the suggested structure, a 9.8 ppm/°C temperature coefficient (TC) BGR across -50°C to 150°C temperature range with 1.8-V supply voltage is achieved. The total power consumption is 200 nW at room temperature. The proposed circuit can work at supply voltage varying from 1.4 V to 2.4 V while still enabling a wide temperature range BGR. All the simulation results were based on the standard 0.18-μm CMOS process.

4.3.1 Circuit Design

In order to improve the gain of the 4T stage, the cascode structure of Figure 4-16(a) can be engaged. With two transistors, MP₄ and MP₅, added as a cascode stage, the gain of the 4T stage is boosted by $1 + g_m r_0$ and the error between V_X and V_Y can be lowered by $1 + g_m r_0$. Therefore, the temperature coefficient of the BGR is degraded. Another challenge faced is, the ability to generate the bias voltage V_B without increasing the supply voltage is a challenge.

coefficient. As demonstrated in Figure 4-17(b), the total power consumption is 200 nW at room temperature. The power supply rejection ratio (PSRR) of the proposed BGR is about -22 dB at less than 10 kHz frequency range (see Figure 4-17(c)), which is the key benefit of the cross-coupled cascode stage. Figure 4-18 proves that the proposed BGR can work at 1.4-V to 2.4-V supply voltage. The resistor value here was chosen accordingly to suit the 1.8-V supply voltage. From Figure 4-18(a), it can be noted that the proposed BGR can function well at wide temperature range, without trimming the resistor value following supply voltage variation. Though the power consumption is seen to increase with the supply voltage, the total power at room temperature is still less than 300 nW at 2.4-V supply voltage, as is attested in Figure 4-18(b).

(a)

(b)

(c)

Figure 4-17 Simulation result of the proposed BGR: (a) BGR output at 1.8-V supply voltage; (b) supply current of proposed BGR at 1.8-V supply voltage; (c) PSRR of proposed BGR.

(a)

(b)

Figure 4-18 Effect of temperature and supply voltage variations: (a) output voltage of proposed BGR; (b) supply current of the proposed circuit.

To study the mismatch effect on the proposed cross coupled BGR. The Monte-Carlo simulation was carried with 200 runs as is shown in Figure 4-19.

Figure 4-19 Monte-Carlo simulation for the cross coupled BGR: (a) at 1.4-V supply voltage; (b) at 1.8-V supply voltage, (c) at 2.4-V supply voltage.

As shown in the Monte-Carlo simulation, the 3σ variation of the proposed cross coupled BGR is about 150 mV, which is within the 20% variation specification for the standby mode application.

4.3.3 Summary

The proposed cross-coupled BGR combines the bias circuit and gain stage of the BGR to realise a BGR with 9.8 ppm/ $^{\circ}\text{C}$ temperature coefficient and operating across a temperature range of -50°C to 150°C , while consuming less than 200 nW of power at 1.8-V supply voltage. The proposed circuit can work at supply voltage that varies from 1.4 V to 2.4 V while generating wide temperature range BGR without trimming the resistor value. The design is

based on the standard 0.18- μm CMOS process. A comparison between this work and some existing works is tabulated in Table 4-4.

Table 4-4: Benchmarking proposed BGR against existing BGRs.

Reference	[19]	[14]	[12]	[16]	[20]	[15]	This work**
V_{dd} (V)	1.2–1.8	2–4	2.5	1.7–2.0	1.8–3.5	1.85	1.4–2.4
V_{REF} (V)	1.09	1.142	0.6177	1.0875	1.2	0.91	1.11
TC (ppm/ $^{\circ}\text{C}$)	147	5.3	13.7	12	12	14.8	9.8
Min. temp. ($^{\circ}\text{C}$)	-40	0	-50	-40	5	0	-50
Max. temp ($^{\circ}\text{C}$)	120	100	150	125	95	100	150
Power consumed (μW)*	0.1	46	95	100	10	110	0.2
CMOS technology (μm)	0.18	0.6	0.35	0.16	0.35	0.35	0.18

*Power consumption are based on room temperature.

** Simulation results.

Chapter 5 Current Sensor Design

To track the efficiency of the power regulator, the input power should be measured. To obtain the high accuracy input power, a high performance current sensor must be designed. An enhanced self-biased full range current sensor is thus proposed in this research for measuring the input current.

5.1 Enhanced Full Range Current Sensing Circuit

The enhanced full range current sensing circuit, based on the self-bias current sensing technology, has been proposed in [37]. After a careful enhancement and modification, the current sensing circuit can be used as a full range of current sensor for a buck regulator. Its structure is depicted in Figure 5-1.

Figure 5-1 Enhanced self-bias full range current sensor.

S_{P2} , S_{P3} and S_{N1} are select switches which control the current sensor to sense the current in the power PMOS and NMOS transistor. During the charging cycle, power PMOS will be turned on and at the same time S_{P3} will be turned off

Figure 5-2.

Figure 5-2 Equivalent circuit for power PMOS current sensing.

Transistors, M_{1-4} , M_{6-9} , form a negative feed-back tracking loop between power PMOS, M_P and sensing MOS, M_{PS} , which forces the voltage of V_{PB} to track the voltage, V_{PA} . When V_{PB} is equal to V_{PA} , the current going through the sensing MOS transistor (I_{PS}) and power MOS transistor (I_P) will therefore obey the equation:

$$\frac{I_P}{I_{PS}} = \frac{W_P}{W_{PS}} = N \quad (5.1)$$

W_P and W_{PS} is the channel width power PMOS and sensing MOS transistor respectively. I_P and I_{PS} is the current going through power and sensing MOS transistor respectively. The value of N should be carefully chosen, if N is too large, sensing accuracy will not be good. A very small error will be multiplied by N . However, N cannot be too small. If N is too small, large current will go through current sensor, which will decrease the efficiency of the current sensor to a great extent. Thus, a trade-off has to be done for sensing accuracy and

power consumption. Hence, N is designed to be 800. Then, I_{PS} will be equal to $I_P/800$. The sensing current I_{PS} will be split to form two current, I_1 and I_2 , which goes into M_6 and M_7 transistor. A part of I_P which is only $1/800$ will be divided to form current, I_3 and I_4 , which will go through M_8 and M_9 transistor. M_7 and M_8 transistors operate as an amplifier. At the same time, M_2 and M_3 transistor operate as a load and in order to achieve high speed, the aspect ratio of M_2 , M_3 , M_7 and M_8 transistor should be as small as possible. However, there is a limit to it otherwise it may suffer from channel length modulation and inherit the effects of short-channel length. This will have a great impact on its sensing accuracy. Hence, the current of M_9 will go through M_4 which will be mirrored by M_5 . At last, the current mirror pair, M_{10} and M_{RS} , will mirror this current to the resistor, R_{SENSE} , and convert this current to a sense voltage, V_{SENSE} , whereby its equation is shown below:

$$V_{SENSE} = \frac{I_P}{800} R_{SENSE} \quad (5.2)$$

This sensing voltage can be used for the comparator input for control purpose. Hence, the current going through M_9 should be as large as possible. In order to keep voltage V_{PB} to be equal to V_{PA} the total current going through M_6 and M_7 should be equal to the current going through M_8 and M_9 which means that: $I_1 + I_2 = I_3 + I_4$. M_7 and M_8 transistor usually have symmetrical structure, thus, $I_2 = I_3$. Hence, I_1 should be equal to I_4 . Therefore, the same aspect ratio is chosen for M_2 , M_3 , M_7 , M_8 , and this goes for M_1 , M_4 , M_6 , M_9 as well. I_2 and I_3 will affect the speed of the current sensor and I_1 and I_4 will affect the accuracy of the current sensor, thus a trade-off has to be carefully considered. I_1 is chosen to be twice the value of I_2 . Thus, M_1 , M_4 , M_6 and M_9 transistor is chosen to be twice of M_2 , M_3 , M_7 and M_8 . In this case, I_4 is $2/3$ of I_{PS} . Thus, the ratio of aspect ratio between M_4 and M_5 is 2:3, and then I_{SEN1} will be equal to I_{PS} . This is so that it can keep I_{SEN} to be equal to I_{PS} whereby the aspect ratio for M_{10} and M_{RS} is 1:1.

During the discharging cycle, the power PMOS will be turned off while power NMOS will be turned on. At the same time, the corresponding switches S_{N1} and S_{P2} will be turned off while S_{P3} will be turned on. The drain of current sensor M_{NS} will be connected to V_{NB} via switch S_{N2} . The current sensor will be turned

The only difference observed is that the voltage tracking loop has changed. For the power NMOS current sensor, a negative feed-back tracking loop was formed by M_{1-4} and M_{6-9} , which forces voltage V_{NB} to be equal to V_{NA} , the sensing current I_{NS} will be divided into two parts as its respective currents, I_3 and I_4 , which goes through M_3 and M_4 . I_1 and I_2 will be directed to ground directly instead of going through power NMOS M_N , which is the only difference between M_N and M_P current sensing. In order to share the same current sensing core, the same sensing ratio N is chosen which yields a value of 800. However, I_1 and I_2 will go through M_P but not M_N , this will also bring a $1/800$ sensing difference between M_N and M_P which can be ignored.

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voltage drop should no doubt be compensated in one way or another. The switch, S_{P1} is used to balance S_{P3} while switches S_{P2} , S_{N2} , S_{N3} , S_{N4} are used for balancing S_{N1} . During the charging cycle, switches S_{P2} and S_{N1} will be turned on while the switch, S_{P3} will be turned off. M_P will be connected with V_{PA} via S_{P2} , there do exist a voltage drop across switch S_{P2} . Therefore, a balancing switch is added to compensate the voltage drop across S_{P2} . Switch S_{N1} will incur a voltage drop between V_{NB} and ground. Balancing switch S_{N3} is included in the circuit design to compensate for the voltage drop across switch S_{N1} . Also, M_4 and M_5 form a current mirror pair, but there is an existing voltage drop across switch S_{N1} between M_4 and ground. Thus, balancing switch S_{N4} is added between M_5 and ground. During the discharging cycle, switch S_{P3} will be turned on while switch S_{P2} and S_{N1} will be turned off. Switch S_{N3} will lead to a voltage drop between V_{NA} and ground. A balancing switch S_{N2} is added to compensate the voltage drop of S_{N3} and allow the source of M_{NS} and M_N transistor to be assumed equal. Also, S_{N4} is still required to compensate the voltage drop of S_{N3} . Balancing switch S_{P1} is used to compensate the voltage drop across switch S_{P3} . However, the PMOS current sensor, M_{PS} will cause a voltage drop between V_{IN} and S_{P1} , hence, a balancing transistor M_{BS} is added to compensate the voltage drop caused by M_{PS} . As a result, the sensing and power MOS transistor can yield approximately the same source, gate and drain voltage. In this condition, the current sensor will yield a very good sensing accuracy compared to the topology where the current sensor and the balancing switch are absent. A comparison has been drawn for with and without the balancing switch. S_{P1} is removed and V_{PB} and the drain of M_{PS} transistor are connected together which is based as a comparison with the current sensor and all balancing switches. Their simulation results are depicted in Figure 5-4.

Figure 5-4 Comparison for balancing switch.

From the waveforms and results shown in Figure 5-4, it is evident that the balancing switch is very important. If one balancing switch is missing, this will reduce the responding speed and accuracy of the current sensor to a great extent.

Besides the balancing switch, there are other circuit techniques to be considered such as the control signal for the switches in the current sensor. The aspect ratio of power MOS is usually very big which gives rise to a large parasitic capacitance since capacitance value is proportional to its area. Hence, the power MOS cannot be turned on and off immediately. Therefore, a dead time interval must be added between the turning off of M_P and the turning on of M_N and vice versa. Thus, the switches should be controlled very carefully during dead time otherwise a large glitch will appear in the output of the current sensor as shown in Figure 5-4.

During the dead-time interval that exist between the turning off of M_P transistor and the turning on of M_N transistor, the switch SP_3 will be turned on and SN_1 will be turned off. Switch SP_3 and transistor M_{BS} will operate as pull up switch like the pull up switch MS_1 mentioned in [27]. SP_3 must not be turned on too early otherwise PMOS sensing will be blocked by the pull up switch, SP_3 , before it gets turned off, which will affect the sensing accuracy of the current sensor. However, the switch SP_3 should be turned on before M_P turns off otherwise a large glitch will appear in the output of the current sensor which can be observed in Figure 5-5.

Figure 5-5 Glitch during SP_3 turning on.

The reason for the glitch is that M_P transistor and switch SP_1 turn off before SP_3 turns on which causes the node voltage, V_{PA} to be floating. For SP_1 , it is operating as a MOS switch hence its body diode will be forced to conduct,

which will pull the voltage node of V_{PA} to a lower level. However, the negative feed-back tracking loop is still trying to force V_{PB} to track the voltage node of V_{PA} , as result, V_{PB} will be pulled down to a lower level. According to the current law, I_{PS} will be very large, hence, glitches will appear. In order to eliminate the glitch, S_{P3} should be turned on earlier than the turning off of transistor S_{P1} . However, S_{P1} and M_P are controlled by the same signal. Hence, S_{P3} should be turned on just a little earlier (usually a few ns) before the turning off of M_P transistor but also not too early as well. Hence, there exists an optimum time which takes into account of all these design trade-offs.

Switch S_{N1} must be turned off after M_P turns off; otherwise another glitch will appear during the turning on of M_N transistor as shown in Figure 5-6.

Figure 5-6 Glitch during S_{N1} turning off.

If S_{N1} turns off too early, the node voltage, V_{NB} , will be floating hence it is connected with M_{NS} via S_{N1} . Although M_{NS} is still turned off, the body diode of M_{NS} will be forced to conduct. V_{NB} and V_{NA} will be connected via S_{N1} , V_{NS} and S_{P2} . A big loop is formed. The voltage node of V_{NB} is not nearly zero again thus large errors will incur in the current sensor. As a result, oscillations will appear in the output of the current sensor. Furthermore, S_{N1} must not be turned on too late otherwise a much longer respond time is required for the current sensor. To make it worse, if the current sensor turns on too late, which is greater than the turning on of M_N , the current sensor will be blocked by the pull down action of switch, S_{N1} . If S_{N1} cannot be turned on before reaching the steady state condition, the power NMOS current sensor will not operate as usual as shown in Figure 5-6. In this steady state equilibrium, the current sensor will not operate

well even though S_{N1} turns off later. Hence, S_{N1} must be turned off after M_P turns off, and before the turning on of M_N transistor.

During the dead-time interval between the turning off of M_N transistor and the turning on of M_P transistor, the switches S_{N1} , S_{P2} will be turned on while S_{P3} will be turned off. S_{N1} should not be turned on too early as illustrated in Figure 5-7.

Figure 5-7 Glitch during S_{N1} turning on.

If it is turned on too early, M_N sensing operation will be blocked which affects the sensing accuracy. This can be seen in Figure 5-7. If S_{N1} turns on too late, V_{NA} will be floating, in this way, the body diode of S_{NS} will be forced to conduct and both voltage nodes, V_{PB} and V_{NA} will be connected through S_{N2} , S_{P2} and body diode of M_{NS} . Hence, a large feed-back loop will be formed between V_{PB} and V_{NA} . When a steady state is established, it will take a very long time for the current sensor to return to its normal sensing state which is observed in Figure 5-7. Even worse, the current sensor cannot recover to its normal working state before the next cycle begins. Thus, S_{N1} should be turned off just a little earlier than M_N (usually a few ns).

Switch S_{P3} cannot be turned off too early otherwise a large glitch will appear in the output of the current sensor as shown in Figure 5-8.

Figure 5-8 Glitch during S_{P3} turning off.

With reference of Figure 5-8, if S_{P3} turns off too early, a glitch will appear in the output of the current sensor. This is because, S_{P3} turns off too early, hence V_{PA} will be floating and the body diode of MOS switch S_{P2} will be forced to conduct. V_{PA} will be connected to ground via the body diode of MOS S_{P2} and M_N . Voltage of V_{PB} will be pushed to a lower voltage level. There may be some leakage coming from power MOS which still need further study in future work. However, the switch cannot be turned off too late otherwise the M_P sensing operation will be ceased and this will bring about some delay in the output. Hence, S_{P3} will be turned off after the turning off of M_N but only a few ns before M_P turning on or probably at the same time as the turning on of M_P transistor. Also, the accuracy at the turning on of M_P is not very accurate and this may not be useful. Thus, to avoid glitches in the output of the current sensor, S_{P3} can be turned off a little later before the turning on the M_P transistor.

According to the analysis shown, a special timing diagram should be designed to fulfil all of the requirements shown above, as illustrated in Figure 5-9.

Figure 5-9 Timing diagram for current sensor switching control.

This control timing diagram is easily achieved. In a real practical design, only one clock will exist in the system. All of the control signal should be generated from the same clock. This kind of control signal will be very difficult to achieve in normal circuit design. But this is not the case in this design. An unsymmetrical driver have been drawn which will be shown in the later

chapters. As a result of the unsymmetrical driver design, this timing diagram can be achieved by adding some delay on the driver output signal.

The control signal during the dead-time interval between the turning off of M_P transistor and the turning on of M_N transistor is provided in Figure 5-10.

Figure 5-10 Control signal during dead-time for M_P turning off and M_N turning on.

The unsymmetrical driver comprises of two stages: the first stage of the driver for M_P and M_N will be generated from the same clock. The turning on control signals for S_{P3} was generated from the first stage driver for M_P with a small delay but the turning on control signals for S_{N1} will be generated from first stage driver for M_N with a larger delay. The last stage driving signal for M_P will be generated from the first stage of M_P with a longer delay than the delay for S_{P3} . The last stage driving signal for M_N will be generated from the first stage of M_N with the largest possible delay. The timing diagram will follow the flow: first, S_{P3} turns on; second, M_P turns off; third, S_{N1} turns off; last, M_N turns on as shown in Figure 5-9.

The control signal during the dead-time interval between the turning off of M_N transistor and the turning on of M_P transistor is illustrated in Figure 5-11.

Figure 5-11 Control signal during dead-time for M_N turning off and M_P turning on.

As described above, the first stage driver for M_P and M_N are generated from the same clock with different delays. The turning on signals for S_{N1} is generated from the first stage driver for M_N which adds a little delay while the turning off signals for S_{P3} is generated from the first stage driver for M_P , with a larger delay. The last stage driving signal for M_P was generated from the signal of the first stage driver of M_P with a relatively larger delay. The last stage driving signal for M_N was generated from the signal of the first stage driver for M_N with small delay, but it is larger than the delay for the turning on of S_{N1} . Thus, the timing diagram will be as follow: first, S_{N1} turns on; second, M_N turns off; third, S_{P3} turns off and M_P turns on simultaneously.

5.2 Post Layout Simulation Result

Current sensor is very sensitive to layout, process and temperature variation. Thus, a very compact layout has to be ensured. Its post-layout simulation results can be observed in Figure 5-12.

Figure 5-12 Post layout simulation for current sensor.

The enhanced self-biased current sensor is designed for sensing a current (<500 mA). The current sensor converts the sensing current to a voltage, which corresponds to a 1mV representing a 1mA of current in the power regulator. From Figure 5-12, a conclusion can be reached. The current sensor exhibits good sensing accuracy. Its peak sensing accuracy can be higher than 96% for a load ranging from 40 to 300mA . It can still yield a high accuracy of $>93\%$ if the load is higher than 500mA . For the valley current sensing part, there exists an offset voltage of 6mV in the output of the current sensor. Its presence can be explained due to the fact that power PMOS and NMOS has different current characteristic. If the offset voltage in the valley current sensing output is

removed, the accuracy of the valley current sensing can yield > 97% accuracy for a load ranging from 25 to 535 mA.

Furthermore, there does exist some glitches in the output of the current sensor. This is due to the parasitic capacitance from the post-layout simulation of the circuit together with its corresponding pads for ESD protection. Due to the presence of these undesirable parasitic capacitances, the control signals for the current sensor switch will be delayed as shown in Figure 5-13.

Figure 5-13 Post layout simulation for control signal.

With reference of Figure 5-13, further analysis can be carried out to investigate the glitches in the output of the current sensor.

A compare table between the proposed design is shown in Table 5-1.

Table 5-1 Comparison between the proposed design and existing current sensor design.

	[27]	[35]	[36]	[37]	This Design
Technology (CMOS)	0.6 μm	0.35 μm	0.35 μm	0.35 μm	0.18 μm
Accuracy	90%	90%	90%	90%	93%
Topology	Buck	Boost	Buck	Buck-Boost	Buck
One cycle full range	no	yes	no	yes	yes
Need bias	yes	yes	yes	no	no

As shown in the compare table, the proposed full range self-biased current sensor is the only design for buck regulator which can sense full range current of the power regulator in one switching cycle.

Chapter 6 Power Stage Design

6.1 Power MOSFET

6.1.1 Design of Power MOSFET

Due to the given rationale mentioned above, the channel width of the power MOS transistor should be carefully designed. In order to achieve adaptive efficiency over a wide load range, the power regulator should undergo careful optimization for each and every load condition. According to the introduction part of this thesis, our target implementation is for portable devices whereby its load current ranges from several tens of mA – 1 A, thus we divide this wide load range into two sub-range which comprises of less than 500 mA (light load), 500 mA – 1A (heavy load). Here is the study for the relationship for power transistor size and load current, which is first step towards the implementation of a wide load range adaptive efficiency power regulator. It first focuses on light load and small step down voltage which just convert 1.8-V supply voltage to 1.2-V output voltage. A careful comparison has been drawn to find the optimized channel width for the power MOS transistor. A test bench was designed for power MOS channel width chosen in accordance to the 0.18 μm CMOS process.

Figure 6-1 Power MOS test bench.

This test bench is only used for testing the loss of the power MOS transistor, thus the efficiency of this test bench can be calculated as

$$Efficiency = 1 - \frac{P_{COND} + P_{SW}}{P_{IN}} = \frac{I_{LOAD} \cdot V_{LOAD}}{I_{IN} \cdot V_{IN}} \quad (6.1)$$

where P_{IN} is input power which equal to supply voltage V_{IN} times input current I_{IN} , I_{LOAD} is current going to load resistance, V_{LOAD} is voltage . The parameters in the test bench were shown in Table 6-1.

Table 6-1 Parameters of the test bench

Parameter	Name	Value	Unit
Input voltage	V_{IN}	1.8	V
Output voltage	V_{LOAD}	1.1-1.2	V
Load current	I_{LOAD}	5-500	mA
M_P single cell channel length	L_P	0.18	μm
M_P single cell channel width	W_P	480	μm
M_N single cell channel length	L_N	0.18	μm
M_N single cell channel width	W_N	160	μm
M_P cell number	N_P	1-100	
M_N cell number	N_N	1-100	
Switching frequency	f	1	MHz
Duty cycle	D	66.6	%
Inductor	L	10	μH
Capacitor	C	10	μF

In the test bench, a single cell of M_N is chosen first chosen with aspect ratio of $160 \mu\text{m}/0.18 \mu\text{m}$. Because, electron mobility is about three times that hole mobility. Thus, M_P channel width is chosen to be about thrice the size of M_N , which is $480 \mu\text{m}/0.18 \mu\text{m}$ here for a single cell. Both M_P and M_N have 1 to 100 cells. The power MOS size will be swept from 1 cell to 100 cells, and the load current sweeping will be done for every channel width. As the first step will focus on light load range, load current sweeping range will be 5 to 500 mA.

Here, 66.6% duty cycle control signal is chosen for this power regulator to convert the 1.8-V input voltage to a 1.2-V output voltage. The simulation result is shown in Figure 6-2.

Figure 6-2 Efficiency versus load and power MOS channel width.

With reference to Figure 6-2, 50 cells yield the best efficiency over a load range of 10 to 200 mA. Thus, 50 cells are chosen here, where M_P is $24000 \mu\text{m}/0.18 \mu\text{m}$, and M_N is $8000 \mu\text{m}/0.18 \mu\text{m}$.

In this test bench, all components are deemed ideal. Only the loss due for power MOS is considered. However, when the loss of inductor and other blocks of the power regulator are added, the curve may be changed. Hence, an adaptive power MOS size control method is needed to find the best power MOS size according to load that can achieve according to its load the highest efficiency for the power regulator which will be illustrated in further chapter.

Furthermore, the duty cycle here is not 50% but 66.6%, thus, the contribution for switching loss of the two power MOS are not the same. However, the

mobility of M_P and M_N are not the same, the size of M_N is usually one-third of M_P with the same turn on resistance. And furthermore, load current, switching frequency will affect the total power loss, M_P and M_N ratio must be calculated according to many factors. This best aspect ratio will be chosen in the future adaptive efficiency power regulator. Here, we only choose the 3:1 ratio in this design.

6.1.2 Layout Design of Power MOS

Due to the large size of the power transistor, the layout design is to be considered carefully, especially since the layout of the power MOS can significantly affect its parasitic capacitance and turn on resistance [94]. Single finger transistor layout is easy to be implemented, but two problems arise: Firstly, the power MOS usually has a very wide channel, which means a larger chip area is required, and so not area efficient. Secondly, the turn on resistance is limited by the metal width of the power MOS no matter how large the channel width of the power MOS [95].

Figure 6-3 Effect of channel width on power MOS resistance [95].

With reference to Figure 6-3, increasing the single finger width of the power MOS can only decrease the channel resistance, but not the total turn on resistance. This is because the power MOS turn on resistance is jointly decided by the channel resistance as well as the resistance of the metal and via of the routing layers. In order to save area and to reduce the power MOS turn on resistance, multi-finger and waffle structures have been proposed in [95-97], and the multi-finger structure is shown in Figure 6-4.

Figure 6-4 Multi-finger structure [95].

In older process technologies, there exists only a few metal layers. Thus, waffle layout structure takes advantage as compared to multi-finger structure. The waffle layout structure is occupied by the inter-connection of metal rather than the active area which result in the turn on resistance of the power MOS to be reduced to a greater extent. Thus, for the same size of power MOS, waffle structure layout will yield a much smaller turn on resistance as compared to multi-figure layout [97]. However, the area occupied by waffle layout is much larger than the multi-finger structure and it requires special PDK to support which may not be practical in normal process. Furthermore, there are more metal layers in the latest CMOS process (six layers in standard 0.18- μm process and nine layers for 65-nm process), which can be used for optimizing the routing line of the power MOS transistor. Thus, a carefully metal routing has to be designed for the layers of metal routing and inter-connection of the power MOS transistor as is illustrated in Figure 6-5.

Figure 6-5 Metal optimization.

Similar to Figure 6-4, both metal-1 and metal-2 are overlapped to reduce the metal resistance of the source and drain of the transistor. However, in Figure 6-4, the current going to source and drain will travel a long way on the metal which will limit the current going through it. In order to reduce the thin metal length which the current will pass through, a special structure was proposed in Figure 6-5. The current originating from metal-3 will go deep through via-2 to metal-2 and further to metal-1 through via-1 to metal-1. This current will only travel 1/4 of the finger length as shown in Figure 6-5 which will no doubt reduce the turn on resistance of the power MOS by a great extent. Figure 6-5 is the unit cell of the power MOS. The same metal optimization idea is applied to connect the entire unit cell together to form the large power MOS transistor. A robust and compact layout is carefully designed, which is provided in Figure 6-6.

Figure 6-6 Power MOS layout.

M_P occupies a silicon area of $160\ \mu\text{m} \times 200\ \mu\text{m}$, whose aspect ratio is $24000\ \mu\text{m}/0.18\ \mu\text{m}$. And the M_N occupies nearly 1/3 of the area of M_P , the turn on resistance of M_P and M_N are summarized as follow:

Table 6-2 Turn on resistance of M_P and M_N

Turn on resistance	M_P	M_N
Pre-Layout	98.6 m Ω	83.1 m Ω

Post layout	105.6 m Ω	89.1 m Ω
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As shown in Table 6-2, the turn on resistance of post layout-simulation is nearly the same as the pre-layout result, which means the well-organized layout only bring about very small parasitic resistance for the power MOS.

6.2 Dead-Time Control

Dead-Time control is very important for power regulator, as it greatly affects the efficiency of the power regulator. A study on the relationship between dead-time control and efficiency of the power regulator is carried out based on the simplified power regulator circuit shown in Figure 6-7.

Figure 6-7 Test bench for relationship between efficiency and dead-time.

Here, both V_{P_DRIVE} and V_{N_DRIVE} are generated from an ideal clock that has a timing diagram as that shown in Figure 6-8.

Figure 6-8 The timing diagram of the gate control signal.

Both T_{DLY1} and T_{DLY2} are dead-time that needs to be controlled for the power transistor gate driving signal. We shall first discuss T_{DLY2} first, which controls the NMOS power transistor M_N to turn on. The load current varies from 10 mA to 87 mA with efficiency versus dead-time as shown in Figure 6-9.

Figure 6-9 Efficiency versus dead-time at different load current.

As shown in Figure 6-9, it can be seen that different load current needs different dead-time to achieve the highest efficiency. At heavy load, short dead-time is needed, while at light load, longer dead-time is needed. This is because, at heavy load, large current will go through the inductor, this current will charge and discharge the parasitic capacitor of the power transistor in a fast speed. Thus, short dead-time is need. If dead-time is too long, the body-diode of the NMOS power transistor will be conducted to reduce the efficiency of the power regulator. At light load, small current goes through the inductor, thereafter, the charging and discharging speed of the parasitic capacitor is limited by the inductor current, which means longer dead-time is needed to discharge the energy from the parasitic capacitor to the inductor. If dead-time too short, the energy stored in the parasitic capacitor of the power transistor will not be fully utilized by the inductor to charge the load. Hence, the efficiency will be limited by switching loss of the power transistor. Several adaptive dead-time control methods to optimize dead-time control have been proposed as shown in the literature review part. However, the adaptive dead-time control circuit usually needs high gain, high speed amplifier to attain a fast response time, and the driver stage is usually very large to help reduce the delay. The last stage driver

size can be therefore as large as $1/3$ of the power transistor. Also, the driver will need several stages, and this means the driver will occupy nearly $2/3$ of the total power transistor area. The driver itself is also inverter chain, which has switching loss and conduction loss to further reduce the total efficiency. Thus, the conventional approach is not best choice for dead-time control.

As are examine Figure 6-9 more carefully, it can be understood that the switching loss is usually large but happens in very short time. On the other hand the body diode conduction loss is proportional to the dead-time and does not increase very fast. Knowing this, we can minimize the total loss by controlling the dead-time to occur at the region where power transistor encounters body diode conduction and not for a too long duration. The driver size should be reduced at the same time instead of having accurate dead-time control combined with strong driver. And prediction idea can be adopted here to further reduce the body diode conduction time over wide load range.

From the points discussed above, two new dead-time control driver methods are proposed in this chapter.

6.2.1 Asymmetrical Dead-Time Control Driver

This sub-chapter presents an asymmetrical dead-time control driver (ASDTCD) for synchronous buck converter operating in continuous conduction mode (CCM). Dead-time control is an important metric for improving the efficiency of switching mode power regulator. Without additional circuit, the proposed ASDTCD can generate dead-time by controlling the slope for the output signal of the driver. The proposed ASDTCD utilizes the transition between triode region and saturation region for the power transistor to avoid body diode conduction and shoot through current while minimizing switching loss. Thus, high speed body diode conduction sensor is avoided; thereby, reducing the power consumption and saving silicon area. And the body diode conduction time accuracy is also enhanced. We achieve less than 1ns body diode conduction time without shoot through current across 10 mA to 450 mA load range. With a power consumption of less than 0.5% of the total input power, the proposed ASDTCD takes less than 1% of the power transistor area which saves

up to 40% of the total chip area. This design is implemented in 0.18- μm CMOS process.

6.2.1.1 Proposed Dead-Time Generating Theory

As discussed above, to control the dead time accurately, a short rise and fall time is needed for the gate control signal of M_P and M_N . As shown in Figure 2-16, in order to get an accurate delay time T_{DLY} , both of edge around T_{DLY} should be very steep, or else, delay error will appear, which will result in shoot through or body diode conduction of M_N . Hence, the buffer driver should have very strong drive capability to get such steep edge. Thus, the tapering factor of the power MOS should be as small as 3-30, which means the area for the last stage of the driver buffer should be as large as 1/3 of power MOS. However, the rising and falling edge itself can be used as dead time control signal. A charging and discharging delay can be used to generate a dead time for the gate control signal of M_P and M_N which can be seen in Figure 6-10.

Figure 6-10 Dead time generated by charging and discharging delay.

As shown in Figure 6-10, different rising and falling edge of the gate control signal for M_P and M_N , will result in different delay. V_{TH_P} and V_{TH_N} are threshold voltage of M_P and M_N . When gate control signal of M_P become lower than $V_{DD} - V_{TH_P}$, M_P will turn on, then, T_{DLY1} will be generated by the slow falling edge of M_P gate control signal and steep falling edge of M_N gate control signal. Similarly, M_N will be turned on when the gate control signal higher than V_{TH_N} , then, T_{DLY2} will be generated by the slower rising edge M_N gate control signal and steep rising edge of M_P gate control signal. Thus, a dead time will be generated by the driver itself instead of additional control circuit. The falling edge of M_P gate control signal is much slower than M_N gate control signal,

which will result in M_P turn on later than M_N off. Hence, shoot through between M_P and M_N will be avoided. The raising edge of M_N gate control signal is much slower than M_P , which will result in M_N turn on later than M_P turn off. Thus, shoot through between M_P and M_N can be avoided here. Furthermore, the non-zero voltage of M_N gate will block body diode conduction of M_N . This is because body diode conduction for M_N need negative voltage exists in drain of M_N . However, this negative drain voltage and positive gate voltage of M_N will force M_N turn on, instead of body diode of M_N to be conducted. Also, steep rising edge is not needed here; hence, the area taken by driver buffer will be much smaller than the adaptive control method.

A relation between rising and falling edge of the gate control signal of the power MOS and tapering factor for the last stage driver buffer have been studied first, which is depicted as follow.

Figure 6-11 Rising edge of M_N gate control signal.

Here, the aspect ratio of M_N is $8000 \mu\text{m}/0.18 \mu\text{m}$, CLK is input signal of the driver buffer, Ratio is the ratio of M_N to last stage driver, which is the tapering factor between power NMOS and last stage driver. The CLK here have 5 ns rising edge, this is used for simulating real clock for the power regulator control. It can be seen from Figure 6-11 that 100 is enough for the ratio between M_N and last stage driver to get a 1 ns rising edge using 5 ns falling edge input clock and 500 is enough to get 5 ns rising edge with the same clock. The falling edge of M_N gate control signal is illustrated in Figure 6-12.

Figure 6-12 Falling edge of M_N gate control signal.

It can be seen from Figure 6-12 that a similar result can be gotten for falling edge M_N gate control signal. 100 is enough for the ratio between M_N and last stage driver to get a 1 ns rising edge using 5 ns rising edge input clock while 500 is enough to get 5 ns rising edge with the same clock.

Similar study has been conducted on M_P which rising edge is shown in Figure 6-13.

Figure 6-13 Rising edge of M_P gate control signal.

Here, the aspect ratio for M_P is $24000 \mu\text{m}/0.18 \mu\text{m}$. It can be seen from Figure 6-13 that 100 is enough for the ratio of M_P and last stage driver to get 2 ns rising edge using 5 ns falling edge input clock, and 500 is enough to get 10 ns

rising edge with the same clock. The falling edge of the M_P is depicted in Figure 6-14.

Figure 6-14 Falling edge of M_P gate control signal.

Very similar to rising edge gate control signal, 100 is enough for the ratio of M_P and last stage driver to get 2 ns falling edge, and 500 is enough to get 10 ns falling edge with 5 ns rising edge clock, which can be seen from Figure 6-14.

6.2.1.2 Proposed Unsymmetrical Driver Circuit

Based on the above discussion, the asymmetrical driver shown in Figure 6-15 is proposed to attain the control logic of Figure 6-10. M_{P_SD1} and M_{N_SD1} form the second driver stage (i.e., last driver stage) for M_P while M_{P_SD2} and M_{N_SD2} form the second driver stage for M_N . C_{P_GS} and C_{P_GD} are parasitic capacitors for M_P , while C_{N_GS} and C_{N_GD} are parasitic capacitors for M_N . r_{P_SD1} , r_{N_SD1} , r_{P_SD2} , r_{N_SD2} are the turn-on resistor of M_{P_SD1} , M_{N_SD1} , M_{P_SD2} , M_{N_SD2} , respectively. M_P and M_N function as power switches in triode region. Thus, the parasitic capacitances for M_P and M_N can be expressed using the triode region transistor parasitic capacitance function, which is

Figure 6-15 Asymmetrical dead-time control driver.

$$C_{GS} = C_{GD} = \frac{1}{2} W L C_{OX} \quad (6.2)$$

where W is channel width of the transistor, L is channel length of the transistor, and C_{OX} is the unit area capacitance for the transistor. L is usually chosen to be the smallest size of the process to save area, and W_P is usually 2 or 3 times of W_N to cater for the mobility difference. Hence, the value for C_{P_GS} (C_{P_GD}) is usually 2 or 3 times of C_{N_GS} (C_{N_GD}).

M_{P_SD1} , M_{N_SD1} , M_{P_SD2} , M_{N_SD2} are drivers for M_P and M_N and are used as switches to operate in the triode region. For a MOSFET operating in the triode region

$$I_D = \frac{1}{2} \frac{W}{L} \mu C_{OX} [2(V_{GS} - V_{TH})V_{DS} - (V_{DS})^2] \quad (6.3)$$

where I_D is the current going through channel, μ is mobility, V_{TH} is threshold voltage, V_{DS} is drain source voltage and V_{GS} is gate source voltage of the transistor. The transistor working in triode region, thus, V_{DS} is usually much smaller than V_{GS} , hence, the turn-on resistance (r_{DS}) of the transistor is

$$r_{DS} = \frac{L}{W(V_{GS} - V_{TH})} \quad (6.4)$$

where V_{GS} is usually the supply voltage and V_{TH} is the threshold voltage (both voltages can be assumed as fixed values during the transition of power transistor switching), and as explained earlier, L is usually chosen to be the smallest value of the process. The turn-on resistance of the driver stage is decided by the channel width W of the driver transistor.

From Figure 6-15, it is easy to understand that the charging and discharging speeds of the parasitic capacitance of power transistors depend on the turn-on resistance of the last stage driver and the parasitic capacitances of the two power transistors.

According to (6.2)–(6.4), the slopes of the rising and falling edges of M_{P_DRIVE} and M_{N_DRIVE} are decided by the ratio between the channel widths of last stage driver and power transistor. Hence, a dead-time can be generated by different channel width ratios between the last stage drivers for M_P and M_N . Different transistors of the last stage driver shown in Figure 6-15 serve to control the dead-time during M_P and M_N turning on. For further analysis, the switching period can be divided into two phases— M_P turn-on and M_N turn-on.

At phase 1, M_N switches off and M_P switches on; the equivalent circuit is given in Figure 6-16. Capacitor C_{P_GS} will be reversely charged by r_{N_SD1} and C_{P_GD} will be discharged by r_{N_SD1} while C_{N_GD} and C_{N_GS} will be discharged by r_{N_SD2} . In order to realize the timing diagram of Figure 6-10, C_{N_GS} and C_{N_GD} are discharged swiftly to allow M_N to switch off quickly. The charging speed of C_{P_GS} and discharging speed of C_{P_GD} are slow to decrease the gate source voltage of M_P (V_{P_GS}) slowly. After V_{P_GS} becomes lower than $V_{DD} - V_{TH_P}$, M_P begins to turn on, which is in saturation region now and V_X will be increased from 0 to V_{DD} . C_{P_GD} and C_{N_GD} will be reversely charged to V_{DD} by r_{N_SD1} and r_{N_SD2} , and after which, M_P will be transited to triode region which serve as high side switch then. Thus, r_{N_SD1} should be much larger than r_{N_SD2} . According to (6.4), the dead-time between M_P and M_N can be controlled by the ratio of W_{N_SD1} and W_{N_SD2} . Hence, W_{N_SD1} should be much smaller than W_{N_SD2} to attain the required dead-time. This is illustrated through the simulations results in Figure 6-17.

Figure 6-16 Equivalent circuit when M_P switched on.

Figure 6-17 Simulation results showing dead-time during M_P turning on.

At phase 2, M_P switches off and M_N switches on. The equivalent circuit of the proposed circuit is illustrated in Figure 6-18. Capacitors, C_{P_GS} and C_{P_GD} , will be reversely discharged by r_{P_SD1} , and capacitor, C_{N_GD} , will be reversely discharged by r_{P_SD2} , while capacitor C_{N_GS} will be charged by r_{P_SD2} . In order to realize the control timing diagram of Figure 6-10, C_{P_GS} and C_{P_GD} are discharged quickly to allow M_P to switch off at a fast pace. After M_P is turned off, V_X begins to decrease and C_{P_GD} becomes positively charged. During this short interval, the current in inductor L (I_L) can be assumed as constant and it

provides the charging current for C_{P_GD} and discharging current for C_{N_GD} . However, the discharging speed of C_{N_GD} and charging speed of C_{N_GS} are both slow, leading to the gate source voltage (V_{N_GS}) of M_N to be increased slowly. When V_{N_GS} is higher than the threshold voltage of M_N (V_{TH_N}), M_N begins to turn on. However, during this time, V_X is higher than V_{N_GS} , which means that M_N is working in saturation region instead of triode region. Thus, the turn-on resistance of M_N is high, which can protect both M_P and M_N from the shoot through current. Also, this large turn on resistance will limit the current go through M_N , which helps the energy stored in the parasitic capacitor to be utilized by the inductor instead of being shorted by M_N to ground. Thereafter, the switching loss is minimized. When V_X equals to V_{N_GS} , capacitor C_{N_GD} becomes positively charged by I_L . Transistor M_N will thus transit from saturation region to triode region. Its turn-on resistance will be substantially reduced to avoid body-diode conduction, as is proven in Figure 6-19. The best time for M_N to turn on is the time when V_X is 0. But in normal body-diode conduction detection or zero voltage detection method, it is quite difficult to have $V_X = 0$. No matter how fast and high gain the amplifier is, there exists some delay and detection errors.

Figure 6-18 Equivalent circuit when M_N switched on.

Figure 6-19 Simulation results showing dead-time during M_N turning on.

Fortunately, in our proposed asymmetrical driver control method, it is not necessary to have precise control over the dead-time. The key timings are when V_{N_GS} arrives at V_{N_TH} , it must be before $V_X = 0$. Also, V_{N_GS} must only be of V_{DD} after node V_X discharged to zero. Similarly, controlling just the ratio of W_{P_SD1} and W_{P_SD2} can yield the dead-time control timing diagram of Figure 6-10. Furthermore, this method does not require the dead-time to be controlled very accurately. Hence, the last stage driver can be much smaller than the power transistor, because they do not require strong driving capability to generate the steep rising or falling edges to shorten the delay between the body diode conduction sensor and driver output signal anymore. This can save both area and power for the driver stage.

The simulation results in Figure 6-17 and Figure 6-19 describe the dead-time during the turn-on of M_P and M_N . It shows that the switching loss is minimized and less than 1.5-ns body-diode conduction is achieved for load current ranging from 10 mA to 500 mA.

To guarantee the performance of the proposed ASDTCD, the process, temperature effects is studied which and are illustrated in Figure 6-20 and Figure 6-21.

Figure 6-20 Simulation results at different corner and temperature during M_N turning on.

Figure 6-21 Simulation results at different corner and temperature during M_P turning on.

As shown in Figure 6-20 and Figure 6-21, the M_P gate control signal and M_N gate control signal will generate different rising and falling times at different corner and temperature. However, this will not affect the performance of the ASDTCD too much. The body diode conduction time is still less than 2ns even

at the worst temperature and corner condition. This is because the proposed ASDTCD utilize control the power transistor at the boundary of saturation and triode region, instead of have very accurate dead-time control. Thus, even the rising and falling edge of gate control signal is varied from temperature and process, the body-diode conduction time is still less than 2ns.

Furthermore, this proposed asymmetrical driver utilize the falling and rising edge of the gate control signal as dead time control generator, thus the tapering factor can be larger than 100, which means the area taken by the driver can be less the 1/100 of the area taken by power MOS. Hence, only 2 stage drivers are needed for power MOS M_P (24000 $\mu\text{m}/0.18 \mu\text{m}$) and M_N (8000 $\mu\text{m}/0.18 \mu\text{m}$). Conventionally, the size of the last stage driver is 1/3 that of the power transistor, but their numbers doubled that of the power transistors. This means that the switching loss at the last power stage drivers is 2/3 of the switching loss in the power transistor. If the switching loss in other driver stages are calculated, the total switching loss for driver stage is nearly the same as the power transistor. However, the proposed design utilizes small transistor in the driver stage to generate dead-time. The size of the last driver stage transistor is as small as 1/100 of the power transistor. Thus, the total switching loss is reduced by up to 50% compared to the conventional design. Furthermore, the area taken by the power stage is thus reduced by up to 50%. As power stage usually takes more than 80% of the total silicon area, the contribution of area saving for the system by utilizing the proposed driver can be up to 40%.

This can be seen from a comparison between the proposed design and the test bench shown in Figure 6-7. The result is shown in Figure 6-22.

Figure 6-22 Comparison between proposed design and an optimized dead-time.

Here, the compared test bench was driven by an ideal clock to generate 3.5 ns and 4 ns dead-time which is optimized for the 100 mA load range. It can be seen that, the proposed ASDTCD can provide an efficiency increase by nearly 2%. This only includes the power loss generated by the driver. However, if the conventional design want to generate the accurate 3.5 ns or 4 ns dead-time, both the body diode conduction detector and fast speed high gain amplifier are needed. If try to get nanosecond level resolution much more area and power will be consumed by the conventional adaptive dead time control circuit.

Additionally, the second stage of the driver has large aspect ratio. Thus, a dead time should be added to the second stage. The first stage driver still utilizes the same asymmetrical approach to generate the control signal for the second stage of the driver to eliminate the shoot through current of the second stage driver, as can be seen in Figure 6-15. A compact layout of the asymmetrical driver, which takes up merely 1% area of the power transistor, consuming only $29\ \mu\text{m} \times 23\ \mu\text{m}$ for the M_P driver and $21\ \mu\text{m} \times 14\ \mu\text{m}$ for the M_N driver, is shown in Figure 6-23.

Figure 6-23 Layout of the proposed ASDTCD.

6.2.1.3 Experimental Result for ASDTCD

The proposed asymmetrical dead-time control driver (ASDTCD) was fabricated in standard 0.18- μm CMOS process which layout is shown in and the micrograph for the chip is given in Figure 6-24.

Figure 6-24 Chip micrograph of proposed ASDTCD.

1.8-V supply voltage and 1-MHz clock are supplied to the test chip with 1.2-V output voltage. The testing board is shown in Figure 6-25.

Figure 6-25 Testing PCB for the proposed design.

As illustrated in Figure 6-26, Figure 6-28 and Figure 6-30, the proposed ASDTCD exhibits small switching loss and no body-diode conduction at 10-mA load. For a 450-mA load, the ASDTCD also have good performance, which can be observed in Figure 6-27, Figure 6-29, and Figure 6-31, where less than 3-ns body diode conduction time existed at 450-mA load. Here, the measured dead-time is a little longer than the simulation results. This is mainly due to the parasitic capacitance of pad, bonding wire, package, PCB trace, probe of oscilloscope, external inductor, etc..

Figure 6-26 Measured dead-time for chip1 at 10-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

Figure 6-27 Measured dead-time for chip1 at 450-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

Figure 6-28 Measured dead-time for chip2 at 10-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

Figure 6-29 Measured dead-time for chip2 at 450-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

Figure 6-30 Measured dead-time for chip3 at 10-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

Figure 6-31 Measured dead-time for chip3 at 450-mA load: (a) full range switch node V_X waveform; (b) falling edge waveform of V_X ; (c) rising edge waveform of V_X .

A higher than 97% peak efficiency can be observed in Figure 6-32. This efficiency is open loop efficiency which includes only ASDTCD and the two power transistors. It decreases linearly as the load current increase linearly, which is attributed to power loss of the unavoidable resistances in the power regulator—power transistors have about 200-m Ω turn-on resistance, inductor has 15-m Ω ESR resistance, bonding wire has about 40-m Ω resistance, package and PCB board have about 5-m Ω resistance, and the load capacitor has about 20-m Ω ESR resistance. Thus, the total resistance of the system is about 280 m Ω which will affect the efficiency decreasing linearly as load current increasing, as illustrated in Figure 6-32. If we assume the power regulator does not have these series resistances, the efficiency of the power regulator can be improved to that shown in Figure 6-33. The system has more than 99% efficiency over load range from 10 mA to 450 mA, which indicates that the body-diode conduction and switching loss of the power regulator are well controlled by the proposed ASDTCD. A comparison between the proposed design and some recently reported works is summarized in Table 6-3.

Figure 6-32 Measured power efficiency versus load current at $V_{IN} = 1.8V$.

Figure 6-33 Simulation results of the efficiency without parasitic resistance.

Table 6-3 Comparison between existing designs and the proposed design

Parameters	TCAS-II '10 [98]	TCAS-I '13 [48]	ESSCIRC '13 [99]	ESSCIRC '10 [8]	E. L. '10 [46]	This work
CMOS Technology (μm)	0.35	0.35	0.35	0.065	0.35	0.18
V_{IN} (V)	1.8-2.4	3.3	1.8-3	4	3.6	1.8
V_{OUT} (V)	1.5	1.5	1.5	1.8	1.8	1.2
Max. load (mA)	180	300	200	200	500	450
Switching frequency (MHz)	0.5	1	0.5	4	10	1
Peak efficiency (%)	91	90	94.6	N.A.	90	97.4 ^a
Body diode conduction time (ns)	20	5	5	4	4	< 1
Area (μm^2)	NA	NA	12390	N.A	N.A.	961

^aThis efficiency is open loop efficiency.

6.2.1.4 Summary

This section presents a new asymmetrical dead-time control driver (ASDTCD) for buck DC-DC power regulator. By controlling the slope of the driver output signal, the proposed ASDTCD can generate dead-time by the driver itself instead of additional dead-time generating circuit. Hence, the proposed dead-time control driver does not need strong capability to reduce delay, which thus result in much smaller power and area consumption compared to conventional dead-time control driver. Measured results demonstrate that our proposed ASDTCD can provide nearly ideal dead-time for buck regulator. Less than 1-ns body-diode conduction time can be observed at load current ranging from 10 mA to 450 mA. This proves that our body diode conduction controlling idea that utilizing the transition between triode region and saturation region to avoid

body diode conduction without bringing in shoot through current functions very well. More than 97% peak power efficiency is obtained which implies that, the proposed idea also have good performance in switching loss control.

6.2.2 Adaptive Dead-Time Control Driver

The proposed ASDTCD can save large amount of area while can still have short body diode conduction time for light load condition. To achieve a short body diode conduction time over wide load range, this is still need to be improved. Thus, an enhanced version dead-time control driver which can do adaptive dead-time control while consumes small area and power is describes in this sub-chapter. By utilizing a predictive idea for dead-time control the proposed adaptive can eliminate the delay for body diode conduction sensor or zero voltage detector. Such approach helps to lower down the power consumption of the system and improve the control accuracy of the dead-time. Unlike conventional predicting method which requires self-adjustment or tuning during testing, a threshold voltage is deployed as predictive information for dead-time control. Thus, the high gain amplifier used for prediction voltage detecting and adjusting circuit is no longer necessary. With the proposed prediction circuit, a less than 3-ns body diode conduction time with minimum switching loss are attained allowing high efficiency over wide load range. The proposed design is fabricated in 0.18- μm CMOS process. The adaptive dead-time driver design can be divided into two parts: power transistor M_P driver design and power transistor M_N driver design.

6.2.2.1 Dead-Time Control Driver for M_N

As is shown in Figure 6-1, the power transistor M_N will be turned on after M_P turns off. The M_N control therefore has two phases, M_N turns on and M_N turns off. The driver circuit for the M_N dead-time control is given in Figure 6-34.

Figure 6-34 Adaptive dead-time control driver for M_N .

Here, M_{PD1-7} and M_{ND1-6} are the driver buffer for power transistor M_N , R_{PD6} is the turn-on resistor for M_{PD6} , R_{ND4} is the turn-on resistor for M_{ND4} , C_{N_GS} and C_{N_GD} are parasitic capacitors of the power transistor M_N .

When PWM control signal changes from low to high, M_P turns off (to be analyzed later). M_{PD4} turns on, M_{ND6} turns off and V_X decreases. Attributing to the parasitic capacitor of power transistor, the V_X falling speed is much slower than M_P turns off. During this short interval, the current in the inductor can be assumed constant, which provides the charging and discharging current for the parasitic capacitor of the power transistor. After V_X is lower than the difference between the supply and threshold voltage of PMOS transistor, i.e. $V_{DD}-V_{TH_P}$, M_{PD6} and M_{ND4} turn on together. In order to lower down this shoot through current, M_{PD6} and M_{ND4} are chosen small W/L to increase the turn on resistance of R_{PD6} and R_{ND4} . To minimize switching loss, M_N must turn off at this moment, or else will short V_X to ground causing the wastage of energy stored in the parasitic capacitor. Here, M_{ND4} is chosen to be much larger than M_{PD6} allows R_{PD6} to be much larger than R_{ND4} . Thus, the node voltage of V_{D1} is smaller than the threshold voltage of NMOS transistor (V_{TH_N}). Thereafter, M_{PD5} is in off state and thus M_{PD6} , which guaranteed the power transistor M_N to be off at this interval. After V_X is lower than V_{TH_N} , M_{ND4} turns off and node voltage V_{D1} raises to V_{DD} , which turns on M_{ND5} and thus M_{PD5} . Hence, the parasitic capacitor C_{N_GD} is charged by M_{PD5} , while C_{N_GS} is discharged by M_{PD5} . When

the gate source voltage of M_N (V_{N_GS}) is higher than V_X , the paracitic capacitor C_{N_GS} will be reversely charged.

When V_{N_GS} is higher than V_{TH_N} , M_N turns on. In order to avoid body diode conduction for M_N , the turn on speed of M_N should be faster than V_X falling speed. Thus, M_{PD4} and M_{PD5} are chosen large W/L to lower their turn-on reistance. In order to minimize the swithching loss of the power transistor, the best turn on time for M_N is when V_X is zero. This helps to utilize all the energy stored in the parasitic capacitor of the power transistor instead of short them to ground through the power transistor M_N . But this is nearly impossible to be achieved. Thus, a comprimize must be done to avoid body diode conduction and minimize swithcing loss of the power transistor. Based on our proposed threshold voltage prediction idea, we can shorten the body diode conduction time while minimize the switching loss to a great extend by controlling the power transistor M_N turns on in the time range of V_X falling from V_{TH_N} to 0.

When PWM control signal changes from high to low, M_{ND6} turns on and M_{PD4} turns off. Thus, M_N turns off immediately and power transistor M_P begins to turn on.

Similar to M_N dead-time control, the dead-time control for M_P also has two phases, i.e. M_P turns on and M_P turns off phases. The driver circuit for M_P dead-time control is presented in Figure 6-35.

to zero and M_{P_DRIVE} decrease from V_{DD} to $V_{DD}-V_{TH_P}$ is nearly the same. Thus, M_P turns on before body diode conduction for M_N happens. As a result, body diode conduction for transistor M_N is avoided during M_P turning on. Furthermore, M_P turns on after M_N turns off. Thus, the shoot through current between the two power transistors M_P and M_N is avoided.

When the PWM control signal changes from low to high, M_{PD14} turns on, M_{ND18} turns off, the parasitic capacitor C_{P_GS} and C_{P_GD} are discharged by M_{PD14} , and M_{P_DRIVE} increases quickly to turn off M_P in a fast speed. V_X begins to fall after M_P turns off.

Thereafter, based on the proposed threshold voltage prediction idea, without using high speed zero voltage detection amplifier or body diode conduction sensor, body diode conduction time can be controlled to a short interval. Also, there is no shoot through current during transient of power transistors switching. Furthermore, the proposed prediction control method also helps in minimizing the switching loss of the power regulator.

6.2.2.2 Simulation Results

To guarantee performances across different corners, temperature, load current and supply voltage, the PVT simulation across 40mA to 1.1A load current were conducted for the proposed dynamic dead-time driver. The simulation results for M_N turning on are illustrated in Figure 6-36.

(a1)

(a2)

(b1)

(b2)

(c1)

(c2)

Figure 6-36 Simulation results of switching node V_x voltage during M_N turning on across PVT corners: (a1) typical corner at 3.2-V supply voltage, (a2) typical corner at 2.4-V supply voltage, (b1) slow corner at 3.2-V supply voltage, (b2) slow corner at 2.4-V supply voltage, (c1) fast corner at 3.2-V supply voltage, (c2) fast corner at 2.4-V supply voltage.

As shown in Figure 6-36, the PVT variation will affect the delay of both the M_P gate control signal and the M_N gate control signal. But, it will not affect the performance of the dead-time control driver. Even at the worst corner, there exists a less than 1-ns body diode conduction time for the power transistor. The dead-time control is still dominated by the load current as can be observed in Figure 6-37.

Figure 6-37 Simulation results of switching node V_X voltage during M_N turning on across load current varied from 40mA to 1.1A .

From Figure 6-37, it is clear that the power transistor M_N turns on when V_X reaches the threshold voltage V_{N_TH} at light load, but it is with some delay to result in short body diode conduction at heavy load. At light load, the parasitic capacitor charging and discharging speed is limited by the inductor current, which is much slower than the delay generated by the driver buffer. On the other hand, at heavy load, large inductor current will charge and discharge the parasitic capacitor in a fast speed. This is much faster than the delay generated by the buffer stage. Thus, the buffer stage will not respond fast enough to allow the power transistor M_N to turn on late and so, body diode conduction will happen.

Usually, this delay can be shorted by increasing the driving capability of the buffer stage. But, this will result in additional power and silicon area consumptions. Thus, a trade-off has to be done in optimizing the size ratio for the driver buffer stage. As observed in Figure 6-36, there is less than 1 ns body diode conduction time at 1-A load. This implies that, the driver capability is sufficient for the driver buffer stage. Simulation result for M_P turning on across PVT with load current varied from 40 mA to 1.1 A is shown in Figure 6-38.

(a1)

(a2)

(b1)

(b2)

(c1)

(c2)

Figure 6-38 Simulation results of switching node V_X voltage during M_N turning on across PVT corners: (a1) typical corner at 3.2-V supply voltage, (a2) typical corner at 2.4-V supply voltage, (b1) slow corner at 3.2-V supply voltage, (b2) slow corner at 2.4-V supply voltage, (c1) fast corner at 3.2-V supply voltage, (c2) fast corner at 2.4-V supply voltage.

As observed in Figure 6-38, the proposed adaptive dead-time control driver can control dead-time well to generate a less than 1-ns body diode conduction time even with PVT variations.

6.2.2.3 Experimental Results

The proposed adaptive dead-time control driver is embed in the buck power regulator and fabricated in 0.18- μm CMOS process. The chip is measured at 3.2-V supply voltage with load current varying from 40 mA to 1.1 A. The measurement result at 40-mA load and 1.1-A load is shown in Figure 6-39 and Figure 6-40, respectively.

Figure 6-39 Measurement results of adaptive dead-time control driver at 40-mA load.

Figure 6-40 Measurement results of proposed adaptive dead-time control driver at 1.1-A load.

Based on the proposed threshold voltage prediction idea, the designed adaptive dead-time control driver can predict the V_X voltage very well for light load condition. Nearly no body diode conduction can be observed at light load as illustrated in Figure 6-39. The short body diode conduction occurred at 1.1-A load current as shown in Figure 6-40. The body diode conduction time at 1.1-A load is longer than shown in the simulation result. This is because of the constitute capacitances of the pad, bonding wire, and PCB trace, which brings more delay to the dead-time control driver during M_N turning on. Hence, longer body diode conduction time can be observed in the measurement result. Even though the body diode conduction time is still less than 3 ns at 1.1-A load, it can be tolerated in the switching power regulator. These results verified that the proposed adaptive dead-time control driver has simple architecture, consumes small silicon area and can effectively control the dead-time according to load current. A comparison between the proposed adaptive dead-time driver and existing design is shown in Table 6-4.

Table 6-4 Comparison between the proposed ADPDT and existing design.

Parameters	TCAS-II '10 [98]	TCAS-I '13 [48]	ESSCIRC '13 [99]	ESSCIRC '10 [8]	E. L. '10 [46]	This work
CMOS Technology (μm)	0.35	0.35	0.35	0.065	0.35	0.18
V_{IN} (V)	1.8-2.4	3.3	1.8-3	4	3.6	2.4-3.2
V_{OUT} (V)	1.5	1.5	1.5	1.8	1.8	1.2
Max. load (mA)	180	300	200	200	500	1.1A
Switching frequency (MHz)	0.5	1	0.5	4	10	1.2
Body diode conduction time (ns)	20	5	5	4	4	<3

It can be seen in Table 6-4, the proposed adaptive dead-time control driver can control body diode conduction to be short over wider load range then the compared design.

6.2.2.4 Summary

This sub-chapter describes a threshold voltage prediction idea to enable adaptive dead-time control for the power transistor of the power regulator. Based on the proposed idea, the system has nearly no body diode conduction at light load and less than 3-ns body diode conduction time at 1.1-A load. Without bringing in shoot through current while minimizing switching loss, the adaptive dead-time control driver enable the system to achieve high efficiency over a wide load range.

Chapter 7 Adaptive Efficiency Power Regulator

To achieve the adaptive efficiency optimized power regulator (AEOPR), an efficiency tracking method is proposed to control the power regulator operating at the best efficiency point. Based on the proposed efficiency tracking method, the power regulator will adjust its power MOS size based on the efficiency of the power regulator instead of the load current. The power MOS size will be selected based on the best efficiency point for different loads and supply voltages. Embedding all the building blocks discussed in this thesis, the proposed AEOPR is fabricated using standard 0.18- μm CMOS process, occupying an area of 2 mm x 2 mm. By optimizing all the building blocks of the power regulator for the adaptive efficiency control method, the proposed AEOPR achieves more than 85% overall efficiency with load current varying from 70 mA to 1.1 A. The design of the efficiency tracker and whole power regulator result will be discussed in this chapter.

7.1 Efficiency Tracker Design

Unlike conventional adaptive power transistor size control method, the proposed adaptive efficiency optimized control method utilizes the efficiency information to track the best efficiency point of the power regulator. Thus, the selection of the power MOS size is a result of both the input voltage and load current instead of just the load current information to decide on the dimension of power MOS. This can be understood from the efficiency calculation equation shown below:

$$\eta = \frac{V_{OUT} I_{OUT}}{V_{IN} I_{IN}} \quad (7.1)$$

where η is the efficiency of the power regulator defined by the load power to input power ration, V_{OUT} is output voltage of the power regulator; I_{OUT} is load current of the power regulator, V_{IN} is supply voltage of the power regulator, I_{IN} is input current of the power regulator. For a fixed load, the output voltage and the load current are fixed, and this implies that the load power is also fixed. Hence, the efficiency of the power regulator is decided by the input power, the smallest

input power will ascertain the highest efficiency. Since the supply voltage is fixed for a short duration, the efficiency of the power regulator is decided by the input current. The smallest input current shall imply the highest efficiency. Through detecting the input current power regulator can attain the best efficiency point. The full range current sensor proposed in Chapter 5 is engaged here to detect the input current. After averaging, the input current is used as the efficiency tracking information for the efficiency tracker, whereby its structure is shown in Figure 7-1.

Figure 7-1 Proposed efficiency tracker.

Here, the CLK is generated from a ramp clock generator, to be divided by a frequency divider to generate a local clock for the efficiency tracker. V_{COMP} and V_{COMP_INV} are used as control signal to sample the input voltage V_{TRACK_IN} that is converted from the averaged input current. At every cycle, both MP_1 and MN_1 turn on, MP_{2-3} and MN_{2-3} turn off to control capacitor C_1 sample the input signal. At every half cycle, both MP_1 and MN_1 turn off, MP_{2-3} and MN_{2-3} turn on, controlling the sampled voltage to be transferred from capacitor C_1 to C_2 , and simultaneously, the capacitor C_3 is charged by the input signal. Thus, the comparator will do a comparison between the new V_{TRACK_IN} and old V_{TRACK_IN} to decide if efficiency has increased. If the voltage on C_3 is higher than C_2 , the size changing action of power MOS gets more power from the supply voltage. This then brings system efficiency down indicating that an incorrect size changing action have been done for the power MOS. With that, the JK latch will be reversed to control the counter changing to the opposite direction. If the voltage on C_3 is lower than C_2 , it implies that the size changing action of power MOS brings less power from the supply voltage to increase the efficiency of the

system. Thereafter, the size changing action of the power MOS is in the right direction and is to be maintained. Thus, the JK latch will not be reversed to control the counter continue the same operation. The efficiency tracker will maintain the operation until the best efficiency point is found and toggling the power MOS size at the best efficiency point. The detail control action can be interpreted in Figure 7-2.

Figure 7-2 Control logic for the efficiency tracker.

As can be seen in Figure 7-2, the control logic will forbid all power MOS shut down condition, as it will cause the power regulator to shut down. Also, the system also does not allow all power MOS to turn on at the same time and still increase the size of the power MOS. Because if the state for Q_{0-4} is 11111, and the counter is still increasing, next state for Q_{0-4} will be 00000, which will control all the power MOS to turn off together. Only Q_{0-3} are used to control the power MOS to do size adjustment. Q_4 , the most significant bit (MSB) is connected to a small power MOS that is always on to ensure that the system will not fall into the state of all power MOS are off. The simulation results of the efficiency tracker is prescribed in Figure 7-3.

Figure 7-3 Simulation result of MOS size selection at 3.2-V supply voltage.

It can be from seen in Figure 7-3 that the least significant bit (LSB) Q_0 is always toggling as is discussed earlier, the transistor size will toggle around the highest efficiency point. When load current is changing, the power transistor array will change its size towards the best efficiency point in a step by step manner. The supply voltage will also affect the size selection of the power MOS. This is because at different supply voltages, the PWM control signal has different duty cycle to affect the optimum size of the power MOS even with the same load current. This can be observed in Figure 7-4.

Figure 7-4 Simulation result of MOS size selection at 2.4-V supply voltage.

It can be seen in Figure 7-4 that at 2.4-V supply voltage, the control bit Q_2 and Q_3 waveform is different from the one at 3.2-V supply voltage. This proves that the proposed adaptive efficiency optimized method can track the best efficiency point to decide the power MOS size and not just relying on its load current.

7.2 Experimental Results

The proposed adaptive efficiency optimized power regulator is fabricated in 0.18- μm CMOS process with a silicon area of 2mm x 2 mm. The micrograph of the design is given in Figure 7-5.

Figure 7-5 Micrograph of the proposed AEOPR.

In Figure 7-5, the PMOS power transistor and NMOS power transistor are the power MOS array, M_P dead-time driver and M_N dead-time driver are driver array for the PMOS power transistor array and NMOS power transistor array, respectively. The BGR and I_{REF} blocks are bandgap voltage and current reference. The BUF block is inserted between BGR output and the several reference inputs to guarantee the performance of the reference voltage. The LDO block is used to provide internal supply voltage. The CS block is current sensor block to sensing the input current information. The EF_TR is efficiency tracker block for tracking the best efficiency point of the power regulator and for selecting the size of power MOS transistor. The fabricated chip is bonded to a QFP-52 package and soldered on the PCB as shown Figure 7-6.

Figure 7-6 Test PCB of the proposed AEOPR.

The test plan is summarized in Table 7-1.

Table 7-1 Test plan of the proposed AEOPR

Parameter	Name	Value	Unit
Input voltage	V_{IN}	2.4 – 3.2	V
Internal LDO output	V_{LDO}	1.8	V
Internal bandgap voltage reference	V_{BGR}	1.1	V
Internal current reference	I_{REF}	10	μA
Internal clock	CLK	1.2	MHz
Load	R_{LOAD}	1 – 50	Ω
Inductor	L	10	μH
Capacitor	C	10	μF

A 2.4-V to 3.2-V variable supply voltage is added to the testing chip. The bandgap and current reference testing results are presented earlier in Chapter 4. The dead-time control driver testing result has also been described in subsection 6.2.2. To show the efficiency improvement of the proposed efficiency tracking method, a comparison between using and not using efficiency tracker (EF_TR) is illustrated in Figure 7-7.

Figure 7-7 Measured efficiency of the proposed AEOPR.

Here, the EFTR means efficiency tracker. The compared efficiency curve was measured by disabling the efficiency tracker, all the power transistors turns on and the adaptive dead-time driver operating. Thus, only the effect of the efficiency tracker is studied. As demonstrated in Figure 7-7, the proposed AEOPR can achieve more than 5% efficiency improvement at light load. This is because enable all the power transistors is only for heavy load application. And more than 85% overall efficiency has been achieved across a load range varying of 70 mA to 1.1 A. With the help of proposed adaptive dead-time control driver, more than 95.1% peak efficiency is attained at 350-mA load with a 2.4-V supply voltage. There exists several peaks in the measured efficiency plot. This is because the efficiency tracker will adjust its power transistor size according to the best efficiency point, and will toggle at the best efficiency point. The power transistor size has its smallest transistor size step, which cannot guarantee the power regulator to work at the highest efficiency for every load. Thus, at some point, the transistor size will have to change, which then brings some valley and peak points at the efficiency plot of the power regulator. As seen in Figure 7-7, the peak efficiency at different supply voltage varies which is not just related to load current but also to the supply voltage.

The switching clock of the power regulator is generated from the internal ramp clock generator, with switching frequency is at about 1.2 MHz. Measurement

results show that the switching frequency is about 1.2255 MHz as shown in Figure 7-8.

Figure 7-8 Measured switching node wave form.

It can be seen from the switching node voltage at Figure 7-8 that the switching period of the power regulator is about 816 ns which is equal to a frequency of 1.2255 MHz frequency. This is a little different from the designed switching frequency caused by the process variation of the capacitor that controls the charging period of the power ramp signal. Thus, the clock frequency have a little variation.

The targeted output voltage is 1.2 V which is suited for supply voltage of nowadays popular process. The output voltage versus load current is illustrated in Figure 7-9.

Figure 7-9 Output voltage vs load current.

Figure 7-9 demonstrate that the output voltage has less than 2%/A load regulation across load current varying from 70 mA to 1.1 A, and less than 1%/V line regulation across input voltage varying from 2.4 V to 3.2V. A comparison between the proposed design and some existing designs is summarized in Table 1-1.

Table 7-2 Summary of existing power regulator designs

Parameters	Tran. P. E. '12 [100]	CICC '14 [101]	JSSC '07 [43]	TCAS-I '13 [48]	ESSCIRC '13 [99]	This Work
CMOS Technology (μm)	0.35	65	0.35	0.35	0.35	0.18
Input Voltage (V)	2.4 – 3.3	2.8, 3.3, 3.8	3.3	3.3	1.8 – 3.0	2.4 – 3.2
Output Voltage (V)	0.9 – 2.0	1.2, 1.8	1.65	1.5	1.5	1.2
Load Range (mA)	1050	589	0.1 – 500	40 – 320	1 – 200	70 – 1100
Switching Frequency (MHz)	0.2 – 2	1	1	1	0.5	1.2
Ripple (mV)	16	N. A.	<35	N. A.	N. A.	5
Line Regulation (%/V)	± 1.7	N. A.	N. A.	N. A.	N. A.	1
Load Regulation (mV/A)	200	N. A.	N. A.	N. A.	N. A.	30
Efficiency (%)	82 – 92.5	50 – 85	82 – 95	80 – 90	69 – 94.6	85 – 95
Inductor (μH)	2	10	4.7	N. A.	1	10
Capacitor (μF)	22	20	4.7	N. A.	6.8	10

As shown in Table 7-2, many design have been proposed for wide load range application. Ref. [50], [76], [77] utilize adaptive dead-time control method to

achieve high efficiency. However, this can only minimize switching loss, which cannot achieve high efficiency at heavy load. Ref. [75] utilize PFM method to optimize at light load, but have bad efficiency at heavy load. Ref. [43] utilizes adaptive power MOS size based on load current, which only applicable for fixed input and output voltage. Our proposed adaptive efficiency power regulator can adjust the power MOS size based the best efficiency point which can work at varied supply voltage and load current. As compared with other design the proposed AEOPR can work with wide input voltage and at wide load range, while still attaining high efficiency and good line regulation and load regulation.

7.3 Summary

This research proposes an efficiency tracking method to enable the power regulator to adjust the power MOS size to achieve high efficiency over a wide load range. The proposed AEOPR offers higher than 85% overall efficiency over load range varying from 70 mA to 1.1 A and can achieve 95.1% peak efficiency at 350-mA load with 2.4-V supply voltage. With all the building blocks embedded on the chip, the proposed AEOPR only needs one supply voltage that can varying from 2.4 V to 3.2 V without any out-chip biasing. The proposed AEOPR is therefore well suited for many industry application. With the embedded low TC BGR voltage reference and temperature independent current reference to compensate the PVT variation, the system can generate 1.2-V output voltage with less than 1%/A line regulation and less than 2%/V load regulation.

Chapter 8 Conclusion and Future Work

8.1 Conclusion

The preliminary work presented in this thesis is a complete structure of an adaptive efficiency prototype power regulator. The work includes circuit design, blocks optimization and system integration.

The bandgap voltage reference and current reference are important building blocks for power regulator as they set the quiescent condition for the power regulator. These reference circuits compensate the PVT variation of the circuit they are connected to guarantee stable performance for the entire system. This thesis has discussed the advantages and disadvantages of existing bandgap voltage references and proposed new low power bandgap voltage reference which can achieve $9.8 \text{ ppm}/^{\circ}\text{C}$ TC with only 200-nW of total power consumption. Next, a novel PVT compensated trim-free $10\text{-}\mu\text{A}$ current reference with $130 \text{ ppm}/^{\circ}\text{C}$ TC and less than $2\%/V$ line regulation is described. Following which, a merged structure bandgap voltage cum current reference circuit (BGVCR) with start-up free feature is proposed. The BGVCR can generate both the bandgap and current references at the same time. Without using additional start-up circuit, the proposed BGVCR can function well and achieves $5 \text{ ppm}/^{\circ}\text{C}$ TC for bandgap voltage reference and $150 \text{ ppm}/^{\circ}\text{C}$ TC for current reference.

The current sensing circuit is one of the most important blocks for the adaptive efficiency power regulator. Several current sensing topologies have been compared and the MOS current sensing topology is chosen for the benefits of attaining good accuracy and low power consumption. In addition, the advantages and disadvantages of the different MOS current sensing topologies have been discussed and analyzed in this thesis. Among the different types of MOS current sensing topology, the self-biased current sensing topology has the prominent merit of achieving high accuracy at heavy load condition and high efficiency at light load condition. Thus, an enhanced full range peak and valley current sensor for the buck regulator based on this topology is proposed. In this design, the control timing diagram of the current sensor must be carefully

designed to ensure stability of the current sensor. In-depth simulation and analysis have all been duly completed for this current sensor. The proposed full range current sensor has achieved higher than 93% and 96% sensing accuracy for the rising and falling edges, respectively.

There are a total of five different power losses related to the power stage of the power regulator. These are: switching, power MOS conduction, body diode conduction, shoot-through current and reverse current loss. The first four losses have been studied intensively in this thesis. And the reverse current will be discussed in future work part.

The switching and power MOS conduction losses are related to the aspect ratio of the power MOS transistor and both have been analyzed in this thesis. Also, a relationship between the aspect ratio of the power MOS transistor and the total power losses has been established. The turn-on resistance of the power MOS is also very sensitive to the metal routing. The power MOS occupies a large amount of silicon area due to its large aspect ratio. Hence, several layout drawing techniques have been evaluated. A new layout drawing method that makes full use of area and metal routing on the chip to achieve lower turn-on resistance and smaller area is thus proposed. With the help of the proposed power MOS metal routing method, the resistance of the power transistor routing metal is only 7 m Ω . The low resistive interconnect helps to minimize the conduction loss of the power regulator to a great extent.

The shoot through current and body diode conduction loss must be carefully controlled to prevent a large efficiency drop in the power regulator. In order to control the shoot through current and body diode conduction, a dead-time must be inserted during the turning on and off of the power MOS transistor. Several adaptive dead-time control methods have been discussed and compared in this thesis. The conventional adaptive dead-time control method usually needs high gain amplifier to sense the switching node voltage and small tapering factor to lower down the delay. Hence, it requires large amount of area and power. An asymmetrical dead-time control driver is proposed for light load application which can achieve less than 1-ns body diode conduction time across load range varying from 10 mA to 450 mA. An adaptive dead-time control driver for wide

load range application is also proposed in this thesis which can achieve less than 3-ns body diode conduction time across load current ranging from 70 mA to 1.1 A. The two proposed control driver are both sensor-less and do not require high gain amplifier to detect voltage. Both designs are able to achieve high efficiency for use in the power regulator. Furthermore, they have simple circuit structures to help them fit easily in any industry products.

PWM which is the most commonly adopted control modulation approach is engaged in this thesis. The basic theory of the PWM generator has been discussed. The high gain cascode amplifier is selected as error amplifier to guarantee the power regulator a stable output voltage. However, the bias circuit of the amplifier will greatly affect the power consumption and performance of the amplifier. A new bias structure is therefore proposed for the cascode error amplifier which helps the error amplifier attains more than 90-dB DC gain with 86° phase margin and less than 40- μ A current consumption.

In conventional wide load range application, segmented power MOS size is controlled by the load current. However, load current is not the only factor that can affect the efficiency of the power regulator since input voltage can also influence the efficiency of the power regulator. Thus, the same load current may require different segmented power MOS to attain a best efficiency. An efficiency tracking method is hence proposed to assist the power regulator with efficiency optimization. The segmented power MOS is controlled by the efficiency optimizing controller to find the highest efficiency point power MOS size when load current or input voltage is changing. The proposed adaptive efficiency optimized power regulator can track the best efficiency point as the power MOS size is being adjusted. Such unique feature aids the power regulator to achieve more than 85% efficiency over load range from 70 mA to 1.1A with supply voltage varying from 2.4 V to 3.2 V. And more than 95% peak efficiency has been achieved for the power regulator at 350-mA load current with 2.4-V supply voltage.

8.2 Suggestions for Future Work

8.2.1 Reverse Current Control

Reverse current contributes to huge power losses in the DCM if it is not controlled well. Normal reverse current control method is based on zero current detection circuit, which requires a very high gain and high speed comparator [49]. However, the high gain and high speed amplifier will consume a large chip area and power, which is power inefficient. Thus, a current prediction idea which can utilize the peak current information from the current sensor to predict the zero current point will be developed to control the reverse current. Hence, the prediction will be completed in one cycle instead of waiting till the next cycle. Based on this idea, high speed respond time is achieved without a high gain and high speed amplifier.

8.2.2 Low Voltage Mode for the Buck Converter

As discussed in Chapter 1, the normal output voltage for the LiFePO_4 battery is between 2.4 V and 3.2 V. If the battery output voltage is lower than 2.4 V, there should be some low power modes. In normal case, the standby mode circuit will not function. When supply voltage is lower than 2.4 V, the standby mode circuit will begin to work with low power feature with performance is not crucial. The BGR discussed in 4.3 will provide the low power BGR reference. When the supply voltage is higher than 2.4 V, the standby mode circuit will be disabled and all the other blocks for normal operating mode will be enabled.

8.2.3 DVS-Enabled Adaptive Efficiency Power Regulator

DVS/DVFS is no doubt a very important technology for power saving especially for a wide load range system. Hence, the proposed power regulator will incorporate DVS feature to achieve its best performance and to work at the lowest voltage level. Finally, the DVS based power regulator will be integrated with a DVS-enabled processor which is widely utilized in today's portable devices.

Author's Publications

Conferences:

Chundong Wu, Wang Ling Goh, Chiang Liang Kok, Wanlan Yang, Liter Siek, "A low TC, supply independent and process compensated current reference", in IEEE Custom Integrated Circuits Conference (CICC), 2015, pp. 1-4.

Chundong Wu, Wang Ling Goh, Yongkui Yang, Alan Chang, Xi Zhu and Lei Wang, "A Start-Up Free 200nW Bandgap Voltage Reference", in 14th IEEE International NEWCAS Conference, Jun. 2016, (accepted).

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