A CMOS power amplifier in nanometer technology for portable applications

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**A CMOS POWER AMPLIFIER IN NANOMETER
TECHNOLOGY FOR PORTABLE APPLICATIONS**

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**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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**A CMOS Power Amplifier in Nanometer Technology
for Portable Applications**

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Table of Contents

ACKNOWLEDGMENT.....	I
TABLE OF CONTENTS.....	II
ABSTRACT.....	IV
LIST OF FIGURES	VI
LIST OF TABLES	IX
LIST OF GLOSSARY	X
CHAPTER 1 INTRODUCTION	1
1.1. Motivations	1
1.2. Objectives	4
1.3. Contributions	5
1.4. Organizations.....	6
CHAPTER 2 LITERATURE REVIEW	7
2.1. Introduction.....	7
2.2. Review of Class-AB Audio Power Amplifier	9
2.2.1. Dhanasekaran's Circuit [3].....	11
2.2.2. Mohan's Circuit [5].....	14
2.3. Review of Low Offset Techniques	18
2.3.1. Yu's Circuit [28]	21
2.4. Review of Frequency Compensation Techniques	25
CHAPTER 3 ARCHITECTURE AND CIRCUIT DESIGN.....	30
3.1. Proposed Digitally-Assisted Offset Calibration Circuit	30
3.1.1. Architecture of Proposed Digitally-Assisted Low-offset Headphone Amplifier	30
3.1.2. Transistor Level of Digitally-Assisted Offset Calibration Circuit	34
3.1.2.1. Balanced Offset Compensation Current Injection Circuit	34
3.1.2.2. Other Circuit Blocks of the Offset Calibration Circuit.....	37
3.1.3. Influence of Input-offset, Temperature and Power Transistors Leakage Current on Quiescent Power Consumption of Headphone Amplifier.....	42
3.1.4. Advantages of Balanced Low-impedance Node Current Injection Circuit..	45
3.2. Proposed Frequency Compensation Topology	47
3.3. Transistor Level Realization of Headphone Amplifier	55

3.3.1. Realization of Input Stage of Headphone Amplifier.....	55
3.3.2. Realization of Second Stage of Headphone Amplifier	57
3.3.3. Realization of Output Stage of Headphone Amplifier	59
3.3.4. CLM-Reduced Class-AB Bias Generation Circuit	60
3.3.5. Bias Generation and Start-up Circuit	68
3.4. Noise Analysis of Proposed Headphone Amplifier.....	71
CHAPTER 4 MEASURED RESULTS AND DISCUSSIONS.....	74
4.1. Measured Input-referred Offset and Quiescent Power	76
4.2. Measured THD+N and SNR Results	78
4.3. Measured PSRR Results	80
4.4. Measured Pulse Response.....	81
4.5. Performance Comparison	83
CHAPTER 5 CONCLUSIONS AND FUTURE WORKS.....	85
5.1. Conclusions	85
5.2. Future Work.....	86
AUTHOR'S PUBLICATION.....	87
REFERENCES	88

Abstract

In recent years, the demand for the battery-powered devices has been increasing rapidly. At the same time, the requirements for the audio power amplifier (APA) also extend to hi-fi quality music playback. In order to achieve high run time per charge for the portable devices, the quiescent power consumption of APA should be made as low as possible. As such, the quiescent power consumption, harmonic distortion and dynamic range become the most significant performance parameters in the design of high-performance headphone amplifiers. Compared to the class-D amplifier, class-AB amplifier has the key advantages of high PSRR, low THD+N, no switching noise and no electro-magnetic interference.

In this thesis, a low-quiescent class-AB headphone driver, which is powered by dual supplies of $\pm 1V$, is presented and analyzed. Due to the small resistive load of APA, the mismatch-induced quiescent current caused by the input-referred offset voltage becomes a significant effect on the quiescent power consumption. It is evident that the mismatch-induced quiescent current of APA will be substantially increased with the increase of amplifier offset. A new balanced offset compensation current approach is presented. Through the aid of digitally-assisted calibration design, the input-referred offset can be substantially reduced while avoiding the unnecessary increase of quiescent power. Since the compensation current is injected into the low impedance nodes of the front-end gain stage, there is no significant degradation in terms of DC gain and power supply rejection ratio (PSRR) of the amplifier. This has demonstrated the robustness of calibration circuit.

An improved compensation technique called NMCFNR2, which is the Type-II implementation of nested Miller compensation with feedforward and nulling resistor (NMCFNR) amplifier, is proposed. It offers the technical advantages of simplicity as well as low-quiescent operation. Besides, the modified frequency compensation permits the APA to drive the worst-case load of $16\Omega//2nF$ whilst sustaining good stability and offering good and balanced performance metrics.

Together with the channel-length modulation (CLM) reduced class-AB bias generation circuit dedicated to the push-pull output stage, the auto-calibrated APA will reduce the input-referred offset of amplifier down to about $85\mu V$ while the total quiescent power is only $0.4mW$ and the GBW is of about $1.78 MHz$. The APA can deliver a peak power of $35mW$ ($1.5V_{pp}$ swing) to the worse case load of ($16\Omega//2nF$) with $-89dB$ THD+N and $93.5dB$ SNR. The extensive measurement results have suggested that the proposed amplifier has achieved the best Figure-of-Merit $FOM1 = (\text{Peak load power}/\text{Quiescent power})$ and the best $FOM2 = [\text{Peak load power}/\text{Quiescent power} * (\text{THD+N})\%]$ when compared with other representative state-of-the-art works.

List of Figures

Figure 1.1 The configuration of headphone amplifier with differential inputs and input-referred offset in DC-coupled topology.	2
Figure 2.1 A two-stage class-AB audio power amplifier with folded-cascode input stage and conventional bias generation circuit.	9
Figure 2.2 Transistor level of the 16Ω driver proposed by Dhanasekaran [3].	12
Figure 2.3 The circuit concept of the compensation scheme proposed by Dhanasekaran [3].	13
Figure 2.4 Architecture of the three-stage audio power amplifier proposed by Mohan [5].	14
Figure 2.5 Simplified schematic of PMOS input fully differential amplifier implemented in the second stage proposed by Mohan [5].	15
Figure 2.6 The architecture of a chopped amplifier.	18
Figure 2.7 Concept of offset calibration circuit proposed in [28].	20
Figure 2.8 Topology of ping-pong operational amplifier proposed in [28].	21
Figure 2.9 Offset adjustable two-stage CMOS op-amp with a programmable current mirror proposed by Yu [28].	23
Figure 2.10 Topology of three-stage NMC amplifier [37].	25
Figure 2.11 Topology of three-stage NMCFNR amplifier [51].	28
Figure 3.1 The headphone amplifier with the proposed digitally-assisted offset calibration circuit.	31
Figure 3.2 Simulated transient response of the important signals in the offset calibration system.	33
Figure 3.3 Concept of balanced offset compensation current injected into differential input stage.	34
Figure 3.4 Transistor level of four current sources for balanced current injection.	35
Figure 3.5 Power-on reset circuit.	38
Figure 3.6 Transient response of the power-on reset circuit when the amplifier starts up.	38
Figure 3.7 Zero-crossing detection logic.	39
Figure 3.8 Transient responses of the signals in zero-crossing detection logic.	40

Figure 3.9 The quiescent power consumption of proposed power amplifier under different temperature and input-referred offset voltage.....	43
Figure 3.10 Temperature variation of power transistors leakage current with in different corners.....	44
Figure 3.11 Comparative simulation results of PSRR for the current injection offset compensation amplifier and the benchmark headphone amplifier: (a) using proposed balanced low-impedance node injection circuit, (b) using single-ended high-impedance node injection circuit.....	46
Figure 3.12 Topology of proposed three-stage NMCFNR2 amplifier.	47
Figure 3.13 Simulated open-loop gain and phase with different nulling resistors for (a) NMCFNR2 amplifier and (b) NMCFNR amplifier.	49
Figure 3.14 Process Monte Carlo histograms for phase and gain margins with the respective load of $16\Omega//0pF$ and $16\Omega//2nF$	52
Figure 3.15 Simulated PM for $R_L=16\Omega$, 32Ω and 50Ω when sweeping the C_L from $0pF$ to $2nF$	53
Figure 3.16 The approximated headphone impedance model [69].....	54
Figure 3.17 The simulated open-loop gain and phase for headphone amplifier using the approximated headphone impedance load model.	54
Figure 3.18 The simplified schematic of the APA with embodiment of proposed balanced offset compensation circuit and CLM-reduced class-AB bias generation circuit.	56
Figure 3.19 Illustration of biasing current flow in one of floating biasing transistors when the output voltage of APA goes positive.....	58
Figure 3.20 CLM-reduced class-AB bias generation circuit.	61
Figure 3.21 Monte Carlo simulation results for offset current using the CLM-reduced bias generation circuit.	62
Figure 3.22 Monte Carlo simulation results for offset current using the conventional bias generation circuit.	62
Figure 3.23 The schematic of APA with high-voltage CLM-reduced bias generation circuit in $\pm 1.5V$ supply.	64
Figure 3.24 Monte Carlo simulation for offset current using the high-voltage CLM-reduced bias generation circuit with $\pm 1.5V$ supply.	65

Figure 3.25 Monte Carlo simulation for offset current using the conventional high-voltage bias generation circuit with $\pm 1.5V$ supply.	66
Figure 3.26 The total quiescent power versus the input offset of amplifier under two different biasing circuits.	66
Figure 3.27 Constant transconductance bias circuit with startup circuit.	68
Figure 3.28 The temperature variation of DC current for bias circuit.	69
Figure 3.29 The folded-cascode stage of the proposed headphone amplifier.....	71
Figure 3.30 Input-referred noise of amplifier versus the input pair channel length.	73
Figure 4.1 The micrograph of the proposed headphone amplifier in 65-nm CMOS.....	74
Figure 4.2 The Cadence layout drawing of the proposed headphone amplifier in UMC 65-nm CMOS.....	75
Figure 4.3 Measured input-referred offset of ten chips with/without offset calibration..	76
Figure 4.4 Measured quiescent power consumption of ten chips with/without offset calibration.	77
Figure 4.5 Measured output signal in FFT with the $1.5V_{PP}$ 1 kHz input sinusoidal wave.	78
Figure 4.6 Measured THD+N versus output amplitude for 1 kHz input signal.	79
Figure 4.7 Measured THD+N versus signal frequency with $1.5V_{PP}$ input sine-wave signal.	79
Figure 4.8 Measured PSRR+ at 217Hz with $700mV_{PP}$ on the 1V positive supply.....	80
Figure 4.9 Measured PSRR- at 217Hz with $700mV_{PP}$ on the 1V negative supply.....	80
Figure 4.10. Measurement result of a rectangular input waveforms of 50kHz and 500mV with the load of $1nF//16\Omega$	81
Figure 4.11 The pulse response of the headphone amplifier with the respective load of $16\Omega//8pF$, $16\Omega//300pF$, $16\Omega//1nF$ and $16\Omega//2nF$	82

List of Tables

Table 3.1 The Offset-induced Quiescent Power Consumption Study of Headphone Amplifier..... 42

Table 3.2 Comparison of poles and zeros for two frequency compensation techniques . 51

Table 3.3 Comparison of APAs with the conventional biasing circuit and the improved biasing circuit for the push-pull output stage..... 67

Table 4.1 Performance comparison of reported prior-art results. 84

List of Glossary

APA	Audio Power Amplifier
CLM	Channel Length Modulation
CMFB	Common Mode Feedback
Cox	Gate Oxide Capacitance
DAC	Digital to Analog Converter
DFCFC	Damping Factor Control Frequency Compensation
FFT	Fast Fourier Transform
FOM	Figure of Merit
GBW	Gain Bandwidth Product
K_{Fn}	Flicker Noise coefficient for NMOS
K_{Fp}	Flicker Noise coefficient for PMOS
LDO	Low Dropout
LHP	Left-Hand Plane
LPF	Low Pass Filter
LSB	Least Significant Bit
MNMC	Multipath Nested Miller Compensation
MSB	Most Significant Bit
NMC	Nested Miller Compensation
NMCFNR	Nested Miller Compensation with Feedforward Stage and Nulling Resistor
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PoR	Power-on Reset

PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
RHP	Right-Hand Plane
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion and Noise
UGF	Unity Gain Frequency
hi-fi	high-fidelity
<i>k</i>	Boltzmann Constant
<i>μ</i>	Mobility Carrier

Chapter 1 Introduction

1.1. Motivations

For the past few years, the development of portable mobile devices has led to the requirement for more features such as low-power consumption and high integration. With the rapid development of smartphones in recent years, it has demonstrated sophisticated features. As one of the most important components in headphone, audio power amplifiers (APA) are widely used in music player, video player and hand-free calls. Therefore, the high performance audio power amplifiers will be another demand in research. Total harmonic distortion (THD), signal-to-noise ratio (SNR) and power supply rejection ratio (PSRR) are the key parameters that qualify the performance metrics of an audio power amplifier. Meanwhile, the total quiescent power consumption of amplifier should be minimized for the purpose of extending the service life of battery [1].

Class-AB power amplifier is one of common architectures which is regularly used in the design of headphone amplifier [2]–[8]. It has some technical advantages over other types of power amplifiers. Compared to the switching amplifier (i.e., class-D amplifier), the linear amplifier can achieve high PSRR, low total harmonic distortion plus noise (THD+N), no switching noise and no electro-magnetic interference [9]–[11] whilst featuring with low power attribute. Therefore, the class-AB topology will be suitable for the low-quiescent high performance headphone amplifier design. In order to achieve a fully integrated circuit, a DC-coupled topology is applied. The example is shown in Fig. 1.1.

Figure 1.1 The configuration of headphone amplifier with differential inputs and input-referred offset in DC-coupled topology.

Although class-AB power amplifiers can achieve high performance with less quiescent power, there are several factors that may degrade the quiescent power in class-AB headphone amplifiers.

Firstly, the input-referred offset for a DC-coupled power amplifier will have a mismatch-induced quiescent current up to hundreds of μA , which is undesirable for a low-power design. With the continual decrease in device sizes, the input-referred offset becomes larger due to the random mismatch in the differential input stage. Refer to Fig. 1.1, in the presence of input-referred offset, the output voltage is obtained as

$$V_{OUT} = \frac{R_2 + R_4}{R_1 + R_3} (V_{IN+} - V_{IN-}) - \left(\frac{R_2 + R_4}{R_1 + R_3} + 1 \right) V_{OFF} \quad (1.1)$$

where the symbols have their usual meanings. When the four resistors are assumed identical in design, the input offset will be amplified by two times.

Secondly, the continual decrease in device sizes and supply voltage in nanometer CMOS technologies will cause the decrease of per-stage gain. As a result, multistage

amplifier topologies are required to achieve sufficient DC gain and linearity. Since the headphone amplifiers should be able to drive the cable capacitance with at least few hundreds of pF or above [12]–[14], the frequency compensation technique must guarantee the stability of headphone amplifier in the context of low resistive load in parallel with high capacitive load. Due to this reason, the frequency compensation becomes crucial because it directly affects the quiescent power of the amplifier for given bandwidth in design. In addition, since the output stage accounts for the majority of the quiescent power in the amplifier, the total quiescent power may increase a lot if the output stage is not well controlled by the bias generation circuit. Several circuit techniques will be proposed in this project to design a low-quiescent power class-AB headphone amplifier. They permit the total harmonic distortion better than or at least comparable to the recently-published works. More importantly, the best Figure-of-Merit (FOM) pertaining to the ratio of peak load power to quiescent power is obtained.

1.2. Objectives

The objectives of this thesis are given as follows:

- (i) To investigate a low offset calibration circuit to eliminate the mismatch-induced current in the headphone amplifier without degrading other performance metrics;
- (ii) To conduct the small-signal analysis of headphone amplifier and devising an improved frequency compensation to drive hundreds of pF capacitive load with good power-bandwidth efficiency;
- (iii) To exploit an improved class-AB bias generation circuit to control the quiescent current of the output stage;
- (iv) To conduct the measurement of the test chips which are fabricated using UMC 65nm CMOS technology.

1.3. Contributions

The main contributions of the research work are summarized as follows:

- (i) By proposing a new offset calibration circuit to reduce the input-referred offset and the mismatch-induced current of headphone amplifier, the input-referred offset can be less than $85\mu\text{V}$ whilst the other performance metrics of headphone amplifier are not degraded.
- (ii) By investigating an improved frequency compensation topology applicable for low-resistive and high-capacitive load driven power amplifier, the compensation technique permits the headphone amplifier to drive a capacitive load range of 0-2nF with good power-bandwidth efficiency.
- (iii) By designing a low-quiescent power class-AB headphone amplifier with dedicated class-AB output stage bias generation circuit, the headphone amplifier consumes lower power than the recently-published state-of-art works whilst offering good power-bandwidth and comparable performance metrics such as THD+N, SNR and PSRR.

1.4. Organizations

This thesis consists of six chapters as follows.

Chapter one introduces the background and defines the objectives as well as the main contributions of the thesis.

Chapter two reviews the representative class-AB headphone amplifier circuit, low-offset design techniques, multistage amplifier frequency compensation techniques and the recently-published state-of-the-art works. These will serve as the benchmarks for this project.

Chapter three describes the design procedures and design considerations pertaining to the proposed headphone amplifier. The working principle of circuit design techniques are discussed and analysed in details.

Chapter four presents the extensive measurement results and discusses the performance aspects of the circuit and the performance comparison with the recently-published state-of-art works, demonstrating the effectiveness of the amplifier.

Chapter five gives the concluding remarks and the recommendations for future improvements.

Chapter 2 Literature Review

The conventional class-AB headphone amplifier design techniques and low-offset circuit techniques will be reviewed in this chapter. The working principle of the recently-published works will be studied and discussed. This is then followed by the discussion of the representative multistage amplifier frequency compensation topologies.

2.1. Introduction

The audio power amplifier is widely used in our daily life. It is used to amplify the low-power audio signal which is in the frequency range of 20-20kHz to drive a loudspeaker. It is widely used in public address systems, home stereo system and concert sound reinforcement systems. Headphone amplifier is an audio power amplifier that is usually used in the portable devices. While the requirements for the headphone amplifier are different from other audio systems, especially the quiescent power consumption for the portable headphone amplifier should be made preferably low whenever possible.

For DC-coupled headphone amplifier, the input offset will be amplified. It induces the offset mismatch-induced current at the output node [15]–[17]. Input offset voltage becomes a significant problem for headphone amplifier when decreasing the total quiescent power consumption is one of primary design objectives. This is mainly because the mismatch-induced quiescent current caused by the input offset voltage tends to be very high if the offset of amplifier is not effectively nulled. Besides, the use of small transistor sizes will degrade the offset performance due to the increase of

random mismatches as well as the channel length modulation effect in nanometer CMOS technology. This may not be mitigated by only layout strategies. Therefore, the offset metric is an important parameter for the headphone amplifier. In order to achieve high-precision amplifiers, three different offset cancellation techniques can be implemented. They are chopping technique, auto-zeroing technique and trimming technique. Chopping and auto-zeroing techniques are common dynamic approaches that they can effectively reduce the offset of amplifiers. Some exemplary dynamic offset cancellation circuits have been reported in [18]–[27]. However, the big power filtering becomes the challenging issue for these techniques to be applied in APA design. Turning to the trimming technique, it is regarded as a static approach through which the input offset is usually calibrated before the main circuit start working. Several offset trimming circuits have been reported in [28]–[36]. This becomes the key focus of this work.

Consider the frequency compensation techniques for the multistage headphone amplifiers, they are similar to that of the capacitive driven op-amp. However, the main issue is that the different types of driven load have caused significant impact on the effectiveness of frequency compensation. A lot of works [37]–[66] are reported on the frequency compensation circuit techniques which are used to stabilize the multistage amplifiers whilst improving the power-bandwidth efficiency. In order to explore the appropriate frequency compensation techniques for use in the headphone amplifier, several representative works [37]–[66] will be reviewed in this chapter.

2.2. Review of Class-AB Audio Power Amplifier

Class-AB headphone amplifier has been widely implemented in many recently-published works [2]–[8]. Most of the architectures in these works are largely based on two-stage or three-stage design.

Figure 2.1 A two-stage class-AB audio power amplifier with folded-cascode input stage and conventional bias generation circuit.

A high-gain APA topology can be configured as shown in Fig. 2.1, which is a two-stage design. It features a high gain folded-cascode input stage and an inverting push-pull output stage. Frequency compensation can be achieved by means of Miller compensation. Refer to the two-stage amplifier example in Fig. 2.1, the output stage biasing circuit makes use of conventional bias generation circuit [67] to bias the NMOS output transistor by two diode-connected transistors having the gate-source tracking relationship that $V_{GSN'} = V_{GSN}$ and $V_{GSM8'} = V_{GSM8}$. However, it suffers from the problem that the drain-source voltage of the replica transistor $M_{N'}$ is different from that of the output transistor M_N . In addition, due to the high-drive requirement, the channel

length of output transistor M_N is made small, and hence its replica M_N' follows the same for tracking reason. As a consequence, the channel length modulation effect becomes a serious problem because this leads to the current matching issue between the bias generation circuit and the output stage. The same goes for PMOS counterpart.

In order to achieve sufficiently high gain, most of audio power amplifiers are three-stage topology [2]–[7]. It is common to see that the same bias generation circuit of Fig. 2.1 is utilized in [3], [7], [8]. In a general three-stage audio power amplifier, the first stage is a differential high-gain stage. The output node of the first stage usually defines the dominant pole of audio power amplifier. The cascode configuration can provide high DC gain and high input common mode level. To further increase the gain, the regulated cascode configuration [2] can be applied. Besides, the folded cascode configuration is commonly used as the front-end stage in other audio power amplifiers [3], [8]. Regarding the second gain stage, it is usually achieved with the non-inverting gain topology having the current mirror active load. It stems from that the fact it permits the ease with the use of Miller frequency compensation for the last inverting driving stage. Finally, the third gain stage consists of an NMOS and PMOS to form the push-pull structure to provide sufficient driving current to the resistive load. Unfortunately, all the reported works [2]–[8] may exhibit high quiescent current in the topologies. To stabilize a three-stage circuit architecture with minimum quiescent current, an effective frequency compensation technique is required in the design of headphone amplifier.

In view of these pitfalls, the bias generation circuit and frequency compensation technique are needed to be explored.

2.2.1. Dhanasekaran's Circuit [3]

Of the performance metrics for headphone amplifiers, the quiescent power consumption, THD+N, PSRR and SNR are identified as the important parameters. Many studies of the class-AB headphone amplifiers are focused on these metrics.

Dhanasekaran presents a class-AB headphone amplifier in 0.13 μ m technology. It can drive 1pF to 22nF capacitive load and achieve -84.8dB THD while consuming a power of 1.2mW [3]. Fig. 2.2 shows the transistor level of Dhanasekaran's headphone amplifier circuit which employs a folded-cascode topology as the input differential stage, a non-inverting second gain stage with current mirror as active load and a push-pull output stage. For the output stage, the conventional floating bias network for push-pull output stage is applied.

Dhanasekaran suggests the frequency compensation scheme which can adjust the damping factor automatically according to the load capacitance. Most of the three-stage frequency compensation techniques are based on Miller compensation, in which the value of damping factor determines the stability of the circuit [50]. Since the damping factor of a nested Miller compensated (NMC) amplifier is inversely proportional to $\sqrt{C_L}$, it can only drive small capacitive load. On the contrary, the damping factor of a damping factor control frequency compensated (DFCFC) amplifier is proportional to $\sqrt{C_L}$. This means that it is suitable for large capacitive load. In order to handle wide range of capacitive load, Dhanasekaran presents a three-stage amplifier with approximately constant damping factor based on DFCFC and NMC, which is illustrated in Fig. 2.3. Since the damping factor of DFCFC is proportional to $G_{mD}\sqrt{C_L}$, an approximately constant damping factor can be achieved if

Figure 2.2 Transistor level of the 16Ω driver proposed by Dhanasekaran [3].

I/G_{mD} can be replaced with a resistor that is proportional to $\sqrt{C_L}$. The equivalent damping resistance R_{D1} due to C_{D2} and G_{m3} becomes

$$R_{D1} = \frac{C_L}{G_{m3} * C_{D2}} \quad (2.1)$$

The total damping resistance of amplifier is given as

$$R_D = R_{D1} \parallel \frac{1}{G_{mD}} \quad (2.2)$$

where G_{mD} is the transconductance of transistor M_5 or M_6 . The resulting damping resistance is approximately proportional to $\sqrt{C_L}$ so that the proposed amplifier is able to drive wide range of capacitive load.

Figure 2.3 The circuit concept of the compensation scheme proposed by Dhanasekaran [3].

However, the circuit architecture will consume extra quiescent power consumption by the active damping stage and the input-referred offset arising from the mismatches in the amplifier.

2.2.2. Mohan's Circuit [5]

The conventional class-AB power amplifier topology shown in Fig. 2.1 is one of the most popular topologies in the implementation of class-AB headphone amplifier. The circuit proposed in [5] applies fully differential internal stages to achieve relatively high output swing and cancel the even-order harmonics. Multiple compensation networks are adopted to guarantee the stability when driving the capacitive load range of 10pF ~ 5nF. The peak load power of the reported headphone amplifier delivered to the 16 Ω resistive load is 93.8mW. The peak THD+N is obtained as -77.9dB.

Figure 2.4 Architecture of the three-stage audio power amplifier proposed by Mohan [5].

Figure 2.5 Simplified schematic of PMOS input fully differential amplifier implemented in the second stage proposed by Mohan [5].

Fig. 2.4 shows the architecture of the reported headphone amplifier in [5]. The outputs of the first fully differential stage are Vo1+ and Vo1-, which have the common mode voltage of 0V. In the fully differential amplifier shown in Fig. 2.5, the first amplifier serves as the input differential amplifier whereas the second amplifier provides the feedback function. There are two fully differential amplifiers implemented in the second stage, with PMOS input pair as shown in Fig. 2.5 and an NMOS counterpart to drive the N-type and P-type output transistors in the output stage, respectively. This architecture can provide same gains and poles frequency at the output nodes of the second stage. The two resistors R_2 and the transistors M_9 - M_{14} in the circuit form the common mode feedback (CMFB) networks. The common mode output voltage of the fully differential stage is determined by the reference voltage V_R in the second

feedback amplifier. The common mode output control voltage in the second amplifier is in turn determined by the cascode current source M_{17} – M_{18} and the replica transistor M_{RN} . Under quiescent condition, the voltage of V_{o2P+} and V_{o2P-} should be made close to that of V_R . Since V_{o2P+} is the gate voltage of N-type output power transistor M_N in the inverting gain stage, $-A_{3N}$, as illustrated in Fig. 2.4, the quiescent current of third stage becomes

$$I_3 = \frac{\left(\frac{W}{L}\right)_{M_N}}{\left(\frac{W}{L}\right)_{M_{RN}}} I_B \quad (2.3)$$

The frequency compensation circuit of this amplifier is realized by three Miller compensation networks as depicted in Fig. 2.4. The frequency compensation technique is similar to the reversed nested Miller compensation except for the application of Miller capacitors C_{C3} which are used to achieve the same pole frequency for the P-type and N-type differential amplifiers in the second stage. In addition, in order to make sure that the poles frequency at the two output nodes of second stage are the same, the local CMFB network resistors in the PMOS input fully differential amplifier are set to be $R_2/2$.

With the second stage differential implementation and three Miller compensation networks, the audio power amplifier [5] has achieved moderate THD+N, low quiescent power and high FOM, which is defined as the ratio of peak load power over quiescent power. Meanwhile, this amplifier can drive a capacitive load range of 10pF ~ 5nF with the total Miller compensation capacitances of only 16.3pF. However, there are still some limitations in the work. Firstly, the DC gain of the fully differential amplifiers

are limited by the resistors, which are used in the common mode feedback circuits. Secondly, based on the fact that the channel length of output transistor is set to be small to sink or source large DC current, the channel length modulation effect will lead to large current mismatch in the last stage. It means that the quiescent current of the output stage cannot be well defined. Lastly, the fully differential amplifiers double the area of the first two stages.

2.3. Review of Low Offset Techniques

Offset and flicker noise are the dominant error sources for operational amplifiers, especially for CMOS technology. The works proposed in [18]-[36] present many different circuit techniques to minimize the offset of amplifiers or ADCs. Most of the circuit techniques can be classified into the two types of offset cancellation technique: dynamic offset cancellation technique and static offset calibration technique. Chopping and auto-zeroing techniques are the two types of dynamic approaches to reduce the offset continuously and discrete time, respectively.

Fig. 2.6 shows the architecture of a chopped amplifier. Firstly, the input signal is modulated by a chopper at a clock frequency of f_{ch} . Then the modulated signal will be amplified by the amplifier together with the input offset. The output of the amplifier is then modulated by the second chopper so that the amplified input signal can be demodulated back to DC whilst the offset will be modulated to the odd harmonics of f_{ch} . The low-pass filter (LPF) removes the unwanted high-frequency signal. As a result, it leads to an amplified signal without offset.

Figure 2.6 The architecture of a chopped amplifier.

Although the dynamic offset cancellation circuit can reduce the offset down to microvolt level, it tends to increase the circuit complexity, resulting in the spurious signals at the amplifiers' output. For audio power amplifiers, they are not feasible

because of the need of external filter to handle big power. The same goes for the sampled-data based dynamic offset cancellation technique. Therefore, the static trimming offset cancellation technique becomes more suitable for the audio power amplifier to achieve low-quiescent power despite of the fact that it is usually implemented in production at the expense of increased test cost due to the additional trimming procedures.

Many state-of-the-art works are reported in [28]–[36] to provide the suitable offset trimming techniques to reduce the input offset. Voltage control and current control are two commonly-used trimming approaches which have been adopted to reduce the input offset. The application of current control is found in [28], [29], [33] whereas that of the voltage control is found in [30]–[32], [34]–[36]. The bulk voltage trimming offset cancellation adjusts the bulk voltage continuously. This may degrade the performance of the audio power amplifier whilst increasing the possibility of latch up due to the forward-biased body of MOSFET transistors. As a result, it may not be suitable for audio power amplifier with the bulk voltage trimming method. The study of the offset in audio power amplifier is conducted in [15]–[17]. The reported offset cancellation circuits [16], [17] allow the reduction of quiescent current in the output stage and the improvement of power efficiency with respect to the audio amplifiers without offset cancellation circuits. Unfortunately, these previously-published works on audio power amplifiers are not efficient on the offset cancellation. The proposed circuit in [15] requires a big capacitor of 50pF for the LPF realization so that it does not influence the amplifier behaviour in the audio frequency range. This will increase the total area. In addition, the resulting offset voltage is signal dependent whereas the DC component at the output is approximately equal to 1.2% of the signal amplitude.

The full analog approach [16] requires an external capacitor to realize the LPF. Alternatively, a cross offset cancellation technique [17] can reduce the offset for class-D amplifier but it is not suitable for class-AB application.

Figure 2.7 Concept of offset calibration circuit proposed in [28].

For the headphone amplifier offset reduction, the automatic trimming offset cancellation technique is more efficient than other mentioned techniques. Fig. 2.7 shows the exemplary signal flow of offset calibration circuit with current control. However, the architecture has suffered from two disadvantages. The first one is that the amplifier requires a ping-pong topology as shown in Fig. 2.8 to obtain the continuous-time output signal. Unfortunately, it doubles the silicon area and power consumption. The second one is that the ping-pong circuit architecture will contribute additional switching noise which may not be desirable in high-performance audio amplifier application. Due to this reason, there is a need to investigate an alternative offset calibration scheme that overcomes the key disadvantages of the aforementioned scheme.

Figure 2.8 Topology of ping-pong operational amplifier proposed in [28].

2.3.1. Yu's Circuit [28]

The main idea of Yu's circuit is to digitally adjust the bias voltage of a programmable current mirror, which serves as the active load of input pairs. Although the bias voltage is changed to reduce the offset, it should be treated as current control like approach [29], [33] since they all modify the offset by changing the biasing current of input stage. The proposed amplifier by Yu is depicted in Fig. 2.9, in which the current mirror is programmable and controllable by the output signal. The current mirror gain can be digitally adjusted by changing the voltage of V_{CB} and V_C . This will adjust the input offset consequently. The basic concept of the offset tuning architecture is illustrated in Fig. 2.7. It consists of a comparator, an up-down-counter and a digital-to-analog converter (DAC). Compared to other adjustable current mirror circuits, the digital

scheme can achieve relatively low offset and avoid charge injection problems. The working principle of the calibration procedures are summarized as follows:

- 1) The output of the main amplifier is compared to a zero voltage when the two terminals are connected to ground.
- 2) Then, the output of the comparator will be used to control the bias voltage V_C through an up-down-counter and a DAC to reduce the input offset of the main amplifier.
- 3) Repeat procedure 1) and 2) until the output of the main amplifier crosses zero.

This algorithm is straight-forward and it can be applied in many offset cancellation circuits. The resolution of the offset cancellation is limited by range of the bias voltage V_C and the comparator. In general, the resolution of the bias voltage is more important than that of the comparator since the tuning block usually requires more power and large area. The offset range of the main amplifier is determined firstly whilst the cancellation should cover the whole offset range. Then the number of bits can be determined to accomplish a specific resolution.

Figure 2.9 Offset adjustable two-stage CMOS op-amp with a programmable current mirror proposed by Yu [28].

In order to estimate the offset range, Yu assumes that the input stage has the dominant effect on the offset voltage. The expression of the input offset voltage is given as

$$V_{OS,in} = V_{OS,12} + V_{OS,34} + V_{OS,VC} + V_{OS,sys} \quad (2.4)$$

where $V_{OS,sys}$ is the systemic offset voltage, which can be very small in carefully designed circuit. $V_{OS,12}$, $V_{OS,34}$ and $V_{OS,VC}$ are the input-referred random offset voltages caused by the mismatches of the input pairs, current mirror active load, and the resistive transistors, respectively. For a careful design without resistive transistors M_{R1} and M_{R2} , the systemic offset voltage is so small that it can be ignored when compared to the input-referred random offset voltage. Refer to the circuit in Fig. 2.9, the overall offset voltage can be adjusted by changing the bias voltage V_C to cancel the dominant random offset voltage, resulting in a low-offset amplifier.

The input-referred random offset voltage can be estimated in [68]. The standard deviation of total input-referred random offset voltage is obtained as

$$\sigma_{VOS} = \frac{|V_{gs1,2} - V_{T1,2}|}{\sqrt{2}} \left[\sigma_L^2 \left(\frac{1}{L_{1,2}^2} + \frac{1}{L_{3,4}^2} + \frac{1}{L_{VC}^2} \right) + \sigma_W^2 \left(\frac{1}{W_{1,2}^2} + \frac{1}{W_{3,4}^2} + \frac{1}{W_{VC}^2} \right) + \frac{4\sigma_{VT1,2}^2}{(V_{gs1,2} - V_{T1,2})^2} + \frac{4\sigma_{VT3,4}^2}{(V_{gs3,4} - V_{T3,4})^2} + \frac{\sigma_{VT,VC}^2}{(V_{gs,VC} - V_{T,VC})^2} \right]^{1/2} \quad (2.5)$$

where $V_{gs1,2}$, $V_{T1,2}$, $L_{1,2}$ and $W_{1,2}$ are the gate-source voltage, the threshold voltage, the channel length and the width of transistors M_1 and M_2 , respectively. Based on the transistors size and [68], the input-referred random offset voltage can be estimated with value of $\sigma_{VOS} = 12.2\text{mV}$. $3\sigma_{VOS}$ almost can cover 99.7% of the offset and it is selected as the compensation range of offset cancellation.

Meanwhile, the range of the bias voltage can be determined by simulation, which is accomplished by a resistor ladder based digital-to-analog converter. In order to achieve full duty cycle, a ping-pong structure is applied in Yu's circuit. It is made up of two identically op-amps shown in Fig. 2.9. When one op-amp works in the normal amplifying mode, the other one will operate in the offset cancellation mode. By changing the operating mode of the two op-amps, a low-offset amplifier can be obtained with the ping-pong topology.

2.4. Review of Frequency Compensation Techniques

An effective frequency compensation scheme plays one of the key roles in low-quiescent headphone amplifier design. The frequency compensation of a headphone amplifier has displayed some differences with that of a capacitive load driven operational amplifier (op-amp). It is mainly because that the DC gain of last stage of headphone amplifier is usually smaller than or close to unity in the presence of very small resistive load. Besides, the output pole frequency contributed by the effective load is usually located at high frequency which is above the audio band. As such, it can be ignored in the frequency compensation analysis. Nevertheless, the frequency compensation techniques used for capacitive load driven op-amp can also be extended or used in headphone amplifier. For better low-quiescent performance, the frequency compensation needs to be addressed.

Figure 2.10 Topology of three-stage NMC amplifier [37].

The nested Miller compensation (NMC) amplifier [37], [50] is the foundation circuit which serves as the benchmark for other multistage amplifiers. The small-signal analysis of headphone amplifier is similar to that of the capacitive driven op-amp except that the third-stage gain of headphone amplifier tends to be small due to very

low resistive load. The following assumptions are made when analysing the small-signal behaviour of NMC headphone amplifier:

- 1) The first two stages have gain much higher than one ($g_{mi}r_{oi} \gg 1$) whereas the gain of output stage is lower than one ($g_{m3}R_L \ll 1$).
- 2) The loading capacitance C_L is much larger than all of the other capacitances ($C_L \gg C_{pi}, C_{mi}$), including the compensation capacitors and the lumped capacitances. The lumped parasitic capacitance of the first stage is much smaller than the compensation capacitance ($C_{m1} \gg C_{p1}$).
- 3) The interstage capacitances can be ignored.

The output resistances, equivalent transconductance and lumped parasitic capacitances of each gain stage are denoted by r_{oi} , g_{mi} and C_{pi} , respectively. C_{m1} and C_{m2} are the Miller capacitors. R_L is the resistive load. The transfer function of NMC amplifier is obtained as

$$A(s) = A_{dc} \frac{1 - s \frac{C_{m2}}{g_{m3}} - s^2 \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}}{(1 + \frac{s}{P_{-3dB}})(1 + s \frac{(g_L + g_{m3})C_{m2} - g_{m2}C_{m2}}{g_{m2}g_{m3}} + s^2 \frac{C_L C_{m2}}{g_{m2}g_{m3}})} \quad (2.6)$$

$$A_{dc} = g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L \quad (2.7)$$

$$P_{-3dB} = - \frac{1}{C_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L} \quad (2.8)$$

It shows that the headphone amplifier frequency response has the same dominant pole expression as that of the capacitive driven op-amp. The expressions of the first zero and non-dominant pole are obtained as follows:

$$z_1 = \frac{g_{m3}}{C_{m2}} \quad (2.9)$$

$$p_2 = \frac{-g_{m2}g_{m3}}{(g_L + g_{m3})C_{m2} - g_{m2}C_{m2}} \quad (2.10)$$

It shows that the unity-gain frequency (UGF) of the inner loop, which is usually set by the intermediate stage transconductance g_{m2} and the inner Miller capacitor C_{m2} , may be quite different from that of the capacitive driven op-amp. For a three-stage NMC headphone amplifier, the inner loop UGF not only depends on the intermediate stage transconductance and the inner Miller capacitor value but it also depends on the small third-stage gain. As a result, the inner loop unity gain frequency of NMC headphone amplifier, which is also the first non-dominant pole, will be much lower than that of a capacitive driven op-amp. In addition, a right-half-plane (RHP) zero created by the feedforward path through inner Miller capacitor will degrade the phase margin and gain-bandwidth product (GBW).

In order to extend the GBW of three-stage headphone amplifier, many frequency compensation techniques [38]–[66] have been proposed. They are damping-factor-control frequency compensation [49], active feedback frequency compensation [56], single Miller capacitor frequency compensation [59], reversed nested Miller frequency compensation [61] and cascode Miller compensation [66]. Nevertheless, these reported works require extra circuits to control the damping factor or provide non-suitable feedforward path which leads to higher quiescent power consumption.

Figure 2.11 Topology of three-stage NMCFNR amplifier [51].

Among the amplifiers, the nested Miller compensation with feedforward stage and nulling resistor (NMCFNR) topology in [51] is preferred due to its low power topology using the nulling resistor method. The topology of three-stage NMCFNR amplifier is presented in Fig. 2.11. In order to investigate the power-bandwidth efficiency of NMCFNR topology, the small-signal analysis of NMCFNR headphone amplifier is also conducted with the same assumptions as that of NMC amplifier. g_{mf2} represents the equivalent transconductance of feedforward gain stage and R_m is the nulling resistor. The transfer function of NMCFNR headphone amplifier is obtained as follows:

$$A(s) = A_{dc} \frac{1 + s \left(R_m (C_{m1} + C_{m2}) + \frac{(g_{mf2} - g_{m2}) C_{m2}}{g_{m3} g_{m2}} \right) + s^2 \frac{(g_{mf2} + g_{m3}) R_m C_{m1} C_{m2}}{g_{m2} g_{m3}}}{\left(1 + \frac{s}{P_{-3dB}} \right) \left(1 + s \frac{(g_L + g_{m3}) C_{m2} - g_{m2} g_L R_m C_{m2}}{g_{m2} g_{m3}} + s^2 \frac{C_{m2} C_L - g_{m2} R_m C_{m2} C_L}{g_{m2} g_{m3}} \right)} \quad (2.11)$$

$$A_{dc} = g_{m1} g_{m2} g_{m3} r_{o1} r_{o2} R_L \quad (2.12)$$

$$P_{-3dB} = - \frac{1}{C_{m1} g_{m2} g_{m3} r_{o1} r_{o2} R_L} \quad (2.13)$$

where A_{dc} and p_{-3dB} have the same expressions as that of the NMC amplifier. Since the non-dominant high frequency zeros and poles are far away from the UGF, one can obtain the first zero and second pole as follows:

$$z_1 = \frac{-g_{m2}g_{m3}}{g_{m2}g_{m3}R_m(C_{m1} + C_{m2}) + (g_{mf2} - g_{m2})C_{m2}} \quad (2.14)$$

$$p_2 = \frac{-g_{m2}g_{m3}}{(g_L + g_{m3})C_{m2} - g_{m2}g_L R_m C_{m2}} \quad (2.15)$$

For the feedforward transconductance $g_{mf2} > g_{m2}$ in (2.14), the left-half-plane (LHP) zero is created. The price paid for the large g_{mf2} is that it will increase the power consumption. If $g_{mf2} < g_{m2}$ is made for low-power criteria, the control of LHP zero will rely on the increased value of nulling resistor R_m [51]. However, the disadvantage of NMCFNR topology is that the LHP pole in (2.14) has the possibility to become a RHP pole when there is a substantial increase of the product $g_L R_m$. To avoid the formation of RHP pole and permit the better placement of the second pole close to the first zero, a three-stage NMCFNR headphone amplifier will be resorted to the tradeoff design among the extra power needed for g_{mf2} and the allowable resistance range of R_m . As a result, the constraint value for R_m will result in the decrease of the GBW. The outcome is the increase of Miller compensation capacitors, C_{m1} and C_{m2} , to guarantee the stability if low-power design is of concern.

Chapter 3 Architecture and Circuit Design

3.1. Proposed Digitally-Assisted Offset Calibration Circuit

3.1.1. Architecture of Proposed Digitally-Assisted Low-offset Headphone Amplifier

Of particular design criteria, it is important that the performance parameters, such as THD+N, SNR, PSRR and so forth remain unchanged when the offset calibration techniques are applied. The widely used dynamic offset techniques may not be appropriate for implementation because the smoothing filter needs to handle high power in the APA. For this reason, the automatic control that deals with active load trimming [28] or current injection [29] with ping-pong topology will be suitable to reduce the input-referred offset of headphone amplifier. However, the single-ended high-impedance node current injection circuit [29] degrades the PSRR due to the unbalanced supply noise path and reduces the effective DC gain of first gain stage. Although the active load trimming with ping-pong topology provides another means to counteract the offset problem, it is at the expense of doubling the silicon area and power consumption. In addition, the ping-pong topology may introduce additional switching noise in the continuous-time process of swap action on the two amplifiers. This is considered undesirable effect in headphone amplifier design. In order to tackle these problems, Fig. 3.1 depicts a digitally-assisted low-offset headphone amplifier incorporating the proposed offset calibration circuit.

Figure 3.1 The headphone amplifier with the proposed digitally-assisted offset calibration circuit.

Refer to the offset calibration circuit in Fig. 3.1, it consists of a comparator, a comparator spike removal circuit, a zero-crossing detection logic, a power-on reset circuit, an up-down-counter, a balanced offset compensation current injection circuit and some control logic gates. The offset voltage is calibrated through digitally adjusting the current injected into a pair of low impedance nodes in the differential input stage on the basis of balance design approach.

As shown in Fig. 3.1, Cal_on_Req (Calibration on Request) is a user-demand or system control signal. Since the proposed offset calibration circuit cannot eliminate the effect of the temperature on the offset voltage, the Cal_on_Req signal may be used by system to activate the offset calibration when there is a need to reduce the increase of

offset under the temperature variation. It is applied in a form of signal pulse format. When the pulse's logic is at high value, it enables the zero-crossing detection logic by setting the logic high output. When the pulse's logic is at low value, it enables the up-down-counter of the system. Normally, this input control signal remains at logic zero.

The offset calibration system is automatically started in the beginning of power-up action. During the start-up transition of the amplifier, the power-on reset circuit goes logic high. Since the Cal_on_Req remains at logic low, the output of zero-crossing detection logic is set to logic high through the internal edge-triggered flip flop as the memory. Meanwhile, the digital outputs of the up-down-counter are in preset state having the middle logic value of 1000,0000. When the startup has completed in a short duration, the power-on reset circuit gives logic low output. Then, the up-down-counter carries out the offset calibration task, dependent upon the up/ $\overline{\text{down}}$ control signal whilst the Cal_on_Req remains low. In the offset calibration mode, the two switches, S₁ and S₂, are closed while the amplifier is set to have the default DC gain of about 51 with respect to the unknown amplifier's input offset voltage to be calibrated. This DC gain is chosen so that the input offset can be amplified so that the resolution of the offset calibration is not significantly degraded by the comparator's offset. In the process of offset calibration, the up-down-counter controls the digitally injecting current into the differential stage. As a result, the input-referred offset and the headphone amplifier output are digitally reduced to the resolution of design. The comparator spike removal circuit is responsible to remove the false analog signal caused by the spike appeared at the analog output of headphone amplifier during the switching action of offset current injection circuit. During calibration, there is no polarity change at the output of comparator. When the zero-crossing detection logic

detects the transition change, either from logic high to low or from logic low to high at the output of comparator, its output goes low to terminate the offset calibration process. Finally, in the normal operation mode, the two switches, S_1 and S_2 open and the up-down-counter is disabled. At this juncture, the headphone amplifier will serve as a driver.

Figure 3.2 Simulated transient response of the important signals in the offset calibration system.

Fig. 3.2 shows the simulated transient response of the key signals in the offset calibration system. After the power-on reset period from $20\mu\text{s}$ - 2ms , the output-referred offset of the amplifier is automatically trimmed from about 2ms to 2.96ms . The zoom-in view of the output signal shows that V_{OUT} settles to the value of -4.1mV under which the offset calibration stops. This is translated to the input offset voltage of $-80.4\mu\text{V}$ based on the closed-loop gain of 51 in offset calibration mode. For the V_{COMP} , there exists several transition waveforms in the form of either short pulse or periodic

transient output response. They come from (i) the system start-up with the short duration pulse at time $20\mu\text{s}$, (ii) the completion of the first offset calibration with the short duration pulse at about 2.96ms and (iii) the output response of comparison based on the periodical input signal after 2.96ms . In this design, when the zero-crossing detection logic detects the transition change of signal V_{COMP} at about 2.96ms which is the end time of offset calibration, the $\overline{\text{Done}}$ signal becomes asserted low. Other subsequent change of transitions from V_{COMP} will not influence the status of $\overline{\text{Done}}$ signal.

3.1.2. Transistor Level of Digitally-Assisted Offset Calibration Circuit

3.1.2.1. Balanced Offset Compensation Current Injection Circuit

Figure 3.3 Concept of balanced offset compensation current injected into differential input stage.

The key idea for obtaining low offset circuit is to inject balanced offset compensation current into the differential stage of the amplifier in order to digitally adjust the input-

referred offset voltage of the amplifier system. Refer to Fig. 3.3, $I_{B1} \sim I_{B3}$ represent three constant current sources, which have the same value. I_{B4} is a digitally programmable current source that can be digitally adjusted by the outputs of the up-down-counter. I_X and I_Y represent the current injected into the node X and Y, respectively. Since I_{B1} and I_{B3} have the same value, the current injected into node Y will be almost zero. The main function of this dummy signal path is used to cancel the supply noise from node X, which will be further explained in the following part.

Figure 3.4 Transistor level of four current sources for balanced current injection.

sequence. The smallest current source of the MSB array is two times that of the largest current source in the LSB array. As a result, the two current source arrays form a current-mode DAC. Of particularly noted, the smallest current source is $I_0 = 20\text{nA}$ in LSB array. Assuming the equivalent transconductance of the input stage is g_{m1} , the resolution of the input-referred offset can be obtained as follows:

$$V_{OFFmin} = \frac{I_0}{g_{m1}} \quad (3.1)$$

In this design, the trans-conductance of input stage is $g_{m1} = 234\mu\text{S}$. Hence, the resolution of offset calibration system is estimated to be $85\mu\text{V}$. During the offset calibration, the DC gain of headphone amplifier is set at 51. This translates to the equivalent amplifier's output DC offset value of $51 \times 85\mu\text{V} = 4.335\text{mV}$ when the calibration has completed. Since the input-referred offset of comparator in Fig. 3.1 is about $\pm 2\text{mV}$ from Monte Carlo simulation results of the design, it does not significantly degrade the resolution of calibrated input-referred offset for the headphone amplifier. Of particularly noted, under normal amplifier operation, the closed-loop gain of the difference amplifier with respect to the calibrated input offset is 2. Based on the calibrated input-referred offset of $85\mu\text{V}$, the induced quiescent power is only $1\mu\text{W}$ when compared to the amplifier circuit with zero offset. The stacked current sources, I_{B1} and I_{B3} , establish an approximately balanced impedance from the right hand side with respect to that of the stacked current sources contributed by I_{B2} and I_{B4} in the left hand side. Therefore, the current I_Y is almost zero.

3.1.2.2. Other Circuit Blocks of the Offset Calibration Circuit

Except for the balanced offset compensation current injection circuit, the offset calibration circuit also consists of five major circuit blocks. They are comparator, comparator spike removal circuit, zero-crossing detection logic, power-on reset and up-down-counter. The comparator is realized by a simple operational transconductance amplifier (OTA), which supports rail-to-rail output. The positive and negative terminals of the OTA are connected to the output of headphone amplifier and the ground at 0V, respectively. The comparator is designed to ensure that the resolution of offset calibration circuit is not greatly degraded. The function of comparator spike removal circuit aims to remove the spikes produced from the headphone amplifier output signal that will falsely trigger the zero-crossing detection logic to produce the false digital output in a form of short duration transition pulse. The comparator spike removal detector circuit is realized by an edge-triggered D-type flip-flop. This is used to synchronize with the long duration calibration clock so as to discriminate against the false digital signal in a form of short transition pulses which are caused by the analog spikes at the input of the comparator. The up-down-counter is a conventional bidirectional counter which comprises eight JK flip-flops and other necessary logic gates. When the amplifier works in the offset calibration mode, the up-down-counter and the amplifier generates an eight-bit digital signal to adjust the weighted current injected into the differential stage. Shown in Fig. 3.5, the power-on reset is made up of a voltage divider, an RC circuit, a comparator and a digital buffer. In order to realize a large time constant and save the silicon area, a pseudo resistor is employed to achieve a high resistance value.

Figure 3.5 Power-on reset circuit.

Figure 3.6 Transient response of the power-on reset circuit when the amplifier starts up.

The transient response of the power-on reset circuit is illustrated in Fig. 3.6. At the beginning of the startup, the momentary negative pulse generated from V_{SS} couples to the negative input V_1 of comparator, it forces the reset circuit output PoR to go high. V_1 gradually settles to a constant voltage V_R of 200mV defined by the voltage divider. When V_1 is smaller than 0V, the comparator output, V_{OUT} , gives logic “0”, which is -1V. When V_1 reaches above 0V, the V_{OUT} turns to logic “1” which is 1V. It is noted

that the choice of 200mV is to allow a suitable pulse width of about 2ms to be generated from the power-on reset circuit output. During this startup period, the zero-crossing detection logic is enabled whereas the up-down-counter is in preset state. Immediately after the period, the offset calibration process will be started in the APA.

Fig. 3.7 shows the circuit of zero-crossing detection logic, which is realized using a complementary delay generation circuit, an XNOR gate, a D-type flip-flop and an inverting output buffer. Whenever any logic transition appears at the output of comparator, it is sensed by the single input of zero-crossing detection logic. On the other hand, the output “ $\overline{\text{Done}}$ ” of zero-detector, which comes from the cascade of inverting buffer and D-type flip flop, is set to logic high by the Cal_Enable signal prior to start the offset calibration.

Figure 3.7 Zero-crossing detection logic.

Figure 3.8 Transient responses of the signals in zero-crossing detection logic.

Fig. 3.8 shows the transient responses of some signals in zero-crossing detection logic. The complementary delay generation circuit within the detector produces the dual logic signals which have the complementary and delay characteristics. The signals V_{COMP} is the output of the comparator spike removal circuit shown in Fig. 3.1 and $\overline{V_{COMP}}$ is the delayed inverting value of V_{COMP} . The V_{COMP} and $\overline{V_{COMP}}$ are tied to the inputs of XNOR gate. The XNOR gate generates a short pulse signal if the comparator spike removal circuit outputs the real detected transition. When the positive transition of the short pulse appears at the clock input of D flip flop, the output signal $\overline{Done}$ of the zero-crossing detection logic changes from logic high to logic low, indicating that the calibration has completed. At this juncture, the $\overline{Done}$ signal opens the amplifier switches as depicted in Fig. 3.1 and stops the up-down-counter. The amplifier goes into normal operation mode. Fig. 3.8 shows the comparator spike removal circuit output, V_{COMP} , in response to the application of a 1kHz sinusoidal input signal to the

APA with 2mV input offset, starting from the system power up at time $20\mu\text{s}$ to the power-on reset period $20\mu\text{s}$ -2ms. Then, this is followed by the offset calibration period between 2ms-2.96ms and the normal operation mode after 2.96ms. It is important to note that the calibration period depends on the input offset of APA. When the zero-crossing detection logic in Fig. 3.7 detects the transition change of signal V_{COMP} , it generates a pulse signal V_{XNOR} . The $\overline{\text{Done}}$ signal, which is obtained from the inverting buffer output of the D-type flip-flop, is only asserted one time when the offset calibration has completed. It remains active low until the Cal_on_Req signal has been triggered to initiate another offset calibration by system or user demand. Other transition changes do not influence the status of $\overline{\text{Done}}$ signal.

3.1.3. Influence of Input-offset, Temperature and Power Transistors Leakage Current on Quiescent Power Consumption of Headphone Amplifier

The quiescent power consumption of a power amplifier is mainly influenced by the input-referred offset, temperature and power transistors leakage current. In order to study the influence of input-referred offset voltage and temperature on the quiescent power consumption without offset calibration, the quiescent power of this amplifier under different temperatures and V_{OFFSET} values is used as example to illustrate the effects. The simulation results are obtained and summarized in Table 3.1 and Fig. 3.9.

Table 3.1 The Offset-induced Quiescent Power Consumption Study of Headphone Amplifier

V_{OFFSET}	Offset-Induced Current (mA)	Total Quiescent Power (mW)	Quiescent Power Increase with respect to APA with 0mV Offset
0mV	0	0.4295	0%
1mV	0.125	0.4811	12.01%
2mV	0.25	0.5798	34.99%
3mV	0.375	0.6931	61.37%
4mV	0.5	0.8119	89.03%
5mV	0.625	0.9330	117.2%

It can be observed that the total quiescent power consumption increases with the input-referred offset voltage. The simulation results have revealed that the quiescent power consumption will increase by 117.2% for a 5mV input-referred offset. This suggests that the offset-related quiescent power becomes a significant part in the total power consumption. The offset-induced quiescent power study has confirmed the fact that the low-offset metric is necessary for a low-quiescent power amplifier design.

Figure 3.9 The quiescent power consumption of proposed power amplifier under different temperature and input-referred offset voltage.

The dependence of total quiescent power consumption of the headphone amplifier on temperature is mainly determined by the biasing circuit. A constant-gm bias generation circuit is used in the amplifier. According to the working principle of constant-gm circuit, the dependence of current on temperature is determined by carrier mobility, threshold voltage and resistor value. Fig. 3.9 shows that the quiescent power consumption will increase with temperature. It is mainly because the threshold voltage is the dominant factor which decreases with temperature, causing the increase of gate-source difference voltage bias on the resistor.

The leakage current may be another factor that may affect the total quiescent power consumption of headphone amplifier in nano-scaled technology. Power transistors with large aspect ratio will become the dominant sources for the leakage current. In the quiescent condition of headphone amplifier, the drain voltage of the power transistors are 0V. In order to identify the value of leakage current and understand its variation

with temperature, the gates of the power transistors are connected to the positive supply and negative supply, respectively.

Figure 3.10 Temperature variation of power transistors leakage current with in different corners.

Fig. 3.10 shows the temperature variation of power transistors leakage current in different corners. It shows that the leakage current of power transistors in fast-fast (FF) corner is much higher than that of other corners. It is because the threshold voltage of transistors in FF corners is smaller. The leakage current increases rapidly with temperature and it is much smaller than the quiescent power consumption of headphone amplifier. Therefore, we can conclude that the leakage current will not degrade the quiescent power consumption of power amplifier despite leakage current is often as one of the main issues in VLSI system.

3.1.4. Advantages of Balanced Low-impedance Node Current Injection Circuit

Compared to the conventional single-ended high impedance node current injection, the proposed balanced topology in this work has offered two key advantages.

Firstly, since the high-impedance offset compensation current sources are injected into two low-impedance nodes of folded-cascode input stage, it will not significantly degrade the gain of first stage. Secondly, when the current injection circuit is coupled to the output of first stage, it may jeopardize the PSRR significantly due to the unbalanced topology. Fig. 3.11 shows the PSRR simulation results for the amplifiers designed with two different current injection circuits. The amplifier design without any current injection circuit serves as the benchmark. Fig. 3.11 (a) compares the PSRR plots for the amplifier with/without balanced offset current injection compensation. It shows that the PSRR obtained from the proposed balanced offset compensated amplifier approximately maintains similar low-frequency PSRR characteristic with reference to that of the benchmark. By comparison, the low frequency PSRR of conventional offset current injection compensation is much lower than that of the benchmark shown in Fig. 3.11 (b). For the critical frequency of 217Hz in mobile applications, the current injection network causes the drop of 13dB in PSRR. It is mainly because the conventional current injection circuit yields an additional supply noise path from the supply to the critical node X in the input differential stage. The implementation of balanced circuit topology introduces a dummy current branch, which not only provides a symmetrical signal path for cancelling the supply noise but it also balances the impedances associated with the critical nodes X and Y.

Figure 3.11 Comparative simulation results of PSRR for the current injection offset compensation amplifier and the benchmark headphone amplifier: (a) using proposed balanced low-impedance node injection circuit, (b) using single-ended high-impedance node injection circuit.

3.2. Proposed Frequency Compensation Topology

In order to design a stable three-stage headphone amplifier with low-quiescent power consumption, an improved frequency compensation topology is devised to solve the RHP pole issue in the reported NMCFNR amplifier [51].

Figure 3.12 Topology of proposed three-stage NMCFNR2 amplifier.

Refer to the multipath nested Miller compensation (MNMC) amplifier in [39], [50], it requires the substantial increase of g_{mf1} to push the first zero close to the second pole. Unfortunately, it may lead to large power consumption if the second pole is located at low frequency. Fig. 3.12 shows the improved frequency compensation topology, called NMCFNR2, which is the Type-II implementation of NMCFNR amplifier. It utilizes the nulling resistors to serve as the main assist for pushing the first LHP zero to low frequency. As a result, it permits low quiescent bias for the feedforward transconductance g_{mf1} in NMCFNR2 amplifier, thus saving power consumption. Comparing this topology with that of NMCFNR, the separate nulling resistor and capacitor compensation network replaces the merged compensation network. Besides, the feedforward transconductance stage is re-arranged across the first and second gain stages instead of that across the second and third gain stages.

Based on the same assumptions in the analysis if NMC amplifier, the transfer function of NMCFNR2 amplifier is obtained as follows:

$$A(s) = A_{dc} \frac{1 + s \left(R_{m1} C_{m1} + R_{m2} C_{m2} + \frac{g_{mf1} C_{m1}}{g_{m1} g_{m2}} \right) + s^2 (R_{m1} R_{m2} C_{m1} C_{m2} + \frac{g_{mf1} R_{m2} C_{m1} C_{m2}}{g_{m1} g_{m2}})}{(1 + \frac{s}{P_{-3dB}}) (1 + s \frac{(g_{m3} + g_L) C_{m2} + g_{m2} g_{m3} R_{m2} C_{m2}}{g_{m2} g_{m3}} + s^2 \frac{C_{m2} C_L}{g_{m2} g_{m3}})} \quad (3.2)$$

$$A_{dc} = g_{m1} g_{m2} g_{m3} r_{o1} r_{o2} R_L \quad (3.3)$$

$$P_{-3dB} = - \frac{1}{C_{m1} g_{m2} g_{m3} r_{o1} r_{o2} R_L} \quad (3.4)$$

With other non-dominant zeros and poles outside the UGF, the first zero and the second pole of NMCFNR2 amplifier are given as

$$z_1 = \frac{-g_{m1} g_{m2}}{g_{m1} g_{m2} (R_{m1} C_{m1} + R_{m2} C_{m2}) + g_{mf1} C_{m1}} \quad (3.5)$$

$$p_2 = \frac{-g_{m2} g_{m3}}{(g_L + g_{m3}) C_{m2} + g_{m2} g_{m3} R_{m2} C_{m2}} \quad (3.6)$$

Refer to (3.5) and (3.6), there is no negative sign in respective denominator for the first zero and the second pole. This indicates that LHP zero and LHP pole are valid for all design conditions. This turns out that there is no possibility to generate the RHP pole in the NMCFNR2 amplifier. As such, the location of the first zero can be designed with larger freedom through the choice of nulling resistors R_{m1} and R_{m2} , and the feedforward transconductance g_{mf1} . It is apparent that no significant restriction using large values for R_{m1} and R_{m2} . This supports low-power design strategy. For instance, z_1 can be made small with small value of g_{mf1} and large values of the nulling resistors without creating the RHP pole as implied in (2.15). Besides, the re-arrangement of

feedforward topology in APA design causes $g_{mf1}C_{m1}/g_{m1}g_{m2}$ in (3.5) $>$ $(g_{mf2}-g_{m2})C_{m2}/g_{m2}g_{m3}$ in (2.14). Therefore, smaller Miller capacitor C_{m1} can be employed for defining the first LHP zero location according to (3.5). This gives the advantages of small compensation capacitance as well as improved GBW.

Figure 3.13 Simulated open-loop gain and phase with different nulling resistors for (a) NMCFNR2 amplifier and (b) NMCFNR amplifier.

Fig. 3.13 shows the simulated open-loop gain and phase responses with different nulling resistors for the NMCFNR2 and NMCFNR amplifiers. They are based on the fixed Miller capacitors ($C_{m1}=4.91\text{pF}$, $C_{m2}=1.78\text{pF}$ in NMCFNR2 and $C_{m1}=20.7\text{pF}$, $C_{m2}=2.5\text{pF}$ in NMCFNR) and the load of $16\Omega//200\text{pF}$. The results have validated that the large nulling resistors in NMCFNR amplifier will introduce the RHP pole, causing the stability problem. Compared to the NMCFNR counterpart, the NMCFNR2 amplifier can improve the phase margin (PM) with large nulling resistive values whilst providing adequate gain margin (GM).

Table 3.2 lists the calculated value for each pole and zero under two frequency compensation schemes in the APA design. In order to achieve a phase margin of 60° at the identical power, the design parameters are that $R_m = 5\text{k}\Omega$ and $C_{m1} = 20.7\text{pF}$ are used in NMCFNR amplifier whereas $R_{m1} = 15\text{k}\Omega$, $R_{m2} = 14\text{ k}\Omega$ and $C_{m1} = 4.91\text{pF}$ are used in NMCFNR2 amplifier. Due to the constraint of the second pole location in NMCFNR amplifier, R_m cannot be made too large, and hence the large value of C_{m1} is needed to push LHP zero to low frequency for partial cancellation of the second pole. Regarding the NMCFNR2 amplifier, smaller Miller capacitor C_{m1} and relatively larger nulling resistors, R_{m1} and R_{m2} , can be used to enhance the GBW in low power design. The simulation results in Fig. 3.13 have confirmed that the GBW of NMCFNR and NMCFNR2 is 0.614MHz and 1.777MHz , respectively at identical quiescent power and phase margin.

Table 3.2 Comparison of poles and zeros for two frequency compensation techniques

NMCFNR2			
Poles	Pole frequency	Zeros	Zero frequency
$p_{-3dB} = \frac{-1}{C_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L}$	-13.5Hz	—	—
$p_2 = \frac{-g_{m2}g_{m3}}{(g_L + g_{m3})C_{m2} + g_{m2}g_{m3}R_{m2}C_{m2}}$	- 0.305MHz	$z_1 = \frac{-g_{m1}g_{m2}}{g_{m1}g_{m2}(R_{m1}C_{m1} + R_{m2}C_{m2}) + g_{mf1}C_{m1}}$	-0.833MHz
$p_3 = \frac{-((g_L + g_{m3})C_{m2} + g_{m2}g_{m3}R_{m2}C_{m2})}{C_{m2}C_L}$	-7.53MHz	$z_2 = \frac{-(g_{m1}g_{m2}(R_{m1}C_{m1} + R_{m2}C_{m2}) + g_{mf1}C_{m1})}{g_{m1}g_{m2}R_{m1}R_{m2}C_{m1}C_{m2} + g_{mf1}R_{m2}C_{m1}C_{m2}}$	-4.32MHz
NMCFNR			
Poles	Pole frequency	Zeros	Zero frequency
$p_{-3dB} = \frac{-1}{C_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L}$	-3.2Hz	—	—
$p_2 = \frac{-g_{m2}g_{m3}}{(g_L + g_{m3})C_{m2} - g_{m2}g_L R_m C_{m2}}$	-0.476MHz	$z_1 = \frac{-g_{m2}g_{m3}}{g_{m2}g_{m3}R_m(C_{m1} + C_{m2}) + (g_{mf2} - g_{m2})C_{m2}}$	-1.124MHz
$p_3 = \frac{-((g_L + g_{m3})C_{m2} - g_{m2}g_L R_m C_{m2})}{C_{m2}C_L - g_{m2}R_m C_{m2}C_L}$	-5.374MHz	$z_2 = \frac{-(g_{m2}g_{m3}R_m(C_{m1} + C_{m2}) + (g_{mf2} - g_{m2})C_{m2})}{(g_{mf2} + g_{m3})R_m C_{m1}C_{m2}}$	-5.535MHz

In order to evaluate the stability, the process Monte Carlo simulations are conducted for the two amplifiers and their histograms for PM and GM are illustrated in Fig. 3.14. It has revealed that the improved frequency compensation is robust against the process variation. Fig. 3.15 shows the simulated PM for $R_L = 16\Omega$, 32Ω and 50Ω under different C_L values. Since large C_L will push the p_3 in NMCFNR2 amplifier close to the unity-gain frequency, the PM will decrease with the increase of C_L . Observing the PM relationship with R_L and C_L , the PM is regarded as the trade-off design parameter between the two variables.

Figure 3.14 Process Monte Carlo histograms for phase and gain margins with the respective load of $16\Omega/0pF$ and $16\Omega/2nF$.

Figure 3.15 Simulated PM for $R_L=16\Omega$, 32Ω and 50Ω when sweeping the C_L from 0pF to 2nF.

A headphone load will display both inductive and capacitive effect in a form of resonant circuit which is reported as the approximated headphone load model [69]. In this design, the impedance of 16Ω headphone model, having a resonant frequency of 2MHz, is adopted. The circuit model is shown in Fig. 3.16, with $R_A=5\Omega$, $C_L=332\text{pF}$, $R_L=17\Omega$, $R_B=340\Omega$, $L_L=20\mu\text{H}$. To assess the stability, Fig. 3.17 depicts the simulated open-loop gain and phase responses of amplifier with the approximated headphone load, yielding $\text{GBW}=6.7\text{MHz}$, $\text{PM}=41^\circ$ and $\text{GM}=9.5\text{dB}$. This amplifier system is considered stable because of having adequate GM. Of particular interest, the GBW is enhanced due to the additional high-frequency zero caused by the inductive effect. To further improve the PM by 10° at the expense of silicon area, a 20pF can be added across the feedback resistor R_2 in Fig. 3.1.

Figure 3.16 The approximated headphone impedance model [69].

Figure 3.17 The simulated open-loop gain and phase for headphone amplifier using the approximated headphone impedance load model.

The simulation result of NMCFNR2 amplifier correlates well with the theory. Due to the relaxation in the design tradeoff, this explains why the GBW can be enhanced with the improved scheme.

3.3. Transistor Level Realization of Headphone Amplifier

Fig. 3.18 depicts the simplified schematic of the proposed class-AB headphone amplifier circuit with the balanced offset compensation circuit for the differential input stage and the channel-length modulation (CLM) reduced class-AB bias generation circuit for the push-pull output stage. This is a three-stage amplifier topology which employs an improved compensation topology, called NMCFNR2 to drive a parallel resistive and capacitive load. As mentioned above, the topology works along with the offset calibration system to reduce the offset arising from the difference amplifier topology. The use of CLM-reduced bias generation circuit offers an improved quiescent bias control in the class-AB push-pull output stage with respect to that of the conventional bias circuit. The employment of improved frequency compensation in the APA design permits low quiescent power consumption whilst yielding adequate gain-bandwidth metric and small compensation capacitors for audio applications in the context of stability against very low resistive load drive. The proposed three-stage amplifier is mainly made up of a folded-cascode differential input stage, a non-inverting gain stage and a push-pull output stage. The detailed design considerations of each stage are discussed in the following sub-sections.

3.3.1. Realization of Input Stage of Headphone Amplifier

The first stage is realized with folded-cascode topology, which is formed by transistors M_1 - M_{11} . An input stage determines the performance of the APA in many aspects, including DC gain, input-referred offset, GBW, input-referred noise and so forth.

Figure 3.18 The simplified schematic of the APA with embodiment of proposed balanced offset compensation circuit and CLM-reduced class-AB bias generation circuit.

Since the first stage is one of the major stages to contribute high DC gain in the APA, the equivalent trans-conductance (g_{m1}) should be maximized whilst the equivalent output impedance of first stage should be made high. For obtaining high current efficiency of g_m , the input transistors M_1 and M_2 are biased in the sub-threshold region with large aspect ratio. The folded cascode topology can enhance the equivalent output resistance of the first stage. The DC gain of first stage can be as high as 90dB.

The input-referred offset voltage and noise of an amplifier are dictated by the first gain stage. Therefore, the size of the differential input transistor pair is made large for biasing in subthreshold region whereas the respective transconductance for current source pair transistors, M_3 and M_4 and the mirror active load transistors, M_{10} and M_{11} , is made small through the use of longer channel length. Not only does this arrangement increase the device matching characteristics, it also reduces both thermal and flicker noise. The noise analysis of the headphone amplifier will be presented in details in the following section. The use of folded-cascode topology provides high output swing as well as high input common-mode range. The bias voltages V_{BP1} , V_{BP2} , V_{BN1} and V_{BN2} are generated by the simple low-voltage cascode bias generators (not shown in Fig. 3.18).

3.3.2. Realization of Second Stage of Headphone Amplifier

The second gain stage of APA is made up of transistors M_{12} - M_{17} , which realizes a dual-input non-inverting gain stage with current mirror active load, M_{14} and M_{15} , as shown in Fig. 3.19. The transistors M_{16} and M_{17} form the floating voltage biasing source. They are of great importance for biasing the output stage. In this circuit, they will be used to bias the CLM-reduced class-AB bias generation circuit. The gain of this

second stage is much lower than that of the first stage since it is a common source amplifier without employing cascode topology to enhance the output impedance.

Consider the output voltage of APA increases from 0V, the source-gate voltage of PMOS output transistor increases continuously. At this juncture, $I_{D,M16}$ drops since the its source voltage decreases with the gate voltage being constant. As illustrated in Fig. 3.19, when the transistor M_{16} enters the cut-off region, all the biasing current of M_{13} will be steered towards the current flow in the floating biasing transistor M_{17} . This leads to increase its source voltage because the gate voltage is kept constant by the CLM-reduced bias generation circuit. As a result, the gate-source voltage of NMOS output transistor significantly drops to almost cutting off state. The similar operation goes for the floating biasing transistor M_{16} for the negative going output voltage of APA.

Figure 3.19 Illustration of biasing current flow in one of floating biasing transistors when the output voltage of APA goes positive.

3.3.3. Realization of Output Stage of Headphone Amplifier

The transistors M_{18} and M_{19} realize the third stage g_{m3} as shown in Fig. 3.18. Since the amplifier is required to drive very small resistive load and large capacitive load, the aspect ratio for M_{18} and M_{19} should be made big to provide enough current for sourcing to or sinking from the load. The quiescent current of output transistors are determined by the DC conditions of the previously mentioned CLM-reduced bias generation circuit. If each current of M_{16} or M_{17} is designed with half of that in the current source transistor M_{13} , the respective gate voltage of the output transistor can be well-defined. Hence, their corresponding quiescent current is under good control. In order to implement a low-power amplifier design, the quiescent current of output transistors needs to be optimised to balance the quiescent power and the distortion. Since the mobility of electrons is about three times of the holes in 65-nm CMOS technology, the width of p-type output transistor is set to be three times of the n-type output transistor for a symmetrical output swing. The large transistor size of the third stage results in large parasitic capacitance in the output node of second stage. This implies that the non-dominant pole arising from the second stage may be pushed towards low frequency. This may jeopardize the frequency compensation of amplifier. Therefore, the smallest channel length of the output stage is commonly utilized to minimize the silicon area as well as the parasitic capacitances. However, the price paid for small channel length transistors is that of the increase of channel length modulation effect, causing the inaccuracy of the biasing current in the output transistors. The employment of CLM-reduced bias generation circuit will relax the drawback.

3.3.4. CLM-Reduced Class-AB Bias Generation Circuit

Fig. 2.1 shows the conventional class-AB bias generation circuit which is made up of two types of biasing network for the complementary output transistors. Each network consists of one current source to power up two series-connected diodes which aims to bias the corresponding floating transistor and the respective power transistor. The problem of the bias circuit is that the DC current of output stage may exhibit higher value than the design value. This is mainly because the drain-source voltage of each output transistor is much higher than that of the replica biasing transistor. For instance, V_{ds} of $M_N > V_{ds}$ of M_N' and V_{ds} of $M_P > V_{ds}$ of M_P' . Furthermore, when the channel length of each output transistor is made small for the purpose of increasing the driving capability with large aspect ratio, the channel length modulation (CLM) between the output transistor and replica biasing transistor is particularly pronounced. This increases the design difficulty to obtain a good tradeoff between the quiescent current control and the offset performance of APA.

In order to achieve a good DC quiescent control for the APA, an improved bias generation circuit called CLM-reduced bias generation circuit is presented in Fig. 3.20. The transistor M_{19}' is a replica of the n-type output transistor M_{19} in Fig. 3.18. The drain-source voltage of M_{19}' is established via the level-shift voltage V_{gs} of M_{17}' such that $V_{ds19}' = V_{gs19}' + V_{gs17}' \approx \frac{1}{2} (V_{DD} - V_{SS})$ which is about 1V at a 2V supply in this design example. Since the transistor M_{18}'' is a replica of the p-type output transistor M_{18} , the drain-source voltage of M_{17}' is close to that of M_{17} in Fig. 3.18. Refer to the left hand side of circuit in Fig. 3.20, the similar biasing network is applied for biasing the p-type output transistor M_{18} of APA. Therefore, the improved bias generation

circuit permits the output stage drawing very close to the quiescent current of design value.

Figure 3.20 CLM-reduced class-AB bias generation circuit.

To compare the relative accuracy of the quiescent control using the conventional biasing circuit and the improved biasing circuit in the APA, the ratio of the M_{19}' and M_{19} is set to be 48. Since the current source I_B is about $2.6\mu A$ in the quiescent condition, the current of the output transistor M_{19} should be about $125\mu A$ in theoretical calculation. For the conventional biasing circuit, the simulation result has suggested that the current of the output transistor M_{19} is $184\mu A$. The difference between the simulation result and the calculation value is 47%. This has confirmed that the quiescent bias of the output stage is not well-defined due to strong CLM. By comparison, the simulation result of the improved biasing circuit gives $118\mu A$, yielding the difference of 5.6% which shows the significant eight times improvement on quiescent bias control.

For further illustration of the performance of two bias generation circuits, the Monte Carlo simulation results are conducted. The offset current is defined as the current difference between the output stage simulation results and the theoretical design values on the basis of the transistor size ratio of the output transistors and their replica biasing transistors.

Figure 3.21 Monte Carlo simulation results for offset current using the CLM-reduced bias generation circuit.

Figure 3.22 Monte Carlo simulation results for offset current using the conventional bias generation circuit.

Fig. 3.21 and Fig. 3.22 show the Monte Carlo simulation results of the offset current for the two bias generation circuits. The biasing currents for each bias generation circuit are designed with the same values. The offset current reveals the actual variation of the output stage biasing current with respect to the target design value. From the simulation results, it can be seen that the mean value of the offset current for the proposed CLM-reduced bias generation circuit is $21\mu\text{A}$ whilst the standard deviation is about $78\mu\text{A}$. In comparison, the conventional bias generation circuit contributes similar value of standard deviation but having the mean value of $82\mu\text{A}$, which is about 4 times larger than that of the improved bias circuit. This has confirmed that the APAs are subject to higher variation of bias current in the output transistor when using the conventional bias generation circuit. On the contrary, the CLM-reduced bias circuit offers relative lower sensitivity to the DC quiescent current variation.

The offset current in the proposed CLM-reduced bias generation circuit mainly comes from the threshold voltage variation and gate-source mismatch between the power transistors and the corresponding replica biasing transistors. Compared to the conventional bias generation circuit, the proposed CLM-reduced bias generation circuit provides better drain-source voltage matching, thus reducing the offset current.

In general, the APA should provide the immunity against the supply variation. The same goes for the bias generation circuit. For the intentional variation of $\pm 10\%$ in the APA powered by the $\pm 1\text{V}$ supplies, the Monte Carlo simulation results have indicated that the standard deviation of both the bias generation circuits do not change significantly. However, the mean value of the bias current of conventional bias circuit changes to about $100\mu\text{A}$. This is about 4 times larger than that of CLM-reduced bias

circuit which has a mean value of $28\mu\text{A}$. For this observation, it can conclude that the CLM-reduced bias generation circuit is relatively insensitive to the change of power supply voltage.

In the context of delivering higher power output for the APA, the supply voltage needs to be increased. For instance, the supply voltage is increased from $\pm 1\text{V}$ to $\pm 1.5\text{V}$. The bias generation circuit should be able to support higher supply APA design. This is achieved by adding two diode-connected transistors M_{20} and M_{21} for additional voltage level shift in the bias generation circuit. Fig. 3.23 depicts the simplified schematic of APA having a modified CLM-reduced bias generation circuit dedicated to $\pm 1.5\text{V}$ supply. Since the CLM-reduced bias generation circuit can still provide similar level of drain-source voltages for the respective output transistor and the corresponding replica biasing transistors, the quiescent current of output stage can be well-defined. The similar change will be applied for the conventional bias circuit powered by $\pm 1.5\text{V}$ supply for comparative study.

Figure 3.23 The schematic of APA with high-voltage CLM-reduced bias generation circuit in $\pm 1.5\text{V}$ supply.

Fig. 3.24 and Fig. 3.25 present the Monte Carlo simulation results of the offset current for the two bias generation circuits in $\pm 1.5\text{V}$ supply. It can be found that the mean offset current value of conventional bias circuit is double when the supply is increased from $\pm 1\text{V}$ to $\pm 1.5\text{V}$. It is also about 8 times larger than that of the improved bias circuit. On the other hand, the quiescent control in the improved circuit remains the same regardless of the supply being increased from $\pm 1\text{V}$ to $\pm 1.5\text{V}$. The improved bias circuit displays robust characteristic in APA design.

Figure 3.24 Monte Carlo simulation for offset current using the high-voltage CLM-reduced bias generation circuit with $\pm 1.5\text{V}$ supply.

Figure 3.25 Monte Carlo simulation for offset current using the conventional high-voltage bias generation circuit with $\pm 1.5\text{V}$ supply.

Figure 3.26 The total quiescent power versus the input offset of amplifier under two different biasing circuits.

Fig. 3.26 shows the plot of the quiescent power against the input-referred offset with two types of bias generation circuit. It can be seen that the total quiescent power in both circuits will increase with the increase of offset voltage. Table 3.3 shows the

value of the total quiescent power with the change of input-referred offset for two different bias generation circuits.

Table 3.3 Comparison of APAs with the conventional biasing circuit and the improved biasing circuit for the push-pull output stage.

Parameters	V_{OFFSET} (mV)	Total Quiescent Power (mW)	Relative Quiescent Power Error (with respect to the 0mV)
Conventional Bias Generation Circuit	0 mV	0.5505 mW	+ 28.17%
	1 mV	0.5795 mW	+ 34.92%
	2 mV	0.6565 mW	+ 52.85%
	3 mV	0.7566 mW	+ 76.16%
	4 mV	0.8673 mW	+101.9%
	5 mV	0.9831 mW	+128.9%
CLM- Reduced Bias Generation Circuit	0 mV	0.4295 mW	+ 0%
	1 mV	0.4811 mW	+ 12.01%
	2 mV	0.5798 mW	+ 34.99%
	3 mV	0.6931 mW	+ 61.37%
	4 mV	0.8119 mW	+ 89.03%
	5 mV	0.9330 mW	+ 117.2%

For APA with the CLM-reduced bias generation circuit at ideal zero offset condition, the total quiescent power consumption is about 0.43mW. With the employment of the proposed calibration system for non-ideal offset nulling, the absolute offset value becomes less than 85 μ V which accounts to the total quiescent power increase by only 0.23%. However, for a class-AB APA with the conventional bias generation circuit without the offset nulling system at ideal zero offset condition, the total quiescent power will increase by 28.17%. The CLM-reduced bias generation circuit is effective for APA with the offset voltage less than 3mV. With the increase of input offset

voltage, the mismatch-induced current will be quite large and the effect of CLM-reduced bias generation circuit on quiescent power consumption will be smaller.

3.3.5. Bias Generation and Start-up Circuit

Figure 3.27 Constant transconductance bias circuit with startup circuit.

The biasing voltage in the proposed amplifier in Fig. 3.18 is generated by the constant transconductance bias circuit shown in Fig. 3.27. In this circuit, the DC current in M_{25} and M_{26} are the same but the transistor channel width has a ratio of $W_{25}:W_{26} = 1:4$. The gate-source voltage of M_{25} and M_{26} are related by

$$V_{gs,M25} = V_{gs,M26} + I_{D,M26}R \quad (3.7)$$

Since M_{25} and M_{26} have the same threshold voltage, the equation can be rewritten as

$$\sqrt{\frac{2I_{D,M25}}{K_n\left(\frac{W}{L}\right)_{M25}}} = \sqrt{\frac{2I_{D,M26}}{K_n\left(\frac{W}{L}\right)_{M26}}} + I_{D,M26}R \quad (3.8)$$

With the identical DC current in M_{25} and M_{26} and the transistor ratio of 1:4, the equation can be simplified as

$$\frac{1}{\sqrt{2K_n\left(\frac{W}{L}\right)_{M25}} * I_{D,M25}} = R \quad (3.9)$$

Due to $g_{m,M25} = \sqrt{2K_n\left(\frac{W}{L}\right)_{M25}} * I_{D,M25}$. it turns out that $g_{m,M25} = 1/R$. Therefore, the

biasing DC current $I_{D,M25}$ is well defined at a constant temperature. In order to investigate the temperature dependence of biasing current on the temperature, the simulation is conducted.

Figure 3.28 The temperature variation of DC current for bias circuit.

Fig. 3.28 shows the simulated results for the change of biasing current with temperature. It can be observed that the biasing current continuously increases with temperature until reaching the saturation at 70 °C. This can be explained by the temperature dependence of the resistor and transistor parameters in the relationship as follows:

$$I_D = \frac{1}{2\mu_n(T)C_{ox}\left(\frac{W}{L}\right)_{M25} R(T)^2} \quad (3.10)$$

Equation (3.10) shows that the biasing current depends on the process constant, the design parameter, the temperature-dependent carrier mobility and the thermal behavior of resistor. With the increase of temperature, the lattice scattering will be increased and the electron mobility will be lower. On the other hand, for the N-well resistor adopted in the amplifier, its value will increase with the temperature. As a result, there is a slight partial cancellation of thermal effect between the two parameters. The simulated results have revealed that the dependence of biasing current on temperature is dominated by the electron mobility in the temperature range of -40 °C to 70 °C, in which the biasing current increases with temperature. For the temperature range of 70 °C to 90 °C, the biasing current is almost constant with the change of temperature, which indicates that both the thermal effects between the electron mobility and the resistor are comparable. Of particularly interest, the biasing current stays fairly constant. Finally, other device parameters, such as threshold voltage mismatch and DC current mismatch may also influence the bias current variation with temperature, but they are not the main contributing factors for the thermal effect on the biasing current.

3.4. Noise Analysis of Proposed Headphone Amplifier

The headphone amplifier is conducted with the noise analysis. The total input-referred noise of a CMOS headphone amplifier is mainly dominated by the flicker and thermal noise in the first stage. The noise in the second stage and output stage can be ignored due to the high gain of first stage. For the APA, the flicker noise is the dominant noise source, and hence the thermal noise is neglected.

Figure 3.29 The folded-cascode stage of the proposed headphone amplifier.

Fig. 3.29 shows the folded-cascode stage of headphone amplifier. The p-channel input pairs are adopted for low noise design because the flicker noise coefficient, K_F , of PMOS transistor is smaller than that of NMOS [70]. The flicker noise is inversely proportional to the frequency and transistor area. As mentioned in the previous section, the gate area of input pair and the active loads are made large. In addition, the balanced offset compensation current sources $I_{B1} \sim I_{B4}$ will also contribute to the input-referred noise since they directly inject current into the input stage. Nevertheless, since the DC

current of the four current sources are injected at the low impedance nodes in the first stage, the noise contribution of these current sources becomes negligible. As a result, the total input-referred noise of the amplifier mainly depends on the transistor M_1 - M_4 , M_{10} and M_{11} whilst the noise contribution of cascade transistors is very small to be ignored.

Based on the Gray and Meyer noise model [71] and neglecting the thermal noise, the total noise current of a single transistor is approximated as

$$\frac{\overline{i_t^2}}{\Delta f} = \frac{K_F g_m^2}{C_{OX} W L f} \quad (3.11)$$

where Δf is the bandwidth and other symbols have their usual meanings. Therefore, the equivalent noise voltage at the gate of the single transistor can be written in a form of

$$\frac{\overline{V_{eq}^2}}{\Delta f} = \frac{K_F}{C_{OX} W L f} \quad (3.12)$$

Regarding the amplifier design in [71], the input-referred noise voltage of amplifier are determined by the transconductance ratio between the input pair and the active load together with the process and design parameters. In the headphone amplifier, $I_{D3} = 5I_{D10}$ and $I_{D1} = 4I_{D10}$. According to the folded-cascode noise analysis in [70], the equivalent input-referred noise of amplifier can be approximated as follows:

$$\frac{V_{eq_APA}^2}{\Delta f} = 2 \left(\frac{K_{Fp}}{C_{OX} W_1 L_1 f} + \frac{K_{Fp}}{C_{OX} W_{10} L_{10} f} \frac{g_{m10}^2}{g_{m1}^2} + \frac{K_{Fn}}{C_{OX} W_3 L_3 f} \frac{g_{m3}^2}{g_{m1}^2} \right) \quad (3.13)$$

Substituting g_{mi} by $2\sqrt{\mu_i C_{OXi} \frac{W_i}{L_i} I_{Di}}$, the equation (3.13) can be simplified as

$$\frac{V_{eq_APA}^2}{\Lambda f} = \frac{2K_{Fp}}{C_{OX}W_1f} \left(\frac{1}{L_1} + \frac{L_1}{4L_{10}^2} + \frac{5K_{Fn}\mu_n L_1}{4K_{Fp}\mu_p L_3^2} \right) \quad (3.14)$$

In general, the mobility of electron is about three times that of holes whereas K_{Fn} is larger than K_{Fp} . In order to find the appropriate input pair channel length and simplify the analysis, one can ignore the flicker noise contributed by M_{10} and M_{11} due to $L_1 \ll L_{10}$. From the equation (3.14), there exists an optimised channel length for input pair such that the amplifier can offer the minimum input-referred noise with respect to the given design parameters.

Figure 3.30 Input-referred noise of amplifier versus the input pair channel length.

Fig. 3.30 shows the simulated input-referred noise of amplifier with different input pair channel length. It shows that the optimized channel length for the input pair is about $0.5\mu\text{m}$ to $0.6\mu\text{m}$. In order to minimize the parasitic capacitances of the input pair, the channel length of $0.5\mu\text{m}$ is used in the headphone amplifier.

Chapter 4 Measured Results and Discussions

Implemented and fabricated in 65-nm CMOS technology, the micrograph and Cadence layout drawing of the headphone amplifier is shown in Fig. 4.1 and Fig. 4.2, respectively. The total active area of the circuit is about 0.15mm^2 ($480\mu\text{m} \times 320\mu\text{m}$), in which the digital blocks and the power transistors contribute to about two thirds. Since the power transistors sink or source large current, they are placed close to the pad whilst far away from the core amplifier. In order to confirm the APA's performance from the design, the crucial parameters of headphone amplifiers are measured, which includes input-referred offset, THD+N, SNR, PSRR and pulse response.

Figure 4.1 The micrograph of the proposed headphone amplifier in 65-nm CMOS.

Figure 4.2 The Cadence layout drawing of the proposed headphone amplifier in UMC 65-nm CMOS.

4.1. Measured Input-referred Offset and Quiescent Power

The measurement results in Fig. 4.3 have shown that the input-referred offset of ten chips can be calibrated to be less than $85\mu\text{V}$ when compared to the maximum offset of 2.25mV without offset calibration. This is consistent with simulation results shown in the previous section and indicates that the comparator offset and spikes in the digital blocks do not degrade the resolution of the offset calibration circuit.

Figure 4.3 Measured input-referred offset of ten chips with/without offset calibration.

Fig. 4.4 depicts the measured quiescent power of ten chips with/without offset calibration. The average power of 10 chips with and without offset calibration is about 0.4mW and 0.46mW , respectively. Of particular interest, without calibration, the power consumption of the 10 chips varies from 0.39mW to 0.56mW . 4 chips out of 10 chips display the substantial increase of quiescent power from 25% or above with respect to that with calibration. It has validated that the offset calibration can reduce the induced quiescent power due to the input-referred offset.

Figure 4.4 Measured quiescent power consumption of ten chips with/without offset calibration.

4.2. Measured THD+N and SNR Results

The test chips are measured by the *Stanford Research System (SRS)* SR1 audio analyzer. Fig. 4.5 shows the FFT output signal of the amplifier with the 1 kHz sinusoidal input signal of $1.5V_{pp}$. It is noted that 0dB in the vertical axis represents $1V_{rms}$ (0dB). All the harmonics are less than -100dB. The headphone amplifier has achieved -91dB THD at peak load power. Finally, the A-weighted THD+N and SNR at peak load power in the 20Hz-20kHz bandwidth are measured with -89dB and 93.5dB, respectively.

Figure 4.5 Measured output signal in FFT with the $1.5V_{PP}$ 1 kHz input sinusoidal wave.

Fig. 4.6 shows the measured A-weighted THD+N versus the output amplitude for 1 kHz input signal. It shows that the THD+N for the headphone amplifier decreases with the input signal level until $1.5V_{pp}$, which confirms that the peak output voltage is $1.5V_{pp}$. The THD+N for small signal input is high because the SNR will drop for low level input signal. With the increase of input signal, the SNR will increase, thus resulting in lower THD+N. Fig. 4.7 shows the A-weighted THD+N having different signal frequencies at peak load power. For the low frequency signal, the flicker noise of amplifier deteriorates the SNR, but displaying better linearity. The combined effect

results in lower THD+N at low frequencies. On the other hand, with increasing the input signal frequency, the distortion increases due to the drop of open-loop gain. Finally, the high-frequency harmonics in the audio band decreases with the increasing frequency, thus contributing to the improved THD+N if the distortion does not significantly degrade the SNR [3], [72].

Figure 4.6 Measured THD+N versus output amplitude for 1 kHz input signal.

Figure 4.7 Measured THD+N versus signal frequency with 1.5V_{PP} input sine-wave signal.

4.3. Measured PSRR Results

Fig. 4.8 shows the FFT plot of the amplifier's output in response to the 700mV_{PP} 217 Hz input signal which is applied on the positive power supply of amplifier. The measured PSRR+ can be obtained with the ratio of the input and output AC signal at 217 Hz, which has the value of 84dB. Similar measurement is also conducted on the negative power supply of amplifier. Fig. 4.9 shows that the PSRR- is 105dB at 217 Hz.

Figure 4.8 Measured PSRR+ at 217Hz with 700mV_{PP} on the 1V positive supply.

Figure 4.9 Measured PSRR- at 217Hz with 700mV_{PP} on the 1V negative supply.

4.4. Measured Pulse Response

The simulation results for the frequency response in previous section have indicated that the proposed APA can drive a capacitive load range of 0-2nF. Fig. 4.10 shows the measurement result of a rectangular input waveforms of 50kHz and 500mV with the load of 1nF//16Ω. In order to verify the driving capability of the proposed headphone amplifier, the large-signal pulse responses of the amplifier at different capacitive loads in parallel with the resistive load are compared and shown in Fig. 4.11. There is no significant peaking or ringing in the measured pulse response. This means that the amplifier can drive the maximum load of 2nF//16Ω. The measured results also show that the proposed APA can achieve the slew rate of 1.1V/μs.

Figure 4.10 Measurement result of a rectangular input waveforms of 50kHz and 500mV with the load of 1nF//16Ω.

Figure 4.11 The pulse response of the headphone amplifier with the respective load of $16\Omega//8\text{pF}$, $16\Omega//300\text{pF}$, $16\Omega//1\text{nF}$ and $16\Omega//2\text{nF}$.

4.5. Performance Comparison

Table 4.1 shows the performance comparison of the headphone amplifier with the recently-published state-of-the-art works. Among the topologies, the proposed amplifier consumes the quiescent power of 0.4mW and requires a total compensation capacitance of 8.5pF, which are considered as the lowest values. The peak THD+N is -89dB, which is higher most of the recently-published state-of-the-art works. The PSRR is 84dB and it is comparable to [5] and the product in [12]. The work in [8] is powered by LDO so that it can provide a high PSRR of 110dB. At the same juncture, it also provides the comparable performance metrics such as A-weighted SNR, GBW and slew rate. The capacitive load range is 0-2nF, which is lower than [2], [3], [5] but higher than the product in [12]. The FOM1, which is defined as the ratio of the peak power over the quiescent power, is obtained as 87.9. Another figure of merit FOM2, which is defined as the ratio of FOM1 over THD+N in percentage, is compared. Both FOM1 and FOM2 have displayed the highest values among those of the reported works, demonstrating the effectiveness of two circuit techniques in the low-quiescent high-performance headphone amplifier design.

Table 4.1 Performance comparison of reported prior-art results.

Parameters	[12] Maxim 2002	[2] ESSCIRC 2006	[3] JSSC 2009	[5] TCASII 2012	[6] VLSIC 2012	[7] JSSC 2012	[8] JSSC 2014	This work
Process (nm)	NA	65	130	500	40	130	40	65
Supply (V)	3.0	2.5	1.2/2.0	3.0	1.1/1.8	1.5	3.1/4.5	2.0
Resistive load (Ω)	16	16	16	16	16	16	16	16
Capacitive Load (F)	0-300p	0-12n	1pF-22n	10p-5n	NA	NA	NA	0-2n
Gain (dB)	60	NA	NA	51.5	NA	NA	NA	113
Phase Margin ($^{\circ}$)	40	NA	>45	72	NA	NA	NA	> 45
GBW (MHz)	2.5	NA	4	1.23	NA	NA	NA	1.78
PSRR@ 217Hz (dB)	90	NA	NA	70	92	NA	110*	84
Slew Rate (V/ μ s)	0.8	NA	0.4	1.2	NA	NA	NA	1.1
Quiescent Power (mW)	12.0	12.5	1.2	1.43	5.2	1.5	3.8	0.4
Output Voltage (V_{PP})	2.5	1.85	1.6	2.45	1.41	2.5	3.24	1.5
A-weighted SNR (dB)	95	NA	92	79.9	100	98	100	93.5
Peak THD+N (dB)	-90	-68	-84	-77.9	-91	-72	-84	-89
Total Compensation Capacitance (pF)	NA	35	14	16.3	NA	NA	NA	8.5
FOM1 &	8.1	4.3	33.3	65.8	6	65.3	43.4	87.9
FOM2 [#]	2561	108	5278	5167	2129	2600	6878	24774

*: Powered by LDO regulator and charge pump

&: FOM1=(Peak load power)/(Quiescent power)

#: FOM2=(Peak load power)/(Quiescent power*THD+N (%))

Chapter 5 Conclusions and Future Works

5.1. Conclusions

A low-offset low-quiescent power class-AB headphone amplifier has been proposed and discussed together with the measurement results and the detailed analysis in this thesis. Two key low-quiescent design techniques for headphone amplifier have been introduced.

Firstly, the digitally-assisted offset calibration circuit architecture is able to reduce the mismatch-induced quiescent current caused by the input-referred offset of amplifier without jeopardizing the PSRR as well as DC gain. The reduction of the input-referred offset is achieved by digitally injecting current into the differential stage. Several digital blocks are implemented to detect the offset value and control the injected current. The low-offset technique is of great importance for power amplifier with the decreasing of the device size in advanced CMOS technologies.

Secondly, the improved frequency compensation permits the amplifier to drive the worst case load of $16\Omega//2nF$ whilst sustaining good stability and providing good GBW at low power. In the conventional frequency compensation topology, the assumption about the third-stage gain is not applicable for headphone amplifier. Therefore, an improved frequency compensation technique called NMCFNR2 that can be applied in the power amplifier is introduced. Other performance metrics like PSRR, THD+N, SNR are obtained with comparable performance. The amplifier outperforms the prior-art works by achieving the best power-related FOM1 and power-(THD+N) related FOM2, demonstrating the efficiency from quiescent state to full power state.

5.2. Future Work

For the power supplies of headphone amplifier, the voltage ripple of the switching noise at 217Hz can be as high as several hundreds of mV. The proposed headphone amplifier in this circuit has achieved positive PSRR of 84dB@217Hz, which is comparable with other works. Nevertheless, the PSRR should be improved further to minimise the impact of the supply noise over the output signal.

The offset calibration circuit proposed in this thesis has achieved relatively low offset. However, the architecture of the calibration circuit produces glitches in the amplifier output signal during the offset calibration period. Future work will focus on the glitch reduction circuit techniques for the power-on start-up and the calibration circuit. In addition, the successive approximation algorithm can be used in the circuit to generate the approximate offset cancellation current after eight clock cycles. Not only does this algorithm save the required offset calibration time, it also reduces the dynamic leakage current.

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