Engineering memristor : control over the fourth fundamental element for memory application and beyond

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NANYANG
TECHNOLOGICAL
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**ENGINEERING MEMRISTOR: CONTROL OVER THE
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Abstract

In 1971 Prof. Leon Chua predicted that on top of the three known fundamental passive elements, the capacitor, the resistor, and the inductor that were discovered in 1745, 1827, and 1831 respectively, there should be a fourth fundamental two-terminals non-volatile device, which he called memristor after the name of memory-resistor. However, it was only a theory for nearly thirty years until the first paper published by HP Labs by the Stanley Williams group in Nature on May 1st, 2008. This announced the first materialization of the memristor, the fourth fundamental element device. Since then, memristor work has gained a tremendous increase in interest due to its unique idiosyncrasy and its special analog properties. This is especially shown in the recent neuromorphic computing since both neuron and memristor operate in ions. In many ways, a memristor is very similar to a synapse (a biological connection between two neurons), which is able to modulate and tune the efficiency of signal transmission between neurons with a high level of plasticity. Memristor based neuron chips can be astonishingly better than conventional CMOS digital approaches in pattern recognition in high speed, low power and parallel processing. The eventual goal is that computer chips can think like human brains too.

Since the announcement of HP's groundbreaking news, numerous papers aimed to analyze the special attributes of the memristor have been published. Moreover, various publications have been submitted for memristor fabrication, modeling, and applications. However, until today many fundamental questions, including an accurate understanding of the switching mechanism, availability for high quality selector devices, and implementation the fundamental element to the novel circuit design etc., are still in question. This work will try to study the fundamental memristor devices including material impact, device characterization, physical modeling, and selector device choice, then apply its unique property to novel applications using various process methods. The ultimate goal is to understand the memristor device deeply and gain control over this fourth fundamental device for memory applications and beyond. In the detailed work depicted here, a comprehensive material dependence of the memristor devices has been conducted and optimized through various physical analysis and electrical testing. Subsequently, a physical compact model for TaO_x systems was developed and calibrated with electrical tests. This was the first two-state-variable device model with high accuracy for practical circuit design and simulation applications. A series of selector work aimed to minimize the sneak path issue was also investigated for the large scale crossbar application. Finally, the selected applications from this study will be introduced from the research work on hamming distance computation, vector production, and neuromorphic computing.

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List of abbreviations

ADC	Analog to Digital Converter
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ARC	Anti Reflective Coating
ARM	Advanced Reduced-instruction-set-computing Machine
APU	Advanced Processing Units
BE	Bottom Electrode
BEOL	Back End Of Line
CBRAM	Conductive Bridge Random Access Memory
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CPU	Central Processing Units
CVD	Chemical Vapor Deposition
DFM	Design For Manufacturability
DFT	Discrete Fourier Transform
DOE	Design Of Experiments
DPE	Dot Product Engine
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
ECM	Electrochemical Metallization Memory
EDA	Electronic Design Automation
EELS	Electron Energy Loss Spectroscopy
FEOL	Front End Of Line
FFT	Fast Fourier Transform
FN Tunneling	Fowler–Nordheim Tunneling

FPGA	Field-Programmable Gate Array
GFLOPS	Giga-Floating Point Operations Per Second
GPU	Graphics Processing Units
HRS	High Resistance State
HRTEM	High Resolution Transmission Electron Microscopy
IC	Integrated Circuit
ILD	Inter-Layer Dielectrics
IMT	Insulator Metal Transition
IoT	Internet of Things
ISR	Intelligence, Surveillance and Reconnaissance
IV	Current-Voltage
KCL	Kirchhoff Current Law
LRS	Low Resistance State
MCA	Memristive Crossbar Array
MIEC	Mixed Ionic Electronic Conduction
MIM	Metal Insulator Metal
MIMO	Multiple Input Multiple Output
MIT	Metal Insulator Transition
MLP	Multi-Level Programming
MSM	Memristive Switching Material
MTJ	Magnetic Tunnel Junction
NDR	Negative Differential Resistance
OTS	Ovonic Threshold Switching
PC-RAM	Phase-Change Random Access Memory
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEALD	Plasma Enhanced Atomic Layer deposition
PTS	Parametric Test Structure

PVD	Physical Vapor Deposition
RIE	Reactive Ion Etching
SCCM	Standard Cubic Centimeters per Minute
SEM	Scanning Electron Microscope
SNR	Signal-to-Noise Ratio
SOC	System On Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
STDP	Spike-timing-dependent Plasticity
STEM	Scanning Transmission Electron Microscope
STT-RAM	Spin-Transfer Torque Random-Access Memory
TDK	Technology and Design Kit
TE	Top Electrode
TEM	Transmission Electron Microscopy
TIA	Trans-Impedance Amplifier
TLG	Threshold Logic Gate
TLTB	Tri-Layer Tunnel Barrier
TMD	Transition Metal Dichalcogenide
TMO	Transition Metal Oxides
VCB	Volatile Conducting Bridge
XPS	X-ray Photoelectron Spectroscopy

Chapter 1 Introduction

1.1 Memristor fundamentals

1.1.1 Background

In today's classic electrical text books, there are only three well-known fundamental passive circuit elements: the capacitor, discovered in 1745 by Ewald Georg von Kleist; the resistor, discovered in 1827 by Georg Simon Ohm; and the inductor, discovered in 1831 by Michael Faraday and Joseph Henry. The relationships between the charge, current, flux, and voltage (q , i , ϕ and v) have been well established for the three classic device components:

$$dv = Rdi \quad (1.1)$$

$$dq = Cdv \quad (1.2)$$

$$d\phi = Ldi \quad (1.3)$$

where R is resistance, C is capacitance, and L is inductance. Charge q and flux ϕ have been defined with respect to time t also:

$$dq = Idt \quad (1.4)$$

$$d\phi = Vdt \quad (1.5)$$

With these five different mathematical relations between the four fundamental circuit variables having been setup, one can find that there is no definition relating ϕ to q . Thus, there should be a missing basic circuit element to describe the remaining relation. In 1971, Prof. Leon Chua proposed that, in theory, there should be a fourth fundamental passive circuit element giving a mathematical relationship between ϕ to q . From the relationship, he defined the memristor using a portmanteau of memory and resistor [1]. From the newly defined memristor, the following mathematic relationship can be established:

$$d\phi = Mdq \quad (1.6)$$

where M is memristance.

Chua did mathematical proofs of circuit function and bounds and also proved that there is no equivalent circuit to the M function which could be made using any R , C , and L passive device components only. In other words, M is a new and unique 'basis function'. The eventual resistance of the memristor device is a result and function of the historical current or charge that has traveled through the device in the past. Even after the device is isolated from any power supply, the resistance value will remain the same as before the electrical isolation. Therefore, memristor is a kind of nonvolatile

resistive device. Now, the whole system is completed in harmony and shown in Fig. 1 as below:

Figure 1 Four fundamental circuit elements with five intervened parameters

Memristance was originally defined strictly as a function of the state variable q , but it was further generalized by Chua and his student S. M. Kang in their publication in 1976 on the topic of memristive devices and systems [1] [2]. In that paper, Chua generalized the concept and introduced the differential formulation of memristive systems, which included memcapacitor and meminductor. After that memristor existed only in theory for nearly thirty years. But many papers were published which showed memristive switching behaviors in the micrometer-scale and nanometer-scale devices. These devices were built out of polymers and metal oxides for various memories and Complementary Metal Oxide Semiconductor (CMOS) studies over the past four decades, but none of them realized that this “anomalous” current-voltage behavior was memristive behavior [3] [4]. At that time these idiosyncrasies were believed to be from certain mysteries electrical breakdown, electrochemical reaction, or other spurious electrical phenomenon, which could be resulted from the high voltages applied to those devices [4]. During the study of nanometer-scale crossbar, the research group from HP Labs led by Dr. Stanley Williams realized that they have found the missing link for the memristor device. The “anomalous” current-voltage behavior showing resistance switching phenomenon, was actually memristive idiosyncrasy, which was exactly as predicted by Chua’s theory. The paper published by HP Labs research group on May 1, 2008 in Nature, announced the first materialization of the memristor with the intention of dedicated memristive switching purposes [3]. After the Nature paper, numerous papers were published studying the memristor due to its wide potential applications.

Memristors are generally solid-state nanoscale devices that are normally constructed from Metal-Insulator-Metal (MIM) multi-layered sandwich structures. The insulator referred to as Memristive Switching Material (MSM) usually consists of a

thin-film oxide or sometimes other material including nitrides [5]. The main reason that memristors attract significant interest is because they will not only extend the Moore's Law to the next generation high density nonvolatile memory [6] [7], but also it can be used for many types of new system applications. Comparing to Random Access Memory (RRAM), which has a similar structure, memristor asserts more applications other than the memory applications: their dynamically nonlinear switching also suggests great potential for alternate nonvolatile logic circuits [8] [9] for in-memory computing, neuromorphic computing for artificial intelligence [10], etc.

1.1.2 Memristor fundamental theory survey

Similar to other solid state devices, the memristor fundamentals are originated from theories of electromagnetic fields. The electromagnetic field theory is well defined by Maxwell's equations. The differential forms of Maxwell's equations are shown below:

$$\nabla \cdot \mathbf{D} = \rho \quad (1.7)$$

$$\nabla \cdot \mathbf{B} = 0 \quad (1.8)$$

$$\nabla \times \mathbf{E} = - \partial \mathbf{B} / \partial t \quad (1.9)$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \partial \mathbf{D} / \partial t \quad (1.10)$$

where D is the electric flux density or electric displacement field in the unit of C/m^2 , ρ is charge density in the unit of C/m^3 , B is magnetic flux density in the unit of Wb/m^2 , E is electric field in the unit of V/m , H is magnetic field in the unit of A/m , and J is current density in the unit of A/m^2 . In free space, D , B and J can be further interpreted as below:

$$\mathbf{D} = \varepsilon_0 \mathbf{E} + \mathbf{P} \quad (1.11)$$

$$\mathbf{B} = \mu_0 (\mathbf{H} + \mathbf{M}) \quad (1.12)$$

$$\nabla \cdot \mathbf{J} = - \partial \rho / \partial t \quad (1.13)$$

where ε_0 is permittivity of free space, μ_0 is permeability of free space, P is the electric polarization, H is magnetic field, and M is the magnetization field.

The main characteristic of Maxwell's equation is that the electric field can be determined by the magnetic field through the time variation of $\mathbf{B}$ as indicated in equation 1.9. The magnetic field can be derived by the electric field through the time variation of $\mathbf{D}$ as indicated in equation 1.10. In other words, time derivative of $\mathbf{D}$ acts as a source of $\mathbf{H}$ and time derivative of $\mathbf{B}$ acts as a source of $\mathbf{E}$, so that the coupling between electric and magnetic fields becomes bilateral. Circuit theory is a limiting special subset of it. In particular, quasi-static expansion of Maxwell's equations can give an electromagnetic interpretation for the characterization of the three classical

circuit elements: Resistor, Capacitor, and Inductor [11]. The key characteristic of a quasi-static electromagnetic field is to involve successive approximations from the time-varying fields. The method of successive approximation is an attempt to circumvent the simultaneous solution of Maxwell's equations by substituting an infinite series of unidirectional coupling from the time derivatives of $\mathbf{D}$ and $\mathbf{B}$ for the bilateral coupling of $\mathbf{D}$ and $\mathbf{B}$. When a time rate parameter α is defined (which can be defined as the time rate of change of charge density ρ), we can study the electrical circuits in which time variations of electromagnetic fields are slow by introducing a new variable τ .

$$\tau = \alpha t \quad (1.14)$$

In terms of the new variable τ , we can find the derivatives of $\mathbf{B}$ and $\mathbf{D}$ in following manner:

$$\frac{\partial \mathbf{B}}{\partial t} = \frac{\partial \mathbf{B}}{\partial \tau} \frac{d\tau}{dt} \quad (1.15)$$

$$\frac{\partial \mathbf{D}}{\partial t} = \frac{\partial \mathbf{D}}{\partial \tau} \frac{d\tau}{dt} \quad (1.16)$$

The Maxwell's equations of 1.9 and 1.10 will be:

$$\nabla \times \mathbf{E} = -\alpha \frac{\partial \mathbf{B}}{\partial \tau} \quad (1.17)$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \alpha \frac{\partial \mathbf{D}}{\partial \tau} \quad (1.18)$$

$\mathbf{E}$, $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$ and $\mathbf{B}$ then can be expanded in a formal power series time-rate variable α . For instance, $\mathbf{E}$ can be expressed in the power series in α as below:

$$\mathbf{E}(x, y, z, \tau, \alpha) = \sum_{i=0}^n \alpha^i \mathbf{E}_i(x, y, z, \tau) \quad (1.19)$$

where $n=0,1,2,\dots$ and

$$\mathbf{E}_0(x, y, z, \tau) = [\mathbf{E}(x, y, z, \tau, \alpha)]_{\alpha=0} \quad (1.20)$$

$$\mathbf{E}_1(x, y, z, \tau) = \left[\frac{\partial \mathbf{E}(x, y, z, \tau, \alpha)}{\partial \alpha} \right]_{\alpha=0} \quad (1.21)$$

$$\mathbf{E}_n(x, y, z, \tau) = \frac{1}{n!} \left[\frac{\partial^n \mathbf{E}(x, y, z, \tau, \alpha)}{\partial \alpha^n} \right]_{\alpha=0} \quad (1.22)$$

From equation 1.19, we can obtain the n th order Maxwell's equation for $\mathbf{E}$ upon equating α^n . $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$ and $\mathbf{B}$ can be obtained in the similar way.

It is assumed that, in this regard, all the series can be differentiated term by term with respect to the independent variables x , y , z , and τ . With the introduction of equation 1.19, equation 1.17 can be expressed as below:

$$\nabla \times \mathbf{E} = \nabla \times \mathbf{E}_0 + \alpha(\nabla \times \mathbf{E}_1) + \dots + \alpha^n(\nabla \times \mathbf{E}_n) \quad (1.23)$$

Then, if all the terms in each equation are combined on one side, equation 1.17 will be derived into the form of a power series in α equating to 0, as below:

$$\nabla \times \mathbf{E}_0 + \alpha \left(\nabla \times \mathbf{E}_1 + \frac{\partial \mathbf{B}_0}{\partial \tau} \right) + \alpha^2 \left(\nabla \times \mathbf{E}_2 + \frac{\partial \mathbf{B}_1}{\partial \tau} \right) \dots + \alpha^n \left(\nabla \times \mathbf{E}_n + \frac{\partial \mathbf{B}_{n-1}}{\partial \tau} \right) = 0 \quad (1.24)$$

Similarly, $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$ and $\mathbf{B}$ can be obtained in the same way. The derived equation of 1.24 will be satisfied for all values of α . That means equation 1.24 will only be true when the coefficients of all the power of α are separately equal to zero. This will be applied to the rest of the equations for $\mathbf{H}$, $\mathbf{D}$, $\mathbf{J}$ and $\mathbf{B}$'s. In this case, equations 1.17 and 1.18 can be obtained in n th-order Maxwell's equations, where $n=0, 1, 2, \dots$. Many circuit theories can be analyzed using zero-order and first-order Maxwell's equation with a good approximation [11]. The corresponding results from the approximation are called quasi-static fields, as mentioned earlier. The zero-order and first-order Maxwell's equation can be obtained as below:

Zero-order Maxwell's equation:

$$\nabla \times \mathbf{E}_0 = 0 \quad (1.25)$$

$$\nabla \times \mathbf{H}_0 = \mathbf{J}_0 \quad (1.26)$$

First-order Maxwell's equation:

$$\nabla \times \mathbf{E}_1 = -\alpha \frac{\partial \mathbf{B}_0}{\partial \tau} \quad (1.27)$$

$$\nabla \times \mathbf{H}_1 = \mathbf{J}_1 + \frac{\partial \mathbf{D}_0}{\partial \tau} \quad (1.28)$$

For the quasi-static approximation, only the first two terms of the power series in equations 1.25-1.27 are kept [1] [11]. At any moment, the rest of the power series can be neglected. In this case, the following approximation can be obtained: $\mathbf{E} \approx \mathbf{E}_0 + \mathbf{E}_1$, $\mathbf{D} \approx \mathbf{D}_0 + \mathbf{D}_1$, $\mathbf{H} \approx \mathbf{H}_0 + \mathbf{H}_1$, $\mathbf{B} \approx \mathbf{B}_0 + \mathbf{B}_1$, and $\mathbf{J} \approx \mathbf{J}_0 + \mathbf{J}_1$.

The three classic circuit elements (resistor, capacitor, inductor) can be solved in the electromagnetic systems with quasi-static approximate solutions corresponding to zero-order and first-order from those derived equations. For example, a resistor can be explained when first-order fields are negligible. By this approximation, the resistor can be characterized by a function of two zero-order fields, E_0 and B_0 . In this case, the resistor is instantaneous. In other words, it is memory-less. Similarly, the capacitor and inductor can be characterized by the same approach with the first-order fields negligible in the electromagnetic system.

Chua's argument is based on those new postulated devices having two important properties: 1) whose first-order electric and magnetic fields are not negligible but the zero-order fields are negligible comparing to the first-order fields; 2) the material from

which the device is made is nonlinear, i.e., nonlinear conductivity, nonlinear magnetic permeability or nonlinear dielectric permittivity. With these assumptions, the following approximations can be obtained for those new nonlinear devices: $\mathbf{E} \approx \mathbf{E}_1$, $\mathbf{D} \approx \mathbf{D}_1$, $\mathbf{H} \approx \mathbf{H}_1$, $\mathbf{B} \approx \mathbf{B}_1$, and $\mathbf{J} \approx \mathbf{J}_1$.

Assume that the nonlinear relationships between the first-order fields can be expressed as:

$$\mathbf{J}_1 = \boldsymbol{\sigma}(\mathbf{E}_1)\mathbf{E}_1 = \mathcal{J}(\mathbf{E}_1) \quad (1.29)$$

$$\mathbf{B}_1 = \boldsymbol{\mu}(\mathbf{H}_1)\mathbf{H}_1 = \mathcal{B}(\mathbf{H}_1) \quad (1.30)$$

$$\mathbf{D}_1 = \boldsymbol{\varepsilon}(\mathbf{E}_1)\mathbf{E}_1 = \mathcal{D}(\mathbf{E}_1) \quad (1.31)$$

$\boldsymbol{\sigma}(\mathbf{E}_1)$, $\boldsymbol{\mu}(\mathbf{H}_1)$ and $\boldsymbol{\varepsilon}(\mathbf{E}_1)$ are the nonlinear conductivity, nonlinear magnetic permeability and nonlinear dielectric permittivity of the material, respectively. $\mathcal{J}$, $\mathcal{B}$, and $\mathcal{D}$ are nonlinear functions of the respective first-order fields over the space coordinates. Substituting equation 1.29 into equation 1.30, we have:

$$\nabla \times \mathbf{H}_1 = \mathbf{J}_1 + \frac{\partial \mathbf{D}_0}{\partial \tau} = \mathcal{J}(\mathbf{E}_1) + \frac{\partial \mathbf{D}_0}{\partial \tau} \quad (1.32)$$

As we have assumed earlier, all zero-order fields are negligible, therefore, $\mathbf{D}_0 = 0$. Equation 1.32 will be reduced to:

$$\nabla \times \mathbf{H}_1 = \mathcal{J}(\mathbf{E}_1) \quad (1.33)$$

The above relationship can be re-written as:

$$\mathbf{E}_1 = \mathcal{F}(\mathbf{H}_1) \quad (1.34)$$

Substituting equation 1.33 into equation 1.31, we obtain

$$\mathbf{D}_1 = \mathcal{D}(\mathbf{E}_1) = \mathcal{D}(\mathcal{F}(\mathbf{H}_1)) \quad (1.35)$$

From equation 1.30, we obtain

$$\mathbf{H}_1 = \mathcal{B}^{-1}(\mathbf{B}_1) \quad (1.36)$$

Substituting 1.35 into 1.34, we get the final relationship:

$$\mathbf{D}_1 = \mathcal{D}(\mathcal{F}(\mathbf{H}_1)) = \mathcal{D}(\mathcal{F}(\mathcal{B}^{-1}(\mathbf{B}_1))) = \mathcal{M}(\mathbf{B}_1) \quad (1.37)$$

Equation 1.37 predicts that a nonlinear relationship can be established between $\mathbf{D}_1$ and $\mathbf{B}_1$ using quasi-static expansion of Maxwell's equations, which is an instantaneous relationship and memoryless. In other words, there could be a solid-state device with two-terminals, in which $\mathbf{D}_1$ is related to $\mathbf{B}_1$ and these quantities are evaluated simultaneously. This can be interpreted as the quasi-static representation of the electromagnetic field quantities of the memristor, in which a monotonically increasing φ - q curve can be established. This completes Chua's logic and scientific

basis using Maxwell's equations in quasi-static approximation to theorize the existence of a new two-terminal device of memristor. Recall equation 1.4 and 1.5 in the integration form:

$$q(t) \triangleq \int_{-\infty}^t i(\tau) d\tau \quad (1.38)$$

$$\varphi(t) \triangleq \int_{-\infty}^t v(\tau) d\tau \quad (1.39)$$

In [12], Chua extended the q and φ definition to more generic form of generic charge and flux of the memristor. In other words, the magnetic field may not be needed for memristor operation as a compulsory physical element. The interaction relationship between charge and magnetic flux becomes one way of expressing the relationships to satisfy the memristor definition, but now it is not the only possible definition of the device. φ is defined as flux, for which, voltage is integrated with time. Based on the control mechanism, a memristor is defined as charge-controlled if $\varphi = \hat{\varphi}(q)$ and memristor is flux-controlled if $q = \hat{q}(\varphi)$. Voltage v can be derived as below:

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq} \frac{dq}{dt} = R(q)i \quad (1.40)$$

where $R(q)$ is called memristance at q in unit of Ohms with the following definition:

$$R(q) \triangleq \frac{d\hat{\varphi}(q)}{dq} \quad (1.41)$$

Similar, current i can be derived as below:

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi} \frac{d\varphi}{dt} = G(\varphi)v \quad (1.42)$$

where $G(\varphi)$ is called memductance at φ in unit of Siemens with the following definition:

$$G(\varphi) \triangleq \frac{d\hat{q}(\varphi)}{d\varphi} \quad (1.43)$$

From equations 1.40-1.43, the memristor memristance $R(q)$ at any given time t_0 depends on the history of the past of $i(t)$ from $t = -\infty$ to $t = t_0$ or memristor memductance $G(\varphi)$ at given time t_0 depends on the entire past history of $v(t)$ from $t = -\infty$ to $t = t_0$ for charge-controlled and flux-controlled memristor, respectively. In other words, memristor is a memory resistor, which remembers the past history of the current or voltage passed. For the generalized Ohm's law, we can have the following expression:

$$v = R(x, i)i \quad (1.44)$$

$$\frac{dx}{dt} = f(x, i) \quad (1.45)$$

where $R(x, i)$ is state-dependent resistance and x is state-dependent variable.

1.1.3 Materializing the state-dependent memristor

As defined in equation 1.44 and 1.45, Chua provided an axiomatic definition for memristors: all solid non-volatile memory devices with two-terminals based on resistance switching are memristors, regardless its construction material and operating mechanism [12]. In order to demonstrate the behavior of a memristor for a single device, Chua constructed an emulator circuit in [1], which consisted of a complex circuit with more than fifteen passive elements and transistors. After proving the concept, the question is how to physically materialize the non-volatile resistance switching device with the state-dependent variable using a single solid-state device.

During the crossbar molecular switch devices study, Williams and his team found that a resistance switch can be formed between stoichiometric titanium dioxide TiO_2 and sub-stoichiometric (oxygen-deficient) titanium dioxide TiO_{2-x} , where x is a small numeric with value about 0.05 (in later sections sub-stoichiometric titanium dioxide may be denoted as TiO_x also for simplification reason, where x is different numeric with value between 0 to 2). The TiO_{2-x} is more than 1000 times more conductive than the stoichiometric TiO_2 . More importantly, Williams found that current–voltage (IV) characteristic curves they have measured, which he called it “pinched-hysteresis loops”, is nearly identical to what Chua had illustrated for memristor. A pinched hysteresis loops IV curve looks like a diagonal “bow tie” with the voltage and current center crossed at the origin. The voltage is initially increased from 0 to certain positive value, then decreased to an opposite polarity value (negative voltage value), and finally the voltage will be returned to 0 (see Fig. 2). Because the device will “memorize” the history of the voltage applied, the current has different levels at same voltage levels on the “increasing” and “decreasing” paths. In other words, the device has a state-dependent resistance.

Figure 2 Memristor Lissajous figure of pinched-hysteresis loops (adapted from [2]). In the figure it indicates that the hysteresis loop becomes closer as the frequency of the circuit increase and tents to be straight line as the frequency goes infinite. In that case, memristor just behaviors as an ideal resistor.

In William’s memristor, the state-dependent resistance is the resistance of a TiO_2 and TiO_{2-x} bilayer. For memristor switching, the key is to change the state and

composition of bilayer. As we know, TiO_2 is a fairly wide-band gap material (actually it has been used as high-K insulating material for the transistor gate), but the TiO_{2-x} is very conductive because of its oxygen vacancies acting as positively charged carrier. These oxygen vacancies were found to be moved under certain voltage bias. Consider the bilayer acts like two serial resistors connected back to back, one resistor is controlled by high resistive TiO_2 layer (considered as full stoichiometric titanium oxide or un-doped oxide) and another resistor is controlled by very low resistive TiO_{2-x} layer (considered as oxygen deficient titanium oxide or doped oxide). When certain positive voltage is applied to the Top Electrode (TE) of the bilayer device, it attracts the oxygen ions towards TE and leaving the oxygen vacancies, which effectively repels the positively charged oxygen vacancies in the TiO_{2-x} layer more into the pure TiO_2 layer. That depletes the effective thickness of TiO_2 layer and increasing the effective thickness of TiO_{2-x} layer (Fig. 3a). The overall resistance drops and sets the device into ON state. When a negative voltage is applied, the memristor will have the opposite effect: the positively charged vacancies are attracted to the Bottom Electrode (BE) and back out of the TiO_2 , and thus, the effective electrical thickness of the TiO_2 layer increases and the device becomes much more resistive, which is turned off (Fig. 3b). By manipulating the bias voltage, we can change the state-dependent resistance.

Figure 3 Bilayer switching of HP titanium oxide memristor. a) under positive bias voltage oxygen ions drift to the TE, which will narrow the tunneling gap and reduce overall resistance; b) under negative bias voltage oxygen ions will be repelled to the BE, which will increase the tunneling gap and increase overall resistance.

The schematic of the bilayer model of HP memristor and switching curve is shown as below:

Figure 4 Vacancy drift model of bilayer TiO_2 memristor. a)&b) Positive and negative switching as described according to Figure 3 a) & b); c) physically bounded memristance from region $[0,L]$, exponentially decreasing rate when approaching bounds; d) HP titanium oxide typical switching curve

From the vacancy drift model of bilayer TiO_2 memristor and equation 1.44, the following IV equation can be derived:

$$v(t) = M(q)i(t) = (R_{off} \frac{w(t)}{L} + R_{on}(1 - \frac{w(t)}{L}))i(t) \quad (1.46)$$

The memristance of the bilayer device is controlled by the size of the doped region $w(t)$ with a time dependence. In the much simplified linear-drift model, the boundary between the doped and undoped regions drifts along the electrical field with a constant speed v_D , which is governed by the equation:

$$\frac{dw(t)}{dt} = v_D = \mu_V \frac{R_{on}}{L} i(t) \quad (1.47)$$

where μ_V is mobility of the ion and we assumed that a current $i(t)$ corresponding to a uniform electric field, $\frac{R_{on}}{L} i(t)$, is across the doped region. Integration of equation 1.47 will lead to the state variable $w(t)$ for the drift front:

$$w(t) = w_0 + \mu_V \frac{R_{on}}{L} q(t) \quad (1.48)$$

where w_0 is the initial width of the doped region. Thus, the width of the doped region $w(t)$ will change in a linear way depending on the amount of historical charge that has passed through it. Substituting equation 1.48 into equation 1.46 will lead to:

$$M(q) = R_{off}(1 - \mu_V \frac{R_{on}}{L} q(t)) \quad (1.49)$$

Equation 1.49 implies that the derived equation fits Chua's ideal memristor model. If we recall, Chua's general memristor definition has essentially two parts of equations: Equation 1.44 defines how the memristor voltage depends on current and the state-dependent variable (the state-dependent resistance). The state-dependent variable could be a quantity measurement of some physical property of a device. In HP Labs' titanium oxide memristor, the state-dependent variable is essentially the effective thickness of the non-stoichiometric TiO_{2-x} in the bilayer switch. Through applied voltage polarity and electrical field strength, thickness of the non-stoichiometric titanium dioxide will change. The increase or decrease in the non-stoichiometric titanium dioxide thickness will cause the memristor resistance to decrease or increase accordingly. The second equation of memristor (equation 1.45) expresses how the change in the state-dependent variable depends on the amount of historical charge (current integrated by time) flowing through the device. In other words, the history of current that the device has gone through under the applied external electrical field. In HP titanium oxide memristor, the TiO_2 's thickness depends on the distribution of the positively charged center (oxygen vacancies) throughout the device. For this newly found solid-state device, the resistance of these devices will not change even when the external voltage is removed. The small reading voltage will not change the resistance since the positive charged center remained immobile until a sufficient positive or negative voltage is applied again across the device. In other words, the memristor device can be used as a non-volatile memory device and beyond. Thirty five years after Chua predicted the memristor theory out of a mathematical construct, a memristor has finally been materialized intentionally with practical applications.

1.1.4 Memristor operations and lab testing

As we discussed earlier, memristors work on the mechanism of that the oxides behaving nominally as insulators then undergoing an abrupt switching event to transition them into a conductive state. Therefore the resistance of the device is switched between two resistance states: High-Resistance State (HRS) and Low-Resistance State (LRS). There are multiple electrical operations. The switching event from HRS to LRS is literally called "Set" process. The switching from LRS to HRS is called "Reset" process conversely. Sometimes the Set process is referred as switch "ON" process and the Reset process is referred as switch "OFF" process. For a lot of memristor devices, a larger voltage is usually required for the fresh samples (virgin state) in its initial resistance state change event than the "threshold" voltage needed to trigger the switching event for the subsequent switching cycles. This voltage is called "Electroforming Voltage" or simply "Forming voltage". The process for the virgin state switching event is called "Electroforming" or "Forming" process. According to the applied voltage polarity, there are broadly two different classified modes for the switching modes as shown below:

Figure 5 Set & Reset IV curve for unipolar and bipolar switching. a) unipolar switching: Set usually requires certain voltage with a compliance current control; Reset demands a large current for the thermal effect; there is no polarity requirement for Set & Reset switching b) bipolar switching: Set and Reset switching direction depends on the amplitude but not on the polarity of the applied voltage; normally a current compliance will be applied for both cases

Unipolar switching refers to a special type of switching, for which the switching direction depends on the amplitude but not on the polarity of the applied voltage. As a result, the Set and Reset can happen at the same polarity of the applied voltage. Nonpolar switching is a special case of Unipolar switching, which refers to the switching that can symmetrically occur at both positive and negative voltages. On the other hand, bipolar switching refers to the switching direction of Set and Reset depending on the polarity and amplitude of the applied voltage. As a result, the Set will happen at the one polarity and Reset will happen on the opposite polarity of the applied voltage. The LRS resistance from the switching can be very small. Therefore during the practical testing or memristor operation, a set of compliance current or voltage is always forced to avoid the device from permanent dielectric breakdown. Depending on the device fabrication structure and operation, many metal oxides can be switched in either Nonpolar or Bipolar switching modes according to the actual situation.

For memristor device characterization, we carried the following testing methods with different characterization purposes in HP Labs:

- Regular IV characterization
- Endurance testing
- Stress test protocol
- Low noise measurements (100 fA range)
- High frequency testing (up to 50 GHz)
- Variable temperature testing

For fundamental device studies, Quasi-DC voltage sweeps based on regular IV measurements are mostly used in this study for the characterization. There are two sets

of testing measurement systems we used in HP Labs: one uses Agilent 4155/6C Semiconductor Parameter Analyzer only and the other uses Agilent B1500A Semiconductor Device Analyzer together with a voltage source generator. For either of the two systems, a four-point probe method (Also known as Kelvin measurement) was used for memristor measurement through different pairs of current-carrying and voltage-sensing electrodes for more accurate measurements than conventional two-terminal sensing. Depending on the actual device type and structure, a forcing voltage will be swept from negative to positive or positive to negative for the Set and reverse polarity swept for the Reset. A current measurement will be conducted for memristor resistance calculation using ohm's law. A forming process may be needed by applying a higher Set voltage to form the conductive filaments as mentioned earlier. A compliance current is set to avoid the device from permanent dielectric breakdown since in the LRS the memristor resistance can be very low. For practical memory applications, this can be done by a memory cell selection transistor/diode or a series resistor. For electrical testing, the compliance current is normally governed and supplied by the semiconductor parameter analyzer hardware itself. Current compliances with various magnitudes are also used to obtain different resistance states after switching events. The voltages mentioned in this report are internal voltages (measured voltage drops on the device) instead of external voltages (applied voltages consisting of voltage drops on the device as well as on the wires and contacts). The internal voltages usually agree with the external voltages in the HRS states but could be much less than the external voltages in the LRS states.

1.2 Motivation of the research

Due to approaching the end of Moore's law scaling as well as the increased challenges in the continuous development of CMOS technology, there is a strong demand to search for other alternative emerging devices and technologies. These devices need to be compatible with current CMOS technology while continuing to provide enough performance in the next decade to go beyond the sub-ten nanometer scale. The need is especially more urgent for the non-volatile memory applications because of the enormous data storage requirement associated with the increased demands from big data and cloud applications. Memristor is initially proposed as a novel memory device since it offers a feasible technical solution to replace current work horse of flash and DRAM memories. In comparison to other competing emerging device including Phase-Change Random-Access Memory (PC-RAM) involving a solid-solid phase transformation material (e.g., $\text{Ge}_2\text{Sb}_2\text{Te}_5$) and Spin-Transfer Torque Random-Access Memory (STT-RAM) involving a Magnetic Tunnel Junction (MTJ), memristor (as a broad concept it will include Resistive Random-Access Memory (RRAM), which uses same architecture based on the current switch mechanism, but asserts a much narrower application) is a relatively new device. However it has been regarded as the most promising universal memory technology because of its low thermal issue, faster write latency, better scalability compared to PCRAM, smaller cell

structure, 3D stackability, and finally more fab friendly processing compared to STT-RAM. On top of these benefits, memristor has huge potential to build analog cross-point memory arrays for neuromorphic computing, computing in memory and implied logic operations.

Despite the progress that has been made during the extensive studies after HP Labs' materialization of the first memristor with intention using nanometer titanium dioxide films, many aspects, including memristor material optimization and characterization, switching mechanism, accompanying right selector devices, etc., are still under research and development. Understanding and controlling this novel element has become extremely necessary, as well as applications using its special attributes being another important area of interest. In this study, we are motivated to go through a systematic end-to-end study in order to give control over this fourth fundamental device for memory applications and beyond. The detailed material dependence of the memristor device is to be conducted through various physical analysis and electrical testing for the goal of device engineering optimization. A practical physics-based compact model for TaO_x systems need to be developed for production circuit simulation. Decent selector work is urgently needed to minimize the sneak path issue for the large scale crossbar applications. Finally, novel applications are highly desired from the research work to provide future novel applications.

1.3 Major contributions

Through HP Labs' research on memristors, more than 10 journal and conference papers have been published and more than 70 patents have been filed. In general, those journal papers and patents are led by the author if the author is listed as first author or lead inventor. The contributions would generally include initializing the concept, designing the experiments, device fabrication with assistance from fab process engineers, electrical testing and characterization, data analysis, and final report. The following is a list highlighting more specified contributions or breakthroughs that have been achieved in several aspects by the author:

1. Several low cost process techniques for the inexpensive memristors with moderate performance were invented by the author as lead inventor. Those memristors can be used as embedded memories for the consume products. The author also initialized and led the project with actual business case. A practical cost effective memristor solution is implemented in the current prototype for future production inside HP using a simple micron-sized NMOS technology. This made it possible to integrate this newly found circuit element into actual mass production for HP. In the process of technology development, more than 50 invention disclosures were filed into the invention disclose system. Among them 37 patent applications have been submitted to the US patent office to enable the low cost memristor technology.

2. The “treasure map” of metal electrodes to guide the material selection to optimize the memristor according to different requirements has been discovered and studied systematically in details. This will greatly save time for the material selection and open up many promising new opportunities for nano-electronics. In this work, the author designed the experiments, then fabricated the devices together with fab process engineer. After that the author performed the electrical characterization testing. A summary paper has been published with the findings by the author and the co-authors. All the team member were involved in the data analysis and discussion. Except the metal electrodes screening, the author was the core team member and performed majority of the electrical characterization and reliability study for other materials (oxide, interface layer, etc.) screening and studies.

3. A huge improvement in the field of memristor modeling using two-state-variable approach has been made. This model accurately captures the effects of internal Joule heating on both the electronic transport and the drift velocity of vacancies in the switching material with great performance. For Integrated Circuit (IC) design in production environment, compact device models with accurate and fast simulation speed are essential for circuit simulation to predict the circuit and product behaviors based on manufacturing process parameters. The model developed will provide the Technology & Design Kit (TDK) support for the Electronic Design Automation (EDA) tools for the circuit simulation of memristor production. The author’s main contribution for this modeling work includes providing initial concept, device fabrication and electrical testing, part of physical equation derivation, and all technical discussions. The main co-author wrote the MATLAB code with fitting parameter fine tuning and drafted the initial publication manuscript. Dr. Stanley Williams provided the vital dynamical equation for the conducting channel area approximation with respect to critical power density. The whole team involved with the data analysis and discussion.

4. Pioneering research for HP’s next generation selector devices has been conducted and demonstrated with promising preliminary results. The selectors are essential devices for the operation of memristors in the high density crossbar memory architecture and are crucial for the 3D stack application. Although the niobium oxide selectors are candidates for first generation products with moderate performance, they are not likely to allow scaling of the crossbars to the significantly larger array sizes desired for future higher density products. A new type of selector technology was discovered and HP holds the foundational IPs. This technology will enable arrays that are orders of magnitude larger than those possible with the present niobium oxide selectors. This provides a path for several generations of higher density memory products. In this research work, the author worked as leading researcher for project management, experiments planning with new materials, electrical testing for screening and characterization, and data analysis. More than 10 patent applications in this area have been filed by the author and the team. The selector study leads to the refined neuromorphic computing device work as well.

5. The author worked as a leading inventor and main contributor on various memristor applications. For instance, a novel, economic, and high efficiency code comparator is introduced through a unipolar switching device, which can increase the code comparing times by thousand times faster and can be used for security purpose. Another example includes a weavable memristor fabrication method that has been introduced for the wearable devices and electronic skin. Critical contribution has been made to the Dot Product Engine (DPE) project as a core team member, which is analog memristor based hybrid computation engine. This is a project sponsored by USA government agency IARPA (Reference No.: IARPA-BAA-12-03). The contributions made by the author for this high profile project include initial DPE concept and brainstorming, initial characterization of the TaO_x analog memristor, CMOS design, memristor process integration, and the DPE applications. The 64 level Multi-Level Programming (MLP) capability was first demonstrated by the author, which demonstrated the feasibility of full capability of the memristor analog properties and DPE promising performance. More than 8 patents applications have been filed by the author and peers. Several publications have been published and a few are pending by the author and the co-authors.

1.4 Organization of the thesis

The thesis is organized by the topics and divided into 5 chapters. Chapter 1 gives a background and introduction of the memristor concept and development, followed by motivation, major contributions of the thesis, and organization of the chapters. Chapter 2 presents the memristor device engineering tuning with characterization. A state of the art two-state-variable compact model for the TaO_x memristor is subsequently discussed in Chapter 3. Chapter 4 gives an introduction to another critical circuit component work done for selector for the high performance crossbar memory application. Chapter 5 provides selected application examples and final conclusion with insight for future work. Finally, Chapter 6 is the conclusion and recommendation for future works.

Chapter 2: Memristor Device Engineering

2.1 Memristor architecture and device fabrication

As discussed in Chapter 1, the memristive behavior arises in a special category of solid-state device in which electronic transport and the charged vacancy/ionic motion are coupled in this electro-ionic system in the presence of an applied electric field. This memristive property has been observed in a variety of material systems arranged in nanometer scale films. Different memristive devices could be classified into two categories based on the nature of the mobile species from the switching material: anion and cation devices. Anion based devices mainly include oxide insulators, for example, various metal oxides, certain complex oxides and large band gap dielectrics, as well as some other non-oxide materials. Cation based devices include the cation ion metals like Cu, Ag etc. No matter which device type, an MIM sandwich structure is generally used to produce this kind of devices using thin-film semiconductors technologies. From the device fabrication perspective, one unique advantage of memristors is that the performance of a memristor largely relies on one critical fabrication parameter, the film thickness from the thin-film deposition process instead of device geometry from the lithography process. The thin-film thickness can be relatively easily controlled at angstroms level without the use of expensive lithography fabrication techniques. On top of that, fabrication of memristor devices does not demand high temperatures. This will enable back-end of line integration of multiple thin-film layers of memristors with a CMOS substrate. This backend of line compatibility also prompts the three dimensional stack for high memory density. A titanium oxide memristor MIM structure on a CMOS wafer is illustrated below:

Figure 6 A titanium oxide memristor MIM structure on a CMOS wafer. The FEOL process will form the substrate and active devices including transistors. Memristors are integrated at backend of process.

Since memristor devices are not active components, the coupled transistors integrated with memristors will provides signal computation and gain, which can achieve all kinds of complex functions including memory applications. However, the

drawback for this memristor-transistor architecture is that it is much less dense than standard architecture. The solution to the density problem is to use a complement crossbar arrays of memristor devices with a conventional CMOS substrate. A crossbar device consists of two electrode wires that physically cross each other. The two wires form a cross-point junction that is composed of a switching material with tailored transport properties. In this architecture, a large array (e.g., 1024 x 1024) consisted only crossbar devices that is located at the backend of line layers of the silicon substrate. The transistors are used for peripheral circuits only located at the front of line of the silicon substrate. In their simplest form, crossbar architecture will provide the highest memory density since the size of memristive devices can be very compact on the order of $4F^2$ where F is a minimum technology feature size. The footprint is essentially determined by the overlap area, where the two perpendicular wires contact and interact at the device region. Comparing to the conventional CMOS circuit and hybrid memristor-CMOS logic, crossbar architectures has great promise in terms of many aspects including good scalability, compact size and lower power consumption. For example, crossbar logic based elements can enable massively parallel computations through the reduction in power consumption and size by roughly up to 2-3 orders of magnitude [13]. We are going to cover certain aspects of application studies as well in Chapter 5. Fig. 7 shows a presentation of a crossbar structure.

Figure 7 A simplified crossbar architecture: top electrode array, bottom electrode array and switching material at the inter-section area between top electrode and bottom electrode

As we can see from Fig. 7, a crossbar array will have multiple parallel input and output lines, which will form a crossed pattern of interconnecting lines. Between them a connection may be built by closing a switch located at each intersection. To address the desired memristor device element, an applied voltage and a sense circuit will be applied to respective TE and BE of the device as shown in Fig. 8 below.

Figure 8 Crossbar device addressing: Row 2 (R_2) and Column 3 (C_3) element is selected for the illustration purpose

Using memristors in crossbar arrays may lead to read and/or write failure due to an inherent sneak current passing through the cells that are not selected. For example, cells on the same row or column as a targeted cell. Failure may arise when the total sneak current through untargeted neighboring cells from an applied voltage is higher than the current through the targeted memristor. Using a transistor or selector with each memristor has been proposed to isolate each cell and overcome the sneak current. We will discuss it in more details in Chapter 4.

All the samples shown in this research, except those cited ones, are fabricated in HP Labs, which are obtained through a series of thin-film deposition and different mask fabrication process for the characterization study. There are mainly two types of memristor devices we used: micro-device and nano-device. Figs. 9 and 10 show an example of the two most common types of devices we fabricated and used to characterize the memristors in HP Labs:

Figure 9 Micro- & nano sized memristor test structure. : a) the micro-device, for example, the stack is Pt/TaSiO_x oxide (8 nm)/Ta with a device size defined by a top electrode pad size (disc device) or inter-section area between bottom electrode and top electrode (crossbar device); b) nano-scale devices, for example, the stack is TiN/ (TaO_{2.5})_{0.7}(SiO₂)_{0.3} (1 nm) /(TaO₂)_{0.7}(SiO₂)_{0.3} (7 nm) /Ta, where a (TaO₂)_{0.7}(SiO₂)_{0.3} sputter target was used to deposit the full oxide in Ar and oxygen gas mixture and the sub-oxide in pure Ar gas. The devices studied had a 30-100 nm diameter for the nano-devices, defined by a TiN bottom electrode via in a device array.

Figure 10 Top view of various test structures used for memristor characterization using Scanning Electron Microscope (SEM). a) a micro-sized fan-out crossbar structure; b) nano-sized nano-wires crossbar structure; c) nano-sized via structure- the via size varies from 30 to 100 nm, the top electrode is not shown here.

We have developed many different process flows for various characterization purposes. For the purpose of the introduction, a crossbar array made through standard process is used here to illustrate the standard process flow. Fig. 11 shows the simplified process flow to fabricate a typical Pt/TaO_x/Ta device that is often used.

Figure 11 Standard process flow to fabricate a crossbar device. The critical step of switching oxide formation and switching area definition are shown in the step 4.1-4.4 in details

The process started with a silicon wafer with pre-deposited SiO₂ thin-film as substrate (e.g., a 4 inches Si wafer with 200 nm SiO₂) as indicated in step 1. In the next step (step 2), the SiO₂ thin-film was gone through lithography process and etched by 20-30nm through Reactive Ion Etching (RIE) process to form a trench. The purpose of this step is to have a more planarized surface for the subsequent process with elimination of expensive Chemical Mechanical Polishing (CMP) process. Subsequently the bottom electrode conductor (e.g., a 5nm Ta with 20nm Pt bi-layers: Ta was used as an adhesion layer and Pt was the bottom electrode layer) was deposited using a lift-off photolithography process, Physical Vapor Deposition (PVD) process designated in step 3. Lift-off process is a method of quick patterning of a target material deposition on the surface of a thin-film with assist of sacrificial material (e.g., photoresist or some polymer material). It is an additive process for the semiconductor manufacturing comparing to more traditional subtracting techniques like etching in micro-structuring technology. For thin-film deposition, another more advanced process technique named Atomic Layer Deposition (ALD) was often used for better process control. Very thin

and conformal metal layer can be deposited through ALD process since the thin-film is deposited layer by layer at atomic scales by exposing the precursors to the growth surface repeatedly. Step 4, switching oxide formation, is the most critical step. It began with a blanket 6 nm TaO_x switching oxide deposition, normally through sputtering. The sputter target was pre-chosen with desired stoichiometry composition. In some rare cases, co-sputtering or reactive sputtering was used also. When the switching oxide is extremely thin (for example, 2 to 3 nm), ALD method was preferred to be adapted. The blanket switching was subsequently lithographed and dry etched. This is to make sure only the cross-point area will have the oxide while the rest of area will have no oxide for the connectivity. The final switching oxide formation area is shown in step 4.1. In the next step (step 4.2), a photo resist was coated through spinning, then lithographed to remain in the bit area and bond-pad area, which will be used for the subsequent lift-off process. The bit area will define the final actual switching area size. A 60 nm SiO₂ or Al₂O₃ Inter-Layer Dielectrics (ILD) was deposited through either normal Chemical Vapor Deposition (CVD) or sometimes using another variation of CVD method with high throughput and lower temperature named Plasma-Enhanced Chemical Vapor Deposition (PECVD). After the lift-off process, the ILD formed the electrical isolation layer except the bit area and bond-pad area as shown in Step 4.4. After cleaning, the top electrode metallization (e.g., a 10 nm Ta with 10 nm Pt bi-layers: Ta will be the top electrode and Pt is the protection layer) was formed similar to Step 2 BE formation, which completed the device fabrication.

For the quick material screening or evaluation, a disc device was often used. For example, for the single oxide layer disc memristor sample preparation, a bottom electrode metal was deposited using a PVD process, then the metal oxide was deposited using PVD or ALD. Subsequently, the top electrode metal was deposited and patterned through the shadow mask lithography process (also known as stencil lithography) in the PVD machine. Shadow mask evaporation is a resist-free method of fabricating desired thin-film patterns without going through conventional thin-film deposition, lithography and etching process flow. It will take place in-situ during thin-film deposition though the hard mask with advantages of avoiding chemical contamination. It is a quick process normally adapted in the lab environment. Due to its intrinsic limitation, the resolution of a shadow mask device is usually very limited, usually at large size of micro-meter level.

With understanding of the device architecture and process integration, now we turn to the material side. As mentioned earlier, memristor can be used by various applications including nonvolatile memory [6] [7], logic circuits [8] [9], and neuromorphic computing [10]. Reversible resistive switching study of memristor is largely driven by the application requirement and each application may need a more finely tuned device properties emphasizing on different aspects. As we know materials play a critical role in memristive devices [14]. The material choice of the electrodes, switching oxide, interface layer, and isolation layer will have direct impact on the memristor switching behavior. Therefore, proper material selection, development, and

characterization are critical prerequisites for memristor device performance and applications. In order to meet all different requirements, we need to understand and characterize the material dependence on memristor. In the subsequent of this chapter, we will characterize and optimize memristor material impact from three perspectives: 1) Firstly, we report a systemic study on the influence of the electrode on the resistive switching properties of tantalum oxide based memristors. 2) Memristor switching oxide tuning is done for performance and high nonlinearity. 3) Finally, a non-oxide material switching material is surveyed.

2.2 Electrode material dependence

As mentioned earlier, the material selection of the electrodes will have direct impact on the memristor switching behavior because the electrodes are responsible for the oxygen ion reserving or releasing as well as electrode-oxide interface interaction. Here we start with a systematic study for the electrode material to understand and characterize the material dependence of electrodes on memristor [15]. Tantalum oxide (TaO_x) is one of the leading materials being considered as the active nonvolatile switching layer for memristors because of its demonstrated high switching speed and endurance. In the electrode material Design Of Experiments (DOE), we carefully prepared a set of disc devices with fourteen different top electrode materials (Ti, Zr, V, Nb, Ta, Cr, Mo, W, Ni, Pd, Pt, Ag, Au and Al) to examine the effect of these metals when used as top electrode contacts on the TaO_x devices. Except for the top electrode materials, all the samples had identical thin-film stacks obtained from the same experimental run.

For the process setup, the bottom electrodes were 100nm Pt films with a 1nm Ta layer sputter-deposited on a thick SiO_2 substrate, and served as a common ground for all the disc devices. Subsequently, a blanket 11nm Ta_2O_5 layer was sputter-deposited on the bottom electrode at ambient temperature. Fourteen different top electrodes were deposited on top of the Ta_2O_5 layer through a shadow mask at ambient temperature. The top electrode shadow mask has various bondpad sizes for the disc devices. For this particular experiments, we choose devices with 100 μm in diameter for the electrical measurement. A 10nm Pt protection layer was added (also through the shadow mask) on the top of different electrodes to prevent oxidation in air and obtain a better electrical contact. All the fabricated devices were highly resistive in the as-prepared state. The devices were tested using two-terminal quasi-DC sweeps for the static IV characterization.

The testing system consisted of a Cascade bench probe station and Agilent 4156 Semiconductor Parameter Analyzer, controlled by custom-built software written in LabVIEW. The simplified device stack and test setup are shown in Fig. 12. The bottom electrodes were grounded during the testing, while quasi-DC voltage sweeps were applied on the top electrodes to operate the devices.

Figure 12 Schematic of the device stack of as-prepared samples and test setup using Semiconductor Parameter Analyzer. The stack is Metal to be tested (30 nm)/TaOx oxide (11 nm)/Pt (100 nm)/Ta (1 nm) with a device size defined by a top electrode pad size (disc device)

After device fabrication, all samples were tested using the test setup mentioned earlier. From the test measurements, all the devices except the one with the Au top electrode were able to switch from an initial virgin High Resistance State (HRS) to a Low Resistance State (LRS) by a so-called “Electroforming” process. Based on the forming and subsequent switching behavior, we categorized the fourteen metals into five subgroups:

- 1) No-switching group of Ti and Zr, where the yield of successful switching was very low; we characterize it as almost no-switching group;
- 2) Nonlinear switching group of Nb, V and Cr, where Negative Differential Resistance (NDR) behavior was observed;
- 3) Linear switching group of Ta, Mo, W and Al, where a linear IV relation in the LRS was observed;
- 4) Non-polar switching group of Ni, Pd, Pt and Au, where the switching is non-polar or unipolar and dominated by thermal effects;
- 5) Cation switching group of Ag, where the switching is more like volatile switching.

Devices with an electrochemically active electrode like Ag usually form a metal conductive bridge responsible for the electrical switching. The switching is caused by the motion of cations instead of oxygen vacancies. Most of the elements within each group are chemically related, as shown by their positions in the periodic table in Fig. 13.

Highlight Legend for Switching Groups

■ "No" switching	■ Nonlinear switching	■ Linear switching	■ Non-polar switching	■ Cation switching
--	---	---	--	---

										IIIA
IVB	VB	VIB	VIIB	VIII B			IB	IIB		
22 Ti Titanium	23 V Vanadium	24 Cr Chromium	25 Mn Manganese	26 Fe Iron	27 Co Cobalt	28 Ni Nickel	29 Cu Copper	30 Zn Zinc	31 Ga Gallium	13 Al Aluminum
40 Zr Zirconium	41 Nb Niobium	42 Mo Molybdenum	43 Tc Technetium	44 Ru Ruthenium	45 Rh Rhodium	46 Pd Palladium	47 Ag Silver	48 Cd Cadmium	49 In Indium	
72 Hf Hafnium	73 Ta Tantalum	74 W Tungsten	75 Re Rhenium	76 Os Osmium	77 Ir Iridium	78 Pt Platinum	79 Au Gold	80 Hg Mercury	81 Tl Thallium	

Figure 13 Five subgroups of the top electrode materials tested: 1) "no" switching; 2) nonlinear switching; 3) linear switching; 4) non-polar switching; 5) cation switching

For the device characterization, the virgin state is first measured, which is an important parameter and indicator to understand the oxide and interface condition before switching. IV relations in the virgin states were measured by sweeping from a small positive voltage to a negative voltage, which were both below the forming voltage. Figs. 14a-d show the IV results when the device was swept between +1 V and -1 V. For the case of Ag top electrode, a smaller voltage (0.2 V) sweeping was used to avoid any switching events, as shown in Fig. 14e. The insets to Fig. 14a-e are the semi-log plots based on the same data as those in the linear-linear plots. The virgin resistance IV curves are arranged into the five groups described above.

Figure 14 Virgin IV curves for the groups of top contact metals: **a**: Group 1 - no-switching, **b**: Group 2 - nonlinear-switching, **c**: Group 3 - linear-switching, **d**: Group 4 - non-polar-switching, and **e**: Group 5 - cation-switching.

From the IV measurements in the virgin states, all devices including Ag top electrode devices except for the Pt top electrode exhibited more or less an asymmetric diode-like behavior. The asymmetry of the IV curve is due to different electrode/oxide interfaces at the top and bottom electrodes. For the Pt/TaO_x/Pt device, the IV curve is symmetric because of the device stack is chemically symmetric. The oxygen affinity of the metal electrode correlates strongly with the device resistance, which has also been observed for TiO₂ based memristors [16]. The electronic properties of the metal-oxide interface are sensitive to oxygen vacancies, and a higher vacancy concentration leads to a lower interface resistance. Consequently, the more reactive metal (with a more negative Gibbs free energy of formation of oxide) corresponds to a lower device

resistance, as can be seen in Figs. 14 b and c. No clear trend is observed between the virgin resistance and the work function of the top electrode, as shown in Fig. 15.

Figure 15 The work function of the top electrodes and the device resistances

After the virgin state comparison, next, the most important switching behavior is studied. The as-prepared devices in this study required an electroforming process to precondition them into a switchable state. Electroforming is essentially a ‘soft’ breakdown process and usually requires a higher voltage than that of the normal subsequent switching [17]. The breakdown process forms conducting channel(s) in the oxide by creating oxygen vacancies in the initially stoichiometric film. Because the as-prepared sample has a limited numbers of defects, a relatively high forming voltage is often needed to create oxygen vacancy defects. This process normally results in a high device variance and failure rate. Utilizing reactive metals on the anode during electroforming to accommodate the oxygen expelled from the switching oxide during forming can significantly improve the device yield and performance. That is a major role played by the top electrode metals. The IV plots of electroforming for devices with different top electrodes are given in Fig. 16 except Group Five, since electroforming is not needed for cation-switching devices.

Figure 16 IV plots of electroforming devices with different top electrode materials: Group 1 - no-switching, Group 2 – nonlinear-switching, Group 3 – linear-switching and Group 4 - non-polar-switching

The electroforming was done by using a quasi-DC voltage sweep with a current compliance. Because of the different chemical properties of the top electrodes, the electroforming of each of the five device groups is different in terms of voltage, current and post-forming resistance, leading to different switching behaviors. It suggests that the subsequent switching behavior depends on the top electrode materials rather than

the specific electroforming process, such as the compliance current. Figs. 17 a-o below show the typical switching behavior of each device group after electroforming.

Figure 17 **a-o** Switching behavior of the TaO_x memristor with different top electrodes: Group 4 - non-polar-switching and Group 5 – cation-switching

As we can see from Figs. 16a-b, , Group One, the metals Ti and Zr react strongly with the tantalum oxide due to their much stronger oxygen affinity than that of Ta [18], which likely results in an overly large amount of oxygen vacancies. After electroforming, the Ti/TaO_x/Pt and Zr/TaO_x/Pt devices are very conductive, which makes OFF switching almost impossible, even at the 0.1 A current level, as shown in Figs. 17a-b. This leads to a very low device yield. It is worth noting here that even though we categorize these two devices in the “no switching” group based on the very low yield obtained with the device stack structures studied here, it does not necessarily mean that these devices do not switch even with a stack specially optimized for these two materials. Figs. 17c-e show the switching loops of Group Two materials, which have nonlinear IV curves in the LRS states. A quantitative measure of the nonlinearity can be defined as the ratio of the current measured at an operation voltage V to the current observed at $V/2$. A linear device has a nonlinearity of 2 because the current will linearly increase two times when the voltage doubles, while that of a nonlinear device is greater than 2. A large nonlinearity is desired for large crossbar memory arrays, because a nonlinear response lowers the sneak path currents and enables the utilization of the array [19]. The Nb/TaO_x/Pt, V/TaO_x/Pt and Cr/TaO_x/Pt devices exhibit a nonlinearity in different degree in the IV curves (indicated by yellow arrows in Figs. 17c-e) that can be attributed to NDR characteristics as the current keeps increasing

while voltages drop down during the double switching [19] [20] [22] [21]. These three metals share a common feature – there is at least one material that displays an Insulator Metal Transition (IMT) among the oxides of each of the three metals. Nb can be oxidized to form NbO_2 , which has an extensively reported NDR behavior induced by Joule self-heating that triggers an IMT around 1000 K when the device is locally heated over that critical transition temperature. VO_2 is also known for NDR, and its resistivity decreases by several orders of magnitude when heated above 340 K [19] [21]. It is surprising to observe NDR in the memristors with Cr top electrode, although some literature reports a possible IMT phenomenon in Cr_2O_3 around 1000 K. Figures 17h-i show the linear switching behaviors from devices with Group Three top electrodes. Ta is the most commonly used top electrode metal for TaO_x memristors [23] [24], and the typical switching curve is shown in Fig. 17g. Mo/ TaO_x /Pt, W/ TaO_x /Pt and Al/ TaO_x /Pt devices exhibit similar linear switching behavior, as shown in Fig. 17f, Fig. 17h and Fig. 17i, respectively. The IV curves of Group Four materials (Figs. 17j-l) show very strong thermal effects, revealed by the downward bending of the IV curves. These IV shapes suggest that metallic channels are formed in the devices and the channel resistance increases significantly by Joule heating rather than electrical field driven during the switching [25]. Typically, no bi-polar but only non-polar switching is observed with these devices. As we know that Ni, Pd and Pt are noble metals, which do not react with Ta_2O_5 to generate a sufficient oxygen vacancy reservoir [14] under the top electrode to initiate bipolar switching. Bipolar switching usually requires an asymmetric device stack where two electrodes have significantly different oxygen affinity, which is lacking in the devices with Ni, Pd or Pt top electrodes. Therefore, in those devices a dielectric breakdown induces a Ta sub-oxide conduction channel(s) [26], resulting in the ON state. The OFF state is caused by thermal rupture of the metallic channel(s), mainly via radial diffusion of vacancies. The device with an Au top electrode behaved differently from the other noble metals. Au has no stable oxide nor is it likely to be ionized by oxidation in the device [27]. Therefore, diffusion rather than drift is the main transport mechanism for Au atoms in these devices, given that Au usually has a high diffusion coefficient. Accordingly, the devices with Au top electrodes cannot be electrically formed or switched, as shown in Fig. 17m. Fig. 17o shows the unique switching characteristics of memristors with an Ag top electrode. This switching behavior can be understood by the formation of an Ag atomic bridge between the Ag top electrode and the Pt bottom electrode, which is a typical switching mechanism for the so-call Conductive Bridge Random Access Memory (CBRAM) [28] [29] [30] [31]. The operation of the device is through Ag and Ag^+ conductive states [32], which we will discuss in more details in the later section. However, Ag is a quick diffuser even at room temperature. If the size of the conductive bridge is not sufficiently thick, the diffusion of the Ag atoms breaks the conductive bridge, leading to a volatile behavior that has been observed in these devices, such as those shown in Fig. 17o.

In this electrode impact study, we have demonstrated the crucial role of the top electrode metals on the device behavior of TaO_x based memristors. The resistance of the as-prepared devices exhibits a certain dependence on the oxygen affinity of the top

electrode metals, and more reactive metals generally result in a more conductive device in the virgin state. Highly reactive metals, such as Ti and Zr, produce a very low switchable device yield. Noble metals, including Ni, Pd, Pt, and Au, do not create sufficient oxygen vacancy reservoirs at the top metal-oxide interface via chemical reactions; therefore, the switching is non-polar and dominated mainly by thermal effects. Devices with electrochemically reactive metals, such as Ag or Cu, are typical conductive-bridge type switches, where the drift of cations is responsible for the switching. Volatile behavior was observed in this case. The rest of the materials, including V, Cr, Nb, Ta, Mo, W, and Al, can induce bi-polar switching behavior when utilized as the top electrode. Both V and Nb top electrodes result in highly desirable NDR characteristics in the LRS state. NDR behavior was observed in the HRS state of the memristors with Cr top electrodes, but the reason is not clear at the moment.

In order to verify the quality of the TaO_x for this study, an endurance testing was done firstly on the Pt/TaO_x/Ta device. The endurance readily passes 100 million of switching cycles, as shown in Fig. 18.

Figure 18 Endurance of Pt/TaO_x/Ta stack to verify the quality of Pt/TaO_x layers shared by all the devices.

Since the device size was relatively large, compared with the memristor resistance, the contact and wire resistance was not negligible, leading to a relatively smaller memory window under two-terminal testing scheme. Nevertheless, the

endurance test indicates the common bottom electrode and oxide quality of the batch devices.

2.4 Switching oxide device engineering

Based on the mobile species adapted in the devices as switching carrier, memristor can be broadly divided into two types: cation based ionic switching devices and anion based ionic switching devices. Cation based devices are sometimes referred as CBRAM and Electrochemical Metallization Memory (ECM). The cation metals like Cu [33] [34], Ag [35] as we discussed earlier, or an alloy of those metals, such as CuTe [36] are often used for the device construction. The switching mechanism for the cation based devices with traditional electrolytes is relatively well understood. Take Ag/ α -Si/Pt device as an example, the switch process is as followings: during the initial electroforming or during the set switching, a positive voltage potential will be applied on the Ag electrode, which oxidizes the electrode Ag atoms into Ag^+ cations. Those cation will be dissolved into the electrolytes (α -Si here) and drift quickly across the solid electrolyte to the inert counter electrode, which is Pt as cathode, under high electric field; once it reaches the insert Pt cathode, the Ag^+ ions are quickly electrochemically reduced to Ag atoms at the cathode and deposited on the surface of the Pt cathode electrode. This process allows the Ag atoms to grow towards the Ag anode electrode as a conducting metal filament, which will turn the switching the device ON. For the switch OFF operation, an opposite electric field is applied. When the positive voltage is applied to Pt electrode, an electrochemically inert material hardly has chemical reaction with other element. For Reset switching, it dissolves the Ag filament anodically starting from the interface of the Ag electrode and Ag filament. The broken of the metallic filament will switch the device OFF. The cation based ionic switching devices are relatively straightforward for the operation mechanism and simple for the structure. However the material used are usually not CMOS compatible like free form Cu or Ag thinfilm. Hence, here we will focus on another type of switching devices for the switch material tuning: anion based ionic switching devices.

As the name suggested, anion based ionic switching device is working on the movement of anions, for example, oxygen ions. Anion based devices was demonstrated using many different insulator materials and systems, such as Transition Metal Oxides (TMO) (oxide compounds composed of oxygen atoms bound to transition metals) [37] [38] [39], complex oxides (a chemical oxide compound that contains oxygen and at least two other elements (or oxygen and just one other element that is in at least two oxidation states)) [40] [19], perovskite oxides (a class of oxide compounds with general perovskite formula ABO_3 or A_2BO_4) [41], and some non-oxide insulators, such as chalcogenides [42] (a chemical compound consisting of at least one chalcogen anion and at least one more electropositive element) including Transition Metal Dichalcogenide (TMD), flexible and organic materials [43] [44], and even carbon nano tube and graphene-based structures [45] [46].

Compared with other switching materials, the binary metal oxides have excellent characteristics including simple manufacturing process, good compatibility with CMOS process, and simple composition with good performance. TiO_x is one of the most extensively studied materials in the earlier days and it is the oxide material used in HP Lab's first memristor device [3]. Since the first demonstration of resistance switching phenomenon based on TiO_x , many binary oxides have been studied as anion based switching materials, such as MgO_x , ZrO_x , HfO_x , TaO_x , CrO_x , MoO_x , WO_x , CoO_x , AlO_x (where x denotes a non-stoichiometric compound) etc. [13]. The worldwide effort has been put in memory development focusing on various aspects of the performance like endurance, forming condition, operation voltage and current, and so on using memristors by evaluating different materials mainly according to the following priority and sequences as shown in Fig. 19:

Figure 19 Engineering effort to improve memristor memory application performance

TaO_x based device has demonstrated high endurance with non-volatility, fast switching, low-energy operation, multiple-state operation, scalability, and stackability characters, which can replace CMOS for reversible and reliable memory applications [23]. The critical drivers behind the mainstream shifting from TiO_x to TaO_x based device is mainly due to the endurance with well mechanism understanding by Yang et al. [23].

Figure 20 TiO_x based memristor system and TaO_x based memristor system comparison: a. TiO_x conducting mechanism is based on gap modulation; b. TaO_x conducting mechanism is based on composition modulation; c and e. highly nonlinear DC sweep and low endurance test results of TiO_x based memristor system; d & f (adapted from [23]). linear DC sweep and high endurance test results of TaO_x based memristor system

The device difference between the TiO_x based memristor system and TaO_x based memristor system is most likely related to the thermodynamic differences in these two oxide systems. The equilibrium solid-phase diagram for the Ta–O system has simple two stable phases under temperature of 1000 K: the single-metal-valence

compound Ta_2O_5 and Ta metal, which can have a few percent of dissolved O (denoted by $\text{Ta}(\text{O})$) (note there are a number of metastable phases like the non-stoichiometry TaO_2 that has the rutile structure between the two phases) [18]. On the other side, TiO_x based memristor system has a large number, especially an entire series of Magnéli phases (the phases with the general formula $\text{M}_n\text{O}_{2n-1}$ named after Arne Magnéli. They are examples of crystallographic shear compounds with the rutile structure) between the Ti metal and full oxide [18]. Due to the material composition and thermodynamic differences, the two systems have fundamental differences in switching mechanisms. TiO_x based memristor device relies on the gap modulation (Fig. 20 a). The conduction channel is crystalline while the oxygen vacancy reservoir (O vacancies) is in series with the channel [37] [14]. While for TaO_x based memristor devices, the switching mechanism is based on composition modulation. The conduction channel is still amorphous and oxygen reservoir (Oxygen anions) is parallel to the channel (Fig. 20 b) [26] [47]. As a result, the DC sweep and endurance test characterization results are very different between TiO_x based memristor system and TaO_x based memristor system, as shown in Figs. 20 c-f.

As we can see from the previous discussion, TaO_x based memristor has the desired endurance while TiO_x based memristor has the nonlinearity, which is important for the large crossbar applications. To achieve the benefits from both systems, a hetero-structure (also known as bi-layer structure) of $\text{TaO}_x/\text{TiO}_x$ oxide device system was proposed and studied in detail. The structure has shown promising results for both endurance and nonlinearity. To understand the hetero-structure better, we need go back to the switching fundamentals. It is possible that several different mechanisms may co-exist, responsible for a switching mechanism, and different mechanisms could be a dominant factor in different operating conditions and materials systems. As we know that metal/semiconductor contacts are typically ohmic contacts when the semiconductor has very heavy doping, and behaving like a rectifier (Schottky-diode like) when the semiconductor has low doping. Single-crystalline TiO_2 was used to elucidate how the metal/oxide interfaces control the device resistance. A single crystal of rutile TiO_2 is wide-bandgap material (bandgap e.g., ~ 3.0 eV). Oxygen vacancies in TiO_2 are known to act as n-type dopants. For the TiO_x oxide device memristor system, the mechanism is to be found dominated by TiO_2 switching, which is in the change of shunting and recovery of the metal/insulator interfacial barrier caused by the localized drift of oxygen vacancies [14] as shown below:

Figure 21 Junctions on Pt/TiO_2 and ohmic interface of Pt/TiO_x show the role of the interfaces in determining the electrical switching behavior, modified from [14]

The experimental results show that electrical conduction in metal/oxide/metal thin-film devices is controlled by a spatially heterogeneous metal/oxide electronic barrier. From Fig. 21 we can see that for TiO_x system, the switching involves changes to the electronic barrier at the Pt/TiO_2 interface due to the drift of positively charged oxygen vacancies under an external applied electric field. During the switch ON process, vacancies drifting towards the interface create conducting channels that shunt the electronic barrier to have high conductance state. The drift of vacancies away from the interface under an opposite voltage annihilates such formed channels, recovering the electronic barrier to switch OFF. Since the Magnéli phase oxide is highly conductive (modeled as a resistor), the location of the device, concentration level and distribution of oxygen vacancies in the as-fabricated TiO_2 film control the device performance including conductance, rectification and switching polarity of the device. To have the desired performance and device characterization of bi-layer $\text{TaO}_x/\text{TiO}_x$ oxide device, we built different devices with engineered oxygen vacancy profiles that predictively and precisely control the memristor switching properties for polarity and conductance as below:

Figure 22 Switching side and non-linearity interface of TaO_x - TiO_{2-x} system study show the role of the switching and interfaces in determining the electrical switching behavior. a) ohmic interface from $\text{Pt}/\text{TiO}_{2-x}$; b) reference memristor device of TaO_x showing very typical switching curve with Pt/TaO_x switching barrier; c) highly nonlinear device of $\text{Pt}/\text{TiO}_{2-x}/\text{TaO}_x/\text{TiO}_{2-x}/\text{Pt}$ with nonlinearity from $\text{TaO}_x/\text{TiO}_{2-x}$ however there is no switching barrier; d) final working TaO_x - TiO_{2-x} bi-layer system with switching and desired non-linearity

As we can see from Fig. 22, by engineering the material choice and stack with deep understanding, we successfully tuned the device according to the desired performance with desired nonlinearity. From the previous discussion, we have demonstrated memristor device performance improvement for endurance and non-linearity. The next targets are switching voltage and current (hence the power). The voltage can be relatively easily tuned through the oxide thickness change. In order to have smaller current, many experiments have been carried out with the theory support behind. For instance, we can have the oxide tuning by introducing a more resistive material (e.g., Al_2O_3 or SiO_2) into the main switching oxide during the sputtering process. A special technique called co-sputtering was often used as shown below:

Figure 23 A mixed oxide memristor introduction through Co-sputtering with 2 sputtering targets

Through the co-sputtering process, we are able to tune the different oxide composition by changing the sputtering target, power distribution, gas flow, and other parameters. Fig. 23 shows an example of 70% of TaO_x mixed with 30% of SiO_2 , which greatly reduces the current by ~ 20 times with the same device and testing condition.

Figure 24 Current reduction study using the oxide engineering. a) & b) Device information of Ta (30nm)/ TiO_{2-x} (10nm)/Pt (100nm) sample and Ta (30 nm)/((TaO₂)_{0.7}(SiO₂)_{0.3})(10nm)/Pt (100nm) sample respectively; c) & d) The DC switching behavior of the two devices. From the IV plot, we can see with small amount

of SiO₂ mixed into TaO_x during the sputtering process, the switching current level has been reduced.

As we can see from the previous various results, engineering switching materials is the most effective approach for the device performance tuning. Many other oxide engineering efforts have been done as well to improve the device performance, for example, the oxide deposition method including sputtering vs ALD, in-situ reactive sputtering etc.

2.5 Interface material engineering and non-oxide switching material

In the previous sections, we have discussed the two most important components of the memristor MIM device: the electrodes and the oxide. In this subsection we introduce another two category works we have done for the memristor engineering: Interface material engineering and non-oxide switching materials, mainly for the fab compatibility and production consideration.

Due to its low resistivity, good adhesion and resilient to electromigration and stress voiding, refractory metal compounds like TiN, TaN, etc. are used widely in the wafer processing as barrier layer or cap layer to the Al, Cu or W plug metallization. Those interfacial layer will act as a clean, uniform nucleating barrier layer and prevent the interaction between Al or Cu and Si. Therefore there will be no junction spiking or Si precipitation. Due to the low reflectivity, it will be served as an anti-reflection coating (ARC) for the subsequent lithography process. Stoichiometric TiN or TaN has atomic 50% each of N and Ti or Ta. For the N concentration more than 50%, the excess N will exist in solid solution in the stoichiometric TiN or TaN. Both films have columnar grains with resistivity in the range of 50-100 $\mu\Omega\text{-cm}$ [48]. In this case, TiN and TaN are explored to be used as interfacial layers to reduce or eliminate the usage of Pt (Pt is expensive precious noble metal and difficult to etch). Fig. 25 shows the initial effort using TiN, which is tried in our reliable TaO_x device system.

Figure 25 TaO_x memristor device with TiN interfacial layer. a) Device structure. The stack is Ta (30 nm)/TaO_x oxide (10 nm)/TiN (30 nm)/Pt (10 nm) with a device size defined by a top electrode pad size (disc device); b) The endurance data on order of 10⁴.

As we can see from the above results, due to the incompatibility of the thermal dynamics, TiN does not work well in the TaO_x system. The switching mechanism becomes much more complicated also with the diffusion of Ti element with the possibility of formation of TiN_xO_y. With the understanding of material implications, TaN has been tried next using the same device structure and size. The results are shown in Fig. 26.

Figure 26 TaO_x memristor device with TaN interfacial layer. a) Device structure. The stack is Ta (30 nm)/TaO_x oxide (10 nm)/TaN (20 nm)/Pt (10 nm) with a device size defined by a top electrode pad size (disc device); b) IV switching data with the inset figure shows the log scale plot; c) The endurance data on order of 10⁶.

Switching TiN to TaN as an interfacial layer, the endurance has improved significantly from 10⁴ to 10⁷ due to the better material compatibility. Fig. 27 shows the TEM picture of the interface.

Figure 27 TEM picture of Ta (30 nm)/TaO_x oxide (10 nm)/Ta₂N₅ (20 nm)/Pt (10 nm) (HV=300 kv, Direct Mag: 4000x, Tilt = -15 °). The ALD deposited thin-film shows good confirmability and clean interface

Non-oxide insulators and semiconductors are materials pool in the semiconductor wafer process that may also exhibit memristive switching behaviors. Those materials can be potentially used for the memristor switching material as well. Some of the materials have been introduced in the previous section. Among the available material, an obvious example of non-oxide semiconductors is nitrides based materials, which has a big potential for memristive phenomena but not well studied. There were a few resistance switching devices incorporating nitrides being reported in the literature, for example, nitrides were used either as an electrolyte material for an electrochemical metallization cell [49] or as an electron trapping medium [50]. But few of them are reported as a mobile ionic species. In principle, ionic switching could also occur in nitrides, such as AlN, in a manner similar to the oxides. The Al-N system has a very simple phase diagram as the Ta-O system does, which may lead to high switching endurance as observed in the TaO_x memristors [23]. The wide band gap, high electrical resistivity of the stoichiometric compound and high thermal conductivity exhibited by AlN could result in superior switching performance, such as a large ON/OFF ratio and a good thermal stability. Most importantly, some metallic nitrides, such as TiN, WN and TaN, are commonly used in semiconductor fabrication foundries as interfacial or cap layer materials as we discussed earlier.

Figure 28 Phase diagram of Al-N-Ti System, adapted from [18]

As we discussed earlier, stoichiometric TiN has atomic 50% each of N and Ti or Ta. For the N concentration more than 50%, the excess N will exist in solid solution in the stoichiometric TiN. That means TiN can be a perfect electrode serving as N reservoir with large solubility. Together with AlN having only two stable solid phases, this makes a semiconducting nitride a possibly more attractive switching material than oxides for memristor applications, because the chemical complexity and potential thermodynamic instability of an interface between an electrode nitride and a switching oxide can be avoided by using nitrides both for the electrode and switching materials. The typical switching loops of the full nitride memristors are shown in Fig. 29:

Figure 29 IV plot of full nitride device with TiN (20 nm) /AlN (8 nm)/Pt (30 nm) stack. a) & b): IV plot in linear scale and log scale of continuous 100 cycles switching at ON Switch: V_{set} -2 V with 2 mA current compliance; OFF Switch: V_{reset} 3 V with 2 mA current compliance. c) & d): IV plot in linear scale and log scale of the 1st cycle (after forming) and after 100 cycles. The plot shows the tight distribution of the switching cycles.

The results shown in Fig. 29 are with a device stack TiN (20 nm) /AlN (8 nm)/Pt (30 nm) stack. The 30 nm Pt is deposited through PVD with a 5 nm Ti adhesion layer. AlN films of 6~8 nm thick were deposited by Plasma Enhanced Atomic Layer Deposition (PEALD) using trimethylaluminum (TMA, $Al(CH_3)_3$) and $N_2:H_2$ (20:40 SCCM) mixed gas as a metal organic precursor and a reactant gas at 625 K [5]. The top electrode was a blanket 20-nm TiN layer grown by PEALD using tetrachlorotitanium ($TiCl_4$) and $N_2:H_2$ (4:40 SCCM) mixed gas as a precursor and reactant gas, respectively, at wafer temperature of 625 K. From Fig. 29, the switching is bi-polar with excellent repeatability and an ON/OFF conductance ratio over 100. The device size was fairly large with 200 μm in diameter and, therefore, the ON current was at the mA level.

Chapter 3 Memristor Device Modeling

For IC design in production applications, accurate and compact device models are essential for circuit simulations that use EDA tools to predict the circuit and product behaviors based on fab manufacturing process parameters. In the Nature paper [3], Strukov et al. proposed a simple one-dimensional model for bipolar resistance switching in TiO_x , which was shown to be equivalent to a memristor element. After that, significant progress has been made in understanding the physical switching mechanism for TiO_x system that is related to the mechanism of coupled electronic and ionic conducting path. For instance, physical processes involved in bipolar switching has been studied and formulated to provide important electrical and dynamical information of the switching for the ion dopant vacancies drift-diffusion in the oxide film under the applied electrical field [51]. A practical TiO_x system memristor device model is provided also [52]. However, at the time of the study, such a practical and accurate model was not available for TaO_x system, which has shown many promising results as mentioned earlier. In order to meet the requirement set by circuit designers for the actual application of memristors, a predictive compact model of TaO_x memristor is urgently needed to be integrated into production design environment into a time domain simulation package for EDA tools like SPICE.

3.1 Memristor models survey

3.1.1 Linear model

Before we introduce our modeling work, we need to survey the previous works first. The earlier works were largely pertaining to TiO_x system memristor since TiO_x memristor was the first memristor materialized and studied mostly so far. As we discussed in Chapter 1, memristance was originally defined strictly as a function of the state variable q [1], where $q(t)$ defines the total charge passing through the memristor though a time window that $q(t) = \int_{t_0}^t i(\tau) d\tau$. The concept was later generalized into a class “memristors” called memristive systems by Chua [2]. From the memristive system perspective, a broader definition of an memristor is given by $v(t) = R(w)i(t)$. W defines the internal state of the memristive system $dw/dt = f(w, i)$. Based on the new definition, memristor is a special case of a memristive system. The current-controlled memristor is described mathematically as:

$$v = R(w, i) \quad (3.1)$$

$$\frac{dw}{dt} = f(w, i) \quad (3.2)$$

where $R(x)$ is a generalized resistance that depends upon the internal state of the device and w is the state variable of the device.

The first physical implementation of the memristor by Strukov et al. [3] was made by using TiO_2 thin-film sandwiched between two platinum electrodes. Previous devices have fixed semiconductor structures and only electronic motion. The memristor

nano-device structure operates in such a way that ionic motion dynamically modulates the semiconductor structure controlling the electronic current. After an electroforming process, oxygen vacancies are formed resulting in a highly conductive channel (TiO_{2-x}) called Conductive filaments that shunt most of the oxide film except for a narrow tunnel barrier w . From High Resolution Transmission Electron Microscopy (HRTEM), the conductive filaments in TiO_x is identified to be oxygen-deficient Magnéli phase (e.g. Ti_4O_7) [53]. By applying a voltage across the device, the tunnel barrier width (w) can be modulated. After the applied voltage is turned off, the oxygen vacancies will not move. Therefore, the tunnel barrier width is frozen. This is how the memristor “remembers” the voltage applied previous. Fig. 30 shows the schematic of the two-terminal memristor based on the HP modeling:

Figure 30 Simplified Memristor model from [3]. a) On and off resistance from doped (oxygen-deficient) and un-doped region; b) the TiO_x consisted of doped and un-doped region; c) schematic representation of the doped and un-doped region

From the above simplified architecture, Strukov *et al.* summarizes an ideal and simplified description of how the actual memristor behaves, as below:

$$v(t) = M(q)i(t) = \left[R_{\text{ON}} \left(\frac{w(t)}{L} \right) + R_{\text{OFF}} \left(1 - \frac{w(t)}{L} \right) \right] i(t) \quad (3.3)$$

where R_{on} is the doped (oxygen depleted) region of TiO_{2-x} , R_{off} is the un-doped stoichiometric region of TiO_2 , w is the doped region thickness and L is the metal oxide (TiO_2) film thickness. The state equation is given as [3]:

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{L} i(t) \quad (3.4)$$

where μ_v is the average drift mobility in unit of $\text{cm}^2\text{S}^{-1}\text{V}^{-1}$.

The above expression is based on the assumption that a uniform electric field is applied across the device, which will cause a linear relationship between drift-diffusion and velocity and the net electric field. Integrating equation 3.4, the following expression can be derived for $w(t)$:

$$w(t) = \mu_V \frac{R_{ON}}{L} q(t) \quad (3.5)$$

q is the amount of charge required to move the boundary from $w \rightarrow 0$ to a distance $w \rightarrow w(t)$.

Memristor memristance is shown below:

$$M(q) = R_{OFF} \left(1 - \frac{\mu_V R_{ON}}{L^2} q(t) \right) \quad (3.6)$$

β is defined as dimension of magnetic flux. Here $\beta = L^2 / \mu_V$ in the unit of sV(Wb). Therefore,

$$M(q) = R_{OFF} \left(1 - \frac{R_{ON}}{\beta} q(t) \right) \quad (3.7)$$

Submitting equation 3.7 to $v(t) = M(q)i(t) = M(q)\left(\frac{dq(t)}{dt}\right)$

we have

$$v(t) = R_{OFF} \left(1 - \frac{R_{ON}}{\beta} q(t) \right) \left(\frac{dq(t)}{dt} \right) \quad (3.8)$$

Re-arranging equation 3.8, we have

$$v(t)dt = R_{OFF} \left(1 - \frac{R_{ON}}{\beta} q(t) \right) dq(t) \quad (3.9)$$

Since $\varphi(t) = \int v(t)dt$, integrating both sides of equation 3.9 and re-arranging, we have

$$\frac{\varphi(t)}{R_{OFF}} = q(t) - \frac{R_{ON}}{2\beta} q(t)^2 \quad (3.10)$$

The solution of equation 3.10 is

$$q(t) = \frac{\frac{2\beta}{R_{ON}} \pm \sqrt{\frac{4\beta^2}{R_{ON}^2} - \frac{4.2\beta\varphi(t)}{R_{OFF}R_{ON}}}}{2} = \frac{\beta}{R_{ON}} \left(1 \pm \sqrt{1 - \frac{2R_{ON}}{\beta R_{OFF}} \varphi(t)} \right) \quad (3.11)$$

In the case of $w \rightarrow 0$, we have $R_{OFF} \approx M(0)$, and recall $M(q) = \frac{d\varphi(q)}{dq}$, we have one solution from equation 3.11:

$$q(t) = \frac{\beta}{R_{ON}} \left(1 - \sqrt{1 - \frac{2R_{ON}}{\beta R_{OFF}}} \varphi(t) \right) \quad (3.12)$$

Since $i(t) = \frac{dq(t)}{dt}$, differentiating equation 3.12 with respect to t , we have

$$i(t) = \frac{dq(t)}{dt} = \frac{\frac{d\varphi(t)}{dt}}{R_{OFF} \sqrt{1 - \frac{2R_{ON}}{\beta R_{OFF}}} \varphi(t)} \quad (3.13)$$

Substituting $v(t) = \varphi(t)/dt$ and $\beta = L^2/\mu_V$, equation 3.12 gives the expression of IV relationship for the linear drift case:

$$i(t) = \frac{v(t)}{R_{OFF} \sqrt{1 - \frac{2\mu_V R_{ON}}{L^2 R_{OFF}}} \varphi(t)} \quad (3.14)$$

Comparing to equation 3.6, equation 3.14 gives the alternative expression in terms of $\varphi(t)$, which completes the arguments for the linkage between $\varphi(t)$ and $q(t)$. From both equations, we can find out that the memristance and TiO_2 thickness L are in inverse square relationship. Thus, the memristance becomes more critical as the memristor device critical dimension shrinks. Based on the above linear drift modeling, the following IV diagram is obtained from the simulation [3]:

Figure 31 IV plot for TiO_x memristor based on linear drift model, adapted from [3]

Another notable point for the memristor is the polarity, which designates the doped and un-doped region directions. Polarity coefficient was added by Joglekar & Wolf [54], which categorized the behavior of two memristors in series as below:

Figure 32 Updated linear memristor model from [54]. a) Schematic representation of the doped and un-doped region; b) & c): Two memristors joint in series with different polarities, adapted from [54].

As shown in the Fig. 32, when both memristor doped regions are simultaneously separated, the memristor effect is retained; when two memristors with opposite polarities were put into series, the net memristive effect will be suppressed. When the polarity coefficient η is defined, the polarity of memristor will be labeled as $\eta = \pm 1$. The simultaneous polarity memristor will have $\eta = +1$ and the opposite polarity memristor will have $\eta = -1$. With the polarity coefficient, the state equation stated in equation 3.4 will become

$$\frac{dw(t)}{dt} = \eta \mu_v \frac{R_{ON}}{L} i(t) \quad (3.15)$$

With the introduction of the polarity coefficient, equation 3.14 will become

$$i(t) = \frac{v(t)}{R_{OFF} \sqrt{1 - \eta \left(\frac{2\mu_v R_{ON}}{L^2 R_{OFF}} \right) \varphi(t)}} \quad (3.16)$$

Linear model is able to show the memristor idiosyncrasy pinched-hysteresis loops switching curve. However, the major drawback of these models is that they are not good for describing the stochastic behaviors naturally exhibited by the memristor devices. For instance, such a model is not suitable for practical SPICE simulations for TiO_x or TaO_x memristors due to its more complicated internal states and switching mechanisms, which cannot be predicted in a straightforward manner. The ionic motion within a device produces a much more complicated relationship between the drift-diffusion process and the electric field applied; thus, a spatial ionic distribution will impact its electronic properties. Another major drawback for the linear ion drift model is that it does not take into account the boundary effect. The boundary effect is that the boundary between the doped and up-doped regions' shift speed is strongly suppressed when it approaches either side of the edge ($w \sim 0$ or $w \sim L$). In the center region, it can maintain a more constant speed [54]. A more complicated model with practical physical considerations is needed to describe the dynamic behaviors since the ionic front velocity is not constant.

3.1.2 Nonlinear drift model

From previous discussions we know that the shift in the boundary between doped and un-doped regions of a memristor determines the effective total variable resistance of the device. Since the dielectric layer used for a memristor is in the nanometer scale, even for a small voltage applied across the device, a significant electric field (measured at mega V/cm) will be present. Under such high electric field, there will be high nonlinearity in ionic drift-diffusion and other possible chemical interactions inside the device with Joule heating as well due to the high electric fields. Quite a few attempts have been carried out with considering nonlinearity in the state equation to characterize the memristor nonlinearity [55] [56] [57]. There are several different approaches so far based on different mechanisms. Majority involves an introduction of a window function, which is multiplied by $F(x)$ to the right-hand side of equation 3.15, where $x = \frac{w}{L} \in (0,1)$.

$$\frac{dw(t)}{dt} = \eta \mu_V \frac{R_{ON}}{L} i(t) F(x) \quad (3.17)$$

The window function can mitigate the boundary issue for which the linear ion drift model cannot be solved. In Strukov *et al.* [58], the window function is a function of the state variable and it is defined as

$$F(x) = \frac{x(1-x)}{L^2} \quad (3.18)$$

From equation 3.18, we have

$$\begin{cases} F(0) = 0 \\ F(1) = \frac{(1-1)}{L^2} = 0 \end{cases} \quad (3.19)$$

This proposed window function meets the essential boundary condition $F(0 \text{ or } L) = 0$. However, a problem associated with this function is the modeling of the approximately-linear ionic drift when $0 < w < L$. In order to address the nonlinear and approximately-linear ionic drift behavior at the boundaries and when $0 < w < L$, Joglekar and Wolf proposed another window function as below [55]:

$$F(x) = 1 - (2x - 1)^{2p} \quad (3.20)$$

where $x = w/L$ and p is a positive integer.

This window function meets the boundary condition $F(0 \text{ or } L) = 0$. And through the second control parameter p , nonlinearity of their window function can be controlled in the region of $0 < w < L$. The figure below shows the window function value with different integer p values:

Figure 33 Window function $F(x)=1-(2x-1)^{2p}$ with $p=2,5,10$

With the window function introduced, better non-linearity IV curve can be extracted. Below shows an example of the memristor IV curve based on [58]:

Figure 34 simulated IV of memristor with window function, adapted from [57]

Another approach for a practical modeling for SPICE simulation has been developed for TiO_x system [52] based on Simmons's tunneling equation. The treatment included tunneling transport characteristics based upon Simmons's model and a time-dependent differential equation, which had been empirically chosen to fit the observed behavior. Simmons's model is developed to describe the cases when two electrodes are separated by a thin insulating film, and the film is sufficiently thin, current can flow between the two electrodes by means of tunneling. Based on Simmons's tunneling, the following current density can be derived from the model [59]:

$$j = j_0 \{ \phi_I e^{-B\sqrt{\phi_I}} - (\phi_I + e|v_g|) e^{-B\sqrt{\phi_I + e|v_g|}} \} \quad (3.21)$$

where v_g is the voltage across the tunnel barrier, m is the electron mass, e is the electronic charge, h is the Planck's constant, ϕ is the barrier height in eV, $j_0 = \frac{e}{2\pi h \Delta w^2}$, $w_1 = 1.2\lambda w / \phi_0$, $\Delta w = w_2 - w_1$ and $B = \frac{4\pi \Delta w \sqrt{2m}}{h}$

The modified current equation with the fitting parameter is given in [52] for the circuit model:

$$i = \frac{j_0 A e}{\Delta w^2} \{ \phi_I e^{-B\sqrt{\phi_I}} - (\phi_I + e|v_g|) e^{-B\sqrt{\phi_I + e|v_g|}} \} \quad (3.22)$$

$$\text{where } \phi_1 = \phi_0 - \frac{|v_g|(w_1 + w_2)}{w} - \frac{0.1148}{\Delta w} \left(\ln \left(\frac{w_2(w - w_1)}{w_1(w - w_2)} \right) \right)$$

$$w_2 = w_1 + w \left(1 - \frac{9.2\lambda}{2.85 + 4\lambda - 2|v_g|} \right)$$

$$B = 10.24634 \Delta w$$

$$w_1 = 0.1261$$

$$\lambda = \frac{0.0998}{w}$$

From this set of equations, a SPICE model has been derived, which allows realistic circuit design with memristive devices. The simulation results and the corresponding experiment data are shown below:

Figure 35 Modeling of TiO_x memristors based on the Simmons's tunneling, adapted from [52]. a) schematic of the circuit used in the simulation; b) simulated results calibrated with the measured data

The SPICE model given in [52] provides a qualitatively accurate description for TiO_x memristor switching for practical circuit simulations. However, the main problem of this approach is that it used a lot of fitting parameters and it was not scalable to other

oxide system. The table below shows a comparison of various representative linear and nonlinear models for TiO_x or ideal memristors:

Table 1 Comparison of representative available models for TiO_x system memristor

Modeling Mechanism	Proposed By	State Variable And Equation	Control Mechanism & Threshold	Matching Memristive Definition & Memristance Deduction	Modeling Accuracy
Linear ion drift	Strukov [3]	Doped region physical width: $0 \leq w \leq L$ $\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{L} i(t)$	Current controlled, No threshold	Yes, Explicit	Very low accuracy
Non-linear ion drift based on window function	Jogelkar [55]	Doped region normalized width: $0 \leq w \leq 1$ $\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{L} i(t) * F(x)$ $F(x) = 1 - (2x - 1)^{2p}$	Voltage controlled, No threshold	No, Ambiguous	Low accuracy
	Biolek [57]	Doped region normalized width: $0 \leq w \leq 1$ $\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{L} i(t) * F(x)$ $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$	Voltage controlled, No threshold	No, Ambiguous	Low accuracy
	Prodromakis [60]	Doped region normalized width: $0 \leq w \leq 1$ $\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{L} i(t) * F(x)$ $F(x) = j(1 - [(x - 0.5)^2 + 0.75]^p)$	Voltage controlled, No threshold	No, Ambiguous	Low accuracy
	Kvatinsky (TEAM) [61]	Doped region normalized width: $0 \leq w \leq 1$ $\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{L} i(t) * F(x)$ $F_{ON,OFF} = \exp[-\exp(\frac{ x - x_{ON,OFF} }{w_c})]$	Voltage controlled, Yes	No, Ambiguous	Low accuracy
Non-linear mathematical model	Yakopcic [56]	No physical explanation, mathematic model based on points where state variable motion limited (x_p and x_n) and the rate at which the exponential decays (α_n and α_p).	Voltage controlled, Yes	No, Ambiguous	Moderate accuracy
Simmons tunneling barrier	Pickett [52]	Un-doped region width: $\alpha_{OFF} \leq w \leq \alpha_{ON}$ No explicit state equation	Current controlled, Practically exists	No, Ambiguous	Very high accuracy

As mentioned earlier, TiO_x system memristor is one of the earliest materials investigated. Since the introduction of the HP Labs memristor, TiO_x memristors have been extensively studied. Although there are a lot of drawbacks and certain fundamental mechanisms are still not clear yet, TiO_x devices have reasonable good device model for circuit applications. Recently TaO_x memristors has drawn much attention due to good endurance, which have demonstrated high reliability of switching up to a trillion cycles and endurance close to 10 billion switching cycles [23] [62]. Comparing to TiO_x system

memristor, TaO_x system memristor has different switching mechanisms. X-ray Photoelectron Spectroscopy (XPS) shows TaO_x memristor normally consists of two stable phases: more conducting TaO₂ and more insulating Ta₂O₅. Oxygen is believed to migrate between the two phases during switching. But detailed mechanism is still under investigation. The model development work for TaO_x system is under focus recently. In the following section we will describe a two-state-variable memristor model of charged oxygen vacancy drift resistive switches that includes the effects of internal Joule heating on both the electronic transport and the drift velocity (i.e., switching speed) of vacancies in the switching material. The two dynamical state variables correspond to the cross-sectional area of a conducting channel in the device and the gap separating the channel from the electrode. The model was calibrated against voltage pulse sweep and state-test data collected from a TaO_x memristor so that the contributions of the channel gap, area and temperature to switching can be visualized with great accuracy and performance. The successful implementation of the proposed model can enable efficient and accurate memristor circuit simulation.

3.2 Our two state variable modeling work for TaO_x system memristor

3.2.1 Introduction to the prior TaO_x model work

In the previous section we introduced the modeling works done for TiO_x memristors. However from the linear model and nonlinear we introduced, they are mainly focused the description of the switching operations and behaviors of the conductive filament without a clear link to the material properties and physical mechanisms. With various failure analyses and switching mechanism work, we already understand that memristor devices are coupled electro-ionic systems that display strongly nonlinear behaviors in both the electronic transport and the charged vacancy/ionic motion [3] [63] [64] [65] [66] [67] [68] [37] that controls the conductivity. Thus, a comprehensive physical description of the forming and switching operations with the charge transport in HRS and LRS is needed for a good predictive model. Several studies have shown that an oxygen deficient conducting channel is formed inside the switching layer of transition-metal-oxide based memristors, such as TaO_x, TiO_x, and HfO_x [14] [63] [66] [37] [17] [69] [70] [71] [72] [73] [74] [75] [76] [13] [23] [38]. Many experiments have been performed to investigate the switching behavior and mechanisms associated with these channels [14] [63] [37] [17] [74] [76] [23] [47] [26] [77] [38] [78] [53] [79]. Different models have been proposed to explain the experimental behavior [80]. For example, TaO_x resistive switches [81] [82] have been simulated using memristor models with one state variable that show reasonable agreement with experimental data. In particular, the model of Strachan et al. [81] reproduced fast switching behaviors at relatively high voltage amplitudes. The present model based on two state variables is a complementary view in that it accurately describes the behavior under low-to-intermediate voltages (calibrated up to ~0.6 V). Kim et al. [83] have proposed a TaO_x model that contains a set of coupled equations and focuses on thermo-electric effects, but such a model is likely too slow to be useful

in production circuit simulations. Models for other material systems such as HfO_x [66] [84] [85] [71] [72] [84] propose field-driven ion migration or electron-trap dynamics as explanations for memristive switching. TiO_x memristor models [69] exemplify systems with electron tunneling and nonlinear switching dynamics. Here, we present a heuristic two-state-variable memristor model that combines axial drift of charged vacancies in an applied electric field for bipolar switching and radial vacancy motion caused by thermophoresis and diffusion for unipolar switching [86]. This model illustrates the details of the state variable changes during multiple memristor reading cycles, especially the longer term changes that can occur because of thermally-driven unipolar effects.

Although the continuity equations for ions, electrons and heat can in principle be solved simultaneously with the Poisson equation to understand resistive switching behavior, such computations require many hours on very large computers, when what is needed are good approximations that will execute in microseconds on a work station. Compact models of resistive switches are best represented by the memristor quasi-static conduction, or state-dependent Ohm's Law, and dynamic state equations of Chua and Kang [2], in which the current-voltage relation depends on one or more state variables that evolve in time when a current is flowing through the device. To date, most of the models have utilized only one state variable. However, the fact that transition metal oxides often display two different resistance switching behaviors even in the same device [39], a bipolar mechanism for which ON and OFF switching depends on the polarity of the applied voltage, and a unipolar switching mechanism that is independent of voltage polarity and thus most likely related to Joule heating, is strong evidence that there could be at least two state variables interacting with each other during a switching process [67] [86]. We have developed an empirical memristor model using the 'black-box' approach to nonlinear circuit element modeling [87] [88] with two-state variables and have calibrated it against experimentally measured data from a TaO_x device to illustrate the potential of the model for memristor circuit simulations. The proposed modeling here is based on two-state variables: A (filament tip area) and h ("gap"). h is determined by nonlinear drift of vacancies. A is determined by Fick and Soret effect. These two independent variables can form various scenarios of filament shape. We focus on the dynamical behavior of the geometry of a conducting channel in a transition metal oxide film. Fig. 36 shows a schematic of the structure, including the insulating film, the top and bottom electrodes, and a conducting channel that nearly but not quite bridges the two electrodes. The channel is defined to be that region in the otherwise insulating film that contains enough O vacancies to have a metallic conductivity [14] [3] [17] [64] [63] [77]. The channel is approximated here as a cylinder with cross-sectional area A and gap h between the end of the cylinder and the unconnected electrode, which are the two independent state variables in the memristor model. The electron transport mechanism through the gap may be the result of several different tunneling or activated mechanisms either in parallel or a sequential series that depends on the nature of the gap (the value of h) for a particular state [14] [17] [74].

Figure 36 Schematic representation of the two state variable models. On the left is the model for a memristor with a serial resistor (parasitic resistance) R_s . Memristor resistance consisted of two parts: R_1 is the resistance attributed to the filament and R_g is the resistance attributed to the gap. On the right it shows the memristor structure (not to scale) with the switching layer specifically highlighted. The conducting channel is approximated by a cylinder that contains a high enough O vacancy concentration to be nearly metallic. The two dynamical state variables for the system are the channel cross-sectional area A (filament tip area) and the gap width h ("gap") between the end of the channel and the opposing (bottom) electrode. h is determined by nonlinear drift of vacancies. A is determined by Fick and Soret effect.

3.2.2 Physical modeling and governing equations

From the schematic shown in Fig. 36, we can have following expression for the voltage and current relation with respect to the conductance:

$$I = VG \quad (3.23)$$

where state-dependent conductance $G(h, A)$ is the overall conductance and defined as (for the convenience of programmability, we choose to use conductance instead of resistance expression. However, these conductance and resistance notation is still corresponded to each other):

$$G = \frac{1}{\frac{1}{G_s} + \frac{1}{G_l} + \frac{1}{G_h}} \quad (3.24)$$

We define the variables and parameters as follows: The conductance of the wires and other external connections to the memristor is defined as G_s . G_l is the channel conductance and G_h is the gap conductance.

Poole-Frenkel emission describes the current conduction when trapped electrons get excited into the conduction band of the oxide [89]. In the Poole–Frenkel effect, the electron under a large electric field does not need as much thermal energy to get into the conduction band because part of this energy comes from being pulled by the electric field. In other words, the electric field decreases the coulombic potential barrier of the electrons and subsequently increases its probability for being thermally excited out from the traps in the oxide region. The schematic energy band diagram of Poole-Frenkel emission is depicted in Fig. 37.

Figure 37 Schematic energy band diagram of Poole-Frenkel emission in a metal-oxide-metal structures

From the equation expression perspective, the exponential part of Poole-Frenkel expression is quite similar to Schottky emission portion. The difference is that the junction barrier height (Φ_B) in Schottky emission is replaced with the depth of traps' potential well (Φ_T) in Poole-Frenkel emission and the barrier lowering effect in Poole-Frenkel is double of Schottky emission due to immobility of positive charge. The current density of Poole-Frenkel expression J_{P-F} can be expressed as in the following equation:

$$J_{P-F} = q\mu N_c E \exp\left(-\frac{q\phi_T}{kT}\right) \exp\left(\frac{q}{kT} \sqrt{\frac{qE}{\pi\epsilon}}\right) \quad (3.25)$$

where μ is the electronic drift mobility, N_c is the density of states in conduction band, E is the applied electric field, Φ_T is the depth of traps potential, k is the Boltzmann constant and T is the absolute temperature.

In our device modeling, the electronic transport in the gap region G_h is modeled with an modified Poole-Frenkel emission conduction equation [81], and the two-state variables enter into the expression for the total conductance in a straightforward fashion.

$$G_h = \frac{I}{V} = \frac{J_{P-F}A}{V} = \frac{\sigma_1 A}{h} \exp\left(-\frac{\varphi}{kT_c}\right) \exp\left(\frac{e}{kT_c} \sqrt{\frac{e}{\pi\epsilon_r\epsilon_0} \frac{V_0}{h}}\right) \quad (3.26)$$

where φ is the activation energy for electrons in the gap region; σ_1 is the conductivity of the gap when the barrier height is zero; k is the Boltzmann constant; T_c is the internal local temperature inside the memristor; T_0 is the ambient temperature (assumed to be 300K); e is the electron charge; ϵ_0 is the vacuum permittivity; and ϵ_r the stoichiometric oxide relative permittivity. V_0 is a parameter with units of volts that is used in the transition of the conduction mechanism between the tunneling-like states and the ohmic state of the device.

The resistance of the filament can be calculated as resistance of a cylinder. For the filament resistance, we need consideration of the thermal effect. The thermal resistivity of the system $\mathcal{V}$ is the relation between temperature increase and power dissipation in the memristor; the internal temperature of the conducting channel and gap region is assumed to be

$$T_c = T_0 + \gamma I \left(V - \frac{I}{G_s}\right) \quad (3.27)$$

The conductance of the filament channel is:

$$G_1 = \frac{I}{V_1} = \frac{\sigma_0 EA}{E(D-h)} = \sigma_0 \frac{A}{D-h} \quad (3.28)$$

where D is the total width of the oxide film, the variable h is the gap width, and $D-h$ is the length of the conduction channel. The channel conductivity σ_0 varies approximately with the temperature T_c as

$$\sigma_0(T_c) = \sigma_0(T_0) \frac{1}{1 + \beta(T_c - T_0)} \quad (3.29)$$

where β is the temperature coefficient of resistivity, $\sigma_0(T_0)$ is the conductivity at ambient temperature, and $\sigma_0(T_c)$ is the conductivity at temperature T_c .

Considering the contributions of the external wires, the conducting channel, and the gap conductance, we substituted equation 3.26 and 3.28 to 3.24 and obtain the overall state-dependent conduction equation as below:

$$G = \frac{1}{\left(\frac{1}{G_s} + \frac{D-h}{\sigma_0 A} + \frac{h}{\sigma_1 A} \exp\left(\frac{\varphi}{kT_c}\right) \exp\left(-\frac{e}{kT_c} \sqrt{\frac{e}{\pi\epsilon_r\epsilon_0} \frac{V_0}{h}}\right)\right)} \quad (3.30)$$

With the overall conductance established, now we come to each part of the equations. Next we need to consider the two dynamical state variables for the system, which are the channel cross-sectional area A (filament tip area) and the gap width h

(“gap”) between the end of the channel and the opposing (bottom) electrode. As we mentioned earlier that h is determined by nonlinear drift of dopant vacancies. A is determined by Fick and Soret effect. To get h and A , we need to start from the thermodynamics first. The Heat Equation is based on applying conservation of energy to a differential control volume within the interested region, through which energy transfer is exclusively by conduction, i.e. change in thermal energy storage is sum of the net transfer of thermal energy into the control volume (inflow-outflow) and thermal energy generation, expressed as below equation:

$$\rho c \frac{\partial T}{\partial t} = \frac{\partial}{\partial x} \left(k \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(k \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(k \frac{\partial T}{\partial z} \right) + \dot{q}(x, y, z, T) \quad (3.31)$$

where ρ is the density, k is the thermal conductivity and c is the specific heat.

Due to the Joule heating, we have the thermal energy generation as below in 1D dimension:

$$\dot{q} = J(r)E = \frac{J(r)^2}{\sigma} \quad (3.32)$$

From the above model shown in Fig. 36, in the horizontal direction, we have the radial heat equation:

$$\rho c \frac{\partial T}{\partial t} - \nabla \bullet \kappa \nabla T = \frac{J(r)^2}{\sigma} \quad (3.33)$$

And since we can neglect the current outside the filament, we assume the current density $J(r) = \begin{cases} J, & r \leq b \\ 0, & r > b \end{cases}$ where b is the radius of the filament tip and $A = 2\pi b^2$ with cylinder tip area consideration.

To get the current density J , we need to consider several factors first. For the mobile species moving, there are three main factors that determine the movement [86]: the presence of a concentration gradient (Fick diffusion), an electric field for charged particles like electrons or ions (Drift) and/or a temperature gradient (thermophoresis or Soret effect diffusion). The corresponding fluxes induced by these gradients in one dimension is shown in below schematic:

Figure 38 Schematic illustration of the 3 possible mechanisms for ions motion. a) Fick diffusion due to concentration gradient; (b) Drift under electrical potential gradient; (c) Thermophoresis (Soret effect diffusion) due to temperature gradient.

The current density of diffusion can be expressed as below expression:

$$\vec{J} = \vec{i}J_x + \vec{j}J_y + \vec{k}J_z = -D\left(\vec{i}\frac{\partial c}{\partial x} + \vec{j}\frac{\partial c}{\partial y} + \vec{k}\frac{\partial c}{\partial z}\right) \quad (3.34)$$

For 1D dimension, current density of Fick diffusion, Drift and Soret effect diffusion is shown as below:

$$J_F = -D_f \nabla n \quad (3.35)$$

$$J_{drift} = D_f n E q / (kT) \quad (3.36)$$

$$J_S = -D_f S n \nabla T \quad (3.37)$$

where n and T are the density of vacancies and local temperature, respectively, E is the electric field, S is the Soret coefficient for vacancies, and k is the Boltzmann constant. Under high electrical field for the nano meter thin oxide, D_f is the position dependent diffusion factor for the vacancies, given by the expression:

$$D_f = f a^2 \exp\left(\frac{-U_a}{kT}\right) \quad (3.38)$$

where f is the effective vibrational frequency of the vacancies within their confining potential wells, a and U_a are the lattice distance and the energy barrier between the potential wells, respectively. In the horizontal direction, we have the following equation:

$$J_F = -D_f \nabla n, J_S = -D_f S n \nabla T, J_{drift} = D_f n E_{horizontal} q / (kT) \approx 0 \quad (3.39)$$

Neglecting the drift current, the continuity equation is shown as below from the conservation of the ions motion:

$$\nabla \bullet (J_F + J_S) + \frac{\partial n}{\partial t} = 0 \quad (3.40)$$

By combination of the continuity equation 3.40 with equation 3.33 and 3.39 with boundary consideration, we will get the following equation after long derivation:

$$\frac{\partial A}{\partial t} = \frac{2D_f}{a} \left(-\pi(S\gamma I^2 \frac{D}{\sigma A} + \Delta') + \frac{SI^2}{4\sigma\kappa A} \right) \quad (3.41)$$

where Δ' is a small derivative item from the equations for the diffusion effect.

Equation 3.41 shows that the area A changes with the electrical and thermal effect. The expression can be simplified by introduce new parameter α , which is a parameter that relates power density inside the memristor to the rate of radial vacancy motion and the parameter Δ , which is the critical power density above which the thermophoretic vacancy flux (which is directed inward toward the center of the channel, since vacancies migrate up a temperature gradient) exceeds diffusion (directed outward, i.e., down the vacancy concentration gradient) and the channel cross section area grows. The dynamical equation for the conducting channel area A is approximated as below:

$$\frac{\partial A}{\partial t} = \alpha \left(\frac{I^2}{A} - \Delta \right) \quad (3.42)$$

The above conclusion is corresponded to the conclusion from [86] considering the competition between vacancy diffusion and thermophoresis. We can see that, for a fixed total power (or current I), the area will increase until it reaches a steady-state value if the initial value of A is small; and vice versa. Similarly, an increase (decrease) of the current will increase (decrease) the value of A . This behavior can lead to a gradual and long-term change in the operating characteristics of a device.

The nonlinear drift velocity of the vacancies under the field enhanced diffusion by hopping mechanism is shown as below [69]:

$$v_f = \frac{2}{a} D_f \sinh \left(\frac{ZqEa}{2kT} \right) = af \sinh \left(\frac{qEa}{2kT} \right) \exp \left(\frac{-U_a}{kT} \right) \quad (3.43)$$

where Z is the charge state of the ion.

Therefore, in the vertical direction (parallel to the axis of the channel), an applied electric field moves the vacancies, causing the end of the conducting channel to extend or contract [69] [3]:

$$\frac{\partial h}{\partial t} = v_f = af \sinh \left(\frac{qEa}{2kT_c} \right) \exp \left(\frac{-U_a}{kT_c} \right) \quad (3.44)$$

$$E = \begin{cases} \frac{V - \frac{I}{G_s} - \frac{I}{G_1}}{h}, & (\text{ON switching}), \\ \frac{I}{G_1(D-h)}, & (\text{OFF switching}) \end{cases} \quad (3.45)$$

where t is time, v_f is the nonlinear drift velocity of the vacancies.

3.2.3 Simulation verification with experimental results

We now have a set of key equations to describe the dynamical switching behavior of a memristor based on oxygen vacancy axial drift and radial thermophoresis in a thin metal oxide film. In order to calibrate our model, we built the plan of record TaO_x system device and performed both pulse sweeps and state tests to compare our simulation results with experimental data. Firstly, we fabricated and measured TaO_x memristor disk devices with a diameter of 100 μm . All the samples had identical thin-film stacks obtained from the same processing run with a stack structure (top to bottom) of Pt 10 nm/Ta 30 nm/TaO_x 11 nm/Pt 100 nm/Ta 1 nm. The broad area bottom Pt electrode preceded by a 1nm Ta adhesion layer was sputter-deposited onto a thick SiO₂ film on a Si substrate, and served as a common ground. Subsequently, a blanket 11nm Ta₂O₅ oxide layer was sputter-deposited onto the bottom electrode at room temperature. Circular 30nm thick Ta electrodes were deposited on top of the oxide through a shadow mask at ambient temperature, followed by 10nm of Pt for a protection layer to prevent oxidation in air and obtain better electrical contacts. The device stack and measurement procedure is shown schematically in the following figure.

Figure 39 Schematic illustration of the experimental procedure. TaO_x memristors were fabricated on a Pt/Ta blanket bottom electrode by depositing an 11 nm TaO_x film and 100 micron diameter Ta top electrodes. Two-wire electrical characterization was performed by applying a pulse with a defined voltage and time across an individual device and determining the resulting state by measuring the current through the device at +0.2 V.

We performed two-probe measurements using the waveform shown schematically in Fig. 40 below on the memristors to obtain switching curves.

Figure 40 Schematic illustration of the waveform of the pulse sweep test. The device state was changed using a ramped set of $2 \mu\text{s}$ pulses that increased or decreased by 0.01 V per subsequent step. After each pulse, a $1 \mu\text{s}$ reading pulse of $+0.2 \text{ V}$ was applied across the device and the current measured to reveal the state of the memristor.

The testing apparatus contains an endurance test board which can also be used to perform pulse sweep test, a current compliance board and a microscope. The endurance board can supply different pulses under different operation modes. The forming was done also using the pulse sweep, in which we control the forming voltage and sweep voltage intervals and pulse width. The memristor device was formed to a steady high conductance state, after which we performed several small voltage Read. Then we performed the OFF switching to tune the memristor to low conductance state and began our experiments. The current compliance board can control the current compliance. In our measurements, we turned the current compliance off in order to observe the full behavior of current during switching. The external series resistance was determined to be 258 ohm in our experiments, which was included in the simulations. The measured and simulated IV plots are shown in Figs. 41 a-b.

Figure 41 Pulse sweep test measurement results and model simulations. (a) (b) Linear and log scale of the sweep IV curve: experimental data and simulation result comparisons. (c) Conductance vs. voltage pulse comparison. (d) Simulated temperature vs. pulse number (and thus amplitude). The temperature value was determined for the simulation of the ramped voltage pulses, not the reading pulses. This was done to see the temperature change during the switching process. (e)(f) Experimental and simulated conductance-voltage plots for sequential switching. (g)

Gap width h vs. pulse number. (h) Channel cross-sectional area A vs. pulse number. All simulation results except for temperature were obtained at the reading voltage of 0.2V (1 μ s).

Experimentally, we saw that the memristor switched ON at about +0.8 V and OFF at about -1.3 V, with the corresponding switching current up to the mA level. In our simulations, the switching voltages and pulse widths were the same as those used in the measurements, and the simulated IV curves agreed well with the experimental data. We also plotted the conductance vs. the applied pulse voltage in Fig. 41 (c). The simulation results agreed quantitatively with the experimental data except after the turning point voltage during OFF switching. This discrepancy was mainly due to the stray capacitance of the measurement system (not included in the simulation), which caused the switching voltage to be larger and slower than the isolated memristor considered in the model. Figure 41 (d) shows the calculated internal temperature during switching as a function of pulse number over five consecutive switching cycles. The model predicts that the maximum temperature increase for the specific device and operating conditions described here is less than 140 K above ambient. The temperature is maximized when the memristor is biased in the ON state, and it is minimized each time the applied voltage is near zero (so the power dissipated in the device is near zero). To observe the influence of the two-state variables during multiple ON/OFF sequences, we plotted the measured conductance vs. pulse voltage results for five consecutive switching cycles in Fig. 41(e) and the simulated results in Fig. 41(f). The experimental results were highly reproducible. The model behavior is in excellent quantitative agreement with the experimental results (except as noted before in the region after the OFF-voltage turning point) [90]. Figure 41(g) shows the simulated dynamical behavior of the gap width h , which varied from ~ 2.0 to ~ 0 nm (physically reasonable values) as a function of switching from the OFF to the ON state, over the five consecutive switching cycles. The large relative change in the gap width in each cycle was responsible for most of the change in the conductance state of the device during switching, and the fact that the OFF state was nearly the same for each cycle accounts for the reproducibility of the simulated conductance vs. device voltage plots. Figure 41(h) shows the channel cross section area A vs. pulse number. The initial area of $\sim 10^4$ nm² corresponds to a channel diameter of ~ 110 nm, which is in good agreement with previous observations of the active channel width that forms in a large area TaO_x device [26]. The oscillations in A vs. pulse number have a significant amount of structure, which indicates that the competition between thermophoresis and radial diffusion is active. The variation of the channel area during a single cycle was less than 2%, and the trend of the A state variable was to decrease by $\sim 2\%$ during the initial five ON-OFF cycles. Thus, the thermophoretic variations of the channel area are much slower than the changes in the gap width for the voltages and currents investigated, and the area state variable A is mainly detectable as a long-term systematic change in the conductance state of a device.

To further exercise the model, we performed a state test on the memristor devices with the waveform shown schematically in Fig. 42.

Figure 42 Schematic illustration of the waveform of the state test. The voltage pulses all have the same amplitude, but the pulse width increased exponentially with pulse number. We applied a small reading voltage of 0.2 V (10 μ s) and measured the current to determine the state of the device after each state-evolution pulse. The total time at voltage shown here was 0.101 s, and the minimum pulse width was 1 μ s. For each state test, we tuned the memristor to the appropriate initial state for the subsequent ON or OFF switching test.

The experimental setup was different from the previous one, in which we used the Agilent B1530 Parameter Analyzer to provide the pulses and control the state test. During the measurement, each pulse with an exponentially growing pulse width is applied on the memristor, after which a single short reading pulse is applied (0.2 V, 10 μ s). The experimental and simulation results for times from one microsecond to 0.1 second and a selection of bias voltages are compared in Fig. 43.

Figure 43 State test results and model simulations. Both positive and negative voltages were applied in the state tests on the same memristor. Small voltages did not change the state of the device significantly. Large voltages switched the device from the OFF/ON to the ON/OFF state. Abrupt changes in conductance vs. time were observed for both experimental data and model simulations. All simulation results were obtained at the reading voltage of 0.2 V (10 μ s).

From the above plot, we can see that small voltage amplitudes (e.g., $|V| \leq 0.3$ V) do not change the conductance substantially, showing that the reading voltage did not cause a significant measurement error of the state in the experiments. Interestingly, both voltage polarities for $|V| = 0.3$ V caused the conductance of the devices to increase slightly over long times (a unipolar switching effect), even though for the -0.3 V case the device was already in a nominally ON high conductance state. For intermediate voltage amplitudes (e.g., ± 0.6 V), there are significant conductance changes over a time

scale of 0.1 second, with a long induction time for ON switching followed by a fast and limited switching event, and a quick OFF switching followed by a long period of little conductance change. The simulations reproduced the trends in the experimental data quite well. A notable observation for ± 0.6 V biases was that OFF switching was about two orders of magnitude faster than ON switching for TaO_x devices; this was predicted from the high speed switching studies of Strachan et al. when extrapolated back to the lower voltage amplitude range [81], which also correctly determined the absolute switching ON and OFF times observed in our data.

Figure 44 (a)(b) The gap h vs. time. Dramatic changes in h were observed for voltage amplitudes 0.6V. (c)(d) The area A vs. time, for positive/negative state evolution voltages. The +0.3 V state test was performed just after the +0.2 V test. Thus we applied consistent state variable values for the +0.3 V simulation. Areas changed

slowly with time. For negative biases, the memristor was reset from the ON state, which was obtained from continuously applying positive voltages. The initial areas should be larger than those for positive voltage state test cases. (e)(f) Temperature vs. time. High temperatures correspond to the ON state with large voltage amplitudes. All simulation results except for temperature were obtained at the reading voltage 0.2 V (10 μ s).

In Fig. 44, we plotted the state variables and internal temperature for memristor switching as a function of time obtained from the simulations for the cases analyzed in Fig. 43. In Fig. 44(a)(b), the small amplitude voltages $|V| \leq 0.3$ V did not cause the gap width to change significantly, which is the reason for the small conductance changes observed in Fig. 43. The gap width did change dramatically under intermediate and large biases $|V|=0.6$ V, meaning that the memristor successfully switched ON/OFF. This shows that the gap width change dominates the ON/OFF state switching. Figures 44 (c)(d) show A as a function time. At low voltages, the changes in A were generally small and required a significant amount of time to accumulate to the point where they could be observed. In Fig. 44(c), the reading voltage of +0.2 V caused the area A to gradually decrease while a +0.3 V bias first minutely reduced the area and then increased it. These observations show that the simulated power density was always below the critical value Δ for the OFF-state device at +0.2 V, and thus radial out-diffusion was slightly larger than inward thermophoresis drift in equation 3.42. For the +0.3 V simulation, the initial simulated power density was still less than Δ , so the area decreased slightly. However, as the conductance of, and thus the current through, the device increased (because of the change in h), the power density increased and eventually exceeded Δ , after which the channel area increased. For a bias of +0.6 V, the power density was always larger than Δ and thus A increased at a slow rate over the entire ON-switching simulation time. In Fig. 44(d), a small voltage of -0.3 V on a device initially in the ON state caused the area A to increase, leading to the unipolar increase in the conductance observed in Fig. 43(b). For larger amplitude negative biases (-0.6 V), the area decreased gradually over the time of the simulation. Figs. 44 (e)(f) show the simulated internal temperature, and the high temperature is seen in ON state under large voltages. However, the area variable has an obvious influence on the conductance and is usually responsible for over switching (too conductive and hard to be turned OFF).

The parameters used in our simulations after the calibrations are in summarized Table 2 below.

Table 2 Values of physical constants, device constants, and model parameters used in this modeling study

Physical Constants	ϵ_0	k	e
Value	8.854E-12	1.381E-23	1.602E-19
Units	F/m	$m^2 \cdot kg/(s^2 \cdot K)$	C

Device Constants	Device Diameter	D	f	a	ϵ_r	T_0
Value	100	11	1E+13	0.3	20	300
Units	μm^2	nm	Hz	nm		K

Model Parameters		V_0	γ	β	U_a	ϕ
Value	Pulse sweep test simulation	0.1	8E5	0.01	0.62	0.13
	State test simulation		3E5		0.75 (ON) 0.96 (OFF)	0.02
Units		V	K/W	1/K	eV	eV

Model Parameters		$\sigma_0(T_0)$	σ_1	α	Δ	R_s
Value	Pulse sweep test simulation	8E2	2E1	3E-19	1.2E6	258
	State test simulation	5E3		3E-22	3E6 (ON) 3E7 (OFF)	10
Units		S	S	m^4/A^2s	A^2/m^2	Ω

There are differences between the parameters used in the pulse sweep and state tests in part because the devices used were different and the process used to form the devices can yield significant differences between devices, and the instruments used to collect the data were different, and with such a simple model, it is difficult to completely remove the influence of the test system from the model. Thus, when using this model for circuit simulation and design, it is important to calibrate it for memristors in the circuit of interest. As we have seen previously, for the model [67] [81], we needed different values for some parameters for ON and OFF switching simulations; a more complex/complete model is required to utilize a single set of parameters that is independent of the initial state of the device. The two state variables control differently

in memristor switching. The gap width represents the electric field contribution to the conduction, while the area reflects the Joule heating effect during switching. The electric contribution makes the memristor to be bipolar switching, and the Joule heating tends to give unipolar switching. Those two aspects compete and determine the final switching state of a memristor.

3.2.3 Summary and recommended further work

In summary, we developed a new two-state-variable memristor model and calibrated it with experimental low-to-intermediate voltage amplitude pulse sweep and state test switching data on simple TaO_x devices. The model reproduced the experimental data reasonably well over the calibration voltage range. The relatively large test circuit capacitance was responsible for most of the difference observed between simulated and experimental data for the pulse sweep mode. The gap width state variable h was responsible for most of the change of the device conductance within a single switching cycle. The area state variable A was responsible for longer time-scale systematic changes in device conductance over many cycles and is, therefore, important in understanding issues such as long-term switching stability and endurance. This compact model is suitable for fast circuit simulations (e.g., SPICE-level) because of the simple form of the dynamic equations for the state variables. Below table summarizes the existing representative TaO_x models' key features and comparisons.

Table 3 Representative TaO_x models key features and comparisons

Models	John Paul's (HP)	Patrick's(Sandia)	Kim's (Samsung)	Our new model
	<small>J.P. Strachan et al. "State Dynamics and Modeling of Tantalum Oxide Memristors", IEEE TED 2015</small>	<small>P.M. Pickett et al. "A Physical model of switching dynamics in tantalum oxide memristive device", APL 2015</small>	<small>S.H. Kim et al. "Physical electro-thermal model of resistive switching in Bi-layered resistive-change memory", Heliyon 2015</small>	
Model variables
State variables	$y = \frac{A_{Ta}}{A_{Channel}}$	r (radius)	(implicit) n (vacancy density)	A (filament tip area) h ("gap")
Direction	2D	2D	2D	3D
Mechanism	Electric, Thermal, State variable changing, Nonlinear eq	Thermal-Soret, Fick, Electric, State variable changing	Electric, Thermal, non-linear drift	Electric, Thermal-Soret, Fick, non-linear drift, P-F conduction
Simulation capability	I-V switching, dynamics, Different on/off switching for different devices	Standard unified eqs, I-V switching, dynamics, Different on/off switching	Self-consistently set equations, I-V switching	Standard unified eqs, Forming, I-V switching, dynamics, both linear & non- linear

Since our publication [91], more memristor modeling works with various two-state variables have been reported to utilize the modeling variability to precisely capture the complex intrinsic dynamics, for example, the recent work by Kim et al. [92]. Similarly to our two-state variables approach, Kim et al. modeled the second order memristor conducting filament size with state variables of radius (r) and depleted gap length (g). The two variables are determined by input signals and internal parameters such as temperature of the device. As a result, Kim's model is able to capture the inherent dynamic device properties for complicated analog applications like mimicking synaptic plasticity effect. However, up to today, there is no generic memristor device modeling yet to describe the total memristor complex property. Further work is needed for us to incorporate a more physically descriptive model of thermophoresis and to extend the range of validity of the model to higher voltage amplitudes and thus faster switching time.

Chapter 4 Selector For High Performance Crossbar Memory Application

New non-volatile memories need to be cost competitive to achieve rapid and wide adoption on top of the desired performance. Low cost per bit can only be achieved if the memory's density is high and its process and driving circuitry is simple. Today both worldwide research institutions and industry are making a large investment in memristive memory because its non-volatility, low power, low latency, and high endurance enable game-changing new computing architectures where memory and storage functions are merged into a single flat memory tier [93] [94] [95] [96]. There are a few available architectures for the various applications [97] [98] [99]. For the application, One Transistor One Resistor (1T1R) [100] [101] [102] and One Selector One Resistors (1S1R) [103] [104] [105] are studied mostly. For transistor-based structures like 1T1R, it is difficult to achieve the true three dimensional stacks using the back end of line process and the chip size dominated by the select transistor and it should be used for low latency, high speed embedded memory operation. Capitalizing its full potential advantages memristor, demands implementing in large, inexpensive three dimensional stacks architecture crossbar arrays, which enhances density by allowing memory cell layers to be stacked above the physical access circuitry. The density and cost requirements also prevent the use of any large, expensive, individual device to control the current flow through each memory cell during read and write operations. Therefore, this high array efficiency crossbar structure demands the 1S1R architecture, which will enable the memristor and selector stack vertically as a memory cell with the same size. Although progress has been made toward creating selectors together with memristors development for the requisite properties, up to date there is no perfect commercially available solution for the selector mass production. The key work described here is the development on selectors with highly nonlinear two-terminal device that can be paired with each memristor to passively regulate the current flowing through it. Without such a selector, reading and writing individual memristors in a large array is not possible.

4.1 Sneak path current issue and need for selector

The advent of fast, low-power, non-volatile random-access memory with high endurance made from 3D stackable back-end of line process would revolutionize computer architectures by facilitating the consolidation of memory and storage into a flat memory structure. The memristor technology promises to fulfill this vision, ultimately replacing conventional Dynamic Random Access Memory (DRAM), Flash and hard disc drives in both memory and storage roles as high performance memory.

As we discussed in Chapter 2, the most efficient high density structure for memristor is the crossbar structure. The difficulty with this approach is that the memristors are nearly linear ohmic devices despite many engineering works have been done as introduced earlier to improve the device, which makes it difficult to address a given memory cell without inducing unwanted 'sneak path currents' through other cells in the array. Sneak path current problem is an intrinsic problem for all crossbar

architectures [106] [107]. The source of the sneak paths is the fact that the crossbar architecture is based on the memristor as the only memory element without gating like transistors or diodes.

Figure 45 Memristor-based memory array with sneak path current. The memristor device is addressed at the intersection between TE and BE of the array. The sneak path current is highlighted where current sneaks through different undesired paths. The red lines show the desired path and the green ones show the effective sneak paths

When one attempts to read the red memristor cell in Fig. 45 by applying voltage, V , to the middle column and a bias of zero to the middle row, there is an opportunity for current to flow along paths such as the one indicated by the dashed green line. This is true regardless of how the unselected rows and columns in the array are biased. What makes the sneak paths problem more difficult to solve is the fact that the sneak paths and currents depend on the content of the memory. For example, the worst case is that a high resistance state memristor is to be addressed but it is surrounded by all low resistance state memristor neighbors. This is due to the fact that the current will always flow with more intensity through the paths with smallest resistance that is memory content dependent. The application of the large memory demands an accompanying circuit element that enables addressing of individual memristors. The sneak path current can cause several critical issues for the crossbar memrory. For example, it can saturate the driving circuitry and generate unwanted Joule heating during the writing/erasing operations. In addition, sneak paths limit the reading operation or even lead to the wrong memory bit reading because of the large background current level with reduced signal-to-noise ratio. To prevent these sneak currents, a highly nonlinear two-terminal circuit element, known as a selector, must be added in series with the memristor in each memory cell in the cross-bar architecture, as shown in Fig. 46.

Figure 46 Cross bar memory architecture with selector. Current through selected cell is shown in red. One possible sneak current path is indicated by the dashed grey line.

The selector is a highly nonlinear device, which may be used to mitigate the sneak path current issue by operating at a voltage in a different voltage region suppressing the total current passing through the non-selected devices in the array at given voltage. Nonlinearity may depend on the operating voltage range, which in turn depends on the materials used and structure of the device stack, which is memristor plus selector. The selector is normally working with a common electrical addressing scheme called “half-V addressing” scheme for either a reading or writing operation [19] [108]. Assume voltage V is the sufficiently high voltage applied across the addressed cell with bias across its selector, which is large enough to make its resistance relatively small, allowing current to flow through the cell. What half-V addressing scheme does is that to apply $V/2$ to one electrode and $-V/2$ to the other electrode of the required memristor, resulting in a total voltage drop of V across the selected device, while the rest of the memristor cells all have a voltage drop of $V/2$ which share a common row or column electrode with the selected device. Fig. 47 depicts the selector for crossbar memory architecture with half-V scheme.

Figure 47 Selector for crossbar memory architecture with half-V scheme. a) Schematic illustration of selector non-linear IV curve. Increasing the addressing voltage from $V/2$ to V (2 times), the current will increase from I_1 to I_2 in many magnitude ($>10^3$). The selector non-linearity is defined by I_2/I_1 ratio. b) the half-V addressing scheme for crossbar memory with selector. Due to the highly nonlinearity, the unwanted sneak path current will be greatly suspended, depending on high good of the nonlinearity.

Due to the high nonlinearity of the selector, all the other cells rather than the selected cell in the array see a lower bias that is insufficient to drive their selectors to a low resistance state, thereby minimizing the sneak currents flowing through them. Therefore, the selected memristor with full voltage drop maintains good conducting path while the half-selected memristor devices in the crossbar array are all electrically suspended for the current.

Crossbar array is practically limited by the degree of nonlinearity of selector, which will greatly impact the sneak path currents [19]. In order to achieve high nonlinearity for the dense crossbar memory application, various devices have been extensively studied as a selector device, including oxide (eg., Pt/TiO₂/Ti [109]) based Schottky diode, chalcogenide alloy (e.g., AsTeGeSiN [110]) based Ovonic Threshold

Switching (OTS) device, semiconductor (eg. TiN/a-Si/TiN [111]) or oxide (e.g., Pt/TaO_x/TiO₂/TaO_x/Pt [112]) based varistor, NDR (e.g., TiN/ NbO_x/TiN [113], VO₂ [114]) based Metal Insulator Transition (MIT) selector, Mixed Ionic-Electron Conduction (MIEC) [115] selector and, last but not least, Volatile Conducting Bridge (VCB) selector. Each selector is associated with different advantages and disadvantages. For example, Schottky diode based device has low current density and it can be used only for unipolar memristor. Semiconductor based varistor requires high fabrication temperature. And today's most of the selector devices face the major issues of the low nonlinearity. Fig. 48 shows the plot of crossbar array size with the available selectors from the simple memristor-selector background current consideration.

Figure 48 Selector non-linearity plot with crossbar array size for various available technologies.

On top of nonlinearity requirements, the selector device needs to meet other requirements also, such as a sufficient high drive current density over $10^6 \mu\text{A}/\text{cm}^2$ for memristor switching and fast read sensing, high endurance for the switching and read operation, small device variation, compatible operating voltage range with a typical TaO_x or HfO_x-based resistive memory, fab back end of line compatible process and material with scalability, suitable operating temperature (323.15 K to meet the non-volatile memory and 394.15 K for the top end spec for servers) and etc. In 2014 IEDM conference, Jo et al. [116] reported a Field Assisted Superlinear threshold (FAST) selector utilizing a Super-Linear Threshold layer (SLT), where a conduction path is

formed at the threshold voltage and disappears below a hold voltage like volatile switching. The claimed performance is excellent with over 10^{10} nonlinearity, large drive current density, excellent endurance and fast turn-on and off times. However, the actual material system has not been revealed yet. Up to date, there is no known solution as a good production candidate for the selector for the large crossbar memory application. The work contained herein stands the state of the art research of the selector development.

4.2 Tunneling based selector

Tunneling is a quantum mechanical phenomenon, where a particle tunnels through a barrier with a lower energy. Depends on thin-film thickness and barrier properties, there are mainly two types of tunneling: direct tunneling and Fowler–Nordheim (FN) tunneling. Encouraging nonlinearity and current density were obtained from multilayered selector devices inspired by the tunneling barrier engineering concept, such as a-Si/SiN_x/a-Si and Ta₂O₅/TaO_x/TiO₂ tri-layers [117] [118]. Tunneling based selector work herein is continued work from Choi et al. on Tri-Layer Tunnel Barrier (TLTB) selectors [119], which utilize the large nonlinearity through a tri-layer structure consisting of a dielectric with a larger bandgap and smaller electron affinity sandwiched between two other dielectric layers with a smaller bandgap and larger electron affinity. The prior art device structure from Choi (TaN_{1+x} (3 nm)/Ta₂O₅ (2.5 nm)/TaN_{1+x} (3 nm)) [119] is shown below:

Figure 49 TaN_{1+x}/Ta₂O₅/TaN_{1+x} Tri-Layer Tunnel Barrier sandwich structures, adapted from [119]

Comparing with the single tunnel barrier, TLTB utilizing crested barrier tunnel barrier engineering, which uses smaller bandgap/ larger bandgap/ smaller bandgap (L/H/L bandgap profile) multiple dielectric stacks to change the barrier profile, which allows high nonlinearity.

Figure 50 Tunnel barrier engineering. a) Single barrier with simple M-I-M structure; b) crested barrier with M-I (smaller bandgap)/I (larger bandgap)/I (smaller bandgap)/-M multiple dielectric layers structure.

Opposite to variable oxide thickness (VARIOT) approach (H/L/H bandgap profile) [120], in crested barriers, the potential barrier height peaks in the middle and gradually or abruptly decreases toward the conducting electrodes. As a result, FN tunneling of electrons through crested energy barriers is much more sensitive to applied voltage than that through barriers of uniform height. Therefore, when the applied voltage increases, the tunnel current may be changed many orders of magnitude comparing to voltage change [121]. Therefore with the TLTB, both the barrier height and effective width were reduced simultaneously under high-voltage bias, yielding a significantly larger nonlinearity.

The feasibility of using [119] selector with a typical memristor has been demonstrated by externally wiring the selector to a discrete memristor as well as by physically integrating them into a multilayered 1S1R cell with reasonable good performance including high endurance ($>10^8$), low variability, and low temperature dependence. However, the main issue of the device is the not enough high nonlinearity, which is around 10^4 and not sufficient to support large size of the crossbar. The new research work here is trying to improve the nonlinearity of this crested barrier tunneling device with new structures proposed. As we know high quality Al_2O_3 and SiO_2 has much bigger bandgap ($\text{Al}_2\text{O}_3 \sim 7 \text{ eV}$ and $\text{SiO}_2 \sim 9 \text{ eV}$). The idea here is to insert a very thin amorphous Al_2O_3 or SiO_2 layer to the structure of [119] selector. As a result, a more resistive layer is added to increase the selector resistance below the selecting voltage, hence to lower the off leakage current. If the approach works, this will increase the nonlinearity of the current selector. The device structure and concept illustration is shown in the below figure.

Figure 51 Modified structure of $TaN_{1+x}/Ta_2O_5/SiO_2$ or Al_2O_3/TaN_{1+x} Tetra-layer Tunnel Barrier selector with increased resistance at off state.

To test the concept, sample devices with several process splits were fabricated on thermally grown 200 nm thick SiO_2 on a Si substrate. Various thin-films were deposited by remote plasma enhanced ALD. Mixed $N_2:H_2$ (40:1 SCCM) gas or NH_3 (50 SCCM) was adopted as a reactant gas on purpose to change the physical properties of thin-film devices. O_2 (50 SCCM) plasma ALD process was used for creating the Ta_2O_5 and SiO_2 or Al_2O_3 barrier layer. Growth temperature was varied from 575 to 675 K. For the crossbar device, a 20 nm thick electron-beam evaporated Pt ribbon with 1 nm thin Ta film adhesion layer was used as the bottom electrode. Blanket thin-film tunnel barriers were grown by ALD on top of the bottom electrode ribbon, and then a Pt top electrode was deposited by electron-beam evaporation through a shadow mask forming crossbar device. After the devices were fabricated, the four-terminal IV characteristics of the devices were measured using a semiconductor parameter analyzer (Agilent 4156) or Agilent B1500, which can extract the actual voltage drop on the device from the total applied voltage. A quasi-DC voltage sweep was applied to the top electrode with the bottom contact grounded at ambient temperature in all the electrical measurements. Fig. 52 and Fig. 53 show IV plot results with the process splits.

Figure 52 IV characterization plot of various process splits. The $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{SiO}_2$ or $\text{Al}_2\text{O}_3/\text{TaN}_{1+x}$ Tetra-layer Tunnel Barrier selector was compared to the $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{TaN}_{1+x}$ Tri-layer Tunnel Barrier selector with thin-film thickness variation.

Figure 53 Current density vs voltage plot of $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{Al}_2\text{O}_3/\text{TaN}_{1+x}$ Tetra-layer Tunnel Barrier selector with thin-film thickness variation on crossbar and nano-via test structures.

As we can see from Fig. 52, by adding a very thin but more resistive Al_2O_3 and SiO_2 layers, the selector off state current has been effectively reduced while at high voltage, the current is not effected too much. A 2 Å Al_2O_3 and SiO_2 thin-film is almost equivalent to 1-1.5 nm effective thickness of Ta_2O_5 thin-film for the OFF state. As a result, the nonlinearity is increased from initial 10^4 to $4-6 \times 10^4$, which will enable bigger crossbar application. From Fig. 53, we realized that the device structure will be another factor to impact the current and current density, which could be due to the reason of the electrodes effective area and surround current impact. And in general, the tunnel barrier selector has relative low current density comparing to the stringent memory read/write operation, which prohibits it to be the ideal selector for the mass production.

To verify the thin-film properties, various failure analysis methods were done for the characterization. The device cross-section and thin-film thickness were

measured using Transmission Electron Microscope (TEM). The crystallinity of the films was analyzed using an X-ray diffractometer in the lab. The bandgap of the TaNx films was measured optically by UV–vis absorption spectroscopy. The atomic concentrations and elements studies were measured by Scanning Transmission Electron Microscope (STEM) with Electron Energy Loss Spectroscopy (EELS). The aberration-corrected STEM/EELS analysis was done using a FEI Titan transmission electron microscopy at an accelerating voltage of 300 KV. The results are shown in Fig. 54 and Fig 55.

Figure 54 TEM picture of TaN/TaO/AlO/TaN stack. The sandwiched insulator stack is 7nm for this case.

Figure 55 STEM picture with EELS color mapping of N, O, Pt, Ta, Al, Ti, Si and W element for TaN/TaO/AlO/TaN stack. EELS mapping pixel size is 0.21 nm.

4.3 Volatile Conducting Bridge selector

In earlier chapter, we proposed and studied Tetra-layer Tunnel Barrier selector based on thin-film stack of $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{SiO}_2$ or $\text{Al}_2\text{O}_3/\text{TaN}_{1+x}$, which has improved the nonlinearity by 4-6 orders. However, for practical application purposes, the selectors currently under development may not be able to meet the stringent production requirements including high nonlinearity ($>10^5$), low leakage current ($< \text{nA}$ at below threshold voltage), and high current density requirements at above threshold voltage (about a few order of $10^6 \mu\text{A}/\text{cm}^2$). In this section, a brand new type of selectors is described, which can satisfy both requirements of high nonlinearity and a few tens of μA . This is a pioneering research work, there is very limited prior research which can be referenced. Our proposed device is based on the cation device. The working hypothesis for the operating principal of the new selector is illustrated in Fig. 56.

Figure 56 Volatile Conducting Bridge selector working hypothesis. a) Ag is ionized in the applied field and driven toward the negative electrode, where it is neutralized and forms a filament; b) when the filament is completed current flows through the device; c) below a critical field the neutralized Ag atoms diffuse away from the filament more rapidly than Ag ions are driven toward it and the filament dissolves.

As depicted in Fig. 56, a solid electrolyte with engineered cation ion material is sandwiched between the top and bottom electrodes. The solid electrolyte is an insulator material, which may be a porous, relatively low density dielectric materials such as SiO_2 and this electrolyte is doped with a high concentration of a mobile species such as Ag or Cu cation metal that is easily ionized and highly mobile in the solid electrolyte. For one device architecture example, the selector insulator is a 10-15 nm thick layer composed of 50% AgO_x and 50% SiO_2 . Co-deposition was used to form the AgO_x - SiO_2 selector insulator. In addition, one or both of the electrodes may include this mobile species. As shown in Fig. 56(a), when a bias is applied across this device, some of the mobile species are ionized and driven toward the negative electrode, where they are neutralized by electrons supplied by that electrode. A filament begins to form because the electric field is geometrically enhanced near the tip of any metallic protrusion; ions are preferentially driven toward the filament tip. When this filament

bridges the gap between the electrodes an electric current is allowed to flow (Fig. 56(b)). Although the neutralized atoms in the filament can diffuse away from it, as long as the electric field remains above a critical value, the rate at which ions are driven toward the filament exceeds the rate at which the neutralized atoms escape and the bridge is maintained. Below this critical field, diffusion of the filament's atoms causes it to rapidly dissolve (Fig. 56(c)). This Volatile Conducting Bridge (VCB) selector results in an IV characteristic that is nearly ideal for a selector. Fig. 57 and Fig. 58 show the characteristic DC IV plots.

Figure 57 Two current-voltage curves for a VCB device illustrating repeatable ON-OFF current ratio of 10^5

Figure 58 Current-voltage characteristic for a modified device with higher switching voltages and nonlinearity ($>10^5$) and it has symmetrical IV curve in linear scale plot (a) and log scale plot (b).

The potential of the volatile cation approach is illustrated by the current-voltage characteristics displayed in Fig. 57 and Fig 58. Fig. 57 shows volatile switching curves for a device that consists of a 15 nm thick layer of a mixture of silver and silicon oxides that is contacted at the top and bottom by titanium nitride (TiN) electrodes. The bottom electrode is only 30 nm in diameter and defines the effective area of the device, which is comparable to that envisioned for the first generation memristor products. The silver oxide provides the mobile silver ions needed to form a conducting bridge. As the voltage is ramped up from zero the device current is initially less than 10 pA. At a critical voltage of about 0.4 V, a conducting bridge is formed and the current increases by 5 orders of magnitude. This conductive state is maintained until the bias drops below about 0.2 V and the conductive bridge dissipates. Two cycles are shown to illustrate the reproducibility of this behavior. More than 1000 cycles have been demonstrated in similar devices without failure. This dependence of current on voltage is nearly ideal for a selector. The large contrast in the ‘ON’ and ‘OFF’ currents enables the use of very large crossbar arrays without untenable sneak currents. However, the threshold voltages of the device shown in Fig. 57 are somewhat lower than desired. The ideal ON and OFF threshold voltages are determined by factors such as the amplitude and variability of the switching voltage of the memristor with which the selector is paired. Typically, threshold voltages centered at about 1 V with a separation ~ 0.5 V are optimum. Therefore, we have endeavored to create devices with threshold voltages in this range; a recent success in increasing the threshold voltages is shown in Fig. 58. This device is similar to that of Fig. 57 but employs a switching layer comprised of a spin-on glass impregnated with a high density of silver nanoparticles. Note that the switching behavior of this device, as well as that of the device of Fig. 58, is bipolar and symmetric. This is a necessary feature of selectors paired with our bipolar memristors. Another important requirement is that this selector switch between conductive and resistive states fast enough to enable adequate data rates.

We have already demonstrated formation and dissipation of the conductive filaments of memristor devices in less than one microsecond, which is excellent

progress toward sub-100 nanosecond goal for the memory device application [122]. In order to test the VCB selector speed, we build the nano-crossbar device shown in Fig. 59.

Figure 59 SEM Cu 10nm/SiO₂ 6nm/Cu 10nm selector device with cross-section area of 30 x30 nm

With the nano-crossbar device sample fabricated as shown above, a dynamic experimental setup is utilized to observe fast switching dynamics as shown in Fig. 60 and Fig. 61, where a nano-crossbar selector is connected in series with a fast pulse generator (Agilent 81160A Pulse Function Arbitrary Noise Generator) and a 20 GHz bandwidth oscilloscope (LeCroy WaveMaster Oscilloscope). The fast scope monitors not only the transmitted voltage through the device but also the incident voltage from the pulse generator and the reflected voltage from the selector. A DC characterization testing was performed using Agilent B1500A Semiconductor Device Analyzer before the dynamic testing.

Figure 60 Schematic view of fast dynamic testing experimental setup, where a nano-crossbar selector is connected in series with a high speed pulse generator and an oscilloscope with 50 ohm impedance

Figure 61 Actual equipment view of the pulse generator with oscilloscope connected with the Cascade Microtech manual probe station for high speed dynamic testing

A customized LabVIEW software is used to control the testing and display the results. A main voltage pulse with 0.8 V voltage is generated by the pulse generator with a rise and fall time of 5 μ s to switch on the VCB selector device. A verification pulse with 0.1 V voltage is used to validate the selector OFF state after the rest time. The verification voltage is much lower than the switching threshold of the device, so it only provides the reading purpose. A second cycle of the switching and verification pulse is performed also to check the repeatability of the device. Fig. 62 shows the dynamic testing setup and the results.

Figure 62 Dynamic behavior of switching and recovery times of the VCB selector. The selector will be switched ON with a finite delay ($<5.5 \mu\text{s}$) at an applied voltage greater than a threshold voltage needed and it will be relaxed/tuned off to the OFF-state in $<15 \mu\text{s}$ once the applied external voltage is removed. The dynamic behavior confirms the volatile operation of the VCB device.

As we can see from Fig. 62, when the voltage larger than a threshold voltage is applied to a selector (0.8 V is applied in this case), the VCB selector is switched ON after a finite delay ($5.5 \mu\text{s}$ in this case). Once the applied voltage is removed after the switching pulse is done, the device can quickly return to a high resistance OFF state with a recovery time $<15 \mu\text{s}$ from the time interval between the fall edge of the switching pulse and rise edge of the verification pulse, confirming the volatile switching operation for the VCB device. The second pulse set (switch pulse and verification pulse) confirms the repeatability. A faster ON time is observed from the second cycle of operation, which could be resulted from the reason that the cation ions are still in excitation modes. Further detailed studies will be carried to explain the detailed mechanism.

With the development work of the VCB selector device, a highly nonlinear device will be switched ON and OFF during the Write, Erase or Read operation of the memristor cell when it is integrated with a memristor cell. As presented in earlier section, a VCB selector has been demonstrated for extremely high nonlinearity ($>10^6$) for very high-density 1S1R array. It provides desired low operation current ($<100 \mu\text{A}$) for the crossbar circuit to minimize the voltage drop and to maximize simultaneous device operations within the allowed maximum supply current. However for dynamic operations, the current VCB selector device is still quite limited by the operation speed,

especially the off time (the device relax time), which is expected to be <50 ns for the ideal memristor operation.

Very recently we developed an Ag/oxide-based threshold switching VCB device with attractive features such as record-high current-voltage nonlinearity ($\sim 10^{11}$), the steepest turn-on slope (less than 1 mV/decade), ultra-low OFF-state leakage current ($\sim 10^{-14}$ A), fast turn ON/OFF speeds (<75/250 ns), and good endurance ($>10^8$ cycles). Combined with a nonvolatile memristor, this selector should enable a 1 Mbit (e.g., 1000×1000) crossbar array with >100 ON/OFF current ratio. The results have just been submitted for publication. The results provide a critical step towards future computing and pave the way for a large-scale crossbar array using memristors. Further research and engineering tuning work is still needed before it goes in production.

4.4 Equal potential virtual isolation scheme

Earlier section describes the various research work done for selector devices in 1S1R architecture, which is to prevent the sneak path current issue by adding a nonlinear selector in series with each memristor that passes current when the full voltage is applied across a memory cell but sharply limits the current at half of the voltage bias. The voltage scheme mentioned here is known as “half-V addressing” scheme as we discussed earlier. Coupling selector with “half-V addressing” scheme, the sneak path current will be highly suspended if the selector device has high nonlinearity, which demands the selector to have all kinds of attributes as we discussed earlier. In this section, we are going to introduce another patented addressing scheme, named “Equal Potential Virtual Isolation scheme”, which can greatly reduce the sneak path current issue with less demand on stringent requirements for selector device performance.

The Equal Potential Virtual Isolation scheme utilizes Kirchhoff Current Law (KCL), which is equivalent to that deal with the current difference in the lumped element model or nodal analysis of electrical circuits. KCL states that at any node or a junction in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node. In this case, we would like to apply the KCL to virtually isolated those un-selected memristor cells in the crossbar network to reduce the background current. From KCL, the lamped current of the voltage node is zero. For the device inside the node, the current is a function of the voltage drop by the following equation:

$$I = \Delta V / R \quad (4.1)$$

where I is the current across the memristor, ΔV is the voltage difference across the memristor, and R is the resistance of the memristor.

Therefore, when the voltage difference, ΔV , is zero, the current through the memristor device is also zero from equation 4.1. Fig. 63 shows the concept of the equal potential virtual isolation for a single device.

Figure 63 Equal potential virtual isolation by Kirchhoff Current Law. a) When voltage difference applied between the two terminals of the device, there is a current flow through it by Ohm's law; b) & c) When the voltage difference is 0, no matter it is through both terminals grounded or applied equal potential, there is no current through the device

In the actual crossbar memory implementation, the voltage control circuit for Read or Write will isolate the target memristor by applying the equipotential principle described above. To do so, we will apply a voltage, such as a Read voltage, to drive a current to the column line that is coupled to the target memristor, which is the memory cell being read. At the same time, we will supply the equal potential to all the row lines except the row line for the targeted memristor to be read, which will be grounded. As such, the various amounts of current sneaked through the other memristors that are coupled to the column line will be virtually isolated eventually. The concept is depicted in the following figure.

Figure 64 Equal potential virtual isolation scheme for crossbar memory application a) Row and column voltage applied for the targeted memristor addressing; b) the equivalent circuit for the crossbar memory from the virtual isolation

As seen from Fig. 64, when we address Column 2 Row 2 memristor (C_2R_2), we apply the Read voltage V_p to C_2 top electrode for reading. However, sneak path current will be un-controlled and will occur everywhere from the surrounding memristors, especially the low resistance ON-state memristors. When we apply the same voltage to

However, there is a downside for the equal potential virtual isolation scheme. The main drawback is that the R_2 row line will experience very higher current, as depicted in Fig. 64 (b). Most of the times this may not be an issue since the reading voltage is very small, for example, 0.2 V. However, in order to mitigate the high row line ground current issue, there is an alternative comprised solution for the modified virtual isolation: we will add a high impedance resistor in series to the row lines. The high impedance resistor will be shunted by a low resistance switch (for example, a passing transistor) during the testing. The virtual isolation working theory is similar as above. However, due to the voltage divider effect between the resistor and sneak path memristor, there will be certain voltage difference along the column line. Therefore, we can only achieve partial isolation. However, the column line reading will still have better accuracy since the sneak path current along the line is reduced, which still increases the reading accuracy. And this partial virtual isolation scheme will work better with adding a selector device. Comparing to the previous schemes, the demand for the selector device is much reduced since the address scheme itself will reduce the majority of the sneak path current already.

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Chapter 5 Memristor Applications

Comparing to other competing emerging devices like PC-RAM and STT-RAM, memristors are newer devices for research and development. However, since its discovery, memristor has been regarded as the most promising nonvolatile memory technology due to its advantage of fast switching speed, good program ratio, high endurance, low operation voltage and current, fab friendly material and 3D stackable for high density memories [6] [7]. The below table summarizes a comparison among the mainstream memory technologies for both commercialized and emerging devices.

Table 4 Technology comparison between memristor, PCRAM, STTAM and commercially available technologies, modified from [13].

	Memristor	PCM	STTAM	SRAM	DRAM	Flash (NAND)	HDD
Reciprocal density (f^2)	≈ 4	4-16	20 - 60	140	6-12	1 - 4 ⁺	2/3
Energy per bit (pJ)	0.1-3	2-25	0.1-2.5	0.0005	0.005	0.00002	1-10x10 ⁹
Read time (ns)	<10	10-50	10-35	0.1-0.3	10	100000	5-8x10 ⁶
Write time (ns)	~10	50-500	10-90	0.1-0.3	10	100000	5-8x10 ⁶
Retention	years	years	years	as long as voltage applied	<< second	years	years
Endurance (cycles)	10 ¹²	10 ⁹	10 ¹⁵	>10 ¹⁶	>10 ¹⁶	10 ⁴	10 ⁴

Competing emerging devices

Commercialized technologies

Memristor-based devices have many unique analog properties to potentially build analog cross-point memory arrays for implied logic, neuromorphic computing, computing in memory and implied logic operations [8] [9] [10]. In the previous chapters, we have introduced and discussed many works done to tune the memristor for memory applications to increase endurance, nonlinearity, reduce the operation voltage and current, etc. There are many good review papers discussing the advantages and progress of memristor as nonvolatile memory. Therefore Chapter 5 will focus on the work we did in HP Labs to utilize its unique analog properties for the application beyond memory applications.

5.1 Hamming distance comparator accelerator

As the integrated circuit clock frequency is behind the increasing demand of the computation, the computer architecture revolution is searching for different solutions to continue application performance scaling [123]. One common approach is using multicore, which uses multiple simple cores that enable higher performance than superscalar processors by dividing tasks in parallelism [124]. Another approach is to use highly customized designs named accelerator at different levels within the system. The accelerator is a separate substructure that is architected using a different set of

special objectives than the base core processor, where these objectives are derived from the needs of a special class of applications. The accelerators can be integrated with the core, specialized cores, attached processors, or attached appliances via interconnect. Here we propose a highly specialized accelerator to do hamming distance based on memristor architecture.

The hamming distance is a widely used concept in information theory. For any pairs of strings or words of equal length, the hamming distance is defined as the total number of positions where the symbols or characters from the pairs are different from each other in the corresponding coordinate positions. In other words, the Hamming distance measures the minimum number of algebraic errors in information communication that could have transformed one string into the other. Below table shows some examples of the harming distance:

Table 5 Hamming distance examples for the string comparison

String 1	String 2	Hamming distance
10 11 10 11 0	10 00 10 01 1	4
TTGTTATC C GCA	TTGTTATC T GCA	1
Ja co b	Ja me s	3

The Hamming distance is very useful in many applications in modern technologies. For example, it was introduced to count the number of flipped bits in a fixed-length binary word for the signal quality as an indicator of estimate of error. Hamming weight analysis of bits has been widely applied in many disciplines including information theory, coding theory, and cryptography [125] [126] [127]. Hamming distance is also used in epidemiology systematics as a measure of genetic distance by counting number of nucleotide differences between two genetic sequences [128].

Strings or words can be converted into sequence code based on binary bits. The task of a Hamming distance comparator in a digital system can be practically reduced to counting the number of binary bit flips that differs from the corresponding digits of the sequence. Using two 8-bit-streams as an example, 01101001 and 10101000 have the Hamming distance of three, i.e., a flip in the first bit, second bit, and eighth bit. Implementing the comparator logic in hardware usually requires an array of 1-bit cells. Traditionally, the harming distance is calculated via digital circuit by XOR gates performing a bit-wise comparison of the incoming data bits and a corresponding decision logic. Full bit length comparator circuit can be faster but at the expense of a

large circuit area and more logic gates. Sequence processing with less logic gates will be more efficient in circuit area but needs more cycles. Since for digital circuit applications, the power consumption is proportion to the circuit capacitance and the number of signal transitions. The power consumption efficiency of traditional approach is low. This is exacerbated when the word or string comparison involves an analog input signal, which needs to be converted to digital first through analog-to-digital conversion. Here we propose a very simple and elegant architecture to do hamming distance calculation using accelerator based on unipolar switch memristors.

As we discussed in the earlier chapter, unlike bipolar switching, unipolar memristor switching refers to the switching of the memristor device depending on the applied voltage amplitude and current compliance only but not depending on the polarity of the applied voltage. As a result, the Set and Reset can happen at the same polarity of the applied voltage. Nonpolar switching is a special case of unipolar switching, which refers to the switching which can symmetrically occur at both positive and negative voltages. As we mentioned earlier, the hamming distance between two strings of equal length is the number of positions at which the corresponding symbols are different. Since strings can be translated into Boolean values, here we use Boolean value to illustrate the working theory (actually the proposed accelerator is able to perform the analog value comparison as well). Using the unipolar switching device, a diagonal Memristive Crossbar Array (MCA) can be constructed as below:

Figure 66 Hamming distance comparator accelerator. Unipolar memristors arranged in a diagonal crossbar architecture is adapted

For N bits string comparison ($A_n \dots A_2 A_1$ comparing to $B_n \dots B_2 B_1$) using harming distance accelerator, N number of unipolar memristors will be in a placement of a diagonal crossbar architecture as shown in Fig. 66. There will be three process steps for this accelerator operation:

Step 1: All unipolar memristors will be reset to Off state (high impedance state), for example, applying smaller voltage but high compliance current.

Step 2: The bits strings $A_n \dots A_2 A_1$ and $B_n \dots B_2 B_1$ will be input to the two sides of the diagonal matrix respectively according to the Boolean value, i.e., all the A_n and B_n input has a reference voltage V for “1” and 0 V for “0”. The voltage V will be equal or greater than unipolar memristor Set voltage. The voltage could be the small digital signal after a voltage level shifter to the desired value. Current compliance control will be applied also either in rows or columns current path.

During the voltage application, if bit A_n and bit B_n have the same value (both are either 1 or 0), the memristor will stay OFF because of the “equal potential” of the two terminals. However if bit A_n and bit B_n have different voltage potentials (1&0 or 0&0 combination), the unipolar memristor will switch and Set into low-resistance state.

Step 3: A small Read voltage will be subsequently applied to one side of the diagonal crossbar and another side will be grounded. The overall summed current from the matrix will be read. The summed current will represent the harming distance through a Trans-Impedance Amplifier (TIA) and Analog to Digital Converter (ADC) peripheral circuit.

Figure 67 Hamming distance computation example based on the unipolar switch memristor accelerator. a) Example of the case where are two bits different between the strings; b) Example of the case when the two strings are identical

Fig. 67 shows two examples of the string comparison based on the unipolar switch memristor accelerator. Fig. 67 a) shows an example of 011 being compared to 110. As we can see the Row1 Column1 and Row3 Column3 memristor have been Set into low resistance state from the switching. From the later current reading and

conversion, we can find that the distance is 2. Fig. 67 b) shows another case when the two strings are identical, therefore the summering current will be 0, which indicates the hamming distance between the two strings is 0. Through this simple and elegant circuit architecture based on memristor, several advantages can be achieved. The unipolar memristor based accelerator is a very simple structure to calculate the harming distance. It will be more energy efficient compared to the digital computations. The operation consumes less time since only three clock cycles are needed to finish the comparing operation.

For the circuit demonstration, a highly symmetrical nonpolar device with large ON/OFF conductance ratio is fabricated for the technical feasibility. The device area of an individual memristor was $5\ \mu\text{m} \times 5\ \mu\text{m}$. In an sputtering system (AJA international, Orion 8), around 20 nm TiO_2 layer was deposited on a 30 nm Pd/Au(50 nm)/Ta(3 nm)/ SiO_2 /Si substrate using a commercial TiO_2 target under a 7 mtorr of Ar (20 SCCM) and O_2 (5 SCCM) ambient. The Pd bottom electrode, Au and Ta layers were deposited by thermal evaporation system (CHA, SE-600). Finally, a 30 nm Pd top electrode and then a 50 nm Au were deposited by thermal evaporation.

Fig. 68 (a) shows an optical microscopic image of a 32×32 MCA and the inset of Fig. 68(a) schematically illustrates the device structure as mentioned earlier. Fig. 68 (b) shows Set and Reset switching operations which can be obtained with either positive or negative voltages (bottom electrode was grounded) with a good symmetry and reproducibility in both voltage and current. In addition, by optimizing the thickness and fabrication condition, electroforming process is not needed to precondition the device for the subsequent Set and Reset switching operations. The Set is done by using a quasi-DC voltage sweep with a current compliance while no current compliance is used in Reset. As shown in Fig. 68(b), the Set and Reset voltages exhibit a good symmetry, which is important for a hamming distance comparator because the voltage difference could be positive or negative depending on the amplitudes of the reference and input voltages. Fig. 68(b) also shows the device has ON/OFF conductance ratio of ~ 1000 at 0.2 V. The large ON/OFF conductance ratio will help to increase the Signal to Noise Ratio (SNR) by suspending the background off current and enable larger MCA size for longer string comparison. Fig. 68 (c) and (d) present the measured variances of operation voltages from cycle to cycle and from device to device, respectively. The maximum standard deviation is less than ~ 0.46 V. The uniform distributions of the Set and Reset threshold voltage demonstrated in fabricated devices determine the accuracy of hamming distance comparator.

Figure 68 Specially designed unipolar memristor and crossbar array for Hamming distance comparison. (a) Optical microscopic image of a 32x32 memristive crossbar array. The inset is a schematic illustration of the device stack structure; (b) semi-log plot of the I - V curve for switching; (c) cycle-to-cycle variability of a single device ; (d) device-to-device variability of 32 devices with lower maximum standard deviation value ≤ 0.46 .

Based on the unipolar switching device discussed above, a full size MCA (i.e., there is a corresponding memristor in every single row and column cross junction) is constructed for demonstration purpose as shown in Fig. 68(a), where only the diagonal memristors in the array are utilized during the testing. In principle, N isolated memristors are needed for an N -bit comparison. In that case, we can use diagonal MCA with N memristors instead of full size MCA ($N \times N$ memristors). And it is possible to arrange the N isolated memristors in single row or column also. However, the MCA design is more optimized for the layout routing and probe card design. Based on the MCA structure we built, Fig. 69 shows two examples of the string comparison using the more complicated analog values to more closely mimic a real application case (digital comparison with fixed voltage notation level will be a much easier case). The 32x32 MCA in Fig. 69 can perform a 32-bit comparison using its 32 diagonal unipolar

memristor devices. Figs. 69 (a) - (c) show case 1 with a Hamming distance being equal to 15. Fig. 69 (a) presents the actual voltages for the two strings to be compared; Fig. 69 (b) shows the voltages applied on each device normalized by the corresponding reference voltage, which can be used to easily determine whether a device will be switched or not. Fig. 69 (c) shows the pre-comparison validation (all devices are in HRS state, black squares) and the post comparison devices (red dots) with high currents for those devices being switched to their LRS states. In this case, 15 devices has been switched, meaning a Hamming distance of 15, which results in a measured total current summation of 7.968 mA. Figs. 69 (d) - (f) provide another example, i.e., case 2, with a hamming distance being equal to 13. In this example, 13 devices have been switched with a total current summation of 6.94 mA. This corresponds to a hamming distance of 13.

Figure 69 Two Hamming distance comparison cases based on analog input values. (a) – (c), case 1 with hamming distance = 15. (a) The actual voltages for the two strings to be compared; (b) the normalized voltage differences by setting reference voltages to be 0 for each device; (c) pre-comparison validation (all devices are in the HRS state) and current readings of post-comparison devices, some of which exhibit the LRS state with a high current level. In this case, 15 devices have been switched, corresponding to a hamming distance of 15. (d) – (f), case 2 with a hamming distance equal to 13. (a) The actual voltages for the two strings to be compared; (b) the normalized voltage differences by setting reference voltages to be 0 for each device; (c) pre-comparison validation (all devices are in HRS state) and the current reads of post- comparison devices, some of which exhibit the LRS state with a high current level. In this case, 13 devices have been switched, corresponding to a hamming distance of 13.

Fig. 70 shows more of such measurements, which can form function of the total current vs. number of actual switched devices. The number of the switched device and the total measured current exhibit a fairly linear relationship because the current contribution from un-switched devices is negligible due to a very large ON/OFF conductance ratio of the memristors. For example, when the measured total current is 7.968 mA, the estimated number of switched unipolar memristor devices from the linear fit is 15.355, which agrees well with the actual Hamming distance of 15. Similarly, when the measured total current is 6.94 mA, the estimated number of switched unipolar memristor devices using the linear fit is 13.311, which, again, is very close to the actual hamming distance of 13. The Hamming distance comparator demonstrates a high accuracy even in the case of analog value comparison.

Figure 70 Total current vs. number of switched devices in the memristor crossbar array. The resultant plot yields a linear fit of $y = 2.72 * 10^{-4}x + 5.01 * 10^{-4}$

In this hamming distance work, we designed and fabricated a new unipolar switching device with some unique switching characteristics, based on which we designed and demonstrated a novel computation circuit scheme, namely, an efficient Hamming distance comparator. It exploits the unipolar switching with a narrowly distributed threshold switching voltage, well-controlled bi-stable states and large ON/OFF conductance ratio. The circuit does not require digital addition or comparison and is capable of determining hamming distance as well as code comparison based on analog values. The threshold switching voltage can be engineered to a desired value with a built-in margin of tolerance for the noise. The comparator core circuit with a

simple and non-digital circuit design features small footprint based on backend of line process. A fast speed and low energy can be achieved since only three clock cycles are needed to finish the core comparing operation. The circuit can potentially achieve higher speed and energy efficiency on real-world signal processing because it does not need ADC support and only three clock cycles are needed to finish the core comparing operation. Last but not least, it can also store the computation result non-volatily in the circuit without the need of additional memory circuits.

5.2 Dot Product Engine

5.2.1 Motivation and introduction

A variety of processing units based on traditional CMOS circuits have been developed to meet different applications in the past forty years since the introduction of Intel 4004. Among them, Central Processing Units (CPUs) and Advanced Processing Units (APUs) have high speed but low power efficiency while recent Advanced RISC Machine (ARM) and grid-processors have high power efficiency but slow speed. However, there are increasing needs for high demanding systems, for example, real-time Intelligence, Surveillance and Reconnaissance (ISR) systems, which require both high power efficiency and high speed for information processing. The increasing mobile device applications and Internet of Things (IoT) have same demoing also for the power and speed. Current solutions are combining traditional CPUs with Graphics Processing Units (GPUs) and using GPUs to tackle computationally intensive problems, including pattern recognition, online data processing, classification, optimization, inference, learning/training and other applications using computations such as the Discrete Fourier transform (DFT). GPUs are well-suited to address data parallel computations, originally for image rendering and processing problems. In fact, many other algorithms can also be accelerated by data parallel processing, from general signal processing or physics simulation to computational finance and computational biology. GPUs with many cores have the advantage of being fairly fast, but at the cost of consuming large amounts of power.

In order to improve computational power efficiency and speed simultaneously, an unconventional solution based on emerging technologies is needed. Many computation-intensive tasks are formulated in vector or matrix format to speed up computation through parallel processing. However, actual performance can be limited in digital implementations, such as CPUs or GPUs, because of a severe memory bottleneck in the system. This leads to a significant increase of the cache hit ratio and the use of kernel registers as virtual cache outweighs the drop in computational parallelism. Some algorithms that directly depend on vector-matrix operations are listed in Table 6.

Table 6 List of some algorithms directly depending on vector-matrix operations

Algorithm	Description	Vector-matrix multiplication dependency
Discrete Fourier transform (DFT)	Frequency↔time domain linear transformation, commonly used in many applications.	Major operation is $X_k = \sum_{n=0}^{N-1} x_n \cdot e^{-i2\pi kn/N}$
JPEG	Image compression	Lossy data compression, converting to frequency domain with FFT, then ignoring some least significant bits.
A*best algorithm	Path finding	Updating open set data: If there are different weights for movement between locations, then it requires massive vector-matrix multiplications.
Perceptron	Pattern classification	Taking weighted summation of input signals as the input for activation function.
Schönhage-Strassen algorithm	An asymptotically fast method for multiplication of large integer numbers. The run-time is $O(N \log(N) \log(\log(N)))$.	Using Fast Fourier Transforms (FFT) in rings

As we can see from Table 6, vector-matrix operations are utilized in data compression, digital data processing and machine learning, while they tend not to be the most important operations for sorting, encryption, searching or optimization algorithms. However, as there are large overlaps between machine learning and other areas, we can realize many algorithms via the help of machine learning models. For instance, the Hopfield model used in machine learning can be utilized to solve general optimization problems, such as the population annealing algorithm [129]. In addition, vector-matrix operations are the main computation in neural networks, which can approximate a general class of algorithms. Consequently, a very large number of important algorithms either directly rely on vector-matrix multiplication, e.g. Fast Fourier Transforms (FFT), or may be efficiently approximated by vector-matrix multiplication based methods, e.g. Metropolis algorithm.

Here we will introduce and demonstrate an unconventional hybrid computation engine, where analog MCAs are used as Dot Product Engine (DPE). We envision that such DPEs will form the basis of accelerators on System On Chip (SOC) multicore processors to dramatically speed up matrix and vector operations with orders of magnitude improvement in power efficiency, and thus benefit many computing algorithms. It can be used in a Threshold Logic Gate (TLG) to perform the matrix product and to compare the sum with a threshold.

The vector and matrix computations are executed through MCA in Fig. 71 : applying a set of input voltages $\mathbf{V}^I$ along the rows of an $\mathbf{N} \times \mathbf{M}$ array and collecting the currents through the columns by measuring the output voltage $\mathbf{V}^O$. On each column, every input voltage is weighted by the corresponding memristance ($1/G_{i,j}$) and the weighted summation is reflected at the output voltage. Thus, the relation between the input and output voltages can be represented in a vector matrix multiplication form: $\mathbf{V}^O$

$= -\mathbf{V}^I \mathbf{G} \mathbf{R}_s$ (negative feedback of op-amp), where $\mathbf{G}$ is an $\mathbf{N} \times \mathbf{M}$ matrix determined by the conductance of the Memristor crossbar array.

Figure 71 Basic architecture of a Memristor array based analog DPE. a) Working principle for dot productions summation; b) Basic circuit for the DPE architecture using linear memristor

MCA is naturally implemented in matrices form, leading to more than many order of magnitudes performance improvement compared to GPU or other accelerators due to the highly parallel computing model and efficient use of electrical signals and physics laws in the hardware implementation. The low operating energy (<pJ) of memristors further reduces the power consumption. For the speed and power efficiency benchmarking, we compared DPE with a state-of-the-art ASIC [130] as an example [131]. Included in our simulation for the DPE is the peripheral circuitry constituted by the DACs, TIAs, and ADCs.

Figure 72 Schematic representation of the of the DPE setup used for performance simulation

Each channel is assumed to be 8-bit, operating at 10 MHz and consume 100 μ W [130]. The peripheral circuit consumes >90% of the total power and >95% of the total chip area. The major speed bottleneck also comes from the DAC and ADC. This result calls for more efficient and compact DAC and ADC design for low speed parallel signal processing. However, the DPE can still achieve the same speed-efficiency product at a crossbar size of 32×32 , and becomes more than 1,000 $\times$ higher (when ASIC is in “maximum speed mode”), or more than 10,000 $\times$ (when ASIC is in “maximum energy efficiency mode”), when crossbar size is scaled up to 512×512 [131].

Table 7 MCA DPE performance and peripheral circuit estimations

Crossbar size(N×N)	32	64	128	256	512
Wire series R (Ω)	10	10	10	10	2.5
Input range (V)	0 – 0.5	0 – 0.25	0 – 0.125	0 – 0.125	0 – 0.125
Output range (uA)	40 – 160	40 – 160	40 – 160	110 – 300	200 – 650
Avg. Power (mW)	1	0.87	0.30	0.47	2.1
Peripheral circuit estimations for each channel (DAC+TIA+ADC)					
Power (uW)	100	Freq. (Hz)	10M	Bits	8

Fig. 73 shows the comparison between DPE and various available computing technology comparison in high level for the computation speed and power efficiency.

Figure 73 Speed and power efficiency chart for Memristor accelerators, CPUs, APUs, GPUs, ARM and grid-processors in terms of Giga Floating Point Operations Per Second (GFLOPS) [131].

As we can see from Fig. 73, the Memristor crossbar DPE can thus significantly outperform a GPU, having about two orders of magnitude improvement in power efficiency. A Memristor DPE occupies a similar area as a single GPU core, but it takes thousands of GPU cores to have a comparable speed to a Memristor DPE for vector-matrix multiplication. The main trade-off is bit accuracy, for which a GPU outperforms. Therefore, the Memristor DPE is suitable for modern applications in which substantial portions of the computations can tolerate lower accuracy but require high speed and power efficiency. This includes image rendering, signal processing, augmented reality, data mining, robotics, speech recognition, and others. The example of Memristor crossbars in processing vector (N)-matrix ($N \times N$) multiplication operations is shown in Fig. 71. Optional ADC/DAC convertors may be used in the input and/or output of the DPE. Memristor based high efficiency ADC/DAC convertors have recently been demonstrated, which may also be integrated within Memristor-enabled high performance computation systems.

5.2.2 Memristor integration for DPE

As we mentioned earlier, there are world-wide efforts and progress on memristors recently and these efforts have focused on developing devices for non-volatile memories [13]. Memory applications are much more demanding on device performance than the proposed DPE, mainly arising from the ultra-high density and very fast programming speed requirements for memory applications. Accordingly,

there are two major challenges facing memristor memory, i.e., variability and nonlinearity. Device variability has been greatly improved in the last few years by adopting better switching materials (such as TaO_x and HfO_x) and fabrication processes [23]. However, due to high speed and high density requirements, memory applications cannot afford sophisticated feedback circuits to precisely control the cell switching to a target value because of the high operation-time and chip-area overheads associated with feedback circuits. Rather, memory applications rely on extremely low device variability. However, DPE applications do not need a cell density as high as memory and do not require frequent switching for reprogramming the cells compared to memory. Therefore, larger area circuits can be readily adopted in DPE to switch cells to target values even in cases where the device variability would be too high for memory applications. The majority of the DPE operations involves applying small voltages as inputs on the rows of an array and measuring the output currents or voltages on the columns. The applied voltages remain lower than the effective switching threshold voltage of the Memristors, and thus, do not induce any noticeable resistance changes in the Memristors. This operation is essentially the memristor reading operation, which is usually highly repeatable with indefinite endurance cycles and very low error rates or imprecision. The repeatability of memristor reading operation is demonstrated already in our lab experiments, where memristor remains fairly stable resistance values after being read for a billion times at low voltage. This is true for both high resistance and low resistance states. Therefore, the DPE functions can be performed by MCA with high repeatability, high speed and low energy, just as the reading operations of memristors. As we can see that DPE significantly relaxes the requirements on variability and non-linearity. Therefore, the DPE study can now piggyback on the great efforts in memory development at HP Labs.

In HP Labs, we built a test chip with integration of MCA with transistor to form 1T1R for prove of concept of DPE. The advantage of having a transistor in series is to have full switching control over the memristor device during programming and the ability to activate the whole array during the computation. This work presents the first integration of memristors on CMOS transistors for DPE through a Back End Of Line (BEOL) process at Labs. The CMOS transistor chip was designed then fabricated using a $2.6\ \mu\text{m}$ technology in the Front End Of Line (FEOL) process. The reason for choosing μm size technology is because current DPE testing architecture design uses a bond-pad pitch size of $60\ \mu\text{m}$ to drive the arrays. The μm -size technology platform provides a quick turn-over time, low-cost evaluation and reasonable performance for the demonstration. In addition, the μm -size technology can supply the required adequate current and operation voltage range for the DPE array operation comparing to the modern deep sub-micron technologies. Fig. 74 depicts the example layout design for an array of 4×4 NMOS transistors integrated with memristors DPE design. Therefore multiple matrix design for the test chip including 4×4 , 8×8 , 16×16 , 32×32 , 64×64 and 64×128 split design. 4×4 layout is shown for the simplification of the structure for the illustration purpose.

Figure 74 Mask layout for an array of 4x4 NMOS transistors integrated with memristors

Table 8 below shows the key design parameters for the matrix design. For the DOE purpose, the associated periphery circuit like voltage source, amplifier, ADC etc. are not integrated on-chip. Therefore the test DPE matrix is bond-pad size driven. The cell size is not constrained by the die size, which gives us more design margin for Design For Manufacturability (DFM) to have better topography for the memristor integration, which we will talk about in the later section.

Table 8 DPE design parameters for the cell and memristor

Design parameter	Size
Cell size	X=26.9 μm Y=28.2 μm
Memristor size	3 μm x 3 μm
Transistor size (W/L)	71.1 μm / 2.8 μm
Formation of MIM	Metal 1-to-Metal 2

An individual TaO_x memristor device is integrated with the built NMOS transistor by a 4-mask process subsequently. The process flow is very similar to the process flow we have discussed in Chapter 2. In this process, the memristor BE is formed by a first mask, a trench etch, e-beam evaporation of 10nm of Ta and 80nm of

Pt and liftoff processes. This follows by a reactive sputtering process to deposit 5nm of TaO_x as a memristor switching material. A bit-area mask and a reactive ion etching process are used for defining individual area where a memristor is formed. A memristor device is formed by a combination of a bit mask and a TE mask. In addition, an ILD between BE and TE is formed by an e-beam evaporation of 55 nm of Al₂O₃ prior to forming TE. A cross section view of the designed processing for BEOL memristor fabrication on top of the NMOS transistors is shown in Fig. 75.

Figure 75 A cross section view of the designed processing for BEOL memristor fabrication on top of the NMOS transistors with a 4-mask process

There are challenges to integrate a memristor device on the NMOS transistors in this case. Due to the foundry resources and capabilities, a CMP process was not performed. Additionally, this CMP process has a high cost of ownership, which increases with operation and maintenance costs, and adds up a time delay for BEOL processing. And these transistors were designed and fabricated for printing products and they were microscale with a special geometry and topography. The surface of the conductor where BE is formed has tens of nanometer surface roughness, which may not be suitable for high performance memristor devices. Physical inspection was the basis to investigate the fabricated devices by using optical microscopy, Atomic Force Microscopy (AFM) and STM. A non-flat surface resulted from the FEOL process as shown in Fig. 76 for 1T1M cell with a series configuration of a transistor and a memristor.

Figure 76 AFM image to show the non-flat surface resulted from the FEOL of the transistor built for DPE

As one can see from Fig. 76, this non-ideal topography of the CMOS transistor die makes it very challenging for further BEOL processing. A functional memristor needs to be fabricated on the top area making contact with the metal via holes. Since memristor standard fabrication procedures at Labs are not compatible with this topography, a completely new fabrication method for BEOL needs further investigation and completion. First, we have carefully tuned the FEOL layout with a DFM tuning to fit DPE requirements. By design around, the memristor is located at a flat region which is maximally allowed by physical constraint. However, due to design rule limitations we still have a topography challenge, which was addressed by a BEOL process implemented on top of the described non-flat surface. We solved this challenge by developing a double exposure photolithography method for the first time at Labs. While standard photolithography method failed in non-flat surfaces, this innovative process facilitates a well-defined disk patterned memristor bit-cell. By the introduction of BEOL memristor into FEOL transistor, the 1T1R device is successfully integrated for DPE application as shown below for an example:

Figure 77 Finished TaO_x memristor with transistor array (4X4 as example here) for integrated 1T1R for DPE application

5.2.3 Electrical testing and results discussion

Currently, the main focus of implementing the integration process is to demonstrate the performance improvement of a hardware accelerator by doing vector-matrix analog multiplication with crossbar 1T1M arrays. Additional to this process demonstration, characterization test have been conducted on the individual device or 1T1R cell from Parametric Test Structure (PTS) as well the whole DPE matrix itself. The more challenging but less frequent DPE operation is the mapping of a matrix onto the memristor crossbar, which requires precision programming (writing) resistance values into the memristors of the crossbar array with a sufficiently high bit precision. There are a number of feedback algorithms for improving programming accuracy. A simple example is a “write then verify” algorithm. In this case, pulses are applied until the device reaches a desired resistance level, such as a minimum resistance during OFF-switching and a maximum resistance during ON-switching. Improved distributions are seen when any programming overshoot is compensated by then utilizing pulses of the opposite polarity, in this way setting a target resistance and error tolerance. These feedback approaches can lead to nearly arbitrarily high state accuracy, with the cost of

increased programming time. However, programming time may not be a primary concern since it is much less frequent than the dot-product calculations. The setup shown in Fig. 78 is used to perform the characterization test developed by our test engineer. It consists of a Field Programmable Gate Array (FPGA) with reconfigurable digital and analog inputs and outputs in combination with a custom-made printed circuit board capable of performing the Write and Read operations required for the feedback scheme. The range of operation during Write is ± 10 V, with minimum pulse width of $2 \mu\text{s}$. The Read operation consists of a voltage of 0.2 V with varying duration, which depends on the resistance value to be measured by the auto-gaining TIA. A smaller PCB located near the memristor TE probe is used as the compliance by setting a resistor in series with the memristor. The memristor BE is connected to two switches configured by the FPGA to either the Read or Write operation. All the logic and control is implemented in the FPGA and monitored by a computer.

Figure 78 Schematic representation of the test-bed for memristor programming for DEP with state feedback scheme

Through the single memristor device on PTS track from the test chip, we have demonstrated before that the device programming can be much better controlled by feedback circuits, and we propose to use such modes of operation in the DPE. The goal is to achieve high bit precision and repeatability in the programming of Memristor resistance levels. Fig. 79 shows an example of successfully programmed TaO_x memristor cell based on the process introduced earlier with 5-bits resolution (32 levels) with the feedback control scheme.

Figure 79 Programmed TaO_x memristor cell to 32 levels (2 kΩ-2 MΩ range) to a 1% tolerance. Measurement setup Signal-to-Noise Ratio is poor for high resistances, and programming pulses are limited to 2 μs minimum.

As we can see from Fig. 79, the ability to attain a high number of bits depends broadly on the magnitude of the resistance swing achievable in the memristors (the “OFF/ON ratio”) and the capability of attaining distinct and sharply distributed resistance levels during the programming operation. To achieve the high resolution, memristor materials engineering and development to maximize the possible resistance swing is needed. As the second approach for accurate bit precision during programming, we utilize current compliance with integrated transistors. The added transistors add an area cost to the implementation, but can allow much higher bit precision, in addition to ultimately allowing for much larger array sizes (e.g., $>256 \times 256$) to be achievable, since unselected bits can be turned OFF with this transistor. By simply using a current compliance imposed by a common semiconductor parameter analyzer, we have already achieved 64 resistance levels from our TaO_x memristors. With some device optimization to enlarge the resistance ratio and using integrated transistors with lower parasitic capacitance and resistance, more resistance levels, and thus, better bit precision is expected. Additionally, we expect a negligible energy cost during the DPE operation if “normally ON” depletion mode transistors are utilized. The PTS track on the test chip comes with the single transistor and 1T1R cell structure. Fig.

80 and Fig. 81 show the single transistor and 1T1R current-voltage characterization results, respectively.

Figure 80 Characteristic IV curves of one of the transistors from the FEOL process measured for different gate voltages. Tuning of the compliance current (maximum current allowed to flow through the memristor) can be achieved by using different gate voltages. This is essential for controlling the switching of the memristor for accessing multiple levels of conductance: a crucial step in programming the DPE arrays.

Figure 81 Five cycles of memristor switching IV curves of a 1T1M single cell demonstrating the successful implementation of the BEOL process

In a test for a discrete memristor device, the sensing current is the device current since there is no parallel resistance connected to the device. However, in crossbar arrays, naturally there is always parallel resistance coming from unselected devices, so the sensing current will not equal the selected device current because of the sneak path current. By implementing 1T1R, for the crossbar array with a transistor at each cross point, each cell is very resistive when the transistor is in its OFF state. Therefore, the

issue can be mitigated. To test the actual crossbar array DPE results, a test-board to provide Multiple Input Multiple Output (MIMO) accessibility for memristor crossbar arrays is developed to first demonstrate the dot-product computation up to 32x32 and bit-accuracy up to 5-bits. Fig. 82 and Fig. 83 show the high level customized board testing architecture and an on-chip cell characterization testing, respectively.

Figure 82 DPE board testing. Complete Input / Output chain involving four different electronic printed circuit boards. Instructions originate from a Workstation CPU.

Figure 83 On-chip cell characterization testing from DPE 4X4 matrix

At this moment, the DPE Read and Write testing activity is still undergoing. We just got the preliminary positive results from the DPE matrix reading and programming for 32X32 matrix. The results will be shared in future publications. Along the demonstration of DPE, more products can emerge and benefit by implementing this technology for other applications such as mobile device, IoT and machine learning.

5.3 Neuromorphic computing

The neuromorphic computing (also known as spike-timing-based computation) inspired by the working mechanism of human brains effectively reduces the data communication cost and consequently, achieves very high computation efficiency. Hardware implementation of neuromorphic computing becomes more important as a new computing paradigm beyond the von Neumann digital architecture system. Conventional neuromorphic computing implemented has often been developed by artificial neural network in software or in digital circuits, which has no or loose connections to neuroscience [132] [133] [134] [135]. For example, the IBM research team has performed a cortical simulation at the complexity of the cat brain for advanced

neuromorphic computing systems on Blue Gene supercomputer [136] [137]. However, those conventional approaches are with limited success partially because these devices do not bear much resemblance to their bio-counterparts and are incapable of a direct emulation. Recently the two-terminal memristor devices that show electrically-triggered dynamically nonlinear resistive switching phenomenon have been proposed as artificial synapse device to directly emulate the biophysics and temporal dynamics of real synapses for neuromorphic computing [10] [138] [139] [140] [141]. The new memristive architecture could benefit applications ranging from pattern recognition, perception, to motor control [142] [143] [131].

Although the exact details of how synapses and neurons work are still controversial, the change of the connection strength of biological synapse is believed to be the fundamental reason for learning. Among all the important aspects, Spike-timing dependent Plasticity (STPD) is an important biological process of biological synapses to adjust the strength of connections between neurons for correlation based Hebbian Learning theory, which relies on relative spike timings of pre- and post-synaptic neurons has been discovered in several biological systems [144] [145]. This critical feature has been demonstrated on various memristor devices for neuromorphic computing [146] [147]. Except the obvious advantages of nanoscale size, low power and analog property, another key aspect that memristor has attracted so much interest neuromorphic computing is because there is close analogy between the biological neural synapse and the artificial oxide synaptic device. As we know that the biological synapse changes its conductance by activating and deactivating ion channels between the membrane and the synaptic junction when there is action potential arrived from pre-synaptic and post-synaptic neurons coherently. On the other hand, the memristor synapse changes its resistance by generation and migration of the oxygen vacancies when the programming voltage pulse that is larger than the threshold is applied [148]. In that sense, the memristor synaptic device works in a similar mechanism to ion diffusion modulation, where the memristance is essentially equivalent to synaptic weight. Both of them have internal complex dynamics during the switching events, which are crucial to enable their functions in processing, storing and transmitting information [141]. Fig. 84 shows the analogy and comparison of the biological synapse and memristor synaptic device.

Figure 84 A comparison and analogy between the biological synapse and the memristor synaptic device. a) A biological synapse is where a pre-synaptic neuron connects with a post-synaptic neuron coherently. In the stimulation event, the pre-synaptic neuron sends an action potential travelling through one of its axons to the synapse. The cumulative effect of pre-synaptic action potentials will generate a postsynaptic action potential at the membrane of the post-synaptic neuron. The biological synapse changes its conductance by activating/deactivating ion channels (Ca^{2+} or Na^+) between the membrane and the synaptic junction when the action potential arrives from pre-synaptic and post-synaptic neurons coherently; b) The memristor synaptic device changes its resistance by modulation of the oxygen vacancies or cation ions when the applied device voltage is larger than the threshold voltage needed; c) Membrane voltage action potential with timing: pre-post spiking $\Rightarrow$ promote Ca^{2+} influx through opening of N-methyl-D-aspartate receptors $\Rightarrow$ LTP (long term potentiation); while post-pre spiking $\Rightarrow$ low level sustained Ca^{2+} rise by opening Voltage-dependent calcium channels $\Rightarrow$ LTD (long term depression) (adapted from [144]); d) Memristor synaptic device emulations (adapted from [141])

The prior works may be able to perform certain STPD emulation function. The synaptic weight will increase if the postsynaptic neuron spikes right after the presynaptic neuron, which is consistent with the Hebbian postulate summarized as “cells that fire together wire together”. However, those memristors switch only when the two spikes overlap with each other to essentially increase the amplitude of the pulse, which is still quite different from the real STDP mechanism. To mimic a better dynamic STPD behavior, we introduced a cation-diffusion based device for memristor, which is leveraged from the VCB selector device. The added cation-diffusion part has two advantages: 1) it will modulate the switching time with dynamics; 2) it will bring highly

nonlinear current-voltage characteristic to enable the operations of a large array by mitigating the sneak path current and half-selected issues as a selector. As a result, the new memristor system will enable a bio-realistic instead of a phenomenological emulation to bio-synapses [141]. The cation-diffusion based device materials have multiple phases consisting fast diffusive ions doped in dielectric materials with large bandgap through co-sputtering Ag with Si or SiO₂ in the presence of O₂, N₂ and Ar gas mixture. Fig. 85 shows the device structure and electrical characteristics.

Figure 85 Ag based cation-diffusion based device. a) and b) Schematic of the device in a crossbar configuration. The inset b) shows the SEM of the corresponding device; c) IV characteristics of Ag:SiO_xN_y; d) Dynamic testing results: Delay and relaxation characteristics of the device showing variation of current (blue) with applied voltage (red) pulse. A read voltage of 0.1 V is used to study relaxation current.

Based on the modified structure and mate device, we emulate the biological synapse in a more straightforward and controllable approach to equip memristor with the highly desired dynamics for neuromorphic computing. Besides the memristor synaptic device work, we have performed preliminary neuromorphic computing research, which was emulated by the cross-point oxide synaptic device array and heavily leveraged from DPE project as discussed in Chapter 4 earlier [131]. All the neuromorphic computing researches introduced here are still in early phases and on-going. More results are to be published in future publications.

Chapter 6 Conclusion

6.1 Conclusion

In this report, the 4th fundamental device, the memristor, has been studied for several key aspects: fundamental material engineering, device modeling, selector device, and its unique applications. Some research gaps have been addressed in the field of memristor material tuning, practical device modeling and high performance selector study for the memory application towards the goal of future mass production. Several unique applications beyond memory application have been proposed and explored as well. Below is the summary for each chapter and areas:

In Chapter 1, a systematic survey and study was conducted that links the basic theory to the materialized device. First, the memristor theory was explored on a fundamental level, from the charge-flux relationship based on Maxwell's equation to the axiomatic definition of memristor. The memristor theory has deep roots in the modern electromagnetic theory from its theoretical concept and finally materialized with intention by HP Labs team in 2008. The memristor was constructed using TiO_2 followed the memristor theory Chua has predicted thirty five years ago. Finally, memristor switching idiosyncrasy and its basic testing methodology was introduced.

In Chapter 2, the memristor architecture and typical lab device fabrication process were introduced. Subsequently, the top electrode material impact based memristors with an identical TaO_x switching oxide layer and bottom electrode stack was studied. We found that the virgin resistance, electroforming and switching performance depend heavily on the chemical property of the top electrode materials. In addition, the electrical properties of metal oxides formed with the top electrodes also contributed to the overall memristor performance, including the nonlinearity of the current – voltage relationship. These results provided insights into the understanding of memristor behavior as well as approaches for device property engineering. In the subsequent section, more material engineering for the device performance improvement was conducted for the oxide choice, non-linearity and interface material. Through material engineering, the device performance was greatly improved. Finally thorough material characterizations on the switching films and control samples was performed to confirm that the AlN layer rather than other impurity materials, such as oxides, unintentionally formed in the ALD process, was responsible for the observed switching behavior. The demonstration of ionic switching behavior in nitrides led to interesting material composition for the resistance switches devices from current CMOS process.

In Chapter 3, we began with the background introduction for the earlier modeling work including linear drift and nonlinear drift models (mainly on TiO_x memristor system since it is studied first). Those models are considered as “toy” model since they are only able to show the behavior IV curve, but are not good enough to show the transient switch or other characteristic studies. With more extensive research, now we understood that the memristor conductance was mainly contributed by the

filament elements, which was the dynamics of the resistor and the gap conductance. In the latest research references, it was already known that the various physical parameters such as electric field, temperature, vacancy density and geometric parameters such as filament size can influence the switching properties of memristors. The two state variable model we developed for memristors combined axial drift of charged vacancies in an applied electric field for bipolar switching and radial vacancy motion caused by thermophoresis and diffusion for unipolar switching. The model can be used to show the dynamics of memristors and illustrate their internal physical behaviors. In our model, we focused on the most dominant physical parameters: electric field and temperature, and we derived the complete set of equations that can be used to describe our model. We modeled the switching layer of a memristor by considering both the filament motion and the remaining conduction. Typically the filament component can be viewed as metallic, according to the experimental results. While the conduction mechanism of the gap region is still under investigation, we modeled the gap mechanism based on the experimental observation and detailed derivations. This proved to be consistent with real data. Typical experimental and modeling results were obtained and compared, which showed excellent consistency, in both static IV curve and dynamic switching. The error from simulation results is small compared to the experimental data. The main error was caused mainly by the potential capacitance inside our measurement system, including the memristor, which contributed to the OFF switching time delay. Also the fluctuations of temperature and the real 3D movement of ions/vacancies can cause the differences between our modeling results and real experimental data. The two state variables provided a clear and accurate way to model the real memristors, and the dynamical behaviors of the state variables leading to deeper understanding of the real devices. The implementation of the two-state-variable memristor model will provide accurate compact model for circuit simulation, however one of the limitations of the current model was that it is accurate and suitable only for low voltage and low speed application. This could be attributed to the gap modulation portion we modeled. Further improvement on this work can be done for the high voltage and high speed dynamic operation.

In Chapter 4, we focused on another half story of the memristor memory application – the selector device. As we know that selector technology has been under development for early generations of memristor products, which will employ crossbar arrays consisting of about 128×128 or bigger memory cells. However, there are limits to how much further the non-linearity of various technology can be improved. It may not be scalable to the much larger arrays envisioned for future high-density product generations. In this chapter, we began with the background introduction, followed by the $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{SiO}_2$ or $\text{Al}_2\text{O}_3/\text{TaN}_{1+x}$ Tetra-layer Tunnel Barrier selector continued research work, which increased four to six nonlinear orders as compared to the previous $\text{TaN}_{1+x}/\text{Ta}_2\text{O}_5/\text{TaN}_{1+x}$ Tri-layer Tunnel Barrier selector with same thin-film thickness. The tunnel barriers are promising because of their high durability and intrinsic speed, however the main drawback is the limited nonlinearity and low current density. Therefore, after the crested barrier selector, we described a new cation based selector,

the VCB technology, aimed at providing the extremely large selectivity needed for future generations of high density non-volatile memory. It will give us a distinct advantage in creating future high-density, low-cost non-volatile memory due to its extreme high nonlinearity and reasonable current density. We actively explored a range of solid electrolytes, mobile ion species, and device geometries to improve the switching speed of these selectors while optimizing their threshold voltages. In addition to electrical characterization of prototype devices, this optimization was guided by a suite of nanoscale material characterization experiments. The VCB selector may enable the final production of memristors for large crossbar applications. The potential for using this innovative device was also to reduce the variability of the memristors' resistive states by regulating their switching processes, thereby reducing bit error rates. Finally, we introduced a patented equal potential virtual isolation scheme for crossbar memory application, which mitigated the sneak path current to dramatically increase the reading accuracy. Applying equal potential virtual isolation scheme will achieve a good isolation in large crossbar applications without using any selector or dramatically reducing the requirements for the selector device.

In Chapter 5, we first talked about a novel hamming distance computation accelerator based on the unipolar memristor. This was a good example that a high efficient and low power circuit can be achieved with the novel memristor device. It will generate many interesting application in the security, signal processing, and so on for wearable device, IoT etc. To test the technical feasibility, we developed and demonstrated a specially tuned unipolar switch device with good symmetrical switching behavior, state ON resistance and large ON/OFF resistance ratio. In the second part, we developed the DPE as an accelerator for approximated vector-matrix multiplications. Comparing to the conventional CPU, GPU, etc., the DPE can have at least three orders of better speed-energy efficiency product using a 512 x 512 crossbar only. We built 1T1R crossbar array test chip to measure the performance and efficiency of the DPE compared to a state-of-the-art ASIC. The DPE is the first complete crossbar-based computing engine design that leverages and integrates existing technologies to pursue a near-term accelerator product. We showed the potential of the DPE for accelerating many important applications, including machine learning, low power signal processing for IoT, and linear transformations such as the Fourier transform for FFT, etc. At the end of Chapter 5, we introduced the latest memristor application work on neuromorphic computing. The memristor devices allowed for extremely compact and low power, but also interesting analog properties that can potentially extend the offerings of availing CMOS technologies for neuromorphic computing. We demonstrated an earlier work that memristors with added cation-diffusion components were promising solution for modeling key features of biological synapses with better dynamic behavior.

6.2 Recommendations for future studies

Due to the time and resource limit, there will be many potential areas for the future opportunities and improvements. Below is a list of several major working areas for future recommended studies:

1). Modeling work

Our current modeling work runs on a more engineering platform like Matlab with implicit equations. The immediate next step is to convert and apply current device model for fast circuit simulations at SPICE level with more explicit form of dynamic equations of state variables. The implementation of the model will fill the missing link in the current memristor eco-system for the circuit simulation of memristors for actual production. For the longer term, there are many other possible mechanisms of the possible electron and ion conduction paths through an MIM stack like (1) direct tunneling; (2) Fowler–Nordheim (FN) tunneling; (3) Schottky emission; (4) tunneling from cathode to traps; (5) emission from defect trap to conduction band (the Poole–Frenkel emission); (6) FN-like tunneling from defect trap to conduction band; (7) recombination; (8) trap to defect trap hopping or tunneling, (9) tunneling from traps to electrode anode, etc. Further studies are needed to understand whether any one particular process dominates, or it is conjugated with complicated interactions in the different phase of the memristive switching with parasitic components consideration, in the presence of joint electrical, chemical and thermal impact. A good compact device model based on the full understanding of the physical switching mechanism needs to be developed for the SPICE simulator to reproduce the experimentally observed results, telegraphy noise, current fluctuations, and switching parameter variations. This will provide the necessary guide for the actual circuit design and simulation.

2). VCB selector

For the current VCB selector devices, high nonlinearity has been achieved. The current main challenge is the operation speed and reasonable operation voltage and current. As we understand that the volatility may be maintained by choosing appropriate dielectric materials, fast-diffusing metal cations, dielectric thickness, and suitable operating voltage regions and among others. Going forward, we need to explore the various combinations for the material selector with different device structure and also the dynamical interactions between these selectors and memristors. These investigations will inform our design of the selectors in order to best control the memristors' dynamics as they are being Set, Reset, or Read.

3). DPE and neuromorphic computing application

With some property tuning, the current memristive devices are able to fulfill the needs for the proof-of-principle demonstration of DPE and neuromorphic computing functions. An ultimate demonstration at requisite power would require a crossbar fabricated in a fab, which could be the next phase of the project. The key memristor attributes that need to be tuned for DPE applications include:

- i) Analog states with increasing the analog precision. Some preliminary results have suggested that exquisite analog switching can be more readily obtained from some materials, such as TaO_x , than others, such as TiO_x . Different switching materials need to be explored to optimize the analog behavior. In addition, a certain feedback circuit may also be adapted to precisely switch memristors to a range of resistances.
- ii) High resistance and low energy. The requirement for a high device resistance (at operating voltage) is based on the static leakage power consumption, which could be large due to the massively parallel operation. In addition, a higher OFF resistance is preferred because it leads to a desirable large OFF/ON resistance ratio given that the ON resistance needs to be large enough that the worst-case voltage drop across the crossbar wires is negligible compared to that across the devices.
- iii) For the neuromorphic computing, we need to apply the modified new memristor structure with added cation-diffusion part to the current DPE crossbar. An associated CMOS control circuit is needed to support the writing and reading functions. The novel hybrid memristor-CMOS neuromorphic circuit based on the tuned DPE will lead a radical departure from conventional neuro-computing approaches, as it uses specially tuned memristors to directly emulate the biophysics and temporal dynamics of real synapses.

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