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POWER AMPLIFIER DESIGN FOR NEXT GENERATION WLAN

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POWER AMPLIFIER DESIGN FOR NEXT GENERATION WLAN

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Table of Content

Acknowledgment.....	i
Table of Content	iii
List of Figures.....	v
List of Tables	xi
Abstract.....	xiii
Chapter 1	1
Introduction	1
1.1 Motivation	1
1.2 Objectives.....	6
1.3 Major Contributions	7
1.4 Organization of the Thesis	8
Chapter 2	11
Literature review of PAs for the 2.4GHz and 5GHz bands.....	11
2.1 WLAN at the 2.4GHz and 5GHz bands	12
2.1.1 Frequency and bandwidth	12
2.1.2 EVM and spectrum mask	14
2.1.3 Configuration of RF front-end	17
2.2 Wide-band matching techniques	18
2.2.1 The Bode-Fano Criterion	19
2.2.2 Network synthesizing.....	20
2.2.3 Network transformations.....	23
2.3 Nonlinearity of PAs.....	26
2.3.1 AM-AM distortion	27
2.3.2 AM-PM distortion	28
2.3.3 Memory effect.....	30
2.4 Reported PAs for WLAN at 2.4/5GHz	33
2.4.1 Narrow band PAs for WLAN at 2.4/5GHz	33
2.4.2 Wideband PAs in stat-of-the-art.....	36
Chapter 3	41
Literature review of PAs for the 60GHz band.....	41
3.1 WLAN at the 60GHz band.....	42
3.2 CMOS transistors at 60GHz.....	43
3.3 60GHz PAs in state-of-the-art.....	46
3.3.1 60GHz PAs with LC matching.....	46
3.3.2 60GHz PAs with transmission line matching.....	47

3.3.3 60GHz PAs with transformer matching	49
3.4 Challenges of 60GHz PA design with TMN	53
3.4.1 TMN design methods	53
3.4.2 In-band degradation of 60GHz PAs	57
Chapter 4	61
Design of a Class-AB PA with a bandwidth of 2-to-6GHz.....	61
4.1 Introduction.....	61
4.2 Matching Requirement of 2 nd Harmonic	64
4.2.1 Effect of load impedance at 2 nd harmonic	64
4.2.2 Target load impedance at the current source reference plane	67
4.3 Output Matching Network Design	68
4.3.1 Wideband matching for fundamental.....	69
4.3.2 Wideband matching for 2 nd harmonic	72
4.3.3 Limitation of bandwidth for 2 nd harmonic matching	76
4.4 Circuit Implementation	79
4.5 Measurement Result.....	83
4.6 Summary	91
Chapter 5	93
Design of a 60GHz PA.....	93
5.1 Introduction.....	93
5.2 Design issues of mm-wave PAs with TMN.....	96
5.2.1 Effects of driver stage power performance at mm-wave.....	96
5.2.2 Mismatch and degradation of power performance.....	98
5.2.3 Challenges of TMN design	100
5.3 Proposed TMN Synthesizing Method.....	101
5.3.1 TMN Modeling	101
5.3.2 Matching mechanism and matching equations of TMN	103
5.3.3 TMN synthesizing Procedure.....	107
5.4 A 60GHz PA with Synthesized TMNs	113
5.5 Measurement Results	118
5.6 Summary	124
Chapter 6	125
Conclusions and Future Works	125
6.1 Conclusions.....	125
6.2 Future Works	127
List of Publications.....	129
Bibliography	130

List of Figures

Figure 1.1: Tri-band operation of the next generation WLAN.....	3
Figure 1.2: A tri-band solution including one chip for the 2.4GHz and 5GHz bands and the other chip for the 60GHz band.....	5
Figure 2.1: Channels of WLAN at the 5GHz band [32]	12
Figure 2.2: (a) Constellation of QAM modulation; (b) Error vector of a QAM modulated signal	14
Figure 2.3: (a) Constellation of 64QAM; (b) Constellation of 256QAM.....	15
Figure 2.4: IM products generated by PA non-linearity, and the required spectrum mask of 802.11ac for a channel bandwidth of 80MHz.	16
Figure 2.5: A configuration of RF front-end for dual-band WLAN at 2.4GHz and 5GHz using PAs designed separately for each band	17
Figure 2.6: A configuration of RF front-end for dual-band WLAN at 2.4GHz and 5GHz using a wideband PA.	18
Figure 2.7: The Bode-Fano limits for RC and RL loads matched with passive and lossless networks. (a) Parallel RC. (b) Series RC. (c) Parallel RL. (d) Series RL.....	19
Figure 2.8: The optimum matching of a complex load given by Bode-Fano criterion [42]	20
Figure 2.9: Low-pass prototype. (a) Prototype beginning with a shunt element. (b) Prototype beginning with a series element.	21
Figure 2.10: Transformation of a low pass prototype network to a bandpass network. (a) A lowpass prototype network. (b) Impedance scaling. (c) Frequency scaling. (d) Low pass to bandpass transformation.	24
Figure 2.11: Norton transformation. (a) From <i>left-L</i> to <i>right-L</i> ; (b) From <i>right-L</i> to <i>Left-L</i>	25
Figure 2.12: Gain compression of an amplifier and the definition of P_{1dB}	27
Figure 2.13: AM-AM of a Class-AB PA with different bias voltages. [19].....	28
Figure 2.14: C_{GS} and C_{GD} of NMOS transistor in different bias regions [53]	28
Figure 2.15: Simplified schematic of PAs (a) without capacitance compensation and (b) with capacitance compensation [54]	29
Figure 2.16: C_{GS} and C_{GD} of a NMOS transistor in different bias regions [54]	29

Figure 2.17: IM3L and IM3H generated by the mixing of fundamental and envelop signals.....	32
Figure 2.18: Vector representation of the composition of IM3L and IM3H [57]	32
Figure 3.1: Worldwide available bandwidth at the 60GHz band.....	42
Figure 3.2: Simulated maximum available power gain of a 65nm NMOS device. [76]44	
Figure 3.3: Measured (a) f_T and (b) f_{MAX} of CMOS transistors in different technology nodes. [79]	45
Figure 3.4: Schematic of the first reported 60GHz PA in CMOS [81]	46
Figure 3.5: (a) Schematic and (b) layout of a transmission line matched 60GHz PA in CMOS [87].....	48
Figure 3.6: The (a) schematic and (b) layout of the first reported transformer based 60GHz PA in CMOS [78]	49
Figure 3.7: A 4-way power combiner based on transformer [93]	50
Figure 3.8: Area comparison between 60GHz PAs matched using (a) transmission lines and (b) transformers. [24]	51
Figure 3.9: P_{SAT} and PAE of 60GHz PAs designed in CMOS in state-of-the-art.....	52
Figure 3.10: A model of transformer using a differential transmission line [23]	54
Figure 3.11: a T model of transformer and its matching mechanism given in [24]	54
Figure 3.12: Transformer viewed as coupled resonators [59].....	55
Figure 3.13: Insertion loss frequency response versus coupling coefficient [59].....	56
Figure 3.14: Measured P_{SAT} and PAE of a 60GHz PA from 55 to 65GHz [25]	57
Figure 3.15: Measured P_{SAT} and PAE of a 60GHz PA from 55 to 65GHz [23]	58
Figure 4.1: Overlap of fundamental and 2 nd harmonic frequencies for PAs with bandwidth larger than one octave.....	63
Figure 4.2: (a) A differential transistor pair; and (b) a model of the drain outputs according to the optimum load impedance at fundamental frequency.....	65
Figure 4.3: Load-pull simulation results for load impedance at 2 nd harmonic. (a) The output current of 2 nd harmonic. (b) Simulation result for the 2 nd harmonic of 2.4GHz. (c) Simulation result for the 2 nd harmonic of 3.7GHz. (d) Simulation result for the 2 nd harmonic of 5.8GHz.....	65
Figure 4.4: Load-pull simulation results for load impedance at 2 nd harmonic at the current source reference plane. (a) The current source reference plane. (b) Simulation result for the 2 nd harmonic of 2.4GHz. (c) Simulation result for the 2 nd harmonic of 3.7GHz. (d) Simulation result for the 2 nd harmonic of 5.8GHz.	67

Figure 4.5: Synthesizing and transformation of the matching network for fundamental.	69
Figure 4.6: (a) Norton transformation of inductors from Right-L to Left-L. (b) Norton transformation of capacitors from Left-L to Right-L.	71
Figure 4.7: Model of transformer.....	71
Figure 4.8: (a) Fundamental currents in differential mode, and (b) 2 nd -harmonic currents in common mode.....	73
Figure 4.9: Different input inductances of transformer primary winding in differential mode and common mode.	73
Figure 4.10: (a) Fundamental currents in differential mode, and (b) 2 nd -harmonic currents in common mode.....	75
Figure 4.11: Load impedance for 2 nd harmonic at the current source reference plane with and without matching for 2 nd harmonic.	75
Figure 4.12: Simulated P_{SAT} and PAE of the PA with and without the matching for 2 nd harmonic.	76
Figure 4.13: Model of the load for 2 nd harmonic.	77
Figure 4.14: Schematic of the Class-AB PA with a bandwidth of 2-to-6GHz.	79
Figure 4.15: Capacitance compensation of a cascode structure using a PMOS varactor.	81
Figure 4.16: C_{in} of the cascode structure compensated by (a) PMOS varactor and (b) PMOS transistor.....	82
Figure 4.17: (a) The bias circuit of the PA. (b) Simulated P_{SAT} and PAE of the PA over temperature variation.	83
Figure 4.18: Die photo of the proposed PA with matching for 2 nd harmonic and a counterpart without matching for 2 nd harmonic.....	84
Figure 4.19: Simulated and measured S-Parameters of the proposed PA.	84
Figure 4.20: Measured gain, Pout and PAE of the proposed PA at 2.4GHz, 3.7GHz, and 5.8GHz.	85
Figure 4.21: Measured P_{SAT} and PAE of the proposed PA with matching for 2 nd harmonic and its counterpart without matching for 2 nd harmonic.	86
Figure 4.22: Measured AM-PM of the proposed PA.....	87
Figure 4.23: Measured IMD3 of the proposed PA at 3.7GHz with a tone spacing of 1MHz.	87
Figure 4.24: Spectrum and constellation of the proposed PA delivering 802.11ac format signal with 256QAM modulation and 80MHz bandwidth at 5.8GHz.	88

Figure 4.25: Measured output power of the proposed PA when delivering 802.11n format signal with an EVM of -28dB and 11ac format signal with an EVM of -32dB.	89
Figure 4.26: Simulated gain, P_{SAT} , P_{1dB} , and PAE of the PA with and without a bonding wire inductance of 1nH.	91
Figure 5.1: (a) Maximum peak PAE, and the ratio of minimum peak PAE over maximum peak PAE from 57 to 66GHz for 60GHz PAs in CMOS. (b) Measured peak PAE of this work from 57 to 66GHz.....	94
Figure 5.2: PAE of a two-stage PA affected by the gain of the output stage and the PAE of the driver stage. (a) Block diagram of a two-stage PA. (b) PAE of the PA (PAE_{PA}) with the variation of PAE_1 and G_{P2} . $G_{P1}=10dB$ and $PAE_2=30\%$ are assumed.	97
Figure 5.3: Mismatch to Z_{opt} and the degradation of transistor power performance. (a) Load-pull simulation result of a transistor with size of $40\mu m$ at its P_{1dB} . (b) Maximum degradation of power performance that may be caused by given mismatches.	99
Figure 5.4: (a) A simplified schematic of a PA using TMNs for input, inter-stage, and output matching. (b) A TMN model including source, transformer and load.	101
Figure 5.5: The model of TMN redrawn for matching analysis.	104
Figure 5.6: Matching mechanism of TMN represented on a Smith chart.	104
Figure 5.7: Flow chart of TMN synthesizing based on the derived matching equations of TMN.....	108
Figure 5.8: k and n calculated according to matching equations (5.7) and (5.9) for L_{TP} of 40 to 200pH.....	110
Figure 5.9: Bandwidth with $ \Gamma_S < -12dB$ for L_{TP} of 40 to 200pH. Adding of a 10fF capacitor on the source side makes the calculated parameters easier to realize.	110
Figure 5.10: (a) Metal layers available in the used 65nm CMOS technology. (b) Concentric transformer designed for the TMN synthesizing example.	111
Figure 5.11: Simulated S-parameters of the TMN matched by the synthesized concentric transformer.	112
Figure 5.12: Simulated S-parameters of the TMN matched by a stacked transformer ($n=1$).	112
Figure 5.13: Schematic of the 60GHz PA.....	114
Figure 5.14: Connections and transistor sizes of active stages.	115
Figure 5.15: $ \Gamma_S $ of synthesized TMNs in the 60GHz PA.....	116
Figure 5.16: Photomicrograph of the 60GHz PA.....	118
Figure 5.17: S-parameters and stability factor (K) of the PA.....	119

Figure 5.18: Measured P_{ldB} and P_{SAT} from 57 to 66GHz, and measured P_{out} of a 16QAM modulated signal with EVM of 8.91% in the 4 channels of 802.11ad.	120
Figure 5.19: Measured gain, output power and efficiency of the PA at 61GHz, and the simulated AM-PM of the PA at 61GHz.....	120
Figure 5.20: Simulated P_{SAT} and PAE of the PA with the variation of temperature.	121
Figure 5.21: Equipment setup for EVM measurement.	122
Figure 5.22: Measured EVM for 16QAM modulated signal at different power back-offs from P_{SAT} at 60.48GHz.	122

List of Tables

Table 2-1	13
Table 2-2	34
Table 2-3	40
Table 3-1	43
Table 3-2	52
Table 4-1	90
Table 5-1	123

Abstract

To meet the demand of achieving a multi-Gbps data-rate for the next-generation wireless local area network (WLAN), the 60GHz frequency band is now being explored as a complementary to the existing 2.4GHz and 5GHz frequency bands for WLAN. To take advantages of the high data-rate at 60GHz and the long communication distance at 2.4GHz and 5GHz, transceivers for the next generation WLAN are required to support all of the three frequency bands. As a block which is critical to the communication distance, data-rate and power consumption of a RF system, power amplifiers (PAs) are very important and challenging to design for the next generation of WLAN.

For the 2.4GHz and the 5GHz bands which have long been used for WLAN, reported PAs have all been designed separately for each band to optimize the performance. To reduce the circuit area and simplify the RF system for the next generation WLAN, a wideband PA with a bandwidth of 2 to 6GHz is designed in this thesis so that both of these two frequency bands can be supported by one PA. By using a technique to design output matching networks for both the fundamental and 2nd harmonic of Class-AB PAs with bandwidth larger than one octave, the designed PA demonstrates a maximum power-added efficiency (PAE) of 28.4% and an overall PAE above 19% in the entire bandwidth, which is comparable to the PAE of reported WLAN PAs designed separately for the 2.4GHz and the 5GHz bands. When compared to a counterpart without matching for 2nd harmonic, the PA shows a maximum improvement of saturated output power (P_{SAT}) and PAE by 1.9dB and 7.5% respectively. From 2 to 6GHz, the PA is capable of delivering an output power of 11.12-13.24dBm with EVM=-28dB for 11n formatted signals with 64QAM

modulation, and 9.31-11.31dBm with EVM=-32dB for 11ac format signal with 256QAM modulation.

For the newly introduced 60GHz frequency band, a big challenge of PA design is to maintain good power performance in the large bandwidth of 57 to 66GHz. To address this challenge, it is analyzed in this thesis that both the inter-stage matching network and the output matching network of a mm-wave PA need to be designed with small mismatch in the entire operating bandwidth. For this purpose, the matching equations of transformer-based matching networks (TMNs) are derived, based on which a method to synthesize TMN is proposed and applied to a 60GHz PA designed for the 802.11ad application. Implemented in a 65nm bulk CMOS technology, the PA achieves smaller degradation of power performance even compared to reported works in more advanced CMOS technologies. From 57 to 66GHz, the PA is measured with P_{SAT} of 13.94 to 14.35dBm, P_{1dB} of 10.81 to 11.68dBm, and peak PAE of 18.9% to 21.1%. With an EVM of 8.91%, the PA is capable of delivering 16QAM modulated signal with an output power larger than 10.8dBm and PAE higher than 10.1% in all the 4 channels of 802.11ad.

Chapter 1

Introduction

1.1 Motivation

Wireless local area network (WLAN) operating at the 2.4GHz and 5GHz bands, which includes the standards of 802.11a/b/g/n/ac and is commonly known as Wi-Fi, is widely used in today's computers, mobile phones, and many other portable devices for wireless communication. With the rapid growing of data demanding applications such as wireless video transfer, wireless docking, and wireless file synchronization, the data-rate provided by the 2.4GHz and the 5GHz bands becomes insufficient. In 802.11n and 802.11ac, multiple-input multiple-output (MIMO) and larger channel bandwidth are used to improve their data-rate. The maximally allowed number of antennas for MIMO is 4 and 8 respectively according to 802.11n and 802.11ac standards. However, in real applications, MIMO is seldom used in small form factor devices such as mobile phones, and MIMO with antenna number above 3 is seldom used even in access points. Therefore, the most practical data-rate for small form factor devices with only 1 antenna is only 150Mbps for 802.11n (40MHz channel bandwidth), 433Mbps for 802.11ac wave 1 (80MHz channel bandwidth), and 867Mbps for 802.11ac wave 2 (160MHz channel bandwidth) [1]. The increasing of channel

bandwidth from 20MHz of 802.11a/g, 22MHz of 802.11b, to 40MHz of 802.11n, and then to 80/160MHz of 802.11ac, directly contributes to the improvement of data-rate but is at the cost of allowing less devices to communicate at the rated speed simultaneously.

To solve this problem, the 60GHz ISM frequency band from 57 to 66GHz is now being explored for the next generation WLAN. With a totally available bandwidth of 9GHz in most of the world, the new standard for the next generation of WLAN, which is named as 802.11ad and certified as WiGig [2], has 4 channels and each channel is assigned with a bandwidth of 2.16GHz. Such a large bandwidth enables a maximum data-rate of 4.6Gbps when using single carrier modulation schemes and 6.7Gbps when using OFDM modulation schemes [3]. Compared to the data-rate of WLAN at the 2.4GHz and 5GHz bands, the data-rate of the new standard is around 10 times faster when only one antenna is used, making it extremely suitable for devices requiring a compact size and a high speed wireless connection. Due to the much larger bandwidth available at 60GHz and the capability of directional transmission, the aggregate data-rate that can be achieved in a dense environment is also greatly improved because many devices can communicate simultaneously without much interference [4].

However, due to the much larger propagation loss and the quasi-optical property of 60GHz signals, the communication at 60GHz is mostly confined within a room range. At the same communication distance, the propagation loss of a 60GHz signal is around 28dB and 21dB larger than that of 2.4GHz and 5GHz signals respectively because of the much shorter wavelength. 60GHz signals feature a quasi-optical property [5], making it easy to be attenuated by obstacles in indoor environments. For example, a human body can attenuate the signal by around 15dB [5] and a typical concrete wall can attenuate the signal by around 36dB [6]. Fortunately, the short wavelength at

60GHz making it feasible to design high gain antenna arrays in a compact size [7, 8], so that a communication distance of 10m can be achieved and the obstruction caused by obstacles can be alleviated by using adaptive beamforming and the reflections of signals [2, 9].

Figure 1.1: Tri-band operation of the next generation WLAN

To fully utilize the advantage of long communication distance at the 2.4GHz and 5GHz bands and the advantage of high data-rate at the 60GHz band, a tri-band operation is required for the next-generation of WLAN [2, 4, 5, 10]. As shown in Figure 1.1, within a tri-band network, we can use the high-data-rate link at 60GHz to support data-demanding applications such as wireless video transfer, wireless docking, and wireless file synchronization; beyond the range of 60GHz, we can use the 2.4 GHz and/or the 5GHz band to maintain the connectivity and perform less data-demanding activities such as accessing the Internet. Within the range of 60GHz, a tri-band operation is also necessary to ensure the robustness of connections because moving obstacles such as human bodies and pets may block the established link at 60GHz from time to time. When the 60GHz link is blocked, the communication needs to be

switched to 2.4 or 5GHz immediately until a new path for 60GHz signals is established by changing the beamforming configuration. By providing seamless hands-off between the three frequency bands, the best connection can always be provided without any user intervention or knowledge.

Despite of the great user experience of the next generation WLAN, the design of RF circuits for the next generation WLAN transceivers involves new challenges to be addressed, including the increased circuit area and cost, and the difficulty of designing 60GHz transceivers with high performance in CMOS.

First, the design of the next generation WLAN transceivers faces great pressure of reducing circuit area on chip and on board. As more and more wireless communication standards need to be supported, RF transceivers occupy a lot of spaces in portable devices. For example, in Apple iPhone 6S, 12 RF chips/modules for wireless applications including cellular, WLAN, Bluetooth, GPS, and NFC are used, occupying around half of the area on the mother board [11]. To support 802.11ad, additional RF circuits will be required, further increasing the area consumed by WLAN. As the cost of a circuit is closely related to its area, the cost of RF solutions for the next generation WLAN will also increase.

Figure 1.2 shows a solution of tri-band WLAN demonstrated by Qualcomm and Wilocity [12, 13], in which one chip is used for WLAN at 2.4GHz and 5GHz, and the other chip is used for WLAN at 60GHz. The chip for WLAN at 2.4GHz and 5GHz supports 802.11n with MIMO of 2×2 , corresponding to a maximum data-rate of 300Mbps. The other chip for WLAN at 60GHz utilizes single-carrier modulation, featuring a maximum data-rate of 4.6Gbps which is more than 10 times faster than that of the chip at 2.4GHz and 5GHz. Similar to many other publications/products [14-22], the chip for WLAN at 2.4GHz and 5GHz contains separate RF circuits for each band

in order to optimize the performance. The two chips fully occupy the area of a half mini PCIe card, which is suitable for the application in notebooks but too large for small form factor devices such as mobile phones. To make the solution more suitable for small form factor devices, it would be better if the two chips can be designed together as one chip and also the area of the chip can be reduced.

Figure 1.2: A tri-band solution including one chip for the 2.4GHz and 5GHz bands and the other chip for the 60GHz band

Second, in order to realize system level integration and reduce cost, 60GHz RF circuits will be designed in CMOS as well, which is similar to what have been done for WLAN at the 2.4GHz and 5GHz bands. However, at the frequency of 60GHz, the gain of CMOS transistors is much lower compared to that at the frequencies of several GHz, making it very difficult to design RF circuits, especially the power amplifiers (PAs), with enough gain, output power, and efficiency. To support the communication at 60GHz over an indoor distance, the transmitter is required to provide an output power of around 10dBm [9]. Such an output power needs to be generated with a high efficiency, so that battery powered portable devices can sustain a longer battery lifetime. From reported PAs at 60GHz, however, it can be seen that the high frequency

and the large bandwidth of the 60GHz band has created a big challenge for PAs to achieve large output power and high efficiency in the entire bandwidth of 57 to 66GHz. It is often observed that some PAs for the 60GHz band have achieved good output power and efficiency in part of the bandwidth, but the output power and efficiency degrades a lot in the whole bandwidth of 57 to 66GHz [[23-30](#)].

To reduce the circuit area of RF solutions for the next generation WLAN and improve the performance at 60GHz, new researches are required for the design of RF circuits, especially the design of PAs in CMOS.

1.2 Objectives

As a block which largely affects the communication distance and the data-rate of a RF system, PAs always consume big chip area and large power consumption. To address the challenges mentioned in last section, this research aims at designing PAs with reduced circuit area and cost for WLAN at 2.4GHz and 5GHz, and also improve the output power and efficiency of 60GHz PAs in the entire bandwidth of 57 to 66GHz. Because a high level of integration and a low cost are both important requirements of WLAN applications, all the designs are to be done in CMOS.

WLAN at the 2.4GHz and the 5GHz bands have similar requirement of output power and linearity, making it possible to design a wideband PA to support both of them. However, reported PAs supporting WLAN at these two frequency bands are conventionally designed separately for each band in order to achieve good power performance [[16](#), [31](#)]. In order to reduce circuit area and simplify the WLAN system, this research aims to design a wideband PA that can support both of these two frequency bands while maintaining an efficiency that is comparable to reported WLAN

PAs designed separately for each band. The PA also needs to feature a good linearity, so that high order modulation schemes such as 256QAM of 802.11ac can be supported with small distortion.

For the new standard 802.11ad, the objective is to design a 60GHz PA that maintains good power performance over the entire bandwidth of 57 to 66GHz, so that all the 4 channels of 802.11ad can be supported with enough output power and high efficiency. Matching techniques available at 60GHz are to be studied in detail, so that matching networks with small mismatch over a large bandwidth can be built at mm-wave frequency.

1.3 Major Contributions

In this research, two PAs are designed in CMOS for the next generation of WLAN, in which one is to support the 2.4GHz and the 5GHz bands, and the other is to support the 60GHz band.

The first PA is designed in Class-AB and has a large bandwidth of 2 to 6GHz so that WLAN at the 2.4GHz and 5GHz bands can both be supported. In order to achieve good power performance in such a large bandwidth, a technique to design output matching networks for both the fundamental and the 2nd harmonic of Class-AB PAs with bandwidth larger than one octave is introduced. Based on a wideband matching network designed for fundamental using traditional network synthesizing and transformation techniques, the wideband matching for 2nd harmonic is added into the matching network without affecting the fundamental matching by utilizing the characteristics of differential circuits and transformers. In the bandwidth of 2 to 6GHz, the PA achieves a maximum power-added efficiency (PAE) of 28.4% and an overall

PAE above 19%, which is comparable to the PAE of reported WLAN PAs designed separately for the 2.4GHz and the 5GHz bands. Compared to a counterpart without matching for 2nd harmonic, the PA shows a maximum improvement of saturated output power (P_{SAT}) and PAE by 1.9dB and 7.5% respectively. From 2 to 6GHz, the PA is capable of delivering an output power of 11.12-13.24dBm with EVM=-28dB for 11n formatted signals with 64QAM modulation, and 9.31-11.31dBm with EVM=-32dB for 11ac format signal with 256QAM modulation.

The second PA is designed at 60GHz, focusing on the challenge of maintaining good power performance in a large bandwidth at mm-wave frequency. A method to synthesize transformer-based matching networks (TMNs) is proposed based on the matching equations derived for TMN, and the challenge of maintaining good power performance in a large bandwidth at mm-wave is addressed by designing both the inter-stage matching networks and the output matching network of the PA with small mismatch in the entire operating bandwidth. Implemented in a 65nm bulk CMOS technology, the 60GHz PA achieves smaller degradation of power performance in the 9GHz bandwidth even compared to reported works in more advanced CMOS technologies. From 57 to 66GHz, the PA achieves P_{SAT} of 13.94 to 14.35dBm, P_{1dB} of 10.81 to 11.68dBm, and peak PAE of 18.9% to 21.1%. The PA is capable of supporting 802.11ad in all the 4 channels with output power larger than 10.8dBm and PAE higher than 10.1% when EVM is 8.91%.

1.4 Organization of the Thesis

Following the introduction of background for this research in Chapter 1, Chapter 2 reviews the techniques of designing wideband matching networks and the non-linearity

of PAs that need to be considered when designing PAs for WLAN at the 2.4GHz and the 5GHz bands. A summary of recently published PAs for WLAN at the 2.4GHz band and/or the 5GHz band, and a summary of wideband PAs designed in CMOS and other technologies are included as well. Chapter 3 reviews state-of-the art 60GHz PAs designed using LC matching, transmission line matching, and transformer matching. The challenge of designing wideband matching networks using transformer, and the in-band degradation of power performance in the bandwidth of 57 to 66GHz, are highlighted for 60GHz PAs. Chapter 4 introduces the design of a wideband PA with a bandwidth of 2 to 6GHz, in which a method to design matching networks for both the fundamental and the 2nd harmonic of Class-AB PAs with bandwidth larger than one octave is demonstrated. Chapter 5 shows the design of a 60GHz PA with high efficiency from 57 to 66GHz, where the synthesizing of TMN is analyzed in detail and applied to the design of matching networks for the PA. Chapter 6 concludes this thesis and gives the further work of this research.

Chapter 2

Literature review of PAs for the 2.4GHz and 5GHz bands

WLAN at the 2.4GHz band and the 5GHz band are both widely used today. As circuit area becomes a precious resource in portable devices, it is beneficial to design a wideband PA that can support both of these two frequency bands. Due to the large bandwidth and the requirement of a low EVM for high order QAM modulation, the design of such a wideband PA is very challenging. In this chapter, wideband matching techniques and the non-linearity of PAs are studied in detail, and reviews are given for recently reported WLAN PAs and wideband PAs.

2.1 WLAN at the 2.4GHz and 5GHz bands

2.1.1 Frequency and bandwidth

The operation of WLAN at the 2.4GHz and 5GHz bands are defined by the IEEE standards 802.11 a/b/g/n/ac [32-36]. For WLAN at the 2.4GHz band, the allocated frequency covers from 2.4GHz to 2.4835GHz for most of the world. Within this frequency range, there are 13 channels for which the center frequencies are allocated from 2.412GHz to 2.472GHz in steps of 5MHz. In Japan, an additional channel with center frequency of 2.484GHz is used for 802.11b. WLAN standards at the 2.4GHz band include 802.11b/g/n, each has a channel bandwidth of 22MHz, 20MHz, and 20/40MHz. The maximum data rates with one antenna are 11Mbps, 54Mbps, 72.2/150Mbps respectively. With multiple-input and multiple-output (MIMO), 802.11n can support a maximum data-rate of 600Mbps when 4 antennas are used.

Figure 2.1: Channels of WLAN at the 5GHz band [32]

The frequency range of WLAN at the 5GHz band is quite different under different regulations. To support WLAN at this frequency band globally, the RF front-end of WLAN transceivers need to cover the bandwidth of 4.91-5.835GHz [37]. Commercial WLAN transceivers at this frequency band, e.g. BCM4330 from Broadcom, usually have a bandwidth of 4.9-5.85GHz [38]. Figure 2.1 shows the channels of WLAN from 5.15 to 5.35GHz and from 5.725 to 5.825GHz given by FCC U-NII [32], which are the mostly used frequency ranges for WLAN at the 5GHz band. WLAN standards utilizing this frequency band include 802.11a, 802.11n and 802.11ac, where each of them may have a channel bandwidth of 20MHz, 20/40MHz, and 20/40/80/160MHz. With larger channel bandwidth, WLAN at the 5GHz band is able to provide higher data-rate than WLAN at the 2.4GHz band. Table 2-1 shows the data-rate of 802.11ac with 80MHz channel bandwidth and a single antenna under different modulation and coding schemes (MCSs). When using a single antenna, the maximum data-rate of 802.11ac reaches 433.3Mbps in MCS9, which is around 3 times of that of 802.11n with a channel bandwidth of 40MHz.

Table 2-1

DATA-RATE OF 802.11AC WITH A CHANNEL BANDWIDTH OF 80MHZ AND SINGLE ANTENNA

MCS	Modulation	Coding rate	EVM (dB)	SNR(dB)	Data-rate (Mbps, 400ns GI)
0	BPSK	1/2	-5	8	32.5
1	QPSK	1/2	-10	11	65
2	QPSK	3/4	-13	15	97.5
3	16QAM	1/2	-16	17	130
4	16QAM	3/4	-19	21	195
5	64QAM	2/3	-22	24	260
6	64QAM	3/4	-25	26	292.5
7	64QAM	5/6	-27	31	325
8	256QAM	3/4	-30	35	390
9	256QAM	5/6	-32	37	433.3

2.1.2 EVM and spectrum mask

To make an efficient use of the frequency spectrum, orthogonal frequency division multiplexing (OFDM) is adopted for WLAN, and the data subcarriers of OFDM are modulated with high order quadrature amplitude modulation (QAM) for WLAN MCSs with a high data rate. To ensure a correct de-modulation on the receiver side and avoid interferences of adjacent channels, the transmitted WLAN signals need to satisfy the requirement of EVM and spectrum mask given by the WLAN standards.

Figure 2.2: (a) Constellation of QAM modulation; (b) Error vector of a QAM modulated signal

In a QAM modulation, digital data bits are converted to the amplitude of an in-phase signal (I) and the amplitude of a quadrature signal (Q), resulting a modulated signal with variable amplitude and phase. Figure 2.2(a) shows the constellation map of a 16QAM modulated signal, which contains 4 states for I and 4 states for Q , corresponding to 2 bits of data modulated on I and 2 bits of data modulated on Q . In reality, there is always some error of the modulation, especially when the modulated signal is amplified by a nonlinear PA. The error of the modulated signal, including the error of amplitude and phase, can be represented as an error vector as shown in Figure 2.2(b). The ratio between the amplitude of the error vector and the amplitude of the ideal signal is then called the error vector magnitude (EVM). To ensure the transmitted

signal can be correctly de-modulated, the EVM of a transmitted signal needs to be less than the EVM given by IEEE standards of WLAN.

(a)

(b)

Figure 2.3: (a) Constellation of 64QAM; (b) Constellation of 256QAM.

Figure 2.3 compares the constellation map of 64QAM modulation and 256QAM modulation. Compared to a 64QAM modulated signal which carries 6 bits of data per symbol, a 256QAM modulated signal carries 8 bits of data per symbol which is 33.3% more. However, a 256QAM modulated signal contains 4 times of points on the

constellation map, allowing a much smaller EVM of the transmitted signal. As shown in Table 2-1, the allowed EVM of 802.11ac MCS7 with 64QAM modulation is -27dB, but the allowed EVM of 802.11ac MCS9 with 256QAM modulation is only -32dB. Such stringent EVM requirement allows very small distortion of the signal in the transmitter chain, making it very important to reduce the non-linearity of the PA.

Figure 2.4: IM products generated by PA non-linearity, and the required spectrum mask of 802.11ac for a channel bandwidth of 80MHz.

Besides EVM, another important requirement of transmitted WLAN signal is the spectrum mask to avoid interference of adjacent channels. When a modulated signal is amplified by a PA, inter-modulation (IM) products are generated due to the non-linearity of the PA. When the IM products are generated in the channel bandwidth, they will degrade the EVM of the transmitted signal. When the IM products are generated out of the channel bandwidth, they will affect the receiving of signals on adjacent channels or even other types of communication systems. To avoid such interferences, the transmitted signal needs to satisfy the requirement of spectrum mask, which gives the upper limit of IM products generated by WLAN transmitters. Figure 2.4 shows the spectrum mask of 802.11ac for the channel bandwidth of 80MHz. It can be seen that the IM products generated by the PA need to be much smaller than the original signal.

2.1.3 Configuration of RF front-end

In order to achieve better performance, reported solutions for WLAN at 2.4GHz and 5GHz have all adopted PAs designed separately for each band. Figure 2.5 shows a configuration of RF front-end that has been used in commercial products to support WLAN at the 2.4GHz and 5GHz bands using PAs designed separately for each band [39]. This configuration requires a total of two PAs, two LNAs, two switches, two bandpass filters, and one dual-band antenna. The two PAs and the two LNAs provides the amplifying of signals during transmitting and receiving. The two switches are used for the switching between TX and RX, and the two band pass filters including one for the 2.4GHz band and the other for the 5GHz band are used to filter out the unwanted frequency spurs during TX and the unwanted noise and interferences during RX. The dual-band antenna has the capability of transmitting and receiving signals at the two frequency bands.

Figure 2.5: A configuration of RF front-end for dual-band WLAN at 2.4GHz and 5GHz using PAs designed separately for each band

To reduce the circuit area and cost, this thesis targets to design a wideband PA that can support both the 2.4GHz band and the 5GHz band. Assuming that the LNA is also designed as wideband, or dual-band as in [40], then a configuration of RF front-end as shown in Figure 2.6 can be adopted. In this configuration, only one PA and one LNA are required, resulting less circuit area, lower cost, and a more simplified RF system.

Figure 2.6: A configuration of RF front-end for dual-band WLAN at 2.4GHz and 5GHz using a wideband PA.

To design a wideband PA for WLAN at the 2.4GHz band and the 5GHz band, however, is very challenging. To cover the two frequency bands, the PA needs to have a bandwidth of 2.4 to 5.9GHz which is larger than one octave, requiring matching techniques that can achieve an extra-large bandwidth. What is worse, to achieve linear amplification with higher efficiency, PAs in Class-AB instead of Class-A are normally used for WLAN, requiring a proper matching of not only the fundamental but also the harmonics. When the bandwidth is larger than one octave, there is overlapping of the 2nd harmonic frequency and the fundamental frequency, introducing additional challenges.

Besides the challenge of wideband matching, there is also the challenge of reducing the non-linearity of the PAs so that the stringent requirements of EVM and spectrum mask can be satisfied. PA non-linearity including AM-AM, AM-PM, and memory effects, all need a careful consideration.

In sections 2.2 and 2.3, wideband matching techniques and the non-linearity of PAs are studied in detail for this purpose.

2.2 Wide-band matching techniques

A wideband PA is a PA in which all the matching networks are designed as wideband. In this section, the technique to synthesize wideband matching networks, and the transformation of networks between different configurations, are summarized.

2.2.1 The Bode-Fano Criterion

Figure 2.7: The Bode-Fano limits for RC and RL loads matched with passive and lossless networks. (a) Parallel RC. (b) Series RC. (c) Parallel RL. (d) Series RL.

The matching of an arbitrary complex load over a non-zero bandwidth is described by the Bode-Fano criterion [41], which gives the limitation of the minimum reflection coefficient magnitude that can be achieved with an arbitrary matching network. Figure 2.7 shows 4 types of complex load and their limitations of matching given by the Bode-Fano criterion, where $\Gamma(\omega)$ is the reflection coefficient looking into the matching network. Bode-Fano criterion points out that the maximum value of the integration of $\ln(1/|\Gamma|)$ is determined by the load, therefore the optimum matching of a

complex load should give $|\Gamma| = 1$ for frequencies out of band and $|\Gamma|$ equal to a constant for frequencies in band so that no integration area is wasted either out of band or in band. Figure 2.8 shows such a frequency response where $|\Gamma| = 1$ for frequencies out of band and $|\Gamma| = \Gamma_m$ for frequencies in band. It can also be concluded that perfect matching ($\Gamma = 0$) of a complex load can only be achieved at a finite number of frequency points rather than a continuous frequency range ($\Delta\omega = 0$). For a given load, achieving larger bandwidth is always at the expense of a larger reflection coefficient (larger Γ_m) in the passband. As the Q of load increases, the quality of the matching decreases, namely, the matching network will have either a smaller bandwidth and/or a higher reflection coefficient in the passband [42].

Figure 2.8: The optimum matching of a complex load given by Bode-Fano criterion [42]

The ideal square-shaped optimum matching of a complex load shown in Figure 2.8 can only be achieved by a matching network with infinite number of elements. In practice, Chebyshev matching networks with a reasonably small order number are used as approximations where the Chebyshev response is made equal to Γ_m [41, 42].

2.2.2 Network synthesizing

The synthesizing of matching networks starts from low-pass prototypes as shown in Figure 2.9 [43], where the components in the network are normalized so that $g_0 = 1$

Figure 2.9: Low-pass prototype. (a) Prototype beginning with a shunt element. (b) Prototype beginning with a series element.

and the network has a cutoff frequency of 1 rad/S. Depending on whether $g_1(g_n)$ is a capacitor in shunt or an inductor in series, $g_0(g_{n+1})$ is considered as the resistance or the conductance of the generator (load).

To obtain the optimum design of Chebyshev matching networks with a given order number of n , various methods were developed in order to find the required values of g elements. Fano has shown that, for a matching network to achieve minimum reflection coefficient in the passband, the g elements need to satisfy conditions given by the following two transcendental equations:

$$\frac{\tanh na}{\cosh a} = \frac{\tanh nb}{\cosh b} \quad (2.1)$$

$$\sinh a = \sinh b + \frac{A_1^\infty}{\omega_c} \sin\left(\frac{\pi}{2n}\right) \quad (2.2)$$

in which $A_1^\infty = 2R/L$ (series reactance) or $A_1^\infty = 2/RC$ (shunt reactance), ω_c is the cut-off frequency and equals to 1 for the low pass prototype matching network.

The solutions of these two equations have been given in various forms [41, 44-46]. In [46], an analytic solution of these two equations is given, providing a method to calculate the value of g elements for matching networks up to the 4th order. For matching networks with a parallel RC load (R_0 and C_1), suppose the target matching bandwidth is from ω_1 to ω_2 , then the center-frequency ω_0 (geometric mean instead of the arithmetic mean) and the fractional bandwidth Δ of the matching network are

$$\omega_0 = \sqrt{\omega_1 \omega_2} \quad (2.3)$$

$$\Delta = \frac{\omega_2 - \omega_1}{\omega_0} \quad (2.4)$$

The Q of the load, which is highly related to the matching quality, is calculated at the frequency ω_0 as

$$Q = \omega_0 R_0 C_1 \quad (2.5)$$

For a matching network with an order number of n , the value of g elements can be calculated by

$$\theta = \frac{\pi}{2n} \quad (2.6)$$

$$c = \frac{2}{Q\Delta} \sin \theta \quad (2.7)$$

$$\sinh a = \sqrt{\left(\frac{c}{2}\right)^2 + r_n} + \frac{c}{2} \quad (2.8)$$

$$D = \frac{2 \sinh a}{c} - 1 \quad (2.9)$$

$$k_{r,r+1} = \sqrt{\frac{\sin^2 r\theta \cos^2 r\theta + (\cos^2 r\theta + D^2 \sin^2 r\theta)(\sin^2 \theta) \left(\frac{1}{Q\Delta}\right)}{\sin((2r-1)\theta) \sin((2r+1)\theta)}} \quad (2.10)$$

$$g_0 = 1 \quad (2.11)$$

$$g_1 = \frac{1}{\left(\frac{1}{Q\Delta}\right)g_0} \quad (2.12)$$

$$g_j = \frac{1}{g_{j-1}k_{j-1,j}^2}, \quad j=2 \text{ to } n \quad (2.13)$$

$$g_{n+1} = \frac{1}{D\left(\frac{1}{Q\Delta}\right)g_n} \quad (2.14)$$

in which

$$r_n = 1, 0.5, 0.317, 0.2244 \quad \text{for } n=1,2,3,4. \quad (2.15)$$

With these formulas, the g elements for a low pass prototype network can be calculated. Based on the low pass prototype with bandwidth of 1 rad/S and $g_0=1$, network transformations can be performed and we can obtain bandpass matching networks required for the design of wideband PAs.

2.2.3 Network transformations

The scaling of impedance and frequency, and the low pass to bandpass transformation, are the techniques required to obtain practical band pass matching networks with required load impedance and bandwidth. Norton transformation is also often used to achieve the required impedance transformation ratio, and also for the purpose of differential to single-end conversion by inserting a transformer.

2.2.3.1 Impedance scaling

From a low pass prototype with $g_0=1$ to a practical circuit with source impedance (conductance) of R_0 (G_0), impedance scaling is performed for all the components in the matching network by multiplying the normalized impedance (conductance) of all the components by R_0 (G_0).

Figure 2.10 shows the procedure of transforming a low pass prototype network to a bandpass network. To perform the impedance scaling, the value of R and L

components are multiplied by R_0 , while the value of C components are divided by R_0 .

After the transformation, a low pass network with source impedance of R_0 and cut-off

frequency of 1 rad/S (or $\frac{1}{2\pi}$ Hz) is obtained.

Figure 2.10: Transformation of a low pass prototype network to a bandpass network. (a) A lowpass prototype network. (b) Impedance scaling. (c) Frequency scaling. (d) Low pass to bandpass transformation.

2.2.3.2 Frequency scaling

For the bandpass matching network to have a bandwidth from ω_1 to ω_2 , a frequency scaling is required so that the cut-off frequency of the low pass network is changed to

$$\omega_c = \omega_2 - \omega_1 \quad (2.16)$$

As shown in Figure 2.10(c), the values of L and C in the matching network are all divided by ω_c for this purpose.

2.2.3.3 Low pass to band pass transformation

As shown in Figure 2.10(d), a low pass network can be transformed into a bandpass network by replacing the shunt C with a parallel LC resonator and replacing the series L with a series LC resonator. For the bandwidth to be from ω_1 to ω_2 , the resonating frequency needs to be selected as $\omega_0 = \sqrt{\omega_1 \omega_2}$. After the impedance scaling, frequency scaling, and the low pass to bandpass transformation, we can obtain a bandpass matching network with source impedance of R_0 and matching bandwidth of ω_1 to ω_2 .

2.2.3.4 Norton transformation

Figure 2.11: Norton transformation. (a) From *left-L* to *right-L*; (b) From *right-L* to *Left-L*.

Norton transformation is a technique that can be used to change the impedance ratio between the source and load of a network while maintaining the response of the network unchanged [46-48]. Figure 2.11(a) and (b) shows the Norton transformation of networks from *left-L* connection to *right-L* connection and from *right-L* connection

to *left-L* connection respectively. In Figure 2.11(a), the values of components have the relationship of

$$N = \frac{Z_P}{Z_S + Z_P} \quad (2.17)$$

$$Z_a = \frac{Z_P}{N} \quad (2.18)$$

$$Z_b = \frac{Z_S}{N} \quad (2.19)$$

In Figure 2.11(b), the values of components have the relationships of

$$N = \frac{Z_S + Z_P}{Z_P} \quad (2.20)$$

$$Z_a = \frac{Z_S}{N} \quad (2.21)$$

$$Z_b = \frac{Z_P}{N} \quad (2.22)$$

When the ideal transformers with turn ratio of $1:N$ are removed from figure 2.11, the impedance seen by the source will be scaled down by N^2 , or identically, the impedance seen by the load will be scaled up by N^2 . This technique can be used to adjust the impedance transformation ratio of a matching network [46]. If the ideal transformer is considered as part of the modeling of a real transformer [49], then real transformers can be inserted into matching networks [50] to replace inductors and realize the required impedance transformation ratio, as will be shown in Chapter 4.

2.3 Nonlinearity of PAs

In order to support the OFDM modulation of WLAN, PAs for WLAN usually need to operate with a high peak to average power ratio (PAPR) of 10-12dB. Due to the stringent EVM requirement, the non-linearity of PAs needs to be very small. Such

non-linearity includes the AM-AM distortion, AM-PM distortion, and the memory effects of PAs.

2.3.1 AM-AM distortion

The AM-AM distortion describes the non-linearity of a PA in terms of the amplitude, which is mainly the gain compression happens when the amplitude of the input signal is too large. As shown in Figure 2.12 [51], when the input signal is small, the output of an amplifier increases proportionally to its input. However, as the input signal becomes larger, there is gradually a saturation of the output power and the output can no longer increase proportionally to the input power. The linear range of a PA is often characterized by the 1dB compression point (P_{1dB}), which is the power where the gain is compressed by 1dB.

Figure 2.12: Gain compression of an amplifier and the definition of P_{1dB} .

Practically, the AM-AM distortion of a PA may include both gain expansion and gain compression. For the design of a Class-AB PA, it is very important to select a suitable bias voltage so that both the gain expansion and the gain compression are small in a wide power range [19, 52]. If the bias voltage of a Class-AB PA is selected too low, then there will be gain expansion at high power levels, while if the bias is selected too high, then there will be soft gain compression starting from small signals. As shown by the blue curve in Figure 2.13, in order to achieve small AM-AM

distortion, a suitable bias should be selected so that the PA has an acceptably small gain expansion while the P_{1dB} of the PA is close to the saturated output power (P_{SAT}) of the PA [19].

Figure 2.13: AM-AM of a Class-AB PA with different bias voltages. [19]

2.3.2 AM-PM distortion

The AM-PM distortion of a PA describes the variation of the phase difference between its input signal and the output signal. Ideally, the phase difference between the input and the output signal of a PA should be a constant. However, in reality, the phase difference may be changed when the amplitude of the input signal is large, resulting in a distortion of phase for the amplified signal.

Figure 2.14: C_{GS} and C_{GD} of NMOS transistor in different bias regions [53]

The AM-PM distortion of a PA can be caused by nonlinear resistance and/or nonlinear reactance in the circuit [52], e.g. the nonlinear C_{GS} of a CMOS transistor.

Figure 2.14 shows the variation of parasitic capacitances inside a NMOS transistor in different bias regions [53]. It can be seen that C_{GS} of the transistor is a value dependent on the V_{GS} applied to the transistor. For a Class-AB PA where the transistor is turned on and off in a period, the effective input capacitance has a value dependent on the amplitude of the input signal.

Figure 2.15: Simplified schematic of PAs (a) without capacitance compensation and (b) with capacitance compensation [54]

Figure 2.16: C_{GS} and C_{GD} of a NMOS transistor in different bias regions [54]

Because the AM-PM distortion is related to both the resistance and reactance of transistors, the selection of bias voltage can significantly affect the AM-PM of a PA [19, 28, 52]. Besides selecting a suitable bias voltage, capacitance compensation [19, 54] is also shown to be an effective method of improving the AM-PM of Class-AB PAs. Figure 2.15 shows simplified schematics of PAs without and with capacitance compensation, and the mechanism of the compensation is given in Figure 2.16. As gate voltage increases, the gate input capacitance of a NMOS transistor will increase whereas the gate input capacitance of a PMOS transistor will decrease. When a PMOS transistor is connected to the gate of a NMOS transistor, a relatively constant input capacitance can be obtained, reducing the AM-PM distortion of a PA.

2.3.3 Memory effect

The memory effect of a PA describes distortions that are time or frequency dependent, e.g. a frequency dependent gain or a frequency dependent phase shift [55]. There are two distinct types of memory effects: electro-thermal memory effects which typically appear at low modulation frequencies below 100 kHz, and electrical memory effects which typically appear above MHz modulation frequencies. Electro-thermal memory effects are caused by thermal dependent characteristics, e.g. g_m of transistors. Electrical memory effects are caused by energy-storing elements such as capacitors and inductors in a PA. The memory effects of a PA can be investigated by applying a two-tone signal at PA input. By varying the tone spacing between the two tones, the memory effects of a PA can be observed by measuring the generated IM products such as the lower IM3 (IM3L) and the higher IM3 (IM3H). If the PA has large memory effects, the measured IM3L and IM3H will be asymmetrical as tone spacing increases.

In a PA, IM3L and IM3H can be generated by 3 mechanisms [56, 57]:

- (i) the 3rd order nonlinearity of the PA

- (ii) the 2nd-order mixing between fundamental and 2nd harmonic
- (iii) the 2nd-order mixing between fundamental and envelop

in which the first two mechanisms will only generate symmetrical IM3L and IM3H but the third mechanism will generate asymmetrical IM3L and IM3H. To understand this, suppose the frequency of the two input tones are ω_1 and ω_2 ($\omega_1 < \omega_2$). Because $\omega_2 - \omega_1$ is very small compared to ω_1 and/or ω_2 , the impedance at ω_1 and ω_2 are almost the same when ω_1 and/or ω_2 varies within the bandwidth of the PA. Therefore, the amplitude and phase of the two tones at ω_1 and ω_2 are changed by the PA by almost the same amount, and the IM3L and IM3H generated by the first mechanism have almost the same amplitude and phase. Similarly, because $2(\omega_2 - \omega_1)$ is very small compared to $2\omega_1$ and/or $2\omega_2$, the IM3L and IM3H generated by the second mechanism also have almost the same amplitude and phase. However, as shown in Figure 2.17, in the 3rd mechanism, the phase of the envelop signal are added to IM3H whereas subtracted from IM3L, resulting asymmetrical IM3L and IM3H. In Figure 2.18, the IM3L and IM3H of a PA are represented as vector sums of IM components generated by the three mechanisms [57]. It can be seen that the resultant IM3L and IM3H (referred as IM3U in Figure 2.18) only becomes asymmetrical when IM components generated by the 3rd mechanism are added.

Depending on the modulation bandwidth of a particular application, the tone spacing between ω_1 and ω_2 can vary from 0 to tens of MHz or even larger. The impedance at the envelop frequency of $\omega_2 - \omega_1$ can change significantly in such a large scale of frequency range. The resultant IM3L and IM3H will therefore be frequency dependent, namely, showing memory effects.

Figure 2.17: IM3L and IM3H generated by the mixing of fundamental and envelop signals

Figure 2.18: Vector representation of the composition of IM3L and IM3H [57]

To reduce the memory effects of a PA, the bias circuit and the power supply network of the PA need to be designed with low impedances in the modulation bandwidth [56], which can be a challenge when the modulation bandwidth is tens of MHz or even larger. Differential PAs, for which the bias and power supply voltages can be applied through the center-tap of transformers, are better choices compared to single-end PAs where the bias and power supply voltages are normally applied through large resistors or inductors [57].

2.4 Reported PAs for WLAN at 2.4/5GHz

2.4.1 Narrow band PAs for WLAN at 2.4/5GHz

Due to the high PAPR of OFDM modulation, which is around 10-12dB for WLAN signals, and the high order modulation schemes which allows very small distortion of the signals (e.g. EVM of -32dB for MCS9), the PAs of WLAN usually need to operate with a back-off of 10dB or even larger from its P_{SAT} . To improve the output power and efficiency in such situation, PAs for WLAN at 2.4GHz and 5GHz in recent years have mainly focused on increasing the output power, linearity, and efficiency.

Table 2-2 summarizes PAs (or SoCs with PAs) designed for WLAN at 2.4GHz and/or 5GHz in recent years, within which many of them are published by leading companies in the WLAN industry. To improve the output power, distributed-LC based power combine has been used in [17] and transformer based power combine has been used in [14, 17, 19] to design PAs with P_{SAT} near or above 30dBm. To improve linearity while do not increase much of the power consumption, a technique called multi-gated transistor (MGTR) is used in [16-18]. In these designs, multiple transistors with independent gate biasing are used together to replace the input device in a cascode configuration, so that the total g_{m3} (2^{nd} order derivative of g_m) is close to

Table 2-2

SUMMARY OF REPORTED PAS FOR WLAN AT 2.4GHz AND 5GHz

Ref.	Freq. (GHz)	P _{SAT} (dBm)	PAE (%)	P _{1dB} (dBm)	Pout(PAE) with modulation			Tech.	VDD (V)	Area (mm ²)	DPD	Other features
					BW=20MHz		BW=40MHz					
					EVM -25dB	EVM -28dB	EVM -30dB					
Analog PA:												
[14]	2.4	29	31.3%*	-	22.3	20.8	-	45nm	3.3	-	Yes	Transformer power combine
	5	26	32.1%*	-	18.7	17.3	-	45nm	3.3	-	Yes	-
[15]	2.4	27	-	-	-	20.8	20	55nm	3.3	-	Yes	Class AB, adaptive bias
	5	26	-	-	-	18.4	18	55nm	3.3	-	Yes	Class AB, adaptive bias
[16]	2.4	28.3	35.3%	26	22.4 (23.2%)	21.2 (19%)	-	65nm	3.3	0.44**	Yes	Class A + B
	5	26.7	25.3%	23.5	20.5 (17.1%)	19.5 (14.1)	-	65nm		0.36**		-
[17]	2.4	31.5	25%	27.5	25.5 (16%)	24.5 (14%)	-	65nm	3.3	6 (with pad)	Yes	Class A + B Distributed-LC power combine
	2.4	33.5	37.6%	30.5	26.4 (22%)	25.7 (20%)	-	65nm	3.3	6 (with pad)	Yes	Class A + B Transformer power combine
[18]	2.4	24.5	32%	24	19.5 (24.8%)	18.2 (21.3%)	-	0.13um	3.3	1.12	No	LS MGTR
[19]	2.4	30.1	33%	28	22.7	-	-	90nm	3.3	4.2	No	Transformer power combine
[20]	2.4	-	-	31.9 (51%)	22.8 (30.1%)	-	-	0.13um	3.3	2	No	Doherty
Digital PA:												
[21]	2.4	27.8	-	-	-	21.3 (19.5%)	20.1	28nm	2.2	-	Yes	DPA
	5	27	-	-	-	20.5 (19%)	18.5	28nm	2.2	-	Yes	DPA
[22]	2.4	27	-	-	-	19.5 @-30	18.6	40nm	3.3	0.3 (no balun)	Yes	DPA
	5	25.5	-	-	-	18.1 @-30	17.8	40nm	3.3	0.4	Yes	DPA

*Drain efficiency

** Area including PA and PA driver

zero in a wide range of input voltage and the IM3 of the PA can be reduced. Another technique to improve the linearity of PAs is adaptive bias as have been used in [15], in which the bias circuit is designed such that the bias voltage of the PA is increased when the amplitude of the PA input is increased. Both MGTR and adaptive bias are techniques that can help to improve the linear output power of a PA while keeping the current consumed by the PA low at small signal, so that the efficiency of the PA at large power back-off is improved. Another technique to improve the efficiency at large power back-off is the Doherty PA. However, Doherty PAs are normally poor in linearity and not suitable for WLAN applications. In [20], a Doherty PA is designed with an outstanding efficiency of 30.1% when delivering 802.11g signals with an EVM of -25dB. However, although special consideration is given for linearity, the output power of the PA is much smaller when an EVM better than -28dB is required. Another method to improve the efficiency at large power back-off is the digital PA (DPA), in which the PA is divided into many small PA units, and each unit is designed as a switching-typed PA controlled digitally for their ON and OFF. State-of-the-art DPAs were reported in [21] and [22] by leading companies in WLAN industry, showing a good efficiency when delivering modulated signal with required EVM. The challenge of DPA, however, is the large channel bandwidth of WLAN signals. Until now, reported DPAs are mainly for channel bandwidth of 20MHz or 40MHz, however, in 802.11ac wave 2, the channel bandwidth will go up to 160MHz.

It is no doubt that reported PAs for WLAN at the 2.4GHz and 5GHz bands have achieved superior performance. Designing of PAs separately for these two frequency bands makes it easier to optimize the performance for each band, however, it would consume less chip area, and therefore lower cost, if a wideband PA can be designed to support both of these two frequency bands. Many of the reported design techniques

used to improve the performance of PAs, such as power combine to improve output power, MGTR and adaptive bias to improve linearity and efficiency, and even DPA, can be used for wideband PAs as well.

2.4.2 Wideband PAs in stat-of-the-art

To achieve better performance, the PAs mentioned in section 2.4.1 are all narrow band PAs designed either for the 2.4GHz band or the 5GHz band. Even for dual-band SoCs supporting both of the two frequency bands such as [14, 15], their PAs are designed separately catering for each frequency band. Wideband PAs, which require more complicated matching techniques and usually have much lower efficiency, have never been adopted by industry companies to support WLAN. However, wideband PAs in state-of-the-art have shown the improvement of output power, bandwidth, and efficiency in recent years, indicating that wideband PAs are potential to be used as a low cost and simplified solution to support the two frequency bands of WLAN at 2.4GHz and 5GHz.

In [50], a wideband PA in 90nm CMOS process is reported, which achieves a bandwidth of 5.2GHz to 13GHz, a peak P_{SAT} of 25.2dBm, and a maximum peak PAE of 21.6%. Biased in Class-AB, the PA has adopted techniques including network synthesizing and Norton transformation to design a 3rd order output matching network to provide the optimum load impedance for transistors in a bandwidth that is larger than one octave. The on-chip transformer used in the matching network replaces the ideal components obtained from network synthesizing and transformation, and provides the important functionality of differential to single-end conversion for the output signal. Due to the large insertion loss of the output matching network and the consideration of matching only for fundamental, the maximum peak PAE of [50] is only 21.6% and the minimum peak PAE is only around 11.5%.

In [58], a PA with a bandwidth of 6.5 to 13GHz is designed in CMOS using transformers for matching. In the bandwidth of 8 to 12GHz, this design achieves P_{SAT} of 19 to 21.5dBm and peak PAE of 11% to 20.3%. Without using additional inductors for matching, this work consumes a very small chip area of 0.47mm $\times$ 1.34mm. However, it can be seen that even within a smaller relative bandwidth, the P_{SAT} and PAE of this work shows larger degradation compared to [50] in which high order matching networks are used for output matching and inter-stage matching. In [59], a PA in GaAs with bandwidth of 17 to 35GHz is designed using transformers realized with microstrip lines. Biased in Class-A, the matching network of the PA is also designed with considerations only given for fundamental. The PA achieves a maximum PAE of 30% to 40% and a P_{SAT} of 22.5 to 23.5dBm, showing good power performance in a wide frequency range. However, this design is based on GaAs technology which is seldom used for WLAN PA due to the higher cost compared to CMOS, and the design method is not suitable for the application of WLAN because the required transmission lines will be too long to be integrated on chip at the frequency of several GHz.

Wideband PAs in CMOS were also reported by stacking multiple common gate transistors on a common source transistor [60-64]. With this configuration, the power supply voltage of a PA can be increased, reducing the required impedance transformation ratio of the output matching network to achieve a large output power. The output matching network is therefore simplified, making it easier to achieve a large bandwidth and low insertion loss. In [60] and [61], there are even no output matching networks used, achieving extremely large operating bandwidth. In [60], a P_{SAT} above 21.2dBm and a peak PAE above 17% were reported in the frequency range of 6 to 20GHz under a supply voltage of 4.5V. In [61], a P_{SAT} of 20 to 22dBm and a

peak PAE of 18% to 36% were achieved in a frequency range of 1 to 5GHz. The method of eliminating the output matching network in [60] and [61], however, is not a universal method of designing wideband PAs because the P_{SAT} of the PA is determined by the supply voltage, whereas the supply voltage is limited by the reverse break down voltage of the drain-bulk diode of the top transistor [64]. On the other hand, when an output matching network is used, the bandwidth of the matching network is still the limiting factor, giving less bandwidth if the output matching network is not specially designed for wideband operation [62-64].

Continuous mode operations [65], in which reactive load impedances are allowed at fundamental and harmonic frequencies, provide another mechanism to design wideband PAs. Based on the concept, wideband PAs in continuous Class-B (Class-J) [66, 67], Continuous Class-C [68], continuous Class-E [69], continuous Class-F [70, 71], continuous inverse Class-F [72], and mode transferring from continuous Class-F to continuous inverse Class-F [73], were reported. The design of continuous mode PAs requires careful engineering of load impedances at both fundamental and harmonics (at least to the 2nd harmonic), which is suitable to realize on PCB using transmission lines but difficult for monolithic designs using lumped elements. What's more, compared to conventional PAs in which a resistive load impedance is used at fundamental frequency, the reactive load impedance at the fundamental frequency of continuous type PAs increases the voltage swing at transistor output for the same output power [65], increasing the risk of reliability for CMOS PAs due to the low breakdown voltage of CMOS transistors. Because of these two reasons, reported continuous type PAs are mostly designed using transmission line on PCB, and are all based on GaN or GaAs technologies with high breakdown voltages.

Table 2-3 summarizes the state-of-the-art wideband PAs designed using techniques mentioned in this section. With only lumped elements available, reported wideband PAs in CMOS has only realized wideband matching for fundamental but not wideband matching for harmonics, resulting in a low PAE. In Chapter 4 of this thesis, a new matching method with the capability of achieving wideband matching for both fundamental and 2nd harmonic over an octave bandwidth will be demonstrated to address this problem. It will be shown that, by using such a matching technique, a wideband PA with bandwidth of 2 to 6GHz can achieve PAE that is comparable to the PAE of reported WLAN PAs designed separately for the 2.4GHz and the 5GHz bands, making it possible to use a wideband PA to replace the two PAs for WLAN at 2.4GHz and 5GHz.

Table 2-3

WIDEBAND PAS IN START-OF-THE-ART

Ref.	Publication	Tech.	Bandwidth (GHz)	Gain (dB)	P _{SAT} (dBm)	Peak PAE (%)	VDD (V)	Area (mm ²)	Matching for harmonics	Features
[50]	JSSC 2010	CMOS 90nm	5.2-13	18.5 (peak)	21.5-25.5	11.5-21.6	2.8	0.45×1.55	No	3 rd -order matching network
[58]	TMTT 2011	CMOS 0.18 μm	6.5-13	25.3 (peak)	19-21.5*	11-20.3*	3.6	0.47×1.34	No	Transformer matching
[59]	TMTT 2012	GaAs	17-35	9-12	22.5-23.5	30-40	4	1.5 mm ²	No	Transformer using microstrip line, Class-A
[60]	JSSC 2013	CMOS 45nm SOI	6-20	6 (peak)	21.2-21.7	17-20.5	4.5 [#]	0.70×0.75	No	Stacked, no output matching
[61]	TMTT 2010	CMOS 0.18 μm	1-5	15-20	20-22	18-36	5	0.90×0.76	No	Stacked, no output matching
[63]	ISSCC 2013	CMOS 65nm	4.6-6.5	14.9 (peak)	25.4-28.2	9-20.6	4.8 ^{##}	1.96×3.00	No	Stacked, with output matching
[70]	IMS 2011	GaN	0.55-1.1	9.5-12	39.3-41.2	65-80 [†]	28	-	Yes	Continuous Class-F
[71]	TMTT 2012	GaN	1.35-2.5	15.2-17	41.1-42.5	68-82 [†]	28	-	Yes	Continuous inverse Class-F

* The data is for the bandwidth of 8-12GHz

[#] This work also supports VDD of 7.2V

^{##} This work also supports VDD of 6.35V

[†] Drain efficiency instead of PAE

Chapter 3

Literature review of PAs for the 60GHz band

The IEEE standard 802.11ad which operates at the 60GHz ISM frequency band is a new standard of WLAN enabling a maximum data-rate of 6.7Gbps. Due to the high operating frequency and the large bandwidth, the design of PAs for 802.11ad is very challenging in terms of gain, output power, and efficiency. To achieve a good power performance, the design of matching network is very critical. In this chapter, we have reviewed state-of-the-art 60GHz PAs with LC matching, transmission line matching, and transformer matching. The challenges of designing matching networks using transformer, and the problem of large in-band degradation of 60GHz PAs in the large bandwidth of 57 to 66GHz in reported works are highlighted.

3.1 WLAN at the 60GHz band

As shown in Figure 3.1, there is a bandwidth of around 9GHz in most of the world at the 60GHz ISM frequency band. Such a large bandwidth is divided into 4 channels, with each channel been allocated with a bandwidth of 2.16GHz. Benefitting from the large channel bandwidth, the WLAN standard 802.11ad at the 60GHz band can achieve a maximum data-rate of 4.6Gbps using single-carrier modulation and 6.7Gbps using OFDM modulation without relying on MIMO.

Figure 3.1: Worldwide available bandwidth at the 60GHz band

Table 3-1 compares the maximum data-rate that can be achieved by WLAN standards at the 2.4GHz, 5GHz, and 60GHz bands. When only one antenna is used, it can be seen that 802.11ad can provide a data-rate that is much higher than WLAN standards at the 2.4GHz and/or the 5GHz band. When MIMO with 8 antennas is used, the standard 802.11ac is able to achieve a comparable data-rate. However, due to the limitation of circuit area and antenna, MIMO is seldom used in portable devices. Even in access points (APs) where more circuit areas are allowed, the maximum number of

antenna used for MIMO is normally only three. 802.11ad which can achieve a data-rate of 6.7Gbps without using MIMO is therefore the most suitable for portable devices requiring a high data-rate and also a compact size. With the high data-rate provided by 802.11ad, a lot of applications can be supported wirelessly, such as wireless display, high-speed wireless file synchronization, wireless docking, etc.

Table 3-1

MAXIMUM DATA-RATE OF WLAN STANDARDS AT THE 2.4GHz, 5GHz, AND 60GHz BANDS

Standard	Channel bandwidth (MHz)	Modulation	Maximum data-rate	
			1 antenna	MIMO
11b	22	DSSS, QPSK	11Mbps	-
11a	20	OFDM, 64QAM	54Mbps	-
11g	20	OFDM, 64QAM	54Mbps	-
11n	20	OFDM, 64QAM	72.2Mbps	288.9Mbps (4 antennas)
	40	OFDM, 64QAM	150Mbps	600Mbps (4 antennas)
11ac	20	OFDM, 256QAM	86.7Mbps	693.3Mbps (8 antennas)
	40	OFDM, 256QAM	200Mbps	1.6Gbps (8 antennas)
	80	OFDM, 256QAM	433.3Mbps	3.47Gbps (8 antennas)
	160	OFDM, 256QAM	866.7Mbps	6.93Gbps (8 antennas)
11ad	2160	SC, 16QAM	4.6Gbps	-
	2160	OFDM, 64QAM	6.7Gbps	-

3.2 CMOS transistors at 60GHz

The continuous scaling of CMOS technology makes it possible to design 60GHz PAs in CMOS [24, 25, 74-76]. However, as frequency increases to the mm-wave region, the performance of active devices and passive devices in CMOS both degrade. The design of PAs for the 60GHz band is therefore much more challenging in terms of gain, output power, and efficiency compared to the design of PAs at the 2.4GHz and/or the 5GHz band.

Figure 3.2 shows the gain of a 65nm CMOS transistor at different frequencies [76]. It can be seen that, with the increasing of frequency, the maximum available power gain of the transistor decreases rapidly. At 60GHz, the gain of transistors in 65nm CMOS is only around 10dB [25, 76]. Considering the insertion loss of matching circuits, 60GHz PAs typically need 3 stages to achieve a gain of around 20dB. Due to the low gain of transistors, the required driving power is also increased, which further reduces the efficiency of 60GHz PAs [23].

Figure 3.2: Simulated maximum available power gain of a 65nm NMOS device. [76]

To generate enough output power, the transistors used in a PA need to be sufficiently large. In deep-scaled CMOS technologies, there is large parasitic resistance of gate connection because the gate poly is very narrow. In such a case, the finger width (W) of transistors can only be several μm in order to achieve a high f_T [77]. On the other hand, as the finger number of a transistor increases, the layout of the transistor becomes larger, introducing additional parasitics which degrades the gain and efficiency of PAs [77, 78]. The limitation on transistor size makes power combine necessary when really large output power is required.

To achieve a high gain and good linearity of 60GHz PAs, transistors need to be biased at the maximum f_T . It is very important observation that the characteristic of

CMOS transistors are highly related to the current density that the transistor is biased with, regardless of the technology node, foundry, and temperature [79]. Figure 3.3 shows the measured f_T and f_{MAX} of CMOS transistors in different technology nodes with the variation of biased current density. It can be seen that for transistors in 0.25 μm , 0.18 μm and 90nm CMOS, the highest f_T are all measured when the transistors are biased with a current density of around 0.3mA/ μm , and the highest f_{MAX} are all measured when the transistors are biased with a current density of around 0.2mA/ μm . For a PA to achieve good linearity, it is important that transistors in the PA can achieve almost the same gain in a wide range of V_{GS} . For the purpose of both high gain and good linearity, 60GHz PAs in Class-A are normally biased with a current density of 0.3mA/ μm [74, 78], corresponding to the optimum f_T of transistors. With 40nm or more advanced CMOS technologies, it is possible to design 60GHz PAs in Class-AB [28] or other classes [80], where a lower bias is used so that a higher efficiency can be achieved.

Figure 3.3: Measured (a) f_T and (b) f_{MAX} of CMOS transistors in different technology nodes. [79]

3.3 60GHz PAs in state-of-the-art

The design of 60GHz PAs has evolved from LC matching, to transmission line matching, and to transformer matching. Brought straight forward from low frequency PA design, LC matching is the first matching technique used to design 60GHz PAs. This technique, however, is not suitable at mm-wave due to the large loss and the single-end operation. With both high Q and acceptable chip area at 60GHz, transmission line matching is then used to design 60GHz PAs, achieving higher efficiency and larger output power. The most widely used matching technique for 60GHz PAs, however, is the transformer matching, which has the advantage of small insertion loss, compact area, differential circuit configuration, and the easy realization of power combine.

3.3.1 60GHz PAs with LC matching

Figure 3.4: Schematic of the first reported 60GHz PA in CMOS [81]

The first 60GHz PA in CMOS is reported in 2006 [81] based on traditional LC matching network. Figure 3.4 shows the schematic of the PA. Important considerations such as the selection of transistor gate width, the bias of CMOS transistors, and the

design of inductors at 60GHz are given in this design [74]. The PA is based on a 90nm CMOS process, which has transistor power gain of around 8dB at 60GHz. The PA has 3 stages, however, achieves only a gain of 5.2dB, showing the large loss of LC matching networks at 60GHz. The power performance of the PA is also affected by the loss of the LC matching network. The PA only achieves P_{1dB} of 6.4dBm, P_{SAT} of 9.3dBm, and PAE of 7%.

The reason of the poor performance of LC matching at 60GHz is mainly the low supply voltage and the lossy substrate of advanced CMOS technologies. For a load with impedance of R , the power delivered into it can be calculated by

$$P = \frac{V^2}{2R}. \quad (3.1)$$

For advanced CMOS technologies which can support 60GHz operation, the power supply voltage is only around 1V. In order to achieve a large output power, an impedance matching network with a large impedance transformation ratio is needed to convert the 50Ω load impedance to a small value at the transistor output [82]. However, as impedance transformation ratio increases, the loss of a matching network will also increase [83, 84], reducing the efficiency of the PA. On the other hand, the resistivity of silicon substrate is only around 10Ω/cm. The capacitive and magnetic coupling from substrate reduces the quality factor (Q) of inductors in matching networks, further increasing the loss of LC matching networks. Due to these drawbacks, LC matching networks are seldom used in following 60GHz PAs.

3.3.2 60GHz PAs with transmission line matching

As frequency goes up to 60GHz, transmission lines become possible to be integrated monolithically because the signal wavelength decreases to about 2.4mm in Si substrate [85]. The inductive Q of transmission lines can be higher than 25 at

60GHz by using properly designed coplanar waveguide (CPW) [86]. Using transmission lines for matching, 60GHz PAs in CMOS with gain higher than 20dB [87-89], output power larger than 13dBm without using power combine [89], and PAE higher than 15% [89, 90], were reported. When power combine is used, output power up to 20dBm has been achieved [91]. However, most of 60GHz PAs using transmission line matching still have a large chip area [87, 88, 90-92] mainly occupied by transmission lines. For example, [87] uses 3 cascode stages to achieve a gain of 25dB, occupying an area of $1.18\text{mm} \times 0.96\text{mm}$. The work [91] uses a 4-way power combine to achieve an output power of 20dBm, and the size is $1.85\text{mm} \times 0.9\text{mm}$. Figure 3.5 shows the schematic and layout of [87].

Figure 3.5: (a) Schematic and (b) layout of a transmission line matched 60GHz PA in CMOS [87]

3.3.3 60GHz PAs with transformer matching

The first 60GHz PA in CMOS using transformer-based matching network (TMN) is reported by [78] in 2008. The schematic and layout of it is shown in Figure 3.6. The PA achieves an output power of 12.3dBm while consuming an area of only $0.66\text{mm} \times 0.38\text{mm}$, showing great potential for TMN based 60GHz PAs to achieve a large output power and a small chip area. Ever since the report of work [78], TMN has been used for the design of many 60GHz PAs [23-25, 28, 93, 94].

Figure 3.6: The (a) schematic and (b) layout of the first reported transformer based 60GHz PA in CMOS [78]

TMN shows many advantages when used for the design of PAs at mm-wave:

(1) TMN doubles the voltage swing at transistor outputs and reduces the loss of matching network

Transformers can be used as a baluns at the input and output of a PA, enabling the using of a pseudo-differential architecture [23-25, 93] in which the voltage swing at transistor output is doubled when compared to that of a single-ended PA. With doubled voltage swing, the required impedance transformation ratio is reduced by a factor of 4 in order to achieve the same output power. Thus the loss of matching network can be significantly reduced. With less loss in the matching network, higher output power and efficiency can be achieved. [95] achieves a P_{SAT} of 14.85dBm without using power combination, while the work in [28, 94] have achieved PAE higher than 20%.

(2) Transformer based power combination is an effective way of achieving large output power

Using transformer, power combination can be performed to achieve higher output power easily. The work in [93] adopts a transformer based power combiner as shown in Figure 3.7, and it achieves a P_{SAT} of 18.6dBm and a PAE of 15.1% in 65nm CMOS.

Figure 3.7: A 4-way power combiner based on transformer [93]

(3) TMN based PAs have smaller size

Figure 3.8: Area comparison between 60GHz PAs matched using (a) transmission lines and (b) transformers. [24]

TMN can greatly reduce the size of 60GHz PAs because DC voltages can be fed from the virtual ground at transformer center-tap, and the area consuming RF chokes can be omitted. In [24], two 60GHz PAs are compared, in which one is designed using transmission line and the other is designed using transformer. Figure 3.8 compares their layout. The transmission line based design occupies an area of $0.75\text{mm} \times 1.2\text{mm}$, while the transformer based design occupies only $0.3\text{mm} \times 1.2\text{mm}$ which is 1/6 of the area of the transmission line based design. The transformer based design also has a gain that is 7 to 8dB higher, and the P_{SAT} is 3.5dB higher. The compact size of 60GHz

PAs with transformer can also be found in many other works [23, 25, 94], even when power combine is used [93].

Transformer based PAs also have other advantages, such as less interference to other circuit blocks because of the differential operation, easy second-harmonic filtering through center-taps, better ESD protection [58], etc.

Table 3-2

SUMMARY OF STATE-OF-THE-ART 60GHz PAs IN CMOS

Ref.	Gain (dB)	P _{SAT} (dBm)	PAE (%)	P _{1dB} (dBm)	VDD (V)	Tech.	Area (mm ²)	Matching
[81]	5.2	9.3	7.4	6.4	1.5	90nm	0.15	LC matching
[87]	25	8	7	5	1.5	90nm	1.13	Transmission line matching
[88]	20	12	9	8.2	1.2	90nm	0.65	Transmission line matching
[89]	30	13.8	12.6	10.3	1.8	90nm	0.33	Transmission line matching
[90]	8.2	11.6	11.5	10.1	1.0	90nm	1.03	Transmission line matching 2-way power combine
[90]	4.2	14.2	5.8	12.1	1.0	90nm	1.20	Transmission line matching 4-way power combine
[91]	20.6	20	14.2	18	1.2	90nm	1.67	Transmission line matching 4-way power combine
[92]	8.3	10.6	-	8.2	1.2	90nm	0.98	Transmission line matching
[78]	7.7	12.3	8.8	9	1.0	90nm	0.25	Transformer matching
[23]	13.8	11	14.6	-	1.0	90nm	0.22	Transformer matching
[24]	15	12.5	19.3	10.2	1.2	90nm	0.15	Transformer matching
[25]	16	11.5	15.2	5	1.0	65nm	0.05	Transformer matching
[93]	20.3	18.6	15.1	15	1.0	65nm	0.28	Transformer matching 2-way power combine
[28]	21.2	17.4	28.5	14	1.0	40nm	0.074	Transformer matching 2-way power combine
[28]	17	17.0	30.3	13.8	1.0	40nm	0.074	Transformer matching 2-way power combine, Class-AB

Figure 3.9: P_{SAT} and PAE of 60GHz PAs designed in CMOS in state-of-the-art.

Table 3-2 and Figure 3.9 summarize the state-of-the-art 60GHz PAs designed using above mentioned matching techniques. It can be seen that 60GHz PAs using transmission line matching and transformer matching can both achieve large output power. However, 60GHz PAs with transformer matching has the advantages of higher efficiency and smaller chip area compared to those with transmission line matching, showing that transformer-based matching networks are the most promising for the design of 60GHz PAs.

3.4 Challenges of 60GHz PA design with TMN

Although transformer-based matching networks (TMNs) have the advantages as described in last section, there are also challenges to be addressed. The designs of matching networks using LC and/or transmission lines are traditional matching techniques that have been well documented. The value of L and C, the impedance and length of transmission lines, are parameters need to be considered when designing matching networks with them and their values are easy to be changed continuously in a wide range. However, the design of TMN is a relatively new topic without much exploring, and the design of TMN has many physical limitations for the value of transformer parameters that can be realized.

3.4.1 TMN design methods

In previous works at mm-wave, [23] developed a distributed model of transformers using a differential transmission line, as shown in Figure 3.10. Transformers with different trace width (W) and outer dimension (OD) are characterized by the characteristic impedance (Z_0), propagation constant (γ), and length (l) of the transmission line. The model can be used for predicting the performance of TMN with

transformers in different size and calculating the impedance of TMN as shown in equation 3.2. However, due to the limitation of the transmission line model, this method is only applicable to transformers with a turn ratio of 1:1.

$$Z_{in} = \frac{\sin\left(\frac{kl}{2}\right) \left(4Z_c Z_d \tan\left(\frac{kl}{2}\right) + jR_L (Z_c + Z_d) \right)}{R_L \cos\left(\frac{kl}{2}\right) - j(Z_c + Z_d) \sin\left(\frac{kl}{2}\right)} \quad (3.2)$$

Figure 3.10: A model of transformer using a differential transmission line [23]

Figure 3.11: a T model of transformer and its matching mechanism given in [24]

In [24] a T-model composed of 3 inductors are adopted for transformers. Based on a Smith chart, this work explains how TMN is matched from the load impedance to the

source impedance by the leakage and mutual inductance of transformer, as shown in Figure 3.11. This method is intuitive, however, not suitable for wideband applications. When there is a large bandwidth, e.g. the 9GHz bandwidth at 60GHz, the source and load impedance of a TMN vary over frequency [58], then the source and load impedance would each be a line segment instead of a point on the Smith chart, making it difficult to compare and find the optimum matching of a TMN with this method.

TMN is also used at lower frequencies. [58] presents a PA operating from 6.5 to 13GHz with the turn ratio of transformer selected according to the capacitance ratio of the source side and the load side, so that the two sides can resonate at the same frequency. The impedance transformation ratio between the two sides, however, is not considered.

The analysis in [59] views a transformer as two coupled resonators and derived the matching condition based on the theory of coupled resonator filter [96]. A wideband PA working from 17 to 35GHz is designed using this method.

Figure 3.12: Transformer viewed as coupled resonators [59]

As shown in Figure 3.12, the two resonators are assumed to have the same self-resonating frequency, so there is relationship that

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} \quad (3.3)$$

When the two resonators are coupled, they will have two resonating frequencies ω_1 and ω_2 . The bandwidth of the circuit can be controlled by selecting a suitable M .

$$\omega_{1,2} = \sqrt{\frac{L_1 C_1 + L_2 C_2 \pm \sqrt{(L_1 C_1 - L_2 C_2)^2 + 4 C_1 C_2 M^2}}{2(L_1 C_1 L_2 C_2 - C_1 C_2 M^2)}} \quad (3.4)$$

$$\omega_{1,2} = \omega_0 \sqrt{\frac{1}{1 \pm k}} \quad (3.5)$$

$$BW = \omega_2 - \omega_1 = \frac{\omega_0}{2\pi} \left(\sqrt{\frac{1}{1-k}} - \sqrt{\frac{1}{1+k}} \right) \quad (3.6)$$

To achieve the required impedance transformation ratio, the turn ratio of the transformer is required to be

$$T = \frac{L_2}{L_1} = \frac{Z_0}{R} \quad (3.7)$$

Figure 3.13: Insertion loss frequency response versus coupling coefficient [59]

It can be seen from equations 3.3 and 3.7 that this method requires the source side capacitance or the load side capacitance to be selected according to other circuit parameters, making this method less applicable to inter-stage matching networks of PAs where the capacitance on both the source and the load sides are mainly

determined by transistors. Another drawback of the matching method is that, a larger bandwidth can only be achieved at the cost of a larger gain ripple according to the simulation result given in Figure 3.13 (Fig. 7 of [59]).

3.4.2 In-band degradation of 60GHz PAs

The most important benefit of the 60GHz band is the large bandwidth available from 57 to 66GHz. However, with such a large bandwidth, it is very challenging to design RF circuits with the capability of maintaining good performance in the entire bandwidth. From reported 60GHz PAs, it is normally found that some works have achieved superior P_{1dB} , P_{SAT} , and PAE in part of the bandwidth; however, there is a large degradation of performance in the bandwidth of 57 to 66GHz.

Figure 3.14: Measured P_{SAT} and PAE of a 60GHz PA from 55 to 65GHz [25]

Figure 3.14 shows the measured P_{SAT} and peak PAE of a 60GHz PA from 55 to 65GHz [25]. At 62GHz, the PA is measured with P_{SAT} of 11.5dBm and peak PAE of 15.2%. However, in the bandwidth of 58 to 65GHz, the P_{SAT} of the PA is degraded to a minimum value of 8.5dBm and the peak PAE is degraded to a minimum value of 10%. In the bandwidth of 57 to 66GHz, the degradation of P_{SAT} is more than 3dB, and the degradation of peak PAE is more than 7.2%. In [23], the PA achieves a P_{SAT} of 11dBm

and a peak PAE of 14.6% at 64GHz, however, at 57GHz the P_{SAT} is degraded to around 6.8dBm which is 4.2dB smaller, and the peak PAE is degraded to around 6% which is 8.6% smaller, as shown in Figure 3.15. The problem of large in-band degradation of performance can also be found in [24, 26, 27, 29, 30] as well.

Figure 3.15: Measured P_{SAT} and PAE of a 60GHz PA from 55 to 65GHz [23]

In a communication system, the output power of PA largely affects the communication distance, while the efficiency of PA dominates the overall efficiency of the transmitter. Therefore, it is very important for PAs to maintain good power performance in the entire operating bandwidth. The design of such a PA requires matching techniques that can achieve small mismatch in a large bandwidth. Despite of the widely using of TMNs for 60GHz PA design, there still lacks a systematic and widely applicable design method of TMN so that a TMN with given source and load impedance can be designed according to the required bandwidth. To address this problem, the design of TMN will be carefully examined in Chapter 5 of this thesis. It will be shown that by investigating the matching mechanism of TMN, the matching equations of TMN can be derived, and the design of wideband matching network for

mm-wave PAs using TMN can be done with small mismatch in a large bandwidth, enabling mm-wave PAs to achieve good power performance in a large bandwidth.

Chapter 4

Design of a Class-AB PA with a bandwidth of 2-to-6GHz

4.1 Introduction

The emerging applications of software-defined radio, wireless high-data-rate communication, and the multiple frequency bands of applications such as Wi-Fi and cellular communication, all call for wideband linear power amplifiers (PAs) designed in CMOS to provide the required spectrum flexibility, bandwidth, efficiency of circuit area and cost, as well as the possibility of system-on-chip (SoC) integration. Compared to narrow band PAs, wideband PAs require more complicated matching networks to provide the required load impedance for transistors in a large bandwidth, making it a big challenge for wideband PAs to achieve high efficiency.

Targeting at achieving minimum reflection coefficient in a wide passband, numerous network synthesizing methods [43, 45, 46] were developed by using Fano's design method [41] for networks with source and load in the forms of series RC and/or parallel RC. Together with network transformation techniques such as low-pass to band-pass transformation and Norton transformation [47, 97], wideband matching

networks can be built with desired center frequency and bandwidth, and can be realized by using various circuit elements such as lumped LC components, transmission lines, transformers, etc. Because series RC and parallel RC are good models of transistor input and output impedances in a large bandwidth [45, 46, 50], these wideband matching techniques provide a solution to the design of wideband PAs, especially for wideband PAs in Class-A, where a good matching for fundamental over the operating bandwidth is considered as necessary and sufficient.

However, PAs in Class-A have the drawback of low efficiency compared to other classes with reduced conduction angle, especially when large power back-off is required for the PA to support linear amplification of signals with high peak to average power ratio (PAPR) [98]. In real applications, Class-AB PAs are often the preferred solution when a linear amplification is required. Unfortunately, for Class-AB PAs to achieve good power performance, more complicated matching network is required. Transistors working in Class-AB, or in other Classes with reduced conduction angle, have output currents containing not only the fundamental but also the harmonic components, requiring the output matching network to provide not only a good matching for fundamental but also a good matching for harmonics. For narrow band PAs in Class-AB, the most common practice is to short the 2nd harmonic with a series LC resonator [54, 99] or a quarter-wavelength transmission line. However, these short circuits for 2nd harmonic are only useful in a narrow bandwidth. Also, when they are added into a wideband matching network designed using existing wideband matching techniques, they will invalidate the wideband matching designed for fundamental. What's worse, as shown in Figure 4.1, when the bandwidth of a PA is larger than one octave, there will be an overlap between the frequency of fundamental and the frequency of 2nd harmonic. The load impedance required by fundamental and 2nd

harmonic, will therefore conflict with each other in the overlapped frequency range, making it even more difficult to satisfy the requirement of both fundamental and 2nd harmonic.

Figure 4.1: Overlap of fundamental and 2nd harmonic frequencies for PAs with bandwidth larger than one octave.

In this chapter, we propose a new matching technique to enable the design of output matching networks for both the fundamental and 2nd harmonic of Class-AB PAs with bandwidth larger than one octave. Based on a differential architecture, the output current of a Class-AB output stage is divided into fundamental currents in differential mode and 2nd-harmonic currents in common mode. The different characteristics of circuit in these two modes are utilized, allowing the wideband matching for fundamental to be designed using traditional network synthesizing and transformation techniques, while the wideband matching for 2nd harmonic can be added into the matching network without affecting the load impedance for fundamental. Detailed analyses are given for the design procedure and also the factors affecting the achievable bandwidth. The proposed wideband matching techniques is applied to a 2-to-6GHz Class-AB PA [100], for which the bandwidth is larger than one octave and there is overlap between the frequency of fundamental and 2nd harmonic. Benefitting from the wideband matching of both fundamental and 2nd harmonic, the PA is measured with a maximum PAE of 28.4% and an overall PAE above 19% from 2 to 6GHz, which is comparable to the PAE of reported WLAN PAs designed separately for the 2.4GHz and the 5GHz bands. Compared to a counterpart without dedicated

matching for 2nd harmonic, the P_{SAT} and PAE of the PA are improved by a maximum of 1.9dB and 7.5% respectively. From 2 to 6GHz, the PA is capable of delivering an output power of 11.12-13.24dBm with EVM=-28dB for 11n formatted signals with 64QAM modulation, and 9.31-11.31dBm with EVM=-32dB for 11ac format signal with 256QAM modulation.

This chapter is organized as follows. Section 4.2 analyzes the effect and the target of load impedance at 2nd harmonic for Class-AB PAs. Section 4.3 introduces the proposed method of designing wideband matching networks for both fundamental and 2nd harmonic. Key factors affecting the bandwidth of matching for 2nd harmonic are also analyzed. Section 4.4 demonstrates a wideband PA designed using the proposed matching technique. Section 4.5 gives the measurement result and Section 4.6 summarizes the chapter.

4.2 Matching Requirement of 2nd Harmonic

In this section, the effects of load impedance at 2nd harmonic on the power performance of a Class-AB PA are verified through load pull simulation. The target areas of load impedance at 2nd harmonic are obtained at the drain output and also the current source reference plane of transistors.

4.2.1 Effect of load impedance at 2nd harmonic

For transistors biased in Class-AB, the output power and efficiency are highly related to the load impedance. Because transistors of a Class-AB PA are in saturation region when they are turned on, the drain current are well controlled by the gate voltage, and the drain voltage is determined by the drain current and the load impedance. To maximize the output power and efficiency, the load impedance of a

Figure 4.2: (a) A differential transistor pair; and (b) a model of the drain outputs according to the optimum load impedance at fundamental frequency.

Figure 4.3: Load-pull simulation results for load impedance at 2nd harmonic. (a) The output current of 2nd harmonic. (b) Simulation result for the 2nd harmonic of 2.4GHz. (c) Simulation result for the 2nd harmonic of 3.7GHz. (d) Simulation result for the 2nd harmonic of 5.8GHz.

Class-AB PA should be designed such that the drain current at fundamental is as high as possible, while the drain voltage can avoid the transistor from entering into the linear region. For PAs in Class-AB, the main components of drain current are the fundamental and 2nd harmonic. At the conduction angle of 180°, the amplitude of the 2nd-harmonic current is theoretically $4/(3\pi)$ [52], or 42%, of that of the fundamental current. Therefore, the load impedances at fundamental and 2nd harmonic both play important roles to determine the PA's output power and efficiency.

Figure 4.2(a) shows the schematic of a differential transistor pair biased in Class-AB. In a bandwidth of 2 to 6GHz, load-pull simulations are performed for load impedances at fundamental and 2nd harmonic respectively. To facilitate the synthesizing of wideband matching network for fundamental, a model composed of a parallel connection of a resistor R_{out} and a capacitor C_{out} is built for the transistor output according to the simulated optimum load impedance for fundamental (Z_{opt_1st}) [45, 46, 50]. As shown in Figure 4.2(b), $R_{out}=27\Omega$ and $C_{out}=0.94pF$ are able to represent the output impedance of the given devices in the interested frequency range.

With Z_{opt_1st} set for fundamental, load-pull simulations are performed for the load impedance at 2nd harmonic. Figure 4.3 shows the simulation result on Smith chart, where the steps of output power and efficiency are 0.5dB and 4% respectively, and the impedances on the Smith charts are normalized to R_{out} . As shown in the figure, at representative frequencies of 2.4GHz, 3.7GH and 5.8GHz, the load impedance at 2nd harmonic can change P_{SAT} by 4.56dB, 4.07dB, 3.58dB, and PAE by 29.6%, 26.1%, 21.1% respectively, indicating that a good matching for 2nd harmonic is essential for Class-AB PAs to achieve good power performance. The target areas in the figure represent impedances for which the degradation of output power and efficiency is less than 0.5dB and 4% respectively. Due to the effects of drain capacitance, the target

areas at different frequencies are largely different. To provide a deeper insight of the circuit operation, it is helpful to see the required load impedance for 2nd harmonic at the current source reference plane of transistors, as will be discussed in the next section.

4.2.2 Target load impedance at the current source reference plane

Figure 4.4: Load-pull simulation results for load impedance at 2nd harmonic at the current source reference plane. (a) The current source reference plane. (b) Simulation result for the 2nd harmonic of 2.4GHz. (c) Simulation result for the 2nd harmonic of 3.7GHz. (d) Simulation result for the 2nd harmonic of 5.8GHz.

Figure 4.4(a) shows the model of a transistor output containing a current source, the output resistance, and the output capacitance. The required load impedance at the current source reference plane is the load impedance where the current source and the output resistance are considered as the source, while the output capacitance is considered as belonging to the matching network. To perform load-pull simulation at the current source reference plane, a negative capacitor with the value of $-C_{out}$ is connected to the transistor drain. Figure 4.4(b)-(d) shows the load-pull simulation result at the current source reference plane of the transistor for the 2nd harmonic of 2.4GHz, 3.7GHz, and 5.8GHz. Again, the target areas in the figure represent impedances for which the degradation of output power and efficiency is less than 0.5dB and 4% respectively. It can be seen that a load impedance close to short circuit, or a capacitive load impedance with normalized magnitude smaller than 1, is required for the PA to achieve large P_{SAT} and high PAE. Compared to Z_{opt_2nd} at transistor drain output, the simulated Z_{opt_2nd} at the current source reference plane of transistor shows much smaller variation as frequency changes, providing a simple and consistent target for the design of matching circuit for 2nd harmonic over a large bandwidth. Compared to ideal Class-AB PAs where all harmonics are terminated with short circuit, the target areas of load impedance for 2nd harmonic in Figure 4.4 results in a small degradation of PA performance, but the represented impedances are much easier to realize in a large bandwidth.

4.3 Output Matching Network Design

The model of transistor output and the target areas of load impedance for 2nd harmonic obtained from load-pull simulations provide the target for the design of output matching networks for the Class-AB PA. In this section, the proposed technique

of designing output matching networks for both fundamental and 2nd harmonic of Class-AB PAs with bandwidth larger than one octave is introduced. The key factors affecting the bandwidth of matching for 2nd harmonic are also analyzed in detail.

4.3.1 Wideband matching for fundamental

The design of wideband matching network for fundamental is based on existing techniques of network synthesizing and transformation. Figure 4.5 shows the synthesized bandpass filter and the procedure of network transformation to obtain the wideband matching network for fundamental. In step (1), the bandpass filter is

Figure 4.5: Synthesizing and transformation of the matching network for fundamental.

synthesized with $R_0 = 2R_{out}$ and $C_1 = 0.5(C_{out} + 0.55pF)$. C_1 is selected to be larger than $0.5C_{out}$ so that the synthesized matching network can absorb some additional capacitance including the parasitic capacitance of the transformer. The frequencies of 2.3 and 6GHz are selected as the lower and the upper band edges to ensure the coverage of the 2.4GHz and the 5GHz ISM bands after chip fabrication. It is worth noting that the network synthesizing has targeted at achieving minimum reflection coefficient [46] in the passband for the given values of R_0 and C_1 , while the final target of achieving 50Ω load impedance is achieved by following network transformations. With an order number of 3, the maximum reflection coefficient is reduced to below -20dB, ensuring that the load impedance presented to transistors are close to Z_{opt_1st} in the entire bandwidth of 2.3 to 6GHz. In step (2), a Norton transformation is performed for L_1 and part of L_2 so that in step (3) a transformer can be inserted into the matching network to realize differential to single-end conversion. After inserting the transformer into the matching network, Norton transformation of capacitors C_2' and C_{3_1}' (part of C_3') are performed in step (4) so that the output resistance R_4' is converted to $R_4''=50\Omega$ after removing the ideal transformer generated in step (5). The circuit in step (5) has the same frequency response as that in step (1), however, it has single-ended output, and the output is matched to 50Ω from 2.3 to 6GHz, which is the required matching for fundamental of the wideband PA.

Figure 4.6 explains the Norton transformation of inductors from right-L to left-L, and the Norton transformation of capacitors from left-L to right-L. The transformers shown in blue in Figure 4.6 are ideal transformers. The value of inductors L_c , L_d , capacitors C_c , C_d , and the turn ratio n of the ideal transformer are all determined by the value of components before transformation. If the ideal transformer is removed from

the circuit after transformation, then the impedance of components connected to the right side will be scaled by a factor of $1/n^2$.

$$L_c = L_a \frac{L_b}{L_a + L_b}, L_d = L_a \frac{L_a}{L_a + L_b}, n = \frac{L_a + L_b}{L_a}$$

(a)

$$C_c = C_b \frac{C_a}{C_a + C_b}, C_d = C_a \frac{C_a}{C_a + C_b}, n = \frac{C_a}{C_a + C_b}$$

(b)

Figure 4.6: (a) Norton transformation of inductors from Right-L to Left-L. (b) Norton transformation of capacitors from Left-L to Right-L.

Figure 4.7: Model of transformer.

Figure 4.7 shows a model of transformer [49], in which L_P is the inductance of the primary winding, L_S is the inductance of the secondary winding, k is the coupling coefficient between the two windings, and n is the turn ratio defined by $n = \sqrt{L_S/L_P}$. From Figure 4.6(a) and Figure 4.7 it can be seen that, two inductors in right-L connection can be transformed to left-L connection, and then replaced by a real transformer. Also, it can be derived that the parameters of the transformer and the inductors before transformation has the relationship of

$$L_P = L_a \quad (4.1)$$

$$k = \sqrt{\frac{L_a}{L_a + L_b}} \quad (4.2)$$

$$n = \sqrt{\frac{L_a + L_b}{L_a}}. \quad (4.3)$$

In the procedure of network transformation shown in Figure 4.5, the inductor L_1 determines L_P of the transformer. For a given L_P , the k and n of transformer that can be realized are limited by metal layers available in a given technology and the construction of transformer. Therefore, during circuit design, only part of L_2 is involved in the transformation and absorbed into the transformer in step (3). The ideal transformer generated is also separated into two ideal transformers, one with turn ratio of $1:n_1$ and the other with turn ratio of $1:n_2$. The first ideal transformer with turn ratio of $1:n_1$ is realized by the transformer in step (3), while the second ideal transformer with turn ratio of $1:n_2$ is applied to components on the right to change the component values in step (3). With wideband matching for fundamental designed using the above method, $Z_{\text{opt_1st}}$ is provided for transistors from 2.3 to 6GHz.

4.3.2 Wideband matching for 2nd harmonic

At the drain outputs of a differential PA, the fundamental currents are in differential mode whereas the 2nd-harmonic currents are in common mode. In Figure 4.8, the matching network built for wideband matching of fundamental is replotted to show the different paths of fundamental currents and 2nd-harmonic currents. The fundamental currents flow into the primary winding of the transformer at one port and flow out of the primary winding from the other port. The center-tap of the transformer functions as a virtual ground for the fundamental current. The 2nd-harmonic currents,

however, flow into the primary winding at both ports and flow out of the primary winding from the center-tap. Such behaviors of the center-tap allow the adding of components at the center-tap to change the load impedance for 2nd harmonic while not affecting the load impedance for fundamental.

Figure 4.8: (a) Fundamental currents in differential mode, and (b) 2nd-harmonic currents in common mode.

Figure 4.9: Different input inductances of transformer primary winding in differential mode and common mode.

In the two different modes, the input inductances of the transformer are also different. Figure 4.9 shows the structure of the transformer used for the matching of fundamental. The primary winding of transformer contains 4 turns and can be

separated into two halves from the center-tap, with each half containing 2 turns. Each half of the primary winding has an inductance of $L_{PH}=0.82\text{nH}$ and there is coupling between them with a coupling coefficient of $k_{12}=0.5$. Due to the polarity of coupling, the input inductance in differential mode L_{DM} and the input inductance in common mode L_{CM} can be calculated by

$$L_{DM} = 2L_{PH}(1 + k_{12}) \quad (4.4)$$

$$L_{CM} = L_{PH}(1 - k_{12}). \quad (4.5)$$

For the given transformer, there is $L_{DM}=2.46\text{nH}$ and $L_{CM}=0.41\text{nH}$. The inductance L_{DM} is the inductance used for matching of fundamental. The inductance L_{CM} , which is a much smaller inductance compared to L_{DM} , can be used for the design of wideband matching network for 2nd harmonic.

Conventionally, the center-tap of transformer is connected to a power supply voltage which is an AC ground. As shown in Figure 4.10(a), in such a situation, the capacitance at the drain output C_{drain} will resonate in parallel with L_{CM} at the frequency of 6.44GHz, which is the 2nd harmonic of 3.22GHz. According to the load-pull simulation results given in Figure 4.4, the power performance around 3.22GHz will be degraded due to a load impedance close to open circuit at 2nd harmonic.

To obtain capacitive load impedance with normalized magnitude smaller than 1 for 2nd harmonic, components are added at the center-tap for this design as shown in Figure 4.10(b). For the load impedance to be capacitive, an inductor $L_{\text{tap}}=1.47\text{nH}$ is connected between center-tap and VDD, so that the parallel resonant frequency is reduced to lower than 4GHz. The inductor is constructed with thick metal layers and has a trace width of $12\mu\text{m}$ so that it only has a parasitic resistance of 0.55Ω at DC. After adding L_{tap} , a capacitor $C_{\text{tap}}=0.5\text{pF}$ is connected to the center-tap to further reduce the magnitude of the load impedance at the lower frequency end.

Figure 4.10: (a) Fundamental currents in differential mode, and (b) 2nd-harmonic currents in common mode.

Figure 4.11: Load impedance for 2nd harmonic at the current source reference plane with and without matching for 2nd harmonic.

Figure 4.11 shows the simulated load impedance for 2nd harmonic at the current source reference plane with and without the matching for 2nd harmonic. Before adding the matching for 2nd harmonic, only load impedances close to the higher frequency end are within the target area and there is a parallel resonance at the frequency of 6.2GHz,

which is very close to the calculated resonant frequency of 6.44GHz. After adding the matching circuit for 2nd harmonic, the load impedance for 2nd harmonic in the frequency range of 4.2 to 12GHz are within the target area, allowing the PA to achieve good power performance in the target bandwidth of 2.3 to 6GHz.

Figure 4.12: Simulated P_{SAT} and PAE of the PA with and without the matching for 2nd harmonic.

Figure 4.12 shows the simulated P_{SAT} and PAE of the PA with and without the matching for 2nd harmonic. As expected, the PA with matching for 2nd harmonic shows improvement of P_{SAT} and PAE in a wide frequency range compared to the PA without matching for 2nd harmonic. The maximum improvement is achieved at 3GHz, which is very close to the parallel resonant frequency.

4.3.3 Limitation of bandwidth for 2nd harmonic matching

To achieve a large bandwidth of matching for 2nd harmonic, the coupling between the two halves of the primary winding (k_{12}) and the inter-winding parasitic capacitance of the transformer play important roles.

Figure 4.13: Model of the load for 2nd harmonic.

Figure 4.13 shows a model of the load for 2nd harmonic. The value of L_{tap} is assumed to be large enough so that its effect on the circuit can be neglected. The capacitor C_{tap} is added for the purpose of reducing $|Z_{2nd}|$ at the lower frequency end to be less than 1 (normalized to R_{out}). As L_{CM} is assumed to be a small inductor, the capacitor C_{tap} can be viewed as a capacitor connected in parallel with C_{drain} at low frequency, reducing the magnitude of the capacitive impedance. However, C_{tap} introduces a parallel resonant frequency at

$$f_{P,Ctap} = \frac{1}{2\pi \sqrt{L_{CM} \frac{C_{drain} C_{tap}}{2C_{drain} + C_{tap}}}}. \quad (4.6)$$

For Z_{2nd} to be within the target area, $f_{P,Ctap}$ needs to be higher than the upper end of the bandwidth for 2nd harmonic matching. Therefore, it is a trade-off between the lower frequency end and the higher frequency end of the bandwidth when selecting C_{tap} . According to (4.4) and (4.5), for a specific L_{DM} required by fundamental matching, the value of L_{CM} is given by

$$L_{CM} = 2L_{DM} \frac{1 - k_{12}}{1 + k_{12}}. \quad (4.7)$$

To achieve a small L_{CM} , a large k_{12} is required. Specially, if $k_{12}=1$, then L_{CM} will be 0 and there is no parallel resonance caused by C_{tap} . In this design, the primary winding

of transformer is constructed with 4 turns so that the two halves of it are overlapped with each other to obtain a large magnetic coupling coefficient of $k_{12}=0.5$. With L_{DM} of 2.46nH, the value of L_{CM} is only 0.41nH. When $C_{tap}=0.5$ pF is added so that the normalized value of $|Z_{2nd}|$ is smaller than 1 for frequencies above 4.25GHz, the parallel resonant frequency $f_{P,Ctap}$ is as high as 17GHz.

Another factor affecting the bandwidth of matching for 2nd harmonic is the inter-winding parasitic capacitance of transformer. In Figure 4.13, the inter-winding parasitic capacitance of transformer is simplified as a lumped capacitor $C_{inter-win}$ connected to GND through an inductor L_S' . Due to the distributive characteristic of inter-winding parasitic capacitance, L_S' is smaller than the inductance of the secondary winding of transformer. $C_{inter-win}$ and L_S' introduce a parallel resonant frequency at

$$f_{P,Cinter-win} = \frac{1}{2\pi \sqrt{L_S' \frac{C_{drain} C_{inter-win}}{2C_{drain} + C_{inter-win}}}}, \quad (4.8)$$

limiting the upper end of the bandwidth for 2nd harmonic matching. Selection of transformer structure with small $C_{inter-win}$ can increase the upper end of the bandwidth for 2nd harmonic matching, however, it is always a trade-off between $C_{inter-win}$ and the coupling coefficient k of transformer because they are both affected by the distance between the primary winding and the secondary winding of transformer. Reducing the value of L_S' is another method yet difficult to realize because the transformer also needs to provide suitable k and n as required by fundamental matching. In this design, the transformer is designed with a distance of 3 μ m between the primary winding and the secondary winding, resulting a $C_{inter-win}$ of 0.2pF and a parallel resonant frequency of 12.2GHz. As can be seen from Figure 4.11, the load impedance for 2nd harmonic at the higher frequency end is close to a parallel resonant point, however, due to the parasitic resistance of inductors, Z_{2nd} close to the parallel resonance is far from the

open circuit point on Smith chart, giving a moderate power performance at frequencies near 6GHz.

4.4 Circuit Implementation

Figure 4.14: Schematic of the Class-AB PA with a bandwidth of 2-to-6GHz.

Figure 4.14 shows the schematic of the PA with the proposed wideband output matching network. Besides the output matching network introduced in Section 4.3, the

input matching and the inter-stage matching networks are also designed as wideband, but only for wideband matching of fundamental from 2.3 to 6GHz.

During the matching network design, EM simulation are performed for inductors and transformers used in the circuit. Modeling of inductors and transformers are conducted, so that the inductance and parasitics of inductors, and the inductance, coupling coefficient, turn ratio, and parasitics of transformers, can be extracted. Because the synthesized matching networks are all based on ideal inductors and transformer, the parasitic capacitance of inductors and transformer need to absorbed into the matching networks. Circuit optimizations are performed so that the matching networks considering parasitics achieve good matching and low insertion loss in the desired bandwidth. By using 3rd order matching networks for inter-stage matching and output matching, the reflection coefficient of them are below -15.8dB and -20dB respectively for fundamental matching in the bandwidth of 2.3 to 6GHz. The output matching for 2nd harmonic enables the PA to achieve good power performance while consumes additional chip area of only 0.04 mm².

Because the proposed wideband matching network can only be used with a differential output stage, an active balun is used as driver stage so that the PA can support single-end input. The active balun is designed based on an architecture with phase error correction [101]. All transistors used in the balun have the same size and are biased with the same current to further reduce the error of phase and amplitude. From 2 to 6GHz, the simulated phase error maintains below 0.5 ° when providing the required driving power. Compared to passive baluns based on transformer, the active balun only consumes a small chip area of 0.13×0.13mm² while providing the required gain and driving power. Benefitting from the high gain of the active balun, a 70Ω resistor is used as a wideband input matching while the PA still achieves a gain>20dB.

Figure 4.15: Capacitance compensation of a cascode structure using a PMOS varactor.

For the PA to keep good linearity when amplifying signals with both amplitude and phase modulation, capacitance compensation is used for the output stage to reduce AM-PM distortion. Different from PMOS transistors used conventionally for capacitance compensation [102], PMOS varactors are used for the compensation in this work because the capacitance of PMOS varactor is found to be more complementary to the cascode structure's input capacitance. As shown in Figure 4.15, the input capacitance of the cascode structure is affected by miller effect and can be calculated by

$$C_{in} = C_{GS} + C_{GD}(1 - A_v), \quad (4.9)$$

in which A_v is the voltage gain of the common source transistor. A_v of the common source device is affected by its g_m and load impedance, and the load impedance is further affected by g_m of the common gate device. This characteristic of cascode structure makes its input capacitance different from that of a common source amplifier without cascode. Figure 4.16 (a) and (b) shows C_{in} of the cascode structure compensated by a PMOS varactor and a PMOS transistor respectively. It can be seen that by using a PMOS varactor, the resulted C_{in} shows less variation when V_{GS} varies.

Figure 4.16: C_{in} of the cascode structure compensated by (a) PMOS varactor and (b) PMOS transistor.

Due to the larger ratio of C_{max}/C_{min} , the total capacitance after compensation using a PMOS varactor is only 1pF, which is much smaller compared to the 1.6pF capacitance after compensation using a PMOS transistor. The reduced capacitance is critical for the inter-stage matching network to achieve a wideband matching with good gain flatness.

In order to reduce the PA's variation of performance over temperature, the bias of the PA is applied using a circuit as shown in Figure 4.17(a) for the common source transistors. When the threshold voltage (V_{TH}) of transistors changes along with temperature, the bias voltage given by the bias circuit can track the variation of V_{TH} ,

maintaining an almost constant bias current. As shown in Figure 4.17(b), from -40°C to 125°C , the simulated variation of P_{SAT} is only 1.1dB, and the simulated variation of PAE is only 2.8%.

Figure 4.17: (a) The bias circuit of the PA. (b) Simulated P_{SAT} and PAE of the PA over temperature variation.

4.5 Measurement Result

The proposed PA with matching for both fundamental and 2nd harmonic, and a counterpart with matching only for fundamental, are both fabricated in a 65nm CMOS process. Figure 4.18 shows their micrographs, in which the proposed PA and its

counterpart each occupy a chip area of 0.89 mm^2 including pads. Measurements of small signal and large signal were performed for both of them at room temperature.

Figure 4.18: Die photo of the proposed PA with matching for 2nd harmonic and a counterpart without matching for 2nd harmonic.

Figure 4.19: Simulated and measured S-Parameters of the proposed PA.

The S-parameters of the PA are measured from 10MHz to 10GHz using a vector signal analyzer. Figure 4.19 shows the simulated and measured S-Parameters. Only the

S-parameters of the proposed PA are given because the proposed PA and its counterpart have the same S-parameter performance, which is determined by the matching for fundamental. With a bias current of 59mA from 1.8V for the driver stage and 23.6mA from 3.3V for the output stage, the PA achieves S_{21} of 23.6 ± 0.8 dB and $S_{11} < -11.8$ dB from 2 to 6GHz. Good gain flatness is achieved in the large bandwidth because of the wideband input matching, inter-stage matching, and output matching.

Figure 4.20: Measured gain, Pout and PAE of the proposed PA at 2.4GHz, 3.7GHz, and 5.8GHz.

The power performance of the proposed PA and its counterpart are both measured from 2 to 6GHz in steps of 0.1GHz. Figure 4.20 shows the measured gain, Pout, and PAE of the PA with input power swept from -25dBm to 5dBm at the frequencies of 2.4, 3.7 and 5.8GHz. The bias current corresponding to a flat gain as input power increases is measured to be 23.6mA, lower than the bias current of 35.7mA during simulation. This difference is believed to be caused by the inaccurate model of active devices, and has caused a decreasing of gain and output power in measurement.

Figure 4.21 compares P_{SAT} and PAE of the proposed PA with matching for 2nd harmonic and its counterpart without matching for 2nd harmonic. The proposed PA

achieves a maximum P_{SAT} of 22.4dBm and a maximum PAE of 28.4% at 2.3GHz. In the whole bandwidth of 2 to 6GHz, the P_{SAT} and PAE of the PA remain above 20.1dBm and 19% respectively, and the P_{1dB} of the PA is in the range of 17.81 to 20.73dBm, which is 1.7 to 2.4dB lower than P_{SAT} . Compared to the counterpart without dedicated matching for 2nd harmonic improves P_{SAT} , P_{1dB} and PAE in a wide frequency range. The maximum improvements of P_{SAT} , P_{1dB} and PAE are 1.9dB, 2.0dB and 7.5% respectively, which are all observed at 3.1GHz, showing a good agreement between analysis, simulation, and measurement.

Figure 4.21: Measured P_{SAT} and PAE of the proposed PA with matching for 2nd harmonic and its counterpart without matching for 2nd harmonic.

The AM-PM distortion of the PA are also measured and the result at 2.4, 3.7 and 5.8GHz are shown in Figure 4.22. Benefitting from capacitance compensation of the Class-AB stage using PMOS varactor, the AM-PM distortion of the PA is less than $\pm 2^\circ$ until P_{1dB} . Two-tone test shows that the PA has good linearity and small memory effect. As shown in Figure 4.23, the PA achieves IMD3 of -30dBc at 13.7dBm per tone, and the IMD3L and IMD3H are symmetric except near the IMD sweet spot [103].

Figure 4.22: Measured AM-PM of the proposed PA.

Figure 4.23: Measured IMD3 of the proposed PA at 3.7GHz with a tone spacing of 1MHz.

To verify the PA's capability of delivering modulated signal over the bandwidth of 2 to 6GHz, input signals with frame format of 802.11n (64QAM; 20 and 40MHz bandwidth) and 802.11ac (256QAM; 20, 40 and 80MHz bandwidth) with center frequency varied from 2 to 6GHz are applied to the PA without using any pre-distortion. The PAPR of the applied signal is around 11dB. Figure 4.24 shows the spectrum and constellation measured when the PA is delivering 7.2dBm 11ac format

Figure 4.24: Spectrum and constellation of the proposed PA delivering 802.11ac format signal with 256QAM modulation and 80MHz bandwidth at 5.8GHz.

signal with 256QAM modulation and 80MHz bandwidth. Figure 4.25 shows the output power recorded when EVM is -28dB for 64QAM and -32dB for 256QAM when the center frequency of signal is varied from 2 to 6GHz. 802.11ac format signal with 160MHz bandwidth is not measured due to limitation of the signal generator used. From 2 to 6GHz, the proposed PA is able to deliver an output power of 11.12-13.24dBm with EVM=-28dB for 11n format signals with 64QAM modulation and 20MHz bandwidth, and 9.31-11.31dBm with EVM=-32dB for 11ac format signal with 256QAM modulation and 20MHz bandwidth. The decreasing of output power for 80MHz modulation bandwidth is highly due to the increased EVM of the input signal

provided by signal generator, which is around -40dB for bandwidth of 20MHz and/or 40MHz, but around -36dB for 80MHz.

Figure 4.25: Measured output power of the proposed PA when delivering 802.11n format signal with an EVM of -28dB and 11ac format signal with an EVM of -32dB.

Table 4-1 summarizes the performances of the PA and compares the PA with its counterpart and other state-of-the-art wideband PAs in CMOS. Benefitting from good matching of both fundamental and 2nd harmonic in the entire bandwidth, the proposed PA achieves PAE above 19% in the entire bandwidth of 2 to 6GHz. The PA with matching for 2nd harmonic has improved P_{SAT} , PAE, P_{1dB} , and output power with modulated signal compared to its counterpart with output matching only for fundamental. These performances demonstrate the PA's capability of supporting applications requiring linear amplification in the frequency range of 2 to 6GHz, such as 802.11 a/b/g/n/ac. Compared to WLAN PAs designed separately for the 2.4GHz [14, 16-19] and the 5GHz [14, 16] bands in Table 2-2, which show an average PAE of 32.3% for PAs at 2.4GHz and an average PAE of 28.7% for PAs at 5GHz, the wideband PA with more a complicated output matching network has achieved lower but still comparable PAE of 28% at 2.4GHz and 20.8% at 5GHz.

Table 4-1

PERFORMANCE COMPARISON OF THE PROPOSED PA AND OTHER PRIOR ART WIDEBAND CMOS PAs

			This work	Counter-part	[50]	[63]	[58]
Wideband 2 nd harmonic matching			Yes	No	No	No	No
Bandwidth (GHz)			2-6	2-6	5.2-13	4.6-6.5	6.5-13
Fractional BW (%)			115.5	115.5	94.9	34.7	70.7
Gain (dB)			23.6±0.8	23.5±0.9	18.5 (peak)	16.9 (peak)	25.3 (peak)
P _{SAT} (dBm)			20.1-22.4	19.5-21.5	21.5-25.5	30.3	19-21.5 (8-12GHz)
PAE (%)			19-28.4	18.2-24.6	11.5-21.6	7-20.6	11-20.3 (8-12GHz)
AM-PM			<±2 °	<±2 °	-	-	-
Pout (dBm)	64QAM -28dB EVM	20M	11.12-13.24	10.72-12.16	-	-	-
		40M	10.66-12.80	10.27-11.93	-	-	-
	256QAM -32dB EVM	20M	9.31-11.31	8.64-10.34	-	-	-
		40M	8.52-10.63	8.04-9.57	-	-	-
		80M	6.69-8.59*	6.23-7.39*	-	-	-
	Area (mm×mm)			0.57×1.57	0.57×1.57	0.45×1.55	1.96×3.00
VDD(V)			3.3	3.3	2.8	6.35	3.6
Tech.			65nm	65nm	90nm	65nm	0.18 μm

*Limited by the EVM of signal generator (-36dB)

It is worth noting that the proposed PA and the benchmark designs in Table 4-1 are all measured without package. To check the effects of bonding wire inductance when the chip is packaged, simulations are done by connecting a typical bonding-wire inductance of 1nH between the output of the PA and a 50Ω load. As shown in Figure 4.26, when compared to the simulation results without the bonding-wire inductance, the simulated variations of gain, P_{SAT}, P_{1dB}, and PAE are in the range of -1.12dB to 1.83dB, -0.36dB to 0.35dB, -1.14dB to 0.3dB, and -3.5% to 2.4% respectively in the bandwidth of 2 to 6GHz. Such variations are believed to be acceptable and can be further reduced if the PA is co-designed with the inductance of the bonding wire.

Figure 4.26: Simulated gain, P_{SAT} , P_{1dB} , and PAE of the PA with and without a bonding wire inductance of 1nH.

4.6 Summary

This chapter focuses on the design of a wideband PA to support the WLAN at both the 2.4GHz band and the 5GHz band. Based on the different characteristics of fundamental current and 2nd harmonic current in a differential output stage, the matching for 2nd harmonic is added to a matching network without affecting the matching for fundamental, making it possible to design high efficiency Class-AB PAs with bandwidth larger than one octave. The designed PA achieves peak PAE that is comparable to WLAN PAs designed separately for the 2.4GHz and the 5GHz bands, and shows its capability of delivering 802.11n and 802.11ac formatted signal in the frequency range of 2 to 6GHz. The designed PA can be used to support WLAN at both the 2.4GHz band and the 5GHz band, reducing the area, cost, and the complexity of the RF system.

Chapter 5

Design of a 60GHz PA

5.1 Introduction

The demand of achieving a data-rate of multi-Gbps in wireless communication has facilitated the using of mm-wave frequency due to its large bandwidth. One of the examples is 802.11ad, the new standard of WLAN which employs the 60GHz frequency band to achieve a maximum data-rate of 6.7Gbps [104-106]. However, as frequency goes up to the mm-wave region, it becomes very challenging to design PAs, especially when CMOS technologies are used. The low supply voltage, lossy substrate, and the low gain of transistors, all challenge the design of CMOS PAs at mm-wave. To alleviate the challenges of the low supply voltage and lossy substrate, transformer-based matching networks (TMNs) have been widely used [23-30, 76, 93, 94, 107-109]. By using TMNs, a pseudo-differential architecture can be used for PAs, in which the voltage swing at transistor output are doubled so that the output power can be increased by a factor of 4 for the same load impedance [82]. TMNs have potentially less insertion loss compared to LC matching networks [110], and can be used for power combine [26-30, 76, 93, 107-109] to further increase PA output power.

Figure 5.1: (a) Maximum peak PAE, and the ratio of minimum peak PAE over maximum peak PAE from 57 to 66GHz for 60GHz PAs in CMOS. (b) Measured peak PAE of this work from 57 to 66GHz.

To ensure the advantage of large bandwidth at mm-wave is fully utilized, PAs are required to achieve good power performance in its entire operating bandwidth rather than only at certain frequency points. This is a challenge, however, for CMOS PAs at mm-wave because of the low gain of transistors. As will be described in section 5.2, the power performance of a PA is not only related to the performance of the output stage but also highly related to that of the driver stages when the gain of transistors is

low. Therefore, similar to the requirement that a PA's output matching network should provide the optimum load impedance (Z_{opt}) for transistors in the output stage [52], the inter-stage matching networks should also provide Z_{opt} for transistors in the driver stages. Unfortunately, because of the large gate capacitance loaded on inter-stage matching networks, achieving good matching in a large bandwidth is much more challenging for the design of inter-stage matching networks. Therefore, wideband PAs at mm-wave frequency are often observed with large degradation of power performance in its operating bandwidth. Figure 5.1(a) shows the peak PAE achieved by recently reported 60GHz CMOS PAs designed using TMN [23-30]. Some of these works have achieved maximum peak PAE above 20% at some frequency points due to the optimization of output matching networks, however, the minimum peak PAE in the bandwidth of 57 to 66GHz are only around 70% or even 40% of their maximum peak PAE.

In this chapter, the TMNs for both output matching and inter-stage matching of a 60GHz PA are designed with small mismatch to provide Z_{opt} in the entire operating bandwidth of 57 to 66GHz. As shown in Figure 5.1(b), implemented in a 65nm bulk CMOS technology, the designed PA achieves peak PAE of 18.9% to 21.1% in the 9GHz bandwidth, corresponding to a ratio of 89.6% between the minimum peak PAE and the maximum peak PAE. Based on the modeling and the analysis of the matching mechanism of TMN, the matching equations of TMN are derived and a TMN synthesizing method is proposed. The solution of the derived matching equations indicates all the possible parameter values of transformer that can match the given source and load of a TMN, so that transformers can be compared and selected according to the bandwidth of TMN. The TMN synthesizing method which is proposed based on the matching equations provides a systematic design flow to build a

transformer according to the required bandwidth. In the synthesizing method, an additional capacitor is also considered as a design freedom to improve the bandwidth of the TMN or make the selected transformer parameters easier to realize with the given metal layers of the technology used.

In the following of this chapter, the design issues of mm-wave PAs and the design challenges of TMNs are described in Section 5.2. The modeling, matching mechanism, matching equations, and the synthesizing of TMN are then given in Section 5.3. Section 5.4 demonstrates the design of a 60GHz PA using the proposed TMN synthesizing method. Section 5.5 shows the measurement result and Section 5.6 summarizes the chapter.

5.2 Design issues of mm-wave PAs with TMN

5.2.1 Effects of driver stage power performance at mm-wave

Figure 5.2(a) shows a block diagram of a two-stage PA with one driver stage and one output stage. The power gain (G_P) and the PAE of the two stages are assumed to be G_{P1} , G_{P2} , and PAE_1 , PAE_2 respectively. It can be derived that the PAE of the PA is

$$PAE_{PA} = PAE_2 \left[1 - \frac{PAE_2 - PAE_1}{PAE_2 + PAE_1 \frac{G_{P1}}{G_{P1} - 1} (G_{P2} - 1)} \right]. \quad (5.1)$$

Also, the OP_{1dB} of the PA ($OP_{1dB,PA}$) is given by

$$\frac{1}{OP_{1dB,PA}} = \frac{1}{OP_{1dB,1} G_{P2}} + \frac{1}{OP_{1dB,2}}. \quad (5.2)$$

Equation (5.2) indicates that to achieve a high $OP_{1dB,PA}$, the PA needs to be designed with $OP_{1dB,1} G_{P2} \gg OP_{1dB,2}$, namely when the gain of the PA compresses,

most of the gain compression should be caused by the output stage. However, to achieve small gain compression in the driver stage is at the cost of low PAE_1 , which as shown by (5.1), will cause PAE_{PA} to be much smaller than PAE_2 when G_{P2} is low.

Figure 5.2: PAE of a two-stage PA affected by the gain of the output stage and the PAE of the driver stage. (a) Block diagram of a two-stage PA. (b) PAE of the PA (PAE_{PA}) with the variation of PAE_1 and G_{P2} . $G_{P1}=10dB$ and $PAE_2=30\%$ are assumed.

As 60GHz, the maximum available power gain (MAG) of 65nm CMOS transistors is only around 10dB [25, 76]. Considering the gain compression when a PA is driven into its high efficiency region and the insertion loss of the output matching network, the gain of the output stage will be even lower. Figure 5.2(b) plots PAE_{PA} of the two-stage PA with the variation of PAE_1 and G_{P2} based on (5.1), where $G_{P1}=10dB$ and $PAE_2=30\%$ are assumed. The figure shows that when G_{P2} is 10dB or lower, a small PAE_1 will make PAE_{PA} to be much smaller than PAE_2 . For example if G_{P2} is only 6dB

when the PA is saturated, a driver stage efficiency of $PAE_1=5.7\%$ will cause $PAE_{PA}=15\%$, reducing PAE_{PA} to be only half of PAE_2 .

Because of load-pull effect, it is required that an optimum load impedance (Z_{opt}) to be presented at the output of a transistor so that a large output power and high efficiency can be achieved [52]. To improve the power performance of driver stages, the inter-stage matching networks of mm-wave PAs need to provide Z_{opt} for driver stage transistors. This is similar to the requirement that the output matching network of a PA should provide Z_{opt} for the transistors in the output stage. However, affected by the large gate capacitance of CMOS transistors, the quality factor of the load (Q_L) of inter-stage matching networks is much higher than the Q_L of the output matching network where the load is a resistance of 50Ω . Consequently, it is much more difficult to design inter-stage matching networks with small mismatch in a large bandwidth compared to output matching networks with the same bandwidth. If the inter-stage matching networks of a mm-wave PA can only provide Z_{opt} with small mismatch in part of its operating bandwidth, then the power performance of the driver stages, and consequently the power performance of the PA, will degrade obviously in the PA's operating bandwidth.

5.2.2 Mismatch and degradation of power performance

In order to know the tolerable mismatch with respect to Z_{opt} , transistors with sizes of $20\mu m$, $40\mu m$ and $90\mu m$ are simulated at $60GHz$ for their load-pull effect at their P_{1dB} . Figure 5.3(a) shows the contours of P_{out} and PAE simulated for the transistor with size of $40\mu m$ on a Smith chart. Because load-pull contours are more like ellipses [98], whereas impedances with a constant mismatch to Z_{opt} are circles on a Smith chart, impedances with the same mismatch may cause different degradations of power performance. Figure 5.3(b) plots the maximum degradation of P_{out} and PAE that may

Figure 5.3: Mismatch to Z_{opt} and the degradation of transistor power performance. (a) Load-pull simulation result of a transistor with size of $40\mu m$ at its P_{1dB} . (b) Maximum degradation of power performance that may be caused by given mismatches.

be caused by impedances with given mismatches. It can be seen that the maximum degradation of power performance caused by impedances with a given mismatch is independent of the size of the transistor, also the degradation of power performance increases rapidly as mismatch increases. For the degradation of P_{out} and PAE to be less than $0.75dB$ and 5% respectively, the mismatch with respect to Z_{opt} needs to be smaller than $-12dB$. When there is a large operating bandwidth, e.g. the $9GHz$ bandwidth of

802.11ad, maintaining mismatch below -12dB can be very challenging for the design of inter-stage matching networks with high Q_L .

5.2.3 Challenges of TMN design

During the design of a TMN, a suitable transformer need to be designed according to the given source and load so that small mismatch (e.g. <-12dB) can be achieved in the entire operating bandwidth. The design of transformer can be very flexible at mm-wave. By varying the structure of transformer, the metal layers used, the trace width and the outer-dimension of each winding, the distance between windings, and the turn number of each winding, transformers with many combinations of parameter values can be realized. Besides transformer, the matching of TMN may also be adjusted by adding an additional capacitor on the TMN's source or the load side [23, 29]. The flexibilities of transformer and the additional capacitor provide many freedoms for the design of TMN and make it possible to achieve large bandwidth for a TMN with given source and load. However, with so many possible variations, the design of TMN becomes challenging and complicated at the same time. To find a proper transformer and possibly the additional capacitor, a tremendous amount of time-consuming EM simulations are often required. To satisfy the requirement of bandwidth may need a transformer with a specific inductance, coupling coefficient and turn ratio, especially for inter-stage matching networks with high Q_L . However, the value of transformer parameters that can be realized is often limited by the given metal layers of the technology used. To address these problems, a systematic method is highly demanded for the analysis and design of TMN.

5.3 Proposed TMN Synthesizing Method

To solve the problems of TMN design and improve the power performance of wideband mm-wave PAs with TMN, this section proposes a TMN synthesizing method based on matching equations derived according to the modeling of TMN and the analysis of the TMN matching mechanism. To demonstrate the proposed TMN synthesizing method, an inter-stage matching network is designed, which achieves mismatch less than -12dB in the bandwidth of 57 to 66GHz despite a large Q_L of 6.22.

5.3.1 TMN Modeling

Figure 5.4: (a) A simplified schematic of a PA using TMNs for input, inter-stage, and output matching. (b) A TMN model including source, transformer and load.

Figure 5.4(a) shows a simplified schematic of a PA using TMNs for input matching, inter-stage matching, and output matching. Resistors and capacitors in gray lines are used to represent the source and load impedance of each matching network,

which can be transistor input/output impedance, the 50Ω source/load of a PA, or possibly some capacitance that is additionally added. Figure 5.4(b) gives a model of TMNs used for the matching analysis. The model of transformer included in Figure 5.4(b) is based on the model reported in [49], in which L_{TP} is the primary winding inductance, k is the magnetic coupling coefficient between primary and secondary, n is the turn ratio defined by $n = \sqrt{L_{TS}/L_{TP}}$ (L_{TS} is the secondary winding inductance), R_{TP} and R_{TS} are parasitic resistances of the primary and the secondary windings respectively. The transformer circled by blue dashed line in Figure 5.4(b) is an ideal transformer with turn ratio of $1:n/k$. C_{TP} and C_{TS} are two capacitors representing the parasitic capacitances of a transformer.

It is worth to note that no center-tap is used for the transformer in the TMN model, and the effects of all the parasitic capacitances of transformer including inter-winding capacitance, winding to substrate capacitance and winding-self capacitance are contributed to C_{TP} and C_{TS} . To do such simplification without losing the model's accuracy for matching analysis, the miller effect of inter-winding parasitic capacitance has been considered. As shown in Figure 5.4(a), when used in different matching networks, the connections of transformers are different. In inter-stage matching networks, the two windings of transformer are both connected differentially with center-taps being AC-ground. In input or output matching networks, the transformer is used as a balun in which one winding is connected differentially with center-tap being AC-ground, while the other winding is connected to a single-ended 50Ω impedance with center-tap being floating. In these different connections, the voltage distribution on the two windings of transformer are also different, causing a variation of the equivalent capacitances at the two ports of transformer (C_{TP} and C_{TS}) due to the miller effect of inter-winding parasitic capacitance. To maintain the TMN model simple

while taking this phenomenon into consideration, the transformer model included in Figure 5.4(b) is adopted while the value of model parameters are extracted for each connection separately. Because the effects of inter-winding parasitic capacitances are contributed to C_{TP} and C_{TS} , there is relatively large variation of their values when connection changes. Other parameters including L_{TP} , k , n , R_{TP} , and R_{TS} also have small variations caused by skin effect and proximity effect [111] as the voltage distribution changes in transformer. Compared to other transformer models including center-tap and inter-winding parasitic capacitances [49, 112, 113], the model in Figure 5.4(b) contains much less parameters and allows easier analysis of TMN matching.

The source and load of a TMN are all simplified as R and C in parallel in the model. To accurately model MOS transistors in a large bandwidth, generally the output impedance of a transistor is modeled as R and C in parallel, but the input impedance is modeled as R and C in series. In order to simplify the TMN model for matching analysis, in this chapter the series RC model of MOS transistor input is converted to a parallel RC model as well [51], such that the parasitic capacitance of transistors and the parasitic capacitance of transformer are connected in parallel and can be viewed as one capacitor. The conversion introduces no error to the calculation of transformer parameters for matching, as long as the conversion is performed at the same frequency where the transformer parameters are calculated.

5.3.2 Matching mechanism and matching equations of TMN

In Figure 5.5 the TMN model is redrawn for the analysis of matching. As described in section 5.2, the target of the inter-stage matching networks and the output matching network of a mm-wave PA is to provide Z_{opt} for the transistors they are connect to. With R_S and C_S retrieved according to the load-pull simulations of transistors, the

target of providing Z_{opt} is equivalent to achieving reflection coefficient $\Gamma_S=0$ in Figure 5.5. It is worth noting that $\Gamma_S=0$ is also the target of an input matching network, except that R_S is a 50Ω resistance in an input matching network.

Figure 5.5: The model of TMN redrawn for matching analysis.

Figure 5.6: Matching mechanism of TMN represented on a Smith chart.

Because the source side of a matching network is either the output of transistors or a 50Ω resistance, it is expected that Q_S of a TMN is much lower than Q of the transformer in practical designs. Therefore, the matching of a TMN is almost not affected by the parasitic resistance R_{TP} on the source side, and there is

$$|\Gamma_S| \approx |\Gamma'_S|. \quad (5.3)$$

As shown in Figure 5.5, when the TMN model is separated into two parts from the Γ'_S reference plane, the left part contains only parameters L_{TP} and k of the transformer, while the parameter n appears only in the ideal transformer contained in the right part. Because ideal transformers only change the magnitude of impedance while keeping the ratio between the imaginary part and real part a constant, when the TMN in Figure 5.5 is matched in conjugate, there is

$$Z_{Left} = Z_{Right}^* \quad (5.4)$$

$$\bar{Q}_{Left} = -\bar{Q}_{Right} = -\bar{Q}_{Right_BT} \quad (5.5)$$

in which the parameter $\bar{Q}$ is defined as the ratio between the imaginary part and the real part of any impedance Z .

$$\bar{Q} = \text{Im}(Z) / \text{Re}(Z) \quad (5.6)$$

$\bar{Q}$ has the same magnitude as the quality factor Q of an impedance, and the difference is that Q is always positive ($\text{Im}(Z) \neq 0$) but $\bar{Q}$ can be positive or negative, corresponding to Z being inductive or capacitive.

The mechanism for TMN to realize matching, as shown in Figure 5.6, can be viewed as accomplished in two steps:

Step 1: $\bar{Q}$ of $R_S \parallel (C_S + C_{TP}) + R_{TP}$ is changed by inductors $L_{TP}(1-k^2)$ and $L_{TP}k^2$, such that $\bar{Q}_{Left} = -\bar{Q}_{Right}$

This step is shown in Figure 5.6 by the red line and the green line. It requires the value of k to be selected correspondingly for each value of L_{TP} . The solution of equation (5.5) gives the first matching equation of TMN as shown by (5.7), in which $Q_S = \omega_0 R_S C_S$ and $Q_L = \omega_0 R_L C_L$.

$$k = \sqrt{\frac{(R_L + R_{TS} + Q_L^2 R_{TS})(C_S(R_S + R_{TP})^2 + Q_S^2(R_{TP}^2 C_S - 2L_{TP}) + \omega_0^2 L_{TP}^2 C_S(1 + Q_S^2))}{L_{TP}(\omega_0 Q_L R_L C_S(R_S + R_{TP} + Q_S^2 R_{TP}) + (R_L + R_{TS} + Q_L^2 R_{TS})(\omega_0^2 L_{TP} C_S(1 + Q_S^2) - Q_S^2))}} \quad (5.7)$$

Step 2: The magnitude of Z_{Right} is adjusted by the ideal transformer such that

$$Z_{Left} = Z_{Right}^*$$

As the blue line in Figure 5.6 shows, in step 2 the impedance is changed along a constant Q curve on Smith chart, which is also a constant $\bar{Q}$ curve. With a turn ratio of $1:n/k$ for the ideal transformer, the impedances are changed such that:

$$\frac{Z_{Right}}{Z_{Right_BT}} = \left(\frac{n}{k}\right)^2. \quad (5.8)$$

Solving equations (5.4) and (5.8) gives the second matching equation of TMN as shown by (5.9).

$$n = \sqrt{\frac{C_L R_L^2 (R_S + R_{TP} + Q_S^2 R_{TP}) + L_{TP} (1 + Q_S^2) (R_L + R_{TS} + Q_L^2 R_{TS}) - C_S R_S^2 (R_L + R_{TS} + Q_L^2 R_{TS})}{L_{TP} (1 + Q_L^2) (R_S + R_{TP} + Q_S^2 R_{TP})}} \quad (5.9)$$

For each value of L_{TP} , a corresponding value of n is to be selected so that the TMN is matched. Specially, if $R_{TP}=R_{TS}=0$, the two matching equations can be simplified as

$$k = \sqrt{\frac{R_S^2 - 2\omega_0 Q_S R_S L_{TP} + \omega_0^2 (1 + Q_S^2) L_{TP}^2}{\omega_0 R_S (Q_L - Q_S) L_{TP} + \omega_0^2 (1 + Q_S^2) L_{TP}^2}} \quad (5.10)$$

$$n = \sqrt{\frac{R_L / (1 + Q_L^2)}{R_S / (1 + Q_S^2)} + \frac{R_L (Q_L - Q_S)}{\omega_0 L_{TP} (1 + Q_L^2)}}. \quad (5.11)$$

Because k can never be larger than 1 in practical designs, the value of L_{TP} needs to be larger than a minimum value given by (5.12) if R_{TP} and R_{TS} are not zero, or simplified as in (5.13) if $R_{TP}=R_{TS}=0$.

$$L_{TP_min} = \frac{C_S \left(R_S^2 + 2R_S R_{TP} + (1 + Q_S^2) R_{TP}^2 \right) (R_L + R_{TS} + Q_L^2 R_{TS})}{Q_S^2 (R_L + R_{TS} + Q_L^2 R_{TS}) + \omega_0 C_S Q_L R_L (R_S + R_{TP} + Q_S^2 R_{TP})} \quad (5.12)$$

$$L_{TP_min} = \frac{R_S}{\omega_0 (Q_S + Q_L)} \quad (5.13)$$

With matching equations (5.7) and (5.9), the required k and n for each value of L_{TP} can be directly calculated. By using a CAD software (e.g. Agilent ADS), the bandwidth of TMN with $|\Gamma_S|$ smaller than a specific value can be calculated and compared for transformers with all possible values of L_{TP} and the corresponding values of k and n . The solutions of TMN can then be selected according to the required bandwidth and possibly other considerations. A method to synthesize TMN can be developed, enabling the transformer and the additional capacitor to be designed systematically, and facilitating mm-wave PAs with TMNs to achieve good power performance in a large operating bandwidth.

5.3.3 TMN synthesizing Procedure

Figure 5.7 shows the design flow of the proposed TMN synthesizing method, by which a transformer with suitable structure and size, and the additional capacitor that may be added on the source or the load side of a TMN, can be designed systematically according to the required bandwidth of a mm-wave PA.

When designing transformers according to the calculated values of L_{TP} , k and n , normally the structure of the transformer is mostly determined by the value of k , while the size and the turn number of each winding are mostly determined by the value of L_{TP} and n . Depending on the metal layers available in the used technology, it may be difficult to realize some values of parameters. In such cases, an additional capacitor can be added on the source or the load side of the TMN and its value can be adjusted so that a solution that is easier to realize can be selected. A more flexible realization of

the selected L_{TP} , k and n is to connect an inductor in series with a transformer. This method will be shown in Section 5.4 for the design of the input matching network of a 60GHz PA.

Figure 5.7: Flow chart of TMN synthesizing based on the derived matching equations of TMN.

It is worth to note that at the beginning of TMN synthesizing, the parasitics of transformer including R_{TP} , C_{TP} , R_{TS} , C_{TS} are unknown. To calculate k and n , some

typical values are assumed for these parasitics at the beginning due to their relatively small variation and small effects on TMN matching compared to those of L_{TP} , k , and n . To ensure the differences between the parasitics used for calculation and the parasitics of the synthesized transformer are small, iteration may be required for several times by using the parasitics of the designed transformer for the next round of calculation.

To demonstrate the proposed TMN synthesizing method, assume an inter-stage matching network of a 60GHz PA is to be designed for which the related transistors are modeled as $R_S=110\Omega$, $C_S=31.5\text{fF}$, $R_L=202\Omega$, $C_L=75.6\text{fF}$. From EM simulations and the modeling of transformers for 60GHz PAs, it is known that the typical values of parasitics for transformers used in 60GHz PAs in a con-centric architecture are $R_{TP}=2.5\Omega$, $R_{TS}=1.5\Omega$, $C_{TP}=C_{TS}=5\text{fF}$ when both windings are differentially connected.

By using matching equations (5.7) and (5.9), the required k and n are calculated for L_{TP} in the range of 40 to 200pH and plotted in Figure 5.8. Based on the calculated k and n , the bandwidth of the TMN for $|\Gamma_S|<-12\text{dB}$ is simulated in a CAD software and plotted in Figure 5.9. for transformers with L_{TP} in the same range. With no additional capacitor added, a TMN with $L_{TP}=136\text{pH}$, $k=0.37$, $n=0.78$ can achieve a bandwidth of 9GHz with $|\Gamma_S|<-12\text{dB}$. With $n\neq 1$ and a relatively small value of k , designing a transformer in con-centric architecture can be a good choice. In such a transformer, the trace width and the gap between windings can be adjusted to achieve a wide range of n and k . However, for the calculated solution with $n=0.78$, the inductance of the two windings have the relationship of $L_{TS}=0.78^2\times L_{TP}=0.61L_{TP}$, requiring a large gap between the two windings to generate this inductance difference. Such a large gap reduces the coupling between the two windings, and value of k that can be realized is much smaller than 0.37.

Figure 5.8: k and n calculated according to matching equations (5.7) and (5.9) for L_{TP} of 40 to 200pH.

Figure 5.9: Bandwidth with $|\Gamma_S| < -12\text{dB}$ for L_{TP} of 40 to 200pH. Adding of a 10fF capacitor on the source side makes the calculated parameters easier to realize.

To make the selected parameters easier to realize, a 10fF capacitor is added on the source side, resulting $C_S = 31.5\text{fF} + 10\text{fF} = 41.5\text{fF}$. With the new value of C_S , the corresponding value of k and n is re-calculated for each L_{TP} , and the 9GHz bandwidth for $|\Gamma_S| < -12\text{dB}$ can be satisfied by a new solution with $L_{TP} = 112\text{pH}$, $k = 0.35$, $n = 0.85$. According to the metal layers available in the technology as shown in Figure 5.10(a), a

con-centric transformer with $L_{TP}=114.7\text{pH}$, $k=0.33$, $n=0.85$, $R_{TP}=2.5\Omega$, $R_{TS}=1.4\Omega$, $C_{TP}=4.5\text{fF}$, $C_{TS}=4.1\text{fF}$ is designed. Figure 5.10(b) shows the 3D structure of the transformer, which has $OD=88\mu\text{m}$, $W_1=8\mu\text{m}$, $W_2=10\mu\text{m}$ and $Gap=7\mu\text{m}$. To reduce the transformer's parasitic resistances, the top two thick metal layers available in the technology are used together to construct the transformer. The design of the transformer is adjusted such that its L_{TP} , k and n to approach the selected values as much as possible. The difference between the parasitics of the transformer and the parasitics used for calculation are very small, requiring no iterations to be performed.

Figure 5.10: (a) Metal layers available in the used 65nm CMOS technology. (b) Con-centric transformer designed for the TMN synthesizing example.

Figure 5.11 plots the simulated S-parameters of the synthesized TMN, in which the S-parameters of the EM-simulated transformer are represented by the solid lines and the S-parameters of the TMN model with parameter values extracted from the designed transformer are represented by the dashed lines. As shown in the figure, the TMN model agrees well with EM simulation, and the synthesized TMN has achieved $|\Gamma_s| < -12\text{dB}$ from 56.8 to 66.1GHz with 9.3GHz bandwidth (shaded area). By using the proposed TMN synthesizing method, the transformer including its structure and size, the value of the added capacitor, are all determined systematically according to the required bandwidth. A tremendous amount of time-consuming EM-simulations are

avoided because the selected values of L_{TP} , k and n provide enough information to design the structure and size of the transformer. The required bandwidth of 57 to 66GHz in which $|\Gamma_s| < -12\text{dB}$ is successfully achieved despite a large Q_L of 6.22 ($Q_L = 2\pi \times 61.5\text{GHz} \times 202\Omega \times 79.7\text{fF}$).

Figure 5.11: Simulated S-parameters of the TMN matched by the synthesized con-centric transformer.

Figure 5.12: Simulated S-parameters of the TMN matched by a stacked transformer ($n=1$).

As a comparison, Figure 5.12 shows the S-parameters simulated for another solution with $n=1$ for the same source and load. Without using the proposed TMN

synthesizing method, a solution with $n=1$ is highly possible to be used because it can be realized by transformers in stacked structure, which is a structure widely used by transformers in mm-wave PAs [23, 28, 93, 107]. The solution with $L_{TP}=68\text{pH}$, $k=0.68$, $n=1$ is represented by the gray point in Figure 5.9. Such a transformer is able to match the given source and load well at 61.2GHz, but the bandwidth for $|\Gamma_S|<-12\text{dB}$ is only 5.5GHz (shaded area). If this solution is selected for the inter-stage matching of a 60GHz PA, the PA would show obviously larger degradation of power performance in the 9GHz bandwidth compared to a PA with the synthesized inter-stage matching network.

5.4 A 60GHz PA with Synthesized TMNs

In this section, a 60GHz PA is designed in a 65nm bulk CMOS technology using the proposed TMN synthesizing method. To achieve good power performance from 57 to 66GHz, the PA is designed with $|\Gamma_S|<-12\text{dB}$ for inter-stage matching networks and $|\Gamma_S|<-18\text{dB}$ for the output matching network in the 9GHz bandwidth.

Figure 5.13 shows the schematic of the designed PA. The PA contains 3 stages to achieve a total gain of around 20dB. In each stage, the transistors and their connections are shown in Figure 5.14. Transistors M_1 and M_2 are used for signal amplifying and are connected as common source, while transistors $M_{\text{neu}1}$ and $M_{\text{neu}2}$ are used to neutralize the C_{GD} of M_1 and M_2 so that the PA is unconditionally stable [25]. Because the value of C_{GD} equals to that of C_{GS} for transistors $M_{\text{neu}1}$ and $M_{\text{neu}2}$, the optimal size of $M_{\text{neu}1}$ and $M_{\text{neu}2}$ is around half the size of M_1 and M_2 . The size of $M_{\text{neu}1}$ and $M_{\text{neu}2}$ for each stage is selected as shown in Figure 5.14 according to S-parameter simulation, corresponding to the minimum $|S_{12}|$ of each stage. Compared to neutralization with metal capacitors, the capacitance of $M_{\text{neu}1}$ and $M_{\text{neu}2}$ can track C_{GD} of M_1 and M_2 under

Figure 5.13: Schematic of the 60GHz PA.

PVT variation, enhancing the stability of the PA and reducing its gain variation under PVT variation [94]. The bias voltage is applied to transistors M_1 and M_2 through resistors R_1 , R_2 and the secondary winding of transformers used in the matching circuits. Compared with applying bias voltages through the center-taps of transformer, the common mode stability of the PA is improved by keeping the center-taps of transformers floating in the PA's inter-stage matching networks [28]. The PA operates with a supply voltage of 1.2V. The transistors used for signal amplifying are biased with a current density of $0.35\text{mA}/\mu\text{m}$, so that the f_T of transistors are optimum and the linear output power of the PA is maximized.

Figure 5.14: Connections and transistor sizes of active stages.

After the design of active stages, each of them is simulated for the input and output impedances and then modeled as R and C in parallel. Following the TMN synthesizing flow chart given in Figure 5.7, each matching network is calculated for the parameter values of L_{TP} , k and n that can realize matching using the derived matching equations of TMN and selected according to the required bandwidth of 57 to 66GHz. Based on the thick metal layers available in the used CMOS technology, transformers are then built with parameter values and 3D structures shown in Figure 5.13. When the selected L_{TP} , k and n are difficult to realize, either an additional capacitor is added on one side

of the TMN or a series connection of transformer and inductor is used to realize a wider range of parameter values for transformer.

Figure 5.15: $|\Gamma_s|$ of synthesized TMNs in the 60GHz PA.

For the design of the output matching network, benefitting from the low Q of source and load ($Q_s=1.42$, $Q_L=1.07$), a bandwidth of 9GHz with $|\Gamma_s| < -12\text{dB}$ or even lower can be achieved with a wide range of L_{TP} . In such a case, transformers in stacked structure are selected due to their advantage of low insertion loss [93]. According to the synthesized TMN parameters, a 34fF capacitor is added on the load side, and a transformer is constructed in stacked structure using the top two thin metal layers which have a distance of $1.45\mu\text{m}$ between them. From 57 to 66GHz, the output matching network achieves small mismatch of $|\Gamma_s| < -18\text{dB}$ as shown in Figure 5.15. The matching network has an insertion loss of only 0.82 to 0.89dB due to the stacked architecture used.

For the design of the two inter-stage matching networks, because of the high Q of the load ($Q_s=2.45$, $Q_L=5.93$ for the inter-stage matching network between stage 1 and stage 2, $Q_s=1.96$, $Q_L=6.22$ for the inter-stage matching network between stage 2 and

stage 3), the value of L_{TP} has to be selected carefully such that $|\Gamma_S| < -12\text{dB}$ are satisfied in the 9GHz bandwidth. The design of the inter-stage matching network between stage 2 and 3 has been explained in Section 5.2 in the TMN synthesizing example. For the inter-stage matching network between stage 1 and 2, a con-centric transformer is used as well. The large value of L_{TP} of this transformer is realized by using two turns for the primary winding.

The input matching network of the PA is designed using the same method but with frequency shifted intentionally such that the 3dB bandwidth of the PA covers the required frequency range of 57 to 66GHz and has some safety margin. Because of the small value of L_{TP} whereas relatively large value of k and n required, the transformer of the input matching network is realized by a strongly coupled transformer in stacked architecture and an inductor which is connected in series. Constructed using two metal layers which have a distance of only $0.6\mu\text{m}$ between them, the transformer has parameters of $L_{TP}=64.9\text{pH}$, $k=0.74$, $n=1.02$. After an inductor is connected in series on the secondary side of the transformer, the transformer and the inductor is equivalent to a new transformer whose parameters L_{TP}' , k' , and n' are given by

$$L_{TP}' = L_{TP} \quad (5.14)$$

$$k' = \frac{L_{TP}kn}{\sqrt{L_{TP}(L_{TP}n^2 + L_{addS})}} \quad (5.15)$$

$$n' = \sqrt{\frac{L_{TP}n^2 + L_{addS}}{L_{TP}}}. \quad (5.16)$$

With an inductor $L_{addS}=143\text{pH}$ added, the modeled parameters of the newly equivalent transformer are $L_{TP}'=64.9\text{pH}$, $k'=0.45$, $n'=1.74$.

Simulations show that the designed PA achieves a peak gain of 21.7dB and the 3dB bandwidth of the PA is 10.6GHz covering from 56.1 to 66.7GHz. In the

bandwidth of 57 to 66GHz, the simulated P_{SAT} is 14.2 to 14.5dBm and the simulated peak PAE is 20.5% to 23.6%, achieving the design target of maintaining good power performance in all the 9GHz bandwidth. By using the proposed TMN synthesizing method, the matching networks of the PA are designed systematically. The TMN synthesizing method is very important for the inter-stage matching networks to achieve small mismatch of $|\Gamma_S| < -12\text{dB}$ in the required bandwidth.

5.5 Measurement Results

Figure 5.16: Photomicrograph of the 60GHz PA.

Fabricated in a 65nm bulk CMOS process, the PA occupies a core area of 0.088 mm² and a total area of 0.22 mm² including pads. Figure 5.16 shows its photomicrograph. Measurements of the PA are performed using on-wafer probing at room temperature.

The PA is firstly measured for its S-parameters from 10MHz to 67GHz using an Agilent vector signal analyzer N5247A and the measured result is shown in Figure 5.17. With a power supply of 1.2V and a DC current of 105mA, the PA is measured with a maximum S_{21} of 20.9dB at 61.7GHz. A 3dB bandwidth of 9.7GHz extending from 57.2 to 66.9GHz is achieved. From 57 to 66GHz, the measured S_{11} of the PA is

below -13.5dB and S_{22} is below -8.2dB. As shown in Figure 5.17, good agreement is achieved between the measured and the simulated S-parameters. In the frequency range of 10MHz to 67GHz, the stability factor (K) of the PA is larger than 12.6, showing that the PA is unconditionally stable.

Figure 5.17: S-parameters and stability factor (K) of the PA.

The PA is then characterized for its large signal behavior from 57 to 66GHz in steps of 1GHz. R&S power meter NRP-Z57, which has an uncertainty less than 0.248dB below 67GHz for the measurement, is used to calibrate the PA's input power and measure its output power. As shown in Figure 5.18 and Figure 5.1(b), the PA is measured with P_{1dB} of 10.81 to 11.68dBm, P_{SAT} of 13.94 to 14.35dBm, and peak PAE of 18.9% to 21.1% from 57 to 66GHz. Benefiting from matching networks designed using the proposed TMN synthesizing method, the output power is degraded by only 0.87dB for P_{1dB} and 0.41dB for P_{SAT} , and the minimum peak PAE of the PA is as high as 89.6% of the maximum peak PAE. Figure 5.19 depicts the measured gain, output power and PAE of the PA at 61GHz. Because the driving power is improved by using the proposed TMN synthesizing method, the P_{1dB} of the PA is only 2.67dB lower than

P_{SAT} and the PAE at P_{1dB} is 12.2%. Due to the limitation of the driving power of VNA, the AM-PM of the PA is not measured. Figure 5.19 shows the simulated AM-PM of the PA at 61GHz, which is around -1.35° at P_{SAT} .

Figure 5.18: Measured P_{1dB} and P_{SAT} from 57 to 66GHz, and measured P_{out} of a 16QAM modulated signal with EVM of 8.91% in the 4 channels of 802.11ad.

Figure 5.19: Measured gain, output power and efficiency of the PA at 61GHz, and the simulated AM-PM of the PA at 61GHz.

Besides frequency, the temperature is another important factor which will affect the PA's performance. Figure 5.20 shows the simulated P_{SAT} and PAE of the PA at

61GHz with the variation of temperature. In the commercial temperature range of 0 °C to 85 °C, the simulated P_{SAT} is 14.73dBm to 14.07dBm, and the simulated PAE is 24.2% to 21.2%. Such variations are comparable or smaller compared to the temperature variation of reported 60GHz PAs [107] [80] and [114], and are believed to have benefitted from the design of inter-stage matching networks which improves the driving power of the PA and a bias circuit (same as the one shown in Figure 4.17) which ensures an almost constant bias current over temperature.

Figure 5.20: Simulated P_{SAT} and PAE of the PA with the variation of temperature.

To measure the PA's capability of delivering modulated signal, a signal with modulation of 16QAM and a symbol rate of 1.76GS/s is applied to the PA using an equipment setup as shown in Figure 5.21. By changing the attenuation of the variable attenuator connected at the PA's input, the input power of the PA is varied and the EVM corresponding to different output power is measured at the 4 channels of 802.11ad. Figure 5.22 shows the measured EVM at different power back-offs from P_{SAT} at channel 2. The center frequency of the channel is 60.48GHz. With an EVM of 8.91% (-21dB), which is the requirement for 802.11ad to support a data-rate of

Figure 5.21: Equipment setup for EVM measurement.

Figure 5.22: Measured EVM for 16QAM modulated signal at different power back-offs from P_{SAT} at 60.48GHz.

4.62Gbps, the PA is capable of delivering an output power of 11.1dBm (3.3dB power back-off) with PAE of 10.7%. For all the 4 channels of 802.11ad, the EVM of 8.91% is supported by the PA with output power of 10.8 to 11.1dBm (as shown in Figure 5.18) and PAE of 10.1% to 10.7%, further demonstrating the PA's capability of maintaining good power performance in the entire operating bandwidth.

The PA's performance is summarized in Table 5-1 and compared to other recently reported CMOS PAs at 60GHz with TMNs. It can be seen that the degradation of power performance in the operating bandwidth and the CMOS technologies used are

Table 5-1

PERFORMANCE COMPARISON OF THE DESIGNED PA AND OTHER 60GHz CMOS PAs WITH TMNs

Ref.	Pub.	Power performance from 57 to 66GHz*						Gain (dB)	BW (GHz)	VDD (V)	Tech (nm)	Active area (mm ²)
		P _{SAT_MAX} (dBm)	Δ P _{SAT} (dB)	P _{1dB_MAX} (dBm)	Δ P _{1dB} (dB)	PAE _M AX (%)	$\frac{\text{Min(peak PAE)}}{\text{Max(peak PAE)}}$ (%)					
[23]	JSSC 2009	11	4.2 [†]	-	-	14.6	41.1 [†]	13.8	-	1.0	90 nm	0.22 [#]
[24]	JSSC 2009	12.5	2 [†]	10.2	-	19.3	38.9 [†]	15	-	1.2	90 nm	0.15
[25]	JSSC 2010	11.5	3	5	-	15.2	65.8	16	>8.5	1.0	65 nm	0.053
[26]	ESSCI RC 2014	20.2	1.2	17.4	2	22.9	67.7	33	9	1.2	65 nm	0.32
[27]	ISSCC 2014	16.4	1.4	13.9	3.9	23	69.6	22.4	-	1.8	40 nm	0.081
[28] **	JSSC 2013	17.4	0.8	14.1	3.4	28.5	80.4	21.2	5.5	1.0	40 nm	0.074
[29]	TCAS-I 2014	16.5	1.5 [†]	11.7	4.7 [†]	12.6	67.5 [†]	24.4	11	2.1	28 nm	0.122
[30]	ISSCC 2015	19.1	2.1	18.6	2	21.5	70.7	15.4	>8	1.0	28 nm SOI	0.16
This work		14.35	0.41	11.68	0.87	21.1	89.6	20.9	9.7	1.2	65 nm	0.088

*Data of [23, 24, 26, 30] is for bandwidth of 57 to 65GHz; data of [25] is for bandwidth of 58 to 65GHz; data of [27] is for bandwidth of 59 to 67GHz

**PAE from 57 to 66GHz of [28] is obtained from [115] in its Class-A mode

[†]Estimated from graphic

-Data not provided

[#]Area including pads

highly related in the reported 60GHz PAs. For example, the ratio of the minimum peak PAE over the maximum peak PAE in the 9GHz bandwidth is improved from around 40% for 60GHz PAs in 90nm CMOS [23, 24], to around 65% for 60GHz PAs in 65nm CMOS [25, 26], and to around 70% for 60GHz PAs in 40/28nm CMOS [27-30]. The improvement is largely contributed by the increased gain of transistors at mm-wave frequency in more advanced CMOS technologies. However, by using the proposed TMN synthesizing method to design the inter-stage matching networks and the output

matching network with small mismatch in the 9GHz bandwidth, the 60GHz PA designed in a 65nm bulk CMOS technology has achieved the smallest degradation of P_{SAT} , P_{1dB} and peak PAE, even compared to other works in more advanced technologies.

5.6 Summary

Based on the modeling and the analysis of the matching mechanism of TMN, the matching equations of TMN are derived and a method to synthesize TMN according to the required bandwidth is proposed in this chapter. Both the inter-stage matching networks and the output matching network of mm-wave PAs can be designed with small mismatch with respect to Z_{opt} in a large bandwidth, enabling wideband mm-wave PAs to achieve good power performance in its entire operation bandwidth.

A 60GHz PA is designed in a 65nm bulk CMOS technology using the proposed TMN synthesizing method for the application of 802.11ad in the next generation of WLAN. From 57 to 66GHz, the PA is measured with small degradations of 0.87dB for P_{1dB} and 0.41dB for P_{SAT} , and the minimum peak PAE is as high as 89.6% of the maximum peak PAE. The PA is able to support the 4 channels of 802.11ad with output power of 10.8 to 11.1dBm and PAE of 10.1% to 10.7% when EVM is 8.91% (-21dB).

Chapter 6

Conclusions and Future Works

6.1 Conclusions

This thesis presents the design of PAs for the next generation of WLAN which includes the operation at 2.4GHz, 5GHz, and 60GHz. The main targets of the thesis include the design of a wideband PA to support WLAN at both the 2.4GHz band and the 5GHz band so as to reduce the circuit area, cost, and the complexity of the RF system for WLAN at these two frequency bands, and the design of a 60GHz PA with good power performance in the entire bandwidth of 57 to 66GHz so that all the 4 channels of 802.11ad can be well supported.

In Chapter 2, WLAN standards at the 2.4GHz band and the 5GHz band are introduced, followed by a study of techniques to design wideband matching networks and to reduce the non-linearity of PAs. A review of recently reported PAs for WLAN, and a review of wideband PAs are also included. The studied techniques are used in Chapter 4 of this thesis, for the design of a wideband PA to support WLAN at both the 2.4GHz band and the 5GHz band with reduce area, cost and complexity of the RF system.

In Chapter 3, the design of 60GHz PAs for 802.11ad is reviewed. At such a high frequency, the characteristics of transistors and the design of matching networks both highly affect the performance of PAs. 60GHz PAs in state-of-the-art with LC matching, transmission line matching, and transformer matching are all examined, showing that transformer-based matching networks are the most suitable for mm-wave PAs. Reported design methods of TMN are summarized, and the challenge of large in-band degradation of 60GHz PAs is also briefly discussed.

In Chapter 4, the design of a Class-AB PA with a 2-to-6GHz bandwidth to support WLAN at the 2.4GHz and 5GHz bands is introduced in detail. The PA is firstly designed for the matching of fundamental using traditional wideband matching techniques, then by utilizing the characteristics of differential circuit and transformer, the wideband matching for 2nd harmonic is added to the matching network without affecting the wideband matching designed for fundamental. From 2 to 6GHz, the PA achieves a peak PAE of 28.4% and an overall PAE above 19%, which is comparable to the PAE of reported WLAN PAs designed separately for WLAN at the 2.4GHz and 5GHz bands. From 2 to 6GHz, the PA is capable of delivering 11.12 to 13.21dBm and 9.31 to 11.31dBm of output power for 802.11n signals with 64QAM modulation at the EVM of -28dB and 802.11ac signals with 256QAM modulation at the EVM of -32dB respectively, demonstrating the capability of supporting WLAN at both the 2.4GHz band and the 5GHz band.

In Chapter 5, a 60GHz PA is designed to support 802.11ad, in which the challenge of maintaining good power performance in a large bandwidth at mm-wave frequency is addressed. By using a TMN synthesizing method which is proposed based on the derived matching equations of TMN, the inter-stage matching and output matching of the 60GHz PA are both designed with small mismatch in the entire bandwidth.

Designed in a 65nm bulk CMOS process, the PA is measured with small degradations of 0.87dB for P_{1dB} and 0.41dB for P_{SAT} , and the minimum peak PAE is as high as 89.6% of the maximum peak PAE in the bandwidth of 57 to 66GHz. The PA can support the 4 channels of 802.11ad with output power of 10.8 to 11.1dBm and PAE of 10.1% to 10.7% when EVM is 8.91% (-21dB).

6.2 Future Works

PAs in Class-AB and inverse Class-D both require a real load impedance at fundamental and short circuits at all harmonics [116, 117]. By using the wideband matching method given in Chapter 4 of this thesis, a real load impedance at fundamental and a impedance close to a short circuit at 2nd harmonic can be realized in a large bandwidth. Considering the capacitance (including parasitic) at transistor drain output, the load impedances at the 3rd and above harmonics can be close to short circuits as well. Therefore, the matching technique described in Chapter 4 can be further extended and used to design wideband PAs in inverse Class-D. As CMOS technology develops, integrated inverse Class-D PAs are able to achieve higher and higher efficiency and can be used as unit cells to construct digital PAs for WLAN at the 2.4GHz and 5GHz bands [21, 22, 118]. When compared to PAs in Class-AB, digital PAs have higher efficiency, especially at a large power back-off. If the proposed matching technique is applied to digital PAs to improve their bandwidth, then it is possible that multiple standards can be supported by one digital PA, achieving very high efficiency and small circuit area.

To further improve the efficiency of 60GHz PAs when delivering a modulated signal, it would be beneficial if pre-distortion can be used in future works. At mm-wave frequency, it is very challenging for PAs to generate large output power with

high efficiency. If pre-distortion can be used so that the EVM-compliant output power can be further increased towards P_{SAT} , then the efficiency of the transmitter can be greatly improved [\[119\]](#). It is worth noting that due to the large channel bandwidth of 802.11ad, digital pre-distortion would be difficult to realize while analog pre-distortion would be a more feasible choice.

List of Publications

W. Ye, K. Ma, K. S. Yeo, and Q. Zou, "A 65 nm CMOS Power Amplifier With Peak PAE above 18.9% From 57 to 66 GHz Using Synthesized Transformer-Based Matching Network," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 10, pp. 2533-2543, Oct. 2015.

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