Data converters using continuous time sigma delta modulators with VCO-based integrator and quantizer for ultra low power applications

Neelakantan Narasimman

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DATA CONVERTERS USING CONTINUOUS
TIME SIGMA DELTA MODULATORS WITH
VCO-BASED INTEGRATOR AND QUANTIZER
FOR ULTRA LOW POWER APPLICATIONS**

**NEELAKANTAN NARASIMMAN
SCHOOL OF ELECTRICAL AND
ELECTRONIC ENGINEERING**

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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2017

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Abstract

Ultra-low power operation is highly desirable for circuits and systems, which run on strict power budgets. The demand has increased with the rise in applications, which work on harvested energy such as autonomous sensor nodes. Data converters are an inevitable part of sensor interface systems and high-performance communication circuits used in various biomedical and portable computing applications. Among different variants of data converters available, the ones using continuous time $\Sigma\Delta$ modulators are extremely popular for achieving high resolution with excellent energy efficiency. Nevertheless, with technology/supply voltage scaling, prominence of second order effects and the absence of voltage headroom have made the design of traditional $\Sigma\Delta$ modulators challenging. VCO-based ADC is a promising solution to address this problem. Since CMOS inverter based ring oscillator is used as VCO, analog information is contained in the phase/frequency of the oscillations. Thus, quantization is performed in the time domain as opposed to voltage domain in the conventional quantizer. Since continuous scaling of the CMOS technology aids the digital nature of the circuit components, VCO-based ADCs form excellent candidates for ultra-low voltage operation and could be used as either quantizer or integrator in a continuous time $\Sigma\Delta$ modulator. However, VCO-based ADCs have various challenges for achieving ultra-low power targets, such as small voltage margin, noise, and nonlinearity.

This thesis focuses on the design and development of data converters using continuous-time $\Sigma\Delta$ modulators with VCO-based integrator/quantizer for ultra-low power applications. Firstly, existing architectures and designs for VCO-based ADCs and other ultra-low voltage $\Sigma\Delta$ modulators are carefully analyzed. Solutions

proposed in the thesis are broadly divided into three parts that include design, analysis and measurement results of three test chips.

I- Open loop First order $\Sigma\Delta$ modulator using VCO-Frequency Delta Sigma Modulators (FDSM)

VCO-based ADC, when employed in the open-loop configuration, gives first order noise shaping for the quantization noise. However, the non-linear voltage to frequency tuning characteristics of a VCO adds distortions at the output. While pseudo-differential operation could correct the even order distortions, odd order harmonics are difficult to remove. This chapter presents a calibration scheme to correct odd order harmonics for realizing a linear open loop VCO-based ADC. The proposed calibration scheme uses digital background calibration architecture operating at ultra-low supply voltages. A replica VCO is used to calibrate the nonlinearity, and a lookup table, in the signal path, is filled with corrected values. The proposed calibration method is at least 256 times faster than other state-of-the-art ones. A prototype design was fabricated in commercial 65nm CMOS technology. Measurement results show that the proposed calibration technique improves the SNDR of the open loop VCO-based ADC from 42dB to 55dB over 10 KHz signal bandwidth while consuming 1.15 μ W power.

II - Closed loop first order $\Sigma\Delta$ modulator using VCO as an Integrator

The performance of an open loop VCO-FDSM is limited by the amount of Nonlinearity correction it can achieve. The mismatch between replica VCO and main VCO, circuit non-idealities at low voltage supplies limit the same. In this chapter, alternate architecture for better linearity is discussed. The phase of a VCO is

proportional to the integral of its input. Thus, VCO can act as a linear integrator if the input to the VCO is within its linear range. Measuring the phase output of the VCOs gives integral of the input. Multi-bit output, when fed back, maintains the VCO input within its linear range. However, one of the main challenges is the variation of the circuit characteristics at ultra low voltages. This work proposes an ultra-low voltage, VCO-based sigma delta modulator with self-compensated current reference against process and temperature variations. The proposed current reference generator sets the feedback current of the multi-bit Non-Return-to-Zero (NRZ) DAC and the VCO tuning coefficient (K_{VCO}) at ultra-low voltage. A test chip fabricated in 65nm CMOS technology demonstrated successful operation at 0.3 V. It consumes 510nW and occupies 0.015mm². The proposed VCO-based $\Sigma\Delta$ modulator achieves peak SNDR of 56.1dB at 0.3 V and 10 kHz input bandwidth, and FoM of 49fJ/conv.-step. Detailed analysis of the architecture needed for design consideration will be provided.

III - Capacitance to Digital Converter using Continuous Time Second Order $\Sigma\Delta$ modulator with VCO as integrator/Quantizer

This work is an extension of dual-VCO based integrators towards a specific application. Early detection/monitoring of diastolic dysfunctions in the human heart can be done using a non-invasive, highly sensitive, portable sound recording system with cardiac sound wave characterization. Capacitive MEMS microphones, which are based on the modulation of electrical capacitance by the acoustic pressure wave from the heart sound, are an excellent choice for the recording device. Since capacitive sensors do not consume static power, they are very suitable for such portable low-power and energy-constrained applications. However, the energy

consumption will be dominated by that of the interface circuit that converts capacitance value to a digital output. This chapter proposes a novel architecture and circuit implementation for capacitance to digital conversion. Proposed capacitance-to-digital converter (CDC) uses a continuous time second-order delta-sigma modulator with multi-bit quantization for digitizing. Along with active-RC integrators using OTAs, this CDC employs VCO-based integrator with multi-bit quantization to achieve second order noise shaping. The proposed CDC has been realized in a 0.18 μ m CMOS technology. Measurement results show that the CDC achieves 13-bit resolution for capacitance-to-digital conversion with a measurement time of 0.125ms while consuming only 42 μ A from 1.2V supply. The design achieves a state-of-the-art figure-of-merit of 0.79pJ/conversion-step.

Chapter 1 Introduction

Scaling in MOS technology has been one of the biggest boons for the humankind. It helped realize complex architecture, which once seemed implausible. Large systems used in networking/communication, imaging, computation and biomedical applications, which used to be bulky and complex, are now being shrunk into miniature SoCs [12-16]. It is commendable that researchers have successfully extended Moore's law towards the fundamental limits. Inspired from Moore's Law and silicon technology many other disciplines such as MEMS devices, microfluidics, non-silicon sensors/imagers, packaging technologies, etc. are trying to leverage the benefits of scaling [17-19]. Nonetheless, increasing packing density in SoCs and co-integration of silicon and non-silicon systems have given rise to numerous sets of problems for the researchers. One of the biggest challenges associated with scaling is the dramatic increase in the power consumption and power density of SoCs [20, 21]. The problem is intensified due to the limitations in battery technology and the usability of cooling solutions. This inadequacy associated with advanced silicon systems has brought a shift in paradigm towards low power, low energy solutions.

1.1 Demand for ultra-low power Systems

Ultra low power, energy efficient circuits have been receiving a significant amount of attention in the recent past [22-24]. Innovations in portable handheld devices and implantable biomedical devices (Figure 1.1) are also playing a vital role in augmenting the need for ultra-low power designs [25-29]. Portable handheld devices like smartphones, tablets, smart watches and other accessories run on a stringent power budget imposed by the capacity of the battery. Implantable biomedical devices

Figure 1.1: Portable consumer electronic devices and impending bio-sensing and actuation nodes

on the other hand, are not easily accessible for battery recharge or replacement. The thermal energy liberated by these devices should be low for sensitive human organs. Hence, the total power consumption of these devices should be as kept as minimum as possible. Another emerging arena is the IoT devices and wireless sensing nodes (Figure 1.2) [30, 31]. Devices connected to IoT provides access to sense and monitor inaccessible nodes and to generate more data points for intelligent decision-making. To benefit fully from the IoT platform it is necessary to make them self-sustaining. This autonomous energy system nature of IoT devices demands innovations in self-powered, intelligent and energy efficient systems. Apart from these low power constraints, harvesting energy from ambient sources also dictates ultra low power operation. Energy harvesters are highly attractive for sensor nodes and biomedical devices where battery replacement or recharge is not very convenient. The main energy sources for such devices are thermal, solar, piezo-electric or inductive sources

Figure 1.2: Conceptual diagram for internet of things [4]

where the harvested voltage level in the range of few nW to mW [25, 32-35]. Due to inadequate availability of energy, it is strongly desirable to make circuits and systems consume ultra-low power.

1.2 Ultra-low power data converters

The advancement in IC technology and possibilities of ultra-low voltage operation has significantly reduced power consumption and energy per operation for digital circuits that have purely capacitive loads [36-38]. However, such design practices have not aided the analog integrated circuits to the same extent. Especially when analog circuits are operated in the sub-threshold region decreased current driveability, reduced intrinsic gain/voltage swing and increased device variability makes the circuit design quite challenging. Nonetheless, constant monitoring in sensing nodes necessitates ultra-low power for the analog circuits in sensor interfaces and wireless nodes [39, 40]. One way to deal with this problem is to compensate for

the robustness and performance of inferior analog circuits with the speed and area advantages of digital circuits. Thus, digital assistance to analog circuit design will help analog circuits to keep pace with shrinking IC design technology and make use of its advantages [41]. It also helps analog circuits to operate at near-threshold and sub-threshold operating voltages. One of the most commonly used subsystems in any biomedical device or a sensor node is a data converter. It acts as the interface between sensors and the digital backend. Challenges associated with scaling of IC design technology directly affect the design of data converters. SAR ADCs are a popular choice for ultra-low power data converter for its minimum use of analog circuitry. However, since the SAR ADCs use voltage levels to quantize the input signal the inherent noise and variations confine the number of quantization levels, when the supply voltage is scaled. This inability to scale quantization levels with supply voltage limits the resolution and dynamic range of SAR ADCs. Other data converters using pipeline or $\Delta\Sigma$ architectures can cater a wider range of resolutions. Nonetheless, due to their analog intensive architecture and innate non-idealities associated with analog circuits in nanoscale CMOS technologies for ultra low voltage operation, designing such ADCs would be challenging. Voltage Controlled Oscillator (VCO)-based ADCs are an emerging class of data converters which can fix the above issues related to technology and voltage scaling because to their digital nature and time domain architecture.

1.3 VCO-based ADCs

VCO-based ADCs could be used as a standalone ADCs or inside a $\Delta\Sigma$ modulator in two primary configurations. This section briefly discusses the operation principle, characteristic features, and limitations for them.

1.3.1 VCO-based Quantizer

Figure 1.3: ADC made of VTC and TDC [6]

"VCO-based quantizer can be viewed as an efficient combination of Voltage to Time Converter (VTC) and Time to Digital Converter (TDC)" [6, 42]. Figure 1.3 explains the operation of VTC and TDC. VTC in discussion is a ring oscillator consisting of array of CMOS inverters. It has a tuning voltage input that controls the frequency of oscillation. Thus, VTC converts input voltage to an oscillation frequency or in other words a signal in voltage domain to time domain. TDC on the other hand quantizes a time pulse to a digital value by passing a time pulse through a series of delay elements. The number of transitions by the time pulse through the delay elements in a sampling clock represents the digital value. As mentioned, ring oscillator is made of simple CMOS inverter structures making the circuit analog in time domain and digital in voltage domain. Such a structure has a high noise margin that makes it technology/voltage scaling friendly. Similarly, the delay resolution of the TDC is limited by minimum delay achievable for a delay element in a CMOS technology. As we know, with technology scaling, delay is going to become smaller and hence we can achieve better delay resolution. The VCO-based ADC in Figure 1.4(a) combines both the converters, i.e. to a voltage to digital converter or an ADC. Thus, it inherits

Figure 1.4: VCO-ADC using Ring Oscillator VCO

all the benefits of technology scaling and supply voltage scaling that is available for VTC and TDC. VCO in Figure 1.4 (a) is made of 31 stage CMOS inverter ring oscillator, oscillating at a frequency

$$F = \frac{1}{2 \cdot N \cdot t_d} \quad (1.1)$$

Where $N = 31$, is the number of delay stages in the VCO and t_d is the delay of an individual delay element controlled by the input $V_{in}(t)$. However, the lowest

possible delay of a delay element improves with technology scaling. The phase sampler and encoder that follows the VCO samples and encodes the distinct phases of VCO to a 5-bit value. The difference between successive phase samples represents the number of transitions in VCO phase in a sampling interval. Since the number of transitions represents the analog input, the output from the transition counter gives the corresponding digital code. As we can see, quantization in VCO-based ADC takes place in time domain i.e. the change of VCO state is quantized using a sampling clock. When compared to the voltage domain quantizer, time domain quantizer is better since the quantization in time domain could be easily implemented using flip-flops. The time domain waveforms can be seen in Figure 1.4(b). The phase output of the VCO is not reset when sampled. Hence, the quantization error in one sample has the residue error from the previous sample. Thus, the quantization error of the VCO-based quantizer is inherently first order noise shaped [6, 43]. Such a VCO-based quantizer can be used as an open loop continuous-time $\Delta\Sigma$ modulator or as a quantizer inside a higher order $\Delta\Sigma$ loop [11, 42, 44].

1.3.2 VCO-based Integrator

The instantaneous phase of a VCO could be represented as the integral of its frequency, which in turn is a function of the VCO input signal. The phase, $\Phi(t)$, of the VCO, is proportional to the integral of its oscillation frequency.

$$\varphi(t) = 2\pi \int_0^t K_{VCO} \cdot x(\tau) d\tau \quad (1.2)$$

Where K_{VCO} is the tuning coefficient of the VCO and $x(t)$ is the input to the VCO. Consequently, by measuring the phase of a VCO, one could obtain the integral of its input. This property of the VCO could be harnessed to be used as the integrators in a

Figure 1.5: VCO Integrator in a closed loop first order $\Delta\Sigma$ Modulator

$\Sigma\Delta$ loop [45, 46]. Unlike traditional active-RC integrators, which suffer from non-idealities such as finite DC gain and limited gain bandwidth, VCO-integrators act like near ideal integrators. They are relatively easier to design, as they are primarily composed of CMOS inverter based ring oscillators (Figure 1.5). The phase of an N-stage VCO is sampled using flip-flops. Sampling the phase of the VCO, which is continuous in time, quantizes the output to discrete in time. The instantaneous phase thus obtained is compared against a reference phase. The digital output from comparison, represents the integral of VCO input. Thus, in addition to being an integrator, a multi-stage ring oscillator could also act as a multi-bit quantizer, which has numerous advantages in higher order $\Sigma\Delta$ modulators. The fed back output using a DAC, is subtracted from the input signal. Multi-bit feedback would keep the VCO in its linear range of operation. Since the output voltage levels of such VCOs are digital in nature and the analog information is contained in the phase of the VCO, they aid voltage/technology scaling and have excellent noise immunity. Akin to VCO-based quantizer, closed loop VCO-based integrator can be used as a stand-alone ADC or as a loop-filter in higher order $\Sigma\Delta$ modulators.

1.4 Comparison with SAR ADCs

Successive Approximation Register (SAR) ADCs are popular choice for ultra-low power data converters, thanks to their digital nature and simple architecture. It would be informative to make a quick comparison between VCO-based ADC architectures and SAR ADCs regarding ultra-low power/voltage operation.

Table 1-1 Comparing VCO-based ADCs with SAR ADCs

SAR ADC	VCO-based ADC
Analog signals are quantized in voltage domain, which makes ultra-low operating voltage challenging. Have poor noise immunity as signals are in voltage domain.	Signals are analog in time and digital in voltage and uses time domain for quantizing analog values that makes ultra-low voltage operation possible.
Needs sample and hold circuits which increases the complexity especially at low voltages.	Sampling operation and hence quantization are performed by flip-flops, which makes it easier to design even at low supply voltages.
Needs buffered voltage reference for the feedback DAC. In ultra-low power regime the additional power consumption of the references degrades energy efficiency.	Normal current or voltage reference is needed for operation. Absence of buffering improves energy efficiency at low operating voltages.
Quantization noise is white; that means energy efficiency does not improve with oversampling.	Quantization noise is first order noise shaped; Oversampling improves energy efficiency significantly.
If used in a sigma delta loop as a quantizer need additional DEM to tackle mismatch in multi-bit DAC.	Various architectures offer inherent DEM for the thermometer output code. Hence when used in a sigma delta loop as quantizer, VCO-based ADCs alleviate the need for additional DEM.

It can be clearly seen that VCO-based ADCs have advantages over SAR ADCs and their prospects could be better at advanced technology nodes and ultra-low supply voltages.

1.5 Motivation for this thesis

The survey of state-of-the-art data converters published in last ten years (ISSCC and VLSIC) typically gives a good indication of the latest trends and future direction in its research [47]. Two major areas for publication are high-performance ADCs for wideband signals in communication applications and ultra low power ADCs for IoT and other biomedical applications. Since this thesis focuses on ultra-low power applications, analyzing the effect of supply scaling on ultra-low power data converters would be insightful. Figure 1.6 plots the Walden FoM (FoM_W), to quantify energy efficiency, for ADCs used in ultra-low power, low bandwidth applications against operating voltage.

$$FoM_W = \frac{Power}{2 \cdot Band\ Width \cdot 2^{ENOB}} \quad (1.3)$$

The data has been collated from Prof. Murmann's ADC survey[47]. Technology and noise set the theoretical limit for ADC performance. For technology-limited architectures like SAR ADCs, switching activity is the primary reason for power consumption. Thus, decreasing supply voltage (V_{DD}) greatly helps such digital-intensive designs.

$$Power_{Tech} \propto V_{DD}^2 \quad (1.4)$$

For noise-limited architectures such as high-resolution $\Delta\Sigma$ modulators, the current consumption of the data converter defines the noise performance. Since power consumption for such architecture is static, scaling the operating voltage yields a linear reduction in power consumption as shown in (1.5).

Figure 1.6: Walden FoM vs. V_{DD} for recent ultra-low power ADCs

Figure 1.7: Schreier FoM vs. V_{DD} for recent ultra-low power ADCs

$$Power_{Noise} \propto V_{DD} \quad (1.5)$$

An envelope for desired performance is carved out by hypothetically scaling the supply voltage for two benchmark ADCs [48, 49], one each from noise-limited and technology-limited categories. A similar exercise is repeated for plotting (Figure 1.7) Schreier FoM (FoM_S), which gives more weighting factor for Dynamic Range (DR).

$$FoM_S = DR + 10 \cdot \left(\log_{10} \left(\frac{Band\ Width}{Power} \right) \right) \quad (1.6)$$

It could be easily noticed that there is significant room for improvement (indicated by arrow mark) in either category, especially in noise-limited designs. It is noteworthy that recent innovations in SAR-ADCs such as the use of noise shaping in the feedback path and oscillator based comparators have pushed the FoM_S beyond its predictable limits (Figure 1.7). Digital intensive architecture for VCO-based ADCs, which can also yield high resolution due to time domain quantization and noise shaping properties, is a good mix of both worlds. Thus, they are promising candidates for operating at ultra low supply voltages for increased energy efficiency.

1.6 Contribution of this thesis

This thesis focuses on the use of VCO-based architectures for data conversion in ultra-low power, ultra-low supply voltage applications. Contributions of this thesis can be listed as follows.

- Even though VCO based architectures are made of digital-intensive circuits, the inherent problem with a VCO such as non-linear voltage to frequency tuning curve, drift in tuning curve of the VCO makes it difficult to be used as a stand-alone data converter. High-performance VCO-based ADC

architectures, which have received significant attention, use interesting techniques to mitigate this problem. However, such techniques are not scalable with supply voltage due to various challenges. This thesis identifies the limitations for the existing techniques to support Ultra-low Voltage/Power operation in VCO-based ADCs.

- Two basic configurations of a VCO-based ADC are to act as a quantizer or as an integrator. This thesis proposes an open-loop VCO-based quantizer and a closed loop VCO-integrator based first order $\Sigma\Delta$ modulator for ultra-low voltage/power operation. The proposed techniques can be used for data conversion in low/medium resolution applications. Although proposed techniques have limited resolution, they could serve as building blocks for higher order modulators. Also, the analysis and design considerations provided along with the proposed designs could give insights on their characteristics.
- A novel current reference tolerant towards any process and temperature variations is also introduced in this thesis.
- This thesis also proposes an application for VCO-integrator/quantizer in wireless sensor nodes. A high/moderate resolution Capacitance to Digital Converter (CDC) will be proposed for ultra-low power microphone based auscultation technique. CDC uses a novel continuous-time architecture with VCO-integrator/quantizer for improved energy efficiency. However, since the SNR achievable for a CDC depends on the supply voltage, a higher operating voltage has been used to implement the test-chip.

1.7 Organization of this thesis

Introduction and motivation for this work are followed by a review of existing VCO-based ADC architectures in Chapter 2. In Chapter 2 existing architectures for VCO-based ADCs for ultra-low power consumption will be examined, and other VCO architectures for high performance will be analyzed for its usability towards ultra-low power/supply voltage. An ultra-low voltage open loop VCO-FDSM will be proposed in Chapter 3. The distortions arising from the non-linear voltage to frequency tuning curve will be corrected using a novel calibration algorithm proposed. Measurement result demonstrates the performance achieved by a test chip when operated at 0.4V. A 0.3V dual-VCO integrator-based closed loop $\Delta\Sigma$ modulator will be introduced in chapter 4. Variation susceptibility of the design is improved by a novel current reference proposed in the same chapter. Various design considerations to be made while designing such low voltage architecture will also be carefully analyzed. Chapter 5 demonstrates an application of VCO-integrators in a higher order $\Delta\Sigma$ loop for an ultra-low power CDC. It would be shown with measurement results that use of VCO-integrator with inherent multi-bit quantization improves the energy efficiency significantly. Lastly, the thesis would be concluded along with proposing scope for future work in Chapter 6.

Chapter 2 Review of existing $\Delta\Sigma$ Modulators for ultra-low voltage /ultra-low power operation

As discussed in section 1.5, FoM of $\Sigma\Delta$ modulators is limited by the innate circuit noises. However, when operated at a ultra-low voltage, their performance degrades drastically due to non-idealities and second order effects. Thus ultra-low power $\Sigma\Delta$ modulators demand novel architectures and circuit techniques to close in with the theoretical limits.

2.1 Existing Ultra-low voltage/power $\Sigma\Delta$ Modulators

Figure 2.1: Ultra-low Voltage Continuous Time $\Delta\Sigma$ Modulator using passive integrators [3]

Several Sigma-Delta ($\Sigma\Delta$) architectures have been proposed for low supply voltage[3, 50-54]. In [3], the authors discuss a continuous time $\Sigma\Delta$ modulator with passive integrators (Figure 2.1). The comparator is designed with a loop gain much larger than one as the passive stage deteriorates the input significantly. Even though it consumes relatively lower power, the leaky integrator limits the signal-to-noise ratio (SNR) even with a higher oversampling ratio (OSR) or higher order. This limitation confines the use of this architecture to a finite set of applications. The driving capability of the digital-to-analog converter (DAC) and the gain of the

comparator have to be high, for a stable operation. This requirement sets the minimum operating voltage of this architecture. These limitations hold true even when this architecture is extended using MASH architecture for wide-bandwidth applications [55].

Figure 2.2: Discrete Time $\Delta\Sigma$ Modulator with switched capacitors

In [51-54], the authors propose higher order discrete time $\Sigma\Delta$ modulators operating at very low voltage Figure 2.2. Ultra-low voltage operation is facilitated by the use of novel opamp structures. In [54] the near-threshold inverter-based amplifiers used for switched capacitor integrators suffer from low bandwidth and low gain, eventually degrading the SNR. Higher order architecture is employed to address this issue, at the cost of additional current consumption. Similar near-threshold inverter strategy is used in [51] where SNR drops at lower operating voltages. In [53] a novel amplifier with increased DC gain, at a low operating voltage, is proposed. However, the amplifier consumes a significant amount of current and decreases the energy efficiency of the circuit. Conversely in the discrete time implementation [52], where the supply voltage is double that of [51, 53, 54], energy efficiency evidently increased due to the higher intrinsic gain and easier implementation of amplifiers.

Similarly, continuous time implementation in [50] lack intrinsic DC gain and voltage swing for the amplifier used in the active-RC integrator. Thus, the resultant implementation has FoM notably larger than the ones imposed by noise limits. It is evident from the analysis that analog intensive architectures are not a good choice for ultra-low voltage operation. This lead to the investigation into a new class of $\Sigma\Delta$ modulators which can take advantages of voltage scaling without inheriting disadvantages of analog circuitry.

VCO-based ADCs are gaining prominence among researchers due to its attractive properties. Numerous researchers have proposed state-of-the-art VCO-based ADCs designed for operating at Nominal supply voltages. As discussed in Chapter 1, VCO-based ADCs are an excellent choice for ultra-low voltage operation. State-of-the-art designs in VCO-based ADCs will be reviewed for energy efficiency and their compatibility to ultra-low voltage operation [2, 8, 9, 11, 42-44, 56-60]. Advantages and limitations of these designs will be discussed.

2.2 VCO-based ADC in open loop

VCO-based quantizer in open-loop is also called Frequency Delta Sigma Modulator (FDSM) since the noise shaping happens in the process of voltage to phase and phase to frequency conversion. [44, 60] were one of the first implementations to harness this property of VCOs to be used as a quantizer. VCO is composed of 3 stage simple inverter based ring oscillator. The delays of VCOs were controlled by modulating the threshold voltage of the MOS devices using their bulk terminal as shown in Figure 2.3 [60]. Bulk control results in a non-linear voltage to frequency transfer function for the VCOs and is corrected using a soft rail transistor with fixed gate bias (V_{BIAS})

Figure 2.3: 0.2V Bulk Controlled VCO-FDSM

to provide a negative feedback, thereby making tuning curve linear. The main advantages of this method are inherent linearity, and supply noise rejection by the soft rail transistor. This work was updated by adding multi-bit quantization and pseudo-differential architecture to improve SNR [44]. However, the header transistor increases the phase noise of the VCO and thus deteriorates the SNR. The VCO power is increased to improve SNR, which degrades the overall Figure of Merit (FoM). Since it is not very easy to design, linear VCOs alternate techniques were proposed.

2.3 Background Non-linearity Calibration

Figure 2.4: Digital background calibration using pseudo random sequence

One way to deal with non-linearity is to calibrate and correct the distortion at the output. Various calibration schemes have been suggested to calculate and correct the distortion added by the VCO. In [8] the authors use pseudo-random patterns with zero mean to estimate the amount of nonlinearity. Figure 2.4 shows the architecture in brief. The pseudo random patterns are input to replica VCO after converting to current signals using a DAC. In the absence of nonlinearity, the output from the VCO-FDSM after being multiplied with the input would average out to zero. On the other hand, any nonlinearity would leave a residue on averaging which could be used to estimate the nonlinearity. Even though this technique could estimate and correct nonlinearity, the proposed architecture requires a linear V/I converter and has long calibration time, which makes low voltage operation at low sampling rates challenging.

Figure 2.5: Nonlinearity calibration using ramp response

Figure 2.5 shows the calibration architecture in [10]. It uses the response from the VCO-FDSM to a slow moving ramp to estimate the inverse nonlinearity model. The harmonics in the signal path is corrected using the inverse nonlinearity model. The final correction could be done using a polynomial correction method or a lookup table method. Even if the calibration procedure is simple, implementing this

technique for background calibration would require a ramp generator and related circuits, which could be challenging to design at low operating voltages.

Figure 2.6: Digital background calibration using signal path dithering

The authors in [83] discuss an interesting way to calibrate nonlinearity in the background without using a replica VCO. Two identical ADCs are arranged in split ADC architecture as depicted in Figure 2.6. The input for the split ADC is generated by adding a self-cancelling dither to the input signal. Dither signal reconstructed by subtracting the outputs of the split ADCs gives information about the slope of the non-linear VCO. The nonlinearity is estimated using Least Mean Square (LMS) computation techniques from the slope information and the corrected output is filled in the LUT. However, since the dither amplitude is tiny, the voltage range for which the nonlinearity of the voltage to frequency curve is calibrated is dependent on the input signal excursion within a given time. Hence, to compute the nonlinearity in the entire tuning range, longer calibration cycles would be needed. For many ultra-low power autonomous sensor nodes where signal acquisition and transmission has to happen within milliseconds, calibration time running into few seconds takes a toll on its energy efficiency [30, 31].

All the calibration algorithms discussed so far try to find a polynomial fit for the nonlinearity. In [11] the authors discuss architecture for computing the inverse nonlinearity curve without assuming a polynomial nature for the voltage to frequency curve of the VCO. If a frequency locked loop could make the nonlinear VCO oscillate at the desired frequency, the digital value corresponding to its input would represent the inverse nonlinear curve for the VCO (Figure 2.7). While the circuit can calibrate the nonlinearity effectively, long calibration time is still needed owing to the settling time of the loop and the loop filter.

Figure 2.7: Calibration using inverse nonlinearity curve

2.4 VCO as a quantizer in closed loop

Figure 2.8: VCO as quantizer in $\Sigma\Delta$ modulator

Non-linearity of the VCO could be corrected using closed loop ADC. VCO is used as the quantizer for a second order $\Sigma\Delta$ loop, thus effectively producing a third order

noise shaping [42]. Figure 2.8 shows the architecture of VCO being used as a quantizer. Non-linear voltage to frequency characteristics of VCO is mitigated by the high gain before the VCO. The high gain stage pre-distorts the input to the VCO so that output is corrected. The $\Sigma\Delta$ loop also shapes the phase noise caused by $1/f$ noise of the devices in VCO. However, use of linear DAC, high gain amplifier and high performance RC integrators limits the ultra-low voltage supply operation. Supply voltages in sub threshold and near threshold region demands minimum transistor stacking in the circuits. Ultra-low power supply also reduces the overdrive and voltage headroom of the transistors. These limitations pose a challenge for high gain of the amplifier across bandwidth. Op-amp based integrators consume considerable amount of power making this approach less energy efficient.

Figure 2.9: VCO as TDC along with PWM in $\Sigma\Delta$ modulator

Another method proposed is the use of linear TDC over a non-linear VCO [56]. In a $\Sigma\Delta$ loop, TDC is used as quantizer instead of VCO. While TDC here is realized using OR gates and associated digital logic, TDC could be implemented using ring oscillators as well [61]. PWM and TDC are embedded in a $\Sigma\Delta$ loop as in Figure 2.9. The loop filter shapes the quantization noise of TDC and nonlinearity of

the PWM. The $\Sigma\Delta$ loop does not use a feedback DAC. The TDC generates feedback pulse, quantized in time, corresponding to output code. These are converted to current pulses using differential pair and are fed back to an op-amp based loop filter. Even if feedback DAC is avoided, the design still uses an op-amp in the loop filter for integration and nonlinearity suppression. The use of op-amp makes this design challenging to be implemented in ultra-low voltage supplies and decreases overall energy efficiency.

2.5 Residue input technique

Figure 2.10: Residue Input VCO-based quantizer [2]

VCO is non-linear only when the input applied is outside its linear tuning range. If the input applied is within the tuning range, we can utilize the benefits of VCO-based ADC without nonlinearity affecting its output. This principle is used in residue input

techniques [2]. The architecture of such designs is shown in Figure 2.10. A coarse quantizer made of Flash ADC is used to quantize inputs exceeding the linear tuning range of the VCO. The quantized output is converted to an analog voltage using a DAC and is subtracted from the original input to obtain a residue. The residue obtained is an analog voltage well within the tuning range of VCO. This residue when fed to VCO-based ADC gives a linear first order noise shaped output. Thus, VCO act as a fine quantizer. The final output is a delay compensated sum of the fine and coarse quantizer. The authors of [2] made a second order $\Sigma\Delta$ modulator by embedding this quantizer in a $\Sigma\Delta$ loop. While this technique eliminates the non-linearity introduced by VCO, gain mismatches between ADC and coarse quantizer needs calibration. Main feedback DAC needs additional Dynamic Element Matching (DEM) techniques to deal with non-linearity. It might also inherit the problems related to Flash ADC such as offset and gain errors. Overall, this architecture is not very suitable for low voltage operation.

Figure 2.11: Two Step open loop VCO based ADC [9]

An alternate method proposed for residue input uses VCO itself as coarse quantizer instead of Flash ADC [9, 62]. The details are shown in Figure 2.11. The coarse quantizer output, which would be non-linear unlike Flash ADC, is subtracted from original input to obtain the residue. This residue thus contains inverse non-linearity of that of the coarse quantizer. The residue is input to the fine quantizer, the output of which would have the inverse non-linearity. When both quantizer outputs are added together, the non-linearity from both the quantizer is canceled. The advantage of this technique over the former is that coarse quantizer output makes use of barrel shifting property of VCO to tackle DAC mismatches [6]. Even though, this architecture uses minimum analog circuitry, the dynamic non-linearity added by the DAC, which is considerable at low supply voltages, could deteriorate SNDR.

2.6 VCO as integrators in sigma delta loop

Figure 2.12: VCO as an integrator/quantizer in higher order $\Sigma\Delta$ loop

As discussed previously in the introduction, the integral relation between input and phase of an oscillator could be utilized to use the oscillator as an integrator. One of the first implementations of VCO-integrators [58] compares VCO phase to the phase

of a reference clock, thereby measuring the absolute phase of the VCO. Architecture for the implementation is in Figure 2.12, and VCO integrator is same as the one in Figure 1.5. The multi-bit feedback generated from the multi-stage VCO is used to limit the input of the VCO to its linear range. However, the output thermometer code from the quantizer needs additional DEM to shape nonlinearities added by the DAC.

Figure 2.13: VCO as integrator in hybrid $\Sigma\Delta$ modulator

Authors in [57] use minimum analog circuitry to implement a digital version of VCO integrator based $\Sigma\Delta$ modulator (Figure 2.13). The output transitions in a $\Sigma\Delta$ modulator are counted using a roll-off counter. Since the tuning range of the VCO is designed to be much larger than the sampling frequency, the output of the integrator is 9-bits. It needs to be truncated to a smaller number of feedback bits using a digital $\Sigma\Delta$ loop. Even though the architecture could be adapted for ultra-low voltage/power implementation, the need for redundant digital logic for truncation, DEM, etc. decreases the energy efficiency. Also, the prototype uses switch capacitor interface at the input for voltage to current conversion, which nullifies the inherent advantages of a continuous time $\Sigma\Delta$ loop, such as the antialiasing property, absence of noise folding. Another low power implementation of VCO-integrator based $\Sigma\Delta$ modulator samples the VCO phase using the reference clock [46]. Unlike the previous

implementation, this work uses single-bit output/feedback obviating any need for additional DEM (Figure 2.14). The input signal to the VCO is scaled down using switched capacitor circuits to linearize input to the VCO. Thus the entire architecture becomes equivalent to a discrete time $\Sigma\Delta$ modulator. Although the implementation is straightforward, scaling VCO input in a continuous time $\Sigma\Delta$ modulator would require an additional amplifier.

Figure 2.14: VCO as integrator with 1-bit feedback

2.7 Other architectures for VCO-based ADC

Several alternate architectures are available for implementing oscillator based ADC. However, most of the techniques are slightly modified versions of the broader configurations as discussed before. Authors in [63] use dithering based linearization for the VCO where VCO-based quantizer is used to quantize the residue from the first stage of a 0-1MASH structure. [64] discuss the use of VCO-based quantizer for Nyquist bandwidth by replacing the digital differentiator at the output of VCO with an analog differentiator at the input of the ADC. Analog differentiator reduces any large swing at the input of the VCO and avoids the quantization noise shaping property of a VCO-FDSM, thereby achieving a wider bandwidth. Various techniques to increase the dynamic range of the ADC such as interpolating the phase

of the VCO by adding Resistive adders [65] and configuring VCOs in a 0-1 MASH structures [66] have been proposed. Since the fundamental principles for these architectures are same as its predecessors, they have not been analyzed in detail.

2.8 Summary for the review

Pros and cons of the existing techniques can be tabulated as follows.

Table 2-1: Comparison for existing VCO-based ADC architectures

Technique	Analog Circuits	Linearization	Pros	Cons
Open Loop Linear VCO	Biasing circuits	Intrinsically Linear VCO	Simple implementation	Variation & increased phase noise
Background Calibration	Minimal depending on algorithm	Using lookup table	Mostly digital & capable of working at low voltage	Long calibration time
Residue Input Method	Amplifiers and DACs	Input to VCO in the linear region	Suppressed distortion	Analog intensive and difficult to implement in low operating voltage
VCO as a quantizer in closed loop $\Sigma\Delta$ modulator	Amplifiers & DAC	Pre-distorting the VCO-input by large loop gain	Good moderate resolution	Analog intensive and SNDR limited by distortion
VCO-as integrator	DAC	Limiting the input to VCO by using feedback	Mostly digital & capable of working at low voltage	Need better solutions for increased energy efficiency

From the above summary, most desirable property for an ultra-low voltage VCO-based ADC could be identified as digital-intensive architecture or minimum use of analog circuits. This thesis proposes two methods to implement a VCO-based quantizer and VCO-based integrator.

Chapter 3 Ultra-low voltage VCO-FDSM with digital background calibration

As discussed before VCO-based ADC is a promising solution for ultra-low voltage/power application because of its the digital nature and the time-based architecture [8, 43, 44, 46, 58, 59]. However, VCO-based ADCs still need analog assistance or on-chip calibration to address the nonlinear voltage-to-frequency characteristic, which makes ultra-low voltage operation challenging. In "Figure" from "section," an ultra-low voltage bulk-controlled VCO-based frequency delta-sigma modulator (FDSM) was discussed. Bulk control VCO was designed to be inherently linear by adding a header transistor, offering negative feedback. However, the header transistor increases the phase noise of the VCO and thus deteriorates the SNR. The VCO power is increased to improve SNR, which degrades the overall Figure of Merit (FoM). In this chapter, a novel calibration scheme is introduced, which circumvents the distortion added by bulk-controlled VCO instead of the header transistor. Thus, the noise performance of VCO is improved resulting in an energy efficient data conversion

Qualitative analysis for state-of-the-art background calibration techniques was provided in "section". Although those calibration algorithms were effective, the time taken to estimate and correct the non-linearity was too long. Various sensor node applications, where data acquisition takes place in few milliseconds, longer calibration cycles are not desirable. [30, 31]. Longer calibration cycle increases the overall energy budget for the ADC. Table 3-1 compares the calibration time of

various existing calibration schemes with that of the proposed solution. Unlike other calibration methods, the proposed calibration scheme uses only 2^{13} clock cycles to compute the correction coefficients, which is at least $256\times$ faster than the prior arts [8, 10, 11]. In addition to the fast calibration cycle, the proposed approach also uses minimal analog circuitry for supply voltage scalability and ultra-low voltage operation.

Table 3-1: Comparison of proposed calibration algorithm with state-of-the-art

Parameter	[8]	[10]	[11]	This Work
Number of Calibration Cycles	2^{26}	2^{22}	2^{21}	2^{13}
Time in seconds for 1.28MHz Clock (ms)	52k	3.2k	1.6k	<5

3.1 VCO-based Frequency Delta Sigma Modulator

Figure 3.1 shows the equivalent functional block diagram of an open loop pseudo-differential VCO-FDSM. The VCO converts an input voltage to the oscillation frequency. The phase of the VCO, $\Phi(t)$, is continuous in time and is proportional to the integral of its frequency of oscillation. The phase sampler at the output of the VCO quantizes the phase in time domain once in every sampling interval. The discrete-time differentiator that follows the sampler computes the change of phase in one clock cycle, which represents the equivalent digital output corresponding to the input. Mathematical model for the same has been analyzed and presented in [43]. In this section, the noise shaping theory of an open loop VCO-FDSM and the VCO non-idealities addressed by the proposed algorithm will be explained.

Figure 3.1: Block representation of open loop pseudo-differential VCO-FDSM

3.1.1 Quantization Noise Shaping in Open Loop VCO-FDSM with Ideal VCO

The voltage to frequency characteristics of a linear VCO embedded in an FDSM like the one in Figure 3.1 is given below

$$f(t) = F_C + k \cdot x(t) \quad (3.1)$$

where $x(t)$ is the instantaneous input to VCO, $f(t)$ is the instantaneous frequency of the VCO for given input, and F_C is the center frequency of the VCO for $x(t) = 0$. The phase of the VCO at any given time is the integral of the frequency over time, which can be written as follows.

$$\varphi(t) = 2\pi \int_0^t (F_C + k \cdot x(t)) dt \quad (3.2)$$

The phase $\Phi(t)$, which is continuous in time, is sampled at a period T and frequency F_S and quantized to $2N$ states. The number of states, $2N$, corresponds to the N -delay stages of the VCO. The quantized phase is represented as below.

$$\varphi(n) = \frac{2N}{2\pi} \cdot \varphi(nT) + Q_e(n) \quad (3.3)$$

The differentiator that follows the quantizer subtracts the previous state from the present state to record the phase change, and hence the FDSM output $D(n)$.

$$D(n) = \varphi(n) - \varphi(n-1) \quad (3.4)$$

Using (3.2) and (3.3), equation (3.4) can be rewritten as follows

$$D(n) = 2N \cdot \int_{(n-1)T}^{nT} (F_C + k \cdot x(t)) dt + Q_e(n) - Q_e(n-1) \quad (3.5)$$

A sinusoidal input $x(t) = A \cdot \cos 2\pi F t$ to the FDSM and solving (3.5) outputs a digital code as below

$$D(n) = 2N/F_S \cdot [F_C + k \cdot A \cdot \cos 2\pi F(n)T] + Q_e(n) - Q_e(n-1) \quad (3.6)$$

Equation (3.6) proves that the quantization noise is first order noise shaped. Finally, the output from the pseudo differential VCO-FDSM could be represented as

$$\begin{aligned} D_{PD}(n) = \frac{4N}{F_S} \cdot [k \cdot A \cdot \cos 2\pi F(n)T] + Q_{e1}(n) - Q_{e1}(n-1) \\ + Q_{e2}(n) - Q_{e2}(n-1) \end{aligned} \quad (3.7)$$

The power of quantization noises $Q_{e1}(n)$ and $Q_{e2}(n)$ from both FDSMs adds up since they are uncorrelated. Thus, pseudo differential operation quadruples the signal power and doubles the noise power, improving the overall SNR by 3dB

3.1.2 VCO Non-linearity in Pseudo-Differential VCO-FDSM

Actual VCOs have a nonlinear voltage to frequency relation. The voltage to frequency relation of a non-linear VCO is given as

$$F(t) = F_C + k \cdot x(t) + k_1 \cdot x^2(t) + k_2 \cdot x^3(t) + \dots k_n \cdot x^n(t) \quad (3.8)$$

where k_1 , k_2 , and k_n are the 2nd and 3rd and n^{th} order non-linearity coefficients, respectively. Distortions above the 3rd order are insignificant and are ignored in the analysis. Sinusoid input $x(t) = A \cdot \cos(2\pi ft)$ to the nonlinear FDSM generates an output digital code as given below

$$D(n) = \frac{2N}{F_S} \cdot [F_C + k \cdot A \cos 2\pi F(n)T + k_1 A^2 \cos^2 2\pi F(n)T + k_2 A^3 \cos^3 2\pi F(n)T + Q_e(n) - Q_e(n-1)] \quad (3.9)$$

The pseudo differential VCO-FDSM results in cancellation of second order non-linearity and generates the following output.

$$D_{PD}(n) = \frac{4N}{F_S} [k \cdot A \cdot \cos 2\pi F(n)T + k_2 \cdot A^3 \cdot \cos^3 2\pi F(n)T + Q_{e1}(n) - Q_{e1}(n-1) + Q_{e2}(n) - Q_{e2}(n-1)] \quad (3.10)$$

From the above equation, it could be seen that the 3rd order non-linearity remains uncorrected. In this work, a calibration algorithm for correcting third order non-linearity will be introduced.

3.2 Proposed Digital Background Calibration

Figure 3.2 shows the abstract view of the proposed calibration architecture [67]. The characteristics, as well as the nonlinearity of the VCO, can change over time due to temperature and other variations. Hence the proposed calibration algorithm employs a replica VCO path similar to [8, 59] as it does not interrupt the main ADC

operation. The signal VCO and the replica VCO are designed to be identical. The replica VCO path inside the calibration block is used to estimate the amount of nonlinearity in the VCO. The estimated nonlinearity information is used to calculate the corrected values, which are stored in the lookup table. The output of the pseudo-differential VCO from the signal path acts as the address for accessing the corrected values stored in the lookup table. The calibration algorithm is executed periodically in the replica path for calibrating time-varying non-linearity, and the lookup table is updated.

Figure 3.2: Architecture of the proposed calibration scheme

3.2.1 Proposed Calibration Algorithm

Consider the setup as shown in Figure 3.3 where two different sinusoids $\cos A + \cos B$ and $\cos A - \cos B$ are input to two identical non-linear systems similar to the one discussed in section 3.1.2. Then, the summation of the two FDSM outputs could be represented as

$$D_{SUM}(n) = \frac{4N}{F_S} [F_C + k \cdot \cos A + k_1(\cos^2 A + \cos^2 B) + k_2(\cos^2 A) + 3k_2(\cos A \cdot \cos^2 B) + Q_{e1}(n) - Q_{e1}(n-1) + Q_{e2}(n) - Q_{e2}(n-1)] \quad (3.11)$$

Figure 3.3: Principle behind the proposed background calibration scheme

Figure 3.4: Simulated output for the principle behind the background calibration

Behavior model of a ring oscillator VCO designed in 65nm technology was extracted, and setup shown in Figure 3.3 was simulated using these models in Matlab. Sinusoids with frequency 2.97 KHz and 2.03 KHz were used to generate the

inputs $\cos A \pm \cos B$ and output from each VCO-FDSM were summed together. The FFT spectrum of the output is shown in Figure 3.4. The terms listed in (3.11) can be easily identified from Figure 3.4. The summation result contains inter-modulation products of sinusoids, $\cos(A+2B)$ and $\cos(A-2B)$ arising out of the term $6k_2(\cos A \cdot \cos^2 B)$ the amplitude of which contains the measure of third order nonlinearity, k_2 . If the inter-modulation product is separated and amplitude is measured, we can estimate the value of k_2 . The proposed calibration scheme provides two known sinusoids as input to the calibration algorithm and estimates the non-linearity coefficient, which forms the basis of the calibration algorithm

3.2.2 Architecture for Implementing Proposed Calibration Algorithm

Architecture for the implementation of the calibration algorithm above is illustrated in Figure 3.5. Differential sinusoid input $\pm x(t) = \pm a_1 \cdot \cos(2\pi F_I t)$ with amplitude a_1 and frequency F_I is summed with a square wave $F_d(t)$. Note that a square wave is composed of a primary frequency component and its odd harmonics. Assuming the sampling frequency is F_s , the frequency of $F_s/4$ is chosen for $F_d(t)$ so that the 3rd order harmonic ($3/4 \cdot F_s$) and other higher order harmonics lie outside of the Nyquist bandwidth. Since VCO-based ADCs have inherent anti-aliasing features, input frequencies greater than Nyquist bandwidth do not generate aliasing problems [43]. Thus, the square wave with the frequency of $F_s/4$ and the amplitude, a_2 , acts as a sinusoidal wave with an amplitude $4a_2/\pi$ with the same frequency within the sampling spectrum. i.e. $F_d(t) \approx 4a_2/\pi \cdot \cos(2\pi F_d t)$. Sinusoids $F_d(t) + x(t)$ and $F_d(t) - x(t)$ are input to the pseudo differential VCO-FDSM and the outputs are added. Using the principles of VCO-FDSM discussed in section 3.1.2 and with inputs $F_d(t) \pm x(t)$ output could be represented as follows

$$D_{SUM}(n) = \frac{4N}{F_S} [k \cdot F_D(n) + k_1 \cdot (F_D(n)^2 + x(n)^2) + k_2 \cdot F_D(n)^3 + 3k_2 \cdot F_D(n) \cdot x(n)^2 + \text{Shaped Quantization Noise}] \quad (3.12)$$

Figure 3.5: Calibration algorithm architecture

Figure 3.6: Simulated output for calibration algorithm architecture

The output represented by the above equation is composed of various terms. $k \cdot F_d(n)$ corresponds to the high-frequency square wave at the input; $k_1 \cdot F_d(n)^2$ and $k_2 \cdot F_d(n)^3$

will be outside the Nyquist bandwidth and could be ignored; $x(n)^2$ is the 2nd order harmonics of the sinusoid $x(t)$. $3 \cdot k_2 \cdot x(n)^2 \cdot F_d(n)$ is the inter-modulation product of the input sinusoids, which bears the information of non-linearity k_2 . Rewriting inter-modulation product using the values $F_d(n) = (4/\pi) \cdot a_2 \cdot \cos(2\pi F_d \cdot n)$ and $x(n) = a_1 \cdot \cos(2\pi F_1 \cdot n)$

$$3k_2 \cdot F_D(n) \cdot x(n)^2 = \frac{3k_2 a_1^2 a_2 N}{\pi F_S} \cdot [2 \cdot \cos 2\pi F_D(n)T + \cos 2\pi(F_D - 2F_1)(n)T + \cos 2\pi(F_D + 2F_1)(n)T] \quad (3.13)$$

Component of output in (3.13) containing k_2 that needs to be separated from the output. Hence, we multiply the signal $D_{SUM}(n)$ with $F_d(t)$ in the digital domain. $F_d(t)$ in the digital domain is a square wave with frequency $F_S/4$ and values -1/+1. i.e. $F_d(n) \approx 4/\pi \cdot \cos 2\pi F_d(n)$. The product results in an array of terms containing frequency $F_d \pm 2F_1$, F_d , $2F_1$, etc. For simplicity, the output expression after multiplication is not shown. A 16-point moving average filter is used at the output of a smoothing filter to minimize the high-frequency components in the signal. The smoothened output could be approximated as

$$C_{LOW}(n) = 24 \cdot N \cdot k_2 a_1^2 a_2 / \pi^2 F_S \cdot \cos(2\pi \cdot 2F_1 \cdot n) \quad (3.14)$$

$$[Q_e(n) - Q_e(n-1)]_0^{F_S/16}.$$

The amplitude of the first term has information about the non-linearity, k_2 , and $[Q_e(n) - Q_e(n-1)]_0^{F_S/16}$ indicates the low-frequency components of quantization noise shifted by $F_d(n)$. Figure 3.6 shows the simulated spectrum of $C_{LOW}(n)$. A peak-to-peak detection logic can be used to find the amplitude of the signal. The magnitude of the signal, from (3.14) is

$$Calib = 24 \cdot N \cdot K_2 \cdot a_1 \cdot a_2 / (\pi^2 F_S). \quad (3.15)$$

If the values of a_1 , a_2 , N and F_S are known, k_2 can be easily calculated and is used to fill up the lookup table in the main signal path with the corrected values. The nonlinear output from the pseudo-differential FDSM (PD-FDSM), for an input $\pm y(t)$, is as follows

$$D_{PD} = 4 \cdot \frac{N}{F_S} \cdot (k \cdot y(nT) + k_2 \cdot y(nT)^3) \quad (3.16)$$

Non-linearity could be corrected by the correction coefficients as shown below

$$D_{CORR}(n) = D_{PD}(n) - x \cdot D_{PD}(n)^3 \quad (3.17)$$

where $D_{PD}(n)$ is the uncorrected value, $D_{CORR}(n)$ is the corrected value and ' x ' is the correction coefficient. Using (3.15), (3.16) and (3.17), the correction coefficient ' x ' could be found as follows

$$x = (4 \cdot N \cdot k_2 / F_S) / (4 \cdot N \cdot k / F_S)^3. \quad (3.18)$$

Rearranging the expression, we get

$$x = \frac{\pi^2 / 6 \cdot (24 \cdot N \cdot k_2 \cdot a_1^2 \cdot a_2 / \pi^2 F_S)}{(4 \cdot N \cdot a_1 \cdot k / F_S)^2 \cdot (4 \cdot N \cdot 4 / \pi \cdot a_2 \cdot k / F_S)}. \quad (3.19)$$

Thus, the correction coefficient ' x ' could be computed using known values as shown below

$$x = \frac{\pi^3 / 24 \cdot (Calib)}{(A_1)^2 \cdot (A_2)} \quad (3.20)$$

where A_1 and A_2 are the amplitudes of the sinusoids F_1 and F_d respectively, measured from the output of a PD-FDSM.

3.3 Implementation Details

3.3.1 VCO-FDSM

Figure 3.7 shows the schematic details of the proposed VCO-FDSM. For simplicity, only positive half of the PD-FDSM is illustrated. VCO is implemented using 16 stages of VCO delay cells. VCO delay cell is made using a differential CMOS inverter. The bulk of the PMOS transistors in the delay cell is connected to the input signal. Thus the input signal changes the threshold voltage of the PMOS, thereby modulating the current through the PMOS. This modulation varies the charging time of each inverter load device, which in turn changes the frequency of oscillation of the VCO. Since the operating voltage of the VCO is low, biasing the body of the PMOS transistor with a voltage lower than the source does not turn on the body diode. The outputs of the VCO delay cells are buffered to avoid any loading effects from the subsequent stages. The buffered output is sampled using a sense amplifier flip-flops (Φ -Sampler). The 16-stage VCO produces 32 distinctive phase states. The phase sampled by Φ -Sampler is encoded to 5 bits using a 32:5 state encoder (Φ -Encoder). Digital differentiator that follows the Φ -Encoder finds the number of state changes between two successive clock cycles. A number of state changes in one clock cycle represents the digital code corresponding to the given analog input. An identical VCO-FDSM is used for the negative half of the PD-FDSM. Outputs from both the FDSMs are subtracted to get a 6-bit digital code. The maximum frequency of oscillation for the VCOs for this design is limited to the sampling frequency, 1.28MHz, to avoid phase roll-off. Since the input to the VCO is to the bulk terminal of the PMOS, the input signal could have a rail to rail swing.

Figure 3.7: Schematic diagram for open loop VCO-FDSM

3.3.2 Digital Background Calibration Block

Figure 3.8 shows the block level architecture of the proposed calibration scheme. All the blocks except analog waveform generator and replica FDSM are implemented using Hardware Descriptive Language and place and route tools. Replica PD-FDSM is designed to be identical with the signal PD-FDSM. To ensure proper matching both PD-FDSMs share common power and ground lines and are placed very close to each other. Clock control block generates the divided clocks CLK/2, CLK/4, CLK/64 and CLK/128 needed by the calibration algorithm. Mode control block generates the necessary control signals required to sequence each mode of operation.

In the beginning, of calibration algorithm, analog, waveform generators produce differential sinusoid $\pm x(t)$ with a frequency 10KHz and amplitude $\pm a_1$. The pseudo-differential FDSM converts the differential sinusoid input to a digital output. A peak detector block, which follows the FDSM, measures the amplitude, A_1 , from the output. The frequency of sinusoid was chosen to be equal to the bandwidth of the modulator, 10 KHz. The procedure is repeated using a square wave input ($F_d(t)$) to the FDSM. A differential square wave with frequency $F_s/4$, i.e. 320 KHz, and amplitude $\pm a_2$ is input to the PD-FDSM. The peak detector measures an amplitude A_2 , corresponding to the square wave as before. Thirdly combination of sinusoid $F_d(t)+x(t)$ and $F_d(t)-x(t)$ is input to the calibration algorithm, which generates the desired signal $C_{LOW}(n)$ needed to calculate correction coefficient 'x' as per (20). The 15-bit corrected values computed using the correction coefficient is used to fill in the lookup table using 6-bit uncorrected value as the address. The sequence of execution of the algorithm and number of clock cycles used for each step is depicted in the

Figure 3.9. It takes approximately 2^{13} clock cycles for one entire calibration cycle, which is at least 256 times faster than other state-of-the-art techniques

Figure 3.8: Block diagram representation of calibration architecture

A ₁ calculation	A ₂ Calculation	Calib Calculation	Lookup table Fillup
256 cycles	256 cycles	4096 cycles	1280 cycles

Figure 3.9: Calibration sequence for a total of approx 2^{13} clock cycles

3.3.3 Analog Waveform Generator

Inputs to the pseudo-differential FDSM as per the calibration sequence are generated by the analog generation block using generated clocks and control signals. The circuit consists of 2^{nd} order active-low pass, resistive adders, and digital logic. For simplicity, only the positive half of analog signal generator is shown in the Figure 3.10. The 2^{nd} order active low pass filters generates the sinusoids $\pm x(t)$ of frequency 10 KHz by filtering differential square waves of frequency $F_s/128$. Inverter based g_m cells, as shown in the Figure 3.10, are used as the active element in the filter because of its simple design and for aiding low voltage operation. Series of PMOS devices biased in the deep sub-threshold region are used as pseudo-resistors

for biasing the inputs of the g_m cells to the output DC level. The simulated waveform of input and output to the filter is shown in Figure 3.11. Digital logic selects the desired clock/DC signals needed to generate the waveforms based on the mode of operation. Resistive adders provide the desired DC shift for $\pm x(t)$ and $\pm F_d(t)$ while computing A_1 and A_2 respectively. While estimating $Calib$, the resistive adder sum the sinusoid and square wave to generate $F_d(t)+x(t)$ and $F_d(t)-x(t)$.

Figure 3.10: Schematic diagram for analog waveform generator

Figure 3.11: Simulated input and output for the 2nd order low pass filter

All the circuit blocks are designed to operate at 0.4V. Minimum channel length devices in the standard cell libraries have higher threshold values to tackle short channel effect that limits the minimum voltage for operation for this design

3.4 Design Considerations for Calibration Algorithm

Like every other circuit, proposed calibration algorithm is also subject to non-idealities. Several factors are to be taken into account while framing the architecture and in implementing schematics.

3.4.1 Number of Clock Cycles for Calibration

Figure 3.12: SNDR vs. Calibration cycles

During the calibration cycle, the non-linearity information is calculated by measuring the amplitude of the 20 KHz sinusoid as per (15). With a sampling frequency of 1.28MHz, it takes only 128 clock cycles to measure the amplitude from a single cycle of the sinusoid. However, the SNR of the resultant waveform would be poor due to the presence of other frequency components. Reduced SNR degrades the

calibration accuracy. Hence, the amplitude of the sinusoid measured across multiple cycles is averaged to minimize the error. The results of behavior model simulations, which plot SNDR/SFDR of the corrected output against the number of clock cycles used for non-linearity detection are shown in Figure 3.12. As we can see from the simulation results, at least 2^{11} cycles are needed to obtain maximum non-linearity correction. Hence, 2^{12} clock cycles were chosen for the same

3.4.2 Effect of Sinusoid Block on SNDR

As discussed in section 3.3.3, the analog waveform generator produces the sinusoids $\pm x(t)$, needed by the calibration scheme, from square waveforms of frequency CLK/128. However, the 2nd order low pass filter in the analog waveform generator cannot suppress the higher order harmonics in the square wave completely. Hence, the effect of higher order harmonics in the sinusoids $\pm x(t)$ on the nonlinearity correction must be carefully studied. Figure 3.13 plots SNDR/SFDR of the corrected output to the amount of 3rd order distortion (in dBc with respect to the primary sinusoid). It is seen that maximum 3rd order distortion that can be tolerated without degrading SNDR is 25dBc. The process variation and mismatch in analog sub-circuits deteriorate the performance of calibration algorithm, especially when they are operated at the weak inversion region. In analog waveform generator, the cut-off frequency of the filter is subject to process variation, which adds harmonic distortion to the sinusoid. Figure 3.14 plots the amount of 3rd order harmonics (in dBc with respect to the primary sinusoid) across 1000 Monte-Carlo simulations. It could be seen that the harmonics are below desirable values in more than 700 cases. This variation could be improved by using variation tolerant designs.

Figure 3.13: Effect of harmonics in $\pm x(t)$ on the output

Figure 3.14: 1000 points Monte-Carlo simulations on low pass filter to measure FDSM harmonics

3.4.3 Effect of Mismatch between Signal VCO and replica VCO

As discussed, the calibration algorithm is run on the replica path of VCO-based ADC. Hence, the mismatch between the replica VCO and the signal VCO is imperative. Offset mismatch between the signal VCO and the replica VCO does not affect the calibration algorithm, as the non-linearity coefficients are unaffected.

However, the gain mismatches in the VCOs affects the nonlinearity calibration as the 3rd order non-linearity calculated using the replica VCO could be different from that of the signal VCO. 100-point Monte Carlo analysis was run on the pair of VCOs to extract the respective voltage to frequency tuning curve. The voltage to frequency curve of the VCOs was fit in the behavioral model for the FDSMs used by the calibration algorithm, and SNDR plots were obtained. Figure 3.15 shows the distribution of SNDR/SFDR with the mismatch between replica and signal VCOs. Special layout techniques have to be adopted to keep the mismatch to its minimum. Delay cells with tunable load capacitances, as shown in Figure 3.7, could be used to adjust the delay to reduce any mismatch between VCOs.

Figure 3.15: 100 Monte-Carlo runs for mismatch between signal VCO and replica VCO

3.4.4 Effect of VCO-phase noise on output SNR

VCO phase noise affects the in-band noise of a VCO-based ADC considerably, hence design parameters for VCO should be carefully considered. Detailed analysis of VCO phase noise on SNR is provided in section 4.3.3, hence the same is omitted in this chapter to avoid redundancy.

3.5 Measurement Results

Figure 3.16: Test chip die photograph.

Figure 3.16 illustrates the die micrograph of the proposed ADC. The prototype design is fabricated using commercial 65nm CMOS process and occupies an area of 0.24mm^2 . All the blocks in circuit schematic shown in Figure 3.7, and Figure 3.8 are implemented on-chip. Various test modes to measure FDSM output without the proposed calibration; to set different modes of calibration and to measure other intermediate outputs in the calibration unit were also included. A 1.28MHz sampling

clock reference, which is also used as the master clock for calibration, is provided by an external clock reference. All other clock sources needed are generated on-chip from the master clock. VCO-FDSMs and Calibration logic operate from a 0.4V power supply. Figure 3.17 shows 2^{13} point FFT spectrum of the output $C_{LOW}(n)$ from calibration block. The amount of nonlinearity information needed to fill in the lookup table is obtained from the amplitude of $C_{LOW}(n)$. The calibration signal is smoothened using a low pass filter to minimize the error in measuring the amplitude.

Figure 3.17: Measured spectrum of $C_{LOW}(n)$

Figure 3.18 shows the 2^{15} -point FFT plots of output averaged 16 times before and after calibration for an input sinusoid of frequency little higher than 1.8 KHz and amplitude 300mV_{PP}. It could be seen from the figure that third order distortions improved by more than 21dB and the SNDR improved from 42dB to 55dB. Due to

the layout mismatches, even order distortions dominate the corrected output. The measured SNDR with and without calibration for different input amplitudes is shown in Figure 3.19. Third order nonlinearity with uncorrected output becomes dominant from 100 mVPP.

Figure 3.18: Measured FFT spectrum of output with and without calibration

Figure 3.19: Measured SNDR vs. Input Amplitude

(a)

(b)

Figure 3.20 (a) Measured spectrum with dual tone inputs without calibration and (b) measured spectrum with dual tone inputs after calibration

Figure 3.20 shows the measured spectrum of the un-calibrated output for the input with dual tones at frequencies 1.3KHz and 2.1KHz. The third order harmonic distortions are clearly visible at -45dB with respect to the input. On applying the corrected values, the SFDR is improved by more than 13dB to 58.2dB as seen in Fig 24. The ADC achieves a peak SNDR of 55dB with an input amplitude of 300 mVPP. The signal VCO FDSM and replica VCO FDSM together consume 2.3 μ W, the analog waveform generator consumes 0.3 μ W, and the Background Calibration consumes 2 μ W. It takes only 5ms to run one calibration cycle, hence the calibration block including replica VCO could be disabled intermittently. Thus, the total power consumed by the ADC is only 1.15 μ W.

Table 3-2 Performance Comparison with state-of-the-art Designs

Parameter	[54]	[53]	[46]	[44]	This work
Process (nm)	130	130	180	90	65
Supply (V)	0.25	0.25	1/0.5	0.2	0.4
Active Area (mm ²)	0.337	0.74	0.06	NA	0.24
Sampling Freq. (MHz)	1.4	1.28	0.25	12	1.28
Bandwidth (KHz)	10	10	2	20	10
Peak SNDR (dB)	61	73.3	58.5	60.3	55
ENOB	9.84	11.88	9.42	9.72	8.84
Power (μ W)	7.5	35.6	0.379	7.5	1.15
FoM (fJ/Conv.-Step)	409	471	137	82	125

The performance of the proposed ADC is compared with other state-of-the-art ultra-low power ADCs in Table 3-2.

$$\text{FoM} = \text{Power} / (2 \cdot \text{BW} \cdot 2^{\text{ENOB}}) \quad (3.21)$$

The figure of Merit (FoM) for this ADC is calculated as (21). The ADC achieves FoM of 125fJ/conv-step for different input frequencies, which is the lower or at par with other ultra-low voltage sigma delta modulators [14, 15, 20, 21]. The calibration algorithm takes less than 2^{13} cycles, which is the fastest among similar works.

Chapter 4 Ultra-low voltage $\Delta\Sigma$ Modulator with dual VCO-integrator using Self-compensated Current Reference for Variation Tolerance

Open-loop VCO FDSM with digital background calibration introduced in the last chapter has some limitations and disadvantages such as susceptibility to mismatch and variation, larger area, etc that needs to be addressed. Another alternative for amplifier less VCO-based ADC design is to use VCO as an integrator in the $\Delta\Sigma$ modulator, several realizations of which were discussed in Chapter 2. One interesting implementation proposed by K. Lee et.al [45] is dual-VCO integrator as depicted in Figure 4.1.

4.1 VCO as Integrators in $\Sigma\Delta$ Modulators

Figure 4.1: First order $\Delta\Sigma$ modulator with dual-VCO-integrator

In Figure 4.1 N-stage dual VCOs with differential input is used as integrators. Differential input causes the phase of the VCOs to rotate in opposite direction. Thus by comparing the phase of one VCO to another, using XOR gates, generates the

integral of the input. The outputs of the XOR gates are sampled at a rate, F_s . The multi-bit output generated from multistage VCOs when fed back using Non-Return to Zero (NRZ) DAC, forces the VCO to operate in its linear range. If V_{CM} is the common mode input voltage, $x(t)$ is the VCO input VCO input and V_{LSB} is the quantization step size, then

$$V_{CM} - V_{LSB} < x(t) < V_{CM} + V_{LSB} \quad (4.1)$$

Dual VCO-integrators offer extra advantage of intrinsic Clocked Level Averaging-Dynamic Element Matching (CLA-DEM) which modulates the DAC element mismatches to twice the center frequency of the VCOs [45]. Even though the circuit looks simple, it's operation is challenging at ultra-low supply voltages.

4.1.1 Effects of Variation in $\Sigma\Delta$ Modulators

Figure 4.2: Continuous-time $\Sigma\Delta$ modulator with m Hz sampling rate

Consider the first order continuous time $\Sigma\Delta$ modulator shown in Figure 4.2. It has a sampling rate of m Hz, a continuous-time integrator with transfer function m_1/s and NRZ DAC (with gain 'k') that converts the discrete-time output pulse trains to

continuous-time pulses. For values m , m_1 , k being unity, it could be seen that the output of the integrator stabilize after one second and the switch samples it at the exact time. The closed-loop response of the system in z -domain could be derived as

$$V(z) = z^{-1} \cdot U(z) + (1 - z^{-1}) \cdot E(z) \quad (4.2)$$

where $E(z)$ corresponds to the quantization noise. When the same modulator operated at a frequency of m Hz with unity DAC gain, the output pulses from the DAC shrinks in width because of frequency scaling. For maintaining the same noise transfer function, the DC gain of the integrator has to be scaled “ m ” times so that the output of integrator stabilizes after $1/m$ sec. If the DC gain of the integrator is a different value, m_1 , then the modified transfer function could be derived as

$$V(z) = z^{-1} \cdot \frac{m_1}{m} \cdot U(z) + \left(1 - \frac{m_1}{m} \cdot z^{-1}\right) \cdot E(z) \quad (4.3)$$

It could be deduced from (4.3) that the in-band quantization noise power and signal power are dependent on the DC gain of the integrator. With $m_1 > m$, the input to the quantizer exceeds its maximum stable amplitude making the loop unstable. For $m_1 < m$, in (4.3), the signal power reduces and quantization noise is not properly filtered thereby deteriorating the SNR. Figure 4.1 is functionally same as Figure 4.2, where VCO acts as the loop filter, the sampling rate is F_s Hz, and output is fed back using an NRZ DAC. As discussed, to maintain the noise transfer function, the DC gain of the integrator must be scaled to F_s . In the case of a VCO, the tuning coefficient K_{VCO} acts as the DC gain. Consider a setup shown in Figure 4.3(a) Input transistor M_1 controls the frequency of oscillation of a 27-stage ring oscillator; M_2 is a weaker device that keeps the VCO oscillating, even when M_1 is completely turned off. The voltage to frequency curve of the VCO is depicted in Figure 4.3(b). If Δf

were the change in frequency for an input change from $V_{CM}-V_{LSB}$ to $V_{CM} + V_{LSB}$, then K_{VCO} is approximately

$$K_{VCO} \approx \Delta f / (2 \cdot V_{LSB}) \quad (4.4)$$

Figure 4.3: (a) Non linear VCO, (b) estimating K_{VCO} from a VCO

Figure 4.4: Simulated effect of K_{VCO} on SNR

An ideal VCO-integrator based $\Sigma\Delta$ modulator with 5-bit quantization was simulated to demonstrate the effect of variation in K_{VCO} on SNR. Result for the simulation is shown in Figure 4.4. The trend observed is in agreement with (4.3). It is well known that, in one oscillation cycle, the phase of a VCO rotates from zero to 2π . By intuition, K_{VCO} could be seen as the rate of change of phase. If K_{VCO} were larger than sampling frequency (F_s), the phase of the VCO in one sampling interval would exceed 2π , resulting in a phase roll off destabilizing the modulator. If K_{VCO} were small, a slower rate of change of phase causes a drop in the gain for high-frequency components of quantization noise, thereby increasing the noise gain inside the bandwidth. Thus, variation in K_{VCO} with process and temperature would affect the overall performance of the modulator.

The closed loop transfer function in Z domain for the modulator in Figure 4.2 with m and m_1 equal to one and with the gain of the feedback DAC set to 'k' could be represented as

$$V(z) = \frac{z^{-1}}{(1 - (1 - k) \cdot z^{-1})} \cdot U(z) + \frac{(1 - z^{-1})}{(1 - (1 - k) \cdot z^{-1})} \cdot E(z) \quad (4.5)$$

A setup as shown in Figure 4.2 was simulated, using behavioral models of ideal integrator as well as VCO integrator, for different DAC gains. Figure 4.5 plots the result for the same. As the DAC gain decreases, the input to the quantizer tries to exceed the limits of its saturation making the modulator unstable. With an ideal integrator, the overall quantization noise power increases thereby degrading the SNR marginally, for an increased DAC gain. Larger DAC gain enlarges the swing at the input of the VCO, which pushes its operation in its non-linear regime. VCO non-

linearity results in an increased in-band noise floor, thereby degrading the SNR with VCO-integrator [68]. Further increasing the DAC gain shifts the input common mode voltage of the VCO, which ends up destabilizing the loop. From the above simulations, it is clear that VCO-integrator based $\Sigma\Delta$ modulator leave only little room for variations in DAC current.

Figure 4.5: Simulated effect of DAC gain on SNR

4.1.2 Variation of a current reference in weak-inversion

As we are aware, the performance of CMOS circuits is affected by variations in process and temperature, especially variation in threshold voltage. The Current reference is one key building block for the architecture shown in Figure 4.1. Any variation in current reference alters the DAC current and biasing current for the VCO, which in turn affect the performance of the modulator. This effect of variation in threshold voltage on current reference is intensified when devices are operated in

Figure 4.6: (a) Monte-Carlo simulation results for threshold voltage variation, (b) output current variation & (c) output current vs. temperature

sub-threshold region, due to the exponential relationship between current and threshold voltage of the MOS device. Figure 4.6(a) shows variation in threshold voltage for a PMOS device from 5000 points Monte-Carlo simulation. When biased using a fixed voltage, the PMOS demonstrate a larger variation in current as illustrated in Figure 4.6(b). When operated in weak inversion region drain current of a MOS device is predominantly diffusion current due to leakage. Hence, change in temperature would have a considerable effect on the drain current as depicted in Figure 4.6(c). Since such large-scale variation in current for a MOS device could

destabilize $\Sigma\Delta$ modulator, variation tolerant current reference is highly desirable. In this Chapter, we propose a novel current-reference and VCO to mitigate these issues across different process and temperature corners.

4.2 Proposed $\Delta\Sigma$ Modulator with ultra-low voltage Current Reference & Differential VCO

Figure 4.7: Basic principle behind proposed current reference (a) schematic details, (b) graphical interpretation

4.2.1 Proposed Current Reference

Two similar transistors M_1 and M_2 are connected in series as shown in Figure 4.7. The operating voltage used is 0.3V and nominal value of threshold voltage for the transistors is around 0.25V. Thus, M_1 is biased in near threshold saturation region with a drain current, I_d , is given as

$$I_d = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \frac{(V_{DD} - |V_{TH}|)^2}{2} \quad (4.6)$$

where μ_p is the hole mobility, C_{ox} is the oxide capacitance, W/L is the sizing for the device, V_{DD} is the source to gate voltage of M_1 and V_{TH} is the threshold voltage of the device. M_2 is operating in weak inversion with a drain current

$$I_d = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (m - 1) \cdot V_T^2 \cdot e^{\left(\frac{V_X - V_{TH}}{mV_T}\right)} \quad (4.7)$$

where V_X is the source to gate voltage for M_2 , m is the sub-threshold slope factor, and V_T is the thermal voltage. Thus, M_1 and M_2 have different relationships between the drain current and V_{TH} . Hence, any variations in V_{TH} , change the voltage at the source of M_2 . Under DC conditions, the drain currents of M_1 and M_2 , in Figure 4.7, will be the same. Differentiating source to gate voltage of M_2 on V_{TH} after equating (4.6) and (4.7) we get

$$\frac{\partial V_X}{\partial V_{TH}} = 1 - \left(\frac{2m_0 \cdot V_{T0}}{V_{DD} - V_{TH0}} \right) \quad (4.8)$$

where, V_{T0} , m_0 , V_{TH0} are the typical values for V_T , m and V_{TH} respectively at room temperature. Thus, variation in threshold voltage leaves a residue at the source of M_2 , V_X , which could be used to compensate for variation in threshold voltage. The ratio can be fixed to be 1/2 by adjusting V_{TH0} and V_{DD} . Due to the reverse short channel, effect the threshold voltage of an MOS device decreases with increasing length. Desired value of V_{TH0} is set by adjusting the length of the transistors. The Relation between V_X and V_{th} could be graphically derived as demonstrated in Figure 4.7. The transistors M_1 and M_2 are sized to keep them in saturation. Figure 4.8 illustrates the proposed current reference generator is biasing M_9 to have constant current under temperature and process variations. To aid ultra-low voltage operation, stacking more than two transistors is avoided. M_3 - M_6 are sized to have gain '2'.

Figure 4.8: Proposed current reference circuit

For a V_{TH} change of ΔV_{th} , due to process variation, the voltage at the source of M_6 changes by $-\Delta V_{th}$. After the NMOS unity-gain source follower (M_7 - M_8), the bias to M_9 is self-adjusted for compensating process variations and generates a reference current (I_{REF}). Drain current for M_9 can be given by the equation;

$$I_d = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (m - 1) \cdot V_T^2 \cdot e^{\left(\frac{(V_{DD} - V_{BIAS}) - V_{TH}}{mV_T}\right)} \quad (4.9)$$

where V_{BIAS} is the voltage at the gate terminal of M_9 . From (4.9) it could be observed that change in temperature affects primarily V_{TH} , V_T and μ_p . The change in V_{BIAS} compensates variation of V_{TH} on temperature. However, additional compensation should be provided to cancel the effects of temperature on V_T and μ_p . The rate of change of I_d on temperature must be equated to zero to find the amount of compensation needed for temperature variation.

$$\frac{\partial I_d}{\partial T} = 0 \quad (4.10)$$

By substituting (4.9) on (4.10) and rearranging the terms

$$\frac{1}{\mu_p} \cdot \frac{\partial \mu_p}{\partial T} + \frac{2}{T} - \frac{(V_{DD} - V_{BIAS}) - V_{TH0}}{m_0 \cdot V_{T0} \cdot T} = \frac{\left(\left[\frac{\partial(V_{DD} - V_{BIAS})}{\partial T} - \frac{\partial V_{TH}}{\partial T} \right] \right)}{m_0 \cdot V_{T0}} \quad (4.11)$$

where T is the room temperature in Kelvin (300K). Transistors M_1 - M_6 generates a bias voltage insensitive to V_{TH} variations as discussed before. Hence, R.H.S for (4.11) is zero. Rearranging (4.11) it can be shown that by choosing a specific value of V_{DD} - V_{BIAS} additional compensation could be avoided.

$$V_{DD} - V_{BIAS} = |V_{TH0}| + m_0 \cdot V_{T0} \left[T/\mu_p \cdot \frac{\partial \mu_p}{\partial T} + 2 \right] \quad (4.12)$$

The source follower M_7 - M_8 generates the desired DC shift. However, the achievable process and temperature compensation are limited by the local mismatch between transistors. This limitation could be improved by trimming the transistor M_{DC3} by setting the switches $SW<0:15>$ on or off, using external calibration (Figure 4.9).

Figure 4.9: 5000-point Monte Carlo simulation results

Figure 4.9 demonstrates Monte Carlo simulation results of 5k points. It could be seen that the proposed reference achieves σ/μ of 0.0175 compared to 0.2075 without any compensation. M_1 has to be biased in strong inversion region for the proposed compensation scheme to be effective. Hence, the threshold voltage of the given technology limits the minimum operating voltage of the current source.

4.2.2 Differential VCO

Figure 4.10: Schematic representation for differential VCO

For making K_{VCO} independent of process and temperature, we propose a truly differential VCO structure as depicted in Figure 4.10. This VCO is analogous to a differential pair with a tail current source and a diode connected the load. Tail current source sets the operating point of the circuit and sets the g_m of the identical input pair transistors. The frequency of oscillation of the VCO is

$$F_{VCO} = 1/(2 \cdot t_D \cdot N) \quad (4.13)$$

where N is the total number of delay stages and t_D is the delay for one delay stage approximately given by

$$t_D = C_D V_{osc} / I_{VCO} \quad (4.14)$$

where C_D is the capacitance seen at each delay node, V_{osc} is the voltage of oscillation and I_{VCO} is the current supplied to the VCO by the control transistor. Additional current generated by the control transistor for any input V_{IN} is

$$\partial I_{VCO} = g_m \cdot V_{IN} \quad (4.15)$$

Combining (4.13), (4.14) and (4.15)

$$K_{VCO} = \frac{\partial F_{VCO}}{V_{IN}} = (g_m \cdot F_{VCO}) / I_{VCO} \quad (4.16)$$

Hence K_{VCO} could be set by setting g_m and I_{VCO} for the circuit. The bias voltage needed for the robust operation of tail current source and DAC current cell is generated using the proposed current reference generator. Effects of variation and mismatch on differential pair transistors and VCOs on the ADC performance are analyzed in the subsequent sections.

4.2.3 Schematic details for the proposed $\Delta\Sigma$ MODULATOR

Figure 4.11 depicts the circuit implementation of the proposed $\Delta\Sigma$ modulator. For simplicity, only the positive half of the VCO is shown. A current domain oscillator used in [45] demands low input impedance, which is hard to achieve at the ultra-low supply voltage. Hence, we use a voltage domain oscillator that eliminates such input impedance requirements. The feedback current, I_{DAC} is converted to a voltage using the resistor, R_{in} . A voltage proportional to the difference between the input and the feedback voltage is generated at the input of each VCO is given by (4.17).

Figure 4.11: Circuit implementation for $\Delta\Sigma$ modulator

$$x(t) = V_{IN}(t) - (I_{DAC+}(n-1) - I_{DAC-}(n-1))/2 \quad (4.17)$$

Where $I_{DAC+(n-1)}$ is the feedback current from the previous sample, I_{DAC} is the total DAC current and R_{IN} is the resistance at the input as shown in Figure 4.11. Each VCO consists of 27 delay stages implemented by simple inverters. The K_{VCO} is designed to be equal to the sampling frequency. The buffered output of the 27 stages collectively holds the instantaneous phase information of the VCO. The phases of both VCOs are compared by a XOR gate (Φ -Comparator) and are sampled using a DFF (Φ -Sampler). The DAC driver prevents the DAC switches turning off at the

same time by generating an overlapping switching pattern. This architecture offers an inherent Clocked Averaging Dynamic Element Matched (CLA-DEM) output [4], which rotates the selection of the DAC elements with the speed of twice the VCO center frequency. Hence, the mismatches in the multi-bit DAC will be up-converted around twice of the VCO center frequency. Reverse short channel effect and inverse narrow width effect were considered when implementing the proposed ultra-low voltage $\Delta\Sigma$ modulator in 65nm technology.

4.3 Design considerations

This section gives guidelines on non-idealities associated with the circuits and design practices to be followed to minimize its effect.

4.3.1 Non-idealities in the differential VCO

Figure 4.12: 1000 Points Monte-Carlo simulation results for variation in VCO frequency

Two main non-idealities associated with differential VCO are the variation of the K_{VCO} and the mismatch between them. From (4.13) and (4.14) one could note that F_{VCO} depends on VCO bias current I_{VCO} and node capacitance C_D . Since the tail

current source is variation tolerant, I_{VCO} could be assumed as constant. However, variations in gate capacitance will change K_{VCO} and would cause SNR variations as depicted in Figure 4.4. Results of 1000 points Monte-Carlo simulation to determine variation in F_{VCO} , for a fixed input current, is illustrated in Figure 4.12. The σ/μ for variation in F_{VCO} is 0.028, which is significantly smaller than the variations in drain current. Mismatch in the K_{VCO} of the oscillators arises from mismatches in the control transistor and/or mismatches between the ring oscillator. In either case, the feedback loop forces the ring oscillators to oscillate at the same frequency by adding an offset.

Figure 4.13: Simulation results for mismatch between the K_{VCO} s in dual VCO integrator

Figure 4.13 shows the results of the $\Delta\Sigma$ modulator simulated using behavior models having K_{VCO} mismatches. It could be observed that the output offset and hence the average input bias voltage of the VCOs changes linearly with different mismatches. As a result, the maximum stable amplitude for the modulator might get affected

because of the change in offset. Another non-ideality is non-linear voltage to the frequency characteristic of the VCO causing higher order distortions as discussed in [45]. However, since the inputs to the VCOs are diminished due to the multi-bit feedback, distortions arising from the VCOs or the mismatch between the VCOs are not a major concern

4.3.2 Quantization noise leaching due to CLA-DEM

Theory and intuition behind the CLA-DEM offered by dual-VCO based integrators have been thoroughly analyzed in [45]. Intrinsic CLA-DEM provided by dual VCO-integrator is useful, as it modulates the distortions arising from DAC mismatches to a higher frequency. However, one significant drawback of the CLA-DEM is the quantization noise leaching due to inter-modulation effect from CLA-DEM. This problem is worsened by the increased mismatch between the current cells when operated in the sub-threshold regime.

Figure 4.14: Simulation setup to demonstrate quantization noise aliasing by CLA DEM

Consider the setup in Figure 4.14 to understand the intuition behind quantization noise leaching. In Figure 4.14, the output of an N-bit quantizer is fed to a CLA-DEM block followed by a non-linear thermometer DAC. The CLA-DEM is set to rotate the DAC elements at 20KHz (F_{CLA}), emulating the rotational effect caused by the

VCO. A DC input to the quantizer generates a quantized DC output, which is converted to a rotational thermometer code by the CLA-DEM. The resultant code, when fed to the non-linear DAC, generates several tones (F_{CLA} , $3 \cdot F_{CLA}$, etc.) at the output of the DAC. Time domain and frequency domain representation of which is illustrate in Figure 4.15(a) and Figure 4.15(b) respectively.

Figure 4.15: (a) Zero mean time domain response for a DC input to Figure 4.14, (b) frequency spectrum of the output (c) frequency spectrum of the output for a sinusoid input to Figure 4.14

The same setup is then excited by a sinusoid of frequency 22.5KHz. A frequency component at 2.5KHz, which was absent in the input, could be observed in the frequency spectrum of the output in Figure 4.15(c). This new component is the result of inter-modulation between F_{CLA} and input sinusoid.

Intuitively, in the presence of a mismatch, CLA-DEM modulates its input data stream around the frequency of element rotation. Any frequency component between the frequency $F_{CLA}-BW$ and $F_{CLA}+BW$ in the DAC input finds its way into the signal bandwidth (BW). It should also be noted that all higher order tones caused by the CLA-DEM result in intermodulation products, i.e. a frequency of 62KHz in the input would cause a 2KHz at the output, so on and so forth. However, since the amplitudes of higher order tone are inferior, F_{CLA} and $3 \cdot F_{CLA}$ are the major contributors for the intermodulation tones. In the case of dual VCO-integrator based $\Delta\Sigma$ modulator, the shaped out-of-band quantization noise around F_{CLA} and $3 \cdot F_{CLA}$, etc. seeps inside the bandwidth and degrade the SNR. The amount of in-band noise depends on the amount of mismatch between DAC cells and the quantization noise power density around the CLA-DEM tones F_{CLA} and $4 \cdot F_{CLA}$. Figure 4.16 shows the output spectrum of a first-order $\Delta\Sigma$ modulator with 5-bit quantizer having a non-linear DAC simulated with and without CLA-DEM. With CLA-DEM the harmonics from DAC mismatch are modulated as higher order tone. Nonetheless, quantization noise floor in the signal band has also increased. Figure 4.17 plots the SNR for dual VCO-integrator based first-order $\Delta\Sigma$ modulator for different DAC mismatches. It could be noticed that SNR degrades with increased mismatch. In a dual-VCO quantizer, VCO-frequency has to be carefully chosen, so that noise power density around twice the VCO frequency does not increase the in-band noise.

Figure 4.16: FFT spectrum for a first order $\Delta\Sigma$ modulator with 5-bit quantizer with and without CLA-DEM for DAC

Figure 4.17: Variation in SNDR with DAC unit cell mismatch

4.3.3 Intrinsic noise sources in the Modulator

Figure 4.18: (a) Phase noise, (b) input referred noise in V^2/Hz for the VCO.

For a dual VCO-integrator based first-order $\Delta\Sigma$ modulator as shown in Figure 4.11, there are three primary sources of intrinsic noise. Phase noise from the VCO, thermal noise caused by the input resistor (R_{IN}) and flicker/thermal noise contributed by the NMOS current DAC and PMOS current source. Since the target bandwidth is low, VCO phase noise caused by the flicker noise sources in the differential VCO is also significant. The phase noise plot of the VCO is as shown in Figure 4.18(a) VCO phase noise has its flicker noise corner around 100Hz. The input referred noise density for a typical VCO at a frequency, Δf , can be computed from its phase noise ($\mathcal{L}\{\Delta f\}$.) at a frequency offset, Δf , from its carrier frequency F_C ,

$$V_{noise-VCO}\{\Delta f\} = N \cdot 10^{\mathcal{L}\{\Delta f\}/20} / |2 \cdot \pi \cdot K_{VCO}/S|^2 \quad (4.18)$$

where $2\pi K_{VCO}/S$ is the voltage to phase transfer function of the VCO, and N is the number of output phases used for the VCO. The resulting input referred noise density spectrum is as shown in Figure 4.18(b). The integrated input referred noise power over 10KHz bandwidth is 0.48nV^2 . The noise contribution from input resistance and

current source/DAC are dependent on the amount of current chosen for the unit DAC cell. The factors determining optimum current for DAC unit cell would be discussed in the next subsection.

4.3.4 Designing for optimum Figure of Merit.

Figure of merit (FoM) of the modulator could be calculated as

$$FoM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}} \quad (4.19)$$

where, BW is the Nyquist bandwidth desired. To obtain lower FoM lower power consumption and high SNDR is desired over a given bandwidth. For reducing total power, minimizing DAC current would look like the obvious choice. A primary limiting factor in reducing DAC current is the mismatch between unit DAC-cells. With reduced DAC current, mismatch increases substantially leading to quantization noise leaching as discussed in 4.3.2. It also demands larger input resistor, R_{IN} , so as to maintain rail-to-rail input signal swing. Thus, reduced DAC current also increases intrinsic noise from R_{IN} and current DAC. Figure 4.19(a) shows simulated results for different noise sources on the unit-DAC current cell. FoM and ENOB obtained from these simulations is plotted in Figure 4.19(b). The minimum energy/conv.-step Achieved by the modulator is for 21nA of unit DAC current.

Another factor that affects the choice of DAC current cell is an excess delay of the continuous-time $\Delta\Sigma$ loop. The gate capacitances and other parasitic capacitances associated with the input node of the differential VCO amount to approx 200fF (from post-layout simulations). This stray capacitance adds a parasitic pole to the transfer function causing excess loop delay. As per (4.16) the input node is charged and discharged using the feedback DAC. Lesser values of DAC current increases the loop

delay by moving the parasitic pole closer to the origin. Figure 4.19(c) illustrates the simulated results for excess loop delay with different unit-DAC cell values. For DAC current lesser than 21nA, the loop delay exceeds more than 20% of the sampling time, which is not recommended. Consequently, the unit value of DAC current for the modulator was fixed as 21nA.

Figure 4.19: (a) DAC unit-cell current vs. circuit noise, (b) DAC unit-cell current vs. performance of the modulator and (c) DAC unit-cell current vs. excess loop delay in the modulator

4.4 Measurement results

The proposed $\Delta\Sigma$ modulator is fabricated in 65nm CMOS process. At 0.3 V, the proposed $\Delta\Sigma$ modulator consumes 400 nW, and the reference current generator dissipates 110 nW. An additional current reference circuit, with compensated and uncompensated current sources, was also implemented in the same die.

Figure 4.20: Measurement results for Current Reference vs. temperature.

Figure 4.20 depicts the measurement results for temperature compensation for the proposed current reference across 10 test chips with and without compensation. Calibration for the current source as discussed in section 4.2.1 was performed off-chip. After calibration, the proposed current reference measures a temperature coefficient of 940PPM/ $^{\circ}$ C averaged across ten chips, against an uncompensated current-reference measuring nearly 18000ppm/ $^{\circ}$ C. Figure 4.21 shows the measured spectrum with a 2031.25Hz and 0.29Vpp-diff input. The $\Delta\Sigma$ modulator achieves a peak SNDR of 56.1dB over a 10 kHz signal bandwidth. From the spectrum, it could be observed that non-linear voltage to frequency characteristic of the VCO is greatly

suppressed. Upconverted DAC mismatches and VCO delay cell, mismatches are seen in the FFT spectrum because of the inherent CLA-DEM offered by the architecture. A peaking in the spectrum around 200 KHz is due to excess delay in the loop caused by the delay from the parasitic pole at VCO input, VCO-buffer, XOR-gates, DAC driver, etc. The time domain representation of the output is depicted in Figure 4.22.

Figure 4.21: Measured FFT spectrum of the output.

Figure 4.22: Measured time domain representation of output code

Figure 4.23 shows the relationship between SNDR and the input amplitude. The modulator becomes unstable for the input greater than 0.29 V as those amplitudes cause a phase roll-off in the VCO. Figure 4.24 summarizes measured peak SNDR from 10 test chips across the target temperature range. Measured SNDR varies only by 3.5dB.

Figure 4.23: Measured SNDR vs. Input amplitude

Figure 4.24: Measured SNDR vs. Temperature for 10 test chips

Figure 4.25 Test chip micrograph

The test chip photo is depicted in Figure 4.25, where the $\Delta\Sigma$ modulator core and the reference current generator occupy the combined area of 0.015mm². Table 4-1 summarizes the test chip results and compares this work with other ultra-low power $\Delta\Sigma$ modulators. The proposed VCO-based $\Delta\Sigma$ modulator achieved a FoM of 49fJ/conv.-step that is the lowest among the similar works.

Table 4-1: Performance Comparison for ultra-low voltage VCO-integrator based $\Delta\Sigma$ modulator with other state-of-the-art works.

Parameter	[54]	[53]	[46]	[44]	This work
Process (nm)	130	130	180	90	65
Supply (V)	0.25	0.25	1/0.5	0.2	0.3
Active Area (mm ²)	0.337	0.74	0.06	NA	0.015
Sampling Freq. (MHz)	1.4	1.28	0.25	12	1.28
Bandwidth (KHz)	10	10	2	20	10
Peak SNDR (dB)	61	73.3	58.5	60.3	56.1
ENOB	9.84	11.88	9.42	9.72	9.02
Power (μW)	7.5	35.6	0.379	7.5	0.51
FoM* (fJ/Conv.-Step)	409	471	137	82	49

4.5 Need for Higher order Modulators

This thesis has proposed two first order continuous time $\Delta\Sigma$ modulators using VCO-based integrators/quantizer. Even though they could work at very low operating voltages there are two limitations. First order continuous time $\Delta\Sigma$ modulators generates idle tones for DC inputs, which needs to be mitigated. Dithering of inputs with self-cancelling pseudo random inputs is one way to circumvent the same [17]. Secondly, first order continuous time $\Delta\Sigma$ modulators have a limited dynamic range which may not be enough for some sensor applications. To increase the dynamic range, oversampling ratio can be increased, which may result in increased power consumption and complexity. Alternate energy-efficient approach is to use higher order delta sigma modulators [85]. SNR achievable for such modulators is depicted in Figure 4.26. Many publications have demonstrated the use of VCO-based integrator/quantizer in higher order loops [2, 42, 56, 58]. Chapter 5 of this thesis demonstrates one such possibility of higher order modulator using VCO-based integrator, which reports a larger SNR and dynamic range for sensory applications.

Figure 4.26 SNR of a $\Delta\Sigma$ modulator vs. OSR and Order of the loop [85]

Chapter 5 Ultra-low power Capacitance to Digital Converter for Microphone-based Auscultation

This chapter proposes an application for VCO-based integrator/quantizer in data converters for ultra-low power applications. It will be shown that continuous-time operation and multi-bit quantization using VCO-based integrators can be leveraged to implement energy efficient Capacitance to Digital Converters (CDC).

In the recent past, there has been a rise in fatality due to heart diseases [69]. Inadequate hospital and diagnostic facilities in low/medium income countries add to the woes [70]. Electrocardiogram (ECG) is a popular technique used for diagnostics. Nevertheless, ECGs have difficulties in detecting structural abnormalities of the heart. Many of the heart conditions could be correlated with or observed from the sounds produced by the heart, while in operation [71]. Listening to heart sounds or heart-auscultation as it is defined, can lead to early detection/monitoring of diastolic dysfunctions in the human heart [72]. Listening to heart sound requires sophisticated skills and expertise. The recent emergence of electronic monitoring paved the way for the development of non-invasive, highly sensitive, sound recording system with cardiac sound wave characterization. However, the usability of such systems is limited to hospitals and diagnostic centers as the setup is expensive and bulky. Therefore, it would be highly desirable to have low cost, compact and portable systems that could continuously monitor heart sounds. Thus, any irregularities in heart sound pattern, for heart patients, could call for immediate attention.

Figure 5.1: (a) Wireless data acquisition using electronic-stethoscope attached externally (b) Primary heart sounds S1, S2 and murmurs between them [5].

Artistic representation of one such system is illustrated in Figure 5.1 where a wearable device can monitor heart sound and wirelessly transfer relevant data for diagnosis. Such a system requires building blocks such as sensors/interface circuitry that can record data with high sensitivity and accuracy. Capacitive MEMS microphones, whose electrical capacitance is modulated by the acoustic pressure wave from the heart sound, are an excellent choice for the recording device. Capacitive data thus obtained can be converted to digital code by using a CDC. Along with CDC, the heart sound monitoring system also requires signal processing and classification unit, which detects any irregularities in heart sounds. If any dysfunctions are detected, wireless transceivers could communicate the same for emergency response. Entire system would be battery operated and compact enough to be made wearable as an electronic-stethoscope. Figure 5.2 represents the block diagram for the same.

Figure 5.2: Block diagram representation of electronic-stethoscope with wireless monitoring

Even though, the capacitive sensors are passive devices with zero static power consumption, the energy consumption is dominated by that of the interface circuit that converts capacitance value to a digital output. In this chapter, problems associated with designing energy efficient Capacitance to Digital Converter (CDC), for a system similar to the one in Figure 5.2, will be highlighted. A novel architecture for the CDC, which embeds a Capacitance to Voltage Converter (CVC) in a continuous-time $\Delta\Sigma$ modulator with VCO-integrator/quantizer CDC, is proposed. Design considerations for circuit schematic will be carefully analyzed, and measurement results for a test chip will be discussed. Comparison with other state-of-the-art CDCs will be drawn in the end. In previous chapters, VCO-based ADCs were operated at a ultra-low voltage for better FoM. On the other hand, CDC proposed in this chapter will be operating at 1.2V to achieve higher energy efficiency for the reasons that will be explained later in this chapter.

5.1 System requirements for the sensing interface

The specifications for a capacitive sensing interface vary with its end application. For a heart sound monitoring system, these specifications arise from various factors such as characteristics of the sensor, ambience in which it is deployed and overall power

budgeting. A brief discussion on the specifications needed for the capacitive sensor interface for a heart sound monitoring system is included in this section.

5.1.1 Dynamic range

Dynamic range for the heart sounds alone, required to diagnose heart conditions is not very high. However, the dynamic range of the CDC is decided by the presence of ambient disturbances internal and external to the converter. Internal disturbances are mainly a group of signals originating internally to the human body such as digestive, respiratory processes. Noise from speech, motion, etc constitute the external disturbances which are high in intensity and wide in bandwidth. Apart from these, there could be occasional disturbances arising during the measurement such as muscle movements, rubbing, and other ambient sources, which have to be dealt with while devising the algorithms for signal processing. It is estimated that sensor and interface should have a dynamic range as large as 100dB to tackle all the unwanted signals, which might be present.

5.1.2 Sensing resolution

Desired sensing resolution could be derived using the dynamic range sought and the characteristic of the sensing device. An electrical model of a typical capacitive sensor is represented in Figure 5.3. C_X is the fixed baseline capacitance of the sensor and ΔC_X is the dynamic capacitance, which represents the measurand such as pressure, humidity, etc. The sensor has parasitic resistances high-value shunt resistance, R_{SHUNT} , (in the range of $G\Omega$) and low-value series resistance R_{SERIES} , (in the range of Ω). Parasitic capacitances, C_{P1} and C_{P2} , associated with capacitor plates and their connecting wires, with reference to ground nodes, are crucial. Sensing resolution is the smallest capacitance change that could be detected [7].

$$C_{resolution} = \frac{\Delta C_X}{2 \cdot \sqrt{2} \cdot 10^{DR/20}} \quad (5.1)$$

where DR is the desired dynamic range, in dB.

Figure 5.3: Electrical model for the sensing capacitor

5.1.3 Measurement Time

Characteristic heart sounds consisting of systolic, diastolic waveforms and various murmurs, comprise a signal bandwidth of around 4KHz. To successfully reproduce the waveform rate of sampling should be at least twice the maximum frequency, i.e. Nyquist sampling frequency is 8KHz. Thus, the desired sensing interface should measure the capacitance of the sensing element once every Nyquist sampling interval i.e. Maximum measurement time allowed is 125 μ S.

5.1.4 Parasitic Capacitance/ Static Capacitance rejection

The electrical model of the sensing element in Figure 5.3 depicts few unwanted capacitive information such as fixed baseline capacitance of the sensor and parasitic capacitors associated with the plates. The desired sensing interface should inherently reject the measurement of such stray capacitance, as they do not produce any meaningful information. It is often noticed that the value of such stray

capacitances, which typically measure a few Pico-farads, results in increased noise floor for the CDC [73]. The proposed sensor interface should be capable of rejecting/overriding any spurious effects of such capacitances.

5.1.5 Power Consumption

Since the desired heart sound monitoring system is a battery operated remote device, power consumption is a vital specification. Since sensing interface will be continuously operated ultra-low power consumption is highly recommended as it directly affects the battery life of the system.

5.2 Recently Proposed Methods

Recently there has been much focus on ultra-low power energy efficient CDCs. The designs could be broadly classified as follows

- a) Capacitance to Voltage Conversion followed by ADC
- b) Discrete Time Delta Sigma Modulators
- c) Period/Duty Cycle Modulation
- d) Other architectures for CDC

Few state-of-the-art designs/architectures published in the near past would be reviewed based on the system requirements discussed in the previous section.

5.2.1 Capacitance to Voltage Conversion followed by ADC

Conceptual diagram of a typical CVC followed by ADC is as shown in Figure 5.4. During pre-charge phase $\Phi 1$, the sensor capacitor, C_X and the reference capacitance C_{REF} are pre-charged to $V_{CM}-GND$ and $VDD-V_{CM}$ respectively. Feedback capacitor C_F is entirely discharged. During the sampling phase, $\Phi 2$, the voltage generated at

the output of the CVC is proportional to the difference between C_X and C_{REF} . The choice of C_F determines the voltage gain or in turn sensitivity of the CDC.

$$V_{OUT} = \frac{2 \cdot (C_X - C_{REF})}{C_F} \cdot V_{CM} \quad (5.2)$$

Figure 5.4: Conceptual diagram representing a CVC followed by ADC

Several state-of-the-art designs demonstrate continuous-time and discrete-time variants of the method illustrated in Figure 5.4 [74-76]. The circuit inherently rejects parasitic capacitances associated with either node of C_X . Popular techniques like correlated double sampling and system chopping mitigate issues related to common mode noise and offset/flicker noise of the circuit respectively. Even though the architecture could be implemented for lower power consumption and finer resolution, the dynamic range of measurement is limited by the voltage swing at V_{OUT} . It becomes more challenging to increase the voltage swing at lower technologies with lower operating voltage. Also, the intrinsic noise requirements of CVC and ADC are equally decisive in terms SNR. Therefore, more biasing current is needed for both the stages resulting in reduced energy efficiency.

5.2.2 Discrete Time Delta Sigma Modulators

Figure 5.5: Discrete Time Delta Sigma Modulators implemented using switched capacitor integrators.

Delta Sigma ($\Delta\Sigma$) modulation is a popular technique when high resolution is desired. Discrete Time $\Delta\Sigma$ Modulators (DT- $\Delta\Sigma$ M), implemented using switched capacitor integrators are predominantly used for the same [73, 77]. Figure 5.5 illustrates a typical implementation of a DT- $\Delta\Sigma$ M. The bit density of the output bit stream, D_{OUT} , is a measure of the ratio of C_X/C_{DAC} and is synchronized with the system clock. Finer resolution could be obtained by filtering and decimating D_{OUT} outside the loop. The sensing capacitor, C_X , is used as the sampling capacitor for the first integrator. The output bit stream controls the connectivity for the capacitive DAC, C_{DAC} , in the feedback path. V_{OUT} is proportional to C_X , if D is zero or $C_X - C_{DAC}$ if D is one. The op-amp balances the charges contributed by C_X and C_{DAC} and integrates the difference onto C_F , DT- $\Delta\Sigma$ M could achieve very good resolution with reasonable measurement time. However, there are two main disadvantages for this technique. The sampling operation at the input in DT- $\Delta\Sigma$ M causes noise folding and results in increased KT/C noise [78] thereby reducing SNR. Even though SNR can be

improved by increasing the OSR, increased OSR will degrade the energy efficiency as the op-amp gain bandwidth and settling time should be improved proportionately. Secondly, DT- $\Delta\Sigma$ employs sensing capacitor as the sampling capacitor for the modulator. Hence, large off-chip and parasitic capacitors are charged and discharged at the same rate as sampling frequency that consumes additional energy.

5.2.3 Period/Duty Cycle Modulation

Figure 5.6: CDC realized using period modulation[1]

Period modulation is another technique used to achieve higher resolution [1, 79]. The capacitive information is converted to duty cycle or frequency using oscillators, typically relaxation oscillators. Pictorial representation of one such implementation is in Figure 5.6. In the first clock phase, Φ_1 , the sensing element C_x is charged to a voltage $V_{DD}-V_{CM}$. In the second clock phase, Φ_2 , C_x is forced to discharge into C_{int} through the virtual ground of the op-amp. In the same clock phase, a constant current source, I_{int} , flushes the charge in C_{int} to replenish the original voltage level. The time

taken for the current source (T_{msm}), measured from starting of Φ_2 , in bringing back the voltage, V_{int} , to its original level is

$$T_{msm} = \frac{V_{DD}}{I_{int}} \cdot C_X \quad (5.3)$$

In such type of CDCs resolution and measurement time are to be traded against each other. Therefore, for applications like microphone-based auscultation, where faster measurement time and higher resolution is desired, period modulation may not be very attractive. The need for a high-resolution time reference also decreases the overall power efficiency of the system.

5.2.4 Other architectures for CDC

Figure 5.7: Iterative delay-chain method for Capacitance to Digital Conversion

In [80] Wanyeong et.al discuss iterative delay-chain discharge method for implementing CDC. The sensor capacitor, C_{SENSOR} , shown in Figure 5.7 is pre-charged to a high voltage V_{HIGH} and is discharged through a chain of delay elements, arranged as a ring oscillator. The number of transitions made by the delay-chain with reference to a reference delay is a function of charge stored in C_{SENSOR} , which in turn is a measure of its capacitance. Architecture uses three consecutive measurements with different connectivity for the C_{SENSOR} to reject parasitic capacitances and one

point calibration to improve temperature/supply voltage insensitivity [80]. Advantages of this technique are its ultra-low power consumption and fast measurement time. However, the sensing resolution is limited by the current sensitivity of the delay chain. In our proposed scheme of heart sound monitoring, we would need to measure sub-fF change in capacitance. Such small capacitance change would produce little or no change in number of transitions in the proposed technique, thereby limiting the sensing resolution.

Figure 5.8: Zoom-in architecture using asynchronous SAR and second order DT- $\Delta\Sigma$ [7]

S. Oh et.al have proposed an interesting zoom-in architecture for implementing energy efficient high-resolution CDCs[7]. As depicted in Figure 5.8, it uses an asynchronous SAR for coarse quantization and a second order DT- $\Delta\Sigma$ as a fine quantizer. In the coarse cycle, Comparator and asynchronous logic in the SAR path balance the charges in sensor capacitance against the 9-bit feedback path. By the end of the coarse cycle, voltages at the inputs of the comparator would be nearly same. In the fine quantization cycle, the difference between C_{DAC} and C_x would be digitized.

Zoom-in architecture alleviates the noise/resolution requirements for the $\Delta\Sigma$ modulator, thereby increasing energy efficiency. One major disadvantage of this approach is that the same sensor capacitor is used during coarse and fine cycle as the input device. Thus, a fast change in C_X is not appreciated during the fine cycle, as it destabilizes the loop [81]. Eventhough the design reports lower FoM, its usability is limited to slow changing or quasi-static capacitance measurements.

Continuous-Time $\Delta\Sigma$ Modulator (CT- $\Delta\Sigma$) on the other hand does not have these problems as the sampling is performed just before the quantizer. Existing CT- $\Delta\Sigma$ (Section 5.2.1), however, needs an additional CVC, which increases power consumption. In addition to it, the dynamic range of the CDC is limited by the voltage swing at the output of CVC. In this chapter, a novel CT- $\Delta\Sigma$ that embeds CVC inside a second order $\Delta\Sigma$ modulator is introduced. This work also employs dual VCOs as an integrator, which also provides multi-bit quantization that alleviates the output swing/biasing current requirements for the amplifiers. Since the actual sensor to be used is still under development a normalized sensing range of 0-10pF is considered in designing the interface.

5.3 Proposed CDC Architecture using CT- $\Delta\Sigma$

5.3.1 Conventional Capacitance to Voltage Conversion

Figure 5.9 shows a conventional CVC that performs charge balancing. The sensor capacitor, C_X , and a reference capacitance C_{REF} are connected in series between VDD and GND. C_{REF} could be selected to cancel out any baseline capacitance of the sensor. C_F is the feedback capacitor; R_{PSEUDO} is a bias resistor, and C_{P1} and C_{P2} are parasitic capacitances associated with sensor capacitor plates. The negative feedback in the amplifier sets the virtual ground to V_{CM} , i.e. $VDD/2$. The readout process then

transfers the charge difference between C_X and C_{REF} to C_F . By virtue of charge balancing, the output voltage, V_{OUT} , can be derived by

$$V_{out} = \frac{C_{REF} - C_X}{C_F} \cdot \frac{V_{DD}}{2} \quad (5.4)$$

Figure 5.9: Capacitance to voltage convertor based on charge balancing

Thus, the output voltage of the continuous-time CVC is indicative of the sensor capacitance value, which is immune to parasitic capacitance C_{P1} , and C_{P2} . A traditional CT- $\Delta\Sigma$ could be used for digitizing the output of the CVC. However, such implementation is not energy efficient as both CVC and the first integrator of the CT- $\Delta\Sigma$ modulator need to meet noise requirements, which increases the current consumption.

5.3.2 Proposed structure with CVC embedded in a CT- $\Delta\Sigma$

In the proposed structure, the CVC performs delta operation inside a CT- $\Delta\Sigma$ modulator as shown in Figure 5.10. Thus, the voltage gain from the CVC alleviates the noise requirements of the integrator that follows the CVC. For simplicity, a one-bit quantizer and DAC are shown. A capacitor, C_{DAC} , is used to feedback the output.

One end of C_{DAC} is tied to the floating node and the other end is switched between V_{DD} and GND depending on the previous output using a switch, SW/SWB. The

Figure 5.10: CVC embedded inside CT- $\Delta\Sigma$ M

switch when set to 1 or 0, positions C_{DAC} parallel to either C_X or C_{REF} respectively, which in turn balances the charge for all the capacitances connected to virtual ground. With every switching, C_{DAC} is charged/discharged from $-V_{CM}$ to V_{CM} or vice versa. Hence, the amount of charge pumped in or out by C_{DAC} for every switching is $\pm C_{DAC} \cdot 2 \cdot V_{CM}$. By virtue of this charge balancing the output of the amplifier from (3.3) becomes

$$V_{out} = \frac{C_{REF} - C_X \pm 2 \cdot C_{DAC}}{C_F} \cdot \frac{V_{DD}}{2} \quad (5.5)$$

If $2 \cdot C_{DAC}$ corresponds to the quantized value of C_X from the previous sampling interval, then the circuit in Figure 5.10, performs the delta operation in a $\Delta\Sigma$ modulator. Thus, the circuit embedded in a $\Delta\Sigma$ loop makes a CT- $\Delta\Sigma$ Modulator. The

value of capacitance C_F sets the gain of the CVC. Even though smaller value of C_F is better for sensitivity, it would increase the swing at the output of the CVC. Thus choosing an optimum value of C_F makes the proposed architecture energy efficient. Detailed analysis of the tradeoffs will be provided in the subsequent sections.

5.3.3 Differential operation for the CVC embedded in a CT- $\Delta\Sigma$

Figure 5.11: Differential operation for CVC connected in full bridge configuration

Since the virtual grounds of the amplifier in Figure 5.11 are connected to capacitors, a large pseudo resistor is used to set the DC bias at the input of the amplifier. This pseudo-resistor adds an undesired zero with the capacitor C_F at the frequency around a few tens of Hz. Thus, the noise transfer function (NTF) of the loop is modified and in-band quantization noise increases. To mitigate this problem capacitive input and the quantization noise within the bandwidth of interest have to be chopped to a higher frequency. To facilitate chopping, differential operation is widely

recommended. Differential operation also helps in rejecting any common mode noise coming from supply or other sources. Two single-ended capacitive sensors are arranged in a full bridge configuration with differential chopping as illustrated in Figure 5.11, so that it imitates a differential sensor. The inputs to the CVC are chopped to a higher frequency and are chopped back at the output of the CVC, thereby avoiding the undesired zero in the signal path. Since, chopping could also take care of the input offset and low-frequency flicker noise of the amplifier, the chopping frequency is chosen to be larger than the flicker corner of the op-amp. Design considerations for choosing the chopping frequency and op-amp specifications will be covered in section 5.4 .

5.3.4 Proposed architecture for the CDC using second order CT- $\Delta\Sigma$ with multi-bit quantization

Figure 5.12: Architecture for the 2nd order CT- $\Delta\Sigma$ Modulator

The proposed architecture showing CVC embedded in a second order $\Delta\Sigma$ loop is in Figure 5.12. The coefficients for loop filter and feedback DAC indicated corresponds to a normalized sampling frequency of 1Hz. An active-RC integrator and a VCO-integrator act as the loop filters for the loop. A cascade of integrators with distributed feedback (CIFB) topology is chosen for the modulator to keep the inputs to the VCO within its linear range of operation. CVC is designed with a voltage gain of 'k' so that

noise requirements of the amplifier used in RC integrator could be relaxed. Choice of CVC gain 'k' is instrumental in deciding the energy efficiency and performance of the modulator. The VCO-integrator also performs a 5-bit quantization. Multi-bit quantization serves two purposes. It keeps VCO-based integrator in its linear range of operation and it reduces the swing at the output of CVC there by alleviating its design requirements. The quantized output is fed back to the CVC for charge balancing using a multi-bit capacitive DAC. The targeted application, heart sound monitoring, demands recording over a nyquist bandwidth of 4 kHz. The modulator is designed for an OSR of 125 with a 1MHz sampling clock.

5.4 Design considerations for the CDC using second order CT- $\Delta\Sigma$ with multi-bit quantization

Since CDC comprises of various blocks, careful design and analysis at top level and block level is needed to maximize the overall efficiency. Various such considerations have been tabulated in this section. Since most of the considerations are mutually inclusive, the optimum design parameters could be found only by multiple iterations.

5.4.1 CVC chopping considerations

In the CDC implementation for microphone based auscultation, bandwidth of interest is very low, consequently low frequency noise components from the circuit has to be kept minimum. Chopping is an effective method to get rid of amplifier offset and low frequency flicker noise. Nonetheless, chopping innately brings few issues associated with it. Finite gain bandwidth of the op-amp causes a voltage swing at the virtual ground input of the amplifier. Chopping causes sudden changes in voltage levels

across the parasitic capacitances at the virtual ground input as well as at the output of the amplifier. Since the change in voltage occurs twice in every chopping cycle, any frequency component in the signal above twice the chopping frequency gets aliased [49]. In case of a $\Delta\Sigma$ modulator, if chopping frequency is lesser than the sampling frequency, out of band quantization noise higher than twice the chopping frequency aliases in band degrading SNR [49].

Figure 5.13: (a) CVC operating in continuous time with system chopping and (b) Effects of chopping at different voltage nodes of the CVC

Consider a standalone CVC in Figure 5.13, chopped using a signal $\text{chop}(t)$ with a period $2 \cdot N \cdot T$, where N is any positive real number and T is the sampling period. At every chopping instance, $N \cdot T$, input capacitances are chopped between V_{DD} and GND as indicated. The change in charge in capacitors C_X and C_{REF} is given by $\pm C_X \cdot V_{DD}$, $\pm C_{REF} \cdot V_{DD}$ respectively. Algebraic sum of charges for the capacitors connected to one virtual ground could be mathematically represented as

$$Q_{SUM}(NT) = (C_X(NT) \cdot V_{DD} + C_{REF} \cdot V_{DD}) \cdot chop(kNT) \quad (5.6)$$

$$\text{Where, } chop(kNT) = \begin{cases} -1, \forall k = 1,3,5.. \\ +1, \forall k = 2,4,6.. \end{cases}$$

where $C_X(NT)$ is the capacitance of the sensing element at time NT . Change in output voltage at node A occurs after a finite time τ owing to the finite gain bandwidth of the op-amp and resistance of the chopping switch. The voltage also depends on $Q_{SUM}(NT)$ stored on C_F . Output at the node A at time NT is

$$V_{CVCA}(NT) = \frac{(C_X(NT - \tau) \cdot V_{DD} + C_{REF} \cdot V_{DD}) \cdot chop(kNT - \tau)}{C_F} \quad (5.7)$$

This output is chopped back using $chop(NT)$ thus output at node B at time NT is

$$V_{CVC}(NT) = \frac{(C_X(NT - \tau) \cdot V_{DD} + C_{REF} \cdot V_{DD}) \cdot chop(kNT - \tau) \cdot chop(kNT)}{C_F} \quad (5.8)$$

$$V_{CVC}(NT + \tau) = \frac{(C_X(NT) \cdot V_{DD} + C_{REF} \cdot V_{DD}) \cdot chop(kNT) \cdot chop(kNT + \tau)}{C_F} \quad (5.9)$$

From 5.8 and 5.9 it could be seen that the presence of finite delay, τ , leaves a small chopping residue, which would be absent, if $\tau=0$ as

$$chop(kNT) \cdot chop(kNT) = 1, \forall k. \quad (5.10)$$

This results in aliasing of signals above twice the chopping frequency. Intuitively the changes in voltage $V_{CVC}(NT)$ and $V_{CVC}(NT + \tau)$ causes a glitch as indicated in Figure 5.13(b). Signal multiplied by the chopping residue at the output in (5.8) and (5.9) is equivalent to sampling V_{CVC} at a sampling period NT . If V_{CVC} contains signal components, having period smaller than NT , they get aliased. From (5.8) and (5.9), it is clear that aliased noise power is a function of the chopping frequency used, the swing at the output and delay τ due to the gain bandwidth of the op-amp and

resistance of the chopping switches. Please note that, similar effect occurs at the virtual ground of the op-amp, due to node capacitances and finite op-amp gain, which is not analyzed since the swing at the output is more significant.

5.4.2 Effect of chopping frequency on quantization noise aliasing

Figure 5.14: CVC embedded in a higher order $\Delta\Sigma$ loop

Since a CVC embedded in higher order $\Delta\Sigma$ loop (Figure 5.14), performs delta operation, out of band quantization noise power is significantly large. Therefore the effect of signal aliasing due to chopping is more dominant, than for an integrator in $\Delta\Sigma$ loop as discussed in [49]. For this reason, chopping frequency has to be carefully chosen for the CVC to minimize aliasing. For the CVC embedded in a $\Delta\Sigma$ loop sampling the output of the integrator at 1MHz makes the output spectrum repeat every 1MHz (Figure 5.15). The output is fed back using an NRZ DAC, which in this case simply holds the sampled output for one clock cycle. The impulse/frequency response of the NRZ DAC is portrayed in Figure 5.16. It could be observed that

Figure 5.15: Output spectrum for a $\Delta\Sigma$ Modulator sampled at 1 MHz

Figure 5.16: (a) Impulse response (b) Frequency response of the NRZ DAC

NRZ DAC, which has the frequency characteristic as a *SINC* function, acts as a low pass filter on the sampled spectrum. To understand the effect of chopping frequency on aliased noise let us look at an arbitrary set of frequency. In the absence of chopping, there is no possibility of aliasing. If the frequency of chopping is gradually increased to an arbitrary value of $F_s/16$, quantization noise aliases from multiples of frequency $F_s/8$ (as indicated by the red lines) in Figure 5.17. However, the degradation in SNR is not as dramatic as one expects because aliasing occurs from both the positive and the negative sides of the spectrum. Since the aliased components from both the sides are correlated and opposite in magnitude they tend to cancel out. Nevertheless, since the sinc filter effect of the NRZ DAC causes a small degradation in the high frequency components, cancellation is not complete leaving a residue that degrades the SNR. If one continues to increase the chopping frequency to $F_s/4$, aliasing effect results in maximum increase in in-band noise. As shown in the Figure 5.18, aliasing happens only from frequencies $F_s/2$ and its multiples, which constitute only from one side of the spectrum. Thus, aliasing results in correlated summation of the total noise, increasing the in-band noise floor. On increasing the chopping frequency further to $5 \cdot F_s/16$, it could be visualized that frequencies from both the sides of spectrum starts aliasing in-band. This effect results in reduced in-band noise, due to cancellation effect as discussed before. When CVC is chopped at a frequency equal to $F_s/2$, the multiples of sampling frequency, F_s , alias into the signal band. It is easy to note that the amount of quantization noise present could be considered insignificant to alias. This results in increased SNR when chopped at these frequencies. The effects are similar for a chopping frequency of F_s . A CVC embedded in a second order $\Delta\Sigma$ loop was simulated across chopping frequencies. The

Figure 5.17: Quantization noise aliasing from the multiples of $F_s/8$ as indicated by the red lines

Figure 5.18: Quantization noise aliasing from the multiples of $F_s/2$ as indicated by the red lines

Figure 5.19: SNR vs. chopping frequency for 1MHz sampling frequency

gain bandwidth of op-amp used was around 25MHz and switch resistance corresponds to a V_{GS} of 1.2V. Swing at the output of CVC was limited to 150mV. Without including the effect of flicker-noise or other noise sources SNR was plotted against chopping frequency. Resultant graph illustrated in Figure 5.19 reflects the pattern in SNR as discussed above. SNR is the best for chopping frequencies 0, $F_S/2$ and F_S . It is worst for frequencies $F_S/4$ and $3 \cdot F_S/4$. Hence, the ideal choice of chopping frequency is either $F_S/2$ or F_S .

5.4.3 Optimum frequency for chopping

Increased the chopping frequency also comes with inherent issues. One of the major challenges is the mismatch in the channel resistance of the switches. Even though switch resistance is not important for chopping frequencies $F_S/2$ or F_S . The mismatch in switch resistance is quite crucial as they cause distortion. Effect of mismatch is exacerbated with higher chopping frequency as chopping switches

would be activated more often. For an application like auscultation, distortion added by the data converter should be as low as possible. Amount of distortion could be controlled by minimizing the effect of mismatch. Two alternate ways for the same are to increase gate-source voltage (V_{GS}) of the switch, so that mismatch reduces, or by decreasing the chopping frequency. Figure 5.20 shows simulation results for behaviour models to validate both ways. It could be seen that similar SNDR numbers can be achieved by choosing lower chopping frequency and lower V_{GS} for the switch.

Figure 5.20: SNDR vs. V_{DD} for different chopping frequencies

Furthermore, chopping decreases the output impedance of the amplifier leading to reduced gain-bandwidth, which adds to the loop delay. Thus, higher cut-off for chopping frequency cannot be as large as $F_s/2$. For maximizing SNR of the circuit, optimum choice of chopping frequency would be double the $1/f$ noise corner of the CVC, as the amount of quantization noise aliasing and harmonic distortion due to chopping could be kept minimum. For this design, optimum chopping frequency was found to be $F_s/64$.

5.4.4 Choosing CVC gain

Larger CVC gain leads to larger voltage swing at the output of CVC. As seen from (5.8) and (5.9) increased voltage swing at the output increases quantization noise aliasing. However, larger CVC gain is needed to reduce the effect of intrinsic noises added by the integrator. Even though the use of multi-bit quantizer helps in reducing the swing at the output of CVC, CVC gain is instrumental in determining the SNR achieved by the modulator. Choice of CVC gain must be a tradeoff between two considerations for a given amount of current consumption. Behavioral model simulations for a CVC embedded in second order $\Delta\Sigma$ loop gives an estimate about the desired gain. 5-bit quantizer was used to reduce swing at the output and an op-amp with 25MHz gain bandwidth was used for implementing CVC. CVC was chopped at 15.625 KHz and active-RC integrator was chopped at 500KHz.

Figure 5.21: SNDR vs. CVC gain after considering intrinsic noises

Intrinsic noises such as flicker noise and thermal noise were also included in the model. Figure 5.21 illustrates SNDR vs. CVC gain plot from multiple simulations. From the figure, it is seen that lower CVC gain causes more intrinsic noise and higher CVC gain increases the quantization noise aliasing it could be noted that CVC gain of two maximizes the SNDR.

5.4.5 Finite gain bandwidth of the amplifiers

Figure 5.22 SNDR and FoM plotted against gain bandwidth of the CVC amplifier

Gain bandwidth of the CVC is instrumental in reducing the effects of aliased quantization noise from chopping and in decreasing the loop delay of the loop. Similarly, gain bandwidth of the active-RC integrator affects the performance of the loop by increasing the excess loop delay and by reducing the RC-time constant of integration. However, choice of gain-bandwidth is directly proportional to the current consumption by the amplifier. Since CVC is detrimental in the overall performance

of the system, it is important to analyze it carefully. Behavioral model simulations were repeated for a CVC embedded in second order $\Delta\Sigma$ loop with 5-bit quantizer, to find optimum gain bandwidth of the CVC considering overall Figure of Merit (FoM). CVC was chopped at 15.625 KHz and active-RC integrator was chopped at 500KHz. intrinsic noise such as flicker noise and thermal noise were also included in the model. FoM is computed using the equation

$$FoM = \frac{Power * Measurement Time}{2^{\left(\frac{SNDR-1.76}{6.02}\right)}} \quad (5.11)$$

Figure 5.22 demonstrates the results of the simulation. For improved efficiency gain bandwidth of the amplifier should be at least 15MHz.

5.4.6 Noise Considerations for the CDC

Figure 5.23 Intrinsic noise sources in the $\Delta\Sigma$ loop

Fundamental limit for energy efficiency of most of the high resolution $\Delta\Sigma$ modulators is set by the intrinsic noise sources. For the CDC proposed in this thesis,

there are two major contributors of noise, CVC and active-RC integrator. Noise added by second integrator is often not considered as it is assumed to be shaped out of the spectrum by the first stage. Low frequency flicker noise from the devices is taken care by chopping, but thermal noise remains. SNR could be defined using the noise source V_N in Figure 5.23 as follows

$$SNR = \frac{(C_X/C_F \cdot V_{DD}/2)^2}{\int_0^{BW} V_N^2} \quad (5.12)$$

where BW is the bandwidth of the modulator, V_N^2 (V^2/Hz) is the total noise in the modulator referred to the output of the CVC and C_X/C_F is the signal gain from the CVC. Equation (5.12) gives a good estimate of the amount of noise that could be tolerated to obtain a desired SNR. It should be noted from (5.12) that SNR is dependent on the VDD used. Hence, larger VDD is desirable for CDCs unlike data converters using VCO-based ADCs where lower VDD yields better FoM. Noise contribution from CVC at its output is

$$V_{CVC-noise}^2 = \frac{(C_X + C_{REF} + C_P + C_{DAC})}{C_F} \cdot V_{IN}^2 \quad (5.13)$$

where C_P is the parasitic capacitance associated with bottom plate of the sensor and input of the CVC amplifier. It is to be noted that, noise contribution from CVC is amplified significantly due to all the capacitances associated with the virtual ground node. Since CVC gain is set to two, it is desirable to set the noise contribution from rest of the loop to be approximately equal to that of CVC.

$$V_N^2 \approx 2 \cdot V_{CVC-noise}^2 \quad (5.14)$$

5.5 Schematic Implementation

Based on the design considerations, the system architecture has been modified as shown in the Figure 5.24. Gain of the CVC is set to two. Owing to CIFB configuration of the architecture, swing at the output of the integrator will be large. Reducing the swing at the output improves linearity. Hence, the coefficient of the active-RC integrator coefficient is scaled down to $1/4^{\text{th}}$ the actual value. Feedback to the VCO-integrator is current feedback and feedback to CVC is using capacitive DAC. All the circuit blocks were designed in $0.18\mu\text{m}$ technology to operate at 1.2V .

Figure 5.24 Architecture diagram for CDC embedded in 2^{nd} order $\Delta\Sigma$ loop

5.5.1 Second order CT- $\Delta\Sigma$ with dual VCO-based integrator

Figure 5.25 shows the circuit implementation for the CDC architecture in . In the example implementation, we have used a chopping frequency of 15.625 KHz . Lowering V_{DD} increases the mismatches in the chopping switches. Therefore, choosing a lower chopping frequency reduces the distortion added by the mismatches in the chopping switches. The output of the CVC is integrated using an active RC integrator. Even though noise requirements of the integrator are alleviated by the gain of the CVC, input offset and flicker noise from the amplifier could degrade the

overall SNR. Hence, the active-RC integrator is also chopped. Unlike the CVC, the amount of charge handled by the chopping switches for RC-integrator is much lesser. This enables us to use a higher chopping frequency of 500KHz.

A dual VCO-based integrator is used as the second integrator [45]. The phase of a VCO is proportional to the integral of its input. Thus, the VCO can act as a linear integrator if the input to the VCO is within its linear range. Comparing the phase outputs of dual VCOs with differential inputs gives integral of the input. Sampling this multi-phase output using a D-Flip-flop (DFF) quantizes the phase in the time domain. A multi-bit NRZ current DAC is used in the feedback path (I_{DAC+}/I_{DAC-}). The output from the active-RC integrator is converted to current (I_{RIN}) using resistance R_{IN} . From KCL, algebraic sum of currents entering and leaving input node of the VCO (positive half) should be zero

$$I_{RIN} + \frac{I_{DAC}}{2} + I_{BIAS} + I_{DAC+} + I_{VCO} = 0 \quad (5.15)$$

Where I_{BIAS} is the biasing current to the VCO, I_{VCO} is any residue current sunk by the VCO and I_{DAC} is the full scale current of the DAC. I_{VCO} acts as the input to the VCO and causes the change in oscillation frequency for the VCO. Multi-bit feedback keeps the input to the VCO (I_{VCO}) within the linear range of the VCO. A VCO made up of 31 stages of differential inverters performs 5-bit quantization. A 5-bit quantized value used in the capacitive feedback reduces the swing at the output of CVC. This cuts down the noise aliasing from the chopping and the current consumption. The output of the VCO-based integrator is inherently Clocked Level Averaged (CLA), which is one form of Dynamic Element Matching (DEM) technique [6]. CLA output

Figure 5.25: Schematic details of proposed CDC with 2nd order $\Sigma\Delta$ modulator

of the VCO modulates any nonlinearity arising from DAC mismatches around twice the center frequency of VCO. The active-RC integrator provides first order shaping for the intrinsic noise contribution from the VCO obviating the need for additional noise reduction techniques. Bias voltages needed for amplifiers, VCO and current DAC were internally generated using self-cascode bias circuits. All the analysis for dual-VCO integrator discussed in Chapter 4 has been considered while designing.

5.5.2 OTA design

Figure 5.26: Symmetric cross-coupled OTA with common mode feedback

Symmetric cross-coupled OTA, as shown in Figure 5.26, was used for designing CVC and an active-RC integrator. This circuit topology was chosen considering its large gain bandwidth and ability to drive resistive loads with given amount of current. Use of OTA instead of op-amp helps in achieving larger gain bandwidth for the amplifiers, which is desirable as per the discussions before. Cross-coupled transistors M_5 and M_6 offer a negative g_m , and boost the DC gain of the OTA. Since transistors M_3 - M_6 were the predominant contributors for the flicker noise, PMOS transistors were used for the same. A pair of resistors and single ended output from a differential amplifier with diode-connected loads sets the output common mode voltage. Owing to the CIFB architecture, the swing at the output for the OTA used in the active-RC integrator is large. Consequently, output chopping for the active RC integrator was performed at node 'A' as indicated in Figure 5.26. This helps in minimizing the distortions added by the chopping. The design parameters for the amplifiers used in CVC and integrator are given in Table 5-1.

Table 5-1: Amplifier Design Parameters

Parameters	CVC	Integrator
Open loop Gain (dB)	50.7	38.2
Phase Margin (degrees)	55	47.5
Unity Gain Bandwidth (MHz)	25	17
CMFB Phase margin (degrees)	75	69
Thermal noise floor after Chopping (nV/ $\sqrt{\text{Hz}}$)	206 (at output)	125 (at input)
Total current (uA)	21	14

5.5.3 VCO-design

Figure 5.27: 31-Stage VCO with differential inverter delay cells

As mentioned before dual VCO-based integrator as the second integrator. 31-stages of differential inverter based delay cell make the VCO. Differential inverters with cross-coupled PMOS devices were chosen as delay cells since it could to achieve wider tuning range at lower operating frequencies. The free running frequency and input resistance of the VCO is set by the bias current, I_{BIAS} . For the architecture in figure the coefficient of VCO-integrator (K_{VCO}) should be twice the sampling frequency i.e. 2MHz/V. Figure 5.28 illustrates a simplified model for different circuit components at the input of a VCO. R_{VCO} is the input resistance of the VCO, V_{CTRL} is the voltage at the input node. The tuning coefficient for the VCO, K_{VCO} could be calculated by measuring frequency change, Δf , for a ΔV_{CTRL} change in input voltage.

$$K_{VCO} = \Delta f / \Delta V_{CTRL} \quad (5.15)$$

Figure 5.28: Simplified model for VCO, DAC and input signal

However, V_{CTRL} is not directly controlled and is a function of voltage at integrator output V_{INT+} , input resistor R_{IN} and input resistance R_{VCO} etc.

$$V_{CTRL} = \left[\frac{(V_{INT+})}{(R + R_{VCO})} + I_{DAC}/2 - I_{DAC+} \right] \cdot R_{VCO} \quad (5.16)$$

Thus for the design of K_{VCO} , several parameters like swing at the output of the integrator, input resistor used, input resistance of VCO designed and unit DAC current chosen are to be considered.

Table 5-2: VCO design parameters

Design Parameter	Value
Bias current for a VCO (I_{Bias})	0.5u
Input resistance of the VCO (R_{VCO})	50K
Free running frequency of the VCO (F_C)	60KHz
Input resistor used (R_{IN})	250K
Total DAC current (I_{DAC})	3uA

Table 5-2 shows a list of parameters and its values for the VCO designed. As in depth analysis of VCO-based integrators have been included in Chapter 4, further details are skipped in this design.

5.6 Other Non-ideal effects

Even though several design considerations were put into practice while devising architecture and circuit specifications some non-ideal effects were ignored. Impact of such non-ideal effects will be discussed briefly in this section.

5.6.1 Finite gain / Gain Bandwidth for the amplifier in active-RC integrator

Active-RC integrator acts as the first integrator in the proposed architecture. It is assumed that the first integrator will shape noise contribution from current DAC and VCO. Since the finite gain of the amplifier is less, active-RC integrator would have a non-zero pole frequency. Thus, the low frequency components of intrinsic noise from DAC and VCO seeps in-band deteriorating SNR. Another consideration is the effect of finite gain bandwidth of the amplifier on the loop coefficients. To ensure stability and to maximize the SNR loop coefficients of the modulator have to be computed after considering finite bandwidth of amplifiers. For this test design, such effects have been neglected. Excess loop delay caused by amplifiers in CVC, active-RC integrator, VCO-integrator and DAC drivers are also considered negligible.

5.6.2 Mismatch between sensor capacitors

Proposed architecture uses two single ended capacitors arranged in full-bridge configuration to emulate differential operation. However, in the actual application of heart sound monitoring, where sound waves will be modulated into capacitances by

the sensors, mismatch between two sensor capacitances will be crucial. Mismatch could arise from imperfections in fabrication, differences in physical location/orientation of sensor or presence of other ambient noises. Mismatches could be broadly classified as two types namely offset mismatch or gain mismatch. From the circuit implementation in figure, it could be understood by intuition that, under steady state conditions, offset mismatch would translate to offset error in the digital output. While gain mismatch between the sensors decreases the sensing gain or in the worst case, inability to track both the halves makes the loop unstable. These problems could be mitigated by the use of one time/periodic calibration for the CDC. Alternate solution is the use of differential sensors, which obviates any such non-idealities.

5.6.3 Effect of PVT variations

As seen from the above sections, three major design blocks in the architecture are OTA, VCO and Current DAC. All the three circuit elements are biased using a current reference, which sets the operating condition for the same. In the absence of a stable current reference any variation in PVT causes changes the DC gain and gain bandwidth of the OTA. This would degrade the SNR of the topology as indicated in Figure 5.22. Similarly change of bias current would cause increase in in-band quantization noise and may even result in instability as discussed in section 4.1.1. Hence stable reference is of at most importance. In this work, stable bias references were generated off-chip using self cascoded biasing circuits. This helped to deal with any PVT variations.

5.7 Measurement results

Figure 5.29: Die photograph

Figure 5.30: Alternate setup to measure SNR and SNDR

The die photograph of the fabricated chip is shown in Figure 5.29. An alternate setup as shown in Figure 5.30 was used to emulate a sinusoidal change in capacitance. Differential sinusoid with 500 mVpp amplitude at 1.34 KHz frequency, which corresponds to a change in capacitance from 0.8 pF to 9.2 pF at the same frequency, was used for measurement. Thus, a target bandwidth of 4 KHz is equivalent to the measurement time of 0.125ms. The sampling frequency is 1MHz. Figure 5.31 shows the FFT spectrum for 2^{14} output samples, convolved with a hanning window. Similar FFT spectrum measured for a static capacitance of 10pF is superimposed in the same figure. The output spectrum shows the chopping spurs at 15.625 KHz and up-converted DAC mismatches around twice the center frequency of the VCO. Non-idealities such as excess loop delay and finite gain bandwidth distorts the spectrum above 100 KHz. The proposed CDC achieves an SNR of 79.2dB over its full range of 0-10pF corresponding to an effective resolution of approximately 0.36 fF. The CDC

Figure 5.31: Measured output spectrum for sinusoidal input and fixed capacitance

consumes 42 μA current from a 1.2 V supply resulting in a FoM of 0.84 pJ/Conv.-step. Table 5-3 compares the proposed design with state of the art ones. Even though the design proposed in [3], using zoom-in architecture with coarse and fine quantization, reports lower FoM, its usability is limited to slow changing or static capacitance measurements. It is evident from the FoM that the proposed continuous time implementation alleviates the noise requirements of the circuit components, thereby reducing current consumption. The VCO-based integrator/multi-bit quantizer helps to reduce the voltage swing at the output of the CVC, which improves the overall energy efficiency. The proposed design could be interfaced with capacitive MEMS microphone for auscultation purposes or other capacitive sensors for ultra-low power applications.

Table 5-3: Comparison table with other state-of-the-art CDCs

Parameter	[2]	[3]	[4]	[5]	This work
Process (nm)	160	180	350	350	180
Method	Period Mod:	DT- $\Delta\Sigma\text{M}$	DT- $\Delta\Sigma\text{M}$	DT- $\Delta\Sigma\text{M}$	CT-$\Delta\Sigma\text{M}$
Input range (pF)	0-8	0-24	NA	0.5-1	0-10
Measurement Time(ms)	6.86	0.23	0.02	0.8	0.125
SNR (dB)	80.6	94.7	104.7	69.6	79.2
ENOB	13.09	15.43	17.09	11,3	12.9
Power (μW)	14	33.7	15000	10.3	50.4
FoM* (pJ/Conv.-Step)	10.6	0.175 $\dagger$	5.5	3.4	0.84

$\dagger$ could be used only with slow moving or static cap measurements

*FoM = Power $\times$ Measurement Time/ 2^{ENOB}

Chapter 6 Conclusion and Future scope

6.1 Conclusion

This thesis presented two architectures and circuit techniques for ultra-low voltage/power VCO-based ADCs. Chapter 3 introduced a novel calibration algorithm and its circuit implementation to correct distortions added by VCO-FDSM operating at the ultra-low supply voltage. The nonlinearity information of the VCO is calculated by measuring the intermodulation terms from the FDSM output from an input, which is the sum of sinusoids. Two main factors, which contribute to the effectiveness of the proposed calibration scheme, are the minimum use of analog circuitry enabling low voltage operation and fast calibration cycle that allows intermittent operation of the calibration block, thereby saving the power. The proposed calibration algorithm is the fastest among existing algorithms. A functioning prototype validates the effectiveness of the calibration scheme at 0.4V. The SNDR and SFDR improved considerably after the calibration cycle. The FoM is comparable to the state of the art designs. The resolution is limited by the phase noise of the VCO caused by some layout imperfections. Careful design of VCO for lower phase noise can yield a better resolution. Currently, the operating voltage is limited by the use of logic cells from standard cell libraries. Design could operate at lower supply voltages with the use of custom designed standard cell libraries.

In Chapter 4, first order closed loop $\Sigma\Delta$ modulator with a novel truly differential VCO and self-compensated current reference for variation tolerance. The proposed current reference operates at 0.3V, which is the lowest operating voltage in current reference circuits known to the authors. A test chip operating at an ultra-low voltage

as low as 0.3V was implemented in 65nm CMOS technology. Measurement results demonstrate that proposed $\Sigma\Delta$ modulator achieved a FoM of 49fJ/conv.-step. Careful analysis of CLA-DEM and other noise sources were instrumental in choosing the optimum value of DAC current which was instrumental in reducing overall power consumption. For the test chip implemented, SNR is limited by the phase noise added by the VCO. The SNR and FoM could be further improved by the careful design of the VCO and the current DAC for better noise performance. Figure 6.1 and Figure 6.2 plots the Walden FoM and Schreier FoM respectively for the proposed VCO-based data converters alongside other state-of-the-art ADCs similar to the illustration in Figure 1.6 and Figure 1.7. It could be clearly noticed that proposed ADCs have moved their FoM closer to the limits set by technology and noise in comparison to similar works.

Figure 6.1: Walden FoM vs. V_{DD} for this work alongside state-of-the-art ADCs.

Figure 6.2: Schreier FoM vs. V_{DD} for this work alongside state-of-the-art ADCs

Chapter 5 proposes an application for VCO-based integrator/quantizer in ultra-low power wireless sensor node applications. A novel CDC that embeds a CVC inside a CT- $\Delta\Sigma$ modulator was introduced. The proposed continuous time implementation alleviates the noise requirements of the circuit components, thereby reducing current consumption. The VCO-based integrator/multi-bit quantizer increases the dynamic range of the CVC output without increasing the voltage swing at the output of the CVC, which improves the overall energy efficiency. The test chip fabricated in 0.18 μm technology demonstrates that measuring capacitance in continuous time achieves better FoM over existing DT- $\Delta\Sigma$ M or period modulation techniques [1, 7, 73, 77, 82]. The proposed design could be interfaced with capacitive MEMS microphone for auscultation purposes or other capacitive sensors for ultra-low power applications.

6.2 Future Scope

VCO-based ADCs are promising candidates for data converter, which are very much in its early stage of research and development. Plethora of issues needs to be addressed and corrected before it can become mainstream data converters, especially in ultra-low voltage/power regime. In this thesis, basic building blocks for a VCO-based $\Delta\Sigma$ modulator were introduced that still has room for improvement. Calibration accuracy for VCO-based quantizer in Chapter 3 is affected by the mismatch between signal VCOs and replica VCOs. It is advisable to include mismatch reduction techniques such as a fine-tuning logic to ensure robust performance. Alternatively, it is worthwhile to inspect possibilities to improve calibration times for background calibration technique without replica VCO, similar to the one in [66] or [83].

Dual VCO-based integrator discussed in Chapter 4 is a good candidate for ultra-low power operation. They offer intrinsic CLA-DEM to minimize distortion from static and dynamic errors in the DAC. However, DAC mismatch degrades the SNR as discussed in Chapter 4. The amount of noise seeping in-band would be larger in higher order modulators. One possible solution is to introduce nulls in the frequency spectrum of the digital input to the DAC, around the CLA-DEM frequency, so that effect of inter-modulation could be minimized. However, such techniques come with inherent stability issues that should be tackled.

The proposed circuit blocks from Chapter 3, and Chapter 4 could be cascaded to build VCO only higher order modulators [84]. Unlike, higher order continuous-time $\Delta\Sigma$ modulators such as [49] where the performance of the modulator is limited by intrinsic gain of the amplifier, VCO based integrators could offer ideal integration

with zero pole frequency. However, it needs additional glue elements like DAC and Digital to Time Converter that increases the complexity and power consumption. Thus higher order continuous-time $\Delta\Sigma$ modulators using purely VCO-integrators and quantizer is a new dimension for research.

This thesis was concluded by proposing a continuous-time $\Delta\Sigma$ modulator for capacitance to digital conversion, which is a research topic by itself. In the proposed solution, the signal to noise ratio is limited by limitations in CVC design, namely intrinsic noise and chopping noise aliasing. The presence of additional capacitances in the input such C_{DAC} worsens the SNR and energy efficiency. Alternate CVC could be proposed to minimize noise gain and maximize signal gain. Novel feedback ideas like FIR-DAC could be introduced [49] to lessen the effect of noise aliasing due to chopping. Proposed architecture in Chapter 5 could also be modified to incorporate a zoom-in mode where a coarse quantization follows a fine quantization to increase energy efficiency.

List of Publications

Conference Papers

- [1] N. Narasimman and T. Kim, "Design Challenges for VCO based ADCs for Ultra-Low Power Operation," *International SoC Design Conference (ISOC)*, pp. 249-252, Nov. 2013
- [2] "An Ultra-low Voltage VCO-based ADC with Digital Background Calibration", N. Narasimman and T. Kim, *International Symposium on Circuits and Systems (ISCAS)*, May. 2016
- [3] "A 0.3 V, 49fJ/Conversion/Step VCO-based __ Modulator with Self-compensated Current Reference for Variation Tolerance ", N. Narasimman and T. Kim, *ESSCIRC*, Sept. 2016
- [4] "A 1.2 V, 0.84 pJ/Conv.-Step Ultra-low Power Capacitance to Digital Converter for Microphone based Auscultation," N. Narasimman, D. Nag, K. C. T. Chuan, and T. Kim, *CICC*, May. 2017

Journal Papers

- [5] "Design and Analysis of 0.3 V, 49fJ/Conversion/Step __ Modulator with dual VCO integrator using Self-compensated Current Reference for Variation Tolerance ", N. Narasimman and T. Kim, *IEEE JSSC* (in submission)
- [6] "Continuous time Sigma delta modulator for capacitance to digital conversion used in ultra low power application", N. Narasimman, D. Nag, K.T.C.Chai and T. Kim. *IEEE JSSC* (in submission)
- [7] "Effects of chopping in a closed loop Sigma Delta Modulator", N.Narasimman, D. Nag, K.T.C.Chai and T. Kim. *IEEE Transactions in Circuits and Systems -II* (in submission)

Patents

- [8] "Continuous time Sigma delta modulator for capacitance to digital conversion used in ultra low power application", N. Narasimman, D. Nag, K.T.C.Chai and T. Kim. *SG PATENT* (Filed)

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