Low power clock generators with digital calibration for sustainable building applications

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**LOW POWER CLOCK GENERATORS WITH
DIGITAL CALIBRATION FOR SUSTAINABLE
BUILDING APPLICATIONS**

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2017

LOW POWER CLOCK GENERATORS WITH DIGITAL CALIBRATION FOR SUSTAINABLE BUILDING APPLICATIONS

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A thesis submitted to the Nanyang Technological University in partial
fulfilment of the requirement for the degree of
Doctor of Philosophy

2017

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

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Date

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Student Name

Abstract

The growth of human population on Earth has increased the awareness on the need for energy saving. The concept of smart building and life are proposed to connect all household appliances up to clouds to allow users to control these appliances with energy distribution in a smarter manner. With the expansion of mobile device usage and internet cloud applications, we are already moving to the big-data age. At the same time, the rapid developing digital signal processing technique requires the stable clock frequency due to different building environments, such as wide temperature range, variable supply voltage, sunshine time, humidity and so on.

This thesis proposes two relaxation oscillator designs and an all-digital phase locked-loop (ADPLL) design as stable clock frequency generators for the sustainable building applications.

The first proposed design presents a novel on-chip RC relaxation oscillator with split-capacitor integrator compensation loop technique to achieve a stable output frequency with environment temperature and supply voltage variations. It can provide a stable frequency signal at 13.5 MHz. Measurements results show that the output frequency has $\pm 0.5\%$ and $\pm 0.5\%/V$ variation with temperature range of -30°C to 120°C and power supply range of 1.5 – 2.1 V. Moreover, the power consumption of the design yields only 48.8 μW .

The second design is also a relaxation oscillator with digital compensation technique to achieve a stable output frequency with environment temperature and supply voltage variations. The digital compensation scheme can avoid the power hungry analog op-amp integrator feedback loop. The digital method not only save more power in the long run, but is easier when comes

to CMOS process scaling. Furthermore, an on-chip reference pulse generator is adopted for the compensation. The digital feedback loop tunes loop delay to adjust the output frequency. The test chips were fabricated in a 0.18- μm standard CMOS process. Effects of this digital compensation method has been verified to maintain frequency stability of the relaxation oscillator. The output frequency is stable at 12.77 MHz at 0.9-V power supply voltage. Measurement results showed that the output frequency has only 31ppm/ $^{\circ}\text{C}$ variation with temperature range of -30 to 120 $^{\circ}\text{C}$ after compensation. The frequency variation over the supply voltage is $\pm 0.5\%/V$. Compared to other state-of-the-art designs, our design achieves better figure of merit (FoM) and has the smallest temperature coefficient. The total power consumption is 56.2 μW when all circuits are enabled. For long term operation, the power consumption can be scaled to only 12.8 μW in the main oscillator.

After introducing the two relaxation oscillators, an all-digital PLL is implemented for digital processing clock signal. In order to reduce power consumption, the proposed ADPLL uses only a flip-flop as the phase detector. The injection locked technique is implemented in this design for jitter performance improvement. The measurement results show that the ADPLL can approach 101 dBc/Hz at 100 kHz offset frequency. This design is taped-out in GLOBALFOUNDRIES 40-nm CMOS process, which only consume about 1.2 mW at 1-GHz output frequency. In future work, it is going to integrate the on-chip relaxation oscillator and digital PLL together to create an entire on-chip clock generation and distribution system.

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Contents

Abstract	ii
Acknowledgment	iii
Table of Contents	vii
Table Captions	ix
Figure Captions	xiv
Abbreviations	xvi
 1 Introduction	 1
1.1 Background and Motivations	1
1.1.1 Sustainable Life and Smart Building	1
1.1.2 Electrical Devices in Smart Building	2
1.2 Clock Generators	5
1.2.1 Off-Chip Clock Generators	5
1.2.2 On-Chip Clock Generators	10
1.3 Objective	15
1.4 Dissertation Overview	15
1.5 Findings and Outcomes	16
References	19
 2 Literature review	 21
2.1 Relaxation Oscillator	21
2.1.1 Conventional On-Chip Relaxation Oscillator	22
2.1.2 Chopper for Offset Cancellation	25
2.1.3 Voltage Averaging Feedback Circuits	27
2.2 All Digital Phase-Locked Loops	29

2.2.1	Conventional Type-II PLL	29
2.2.2	All Digital PLL Architecture	30
2.2.3	ADPLL without TDC	35
2.3	Conclusions	36
	References	41
3	A Relaxation Oscillator with Split-Cap Technique	43
3.1	Introduction and Motivations	43
3.1.1	Radio Frequency Identification	43
3.1.2	Organization	45
3.2	Proposed Relaxation Oscillator with Split-Capacitor Technique	45
3.2.1	The Architecture of Proposed Oscillator	45
3.2.2	Relaxation Oscillator with Split-Capacitor Technique	47
3.2.3	Comparator Offset Cancellation	49
3.2.4	Split-Cap Control Logic	50
3.2.5	Noise Reduction	52
3.3	Measurement Results	55
3.4	Conclusions	59
	References	62
4	A Relaxation Oscillator with Digital Compensation Method	63
4.1	Introduction and Motivations	63
4.1.1	Digital Circuits in CMOS	63
4.1.2	Organization	65
4.2	Proposed Relaxation Oscillator with Digital Compensation .	65
4.2.1	The Architecture of Proposed Relaxation Oscillator .	65
4.2.2	Reference Pulse Generation	69
4.2.3	Time-to-Digital Converter and Loop Delay Controller	71
4.2.4	CTAT current Bias and Resistance Temperature Com- pensation	73
4.3	Proposed Digital Compensation Method	74
4.4	Measurement Results	77
4.5	Conclusions	84

References	87
5 An Digital Phase-Locked Loop with Injection Locked Tech- nique	89
5.1 Introduction and Motivations	89
5.1.1 ISM Band Application	89
5.1.2 Motivation	90
5.1.3 Organization	91
5.2 Digital Phase-Locked Loop Design	91
5.2.1 Architecture of ADPLL	91
5.2.2 System Model	93
5.2.3 Digital Loop Filter	99
5.2.4 Digitally Controlled Oscillator	102
5.3 Injection-Locked Circuits	104
5.3.1 Injection-Locked Oscillators	105
5.3.2 PLLs with Injection-Locked	107
5.3.3 Dual-Loop Injection-Locked PLL	109
5.4 Measurement Results	112
5.5 Conclusions	117
References	120
6 Summaries and Future Work	121
6.1 Summary of Thesis	121
6.2 Future Work	123
6.2.1 An Entire Clock Generator and Network	123
6.2.2 Frequency Synthesizer	125
References	127
A Temperature Effects in Semiconductors	129
B Author's Publications	133

CONTENTS

Table Captions

1.1	The stability of oscillator based on crystal	13
2.1	The comparison of analog PLL and all digital PLL	31
3.1	Relaxation oscillator with split-cap performances summary .	59
4.1	Performance comparison between analog and digital circuits.	64
4.2	Performances summary and comparison	85
5.1	Performance comparison	117

TABLE CAPTIONS

Figure Captions

1.1	All electronic devices are connected to the Cloud service in a smart building [8].	4
1.2	Some clock generators: (from left to right) a quartz crystal resonator, a ceramic resonator and a clock generator IC. . .	6
1.3	Quartz crystal equivalent model circuits.	7
1.4	Quartz crystal output impedance versus frequency.	8
1.5	Pierce oscillator with inverter and feedback network.	11
1.6	Block diagram for a typical TCXO.	12
1.7	Ring oscillator using: 1) five digital inverters, 2) fully differential amplifiers.	14
2.1	(a) Conventional on-chip RC relaxation oscillator, (b) Operating waveforms for the conventional oscillator.	22
2.2	Architecture of the relaxation oscillator with offset compensation.	25
2.3	Operating waveforms for the chopper offset cancellation circuit.	26
2.4	(a) The voltage averaging feedback concept presented in [5], (b) waveform of the oscillation.	28
2.5	Basic architecture of a charge pump PLL.	30
2.6	From analog to all digital PLL.	31
2.7	Cycle interpolation time-to-digital converter (TDC).	33
2.8	(a) Architecture of a Vernier delay-line TDC, (b) speed and resolution comparison among TDCs.	34
2.9	Standard delay cell of digitally-controlled oscillator with driving strength control.	35

FIGURE CAPTIONS

2.10	A block diagram of a bang-bang ADPLL.	36
3.1	Block diagram of an analog frontend for RFID reader.	44
3.2	The proposed relaxation oscillator with split-capacitor technique.	46
3.3	The operating waveforms of the proposed split-capacitor technique in the oscillator at different phases: (a) when ϕ_1 is high; (b) when ϕ_2 is high.	48
3.4	The control logic of split-cap technique.	50
3.5	The operation waveform of the control logics for split-cap.	51
3.6	The noise transfer models of the relaxation oscillator.	53
3.7	The oscillator phase noise simulation results with and without integrator.	55
3.8	Die photograph of the proposed relaxation oscillator with split-capacitor.	55
3.9	Measured oscillation frequency of three chips versus temperature at 1.8-V power supply.	56
3.10	Measured oscillation frequency of three chips versus supply voltage at room temperature.	57
3.11	Measured oscillation phase noise performance.	57
4.1	Architecture of the proposed relaxation oscillator with digital compensation feedback loop.	66
4.2	Waveforms of the proposed relaxation oscillator.	67
4.3	Operating waveforms of the reference pulse generation.	68
4.4	(a) Monte Carlo simulation results of reference pulse at room temperature, (b) Simulated Mean and σ versus temperature.	71
4.5	(a) Schematic diagram of TDC with thermal code output, (b) schematic of digitally controlled delay cell.	72
4.6	Schematic diagram of complementary to absolute temperature (CTAT) current bias.	73
4.7	Resistance temperature compensation by P-poly and N-plus resistors.	75
4.8	Flow chart of the digital compensation algorithm.	76

FIGURE CAPTIONS

4.9	Chip micrograph of proposed relaxation oscillator.	77
4.10	Measured waveform of output frequency and reference pulse.	78
4.11	The simulation power consumption pie chart.	79
4.12	(a) Phase noises performance, (b) period jitters with and without digital compensation.	80
4.13	(a) PCB of measurement, (b) measurement environment.	80
4.14	Measured oscillation frequency and reference pulse width versus temperature at 0.9-V power supply.	81
4.15	Measured oscillation frequency of four chips and with compensation.	81
4.16	Measured oscillation frequency versus supply voltage.	82
4.17	Measured oscillation frequency versus supply voltage of four chips after compensation.	83
5.1	Architecture of the ARM CoreTile Express processor.	90
5.2	Architecture of the proposed all-digital phase-locked loop.	92
5.3	(a) System model of a continuous PLL, (b) circuits model of loop filter in a charge pump PLL.	94
5.4	(a) Step response result of CPLL, (b) Phase margin of CPLL.	96
5.5	Matlab model of whole proposed ADPLL.	97
5.6	(a) Spectre simulation result of system model, (b) time domain waveform simulation results.	98
5.7	(a) Phase noise simulation without injection in system model, (b) with injection.	99
5.8	Transformation of a RC filter to a discrete digital filter.	100
5.9	(a) Frequency locking RTL simulation in Modelsim, (b) Phase locking simulation.	101
5.10	Circuits of digitally controlled oscillator.	102
5.11	(a) Injection circuits in the 2nd DCO stage, (b) DCO fine tuning by capacitors.	104
5.12	(a) MOSFET capacitance cross view, (b) capacitance verses gate and source voltage.	104
5.13	Simulation results of DCO and the DCO layout design.	105

FIGURE CAPTIONS

5.14	Model of an injection-locked oscillator.	106
5.15	Timing issue due to loop delay of ILPLL.	108
5.16	First operation step of the ADPLL.	110
5.17	Second operation step of the ADPLL.	111
5.18	Third operation step of ADPLL and the frequencies variation of three steps.	111
5.19	Injection locked circuits and waveforms.	112
5.20	Design flow of the mixed-signal ADPLL.	113
5.21	Die photograph and layout of the proposed ADPLL.	114
5.22	Measured phase noise output of the ADPLL.	114
5.23	Measured jitter performance of the ADPLL.	115
5.24	The power distribution pie chart.	116
6.1	A clock generation and distribution network example.	124
6.2	A SoC with WLAN and Bluetooth subsystem baseband and processors [1].	125
6.3	A frequency synthesizer block diagram.	126
A.1	Temperature dependence of electron and hole mobilities in Si.	130
A.2	Threshold voltage temperature dependence versus dopant con- centration with oxide thickness d	131

Abbreviations

ADPLL	All Digital Phase Locked Loop
CMOS	Complementary Metal-Oxide-Semiconductor
CTAT	Complementary to Absolute Temperature
DCO	Digitally Controlled Oscillator
FoM	Figure of Merit
HVAC	Heating, Ventilation, and Air Conditioning
IC	Integrated Circuit
ILO	Injection-Locked Oscillator
ILPLL	Injection-Locked PLL
ISM	Industrial, Scientific and Medical
IoT	Internet of Things
LPF	Low Pass Filter
MIM	Metal-Insulator-Metal
MOSFET	The Metal-Oxide-Semiconductor Field-Effect Transistor
OCXO	Oven Controlled Crystal Oscillator
OSC	Oscillator

PCB	Printed Circuit Board
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
PTAT	Proportional to Absolute Temperature
PVT	Process, Supply Voltage and Temperature
RF	Radio Frequency
RTL	Register-Transfer Level
SoC	System on Chip
SVS	Smart Vertical Solution
TCXO	Temperature Compensated Crystal Oscillator
TDC	Time-to-Digital Converter
VCO	Voltage-Controlled Oscillator
WSN	Wireless Sensor Network

Chapter 1

Introduction

This chapter provides the research background and motivation in achieving amongst sustainable life and the importance of having smart buildings. In order to communicate the intelligent devices, wireless sensor networks are widely used in smart home automatic control system. In every electronic device, the fundamental building block is the clock generator, that guarantees reliable and sustainable operation.

1.1 Background and Motivations

1.1.1 Sustainable Life and Smart Building

If the population growth maintains the same growth rate as of today, the global human population will reach 9.6 billion by 2050. In addition, when the population on Earth continues to expend power energy at the same rate, the power consumption will be doubled in 2035, and by 2050 it is forecast that the human race will need the CO₂-absorption capacity and natural resources of three Earths [1]. With the rapid development of

technology, nowadays, the major challenge for the electrical industry is that how to achieve a sustainable daily life within the Earth's limited resources.

In the recent years, the concept of smart home or intelligent building control has been explored and is envisioned to be a solution for sustainable living. A smart building is a structure that uses automated processes to automatically control the building's operations including heating, ventilation, air conditioning, lighting, security and other systems [2, 3]. A smart building uses sensors, actuators and microchips, in order to collect data and manage them according to business functions and services. This infrastructure helps owners, operators and facility managers to improve asset reliability and performance, which reduces energy usage, optimizes space and minimizes the environmental impact of buildings [4].

1.1.2 Electrical Devices in Smart Building

There are many commercial solutions for the intelligent, smart and green buildings in the market. For example: ST8800 UNIZON, Intelligent Building Management System Brochure from ST Electronics Engineering [5]. In this system, it offers a suite of management applications to give users a complete building asset information. To-date, all building control systems are looking at energy management and green environment from a global perspective. By integrating information from the various building subsystems, managers are able to plan, benchmark and optimise energy strategies; and to monitor and manage the condition of indoor air composition and flow of the respective building space.

The Smart Vertical Solution (SVS) system is from Samsung [6], which focuses on improving buildings' HVAC (Heating, Ventilation, and Air Con-

ditioning) systems. The SVS allows large coffee and fast-food franchises to remotely monitor the HVAC environment in all their independent shops, setting the temperature or turning the lights on and off at their discretion, depending on the season or opening hours of each shop. Should trouble occur in the HVAC system at any shop, the SVS can immediately detect it and allow the user to take responsive measures.

The HOMETOUCH's Energy Saving School Solution (ESSS) [7] was helped many schools to reduce energy costs by seamlessly integrating heating and cooling infrastructure, lighting, and other equipment. It can build a fully automated HVAC system with sensors, meters and timers to shut system off when rooms are not in use, thus saving energy. Moreover, timer and real-time temperature monitoring can sense the suitable temperature to limit air-con use.

From the above discussed commercial smart building solutions, many such electronic devices, including sensors, micro-controllers, radio frequency devices and etc., are noted in smart building system to sense the environments, collect data and to control them. Figure 1.1 shows the consumer electronics implemented in our current or future daily lives [8]. In this intelligent house, customers' data are collected and store in the cloud by the electrical smart sensors, to be distributed around the house. The control system improves building's HVAC systems through the Internet of Things (IoT) network [9]. At the same time, customers can also receive entertainment shows and other information from the cloud servers at their own terminals within the smart home.

For the intelligent energy networks in smart building applications, through the use of automated technical infrastructure and physical and digital con-

nections to local energy networks, they offer the possibility to buffer excess electricity from fluctuating renewable sources in thermal and electrical storage units [10]. As such, buildings become an integral part of an intelligent energy network, the so-called smart grid, and are able to do three things: produce, store and consume energy. The trend toward higher integration in buildings can be further developed. The goal of smart building is to optimize human comfort and be sustainable. To do so, further automation function is required in buildings, which is generally known as power management. In addition, such building has to be linked to the needs of the network, for example in the form of variable electricity tariffs or a demand-response function, especially in the case of a decentralized energy supply.

Figure 1.1: All electronic devices are connected to the Cloud service in a smart building [8].

In all electronics systems and customized synchronous digital processing circuits, the digital clock information is used like a metronome to coordi-

nate the activities of digital circuits [11]. For smart building applications, since many electrical sensors are dispersed all around, the devices' working environments are much different. For example, some sensor nodes are implemented outside the buildings, and located in high latitude that may be exposed to -40°C outdoor temperature in the coldest winter. On the contrary, buildings that are located near the equator need work at temperature greater than 40°C and with high humidity. The so varied working environments call for electronic devices even the clock generator blocks, to function well within the wide temperature variations. In the section of follows, clock generators that are popularity deployed in the current market will be described.

1.2 Clock Generators

A clock generator in electronic system is a kind of circuit that produces a continuous, synchronized electrical signal for timing control in a wide variety of devices. In digital circuits, it always generates an alternative high and low signal. Clock generators are often a key component in many devices in order to ensure all other components work synchronously and harmoniously. By the relative position between the clock generators and the electrical system, the clock generator can be divided into two main categories: off-chip clock generator and on-chip generator.

1.2.1 Off-Chip Clock Generators

The most common Off-chip clock generators are generally Quartz Crystal Oscillators, Ceramic Resonators and so on. Figure 1.2 shows the different types of clock generators.

Figure 1.2: Some clock generators: (from left to right) a quartz crystal resonator, a ceramic resonator and a clock generator IC.

I Quartz Crystal Resonator

A quartz crystal resonator is an electronic oscillator circuit that makes use of the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a precise frequency [12]. Generally, the frequency of quartz oscillator are manufactured from a few tens of kilohertz to hundreds of megahertz. Nowadays, they are very widely used in all electronic systems such as wristwatches, radios, computers, cellphones, etc. In the left side of Figure 1.2, it shows a quartz oscillator that has a precise 16-MHz frequency.

When a voltage source signal is added to the two sides of a quartz crystal, the thin crystal is forced to change shape leading to a phenomenon called as the piezoelectric effect [13]. It is also the working principle of crystal oscillators. This piezoelectric effect is the property of a crystal by which an electrical charge produces a mechanical force by changing the shape of the crystal and vice versa, i.e., a mechanical force applied to the crystal to produce an electrical charge. Once the crystal cut and shaped, it cannot be oscillated at any other frequency signal. It is because that its physical characteristics (size, thickness, shape, etc.) determine its intrinsic frequency. The characteristic (oscillation frequency) of crystals is inversely proportional

Figure 1.3: Quartz crystal equivalent model circuits.

to its physical thickness between two thin surfaces. An equivalent electrical circuit can be introduced to a mechanically vibrating crystal, which consists of a low series resistance R_s , a large inductance L_s , a small series capacitance C_s and a large parallel capacitance C_p , as illustrated in Figure 1.3. The circuit in this figure is similar as a series RLC resonance circuit [14].

Using the Laplace transform, the impedance of this equivalent circuit can be written as:

$$Z(s) = \left(\frac{1}{s \cdot C_s} + s \cdot L_s + R_s \right) \parallel \left(\frac{1}{s \cdot C_p} \right) \quad (1.1)$$

It can also be derived as:

$$Z(s) = \frac{s^2 + s \frac{R_s}{L_s} + \omega_s^2}{(s \cdot C_p)(s^2 + s \frac{R_s}{L_s} + \omega_p^2)} \quad (1.2)$$

where ω_s and ω_p can be expressed as:

$$\omega_s = \frac{1}{\sqrt{L_s \cdot C_s}} \quad (1.3)$$

Figure 1.4: Quartz crystal output impedance versus frequency.

$$\omega_p = \sqrt{\frac{C_s + C_p}{L_s \cdot C_s \cdot C_p}} = \omega_s \sqrt{1 + \frac{C_s}{C_p}} \quad (1.4)$$

Figure 1.4 shows the crystal's impedance versus output frequency variation. With the resonant frequency variation, the crystal appears different device characteristics, i.e., capacitive or inductive. The equivalent circuits of the series capacitor C_s and inductor L_s can be expressed as a series resonance oscillator which can reduce the output impedance to a minimum value (R_s). This frequency point is called the crystals series resonant frequency f_s , and below the point, the quartz crystal shows capacitive. As the same definition, there is a special frequency point which is related to the series inductor L_s and parallel capacitor C_p . The inductor and parallel capacitor construct a parallel LC resonation oscillator. This frequency point is defined as parallel resonant frequency (f_p), and the impedance across the crystal reaches its maximum value at f_p . Above the frequency f_p , the crystal also appears capacitive. The crystal performance between two frequency points (f_s and f_p) shows inductive. The value of f_s and f_p is determined by the physical

parameters of a crystal. Moreover, there are two stable oscillation frequency of a crystal (series and parallel resonance), and in some applications, only one required frequency is needed. Therefore, there must be a tuning circuits of crystal oscillator to control a stationary frequency. Generally, the parallel capacitance C_p is much larger than the series capacitance C_s [15]. The two frequencies, f_s and f_p , are very close. That explains why crystal oscillator will always have very high Q-factor (Quality Factor).

The mobility of interstitial ions depends on temperature. Hence, the temperature performance of crystal oscillator is around dozens ppm/°C generally. A more precise frequency performance versus temperature may be desired at time; thus different types kinds of crystal oscillators with temperature compensation circuits, such as the TCXO (Temperature Compensated Crystal Oscillator) and OCXO (Oven Controlled Crystal Oscillator) were developed. Both of them consist of a basic quartz resonator and some more important on-chip compensation circuits, which will be described later in the on-chip generators subsection.

II Ceramic Resonator

There is another electronic component called ceramic resonator. This device is constructed by a piece of a piezoelectric ceramic material with two or more metal electrodes attached for connection. Because of high-stability piezoelectric ceramics, it generally leads zirconium titanate (PZT) and can operate as a mechanical resonator with a high accuracy frequency. Like the quartz crystal, it can be also implemented as a source of clock signal for digital circuits [16].

III Summary

Although these off-chip clock sources offer precise frequency and good frequency stability during environment variations, they are usually made from different materials with varied processes compared to the modern CMOS technology. On the other hand, the industries are moving towards integrating all components of the electronic system onto a single chip, which is called System on Chip (SoC), to reduce the power consumption and cost. These off-chip devices are separated with other electronic systems such as power management, RF circuits, micro-controller, processors, etc. In order to save more power and cost, this research will study and explore using the standard CMOS process to integrate in a single chip.

1.2.2 On-Chip Clock Generators

On-chip clock generators mean that state them are integrated with other electronic systems for precise clock signals. Some of these on-chip clock generators are also based on the off-chip crystal resonators, such as TCXO and OCXO; whereas some are fully on-chip design.

I Pierce Oscillator

In most microprocessors, a crystal oscillator in Pierce configuration is used as a clock named after its inventor, George Pierce [17]. Figure 1.5 shows the fundamental circuits structure.

In the figure, R_f is a feedback resistor which is able to bias the inverter. The inverter with biasing works as a high gain inverting amplifier. The PI-Element C_1 , C_2 and the crystal constitute a narrow bandpass filter with frequency-dependent phase shift. The oscillation condition requires the total

Figure 1.5: Pierce oscillator with inverter and feedback network.

phase shift to be 360° . At the resonant frequency, an inductive activity is appeared. Therefore, the off-chip crystal can be considered a large, high Q inductor. The “inductor” and two capacitors (C_1 and C_2) perform a resonant circuits. In order to oscillate at the desired frequency, it must make sure that the capacitances in the circuit (C_1 and C_2) match the value specified on the crystal’s requirement. The total load capacitance (C_L) can be calculated as:

$$C_L = \frac{(C_1 + C_i) \times (C_2 + C_o)}{C_1 + C_i + C_2 + C_o} + C_S \quad (1.5)$$

where C_i and C_o are the parasitic capacitances of the inverter input and output terminals, respectively. C_S is the stray capacitance from the printed circuit board (PCB), and is generally $2 \sim 3\text{pF}$. This oscillator does not have temperature control or compensation technique. Its frequency-to-temperature coefficient depend on the crystal physical characteristics.

II Temperature Compensated Crystal Oscillator

The Temperature Compensated Crystal Oscillator (TCXO) device has temperature compensation blocks to keep oscillation frequency stable versus surrounding temperature variations. Figure 1.6 shows the block diagram of a typical TCXO structure. The output signal from a compensation block is used to generate a correct voltage that is to be applied to the variable reactance (generally a varactor) in the crystal oscillator circuits. Generally, a TCXO can provide about twenty times improvement over the conventional crystal oscillator's temperature performance.

Figure 1.6: Block diagram for a typical TCXO.

III Oven Controlled Crystal Oscillator

As the name suggested, an Oven Controlled Crystal Oscillator (OCXO) contains an oven block to maintain the variation of temperature. It usually consists of temperature sensors, heating elements, oven circuitry, and insulation functions. By keeping stable the temperature of the crystal and other temperature sensitive components, great improvements in oscillator performance can be realized such that the crystal's frequency versus temperature variation can achieve a zero slope [18]. Table 1.1 summarizes frequency stability of the three types of crystal oscillators versus temperature variations in different temperature range.

From Table 1.1, it is noted that the three types of oscillator can maintain excellent frequency stability versus temperature variation. However, they all

Table 1.1: The stability of oscillator based on crystal

Temperature	Crystal	TCXO	OCXO
0°C to 70°C	$\pm 10\text{ppm}$	$\pm 0.5\text{ppm}$	$\pm 0.003\text{ ppm}$
-20°C to 70°C	$\pm 25\text{ppm}$	$\pm 0.5\text{ppm}$	$\pm 0.003\text{ ppm}$
-40°C to 85°C	$\pm 30\text{ppm}$	$\pm 1\text{ppm}$	$\pm 0.02\text{ ppm}$

consist of off-chip components. In order to save cost and to merge the clock generators with other electronic system on a single chip, this research will focus on oscillator designs based on standard CMOS technology.

IV CMOS Oscillators

There are many different types of CMOS oscillators, but with two main classifications: those that directly generate sinusoidal signals as and those that provides square wave signals from high to low in digital circuits. Some types of oscillators, as a LC tank resonator, can generate a sinusoidal output. The square-output oscillators are usually constructed using a nonlinear feedback circuit such as a relaxation oscillator or a ring oscillator [19]. The LC tank oscillator has higher output frequency and better phase noise performance than a ring oscillator generally. However, the inductor is more difficult to design in standard CMOS process. The LC oscillator also occupies much more silicon area compared to ring or relaxation ones. Based on energy and cost saving, this research will focus on the relaxation oscillator and ring oscillator.

A ring oscillator's operation principle is based on the "Barkhausen's Criteria". Placing odd number of open-loop inverting amplifiers in a feedback loop is a simple method for oscillation. The simplest type of amplifier is a simple digital inverter (See Figure 1.7). This circuit sort of employs negative feedback with five stages of inverter. At the oscillation frequency of the ring

Figure 1.7: Ring oscillator using: 1) five digital inverters, 2) fully differential amplifiers.

structure, each inverter provides some phase delays and amplifier gains. The topology guarantees a loop gain that is greater than unity when the phase shift around the loop becomes greater than 180° . With that, the circuit is unstable to cause the oscillation. For example, if there are n inverters in the loop, with delay of τ_{inv} for a single inverter, the oscillation frequency can be defined as:

$$f_{osc} = \frac{1}{2n\tau_{inv}} \quad (1.6)$$

In most on-chip ring oscillators of integration circuits, some fully differential amplifiers are applied to suppress the coupling noise from power supply voltage. The oscillator of Figure 1.7 is also one with an even number of differential amplifiers. In the even order loop, the inversion can be achieved by simply switching the output terminals of the last amplifier connections. For example, the positive output is connected to the negative input node in the last stage. The delay of each cell is proportional to the oscillation frequency, whereby:

$$\tau_{amp} \propto \frac{C_L}{g_m} \quad (1.7)$$

Hence C_L is the load capacitance of the amplifier and g_m is the transconductance of the drive transistor in it.

However, the frequency of CMOS ring oscillator varies a lot with different process, supply voltage and temperature (PVT). The temperature effects on semiconductors are provided in Appendix A.

1.3 Objective

With the understanding of clock generators, this research aims to develop a novel fully on-chip clock generators for electronic system in smart building application. First of all, the target clock source must have excellent frequency stability with temperature variation due to exposure to different environment for the buildings in the different parts of world. The design will replace the off-chip crystal oscillator to save more energy consumption, and to enable fully integration of the entire electronic system. Furthermore, the power consumption within the clock generator is to be of a minimum. The battery will somehow always be the bottleneck of the aging devices, especially for some wireless sensor nodes that are implemented on the building surface.

1.4 Dissertation Overview

This report consists of six chapters and they are organized as follows:

Chapter 1 provides relevant background and motivation of the clock generators for smart building applications.

Chapter 2 reviews several past literatures with regard to the two different modes of clock generators: the on-chip oscillator and phase-locked loop

design.

Chapter 3 presents a 13.5-MHz low-power, RC on-chip relaxation oscillator with split-capacitor technique. It implements only one comparator and one reference voltage to minimize power consumption and silicon area. A loop delay variation cancellation technique that employs an integrator loop and a split-capacitor architecture helps attained the temperature stability in the proposed oscillator.

In Chapter 4, a design of a 12.77-MHz on-chip RC relaxation oscillator with digital calibration technique is presented. To maintain the frequency stability versus temperature and supply voltage variations, loop delay tuning by a digital feedback loop is developed in this system. It also generates an on-chip reference pulse for digital calibration.

Chapter 5 introduces an 1-GHz all-digital PLL design for processors and micro-controllers applications. To avoid power hungry TDC based structure, only one D flip-flop is implemented as a phase detector. In order to improve the phase noise performance of this PLL, injection locked is introduced in this design.

Finally, Chapter 6 concludes the researches conducted and provides discussion for some future work.

1.5 Findings and Outcomes

This research has led to several novel outcomes:

1. A novel 13.5-MHz low-power, RC on-chip relaxation oscillator with split-capacitor technique in Chapter 3, with frequency variation only $\pm 0.5\%$ versus temperature range of -30°C to 120°C .

2. Another on-chip RC relaxation oscillator in Chapter 4. A proposed digital compensation technique is implemented in the circuits which can achieve 31 ppm/°C variation with temperature variation range of -30 to 120°C.
3. A all digital PLL with injection-locked scheme in Chapter 5, consuming only 1.2 μ W.

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Chapter 2

Literature review

This chapter reviews some key techniques focused on fully on-chip relaxation oscillators and phase locked loops design. Upon describing the conventional structure, the drawbacks and error sources will be discussed. Several State-of-art designs will be also presented.

2.1 Relaxation Oscillator

Digital electronic systems generally require a clock signal that periodically switches from zero to one. Therefore, an oscillator that generates a square wave directly is preferred, and a relaxation oscillator is a better choice amongst the clock generators.

A relaxation oscillator operates by alternatively charging and discharging the energy stored in a capacitor or inductor by using a nonlinear device such as a transistor, causing abrupt changes in the output waveform. A relaxation oscillator often produces a non-sinusoidal periodical output signal, such as a square wave or a triangular wave [1]. Relaxation oscillators are widely used for the easy of design than linear oscillators, and that they are easier

to fabricate on integrated circuit since they do not require inductors like the LC oscillators, and can be tuned across a wide range of frequency [2]. In the following section, the relaxation oscillator circuits will be presented in details.

2.1.1 Conventional On-Chip Relaxation Oscillator

Figure 2.1: (a) Conventional on-chip RC relaxation oscillator, (b) Operating waveforms for the conventional oscillator.

Figure 2.1 illustrates the architecture and timing diagram of a conventional relaxation oscillator. The oscillator consists of a bias current circuit, a RC timing circuit, a comparator block, and a SR latch. The operation of the oscillator can be described as follows [3]. A constant reference voltage

V_{ref} is generated by a reference current I_B through a resistor R . Assuming $\phi1$ is high and $\phi2$ is low initially, the voltage of capacitor C_1 is charged up while V_2 is connected to ground by a closed switch. The two comparators are then triggered when V_1 or V_2 reaches $V_{ref} = I_B \times R$. Ideally, the oscillation frequency should only depends on the capacitance and resistance values. When the two capacitors are of the same value C , the half period of conventional oscillator t can be expressed as:

$$\frac{I_B \cdot t}{C} = I_B \cdot R \quad (2.1)$$

Therefore, the oscillation period is twice of it:

$$T_{osc} = 2 \times RC \quad (2.2)$$

Equation (2.2) shows that the oscillation frequency is independent of bias current source ideally. It is only set by the time constant, the production value of the resistor and the capacitor (RC). Therefore, if the comparator and other logics are ideal, only a temperature stable resistor and capacitor are required for a stable oscillation period. In general modern CMOS process technologies, the temperature coefficient of the metal-insulator-metal (MIM) capacitor is very small (on the order of 20ppm/°C) [4] and is thus neglected in many works. For the resistors implemented in this kind of design, it is usually used different kinds of resistors with opposite temperature coefficient for the temperature compensation. For example, in standard CMOS process, the P-type polysilicon resistor has a negative temperature coefficient, and the N-type resistor has a positive temperature coefficient. Many designs combined the two different types of resistor together to get a stable resistance, as published in [5, 6, 7]. By the way, there are also some

papers which use special process technique to get a stable resistor with high temperature coefficient [8, 9]. However, in order to save more cost and process, the designs discussed in this article are only based on the standard CMOS process. It means that we focus on the circuits design techniques to stabilize the oscillation frequency, rather than by process compensation.

In reality, the circuits cannot trigger immediately when the ramp voltages on the capacitors cross V_{ref} . The loop delay t_d of the comparators and logics can directly affect the oscillation frequency. After considering the loop delay t_d , the oscillation period can be shown as:

$$T_{osc} = 2(RC + t_d) \quad (2.3)$$

Moreover, the loop delay varies significantly with temperature and power supply voltage. In order to have a stable frequency, some methods to minimize variations in the loop delay must be explored.

Another important error source is from the offset voltage of comparators. The comparator offset voltage is also temperature and supply voltage dependent. After considering the comparator offset voltage V_{os} , the half oscillation period T_{half_osc} can be expressed as:

$$T_{half_osc} = RC - \frac{C \cdot V_{os}}{I_B} \quad (2.4)$$

Generally, in kilohertz range, the comparator offset (V_{os}) is typically the main challenge and can be reduced using chopper techniques to cancel the offset voltage as reported in [6] and [10]. Moreover, in [9] and [11], a switching-point insensitive oscillator architecture managed to diminish the V_{os} impact. For a relatively high frequency output (over 10 MHz), the temperature-dependency of the loop delay and comparator delay (t_{comp}) typ-

ically are the main bottleneck.

2.1.2 Chopper for Offset Cancellation

As shown in equation (2.4), one important error source of frequency stability is the comparator offset voltage, which is especially crucial in the kilohertz frequency range. One effective method to cancel the offset voltage is chopper technique. Figure 2.2 shows the chopper structure with only one comparator compared to the conventional circuit [6]. Similar with the

Figure 2.2: Architecture of the relaxation oscillator with offset compensation.

conventional approach, a constant biasing current I goes through a resistor R to generate a reference voltage $I \cdot R$. During the first half period (i.e.: $\phi = 0$ and $\bar{\phi} = 1$), this reference voltage is connected to node V_2 . At the same time, the same current I also charges the capacitor on the left side (C_1). The charging signal transfers to node V_1 . When the voltage V_1 crosses V_2 , the comparator will be triggered after a small delay time (t_d) due to the delay of the comparator and the following buffers. The comparator toggles the signal ϕ to 1, which in turns charges capacitor C_2 and resets the voltage across C_1 . In addition, due to chopping technique, the connections for the two comparator inputs are reversed, with V_1 being the reference voltage

Figure 2.3: Operating waveforms for the chopper offset cancellation circuit.

and V_2 the charging voltage across capacitor C_2 . The period of oscillation can be expressed as $2RC + 2t_d$ nominally. The switching scheme also can cancel offset voltage of the comparator. The operation waveform is shown in Figure 2.3. The operation can be expressed as follows. If there is an offset voltage V_{os} in the comparator, the reference voltage for comparison changes to $I \cdot R \pm V_{os}$. Therefore, the charging duration of phase $\phi = 0$ increases by CV_{os}/I , however the opposite phase $\phi = 1$ decreases by the same amount, thus the total period of oscillation is constant. What's more, the chopper cancellation technique also reduces much power consumption of the relaxation oscillator. First of all, it is only required one comparator in the oscillation loop. Second, the oscillation wave can be set as a lower swing signal, because there is no need to enlarge output swing to compensate the offset variation effect. Finally, compared to conventional oscillator design, the design specifications of comparator can be relaxed. The designers need

not to allocate more power to optimize the comparator offset parameter.

However, although this offset cancellation technique can handle the offset error efficiently, for higher frequency relaxation oscillators (megahertz), the loop delay (comparator delay and other circuits delay) is the dominant source of frequency variations. In the next section, we will introduce other techniques to average the loop delay.

2.1.3 Voltage Averaging Feedback Circuits

The voltage averaging feedback (VAF) technique in Figure 2.4(a) is a viable method to achieve a stable and accurate period by averaging the loop delay t_d [5]. In this circuits, the relaxation oscillator can be considered as a voltage-controlled oscillator which is controlled by a voltage signal V_c . Two waveforms of oscillator V_{OSC1} and V_{OSC2} are connected to V_{OSC} and transfer to the analog integrator. The oscillation voltage can be expressed as:

$$V_{OSC1,2}(t) = VDD \cdot (1 - e^{(-1/RC)t}) \quad (2.5)$$

And from the VAF integration loop:

$$\frac{1}{T} \int_0^T V_{OSC1,2}(t) dt = V_{ref} \quad (2.6)$$

Using equations (2.5) and (2.6), we obtain the following simplified equation:

$$\frac{(1 - \alpha)T}{RC} = 1 - e^{-T/RC} \quad (2.7)$$

where α is the ratio of reference voltage (V_{ref}) and the power supply, $\alpha = V_{ref}/VDD$. From equation (2.7), the oscillation period is simply a time constant RC and the voltage ratio α . The circuits operation waveform

Figure 2.4: (a) The voltage averaging feedback concept presented in [5], (b) waveform of the oscillation.

is shown in Figure 2.4(b). The variation of delay t_d has little effect on the frequency because the VAF technique can automatically adjust V_c to

maintain the stable desired frequency. For example, when t_d is shorter, the integrator feedback loop will increase V_c to maintain the same frequency.

The VAF technique minimizes dependencies of power supply voltage, surrounding temperature and the oscillator loop delay. On the other hand, it can also improve the low offset frequency phase noise. However, it requires an analog amplifier integrator to create the voltage (V_c) for comparison. And in the whole circuits, it is needed two comparators for operation totally. For the long term operation, it will consume a lot of power.

Besides relaxation oscillators, many SoCs with digital signal processing or CPUs always need a high frequency clock signal to synchronise digital data. The clock signals for processors are generally around several hundred megahertz or gigahertz. That is the reason why we are looking for another circuits which can generate such high frequency on-chip.

2.2 All Digital Phase-Locked Loops

The concept of phase locking was invented in the 1930s and widely used in electronics and communication techniques. A phase-locked loop (PLL) is a key building block in modern integrated circuits. It can generate output signals with a N times frequency compared to the reference signal like a frequency multiplication, so as to provide clock for digital systems or a carrier in the radio frequency front-end for wireless applications.

2.2.1 Conventional Type-II PLL

A type-II or charge pump phase-locked loop is illustrated in Figure 2.5 [12]. The reference clock (CLKIN) injects into a phase-frequency detector (PFD) block which can distinguish frequency and phase difference from one

to the other. The feedback clock came from voltage controlled oscillator (VCO) and divider also goes into the PFD. Such the PFD implementation senses the transitions at the input reference and divider output, detects phase or frequency differences, and activates the charge pump accordingly. A charge pump (CP) can converter the results of PFD, usually some pulse sequences, into a voltage variation. A low-pass filter (LPF) following CP, cannot only smooth down the ripples of output voltage with very large capacitors, but also is more important for loop stability issues. The LPF comprises of a pole and a zero (the serial RC node) to stabilize the feedback system. Generally, the single capacitor in Figure 2.5 is about one-fifth or one-tenth of the one in series with the resistor. A VCO is the most important block in a PLL, which is implemented as a clock frequency source. And the performance of VCO determines the performance of PLL system, such as working frequency, tuning range, phase noise, etc. Additionally, a divider following the VCO is generates an accurate divide by N clock frequency compared to input reference.

Figure 2.5: Basic architecture of a charge pump PLL.

2.2.2 All Digital PLL Architecture

Referring to the brief introduction of Phase-Locked Loops (PLLs) in section 2.2.1, the PLL on a chip is usually used for clock alignment and

multiplication. However, the conventional charge-pump PLL implementation has several drawbacks in many mixed-signal and digital applications. One is that the analog building blocks in traditional PLLs on a most digital chip pose design and design simulation challenges. Although many design tools have the function of mixed-signal verification, the simulation accuracy and total locking time are still big problems. Another reason is that the analog PLL always occupies a larger area, especially the large capacitor in the loop filter. Hence, it is desirable to research for a better PLL to provide excellent performance with a lower cost and lower power consumption. The comparison table of traditional analog PLL and all-digital PLL (ADPLL) is shown in table 2.1.

Figure 2.6: From analog to all digital PLL.

Table 2.1: The comparison of analog PLL and all digital PLL

Category	Phase detector	Loop filter	Oscillator	Area size
Analog PLL	Analog/Digital	Analog	VCO	Large
All Digital PLL	Digital	Digital	DCO	Small

Figure 2.6 shows the changes from a conventional analog PLL to an all-digital PLL (ADPLL) [13]. In this digital circuits based architecture, a

Time-to-Digital converter (TDC) replaces the phase and frequency detector (PFD); a digital loop filter is implemented instead of analog loop filter; and the voltage-controlled oscillator (VCO) in traditional design is replaced by a digitally-controlled oscillator (DCO) circuit. The main advantage of ADPLL is that the digital loop filter is area efficient and very insensitive to leakage of transistors. However, these changes also bring some new challenges, such as high performance TDC and DCO design.

I Time-to-Digital Converter

Time-to-Digital Converter (TDC) is a digital converter to quantize the time interval between a start and a stop signal with the resolution of some pico-seconds. The TDC resolution is equivalent to that of a digital counter and synchroniser clocked at a very high frequency. Recently, the typical resolution of TDC is equivalent to that obtained with a clock frequency of 8 GHz or higher [14]. A classical TDC circuit design is shown in Figure 2.7. In this architecture, phase error between *Input* and *Ref* is measured with delay line and many register taps. The resolution is limited to buffer delay and is sensitive to process and environmental variations. On the other hand, this type of TDC occupies small implementation area and is easy to shrink down with the technology development. When the TDC is implemented in an all digital PLL to replace the phase detector of traditional PLL system, the phase error is converted to time error by a scaling factor of $T/2\pi$. Generally, it is important to understand that from the overall ADPLL performance, the TDC will dominate a ADPLL phase noise at low frequency offset, but the digitally-controlled oscillator dominates phase noise at high frequency offset [15]. Therefore, a high-speed and high-resolution TDC is required to achieve better phase noise in some applications.

Figure 2.7: Cycle interpolation time-to-digital converter (TDC).

As shown in Figure 2.7, although the delay line based TDC operates at the highest convention rate, its minimum time resolution is determined by the minimum propagation gate-delay in CMOS process. A Vernier structure can be adopted in [16] to achieve higher time resolution, as shown in Figure 2.8(a). The minimum time resolution (τ) in a Vernier TDC is decided by the delay difference between two types of delay cells. It can be expressed as: $\tau = \tau_s - \tau_f$, where τ_s and τ_f are the propagation time of a slow and fast delay cell, respectively. Therefore, a Vernier delay line TDC (VDL) can achieve a time resolution value less than minimum CMOS gate delay. However, since it doubles the number of delay cells, the complexity and power consumption are much more. Here is an example. Assuming that the minimum delay cell is around 20 ps in the CMOS process, and the measured timing slot is from 0 to 400 ps, a conventional delay-line TDC needs 400 ps (20 ps $\times$ 20 delay cells) to convert the entire range. In a VDL, if the two different invertor delay is set as $\tau_s = 50$ ps and $\tau_f = 40$ ps, a finer time resolution of 10 ps can be achieved. But it requires 2 ns (50 ps $\times$ 40 delay cells) to quantize the identical time value. Moreover, its conversion rate also becomes lower. In recent years, a lot of multiple types of VDL, i.e., 2D-VDL [17], 3D-VDL [18], Vernier-ring [19], Vernier-GRO [20], and Cyclic-Vernier delay-lines [21] are

reported. The details of these types of VDL are not discussed in this thesis. Overall, the trade-off between operation speed and digital bits resolution of VDLs is shown in Figure 2.8(b). Besides these, there are some publishing about second generation TDCs with time-amplifiers, such as two-step [22], cyclic [23], and pipeline TDCs [24], which will not give further discussion in the article.

Figure 2.8: (a) Architecture of a Vernier delay-line TDC, (b) speed and resolution comparison among TDCs.

II Digitally-Controlled Oscillator

Unlike the traditional oscillators and relaxation oscillators mentioned above, a digitally-controlled oscillator (DCO) is a hybrid oscillator which consists of a VCO and digital bits controller. In the ADPLLs system, DCOs are a replacement for the conventional VCOs. They are more flexible and robust as tuned by many digital controlling bits to adapt environment variations. Compared to traditional voltage-controlled oscillators, the control signal of DCO is not an analog voltage, but digital bits. These digital control bits tune currents of every delay cell in a oscillator loop step by step. The typical structure of a DCO design is shown in Figure 2.9 [25]. The

frequency of the whole DCO can be calculated from:

$$f_{DCO} = 1/(T_{ini} - D \cdot T_{step}) \quad (2.8)$$

where f_{DCO} is the DCO frequency to be achieved, T_{ini} is the delay time of the loop initially, D is the digital control bits from D_0 to D_n , and T_{step} respects every step delay time changed by control bits varying one bit.

Figure 2.9: Standard delay cell of digitally-controlled oscillator with driving strength control.

2.2.3 ADPLL without TDC

A Time-to-digital converter (TDC) is used to convert different time information into some digital bits information for processing in conventional ADPLLs. However, a TDC typically is power hungry and is always required complex structure to endure sensitivity to CMOS process, supply voltage and environment temperature variations. In recent years, many ADPLL designs try to avoid a power hungry TDC structure to achieve a much smaller power consumption and silicon area.

A good replacement of TDC for low-power and small area ADPLL ap-

plications is using a bang-bang phase and frequency detector (BBPFD) to compare the phase different between reference clock and feedback signal. In [26], a bang-bang all-digital fractional-N PLL is presented, as shown in Figure 2.10. The DCO is tuned by an automatic frequency controller (AFC) for fast locking scheme. Generally, the noise in power supply is the major contribution of the overall PLL total noise. Thus, a supply-noise cancelling architecture is employed in the oscillator block to reduce the power supply noise. The phase selection in this ADPLL is controlled by a walking-one phase selector. The phase selector is constructed by a closed chain of 32 unit cells, which mainly act as DFFs and propagate the selection signal of a 32:1 MUX. During the phase comparison, the FEED signal will try to move to the nearest phase step by step due to the frequency multiplication ratios. Furthermore, in this design, clock gating technique is deployed in the DFF chain to reduce the power consumption.

Figure 2.10: A block diagram of a bang-bang ADPLL.

2.3 Conclusions

In this chapter, recent publication of on-chip relaxation oscillators and ADPLLs are discussed. After brief introduction of the conventional relaxation oscillator, comparator offset cancellation and voltage averaging feed-

back techniques are reviewed in details.

Besides, the architecture of ADPLL is presented with some techniques of high speed and high resolution TDCs. Also, an ADPLL structure without power hungry TDC is described.

In the next chapters, a number of proposed designs will be introduced.

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Chapter 3

A Relaxation Oscillator with Split-Cap Technique

This chapter presents a 13.5-MHz low-power, RC on-chip relaxation oscillator with split-capacitor technique. It implements only one comparator and one reference voltage to minimize power consumption and silicon area. A loop delay variation cancellation technique that employs an integrator loop and a split-capacitor architecture helps attained temperature stability in the proposed oscillator.

3.1 Introduction and Motivations

3.1.1 Radio Frequency Identification

Radio-frequency identification (RFID) uses electromagnetic fields and electrical systems to automatically identify and track tags attached to objects. The RFID tags can communicate with the reader and restore data in their own memories. In recent years, a lot of applications are based on RFID technology in the daily life, i.e., security access, item level inventory

tracking, race timing in sport, etc. There are many standards and protocols for RFID specification, such as the International Organization for Standardization (ISO), the International Electrotechnical Commission (IEC) and so on. The ISO/IEC 18000-3 is an international standard for RFID item level identification, which describes the parameters for interface communications at high frequency (HF) 13.56 MHz [1].

Figure 3.1: Block diagram of an analog frontend for RFID reader.

In many smart buildings, the RFID readers and tags are used for security access or for the car parking systems. Figure 3.1 shows the block diagram of an analog front-end integrated circuit for 13.56 MHz RFID reader [2]. The oscillator in Figure 3.1 is a critical block in the system. It is driven by a 13.56 MHz external crystal to generate the RF frequency. The external quartz crystal is connected to the load capacitors. In order to save cost and power consumption of the RFID system, our research target is to build

an on-chip relaxation oscillator to replace the external quartz crystal as a clock source. It is required that the on-chip oscillator has a stable frequency performance versus temperature and supply voltage variations.

3.1.2 Organization

This chapter is organized as follows: Section 3.2 describes the proposed relaxation oscillator with split-capacitor technique, which includes the architecture, the operation principle of split-capacitor, the comparator offset cancellation technique, control logic structure and noise reduction due to integrator. Section 3.3 shows the measurements results of the design. Finally Section 3.4 concludes this chapter.

3.2 Proposed Relaxation Oscillator with Split-Capacitor Technique

3.2.1 The Architecture of Proposed Oscillator

To overcome the concerns mentioned in Chapter II, we proposed a novel RC relaxation oscillator that uses a integration loop with a split-capacitor technique for frequency stability, as shown in Figure 3.2. It is constructed by three parts – (1) A main oscillator is used to generate a clock signal. The four switches near the comparator operate as a chopper structure to cancel the offset of the comparator as in [3]. Moreover, the oscillation capacitors are separated into two small ones (C_{11} , C_{12} , C_{21} and C_{22}) in this proposed design. (2) A integrator loop with reference voltage divided by the power supply, provides a voltage to the comparator. (3) The split-cap control logic consists some logics to generate six timing control signals with differ-

Figure 3.2: The proposed relaxation oscillator with split-capacitor technique.

ent phases, which will be described in detail following. In this design, the resistors are combined by Poly and N-well two types, in order to minimize the resistance variation with temperature. The oscillation period T can be expressed as:

$$VDD \cdot (1 - e^{-t/RC}) = \alpha \cdot VDD \quad (3.1)$$

$$T = 2RC \cdot \ln(1 - \alpha)^{-1} \quad (3.2)$$

where α is the ratio between the reference and supply voltage ($\alpha = V_{ref}/VDD$), C is the sum of capacitance in each side ($C = C_{11} + C_{12} = C_{21} + C_{22}$) and t is the charging period of the comparator just before reaching V_{ref} , i.e. half oscillation period.

The advantages of our proposed oscillator can be summarized as follows. First, there is only one comparator in the circuit, hence there is minimum power consumption and active silicon area. Second, a feedback loop with

an integrator and two pairs of split-capacitor are used for loop delay cancellation. Furthermore, due to the close loop feedback structure, the noise of the oscillator can be compressed. Compared to [4], the circuit does not require additional reference voltages at the integrator feedback loop. Third, the two resistors replace the current sources that are needed for charging the capacitors in the conventional architecture. Current sources can in fact lead to reliability issues over a prolonged period of time. Finally, at the input of the comparator, a chopper technique is used to cancel the offset variation, which is controlled by a pair of non-overlap clocks, ϕ_1 and ϕ_2 . The working principle of split-capacitor technique will be described in details in the next section.

3.2.2 Relaxation Oscillator with Split-Capacitor Technique

According to equation (2.3), the delay variation t_d results in frequency fluctuation with voltage and temperature. In the proposed design, both the split-capacitor structure and the integrator feedback loop are used to realize oscillation that is independent of delay.

The split-capacitor technique (see Figure 3.2) includes the capacitors (C_{11} to C_{22}), an integrator and some control logics. The circuit operation with waveforms are detailed in Figure 3.3. Assume that ϕ_1 is high and ϕ_2 is low initially as in Figure 3.3(a). Capacitance C_{21} is charged by a resistor limiting current. The voltage at node V_2 is an exponential curve followed by RC_{21} constant value. V_2 is connected to the positive terminal of the comparator (V_{cp}). During this phase, the voltage at node V_1 is maintained at a stable value due to ϕ_{1r} still low at the beginning, and it is connected

quarter of the period. This will connect an additional parallel capacitor C_{22} to V_2 node. The parallel capacitor creates a drop in voltage V_2 . Then, V_2 is charged again to produce the $R(C_{21} + C_{22})$ value. The time between this voltage drop and the second charging peak will in turn compensate the loop delay of the entire signal path. When the oscillator is operating, the delay of the circuit will change if the temperature varies. The integrator loop will track this change to tune V_c , which is in fact the reference voltage (i.e: V_{cp} or V_{cn}) of the comparator. The output period is also adjusted by the different V_c . When the second charging peak reaches comparison value V_c , ϕ_1 will go low and ϕ_2 will be high. The operating circuits and waveform of ϕ_2 is shown in Figure 3.3(b).

3.2.3 Comparator Offset Cancellation

As mentioned above, only one comparator is implemented in this design. The comparator offset cancellation schema is same as [3]. When phase $\phi_1 = 1$, C_{21} is charged to generate the voltage V_2 that is to be fed to the positive input terminal of the comparator. At the same time, the negative node of the comparator is connected to the output of the integrator for the adjustment of reference voltage V_c . When the duration for comparison ends, the comparator and logic circuits will change the state of the output, i.e: ϕ_1 and ϕ_2 . When ϕ_2 changes to 1, these switches are reversed, with V_c connecting to the negative input node and the voltage of capacitor V_2 fed to the positive input terminal. As the integrator output and capacitors voltage are connected to the input terminal of the comparator alternately, the comparator offset can be cancelled by this switching chopper scheme.

3.2.4 Split-Cap Control Logic

Because of the split-cap technique, the comparator is needed to trigger twice at one half of the oscillation period: first time for the total capacitor ($C_{11} + C_{12}$), and the second time for the single capacitor after separated. The first one is just used for beginning of capacitors splitting, and the second is for the oscillation finally. Therefore, there are some logics needed to control them. Figure 3.4 shows the control logic of split-cap technique in the proposed circuits design. In this figure, the signal In comes from the output of comparator and Schmitt trigger. V_i is after two absorbed capacitors from In , and also as an input of two non-overlapping clocks generation. The two non-overlapping clocks (ϕ_1 and ϕ_2) control the reset signals of two D flip-flops. The two D flip-flops inputs are connected to constant high at all the time. After these two D flip-flops, there are two reset signals, and two sample signals at the two NOR outputs.

Figure 3.4: The control logic of split-cap technique.

The operation waveforms of the control logic are shown in Figure 3.5.

Figure 3.5: The operation waveform of the control logics for split-cap.

There are several pulses in the In signal due to capacitor splitting. In this design, two capacitors (C_1 and C_2 in Figure 3.4) are added to remove these pulses. The input signal In goes through some buffers and absorbed caps to generate signal V_i . After these absorbed caps, the first pulse (t_1 to t_2) will be cancelled. The operation of the logic can be expressed as follows. When the comparator triggers at time t_1 , it generates a rising edge at the first time. The D flip-flop (Q_1) is also triggered to sample the high level voltage. Its output (ϕ_{1r}) goes high. Due to the split-cap technique, the voltage for comparison will be dropped after a short time. Therefore, the output signal drops to low at time t_2 . Because of the edge trigger characteristic of the flip-flop, ϕ_{1r} remains constant high voltage until ϕ_2 goes high to reset the flip-flop at time t_3 . A NOR operation between ϕ_2 and ϕ_{1r} produces the sample signal ϕ_{1s} . This is similar for the other two control logic ϕ_{1r} and ϕ_{1s} .

3.2.5 Noise Reduction

The noise performance is an important parameter of the low-power relaxation oscillators. Under low frequency operation, the concern for flicker noise is even pronounced. One effective way to reduce the noise is the anti-jitter noise reduction method [5], but is needed an extra current source for compensation. Other published approaches to reduce the phase noise of the oscillators [6, 7] are mainly based on the balancing of impulse sensitivity function [8], but are with limited to at most 3dB.

It is a good idea to remove the current sources in the oscillator through their flicker noise reduction approaches. After removing the noise in the current sources, the key remaining flicker noises are from the comparators. Hence, enlarging the size of transistor is effective to reduce the flicker noise. However, when the size of transistor increases, the parasitic capacitances also increases. These parasitic capacitances are sensitive to voltage and temperature variations. Thus, to decrease the parasitic capacitances ratio, the common traditional solution for frequency stability was to increase the capacitor C as well as oscillation time constant, which also costs lots of power.

The proposed split-cap technique with the integrator loop can overcome this tradeoff due to closed-loop feedback. An entire noise model of the relaxation oscillator as [9] can be created when the analog amplifier based integrator is replaced by the switch capacitors structure. The noise model is shown in Figure 3.3.

The circuits in Figure 3.2 can be represented as a Voltage-Controlled Oscillator (VCO) with a control voltage V_c . The frequency gain can be expressed as K_{VCO} , and ϕ_{osc} is the output of it. After feedback, the control

Figure 3.6: The noise transfer models of the relaxation oscillator.

voltage is the V_{osc} . ϕ_n is the phase noise of oscillator. The noise introduced by the comparator is V_N . A coefficient β is the feedback factor of this closed loop. The ϕ_{out} is the total output phase noise of this circuits. The benefit of integrator is that the low offset frequency part of phase noise of the VCO is suppressed by negative feedback effect. It means that the comparator can be constructed by small transistors with low power.

Here, there are two main noise sources in this circuit: 1) noise generated from the comparator (V_N), 2) phase noise from the oscillator part (ϕ_n). We will consider them one by one.

Because of the switch capacitor in the closed loop, we implement the Z domain analysis. When Z domain variable are replaced by e^{sT} , an equation of oscillator noise can be shown as:

$$\phi_{out} = \frac{K_{VCO}(e^{sT} - 1)}{s(e^{sT} - 1) + s^2\beta C_1/C_s} V_N \quad (3.3)$$

where the V_N expresses the integrator noise in the loop.

Considering two different limits: s approaches zero and infinity. When s approaches zero, there is an approximation:

$$e^{sT} - 1 \approx sT \quad (3.4)$$

After this approximation, equation (3.3) can be rewritten as:

$$\phi_{out} = \frac{K_{VCO}T}{s(T + \beta C_1/C_s)} V_N \quad (3.5)$$

It is a low-pass filter performance.

When s approaches infinity, the portion e^{sT} is much greater than s^2 . The equation (3.3) can be rewritten as:

$$\phi_{out} = \frac{K_{VCO}}{s} V_N \quad (3.6)$$

which is also a low-pass transfer function. From equations (3.5) and (3.6), the high frequency noise of V_N can be expressed by the large loop gain.

After introduced the phase noise of oscillator ϕ_n , the transfer function is:

$$\phi_{out} = \frac{e^{sT} - 1}{(e^{sT} - 1) + K_{VCO}\beta C_1/C_s} \phi_n \quad (3.7)$$

It is a high pass characteristic. It means that the loop can reduce the low offset frequency part of oscillator phase noise performance.

The phase noise simulation (PSS + Pnoise simulation in Spectre) is shown in Figure 3.7 with and without the integrator. It is important to note that this simulation is just the oscillator intrinsic noise reduction as shown in the equation (3.7). For the total output noise, the noise of the oscillator can be filtered by the closed feedback loop as in equation (3.3). The

low offset frequency noise is depended by the comparator noise performance.

Figure 3.7: The oscillator phase noise simulation results with and without integrator.

3.3 Measurement Results

Figure 3.8: Die photograph of the proposed relaxation oscillator with split-capacitor.

Figure 3.8 shows the chip micrograph of the proposed relaxation oscillator with split-capacitor technique. It is fabricated in 0.18- μm GLOBAL-

Figure 3.9: Measured oscillation frequency of three chips versus temperature at 1.8-V power supply.

FOUNDRIES CMOS process, which occupies a chip area of $180 \mu\text{m} \times 180 \mu\text{m}$. This design consumes $48.8 \mu\text{W}$ at 1.8-V power supply and room temperature 27°C .

The chips are measured by TEMPTRONIC's Thermal Stream 4310 for temperature variation. At the room temperature and normal power supply 1.8 V, the output frequency is set at 13.5 MHz for RFID application. Figure 3.9 illustrates the frequency of proposed oscillator variation versus temperature of three different chips. With temperature range of -30°C to 120°C , in the worst case, the output frequency varies from 13.484 MHz to 13.595 MHz, and the frequency variation is less than $\pm 0.5\%$. In Figure 3.10 the oscillation frequency versus supply voltage is illustrated. In this measurement, the power supply voltage is changed from 1.5 V to 2.1 V. Here, the oscillation frequencies of three chips are from 13.53 MHz to 13.62 MHz after the closed loop integrator compensation, which is about $\pm 0.5\%/V$.

The Figure 3.11 shows the phase noise performance with the integration loop. Compared this figure with the simulation one (Figure 3.7), the low

Figure 3.10: Measured oscillation frequency of three chips versus supply voltage at room temperature.

Figure 3.11: Measured oscillation phase noise performance.

offset frequency is suppressed. This is because that the closed feedback loop characteristics. The noise of comparator is low pass performance. On the contrary, the total noise from oscillator noise portion is a high pass response. In the measurement results, the phase noise is -55 dBc/Hz at 10 kHz offset, and it can reach -102 dBc/Hz at 1 MHz offset frequency.

The Figure of merit (FoM) is normally used for oscillation performance measurement with different oscillation frequencies and different processes. The commonly used FoM is frequency to power ratio [10].

$$FoM_1 = 10\log(f/P) \quad (3.8)$$

However, for the FoM in equation (3.8), there is no parameters of temperature coefficient and the process information. Therefore, another FoM can be introduced:

$$FoM_2 = 10\log\frac{f \cdot \Delta T}{P \cdot TC} \quad (3.9)$$

where the ΔT is the temperature range, and TC is the temperature coefficient. From these two equations 3.8 and 3.9, the larger FoM values means that oscillators have larger output frequency, smaller power consumption, larger temperature range and smaller temperature coefficient.

The performance of the proposed on-chip relaxation oscillator compared to other the state-of-the-arts are tabulated in Table 3.1. Compared to circuits with similar frequency design [4], our work achieves lower power consumption and better temperature performance versus temperature variation. Furthermore, our active area is also quite small as compared to other designs designed based on the same CMOS process technology. When compared to other designs with advanced technology process, the proposed design achieves comparable silicon area to reference [3, 4, and 6]. Referring to Table 3.1, when compared to designs of [4] and [11] where both offer mega-Hertz oscillation frequency output signal, this work has the smallest temperature coefficient. For the better temperature coefficient designs in [3, 6], the output frequency is lower. For the design reported in [13], its active area and temperature coefficient are both better than the proposed work. However,

its power consumption is much larger. Overall, this work has the best overall performance which has also been proven in the two FoM values.

Table 3.1: Relaxation oscillator with split-cap performances summary

Reference	[3]	[4]	[6]	[11]	[12]	[13]	This Work
Process (nm)	65	65	130	180	130	180	180
Active Area (mm ²)	0.032	0.01	0.07	0.04	0.007	0.22	0.032
Frequency (MHz)	0.0185	12	3.2	14	1	10	13.5
Temperature (°C)	-40 – 90	0 – 80	20 – 60	-40 – 125	25 – 200	-20 – 100	-30 – 120
Temperature Coefficient	±0.25%	±0.82%	±0.25%	±0.75%	±0.9%	±0.4%	±0.5%
Supply (V)	1.2	1.1 – 1.5	1.4 – 1.6	1.7 – 1.9	2.5	1.2	1.5 – 2.1
Freq. with VDD (%/V)	1	±0.175	±0.4	±0.8	1.09	±0.05	±0.5
Power (μW)	0.12	98.4	38.2	45	428	80	48.8
FoM_1^*	112	111	109	115	94	111	114
FoM_2^{**}	159	151	151	158	137	156	159

* $FoM_1 = 10\log(f/P)$

** $FoM_2 = 10\log\frac{f \cdot \Delta T}{P \cdot TC}$

3.4 Conclusions

This chapter presents a novel on-chip RC relaxation oscillator with split-capacitor integrator compensation loop technique to achieve a stable output frequency with environment temperature and supply voltage variations. For replacing off-chip quartz crystal, the on-chip relaxation oscillator can provide a stable frequency signal at 13.5 MHz for RFID application. The split-capacitor technique with analog integrator can reduce comparator number in the oscillation loop, and also can cancel the comparator offset voltage and average the loop delay errors. Measurements results show that the output frequency has ±0.5% and ±0.5%/V variation with temperature range of

-30°C to 120°C and power supply range of $1.5 - 2.1$ V. Moreover, the power consumption of the design yields only $48.8\ \mu\text{W}$. However, the proposed method also implements the analog circuits to maintain the frequency stability. In order to avoid the power hungry amplifier in the integrator loop, we will discuss another digitally compensation method in the following chapter.

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Chapter 4

A Relaxation Oscillator with Digital Compensation Method

The design of a 12.77-MHz on-chip RC relaxation oscillator with digital compensation technique is presented in this chapter. To maintain frequency stability versus temperature and supply voltage variations, a novel delay tuning technique via a digital feedback loop is developed in this system. The compensation circuits also generate an on-chip reference pulse for digital calibration.

4.1 Introduction and Motivations

4.1.1 Digital Circuits in CMOS

As the semiconductor industry advances, the minimum length of CMOS continues to shrink. TSMC shipped 14-nm silicon process in 2015, is moving onto the 7-nm process in the coming two years [1]. Technology scaling significantly lowers the cost of digital logic and memory, and there are great incentives to implement high-volume baseband signal processing using the

most advanced process technology available. With the development of the CMOS process, digital integration circuits will benefit more, such as higher processing speed, smaller area and lower power consumption. On the contrary, the analog circuits will face a lot of issues with the scaling of silicon devices, such as larger leakage current, smaller intrinsic gain, worse signal-to-noise ratio and more complex layout rules [2]. Table 4.1 provides a comparison between the analog and digital circuits in the trend of process shrinkage. Therefore, in modern technology, more and more publications will focus on digitally assisted analog circuits design, or digital calibration technique in conventional analog design.

Table 4.1: Performance comparison between analog and digital circuits.

	Analog Circuits	Digital Circuits
Singal Processed	Continous (Real Value)	Discrete (High or Low)
Noise Sensitivity	High	Low
Programmable	Complex	Simple
Performance with Scaling	Worse	Better

Numerous research publications on digitally assisted analog circuits are available. Most of them focused on the interface circuits between analog and digital circuits, such as the analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and so on. In previous chapter 3, a relaxation oscillator with stable frequency performance against temperature and supply voltage variations has presented. The design, however, still uses an analog technique to compensate the loop delay variation. According to Figure 3.2, an analog integrator loop that is inherent to in the circuits, engages a power hungry operational amplifier. It will be extremely complex if migra-

tion to advance process technology is required in the future. Hence, in this chapter, a 12.77-MHz relaxation oscillator with digital calibration method is explored. The digitally assisted method not only save power, but offers ease of implementation when process technology shrinks in the future.

4.1.2 Organization

This chapter is organized as follows: Section 4.2 presents the proposed relaxation oscillator with digital compensation technique, which includes the digital compensation method architecture, reference pulse generation, the time-to-digital converter design, CTAT current biasing and so on. Section 4.3 describes the digital calibration method in details. Some measurements results are shown in Section 4.4, which includes the chip die photo, measured phase noise, jitter performance, and frequency variation versus temperature and supply voltage. Section 4.5 concludes the chapter.

4.2 Proposed Relaxation Oscillator with Digital Compensation

4.2.1 The Architecture of Proposed Relaxation Oscillator

A digitally compensation method is proposed to minimize the loop delay variation in the oscillators discussed above. Figure 4.1 shows the architecture of the proposed relaxation oscillator with digital compensation technique.

This proposed design consists of five parts: (1) A main oscillator from [3] is used to generate a clock signal, and the four switches here operate as a chopper structure to cancel the offset of the comparator. For exam-

Figure 4.1: Architecture of the proposed relaxation oscillator with digital compensation feedback loop.

ple, assuming the oscillator has an offset V_{os} , the duration of phase $\phi = 0$ increases. However, the opposite phase $\phi = 1$ will decrease by the same value; thus the total period of oscillation remains constant. (2) The reference pulse generation circuit provides a digital calibration reference pulse. (3) The loop delay tuning block consists of several different delay lines that are controlled by some feedback bits. As shown in the equation (2.3), the loop delay will affect the oscillation frequency. In this work, the digital feedback loop will tune the loop delay to compensate the output frequency. If the output frequency is higher than the desired one, it will increase the loop delay to reduce frequency. (4) The digital compensation circuits consist of two time-to-digital converters (TDCs) and a digital calibration algorithm. The two TDCs are used to convert timing information from the oscillation period and reference pulse into digital bits. The digital calibration block then processes these bits to provide some feedback control bits to tune the delay cell. (5) The complementary to absolute temperature (CTAT) current bias generator provides all the bias current in the system. Due to the low supply voltage design (0.6 V to 1.1 V) in 0.18- μm CMOS process, all circuit-

Figure 4.2: Waveforms of the proposed relaxation oscillator.

s operate at near-threshold region. The propagation delays of the circuits becomes larger when temperature decreases. The CTAT current source is therefore selected to compensate such effect.

Figure 4.2 shows the operating waveform of the oscillator. The comparison reference voltage V_{ref1} is generated by a bias current I_B and a constant resistor R_1 . During the phase $\phi = 1$, a current charges capacitor C to generate a ramp signal V_{ramp} , which is to be used for reference pulse generation, and will be discussed in the next section. When node V_{C1} crosses node V_{C2} , ϕ changes to zero after some delay time which is the total delay of the comparator delay (t_{comp}) and the digitally controlled delay cell (t_{dig}). Therefore, the two comparator inputs are alternatively reversed. And the period of oscillation can be expressed as $2(RC + t_{comp} + t_{dig})$.

The advantages of the proposed approach can be summarized as follows. Firstly, compared to the analog integrator loop to tune the reference voltage of the comparator in [4, 5, 6], the proposed calibration loop circumvents the use of integrators that entails power-hungry amplifiers. Instead, only one comparator is needed. Secondly, the frequency is tuned digitally. This

Figure 4.3: Operating waveforms of the reference pulse generation.

means all the compensation segments can be shut down after the calibration process is completed, allowing massive power saving in long term operation. The details of digital calibration technique is introduced in the following section 4.3. Since the ambient temperature does not change drastically in the application, the digital compensation circuit is periodically turned on to track temperature variations. Thirdly, the self-compensation is mostly in the digital domain, which can in fact scale better in CMOS process technologies than using analog compensation. Furthermore, the digital compensation section can merge with a larger DSP or SoC system to reduce the overhead. However, due to the digitally controlled method, the tuning step is discrete compared to the analog method. The resolution is determined by the minimum value of the delay cell.

4.2.2 Reference Pulse Generation

A reference signal that has no relationship with the sensitive loop delay is mandatory in the proposed self-calibration system. As shown in Figure 4.1, an additional reference voltage (V_{ref2}) and a replica comparator ($COMP_2$) are used to generate a reference pulse in the on-chip digital compensation technique. The waveforms of pulse generator are given in Figure 4.3. Initially, when the clock signal ϕ is high, the capacitor C_1 is charged by a current source, and the generated ramp voltage V_{ramp} is connected to the negative node of $COMP_1$. Assume that the delay of comparator is t_{comp} , and the digitally controlled delay cell in Figure 4.1 is t_{dig} . After $COMP_1$ triggers, the pulse width of V_1 can be expressed as:

$$t_1 = R_1 \cdot C + t_{comp} \quad (4.1)$$

At the same time, the signal V_{ramp} is also connected to the positive node of the additional comparator $COMP_2$. When $COMP_2$ changes from zero to one, time t_2 is also expressed as:

$$t_2 = R_2 \cdot C + t_{comp} \quad (4.2)$$

These processes allow us to acquire the reference pulse from the time difference between the two t_1 and t_2 , where:

$$P_{ref} = t_1 - t_2 = (R_1 - R_2) \times C \quad (4.3)$$

From equation (4.3), there is no delay parameter in the pulse width expression obviously. The period of the pulse width is only related to resistor and capacitor. It is therefore used as a reference time value for digital compen-

sation algorithm.

The reference pulse is in fact generated by the difference between the two comparators' output V_1 and V_2 , which is an AND function of the two. The mismatch during high-to-low and low-to-high transitions within the same comparator will have little influence on the reference pulse. When considering the non-ideal mismatches between the two comparators, the reference pulse can be expressed as:

$$P_{ref} = (R_1 - R_2)C + \frac{C}{I_B}(V_{os1} - V_{os2}) + t_{comp1} - t_{comp2} \quad (4.4)$$

where V_{os1} and V_{os2} are the offset voltages of two comparators. In order to minimize the offset voltage and comparator delay mismatch, the two comparators are carefully designed during the layout drawing. Figure 4.4(a) shows the effect of process and mismatch on the reference pulse width at 0.9-V power supply voltage. Based on 300 Monte Carlo simulations, the average pulse width is 20.52 ns with a standard deviation of 0.971 ns. Figure 4.4(b) shows the mean value and standard deviation variation within the -55 to 135°C temperature range. The average of reference pulse in the whole temperature range is from 21.14 ns to 20.42ns, and the standard deviation is less than 1 ns when the temperature is above -25°C . In final implementation, R_1 is chosen to be 150 k Ω and R_2 is 80 k Ω . These two resistors are combined with P-poly resistors and N-plus resistors to minimize the temperature coefficient. The layout of R_1 and R_2 are also merged to reduce mismatch.

Figure 4.4: (a) Monte Carlo simulation results of reference pulse at room temperature, (b) Simulated Mean and σ versus temperature.

4.2.3 Time-to-Digital Converter and Loop Delay Controller

Figure 4.5 shows the time-to-digital converters (TDCs) and digitally controlled delay cell architectures. A simple TDC structure is utilized in this design [7]. The time signal passes through a string of delay elements. In order to increase the delay, each of the delay cells in the two TDCs is customized to increase its stage delay time. An array of flip-flops is used to sample every delayed signal. In the proposed design, the precise values of f_{out} and P_{ref} are not required. Instead, a mapping relationship between the reference pulse and the output period will suffice. Therefore, the measured signal goes through a larger delay at first, and is measured by the simple structure to find the falling edge. The TDC1 is an 8-bit thermal code and the TDC2 is of 5 bits, with different weight in each bit. The minimum step of the TDCs is 0.4 ns. Both TDCs use the same delay cells to avoid mismatch. We used the same delay cells for oscillation period and reference pulse measurements, and calibrate the loop delay by reference pulse width.

Therefore, the delay cell variations with temperature and supply voltage will not affect the results of calibration.

The digitally controlled delay line has 6-bit control signals. The first bit is a sign bit to indicate increasing or reducing delay cell. The other 5 bits are thermal codes with different weights: the LSB stands for 0.2 ns, and the MSB represents 1 ns. Therefore there are 5 steps of changing delay, from 0.2 ns to 3 ns. The simulated power consumption of the delay line is about $8.2 \mu\text{W}$ at 0.9 V supply voltage.

Figure 4.5: (a) Schematic diagram of TDC with thermal code output, (b) schematic of digitally controlled delay cell.

Figure 4.6: Schematic diagram of complementary to absolute temperature (CTAT) current bias.

4.2.4 CTAT current Bias and Resistance Temperature Compensation

As all the blocks of the proposed system are working in the near-threshold region, the propagation delay becomes smaller when the environment temperature increases. Therefore, a complementary to absolute temperature (CTAT) current bias source is deployed to compensate this effect. As shown in equation (2.1), the value of current bias can be cancelled in the oscillation period. Hence, precise current value is not critical in the system. Figure 4.6 shows the CTAT current bias generator in the design [8]. Four MOS-FETs (M_1 to M_4) and a resistor (R_1) makes up a normal proportional to absolute temperature (PTAT) source. M_8 copies the current from the PTAT current portion, and offer a low current to M_7 which also operates in sub-threshold region. So the gate-source voltage (V_{GS}) of M_7 has a negative temperature coefficient [9]. Transistors M_5 , M_6 and M_9 build up a negative feedback to fix the voltage V_{GS7} . The value of CTAT current is decided by V_{GS} of M_7 and resistance R_2 , as shown in equation (4.5). In this design, each branch

of current sources is 100 nA. The typical CTAT current is around 200 nA at room temperature and with 0.9-V supply voltage.

$$I_{CTAT}(T) = \frac{V_{GS7}(T)}{R_2} \quad (4.5)$$

From the equation (2.2), the oscillation frequency is dominated by the capacitance and resistance value. In modern CMOS process, the variation of capacitance with temperature can be ignore. However, the resistance varies versus with temperature a lot. Therefore, in order to minimize the temperature coefficient of resistors, two different types of resistors are blended together. In standard CMOS process, the P-type polysilicon resistor has a negative temperature coefficient. The simulated variation is about 1.6% from -55°C to 125°C . On the other hand, the N-type resistor has a positive temperature coefficient of about 18% within the $-55 - 125^\circ\text{C}$ temperature range. Figure 4.7 shows the simulation result of R_1 resistance. Typically, the resistance of R_1 is 150 k Ω . With these two types of resistors, the variation of R_1 becomes 0.51% across the temperature range indicated above.

4.3 Proposed Digital Compensation Method

Figure 4.8 shows the digital compensation algorithm in the feedback tuning loop. Two TDCs are used to convert the time information into digital domain. An reference pulse (P_{ref}) is generated on-chip for calibration, which is described for circuits level in the next section. Here, we describe the digital compensation sequence as follows:

1. At the beginning of oscillation, the main oscillator is initiated while the other blocks are disabled. This creates an oscillation signal f_{out} .

Figure 4.7: Resistance temperature compensation by P-poly and N-plus resistors.

2. When the compensation loop is enabled, the on-chip reference pulse width (P_{ref}) is generated. $TDC2$ measures the pulse width of P_{ref} , converting the time pulse into a digital code N_2 . At the same time, N_1 is obtained by $TDC1$ which measures the width of the output frequency f_{out} .
3. Ideally, the high level pulse of the output frequency can be expressed as $R_1C + t_{con}$, where t_{con} is a constant delay value if the loop delay remains stable when PVT of the chips are varied. Comparing this formula and the reference period value (see equation (4.3)), it is easy to infer a relationship between P_{ref} and the high level width of f_{out} . Therefore, we can estimate a frequency value N'_2 from N_2 .

Figure 4.8: Flow chart of the digital compensation algorithm.

4. Comparing the estimated value N'_2 to a real value N_1 , if N_1 is greater than N'_2 , it means that the frequency is slower than ideal. The loop delay is controlled by several registers to reduce t_d . To ensure a stable loop, when $N_1 = N'_2$ or $N'_2 - 1$, we assume that compensation has been completed. There is a 1-bit margin as far as loop stability is concern. Without this margin, the loop may oscillate at the edge of N'_2 .
5. After the compensation process is completed, all the digital parts and reference pulse generator can be shutdown, leaving just the control bits which are stored in registers to maintain the tuned loop delay. The calibration circuits will be awoken in the next round of compensation.

In practice, N_2 is of 5-bit resolution, whereas both N_1 and N'_2 are of 8-bit digital codes. The digitally controlled delay cell has 6 bits. Because of the digitally controlled delay cell, the compensation circuits such as the replica comparator, TDCs, etc., can be shut down for power saving after compensation.

4.4 Measurement Results

Figure 4.9: Chip micrograph of proposed relaxation oscillator.

The proposed relaxation oscillator was fabricated in 0.18- μm standard CMOS process. Figure 4.9 shows the chip micrograph of the proposed relaxation oscillator, which occupies a chip area of $150\ \mu\text{m} \times 80\ \mu\text{m}$. The analog circuit occupies a space of only $80\ \mu\text{m} \times 73\ \mu\text{m}$. And the digital compensation portion is $80\ \mu\text{m} \times 77\ \mu\text{m}$. For the compensation portion, the digital algorithm is synthesized automatically using digital design flow. We designed the digital circuit by Verilog code at first, then synthesize them from RTL code to final layout block. The additional comparator, TDCs, and

Figure 4.10: Measured waveform of output frequency and reference pulse.

digitally controlled delay line are customized. Figure 4.10 shows the output oscillation clock signal (f_{out}) and the reference pulse signal (P_{ref}) at room temperature. As can be seen, the clock frequency settles at 12.77 MHz, and the reference pulse width is around 21.90 ns. In measurement results, the system consumes 56.2 μ W of power when the compensation circuit is enabled at 0.9-V power supply voltage and room temperature environment. Figure 4.11 shows the simulated power distribution of each portion in the proposed design. Most power consumption is in the TDCs, for converting the time period into numbers, which consumes 26.4 μ W. The main oscillator and pulse generator part both have a comparator which cost some power during operation. After calibration is completed and the compensation part of the system is powered down, only the main oscillator, the bias circuit and one branch of the digitally controlled delay line are operating, consuming 12.8- μ W of power during circuit measurement.

The measured phase noises and period jitters are shown in Figure 4.12.

Figure 4.11: The simulation power consumption pie chart.

Figure 4.12(a) illustrates almost identical phase noises, both with and without digital compensation. Due to the frequency output path (see Figure 4.1), the digital compensation technique only changes the circuit loop delay. When the compensation loop is stable, the loop delay will also remain as a constant value. Therefore, the phase noise of this relaxation oscillator is determined by the analog segment. In the case of the period jitters, as shown in Figure 4.12(b), the standard deviations (σ) are also approaching. Because of the noise in digital circuits, the jitter with compensation is slightly greater than those that has no compensation. However, for design applications, the phase noise and jitter performance are not the most critical parameters. Hence, emphasis has been placed on the frequency stability versus temperature and supply voltage.

The measured PCB and measurement environment are shown in Figure 4.13. In the self-designed PCB (see in Figure 4.13(a)), the output of relaxation oscillator is located on the top. And the power supply of analog

Figure 4.14: Measured oscillation frequency and reference pulse width versus temperature at 0.9-V power supply.

Figure 4.15: Measured oscillation frequency of four chips and with compensation.

is 3.8% without digital compensation, which is about 250 ppm/°C. After the proposed digital compensation, the output frequency varies from 12.71

Figure 4.16: Measured oscillation frequency versus supply voltage.

MHz to 12.77 MHz at 0.9-V supply voltage. The temperature stability is 31 ppm/°C. Furthermore, the measured frequency variation with temperature of four different chips is plotted in Figure 4.15. The frequency range among the four chips is from 12.61 MHz to 12.85 MHz, and the frequency variation in each chip is less than $\pm 0.4\%$. For the largest variation in Chip 4, its output frequency varies from 12.61 MHz to 12.7 MHz. The calculated frequency accuracy is 47 ppm/°C. Since the frequency of the relaxation oscillator is based on the RC time constant, and the RC values vary a lot with different processes. It is thus difficult to guarantee a constant value among different chips. In our application intended, the interest is on the frequency stability versus temperature variation. The frequency difference among different chips can be resolved by trimming manually.

In Figure 4.16, the oscillation frequency versus supply voltage is illustrated. In order to keep the MOSFET in the sub-threshold range, the supply voltage varies only from 0.6 V to 1.1 V. Here, the frequency variation is

Figure 4.17: Measured oscillation frequency versus supply voltage of four chips after compensation.

less than $\pm 0.5\%/V$ after compensation. Figure 4.17 shows the measured frequency results of four different chips. The largest variation is in Chip 3, where frequency varies from 12.68 MHz to 12.8 MHz after compensation.

The performance of our on-chip oscillator compared to other state-of-the-arts are tabulated in Table 4.2. The definitions of the two Figure of merits (FoMs) are already listed in Chapter 3.3 (see Equations 3.8 and 3.9). When compared to circuits with similar frequency design, the proposed work achieves lower power consumption and better temperature coefficient. Compared to other conventional analog compensation designs, the digital compensation circuits in this work can be shut down after temperature is stable. This scheme can save much more power consumption from $56.2 \mu\text{W}$ to $12.8 \mu\text{W}$. In addition, the chip area is one of the lowest referring to designs listed in Table 4.2. Even when compared to designs based on the 65-nm

process, the proposed design's FoMs are better (second largest of FoM_1 and the largest of FoM_2). The better FoMs mean that this relaxation oscillator is higher output frequency, lower power and better temperature coefficient. Furthermore, with the digital compensation approach, it is also easier for CMOS process scaling than using the conventional analog compensation techniques.

4.5 Conclusions

In this chapter, a novel on-chip RC relaxation oscillator with digital compensation technique to achieve a stable output frequency with environment temperature and supply voltage variations is presented. The digital compensation scheme can avoid the power hungry analog op-amp integrator feedback loop. The digital method not only save more power in the long run, but provides the ease of design when comes to CMOS process scaling. Furthermore, an on-chip reference pulse generator is adopted for the compensation. The digital feedback loop is also able to tune the loop delay to adjust the output frequency.

The relaxation oscillator test chips were fabricated in a 0.18- μm standard CMOS process. The performance of the proposed digital compensation method has also been verified to maintain frequency stability of the relaxation oscillator. The output frequency is stable at 12.77 MHz, 0.9-V power supply voltage. The measurement results showed that the output frequency has only 31 ppm/ $^{\circ}\text{C}$ variation with temperature range of -30 to 120 $^{\circ}\text{C}$ after compensation. The frequency variation over the supply voltage is $\pm 0.5\%/V$. Compared to other state-of-the-art designs, the relaxation oscillator design has better FoM performance and the smallest temperature coefficient. The

Table 4.2: Performances summary and comparison

Reference	[3]	[4]	[5]	[6]	[10]	[11]	[12]	[13]	This Work
Process (nm)	65	130	65	180	65	180	180	180	180
Technology	Comp. offset cancellation	Integrator feedback	Switched-cap integrator	VAF feedback	Self-chopped oscillator	Analog compensated	Regulated ring oscillator	Comp. with ADPLL	Digitally compensation
Area (mm ²)	0.032	0.007	0.01	0.04	0.048	0.22	0.086	1.04	0.012
Frequency (MHz)	0.0185	1	12.6	14	0.032	10	4.7	2 – 40	12.77
Jitter (σ) (ps)	N.A.	N.A.	N.A.	30	N.A.	N.A.	93	N.A.	78.7
Temp. (°C)	–40 – 90	25 – 200	0 – 80	–40 – 125	–20 – 100	–20 – 100	–40 – 125	0 – 70	–30 – 120
Temperature Coefficient (%)	± 0.25	N.A.	± 0.82	± 0.75	± 0.1	± 0.4	± 0.35	N.A.	± 0.4
Temp. Coefficient (ppm/°C)	38	108	205	90	32.4	66	21	2.42	31
Supply (V)	1.2	2.5	1.1 – 1.5	1.7 – 1.9	1.6 – 3.2	1.2	1.4 – 3.3	3.3/1.8	0.6 – 1.1
Freq. Variation with VDD (%/V)	1	1.09	± 0.175	± 0.8	± 0.1	± 0.05	± 0.2	± 30 ppm	± 0.5
Power (μ W)	0.12	428	98.4	45	4.48	80	53	2900*	56.2 (12.8 for OSC)
FoM_1^{**} (dB)	113	93	111	115	98.5	111	109	101	113 (120)
FoM_2^{***} (dB)	177	156	167	178	164	174	178	176	180 (186)

*Include on-chip heaters.

** $FoM_1 = 10 \log(f/P)$

*** $FoM_2 = 10 \log \frac{f \cdot \Delta T}{P \cdot TC}$

total power consumption is $56.2\ \mu\text{W}$ when all circuits are enabled. For long term operation, the power consumption can be scaled to only $12.8\ \mu\text{W}$ in the main oscillator.

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Chapter 5

An Digital Phase-Locked Loop with Injection Locked Technique

The design of an all-digital phase-locked loop for processor clock generator application is presented in this chapter. In order to save on power consumption and also to reduce the design complexity, the proposed design avoids power hungry time-to-digital converter (TDC) phase detector, and instead uses a D flip-flops (DFF) bang-bang phase detector. The injection-locked technique is used to improve the phase noise performance. This design is fabricated in 40-nm CMOS process.

5.1 Introduction and Motivations

5.1.1 ISM Band Application

The industrial, scientific and medical (ISM) radio bands are radio bands (portions of the radio spectrum) reserved internationally for industrial, sci-

entific and medical purposes other than telecommunications [1]. Despite the intent of the original allocations, the fastest-growing deployment of these bands in the recent years have been for the short-range, low power communications systems. The wireless phones, Bluetooth devices, near field communication (NFC) devices, and wireless computer networks are all using frequencies allocated to low power communications and also the ISM band.

The ISM bands are defined by the International Telegraph Union (ITU) radio regulations (article 5) in footnotes 5.138, 5.150, and 5.280 of the radio regulations. There are several frequency allocations and the research were focused on smart building. Thus, the frequencies of interest are: 433 MHz, and 915 MHz.

5.1.2 Motivation

Figure 5.1: Architecture of the ARM CoreTile Express processor.

This design is implemented as a clock generator for a DSP processor in

wireless sensor network which is for smart buildings data communication and processing using ISM band. Figure 5.1 shows the architecture of ARM CoreTile Express processor [2]. As shown in this figure, the pink box is the internal clock generation, which is generally an internal phase locked loop (PLL). As it is a customized processor, the highest clock frequency is around 1 GHz. For low-power low-cost purposes, the all digital PLL structure is chosen.

5.1.3 Organization

This chapter is organized as follows. After the introduction and motivation for processors, Section 5.2 shows the architecture of proposed all-digital phase-locked loop (ADPLL). The injection-locked scheme is also discussed with analysis. Section 5.3 presents the injection-locked technique in the proposed ADPLL. The measurement results both with and without injection scheme, are detailed in Section 5.4. Finally, Section 5.5 concludes the chapter.

5.2 Digital Phase-Locked Loop Design

5.2.1 Architecture of ADPLL

The architecture of the proposed all-digital phase-locked loop is illustrated in Figure 5.2. This proposed system mainly consists of two loops. One consists of the replica oscillator which is named as a replica loop: a replica ring oscillator, a digital loop filter, a DFF for phase detector, a multiplexer for switching between two loops, and a frequency divider. The other loop is the main oscillator loop, which contains the main ring oscillator for final frequency output and the injection-locked circuits. A multiplexer is located

Figure 5.2: Architecture of the proposed all-digital phase-locked loop.

between oscillators and frequency divider, which is used for switching the two oscillators in the loop. The main reason of having two loops is to solve the injection-locked timing delay issue. Further details of the injection-locked technique will be provided in the following section.

This PLL also includes two loops. One is the frequency locked loop, and the other is the phase locked loop. For the frequency locked loop shown in Figure 5.2, it uses digital up-down counters as a simple structure to trace the oscillator frequency coarsely. At the beginning of frequency locked, two counters in the frequency locking loop calculates the feedback oscillation numbers and reference clock period numbers. When the values of two counters are nearly the same, we can consider that the divided oscillation frequency nearly equals to the reference one. After the oscillator frequency is locked to the desired output frequency, the PLL will be switched into the phase locking loop operation step. The phase locking scheme includes a DFF and a digital loop filter. The DFF is worked as a bang-bang phase detector

to compare the difference phases between reference clock and feedback signal. The phase error will be sent into digital loop filter (DLF) for processing. The outputs of DLF tune the output frequency of digitally controlled oscillator (DCO). Compared to conventional high-resolution TDC phase detector, it can save much power and active area. However, the performance of bang-bang phase detector is also worse than TDC based architecture. Therefore, we also implement a injection locking technique to improve the phase noise and jitter performance of the proposed ADPLL.

5.2.2 System Model

Generally, a PLL is a higher order closed loop system. In order to verify the loop stability and performance, Matlab modelling of the system is preferred. There are several benefits of using Matlab models. Firstly, it can build mathematical models and transfer functions, which helps in the understanding and appreciation in both the principle of operation and loop stability. Second, the behavior model simulation is much faster than circuits level simulation. It can verify these ideas easily and efficiently. In addition, Matlab simulation is most helpful debugging after constructing the transistor level circuits. When simulating transistor level circuits in Cadence Spectre, any major deviation from the behavior model allows the designer to replace the transistor circuits with ideal model to identify the root cause. Finally, for PLL simulation, it is difficult to acquire the final closed loop phase noise performance in Spectre simulation. Therefore, a combination of the Matlab and Spectre simulation is always necessary. From Cadence Spectre, the oscillator simulation phase noise data is obtained and ported into Matlab model to simulate the complete phase noise performance for the

loop.

(a)

(b)

Figure 5.3: (a) System model of a continuous PLL, (b) circuits model of loop filter in a charge pump PLL.

Because it is difficult to get a discrete time transfer function directly, the conventional continuous time loop filter always is the first to be built. Figure 5.3 shows a Matlab behavior model of a conventional charge pump PLL (CPLL). The loop filter in Figure 5.3(a) is constructed using two modules; one is the transfer function model (in the top box), and the other is the RC circuits loop compensator (in the bottom box). Figure 5.3(b) illustrates

the RC loop filter circuits model. From the conventional charge pump PLL model, the loop transfer function can be derived as [3]:

$$H(s) = \frac{\frac{I_{cp}}{2\pi}(R_2 + \frac{1}{C_2s})\frac{K_{VCO}}{s}}{1 + \frac{1}{K_n}\frac{I_{cp}}{2\pi}(R_2 + \frac{1}{C_2s})\frac{K_{VCO}}{s}} = \frac{\frac{I_{cp}K_{VCO}}{2\pi C_2}(R_2C_2s + 1)}{s^2 + \frac{I_{cp}}{2\pi}\frac{K_{VCO}}{K_n}R_2s + \frac{I_{cp}}{2\pi C_2}\frac{K_{VCO}}{K_n}} \quad (5.1)$$

where I_{cp} is the current of charge pump, K_{VCO} is the gain of voltage controlled oscillator in continuous time PLL, and K_n is the divider ratio. From equation (5.1), two important parameters of the PLL are obtained:

$$\omega_n = \sqrt{\frac{I_{cp}}{2\pi C_2} \frac{K_{VCO}}{K_n}} \quad (5.2)$$

$$\zeta = \frac{R_2}{2} \sqrt{\frac{I_{cp}C_2}{2\pi} \frac{K_{VCO}}{K_n}} \quad (5.3)$$

ω_n is the natural frequency, and ζ is the damping factor. The natural frequency expresses a measure of the response time of the loop, and the damping factor means the signal overshooting and ringing when the stability is rebuilt. Theoretically, the natural frequency should be high enough for fast settling and the damping factor is set to be near the critical damping activity ($\zeta \approx 0.707$) [4].

The loop parameters can be determined through the Matlab behavior simulation. The loop stability was simulated and shown in Figure 5.4. Figure 5.4(a) expresses the step response of the continuous CPLL. After amplitude normalization, the damping factor is set to around 0.7. As seen, both the overshoot and settling time are within the acceptable value of $0.4 \mu s$ and $1.04\times$ overshoot. Figure 5.4(b) shows the phase margin of the closed loop. From the behavior simulation, the loop bandwidth is set at about 1.5 MHz, and the phase margin is 65.2° , which can ensure a stable loop.

Based on the loop parameters of the conventional continuous CPLL, the

Figure 5.4: (a) Step response result of CPLL, (b) Phase margin of CPLL.

discrete time loop filter in Z-domain is determined. After got the discrete time digital loop filter transfer function, the entire ADPLL behavior model can be obtained as shown in Figure 5.5. The behavior model of ADPLL

Figure 5.5: Matlab model of whole proposed ADPLL.

is same as the block architecture level in Figure 5.2, which consists of a DFF phase detector, digital loop filter, injection signal generator, and two DCOs. The DFF phase detector acts a simple bang-bang PFD. This implies that it can only determine if the feedback signal arrives earlier or later than the reference clock. The z-domain transfer function based digital loop filter achieves the same performance as a continuous charge pump loop filter as mentioned above. Because it is a behavior simulation for idea verification, the switching between two loops are controlled manually in this whole loop simulation.

Figure 5.6 shows some Matlab simulation results of the proposed ADPLL. The output oscillation frequency spectrum is given in Figure 5.6(a). The reference clock signal is chosen 40 MHz in the proposed design. From this spectrum waveform, when the frequency divider ratio is set at 26, the output frequency is 1.04 GHz. Figure 5.6(b) shows the time domain waveforms of the critical signals in the loop. When the DFF phase detector triggers to zero, it means that the feedback signal is earlier than the reference clock. On the contrary, the feedback is later than the reference clock if the DFF phase

(a)

(b)

Figure 5.6: (a) Spectre simulation result of system model, (b) time domain waveform simulation results.

detector gives high. The output of phase detector is sent to a digital loop filter for processing. The long trail of DLF output in the fourth row is due to the loop delay from the PD to the feedback signal. The last two rows show the output behavior waveforms when the injection signal is enabled. The simulated phase noise performance both with and without injected signal

are illustrated in Figure 5.7. These waveforms are achieved by co-simulation with Matlab and Cadence Spectre. This allows the oscillator phase noise to be acquired from the transistor level circuit simulation in Cadence Spectre. The phase noise data of the oscillator will then be used in Matlab to evaluate the closed loop performance. From the simulation results, the in-band phase noise can be improved from 73 dBc/Hz to 96 dBc/Hz using the injection-locked technique. Here, the out-band noise performance remains almost the same. This is because of the closed loop characteristics of the PLL which is in fact, a high-pass filter for the oscillator noise [5].

Figure 5.7: (a) Phase noise simulation without injection in system model, (b) with injection.

5.2.3 Digital Loop Filter

In conventional continuous time CPLL, the analog RC loop filter is usually engaged. Figure 5.3(b) presents its behavioral model. A digital loop filter can be actually derived from analog filter using the bilinear transform (see Figure 5.8) [6]. The equivalent digital filter is constructed of two major paths: a proportional path and a integral path. Assuming parameters α and β are the gain of the proportional path and integral path, respectively, they

Figure 5.8: Transformation of a RC filter to a discrete digital filter.

can transfer from an analog filter's parameters (R and C in Figure 5.8). The bilinear transform is commonly used to design digital filters based on their analog prototypes [7]:

$$s = \frac{2}{T_s} \frac{1 - z^{-1}}{1 + z^{-1}} \quad (5.4)$$

where T_s is the sampling period of a z-domain system, which is just equal to $1/f_{clk}$ in the digital filter design. The z-domain transfer function of the digital loop filter can be expressed as:

$$H(z) = \alpha + \beta \frac{1}{1 - z^{-1}} = \frac{(\alpha + \beta) - \alpha z^{-1}}{1 - z^{-1}} \quad (5.5)$$

The s-domain transfer function of the analog filter shown in Figure 5.8 can be expressed in the discrete time (z-domain) as follows:

$$Z(s) = \frac{V(s)}{I(s)} = R + \frac{1}{sC} \quad (5.6)$$

$$Z(z) = \frac{(\frac{T_s}{2C} + R) + z^{-1}(\frac{T_s}{2C} - R)}{1 - z^{-1}} \quad (5.7)$$

Comparing equation (5.5) and (5.7), the values of α and β can be found as:

$$\alpha = R - \frac{T_s}{2C} \quad (5.8)$$

$$\beta = \frac{T_s}{C} \quad (5.9)$$

(a)

(b)

Figure 5.9: (a) Frequency locking RTL simulation in Modelsim, (b) Phase locking simulation.

After obtaining these important parameters, i.e., α and β , the digital loop filter mathematical model is converted to a register-transfer level (RTL) code model. The RTL is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers. The RTL simulation was also finished by Modelsim tool with some results shown in Figure 5.9. During this simulation, all blocks RTL model were built, and connected together as a closed loop in testbench. In Figure 5.9(a), it shows the frequency locking procedure. In the frequency locking step, the fine tuning codes are freezed, and only coarse tuning codes change the oscillator

current for changing frequency step by step. After frequency locking, the system will give a tag signal to turn on phase locking process. In phase locking process, the coarse tuning nearly maintains stable except extreme situation. Figure 5.9(b) illustrates some results of phase locking. In this figure, the feedback signal and reference clock almost have the same phase. The coarse tuning bits are kept constant, and only fine bits control the oscillation frequency.

5.2.4 Digitally Controlled Oscillator

Figure 5.10: Circuits of digitally controlled oscillator.

Figure 5.10 shows the transistor level circuits of digitally controlled oscillator design in the proposed ADPLL. Because of the area consideration and about 1 GHz highest oscillation frequency, a ring oscillator structure is chosen. Compared to LC tank oscillator, a ring oscillator generally has a compact silicon area but worse phase noise performance. In this design, the DCO has three stages delay cells which are controlled by PMOS current sources. Each delay cell consists of two inverter based amplifiers and a pair

of negative resistor loadings except the second stage. They can improve the intrinsic gain of each stage. In the second stage, due to injection locked technique, an additional switch is appended between the two outputs of delay cell, as shown in Figure 5.11(a). When the injection signal occurs, it will connect the amplifier differential outputs together. After the injection signal goes from high to low, the switch is released. Therefore, the edge of oscillation in this stage will be aligned with the injected reference signal. The detail principle of injection locking technique will be described in the next section.

There are two tuning controller in this DCO. For the coarse tuning, the control bits tune the current mirrors of the oscillator. In the fine tuning structure, we control the capacitance on and off to change each stage capacitance loading. The circuits of DCO fine tuning is shown in Figure 5.11(b). In the fine tuning, the loading MOS-FETs' source and drain are connected together as capacitors. The bulk of transistors is fixed to ground. The gate terminal is used as a controller. Figure 5.12 shows the MOSFET capacitor cross overview and the capacitance variation verses gate-source voltage [8]. In Figure 5.12(b), the red dash line is the capacitance variation when three terminals (source, drain and bulk) are all connected together. For the connection in this design, the capacitance curve is shown as black solid line. Due to body effect, the threshold voltage of transistor (V_{th}) shifts. The fine tuning control bits are connected to drain and source terminals of loading transistors. When the control bits switch, the capacitance value also varies. In this design, the minimum capacitance variation is about 4 fF in simulation.

The simulation results of DCO and layout are shown in Figure 5.13.

Figure 5.11: (a) Injection circuits in the 2nd DCO stage, (b) DCO fine tuning by capacitors.

Figure 5.12: (a) MOSFET capacitance cross view, (b) capacitance versus gate and source voltage.

The frequency range of DCO can cover from 400 MHz to 1.2 GHz, which is suitable for processor clock frequency. And the layout area is only $20 \mu\text{m} \times 20 \mu\text{m}$.

5.3 Injection-Locked Circuits

When two different frequency signals inject into one oscillation circuits, one frequency will be coupled to another one. It is called injection lock-

Figure 5.13: Simulation results of DCO and the DCO layout design.

ing phenomenon [9]. The frequency sources can be oscillators, PLLs and etc. These two frequencies are the injection signal and the original signal, respectively. Two phenomenons occur in the original oscillator: frequency pulling and phase locking. Generally, frequency pulling means that the operation frequency of original oscillator is changed by other environment parameters, such as power supply and loading impendence. Usually, phase locking has several important applications, but frequency pulling is undesired. The phase locking technique is used in many systems as: frequency dividers, multiple equal phase output oscillators, frequency multiplier and clock and data recovery circuits. In this section, the case of a multiplier is only discussed.

5.3.1 Injection-Locked Oscillators

An mathematical model of injection-locked oscillator (ILO) is shown in Figure 5.14 [10], where $f(e)$ is a nonlinear block followed by a frequency selective block $H(\omega)$. The nonlinear block is used to model all nonlinearities in the oscillator. In this model, the output frequency consists of many high

Figure 5.14: Model of an injection-locked oscillator.

order harmonics, which can be expressed as:

$$y(t) = \sum_{m=0}^{\infty} b_m \cos(m\omega_o t) \quad (5.10)$$

where ω_o is the free-running frequency of the injection-locked oscillator and b_m is the amplitude of the m th harmonic signal. The injection signal can be shown as:

$$v_i(t) = \sum_{n=0}^{\infty} a_n \cos(n(\omega_i t + \phi)) \quad (5.11)$$

where ω_i is the frequency of the injected signal, a_n is the amplitude of the n th harmonic, ϕ is the phase difference from the local oscillator. The signal will inject into a free running oscillator. The results of injection can be given:

$$u(t) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} a_n b_m \cos(n\omega_i t + n\phi) + \cos(m\omega_o t) \quad (5.12)$$

When the ILO is used as a multiplier, equation (5.13) can be simplified by trigonometric function [11].

$$\begin{aligned} u(t) = & a_0 b_1 \cos(\omega_o t) + \frac{1}{2} a_N b_0 \cos(\omega_o t + N\phi) \\ & + \frac{1}{2} \sum_{n=1}^{\infty} a_n b_{Nn\pm 1} \cos(\omega_o t + n\phi) \end{aligned} \quad (5.13)$$

where N is the ratio between ω_o and ω_i . From these equations above, we mentioned that the multiplication used much weaker harmonics to produce the injection signal. However, there are some issues about it. The first issue is that when the oscillator is a voltage-controlled oscillator (VCO), to avoid the ILO locks to a wrong frequency, the control voltage must be set in a specific value. Because if the control voltage varies much, the frequency might be locked in a wrong ratio. Secondly, the phase noise performance of the ILO will track to the injection signal. And it is also related to the locking range. Thus, to achieve the best phase noise of ILO, the location of ILO frequency should be set to the center of the locking range. It needs a precise tuning circuits for the oscillator. Thirdly, it is difficult to ensure a precise frequency and phase ratio between the ILO free-running frequency and the injection signal. Thus, there is a phase mismatch between the injection signal and the ILO output.

5.3.2 PLLs with Injection-Locked

To endure the injection issues introduced in the above subsection, a PLL feedback system is adopted with injection locking technique [12]. The PLL system can force the ILO oscillation to locate at the center of the desired frequency range as well as the locking range. Nevertheless, due to the delay of PLL loop, a phase difference between the injection reference and the oscillator feedback signal occurs, as shown in Figure 5.15. We assume that the injection generator delay is t_i , and the time delay from oscillator to feedback is t_d . The injection signal will push the phase of ILO to be equal to *Ref* injection signal, and the PLL closed loop system is going to pull the phase away to reference due to the time delay. In Figure 5.15, the red rising

Figure 5.15: Timing issue due to loop delay of ILPLL.

edge is the effect of injection locking scheme. This period time becomes $t_d + t_i$ not the original oscillation period. The delay will cause significant spurs and might affect the stability issue of the PLL system. Thus, in order to stabilize the entire system, the delays in the injection path and in the feedback path need to be calibrated to be matched. Generally, this compensation also need a calibration system such as a delay-locked loop (DLL) system to adjust the injection position and strength.

There are many publications for solving this issue. In [13], it added two digitally controlled delay-lines (DCDLs) to re-timing injection windows. However, this method cost a lot of silicon area and power consumption. In [14], a combination of frequency locked loop, subsampling PLL and injec-

tion locking is implemented. In the proposed design, we use a dual-loop architecture to avoid the time issues.

5.3.3 Dual-Loop Injection-Locked PLL

In this design, a dual-loop injection-locked ADPLL is proposed as shown in Figure 5.2. This system can avoid delay issues discussed above compared to the conventional injection locked PLL. In this system, there are two loops and two oscillators. The replica one copies from the main oscillator directly, and they are located together in the layout design to minimize mismatches. In normal operation of the system, the replica oscillator is replaced in the PLL feedback loop to grantee the its oscillation frequency to be in the desired lock range. The control bits of the replica oscillator are also used to control the main oscillator after digital calibration. The main DCO is located out of the PLL loop to avoid the feedback effect. Due to frequency locking of the replica one in the loop, the main DCO is also set to a desired output frequency for injection locking technique. Therefore, no timing issues will occur when the reference signal is only injected into the main oscillator to align the phase information.

This system operation consists of three steps. The first two steps are used to start up and to calibrate the mismatch between two oscillators, whereas the third phase is used for general frequency generation. The first step is only enabled the replica oscillator and recorded the control bits (see Figure 5.16). In this step, only the replica oscillator is connected into the PLL feedback loop in order to record the coarse and fine tuning value when the system is stable. The control bits are stored in some registers. After the replica oscillator reaches stable, the system will move onto the second

step. It starts by connecting the main oscillator into PLL feedback loop and remove the replica one from the loop, which is shown in Figure 5.17. In the second step, the main oscillator is connected into system loop until the loop is stable. But the injection locked circuits are not turned on at this moment. Similarly, these coarse and fine control bits are also stored. Then we compare the bits in second step with the bits from first step. It is used for mismatch cancellation between the two oscillators. The tuning bits difference are compared and stored to calibration the main oscillator frequency drift due to process or temperature variations in the following operation.

Figure 5.16: First operation step of the ADPLL.

Figure 5.18 shows the third operation step of the system. In this step, the MUX chooses the replica oscillator in the feedback loop. Thus, the main oscillator can be seen as a free-running oscillator with injection locking technique. The replica DCO within the feedback loop can also be seen as a frequency locked loop. Because of the mismatch calibration in the second step, the frequency of replica one is the same as the main DCO. The feedback loop and replica DCO can maintain the main oscillator to stay in the correct

Figure 5.17: Second operation step of the ADPLL.

Figure 5.18: Third operation step of ADPLL and the frequencies variation of three steps.

frequency range of injection. The injection locking circuits are also enable in this step, which can help to keep output frequency of main DCO precisely and to improve the jitter performance. On the right side of Figure 5.18, the frequencies variation pattern during the three process steps is illustrated. During the first two steps, the system operates for calibration of mismatches between the main DCO and the replica one. Step 3 is used to generate the final frequency output with injection locked technique.

The circuits of injection locked is shown in Figure 5.19. The injection signal is generated by the reference signal and several logic gates. The injec-

tion pulse is sent into the second stage of ring oscillator which is described in Section 5.2.4. The injection pulse will connect the two differential outputs of delay stage together, and then release them at the falling edge. In Figure 5.19, it also shows the waveforms of oscillator free running and injection locked. After the injection locked, the phase of oscillator will be aligned at the falling edge of injection pulse.

Figure 5.19: Injection locked circuits and waveforms.

5.4 Measurement Results

The proposed ADPLL design involves both the conventional analog circuits and digital circuits. The flow of such mixed-signal design is shown in Figure 5.20. In the figure, the rectangle shapes follows the conventional analog circuits design flow. The schematic is designed using Cadence Virtuoso,

and then customized the layout circuits manually. On the other hand, for the digital circuit portions, such as loop filter, divider, frequency locked loop, are designed by the digital flow. The RTL code is designed and simulated by Modelsim, synthesized into gate level circuits by the Design Compiler of Synopsys. For the placing and routing step, Synopsys' IC Compiler is chosen to generate the layout and post timing documents. After completing the layout procedures, the two parts were combined with the pads frame.

Figure 5.20: Design flow of the mixed-signal ADPLL.

The die photograph of the proposed ADPLL is shown in Figure 5.21. It is fabricated in 40-nm GLOBALFOUNDRIES CMOS process. There is a non-volatile memory layer on the top of the process. Thus, the circuits detail cannot be displayed under the microscope except the logo. The entire layout of the proposed design is also shown nearby the die photograph. It only occupies a chip area of $120 \mu\text{m} \times 60 \mu\text{m}$, which is even less than a pad silicon area. The ADPLL can generate a frequency from 400 MHz to 1 GHz for processor applications. The external reference clock is set to be 40 MHz.

Figure 5.21: Die photograph and layout of the proposed ADPLL.

Figure 5.22: Measured phase noise output of the ADPLL.

Figure 5.22 shows the measured phase noise performances, both with and without injection locking signal, using a spectrum analyzer. The line at the top and the middle line are the phase noise without and with injection locking, and the bottom curve shows the reference phase noise performance.

Figure 5.23: Measured jitter performance of the ADPLL.

From this figure, it is evident that the injection locked technique can improve the phase noise performance of ADPLL significantly. The system loop bandwidth is set to around 1.4 MHz. Thus the phase noise performance nearly keeps the same value out of band. And the injection locked circuits can improve the in-band phase noise, from 86 dBc/Hz at 10 kHz frequency offset to 95 dBc/Hz. At 100 kHz offset, it is improved to 101 dBc/Hz from original 94 dBc/Hz. The red curve shows the reference signal provided by signal generator, which is sent into main oscillator to align the edges. The performance of reference clock can determine the final output signal directly. In case there is lower noise reference clock source, the results will be better.

Figure 5.23 illustrates the measured jitter performance of the output clock signal at 1 GHz. The RMS jitter is about 4.87 ps, and the peak-to-peak jitter can be measured as 33.33 ps. The measured power consumption

of the ADPLL is about 1.2 mW at 1-V power supply. The power distribution of each portion is shown in Figure 5.24. In this design, the power hungry TDC architecture is discarded. Therefore, the two DCOs are the most power hungry blocks of the whole system. Since the current staving DCO uses current sources to control the output frequency, great amount of current is required to cover all the process and voltage variations. The second power consuming block is the DLF which consists of a digital loop filter to stabilise the loop and also to perform calibration, i.e., the first two steps of the tuning process in the ADPLL. From this figure, if it is going to reduce more power in the future work, the DCO and DLF portions are the most important.

Figure 5.24: The power distribution pie chart.

The performance comparison between the proposed ADPLL and other states-of-arts is provided in Table 5.1. It is evident that the proposed ADPLL achieves a FoM of about -225.4 dB where the FoM is defined as:

$$FoM = 10 \cdot \log\left[\left(\frac{\sigma_t}{1s}\right)^2 \left(\frac{P}{1mW}\right)\right] \quad (5.14)$$

where σ_t is the root mean square (RMS) phase jitter of the PLL output frequency, and P is the power consumption of the ADPLL. When the FoM is lower, the jitter performance of PLL will be better and power consumption is lower. Among the five digital PLL designs in this table, our work can get the second lowest FoM value. The work in [15] has a closer performance compared to the proposed. However, it consumes more power. The designs of [16] and [17] used advantage process technology but have less FoM. In [18], its FoM is much better, but it is implemented at 130nm process and occupies much more silicon area.

Table 5.1: Performance comparison

Reference	[15]	[16]	[17]	[18]	This Work
Process (nm)	65	28	28	130	40
Area (mm ²)	0.048	0.04	0.026	0.25	0.072
Ref (MHz)	50 – 400	15	10 – 30	375	40
Freq. (GHz)	0.8 – 1.7	0.01 – 0.63	0.032 – 2	0.8 – 1.8	0.4-1
Supply (V)	1.2	0.9	1	1.2	1
Power (mW)	3 @ 1.5G	3.1 @ 250M	2.2 @ 1G	0.89	1.2 @ 1G
Jitter (ps)	3.6	30	16.1	0.92	4.9
FoM^* (dB)	-224.2	-205.5	-212.4	-249	-225.4

$$* FoM = 10 \cdot \log\left[\left(\frac{\sigma_t}{1s}\right)^2 \left(\frac{P}{1mW}\right)\right]$$

5.5 Conclusions

The chapter presents a proposed all digital phase locked loop (ADPLL) design with injection locking technique for processor clock generator. Two loops and two digital controlled oscillators can solve the timing issues in

conventional injection locked PLL. For the main oscillator, it is set out of the feedback loop of PLL and uses information from replica one to keep the injection locking range. Furthermore, the injection scheme can avoid using power hungry high resolution TDC in conventional architecture. The system is fabricated in GLOBALFOUNDRIES 40-nm CMOS process, which occupies only a silicon area of just 0.072 mm^2 . In measurement results, the in-band phase noise can reach 101 dBc/Hz at 100 kHz offset. Its jitter performance is around 4.87 ps for RMS jitter and 33.33 ps peak-to-peak jitter. The measured power consumption is a mere 1.2 mW.

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Chapter 6

Summaries and Future Work

This chapter summarizes the research work accomplished throughout the graduate studying. After providing the introduction and literature review, two relaxation oscillators for replacing the off-chip crystal oscillators are discussed. An all-digital PLL is then designed for on-chip clock generation network. In the future, a method to combine the relaxation oscillator and PLL clock generator together will be explored. An entire clock provider network will finally be built on-chip for the electrical systems.

6.1 Summary of Thesis

In this thesis, a brief introduction and literature review of the clock generators for electrical system in smart buildings application are described in the first two chapters. The focuses are on the electrical systems for smart buildings application. Because of the different outdoor environments and locations of buildings, these clock generators are required to generate a stable frequency during such complex environments, especially the temperature variations.

Two RC on-chip relaxation oscillators are discussed in detail in the Chapter 3 and Chapter 4. One uses conventional analog compensation method, and the other one operates with a novel digitally calibration way to approach a stable output frequency. In the measurement results, both of them can generate a stable frequency with temperature and voltage variations. In the lab environment, thermal stream is used to change temperature from -30° to 120° . This temperature variation is far more than the general outdoor and building surface temperature range. Even under such large variations, the two on-chip relaxation oscillators can maintain frequency variations to about $\pm 0.5\%$, hence meeting the requirements of smart buildings. Also, the power consumptions of each oscillator are $48.8 \mu\text{W}$ and $56.2 \mu\text{W}$ in total. In the second relaxation oscillator design, the compensation portion from analog domain was shifted to the digital domain. This will benefit as the technology continues scale down and also allows merging of the oscillator with other digital signal processing blocks. The main drawback of the on-chip RC relaxation oscillators is the difficulty in handling of the process variation as the oscillation period is based on the RC production value. The absolute values of resistors and capacitances vary significantly in the solid state CMOS processes. This will be the key issue to resolve in the future design.

After the evaluation of the on-chip relaxation oscillators, the research efforts were shifted to much higher frequency clock generator for digital processors in SoCs, the phase locked loop. In Chapter 5, an all-digital PLL with injection-locked technique is presented. In the proposed ADPLL design, it removes the power hungry TDC in conventional structure to save power consumption. The injection locked technique is implemented to improve

phase noise and jitter performance further. The dual-loop architecture is used to solve the delay issue between divider delay and injection circuits delay time. In measurement results, the in-band phase noise is about 100 dBc/Hz at 10 kHz offset. Its jitter performance is around 4.87 ps for RMS jitter and 33.33 ps peak-to-peak jitter. The measured power consumption is only 1.2 mW at 1 GHz output frequency. The proposed ADPLL can generate a clock signal from 400 MHz to 1 GHz, and has an excellent jitter performance, which is suitable for customized digital signal processors.

6.2 Future Work

There are still many work to be done in the on-chip clock generation area. With the rapid development of semiconductor's technology, the SoC chips are smaller, faster and contains more function blocks. To pursue this trend, the clock generator is also required to integrate more functions.

6.2.1 An Entire Clock Generator and Network

In this thesis, some low frequency relaxation oscillators to replace the off-chip crystal, and a higher frequency ADPLL for processors are presented. The plan for the next phase is to integrate all together, to build a complete clock generation system on chip. A preliminary proposed clock generator and distribution network is shown in Figure 6.1.

In this on-chip clock generator system, a relaxation oscillator is implemented to provide a reference clock which is stable versus temperature and voltage variations. The oscillation frequency is about dozens of megahertz. This clock works as a reference clock to a phase locked loop (PLL_1) in the first clock generation level. PLL_1 generates frequency around several hun-

Figure 6.1: A clock generation and distribution network example.

dred megahertz or gigahertz. The clock streams will be sent to each blocks after many dividers and buffers. One of them is sent to PLL₂ in secondary clock generator. The PLL₂ in Figure 6.1 is used for some portions which need much cleaner jitter clock, such as high resolution ADCs or RF transceiver blocks. The reference clock of this PLL₂ comes from the first one after division, which is about several hundreds megahertz generally. The reason using such high frequency is that it can help to reduce the noise and improve the jitter performance. Moreover, a digital calibration method is also implemented. The digital feedback compensation provide some control bits to every level clock generator source. As mentioned in the Chapter 4, it can help to keep frequency stability versus process, voltage and temperature variations.

In this system, the on-chip relaxation oscillator and PLL are combined together, and the analog circuits (as the RC relaxation oscillators) and digital circuits (such as DPLL, digital calibration) are merged into one complex system. This not only save the cost of SoC system, but also meet the trend of semiconductor process shrinking.

6.2.2 Frequency Synthesizer

The ever increasing adoption of communication interfaces requires the integration of protocol stacks for electrical systems and wireless communication standards onto ASICs or full custom SoCs. Generally, many subsystems for each interface are merged and integrated together in a single SoC. Most subsystems have their own dedicated CPU cores, baseband processors, analog to digital interface, and RF circuit, as shown in Figure 6.2 [1]. As the modern SoCs integrate digital processors, analog baseband circuits and RF transmitters together, in order to save more power and cost, it would be ideal if only one on-chip clock generator is used to provide the necessary frequency signals for all blocks. Therefore, the clock generator should also be able to act as a frequency synthesizer for the RF front end circuits.

Figure 6.2: A SoC with WLAN and Bluetooth subsystem baseband and processors [1].

There are three major conventional frequency synthesis techniques: di-

rect analog mixer, direct digital synthesis (DDS), and indirect by PLLs [2]. The work here focuses only on the last. In general, the indirect synthesizer uses a PLL and a programmable fractional-N divider, which multiplies the stable frequency f_{ref} . Figure 6.3 shows a block diagram of a proposed frequency synthesizer based on digital PLL. The key components of the structure are a high-resolution TDC, a digital-to-analog converter with a passive implementation to control the oscillator, a digital correlation circuits to cancel the quantization noise in TDC [3], and a divider with channel selection and $\Sigma\Delta$ modulator.

Figure 6.3: A frequency synthesizer block diagram.

The relaxation oscillator is also implemented as an on-chip reference clock provider. The channel selection and $\Sigma\Delta$ modulator can switch each channel in the RF transceiver protocol requirements. If the electrical system uses different communication protocols, the channel frequency and bandwidth will also be different. For example, the 2.4-GHz Wi-Fi discussed, the 802.11 WLAN standards specify a bandwidth of 22 MHz and the channels are on a 5-MHz incremental step. In the future work, an electrical system based

on 2.4-GHz Wi-Fi and Bluetooth to communicate with several terminals surrounding a smart building will be created. The frequency synthesizer is also proposed to provide the frequency signals for the whole system.

References

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Appendix A

Temperature Effects in Semiconductors

There are some impact of temperature on the MOSFET. In the appendices, we only discuss some important parameters, mobility, threshold voltage and leakage current.

1. Mobility

The carrier mobility, μ ($\text{cm}^2/\text{V}\cdot\text{s}$), describes the drift velocity of a particle in an applied electric field. Under small to moderate electric fields, $\mu = v_d/\xi$, where v_d is the drift velocity, and ξ is the electric field. The mobility has very complex temperature dependence, depending on several parameters: phonon scattering, surface roughness scattering, bulk charge Coulombic scattering and interface charge Coulombic scattering. Each of these scattering parameters is related to the temperature of the material, and the effective transverse electric field in the channel, ξ_{eff} . Phonon scattering refers to the potential for an electron to be scattered by a lattice vibration. As temperature increases, lattice vibrations increase and the probability of an electron being scattered by the lattice increases; thus, high temperature mobilities are limited by phonon scattering, causing mobility to

decrease as temperature increases as shown in Figure A.1. Surface roughness scattering becomes dominant when high electric fields pull electrons closer to the Si/SiO₂ surface.

Figure A.1: Temperature dependence of electron and hole mobilities in Si.

2. Threshold Voltage

The MOSFET threshold voltage is given by:

$$V_T = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad (\text{A.1})$$

where $V_{FB} = \phi_{gs} - (Q_{ss}/C_{ox})$ is the flat band voltage, with the gate-substrate contact potential $\phi_{gs} = \phi_T \cdot \ln(N_A N_G / n_i^2)$, N_A and N_G are the substrate and gate doping concentrations respectively, Q_{ss} the surface charge density, and C_{ox} the oxide capacitance. γ is the body effect parameter. ϕ_F is the Fermi energy. n_i is the intrinsic carrier concentration of Si.

Of the parameters in equation (A.1), ϕ_{gs} and ϕ_F vary with temperature (each contains ϕ_T and n_i terms). The threshold voltage temperature dependence $\partial V_T/\partial T$ may be:

$$\frac{\partial V_T}{\partial T} = \frac{\partial \phi_{gs}}{\partial T} + 2 \frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} \quad (\text{A.2})$$

where the temperature dependencies of ϕ_{gs} and ϕ_F are:

$$\frac{\partial \phi_{gs}}{\partial T} = \frac{1}{T} \left(\phi_{gs} + \frac{E_{G0}}{q} + \frac{3kT}{q} \right) \quad (\text{A.3})$$

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T} \left[\phi_F - \left(\frac{E_{G0}}{2q} + \frac{3kT}{2q} \right) \right] \quad (\text{A.4})$$

From these equations, the threshold voltage in a MOSFET is commonly modeled to decrease linearity with increasing temperature. The curve is plotted in Figure A.2 over a range of oxide thickness d and dopant concentrations N_A .

Figure A.2: Threshold voltage temperature dependence versus dopant concentration with oxide thickness d .

3. Leakage Current

Subthreshold leakage current I_{sub} is exponentially dependent on temperature. A common rule of thumb is that leakage current doubles for every 10°C increase in temperature. When $V_{GS} = 0$, I_{sub} may be represented by the Shockley diode model:

$$I_{sub} = I_0(e^{\frac{V_{DS}}{e\phi_T}} - 1) \quad (\text{A.5})$$

$$I_0 = ATe^{-\frac{1.12}{2\phi_T}} \quad (\text{A.6})$$

where I_0 is the reverse saturation current, A is a constant, V_{DS} is the drain-source voltage, and $\phi_T = kT/q$. The temperature dependence of gate leakage current is almost same as the subthreshold leakage current.

Appendix B

Author's Publications

1. **Jiacheng Wang**, Wang Ling Goh, Xin Liu and Jun Zhou, “A 12.77-MHz 31 ppm/°C On-Chip RC Relaxation Oscillator with Digital Compensation Technique”, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 11, pp. 1816-1824, 2016.
2. **Jiacheng Wang** and Wang Ling Goh, “A Digital Phase-Locked Loop with Injection Locked Technique in 40-nm CMOS Process”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (submitted).
3. **Jiacheng Wang** and Wang Ling Goh, “A 13.5-MHz relaxation oscillator with $\pm 0.5\%$ temperature stability for RFID application”, IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2431-2434, 2016.
4. **Jiacheng Wang**, Wang Ling Goh, Xin Liu and Jun Zhou, “A 12.77-MHz on-chip relaxation oscillator with digital compensation for loop delay variation”, IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 169-172, 2015

5. **Jiacheng Wang**, Leong Hai Koh and Wang Ling Goh, "A 13.8-MHz RC oscillator with self-calibration for $\pm 0.4\%$ temperature stability from -55 to 125 $^{\circ}\text{C}$ ", IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 423-426, 2015.
6. **Jiacheng Wang** and Wang Ling Goh, "A 12.4-kHz On-chip RC Oscillator with Comparator Offset Cancellation for PVT Variation Tolerance", International Symposium on Integrated Circuits (ISIC), 2016.
7. Di Zhu, **Jiacheng Wang** and Liter Siek, "A close-loop time-mode temperature sensor with inaccuracy of -0.6 $^{\circ}\text{C}/0.5^{\circ}\text{C}$ from -40°C to 120°C ", IEEE International Symposium on Circuits and Systems (IS-CAS), pp. 942-945, 2016.
8. Di Zhu, **Jiacheng Wang** Chiang Liang Kok, Liter Siek and Yuanjing Zheng, "A new time-mode on-chip oscillator-based low power temperature sensor", IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 411-414, 2015.
9. Di Zhu, **Jiacheng Wang**, Liter Siek, Chiang Liang Kok and Yuanjing Zheng, "High accuracy time-mode duty-cycle-modulation-based temperature sensor for energy efficient system applications", International Symposium on Integrated Circuits (ISIC), pp. 400-403, 2014.