NANYANG
TECHNOLOGICAL
UNIVERSITY

**SOFT-SWITCHED DC-DC CONVERTERS FOR
PHEV CHARGER**

KANAMARLAPUDI VENKATA RAVI KISHORE

**INTERDISCIPLINARY GRADUATE SCHOOL
ENERGY RESEARCH INSTITUTE @ NTU (ERI@N)**

2017

SOFT-SWITCHED DC-DC CONVERTERS FOR PHEV CHARGER

**KANAMARLAPUDI VENKATA RAVI
KISHORE**

**Interdisciplinary Graduate School
Energy Research Institute @ NTU (ERI@N)**

**A thesis submitted to the Nanyang Technological
University in partial fulfilment of the requirement for
the degree of
Doctor of Philosophy**

2017

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

16th Aug. 2017

.....
Date

.....
Kanamarlapudi Venkata Ravi Kishore

Abstract

An efficient power conditioning system plays a significant role in the design of battery charging systems for plug-in hybrid electric vehicles (PHEVs). A typical PHEV battery charging system consists of two stages. The first stage is an ac-dc conversion stage which regulates the input power factor, input current total harmonic distortion and intermediate dc bus voltage. The second stage is a dc-dc conversion stage which regulates the output voltage and provides galvanic isolation between utility grid and PHEV battery pack. The research works presented in this thesis focus on the dc-dc conversion stage of a PHEV charger.

The phase-shift modulated (PSM) isolated full-bridge (FB) dc-dc converter topology is commonly preferred for the dc-dc stage. High efficiency, high power density, high reliability, and galvanic isolation are the main features of this topology. However, zero-voltage switching (ZVS) is not ensured for all switches at light-load conditions resulting in poor efficiency of the converter. Furthermore, high voltage spikes are present across output rectifier diodes due to voltage ringing on the secondary side. These voltage spikes are further intensified with the increase in series inductance or leakage inductance of the transformer, output filter inductance and switching frequency. In addition, the voltage spikes increase the electromagnetic interference (EMI) of the converter. Therefore, the motivation for the research work presented in this thesis is to address these drawbacks in order to obtain an improved performance for the dc-dc converter over the entire operating range.

Auxiliary circuits can be added to the FB converter for improving the ZVS range. Additionally, snubber circuits can minimize the voltage spikes. In this research work, two new gating techniques, namely asymmetrical pulse-width modulation (APWM) and trailing-edge pulse-width modulation (TEPWM) gating techniques and a passive auxiliary circuit assisted topology are proposed to improve the performance of the dc-dc conversion stage in a PHEV charger.

APWM/TEPWM gating techniques minimize the auxiliary inductance value by a factor close to 2 compared to PSM for zero-voltage and zero-current switching (ZVZCS) FB dc-dc converter with auxiliary inductor at both legs. An adaptive frequency control, namely asymmetrical duty cycle frequency control (ADFC) method is also proposed to further reduce the auxiliary inductance and improve the efficiency for the same converter.

Another research work presented in this thesis comprising a FB dc-dc converter with inductive and capacitive output filter topologies assisted by an auxiliary transformer and auxiliary inductor is proposed. The proposed converter topologies achieve ZVS for all switches over the entire battery charging range. The proposed converter topology with inductive output filter is employed with a diode clamping network on the primary side to minimize voltage spikes across output rectifier diodes. The proposed converter topology with capacitive output filter is operated as a current-driven rectifier to eliminate voltage spikes. These converter topologies can achieve higher efficiency with the proposed APWM technique compared to the conventional PSM technique.

In this thesis, the operation and steady-state analysis of each proposed converter topology are explained in detail. The design considerations for the circuit parameters are also given. The improved performance of the proposed gating techniques and converter topologies is validated with experimental results obtained from 100 kHz, 1.2 kW converter hardware prototypes.

Acknowledgements

I take this opportunity to thank several individuals who helped me in the preparation and completion of this study.

First of all, I wish to express my utmost gratitude to my supervisor, Associate Professor So Ping Lam, for giving me an opportunity to undertake the research works presented in this thesis. He has also given me the opportunity to involve in writing research proposals and to supervise undergraduate project works. His expertise in power systems and power electronics research, and hunger for learning motivates me to go an extra mile in pursuing research studies. His timely assistance in publishing several journals and conference papers is invaluable. He has always been my inspiration and role model as I overcome all the obstacles in the completion of this work. I would also like to thank my co-supervisor Associate Professor Chan Chi Chiu Julian and mentor Assistant Professor Tang Yi. Their professional attitude and support deserve special acknowledgment. I am deeply impressed by their serious attitude and enthusiasm towards academic research which will have a positive effect on my future research work and professional career.

I would like to thank Dr. Sivaneasan Balakrishnan, Dr. Nanda Kumar Kandasamy and Dr. Wang Benfei who are my fellows. As senior students, they generously share their experience on research and make a good example of a Ph.D. student for me. I would like to especially thank Naga Brahmendra for his technical support and guidance in building the initial hardware setup. Moreover, his suggestions help me to improve the quality of my research papers. I thank Dr. Wang Yu, Thomas John, Dr. Abhinava Chaitanya, Dr. Karthik Kandasamy, Dr. Roomi, Hossein, Kalpesh, Sandeep, Srinivas, Dr. Swami Naidu, Dr. Nagesh, Ujjal and Yeap for the in-depth

and fruitful discussions on the research work. I would also like to thank my dearest friends Nagendra, Karthik, Solomon, Mukesh, Ravi Teja, Jhansi, Harish, Jeswanth, Sushant, Dr. Dhiraj, Dr. Sumit, Dr. Sumedh, Dr. Nishanth, Dr. Kushal and Balu for their invaluable kindness, unconditional help and moral support.

Furthermore, I am thankful to Associate Professor Gooi Hoay Beng for giving me an opportunity to work with Energy Research Institute @ NTU (ERIAN) before starting my Ph.D. study. I am grateful to ERIAN, Interdisciplinary Graduate School, Nanyang Technological University for providing me an opportunity to continue research and pursue my graduate study with a research scholarship. I am also thankful for the technical support provided by the laboratory staff Chia-Nge Tak Heng, Foo Mong Keow Thomas and Lin Zhi Ren at Clean Energy Research Laboratory. I especially thank Ms. Lily Lim Seok Kim at ERIAN for her administrative support.

Last but not least, I am delighted to express my deepest appreciation to my family members for believing in me, accepting my decisions and encouraging me to achieve my dreams. I specially appreciate my brother Mr. Kiran Kumar for taking few family responsibilities away from me and supporting me when in need.

Table of Contents

Abstract	i
Acknowledgements	iii
Table of Contents	v
Table Captions.....	ix
Figure Captions	xi
Nomenclature	xix
Abbreviations	xxv
Chapter 1	1
Introduction.....	1
1.1 Background and Motivations	2
1.1.1 Background	2
1.1.2 Motivations	6
1.2 Objectives and Scope	11
1.3 Contributions of Thesis	12
1.4 Organization of Thesis	13
References.....	16
Chapter 2	19
Literature Review.....	19
2.1 Gating Techniques and Adaptive Control Methods	20
2.2 Soft-Switched Full-Bridge DC-DC Converters for Battery Charging	23
2.2.1 Resonant Full-Bridge DC-DC Converters	25
2.2.2 Active Auxiliary Circuit Assisted Full-Bridge DC-DC Converters	31
2.2.3 Passive Auxiliary Circuit Assisted Full-Bridge DC-DC Converters.....	33

2.3	Methods to Suppress Voltage Spikes in Full-Bridge Converters	35
2.3.1	RCD Snubber	36
2.3.2	Diode Clamp Snubber	37
2.3.3	Active Clamp Snubber	38
2.3.4	Energy Recovery Clamp Snubber	38
2.3.5	Current-fed Full-Bridge Converters	40
	References	41
	Chapter 3*	61
	ADFC Full-Bridge DC-DC Converter for PHEV Battery Charging with Reduced Auxiliary Magnetics Requirement	61
3.1	ADFC ZVZCS Full-Bridge DC-DC Converter	62
3.1.1	Asymmetrical Duty Cycle Frequency Control	64
3.2	Steady-state Analysis of Auxiliary Circuit	65
3.3	Circuit Parameters Design	68
3.3.1	Transformer Turns Ratio	68
3.3.2	Series Inductor	69
3.3.3	Auxiliary Inductors	69
3.3.4	Auxiliary Capacitors	72
3.3.5	Output Filter Capacitor	72
3.4	Loss Analysis of Converter	73
3.4.1	MOSFETs Switching Losses	73
3.4.2	MOSFETs Conduction Losses	73
3.4.3	Gate Driver Losses	76

3.4.4	Rectifier Diodes Switching and Conduction Losses	76
3.4.5	Transformer and Series Inductor Core and Winding Losses.....	77
3.4.6	Auxiliary Inductors Core and Winding Losses	78
3.4.6	Loss Analysis Results.....	78
3.5	Experimental Results	82
3.5.1	APWM ZVZCS Full-Bridge DC-DC Converter.....	82
3.5.2	ADFC ZVZCS Full-Bridge DC-DC Converter	90
3.5.3	Comparative Analysis	97
3.6	Conclusion.....	100
	References	100
	Chapter 4*	103
	APWM ZVS Full-Bridge DC-DC Converter for PHEV Battery Charging	103
4.1	APWM ZVS Full-Bridge DC-DC Converter Topology	104
4.2	Operating Principle of Converter	105
4.3	Steady-state Analysis of Auxiliary Circuit.....	118
4.4	Experimental Results	122
4.5	Conclusion.....	131
	References.....	132
	Chapter 5*	133
	APWM ZVZCS Full-Bridge DC-DC Converter for PHEV Battery Charging.....	133
5.1	APWM ZVZCS Full-Bridge DC-DC Converter Topology	134
5.2	Operation Principle of Converter	135
5.3	Steady-state Analysis of Converter	150

5.3.1	Voltage Gain Analysis	150
5.3.2	Auxiliary Circuit Voltage and Current	151
5.3.3	Soft-switching Analysis	151
5.3.4	Features of Proposed APWM Converter.....	153
5.4	Circuit Parameters Design.....	156
5.4.1	Transformer Turns Ratio	156
5.4.2	Series Inductor	156
5.4.3	Auxiliary Inductor	156
5.4.4	Auxiliary Capacitors	157
5.4.5	Output Filter Capacitor	158
5.5	Magnetics Design.....	159
5.6	Experimental Results	164
5.6	Conclusion.....	174
	References	175
	Chapter 6	179
	Conclusions and Future Works	179
6.1	Conclusions	180
6.2	Future Works	184
	List of Publications	185
	Appendix.....	187
1.	Small-Signal Analysis of ZVS FB DC-DC Converter	187
2.	Small-Signal Analysis of ZVZCS FB DC-DC Converter	191
3.	Control Block Diagram of ZVZCS Converter.....	195

Table Captions

Table 1.1	Modeled charging scenarios [2]	3
Table 2.1	Comparison of resonant converters [52]	31
Table 3.1	Design specifications of the ADFC converter	67
Table 3.2	Load points in Li-ion battery charging profile.....	68
Table 3.3	Optimal switching frequency details for converter.....	78
Table 3.4	Component list of ADFC converter	81
Table 3.5	Efficiency comparison of converter with PSM, APWM and ADFC	99
Table 3.6	Comparison of FB dc-dc converters	99
Table 4.1	Design specifications of APWM ZVS converter	121
Table 4.2	Main load points in Lithium-ion battery charging profile	121
Table 4.3	Component list of APWM ZVS converter.....	121
Table 4.4	Efficiency comparison of converter with PSM and APWM.....	131
Table 5.1	Design specifications of APWM ZVZCS converter.....	149
Table 5.2	Key load points in Li-ion battery charging profile	149
Table 5.3	Critical parameters of magnetic components.....	160
Table 5.4	Component list of APWM ZVZCS converter	163
Table 5.5	Efficiency comparison of converter in with PSM and APWM	172
Table 5.6	Comparison of converters	173
Table 6.1	Comparison of the proposed dc-dc converters.....	177

Figure Captions

Figure 1.1	Global greenhouse gas emissions by economic sector [1].	2
Figure 1.2	Modeled grid profiles representing varying levels of carbon intensity [2].	3
Figure 1.3	Emission comparison on a low carbon grid [2].	4
Figure 1.4	Emission comparison on a high carbon grid [2].	4
Figure 1.5	Powertrain block diagram of series PHEV and EV [12].	5
Figure 1.6	Block diagram of on-board two-stage battery charger.	7
Figure 1.7	Turn-on and turn-off transition of hard-switched converter [21].	8
Figure 1.8	Zero-voltage switching [26].	9
Figure 1.9	Zero-current switching [26].	9
Figure 1.10	Isolated FB dc-dc converter [15].	11
Figure 2.1	Basic PWM strategy [2].	20
Figure 2.2	Asymmetrical duty cycle control method [4].	21
Figure 2.3	Phase-shift modulation method [2].	21
Figure 2.4	FB converter with a simple passive auxiliary circuit.	22
Figure 2.5	CC-CV charging strategy [36].	23
Figure 2.6	Series resonant FB dc-dc converter [48].	26
Figure 2.7	Parallel resonant FB dc-dc converter [55].	27
Figure 2.8	LCC series-parallel resonant FB dc-dc converter [57].	28
Figure 2.9	LLC series-parallel resonant FB dc-dc converter with inductive output filter [60].	29
Figure 2.10	LLC series-parallel resonant FB dc-dc converter with capacitive output filter [62].	30
Figure 2.11	FB converter with a simple active auxiliary circuit [76].	31
Figure 2.12	FB converter with a passive auxiliary circuit on both legs [96].	33
Figure 2.13	FB converter with adaptive passive auxiliary circuit [110].	34

Figure 2.14	FB converter with RCD snubber [115].	36
Figure 2.15	FB converter with diode clamp snubber [121].	37
Figure 2.16	FB converter with active clamp snubber on secondary side [122].	38
Figure 2.17	FB converter with energy recovery clamp snubber on secondary side [126].	39
Figure 2.18	Current-fed FB converter with capacitive output filter [23].	40
Figure 3.1	ZVZCS FB dc-dc converter with auxiliary inductor at both legs [1].	62
Figure 3.2	Theoretical operational waveforms of the auxiliary circuit with APWM.	62
Figure 3.3	Theoretical operational waveforms of the auxiliary circuit with TEPWM.	63
Figure 3.4	Comparison of voltage across auxiliary capacitors with APWM/ADFC and PSM.	66
Figure 3.5	Comparison of peak value of auxiliary inductor's current with APWM and PSM under variable switching frequency.	67
Figure 3.6	Lithium-ion battery charging profile.	68
Figure 3.7	Load points versus V_{C2} at different auxiliary inductance values with APWM.	70
Figure 3.8	Load points versus V_{C2} at different auxiliary inductance values with ADFC.	70
Figure 3.9	Key steady-state operating waveforms for loss analysis of the converter.	74
Figure 3.10	Flux density waveforms. (a) Transformer. (b) Auxiliary inductor.	77
Figure 3.11	Peak value of auxiliary inductor's current with ADFC, APWM and PSM.	79
Figure 3.12	Comparison of converter power losses with PSM, APWM and ADFC. (a) CC mode. (b) CV mode.	81

Figure 3.13	Prototype of ZVZCS FB dc-dc converter with auxiliary inductor at both legs.	81
Figure 3.14	ZVS waveforms of S_3 with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	83
Figure 3.15	ZVS waveforms of S_4 with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	84
Figure 3.16	Operating waveforms of T_r primary with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	85
Figure 3.17	Operating waveforms of T_r secondary with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).	86
Figure 3.18	Auxiliary circuit waveforms with PSM ($L_a = 60\mu\text{H}$). (a) Auxiliary capacitor voltages. (b) Auxiliary inductors voltage and current.	87
Figure 3.19	Auxiliary circuit waveforms with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	88
Figure 3.20	Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.....	89
Figure 3.21	ZVS waveforms of S_3 with ADFC. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	91
Figure 3.22	ZVS waveforms of S_4 with ADFC. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).....	92

Figure 3.23	Operating waveforms of T_r primary with ADFC. (a) At load point P_I (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{I0} (320V, 0.375A).....	94
Figure 3.24	Operating waveforms of T_r secondary with ADFC. (a) At load point P_I (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{I0} (320V, 0.375A).	95
Figure 3.25	Auxiliary circuit waveforms with PSM ($L_a = 125\mu\text{H}$). (a) Auxiliary capacitor voltages. (b) Auxiliary inductors voltage and current.	96
Figure 3.26	Auxiliary circuit waveforms with ADFC. (a) At load point P_I (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{I0} (320V, 0.375A).....	97
Figure 3.27	Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.....	98
Figure 4.1	Proposed APWM ZVS FB dc-dc converter. (a) Topology. (b) APWM gating technique.....	104
Figure 4.2	Theoretical operational waveforms of the converter with APWM.	106
Figure 4.3	Interval I.	107
Figure 4.4	Interval II.	108
Figure 4.5	Interval III.....	109
Figure 4.6	Interval IV.	110
Figure 4.7	Interval V.....	111
Figure 4.8	Interval VI.	112
Figure 4.9	Interval VII.	113
Figure 4.10	Interval VIII.....	113
Figure 4.11	Interval IX.	114
Figure 4.12	Interval X.....	115
Figure 4.13	Interval XI.	116
Figure 4.14	Interval XII.	116

Figure 4.15	Interval XIII.....	117
Figure 4.16	Interval XIV.....	118
Figure 4.17	Auxiliary inductor voltage and current waveforms. (a) PSM. (b) APWM.	119
Figure 4.18	Comparison of voltage across auxiliary capacitors and peak current through auxiliary inductor with PSM and APWM.	119
Figure 4.19	Lithium-ion battery charging profile.	121
Figure 4.20	APWM ZVS FB dc-dc converter prototype.	122
Figure 4.21	ZVS waveforms of S_3 with APWM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	123
Figure 4.22	ZVS waveforms of S_4 with APWM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	124
Figure 4.23	T_r primary and secondary results without clamp diodes. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	125
Figure 4.24	T_r primary and secondary results with clamp diodes. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	126
Figure 4.25	Auxiliary circuit waveforms with APWM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	127
Figure 4.26	Auxiliary circuit waveforms with PSM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).	128
Figure 4.27	Comparison of peak auxiliary inductor current with APWM and PSM over battery charging profile.....	129
Figure 4.28	Comparison of total switch's current stress with APWM and PSM over battery charging profile.....	130

Figure 4.29	Efficiency of the converter with APWM and PSM over battery charging profile	130
Figure 5.1	Proposed APWM ZVZCS full-bridge dc-dc converter.	134
Figure 5.2	Key operational waveforms of the proposed converter.	136
Figure 5.3	Theoretical operational waveforms of converter when $D < D_{boundary}$	137
Figure 5.4	Interval I.	138
Figure 5.5	Interval II. (a) Heavy-load. (b) Light-load.	140
Figure 5.6	Interval III. (a) Heavy-load. (b) Light-load.	142
Figure 5.7	Interval IV. (a) Heavy-load. (b) Light-load.	144
Figure 5.8	Interval V. (a) Heavy-load. (b) Light-load.	146
Figure 5.9	Interval VI.	148
Figure 5.10	Lithium-ion battery charging profile.	149
Figure 5.11	Voltage gain characteristics of the converter.	150
Figure 5.12	ZVS range of low-side switches over battery charging profile.	152
Figure 5.13	Comparison of ZVS currents with APWM and PSM operated converter.....	155
Figure 5.14	Load versus V_{C2} for different values of L_a	157
Figure 5.15	Voltage, current and flux density waveforms of L_a	159
Figure 5.16	(a) Proposed APWM ZVZCS converter prototype. (b) Experimental setup of the system.	164
Figure 5.17	ZVS waveforms for high-side switch S_3 . (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At re-charge point....	166
Figure 5.18	ZVS waveforms for low-side switch S_4 . (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At re-charge point....	167
Figure 5.19	T_r secondary operating waveforms. (a) At transition point. (b) At end point.	168

Figure 5.20	Auxiliary circuit waveforms with APWM. (a) At transition point. (b) At end point.....	169
Figure 5.21	Auxiliary circuit waveforms with PSM. (a) At transition point. (b) At end point.....	169
Figure 5.22	Comparison of peak current of auxiliary inductor with APWM and PSM over battery charging profile.....	170
Figure 5.23	Comparison of ZVS switch's current with APWM and PSM over battery charging profile.....	170
Figure 5.24	Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.....	171

Nomenclature

A_{ce_Lse}	Effective Cross-sectional Area of Inductor L_{se} Core
A_{ce_Tr}	Effective Cross-sectional Area of Transformer T_r Core
A_e	Effective Magnetic Cross-section Area
A_w	Core Window Area
B_{La}	Flux Density of Inductor L_a
B_{sat}	Saturation Flux Density at $25^\circ C$
C_1-C_4	Body and Snubber Capacitance across S_1-S_4
$C_{a1}-C_{a4}$	Auxiliary Capacitances
C_{as1}, C_{as2}	Body and Snubber Capacitance across S_{a1}, S_{a2}
C_f	Output Filter Capacitance
C_g	Gate Capacitor
C_{sb}	Snubber Circuit Capacitance
D	Duty Cycle
D_1-D_4	Output Rectifier Diodes
D_{a1}, D_{a2}	Clamping Diodes on Primary Side of Transformer
D_{as1}, D_{as2}	Anti-parallel Body-diodes of S_{a1}, S_{a2}
D_{max}	Maximum Duty Cycle
$D_{S1}-D_{S4}$	Anti-parallel Body-diodes of S_1-S_4
D_{sb}	Snubber Circuit Diode
D_{sb1}, D_{sb2}	Clamping Diodes on Secondary Side of Transformer T_r
f_{smax}	Maximum Switching Frequency
f_{smin}	Minimum Switching Frequency
f_{sopt}	Optimal switching frequency
$G_{S1}-G_{S4}$	Gating Signals to S_1-S_4 respectively
i_{DS1}, i_{DS2}	Current through Body-diodes of S_1, S_2
i_{La}	Current through Inductor L_a

i_{La1}, i_{La2}	Current through Inductors L_{a1}, L_{a2}
I_{La1P}	Peak Current Value of Auxiliary Inductor L_{a1}
I_{La2P}	Peak Current Value of Auxiliary Inductor L_{a2}
I_{LaP}	Peak Current Value of Auxiliary Inductor L_a
I_{LaRMS}	RMS Current through Inductor L_a
I_o	Output Current
i_p	Transformer T_r Primary Current
I_{pP}	Peak Current Value of Main Transformer T_r Primary
i_{S1}, i_{S2}	Current through Main Switches
$I_{S1,S4-ZVS-APWM}$	Current during ZVS Transition of S_1, S_4 with APWM
$I_{S1,S4-ZVS-PSM}$	Current during ZVS Transition of S_1, S_4 with PSM
$I_{S2,S3-ZVS-APWM}$	Current during ZVS Transition of S_2, S_3 with APWM
$I_{S2,S3-ZVS-PSM}$	Current during ZVS Transition of S_2, S_3 with PSM
i_{sec}	Transformer T_r Secondary Current
I_{sw}	Current through MOSFET
i_{SW3}	Current through MOSFET Switch SW_3
i_{SW4}	Current through MOSFET Switch SW_4
I_{SWrms}	Total MOSFETs RMS Current Stress
K_c	Core Loss Coefficient
$K_{electrical}$	Core Electrical Constant
K_{fe}	Core Loss Geometrical Coefficient
$K_{geometry}$	Core Geometrical Constant
K_i	Core Material Parameter
K_u	Winding Fill Factor
L_a	Auxiliary Inductance
l_e	Effective Magnetic Path Length
L_f	Filter Inductance
l_g	Air Gap Length

L_{lk}	Leakage inductance of Transformer T_r
L_{se}	Series Inductance and Leakage inductance of T_r
MLT	Mean Length per Turn
n	Transformer Turns-ratio
N	Number of Turns
N_{La}	Number of Turns for Inductor L_a
N_{Lse}	Number of Turns for Inductor L_{se}
P_1-P_{10}	Load Points in Battery Charging Profile
P_{cu_La}	Copper Winding Loss in Inductor L_a
P_{cu_Lse}	Copper Winding Loss in Inductor L_{se}
P_{cu_Tr}	Copper Winding Loss in Transformer T_r
$P_{D1, D2, D3, D4_cond}$	Output Rectifier Diodes Conduction loss in D_1-D_4
$P_{DS1, DS3_cond}$	Body-diodes Conduction Loss in DS_1, DS_3
$P_{DS2, DS4_cond}$	Body-diodes Conduction Loss in DS_2, DS_4
P_{fe}	Relative Core Losses
P_{MOS_cond}	Total MOSFET's Conduction Losses
$P_{MOS_High-side_cond}$	High-side MOSFET's Conduction Losses
$P_{MOS_Low-side_cond}$	Low-side MOSFET's Conduction Losses
P_o	Output Power
P_{omax}	Maximum Output Power
$P_{S1, S3_cond}$	Conduction Loss in S_1, S_3
$P_{S1, S3_off}$	Turn-off Switching Loss in S_1, S_3
$P_{S2, S4_cond}$	Conduction Loss in S_2, S_4
$P_{S2, S4_off}$	Turn-off Switching Loss in S_2, S_4
P_{sw}	Total Switching Losses
P_{sw-off}	Turn-off Switching Loss
P_{sw-on}	Turn-on Switching Loss
P_v_La	Volumetric Core Losses of Inductor L_a

$P_{V_Tr,Lse}$	Volumetric Core Losses of T_r , Inductor L_{se}
Q_{gtot}	Total Gate Charge of MOSFET
R	Winding Resistance
$R_{ds(on)}$	On-state Drain-Source Resistance of MOSFET
R_{ebat}	Battery Charging Equivalent Load
R_{La}	Resistance of Inductor L_a Winding
R_{Lse}	Resistance of Inductor L_{se} Winding
R_{pri}	Resistance of Transformer T_r Primary Winding
R_{sb}	Snubber Circuit Resistance
R_{sec}	Resistance of Transformer T_r Secondary Winding
S_1-S_4	Main Switches
S_{a1}, S_{a2}	Auxiliary Circuit Switches
S_{sb}	Snubber Circuit Switch
SW_1-SW_4	MOSFET Switches $((S_1-S_4) + (D_{S1}-D_{S4}) + (C_1-C_4))$
T_a	High Frequency Auxiliary Transformer
t_d	Dead-time between Gating Signals
t_f	Voltage Fall-time of MOSFET
T_r	High Frequency Power Transformer
T_s	Switching Period
V_{AB}	Inverter Output Voltage
$V_{C1}-V_{C4}$	Voltage across Switches S_1-S_4
$V_{ca1}-V_{ca4}$	Voltage across Auxiliary Capacitors $C_{a1}-C_{a4}$
V_{D1}	Voltage across Output Rectifier Diode D_1
V_{dr}	MOSFET Gate Drive Voltage
V_{DS}	Drain-Source Voltage of MOSFET
V_{DS3}, V_{DS4}	Drain-Source Voltage of MOSFET Switches SW_3, SW_4
V_e	Effective Magnetic Core Volume
V_F	Forward Voltage of Rectifier Diode

V_{GS}	Gate Supply Voltage
V_{in}	Input DC Voltage
V_{La}	Voltage across Inductor L_a
v_{Tap}	Auxiliary Transformer Primary Voltage
V_{La}^{+}	Positive Half-cycle Voltage across Inductor L_a
V_{La1}	Voltage across Inductor L_{a1}
V_{La1}^{-}	Negative Half-cycle Voltage across Inductor L_{a1}
v_{La1}, v_{La2}	Voltage across Inductors L_{a1}, L_{a2}
V_{La1}^{+}	Positive Half-cycle Voltage across Inductor L_{a1}
V_{La2}^{+}	Positive Half-cycle Voltage across Inductor L_{a2}
V_{La2}^{-}	Negative Half-cycle Voltage across Inductor L_{a2}
V_o	Output Voltage
V_{omax}	Maximum Output DC Voltage
V_{pri}	Voltage across Transformer T_r Primary
V_{sec}	Voltage across Transformer T_r Secondary
v_{Tas}	Auxiliary Transformer Secondary Voltage
W_a	Litz Wire Area
α, β	Core Material Constants
α_{ZVL}	ZVS Range Coefficient without Auxiliary Circuit
α_{ZVLA}	ZVS Range Coefficient with Auxiliary Circuit
λ	Voltage-Second Product
ΔB	Flux Density Ripple
ΔB_{La}	Peak to Peak flux-density of Inductor L_a
ΔB_{Lse}	Peak Flux Density of Inductor L_{se}
ΔB_{Tr}	Peak Flux Density of Transformer T_r
ΔV_{ca}	Ripple Voltage Limit of Capacitor C_a
ΔV_{cf}	Ripple Voltage Limit of Capacitor C_f

Abbreviations

AC, ac	Alternating Current
ADFC	Asymmetrical Duty cycle Frequency Control
APWM	Asymmetrical Pulse Width Modulation
AWG	American Wire Gauge
CC	Constant Current
CEV	Combustion Engine Vehicle
CV	Constant Voltage
DC, dc	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electro Magnetic Interference
EV	Electric Vehicle
FB	Full-Bridge
IGBT	Insulated Gate Bipolar Transistor
iGSE	Improved General Steinmetz Equation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NREL	National Renewable Energy Laboratory
PFC	Power Factor Corrector
PHEV	Plug-in Hybrid Electric Vehicle
PRC	Parallel Resonant Converter
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RCD	Resistor-Capacitor-Diode
RMS	Root Mean Square
SAE	Society of Automotive Engineers
SOC	State Of Charge
SPRC	Series Parallel Resonant Converter

SRC	Series Resonant Converter
TEPWM	Trailing-Edge Pulse Width Modulation
THD	Total Harmonic Distortion
ZCS	Zero-Current Switching
ZEV	Zero Emission Vehicle
ZVS	Zero-Voltage Switching
ZVZCS	Zero-Voltage Zero-Current Switching

Chapter 1

Introduction

Motivated by the reduction in carbon emissions and air pollution as well as the rise of fuel price, zero emission vehicles (ZEVs) are being penetrated into the transportation sector. This chapter presents the background of this research work, which includes the developments, advantages and challenges of the plug-in hybrid electric vehicle (PHEV) or electric vehicle (EV) charger. In particular, the research work presented in this thesis aim to analyze, design and implement high performance dc-dc converters for PHEV/EV charger. In addition, the research contributions and organization of the thesis are also presented in this chapter.

1.1 Background and Motivations

1.1.1 Background

Nowadays, there is growing awareness around the world that the availability of fossil fuel resources is limited and the world energy consumption is expected to rise. At the same time, environmental issues related to the greenhouse gases emissions such as carbon dioxide, methane, nitrous oxide and fluorinated gases have increased significantly. The global greenhouse gas emissions by economic sector are shown in Figure 1.1. It indicates that the transportation sector contributes about 14% of global greenhouse gas emissions [1]. Zero emission vehicles (ZEVs) such as series plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs) offer the advantage of lesser dependency on fossil fuels and significant reduction in vehicle carbon emissions.

Figure 1.1 Global greenhouse gas emissions by economic sector [1].

A research study was conducted by the National Renewable Energy Laboratory (NREL), USA on the amount of emissions associated with PHEV/EV charging considering the impact of electricity generation mix, charging infrastructure availability, and vehicle type [2].

Figure 1.2 Modeled grid profiles representing varying levels of carbon intensity [2].

Table 1.1 Modeled charging scenarios [2]

Scenario	Charging place	Time of charging	Charging level
Home L1 (H1)	At home	Anytime	Level 1
Home L2 (H2)	At home	Anytime	Level 2
Time restricted (TR)	At home	12 A.M. – 1 P.M.	Level 2
Workplace (WP)	At home and work	Anytime	Level 2

This study used five grid generation profiles with varying levels of carbon intensity and hourly generation profiles as shown in Figure 1.2 [2]. Low carbon grid is composed largely of renewable energy or a grid with emissions-free generation sources. The modeled PHEV/EV charging scenarios represent a variety of situations as listed in Table 1.1 [2]. The first two charging scenarios, home L1 (H1) and home L2 (H2) represent opportunistic charging where the driver can use Level 1 or Level 2 charger at home whenever needed.

Figure 1.3 Emission comparison on a low carbon grid [2].

Figure 1.4 Emission comparison on a high carbon grid [2].

The third scenario, time restricted (TR) charging represents the incentives offered to ZEV owners during off-peak hours. The last scenario, workplace (WP) charging represents the vehicle that can use Level 2 charger at home/workplace during anytime. The comparisons of total emissions from EVs and PHEVs to those generated when only combustion engine vehicle (CEV) is used to take the same set of trips are shown in Figures 1.3 and 1.4 [2]. In the case of low carbon grid, EVs and PHEVs result in about one-third of the total emissions of a CEV as shown in Figure 1.3. In the case of high carbon grid, EVs and PHEVs result in slightly lower emissions than a CEV as shown in Figure 1.4. These results indicate that the transformation of CEV to ZEV contributes to a cleaner environment. Also, ZEVs can achieve higher powertrain energy conversion efficiency, regeneration capability, and less acoustic and vibration, as compared to CEVs. Therefore, ZEV technology has been an attractive research area in the past decade for automotive manufacturers as well as for academic researchers [3]-[9]. High performance power conditioning systems play a vital role in the development of ZEVs [10], [11]. The powertrain block diagram of such vehicles is shown in Figure 1.5 [12].

Figure 1.5 Powertrain block diagram of series PHEV and EV [12].

1.1.2 Motivations

Series PHEVs/EVs use a high voltage, and high energy density rechargeable battery pack for powering the traction motor drive system. This battery pack is typically recharged from the utility grid using a battery charger. Therefore, the development of high efficiency battery charger is one of the key components to allow PHEVs/EVs to succeed in the automotive market.

1.1.2.1 Battery Chargers

Society of Automotive Engineers (SAE) classified the battery chargers into two categories: with different electrical standard levels [13].

On-board AC chargers: The power conditioning system for the battery charger is integrated into the vehicle. The on-board conductive coupled chargers use AC Level 1 and AC Level 2 charging power levels in accordance with SAE J1772 standard [13]. AC Level 1 is defined as single-phase 120V AC and 16A with a maximum charging power of 1.92 kW, and AC Level 2 is defined as single-phase 208V-240V AC and 80A with a maximum charging power limit of 19.2 kW.

The on-board inductive coupled chargers use AC Level 1, AC Level 2 and AC Level 3 charging power levels in accordance with SAE J1773 standard [14]. Inductive coupled chargers are operated with high-frequency magnetic power link ranging from 130 kHz to 360 kHz. AC Level 1, AC Level 2, and AC Level 3 have maximum charging power limits 3.6 kW, 19.2 kW and 150 kW respectively.

Off-board DC chargers: The power conditioning system for the battery charger is placed in a public charging station. The off-board conductive coupled chargers use DC Level 1 and DC Level 2 charging power levels in accordance with SAE J1772

standard [13]. DC Level 1 is defined as 200V-500V and 80A with a maximum charging power of 40 kW, and DC Level 2 is defined as 200V-500V and 200A with a maximum charging power of 100 kW.

Figure 1.6 Block diagram of on-board two-stage battery charger.

Most of the EV users prefer to recharge the high-voltage battery pack using the on-board charger overnight at home [10]. The typical block diagram of a two-stage power conditioning system for the on-board EV battery charger is shown in Figure 1.6 [10]. One of the main advantages of this two-stage approach is that the low-frequency ac ripple can be easily rejected by the second stage, which is very favorable for charging lithium-ion batteries.

The two stages are: (i) Front-end ac-dc power conversion stage – which regulates the input power factor, input current THD, and intermediate dc bus voltage. (ii) dc-dc conversion stage – which regulates the output voltage and current as required by the battery charging algorithm. It also provides galvanic isolation between utility grid and battery pack [15]-[17]. Galvanic isolation is necessary to comply with the UL-2202 and UL-2231 safety standards of EV charging system [18]-[20]. The implementation of high-frequency transformer isolation gives the advantage of small size, i.e., high power density. As a result, the power switches have to be operated at high frequency. The high frequency operated dc-dc converters are classified into hard-switched converters and soft-switched converters which are discussed in the following section.

1.1.2.2 Hard-switched Converter

Figure 1.7 Turn-on and turn-off transition of hard-switched converter [21].

Typical waveforms during turn-on and turn-off transitions of a semiconductor switch in a hard-switched converter are shown in Figure 1.7 [21]. The simultaneous presence of drain-source voltage V_{DS} and current through the switch I_{SW} during turn-on and turn-off transitions results in power loss P_{sw} given by

$$P_{sw-on} = \frac{V_{in} I_p t_{on} f_s}{2} \quad (1.1)$$

$$P_{sw-off} = \frac{V_{in} I_p t_{off} f_s}{2} \quad (1.2)$$

$$P_{sw} = P_{sw-on} + P_{sw-off} \quad (1.3)$$

Thus, a hard-switched converter requires a large heat sink to dissipate the generated switching losses. In addition, the switching frequency f_s range has to be limited for better efficiency as the switching losses are proportional to f_s . However at lower switching frequency operation, the size of magnetics and capacitors become larger, i.e., low power density for converter. Moreover, additional lossy RC snubber circuits are required to minimize voltage surge dv/dt and current surge di/dt . Also, electromagnetic interference is higher in hard-switched converters. The switching losses in hard-switched converters are minimized using soft-switching techniques which are discussed in the following section.

1.1.2.3 Soft-switched Converter

Figure 1.8 Zero-voltage switching [26].

Figure 1.9 Zero-current switching [26].

From (1.1)-(1.3), turn-on and turn-off losses of MOSFET/IGBT increase with switching frequency. These losses can be minimized by using soft-switching techniques without reducing the switching frequency. Zero-voltage switching (ZVS) and zero-current switching (ZCS) are two popular soft-switching techniques which eliminate the turn-on loss and turn-off loss respectively [21]-[26]. Converters that operate based on these principles are called soft-switched converters.

In ZVS, the voltage across the switch drops to zero before the gating signal is applied, thus eliminating the turn-on loss in MOSFET/IGBT. The turn-off loss can be minimized by adding a capacitor across the switch which limits the rate of rise of the voltage across the switch so that the device current falls to zero before the voltage across the switch rises to maximum (i.e., input voltage). The corresponding ZVS transition and switching trajectory for a MOSFET are shown in Figure 1.8.

In ZCS, the current through the switch reaches to zero before the gating signal is removed, thus eliminating the turn-off loss in MOSFET/IGBT. The turn-on loss

can be minimized by adding an inductor in series with the switch which limits the rate of rise of current through the switch so that the device voltage falls to zero before the current through the switch rises to maximum (equivalent to load current). The corresponding ZCS transition and switching trajectory for a MOSFET are shown in Figure 1.9. The other advantages of soft-switching techniques in dc-dc converters include the high switching frequency operation, high power density, lower dv/dt and di/dt stresses, and reduced electromagnetic interference (EMI).

In battery charging applications, ZVS is more important compared to ZCS as the converter has to be operated with a higher dc link voltage. The following are the requirements for designing a dc-dc converter for high-voltage battery charging application:

- a) Galvanic isolation between battery charger and utility grid;
- b) Wide output voltage and output current regulation according to battery charging profile;
- c) Soft-switching for all active switches on primary side throughout the converter operating range;
- d) Low voltage rating for secondary rectifier diodes;
- e) Minimal circulating current and losses;
- f) Narrow switching frequency variation to minimize switching and conduction losses.

The phase-shifted full-bridge (FB) isolated dc-dc converter shown in Figure 1.10 is a commonly preferred topology for the dc-dc power conversion stage in EV battery charger [15], [16]. However, it has the following drawbacks: a) ZVS for active switches in a narrow load range, b) high circulating current during the freewheeling period, c) duty-cycle loss, d) high voltage spikes across the output rectifier diodes, and e) the associated EMI. These drawbacks have to be addressed properly for the EV battery charging applications to meet the above-mentioned requirements ensuring satisfactory performance of the converter over its operating range.

Therefore, the motivation for this thesis is to analyze, design and implement high performance dc-dc converters which satisfy these requirements.

Figure 1.10 Isolated FB dc-dc converter [15].

1.2 Objectives and Scope

The objectives of the research work are listed as follows:

- i) Implementation of new gating techniques and control methods for improving the performance of the converters.
- ii) Theoretical operational analysis of new dc-dc converter topologies which meet the following goals.
 - a) Achieve ZVS for all active switches throughout the battery charging range.
 - b) Minimize the voltage stress on secondary rectifier diodes.
 - c) Reduce circulating losses during freewheeling periods.
- iii) Development of design considerations for main components of the converter and experimental prototype.
- iv) Validation of theoretical analysis using experimental results.

1.3 Contributions of Thesis

The main contributions of this thesis are summarized as follows:

1. Two new gating techniques called asymmetrical pulse-width modulation (APWM) and trailing-edge pulse width modulation (TEPWM) are proposed for the passive auxiliary circuit assisted FB dc-dc converters. The adoption of the proposed gating techniques reduces the required auxiliary inductance of auxiliary circuit compared to the conventional phase-shift modulation (PSM) technique.
2. The auxiliary inductance required in zero-voltage zero-current switching (ZVZCS) FB dc-dc converter with auxiliary inductors at both legs [27] is reduced by a factor close to 2 when operated with the proposed APWM/TEPWM compared to PSM. An adaptive frequency control called asymmetrical duty cycle frequency control (ADFC) method is also proposed to further improve the efficiency of the converter and to reduce the auxiliary inductance by a factor close to 2.3.
3. An auxiliary transformer and auxiliary inductor assisted FB dc-dc converter with inductive output filter topology is proposed. The proposed converter achieves ZVS for all switches on the primary side over the entire battery charging range. The converter is integrated with diode clamp network on the primary side to minimize the voltage spikes across output rectifier diodes. The proposed converter achieves higher efficiency when gated with the proposed APWM technique compared to PSM technique.
4. An auxiliary transformer and auxiliary inductor assisted FB dc-dc converter with capacitive output filter topology is proposed. The proposed converter achieves ZVS for all switches and near ZCS for two switches on the primary side

over the entire battery charging range. The converter is operated in discontinuous conduction mode to eliminate the voltage spikes across output rectifier diodes. The switching and conduction losses, and circulating losses are reduced with APWM compared to PSM. Also, the auxiliary inductance required to ensure ZVS with APWM is reduced compared to PSM by a factor close to 1.3.

5. The operation and steady-state analysis of each converter topology operated with APWM are explained in detail. Design considerations for the selection of the main component values are presented. Experimental converter prototypes are developed, and the results are presented to validate the theoretical analysis and design.

1.4 Organization of Thesis

The thesis is organized into six main chapters as follows:

Chapter 1: Introduction

This chapter provides background information about electric vehicles and battery chargers including their developments, applications, and challenges. The motivations, objectives, and contributions of this thesis, as well as the organization of this thesis, are also discussed.

Chapter 2: Literature Review

In this chapter, a comprehensive review of existing research works in the areas of (i) gating techniques and the corresponding features of FB dc-dc converter, (ii) resonant FB dc-dc converter topologies, (iii) active auxiliary circuit assisted FB dc-dc converter topologies, (iv) passive auxiliary circuit assisted FB dc-dc converter

topologies which extend the soft-switching range of active switches, and (v) different snubber circuits for minimizing or eliminating the voltage spikes across the output rectifier diodes is presented.

Chapter 3: ADFC Full-Bridge DC-DC Converter for PHEV Battery Charging with Reduced Auxiliary Magnetics Requirement

In this chapter, new gating techniques and adaptive frequency control to improve the efficiency of full-bridge dc-dc converter for battery charging in electric vehicles are presented. The conventional FB converter is assisted by a passive auxiliary circuit to extend the soft-switching range. The uncontrolled auxiliary circuit current with PSM increases the switching and conduction losses of the converter, whereas the proposed methods control the auxiliary circuit current and thus improve the overall efficiency of the converter. The steady-state analysis of the auxiliary circuit with the proposed gating techniques and control methods is presented. A comparative loss analysis with the proposed gating techniques and PSM gating technique is also given. A 100 kHz, 1.2 kW converter hardware prototype is developed. The experimental results are presented which validate the theoretical analysis of the converter with the proposed asymmetrical duty cycle frequency control (ADFC) method.

Chapter 4: APWM ZVS Full-Bridge DC-DC Converter for PHEV Battery Charging

A new ZVS full-bridge dc-dc converter for battery charging is proposed in this chapter. The main switches in the converter turn-on at zero-voltage over full-load range with the help of passive auxiliary circuit. The diode clamping circuit on the primary side eliminates the voltage spikes across the output rectifier diodes which are commonly present in the conventional FB dc-dc converters. The switches are

controlled with the APWM technique proposed in *Chapter 3* for improving the efficiency of the proposed converter. Use of APWM also reduces the current stress of the main switches and the circulating losses by minimizing the auxiliary reactive current over the operating range of the converter compared to the conventional PSM method. The steady-state analysis of the converter is explained in detail with time intervals, and the respective governing analytical equations are provided. A 100 kHz, 1.2 kW laboratory prototype is developed to validate the performance of the proposed converter. The advantage of APWM over PSM is also verified through the current stress results of the main switches at different loads for the proposed converter.

Chapter 5: APWM ZVZCS Full-Bridge DC-DC Converter for PHEV Battery Charging

In this chapter, a new ZVZCS full-bridge dc-dc converter is proposed to reduce the power conversion losses. The proposed converter incorporates APWM gating technique proposed in *Chapter 3* for the improved performance over battery charging load range. The proposed dc-dc converter topology achieves ZVS for all the switches and near ZCS for low-side switches throughout the charging range of the battery. Use of the proposed APWM technique reduces the switching and conduction losses compared to the PSM technique. The auxiliary inductance required to ensure ZVS with APWM can also be reduced compared to PSM. Analysis, design, and implementation of the proposed APWM ZVZCS FB dc-dc converter are discussed in this chapter. A 100 kHz, 1.2 kW laboratory prototype is developed, and the experimental results are presented. The results validate the analysis and performance of the proposed converter.

Chapter 6: Conclusions and Future Works

An overall conclusion of this research is discussed in this chapter. Further research directions are pointed out.

References

- [1] Climate Change 2014: Mitigation of Climate Change [Online]. Available: <https://www.ipcc.ch/report/ar5/wg3/>.
- [2] Emissions Associated with Electric Vehicle Charging: Impact of Electricity Generation Mix, Charging Infrastructure Availability, and Vehicle Type, National Renewable Energy Laboratory, USA, 2015 [Online]. Available: http://www.afdc.energy.gov/uploads/publication/ev_emissions_impact.pdf.
- [3] Understanding the Electric Vehicle Landscape to 2020 [Online]. Available: https://www.iea.org/publications/freepublications/publication/GlobalEVOutlook_2013.pdf.
- [4] The China New Energy Vehicles Program Challenges and Opportunities [Online]. Available: <http://siteresources.worldbank.org/>.
- [5] Electric Vehicle Pilot Program - U.S General Services Administration [Online]. Available: <https://www.gsa.gov/portal/content/281581>.
- [6] Electromobility in Germany: Vision 2020 and Beyond [Online]. Available: http://www.gtai.de/GTAI/Content/EN/Invest/_SharedDocs/Downloads/GTAI/Brochures/Industries/electromobility-in-germany-vision-2020-and-beyond-en.pdf.
- [7] Alternate fuels for surface transportation program, India [Online]. Available: <http://mnre.gov.in/schemes/new-technologies/transportation/>.

- [8] Electric Vehicles test-bed program, Singapore [Online]. Available: https://www.ema.gov.sg/Electric_Vehicles_Test_Bed.aspx.
- [9] Implementing Agreement – Hybrid Electric Vehicle program (IA-HEV) [Online]. Available: <http://www.ieahev.org/>.
- [10] M. Yilmaz and P. T. Krein, “Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles,” *IEEE Trans. Power Electronics*, vol. 28, no. 5, pp. 2151-2169, May 2013.
- [11] A. Emadi, Y. J. Lee, and K. Rajashekara, “Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles,” *IEEE Trans. Industrial Electronics*, vol. 55, no. 6, pp. 2237-2245, Jun. 2008.
- [12] A. Emadi, K. Rajashekara, S. S. Williamson, and S. M. Lukic, “Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations,” *IEEE Trans. Vehicular Technology*, vol. 54, no. 3, pp. 763-770, May 2005.
- [13] SAE Electric Vehicle and Plug-in Hybrid Electric Vehicle Conductive Charge Coupler, SAE Standard J1772, Oct. 2012.
- [14] SAE Electric Vehicle Inductively Coupled Charging, SAE Standard J1773, Jun. 2014.
- [15] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, “An automotive onboard 3.3-kW battery charger for PHEV application,” *IEEE Trans. Vehicular Technology*, vol. 61, no. 8, pp. 3466-3474, Oct. 2012.
- [16] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, “A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices,” *IEEE Trans. Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.
- [17] N. D. Weise, G. Castelino, K. Basu, and N. Mohan, “A single-stage dual-active-bridge-based soft switched AC–DC converter with open-loop power

- factor correction and other advanced features,” *IEEE Trans. Power Electronics*, vol. 29, no. 8, pp. 4007-4016, Aug. 2014.
- [18] Standard for electric vehicle (EV) charging system equipment, UL- 2202.
- [19] Standard for safety for personnel protection systems for electric vehicle (EV) supply circuits: General requirements, UL-2231-1.
- [20] Standard for safety for personnel protection systems for electric vehicle (EV) supply circuits: Particular requirements for protection devices for use in charging systems, UL-2231-2.
- [21] Deepak Gautham, “Investigation of high-performance DC-DC converters for plug-in hybrid electric vehicle battery chargers,” *Ph.D. Thesis*, The University of British Columbia, Canada, 2014.
- [22] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd edition. Kluwer, 2001.
- [23] G. Hua and F. C. Lee, “Soft-switching techniques in PWM converters,” *IEEE Trans. Industrial Electronics*, vol. 42, no. 6, pp. 595-603, Dec. 1995.
- [24] R. L. Steigerwald, “A review of soft-switching techniques in high performance DC power supplies,” in *Proc. 21st Annual Conference of IEEE Industrial Electronics Society (IECON)*, Florida, 1995, pp. 1-7.
- [25] T. W. Ching and K. U. Chan, “Review of soft-switching techniques for high-frequency switched-mode power converters,” in *Proc. IEEE Vehicle Power and Propulsion Conference*, Harbin, 2008, pp. 1-6.
- [26] Naga Brahmendra Yadav Gorla, “A new active soft-switching circuit for phase-shifted full-bridge DC-DC converter,” *M.Sc. Thesis*, Indian Institute of Technology Madras, India, 2013.
- [27] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, “A novel ZVZCS full-bridge DC-DC converter used for electric vehicles,” *IEEE Trans. Power Electronics*, vol. 27, no. 6, pp. 2752-2769, Jun. 2012.

Chapter 2

Literature Review

In this chapter, a comprehensive review of the related research works on gating techniques and adaptive control methods for full-bridge converters are presented in detail. Earlier works related to full-load range soft-switched resonant full-bridge dc-dc converters, active auxiliary circuit assisted full-bridge dc-dc converters and passive auxiliary circuit assisted full-bridge dc-dc converters are also discussed. Finally, a review of state-of-art methods to minimize voltage spikes across output rectifier diodes in the full-bridge dc-dc converter is presented.

2.1 Gating Techniques and Adaptive Control Methods

Figure 2.1 Basic PWM strategy [2].

The circuit configuration of conventional FB dc-dc converter with inductive output filter is shown in Figure 1.10. The gating techniques are explained according to the converter topology in Figure 1.10. The basic PWM strategy is presented in Figure 2.1 in which the diagonal switches S_1 and S_2 or S_3 and S_4 turn on/off simultaneously and are gated with same duty cycle ‘ D ’ [1]-[3]. The disadvantage of this method is that soft-switching is not achieved. Also, in the case of current-doubler rectifier circuit on secondary side, the output voltage control is lost at light-load conditions. An asymmetrical duty cycle control method proposed in [4]-[7] achieves ZVS over narrow load range as shown in Figure 2.2. In this approach, the diagonal switches S_1 and S_2 are gated with duty cycle ‘ D ’ and S_3 and S_4 are gated with duty cycle ‘ $(1-D)$ ’. Similarly, in the case of half-bridge converters, the high-side switch is operated with duty cycle “ D ” and the low-side switch is operated with duty cycle ‘ $(1-D)$ ’ [8]-[12]. In both cases, the asymmetrical nature of inverter output voltage V_{AB} increases the conduction and transformer core losses [13]. However, the core loss is minimized with modified secondary rectifier stage, i.e., at the cost of additional components [14].

Figure 2.2 Asymmetrical duty cycle control method [4].

Figure 2.3 Phase-shift modulation method [2].

As shown in Figures 2.1 and 2.2, the two diagonal switches turn-off simultaneously. ZVS transition is also possible when the two diagonal switches are turned off in a staggered manner which is called as PSM [1]-[3]. In this method, the output voltage is controlled through phase-shift between two legs of the converter as shown in Figure 2.3. This introduces the concept of leading-leg and lagging-leg. The leading-leg switches S_1 and S_4 realize ZVS over wide load range whereas the lagging-leg switches S_2 and S_3 realize ZVS over narrow load range. ZVS for

leading-leg switches may not be guaranteed in the case of high input voltage and light-load conditions.

Figure 2.4 FB converter with a simple passive auxiliary circuit.

FB converter requires additional auxiliary circuit components to achieve full-load range ZVS for all active switches. A simple passive auxiliary circuit assisted FB converter is shown in Figure 2.4. PSM combined with duty cycle control technique has been proposed in [15]-[18] for the converter shown in Figure 2.4 to achieve better efficiency. In this method, the output voltage is controlled using the phase-shift between two legs and the auxiliary circuit current i_{La} is controlled through duty cycle of switches.

A modified asymmetrical duty cycle control method has been proposed for three-phase dc-dc converter [19]-[21]. Trailing-edge and leading-edge PWM methods have been proposed in [22]-[26] for FB dc-dc converters. Motivated from these works, a new asymmetrical pulse-width modulation (APWM) for auxiliary circuit assisted FB dc-dc converters is proposed in this thesis which is explained in Chapters 3, 4 and 5. The proposed method achieves the same efficiency as PSM combined with duty cycle control method. The proposed method also reduces the auxiliary inductance required for ZVS over the entire battery charging range. Similar advantages can also be achieved using trailing-edge PWM [22], [23].

Load adaptive variable frequency control methods have been proposed in [7], [27]-[35] for resonant FB converters to achieve higher efficiency at light-load conditions. The proposed APWM combined with adaptive frequency control makes further improvement in efficiency and reduction in auxiliary inductance.

Figure 2.5 CC-CV charging strategy [36].

2.2 Soft-Switched Full-Bridge DC-DC Converters for Battery Charging

Let us first understand the load characteristics and then soft-switched converters. Most of the PHEVs/EVs are deployed with Li-ion batteries because of high power density, high energy density, no memory effect, and low self-discharge rate [36]. Li-ion battery pack is typically charged with constant current (CC) and constant voltage (CV) charging strategies as shown in Figure 2.5 which can achieve fast charging while avoiding performance degradation [36]-[40]. The depleted battery pack is firstly charged in CC mode, where the battery voltage begins to increase and reaches maximum pack voltage. Then, it is charged in CV mode, where the charging current begins to decrease. Therefore, the dc-dc converter has to be operated with a satisfactory performance throughout the CC-CV battery charging.

As mentioned earlier, the performance characteristics of dc-dc conversion stage in battery charger are highlighted here again for reviewing the state-of-art.

- a) Soft-switching for all active switches throughout the battery charging range;
- b) Wide output voltage and current regulation according to battery charging profile;
- c) Minimal circulating losses during freewheeling period;
- d) Low voltage rating for secondary rectifier diodes;
- e) Low dv/dt , di/dt and EMI;
- f) Narrow switching frequency variation to minimize switching and conduction losses (in the case of variable frequency operated converters).

The most preferred dc-dc converter topology for on-board PHEV/EV battery chargers is the ZVS FB converter operated at a constant frequency as shown in Figure 1.10 [41]-[47]. FB converter has the following advantages:

- Minimum voltage and current stress in power switches;
- Natural ZVS;
- Low output current ripple.

Since the battery pack voltage is very high and varies over a wide range during battery recharging, the converter suffers from the following:

- Loss of ZVS under light-load conditions in CV charging mode as the energy in leakage inductor is not sufficient to completely discharge MOSFET capacitor;
- High circulating currents and conduction losses during freewheeling period;
- Duty cycle loss;
- Severe voltage spikes across secondary rectifier diodes due to the parasitic ringing with transformer leakage inductance;
- Increased EMI.

For these reasons, the conversion efficiency of FB dc-dc converter is low and cannot achieve superior performance throughout the charging range. Several

modified FB converter topologies have been proposed and analyzed in [48]-[114] to guarantee ZVS over operating range without loss of duty cycle as well as reduced circulating current resulting in higher efficiency and higher power density for dc-dc converters. These topologies are broadly classified into resonant converters, active auxiliary circuit assisted converters, and passive auxiliary circuit assisted converters. Various snubber circuits and topologies are proposed in [115]-[149] to mitigate voltage spikes across output rectifier diodes. The trade-off analysis of these topologies is discussed in the following sections.

2.2.1 Resonant Full-Bridge DC-DC Converters

Based on the type of resonant circuit in series/parallel and its relationship with the load, resonant dc-dc converter topologies are classified into four categories: (a) series resonant converter (SRC); (b) parallel resonant converter (PRC); (c) LCC series-parallel resonant converter (LCC-SPRC); and (d) LLC series-parallel resonant converter (LLC-SPRC).

In resonant converters, the input impedance of the resonant circuit could be capacitive or inductive in nature which is based on the load condition and the switching frequency of operation. When the operation is in the capacitive region, the input current leads input voltage which creates ZCS for switches. However, the turn-on process of switches and turn-off process of body-diodes are hard switching which leads to significant switching losses in the converter. Therefore, MOSFETs are not suitable as the primary switches in high switching frequency applications and are not suitable for capacitive region operation. When the operation is in the inductive region, the input current lags input voltage which creates ZVS for switches and ZCS for body-diodes. However, the turn-off process of switches is hard switching. The reverse-recovery losses of body-diodes are also eliminated. Therefore, MOSFETs are suitable as primary switches in high switching frequency

applications. In this case, the turn-off losses of the switches could be minimized by adding a snubber capacitor in parallel with the switches. The advantages and disadvantages of different types of resonant converters are discussed in the following sub-sections.

2.2.1.1 Series Resonant Full-Bridge Converters

Figure 2.6 Series resonant FB dc-dc converter [48].

Series resonant FB dc-dc converters with capacitive output filter have been proposed in [7], [48]-[50] and the typical circuit configuration is shown in Figure 2.6. Under fixed-frequency control, the converter may achieve ZVS or ZCS for all switches depending on the load conditions [51].

Under variable frequency SRC control, all switches achieve ZVS throughout the load range. During CC charging phase, the circulating and conduction losses are smaller as the required operating switching frequency range is small. Another advantage of SRC is its good short-circuit protection performance due to the easy switching frequency boosting for controlling the short-circuit current. During CV charging phase, the circulating losses are small as the circulating current in resonant tank is equal to the load current. However, the light-load conditions

require higher switching frequency operation to achieve ZVS, i.e., SRC suffers from high switching loss in CV charging phase. Moreover, SRC has poor voltage regulation at light-load conditions [52]. The FB dc-dc converters with secondary series resonant tank have been proposed in [53], [54]. Soft-switching and resonant operations can be separated in these converters. The advantages and disadvantages of these converters are same as SRC. However, the converter in [54] is operated by fixed frequency duty cycle control for improved output voltage regulation at light loads.

2.2.1.2 Parallel Resonant Full-Bridge Converters

Figure 2.7 Parallel resonant FB dc-dc converter [55].

Parallel resonant FB dc-dc converters have been proposed in [55], [56] and the circuit configuration is shown in Figure 2.7. Under fixed frequency control, PRC offers ZVS from no load to full load, but the inverter peak current does not reduce with the reduction in load current which increases the circulating losses at light-load conditions [51].

Under variable frequency PRC control, all switches achieve ZVS throughout the load range. During CC charging phase, PRC also has good performance same as

SRC, i.e., small circulating and conduction losses, and good short-circuit protection performance.

During CV charging phase, the input current is relatively independent of the load conditions which is the main disadvantage of PRC. Because of this characteristic, most of the current circulates in the resonant tank and does not transfer power to the load. Therefore, PRC has poor efficiency under light-load conditions [52].

2.2.1.3 Series-Parallel LCC Resonant Full-Bridge Converters

Figure 2.8 LCC series-parallel resonant FB dc-dc converter [57].

Series-parallel resonant LCC FB dc-dc converters have been proposed in [57]-[59] and the circuit configuration is shown in Figure 2.8. Under fixed frequency control, LCC SPRC cannot maintain ZVS for all active switches for the wide variation in line and load conditions [51].

Under variable frequency LCC-SPRC control, all switches achieve ZVS throughout the load range. However, during CC charging phase, LCC-SPRC has relatively high circulating energy in the resonant circuit which results in significant conduction losses. During CV charging phase, the LCC-SPRC also has more

circulating power compared to SRC and same circulating power as that of PRC which increases the conduction losses resulting in lower conversion efficiency [52].

2.2.1.4 Series-Parallel LLC Resonant Full-Bridge Converters

Figure 2.9 LLC series-parallel resonant FB dc-dc converter with inductive output filter [60].

Series-parallel resonant LLC FB dc-dc converters with inductive output filter have been proposed in [60], [61] and the basic circuit configuration is shown in Figure 2.9. Series-parallel resonant based LLC FB dc-dc converters with capacitive output filter have been proposed in [33], [62]-[74] and the basic circuit configuration is shown in Figure 2.10.

LLC SPRCs offer ZVS for all switches throughout the operating range, and it is the best-suited topology for battery charging applications compared to other three resonant converters.

During CC charging phase, LLC-SPRC also has relatively smaller circulating energy in the resonant circuit which results in lower conduction losses similar to SRC.

Figure 2.10 LLC Series-Parallel resonant FB dc-dc converter with capacitive output filter [62].

During CV charging phase, the LLC-SPRC has better output voltage regulation compared to SRC due to the large slope of voltage curve. However, the short-circuit performance of LLC SPRC converter is not better than other three resonant converter types [52].

LLC SPRCs with inductive output filter suffer from severe voltage spikes across output rectifier diodes and secondary duty cycle loss whereas the converter with capacitive filter has the voltage across secondary diode that is clamped to output voltage.

The summary of the performance comparison of resonant converters in PHEV/EV charging applications is highlighted in Table 2.1. It can be inferred from summary table that the resonant converters have to be operated over wide switching frequency range to achieve soft-switching. Variable frequency operation of converter leads the resonant operation to be impractical and difficult design of filters and protection circuits [75].

Table 2.1 Comparison of resonant converters [52]

Performance	Charging mode	SRC	PRC	LCC SPRC	LLC SPRC
Short-circuit protection	CC & CV modes	Very good	Very good	Very good	Good
Frequency variation range	CC mode	high	low	Very low	Very high
Conduction loss	CC mode	Very small	Very small	Very large	Small
Efficiency	CC mode	High	High	Moderate	High
Frequency variation range	CV mode	Very high	Low	High	Very low
Circulating loss	CV mode	Very small	Very large	Very large	Large
Conduction loss	CV mode	Large	Small	Moderate	Small
Efficiency	CV mode	Moderate	Low	Low	Moderate
Voltage regulation	CV mode	Bad	Good	Good	Good

2.2.2 Active Auxiliary Circuit Assisted Full-Bridge DC-DC Converters

Figure 2.11 FB converter with a simple active auxiliary circuit [76].

As discussed earlier, the ZVS range of FB converter is extended by creating controlled resonance switching transitions using active auxiliary circuits. As the name suggests, the active auxiliary circuit is comprised of gate controlled switches, diodes, and inductors/capacitors. Active auxiliary circuit assisted FB dc-dc converters have been proposed in [76]-[87] and their basic circuit configuration is shown in Figure 2.11.

PSM converter proposed in [77] aids ZVS for lagging leg switches over the full-load range. The conduction losses due to the auxiliary circuit are less as it is operated for a short time. But the auxiliary switch's turn-off losses cannot be eliminated. The converter also has high conduction losses in the main power circuit. The soft-switching circuits proposed in [78], [79] have higher conduction losses due to the operation of auxiliary switches for a longer time, and the turn-off switching losses are also present. The auxiliary circuit proposed in [80] has minimal conduction losses in the main power circuit. The series resonant active auxiliary circuit in [81] further reduces the auxiliary circuit and main circuit conduction losses. However, the turn-off switching losses remain present. The active auxiliary circuit configuration proposed in [82] eliminates turn-off switching losses at the cost of increased component count. The FB converter in [82] is further improved by adopting APWM in which the active auxiliary circuit is required to be integrated for both low-side switches [83]. FB converters proposed in [84], [85] are combined with secondary-side phase-shifted active switches for achieving extended ZVS range. Also, these topologies minimize the circulating losses in the primary side. The required number of auxiliary circuit components is reduced using new pulse width modulation technique as proposed in [86], [87].

In summary, active auxiliary circuit assisted FB converters offer soft-switching transitions independent of the load condition. However, active auxiliary circuits make the power converter circuit complex, increase the cost, require additional gate drivers, and reduce the reliability of the dc-dc converter. ZVS for auxiliary switches is also necessary to improve the efficiency of the converter as battery charger operates at a higher voltage. Also, ZVS for leading-leg switches may not be possible at light-load in CV charging phase. This phenomenon requires additional auxiliary circuits which further degrades the performance of the converter. Therefore, active auxiliary circuit assisted FB dc-dc converters are not much suitable for dc-dc conversion stage in PHEV/EV charger.

2.2.3 Passive Auxiliary Circuit Assisted Full-Bridge DC-DC Converters

Figure 2.12 FB converter with a passive auxiliary circuit on both legs [96].

In this type of converters, the passive auxiliary is typically formed by transformer/inductor and capacitors. In [88], the extended ZVS range for FB converter is achieved either by increasing the leakage inductance of the transformer or by adding an external series inductor. However, this approach results in reduced effective duty cycle, higher switch currents, increased circulating current, and causes severe voltage spikes across output rectifier diodes. The duty cycle loss in [88] is reduced using a saturable inductor [89], [90] in place of the external series linear inductor, but it requires a large core size which decreases the power density of converter. The converters in [91], [92] use additional power transformer, forming two parallel half-bridge inverters to achieve full ZVS range. The parallel configuration also reduces the voltage stress across secondary rectifiers compared to conventional FB converter, but the voltage spikes are not eliminated completely. The FB converter topologies proposed in [93]-[95] use energy stored in the magnetizing inductance of auxiliary transformer to achieve full-load range ZVS. However, the overall conduction and auxiliary circuit losses are high as the energy stored in this auxiliary circuit is independent of the load conditions. Also, the auxiliary circuit guarantees full load range ZVS for lagging leg only and not

guaranteed for leading leg switches at very light-load conditions. In [96], [97], the auxiliary pole circuit is added to both legs of the full-bridge converter which achieve ZVS for both leading and lagging leg switches from no load to full load. The configuration of a converter of this type is shown in Figure 2.12. However, these topologies increase circulating and conduction losses at heavy-load conditions as the auxiliary circuit currents are independent of the load. Therefore, these converters are further improved using a resonant auxiliary circuit [98], [99] which reduces the conduction and auxiliary circuit losses.

Ideally, an auxiliary circuit is not required to store energy at heavy loads as ZVS is achieved using the leakage inductance of power transformer. It has to store required additional reactive energy when the energy stored in leakage inductor is not sufficient to create ZVS, i.e., the auxiliary circuit energy should be dependent on load condition or should be load adaptive for higher power conversion efficiency of FB converter.

Figure 2.13 FB converter with adaptive passive auxiliary circuit [110].

ZVS full-bridge converter topologies assisted with adaptive passive auxiliary circuits have been proposed and analyzed in [100]-[110]. One of the adaptive auxiliary circuit topologies is shown in Figure 2.13 [110]. The auxiliary circuit configurations proposed in [107]-[110] reduces the auxiliary inductance by a factor

of two compared to the topologies in [100]-[106]. However, the applicability of these topologies is limited by reduced effective duty cycle and high voltage spikes across rectifier diodes.

In summary, passive auxiliary circuit assisted FB converters create ZVS transitions throughout the load range at the cost of extra conduction losses [111]-[114]. The passive auxiliary circuits are easy to implement and more reliable compared to active auxiliary circuits as they do not require additional active switches and gate driver circuit. It is also easy to implement gating techniques as active switches are not required in these topologies. Therefore, passive auxiliary circuit assisted FB dc-dc converters are much more suitable for dc-dc conversion stage in PHEV/EV charger. However, they decrease the power density of power conversion system.

2.3 Methods to Suppress Voltage Spikes in Full-Bridge Converters

Another major problem of conventional FB converters is the voltage spikes across the output rectifier diodes due to secondary-side ringing (resonance) between junction capacitance of rectifier diodes with the transformer leakage inductance. The voltage spikes are intensified with the increase in the leakage inductance of the power transformer and increase in operating switching frequency of the converter. Therefore, the output rectifier diodes and the output filter should be overrated to withstand voltage spikes. Overrated diodes lead to increased losses due to higher forward voltage drop and poor reverse recovery characteristics. Overrated filter diminishes the power density of the converter. Also, the voltage spikes significantly increase the EMI and reduce the reliability of the converter. Different methods have been proposed in the literature [115]-[149] to solve the voltage spikes issue in FB converters which are discussed in the following sub-sections.

2.3.1 RCD Snubber

Figure 2.14 FB converter with RCD snubber [115].

Resistor-Capacitor-Diode (RCD) snubber circuits have been proposed and analyzed [115]-[119] to suppress the voltage spikes across output rectifier diodes in an FB converter. The snubber circuit is simple and uses only passive components. The basic circuit configuration of an RCD snubber assisted conventional FB converter is shown in Figure 2.14.

The disadvantage of RCD snubber circuit is that the energy stored in the capacitor is dissipated in snubber resistor which considerably reduces the efficiency of the converter. The rating and power loss of snubber circuit increases with the increase in the leakage inductance of power transformer. Also, it can only reduce the peak value of voltage spikes. Therefore, RCD snubber circuit is not much suitable for dc-dc conversion stage in PHEV/EV charger.

2.3.2 Diode Clamp Snubber

Figure 2.15 FB converter with diode clamp snubber [121].

The FB converters proposed in [108], [120], [121] can handle the voltage ringing problem using two clamping diodes on the primary side. The conventional FB converter with a clamping diode snubber is shown in Figure 2.15. After one of the switches is turned off, the voltage across output rectifier diodes raises due to the resonance between junction capacitance of rectifier diodes with the transformer leakage inductance and external series inductor. One of the clamping diodes is turned on when the reflected transformer primary voltage is greater than the input voltage. At the same time, the external inductor is shorted through clamping diode and one of the lagging leg switches. Therefore, the energy stored in the external inductor is separated from the resonance, which results in low-voltage ringing across rectifier diodes. However, the secondary side duty cycle loss problem is not eliminated. Also, the voltage spike level is reduced but not completely mitigated due to the presence of transformer leakage inductance. Therefore, the power transformer should be designed to have very low leakage inductance.

2.3.3 Active Clamp Snubber

Figure 2.16 FB converter with active clamp snubber on secondary side [122].

Zero-voltage zero-current switching (ZVZCS) FB converters have been proposed [122]-[149] to eliminate voltage spikes across rectifier diodes, reverse-recovery losses in rectifier diodes and circulating losses during the freewheeling period on the primary side. The fundamental principle of the converter is that the primary current during the freewheeling period is reduced to zero.

In [122]-[125], an active clamp circuit has been added on either primary/secondary side to reset the transformer primary current at which the voltage across rectifier diodes is clamped to the output voltage. The FB converter with an active clamp on the secondary side is shown in Figure 2.16. However, the active clamp circuit approach increases the cost and complexity of the converter and reduces the efficiency due to hard switching.

2.3.4 Energy Recovery Clamp Snubber

In energy recovery clamp (ERC) snubber circuits [126]-[140], the ZVZCS condition is achieved by adding lossless auxiliary circuits on the secondary side.

Figure 2.17 FB converter with energy recovery clamp snubber on secondary side [126].

The widely used FB converter with the passive auxiliary circuit to reset the transformer primary current is shown in Figure 2.17 [126]-[132]. In [133]-[135], improved ERC snubber circuit configurations have been proposed to accommodate the effects of voltage spikes for a wide range of input voltage. In [136], the primary current is brought to zero by adding a transformer auxiliary winding and a simple auxiliary circuit on the secondary side. All the active and passive elements are operated under minimum voltage and current stresses. In [137], an output coupled inductor has been used to reset the transformer primary current, and the circulating current is kept at minimum values which increase the efficiency over wide load range. In [139], an auxiliary voltage source is applied to reset the transformer primary current and soft-switching is achieved without any increase of voltage and current stresses of all elements. In [139], [140], resonant and hybrid-switching methods have been used to eliminate voltage spikes across output rectifier diodes. Also, the output filter size is optimized. Although these ERC snubber techniques can reduce the voltage stress of the output diodes, the amount of the voltage stress depends on the duty cycle ratio and input voltage of the converter in most of the ERCs methods. Hence, these techniques are not much preferred in battery charger applications, as the duty cycle and output voltage vary over wide load range. Also,

extra semiconductor elements are necessary for all these methods mentioned above.

2.3.5 Current-fed Full-Bridge Converters

Figure 2.18 Current-fed FB converter with capacitive output filter [23].

Current-fed FB converters [23], [141]-[149] have received much attention due to their inherent capability to minimize the voltage spikes across output rectifier diodes. The current-fed FB dc-dc converter with capacitive output filter is shown in Figure 2.18 [23].

These types of converters are operated in discontinuous conduction mode (DCM) for resetting the primary current of the transformer. The circulating losses during the freewheeling period in primary side and reverse-recovery losses of output rectifier diodes are greatly minimized. Also, these topologies do not require any additional clamp snubber circuits which increase the power density and reliability of the converter. However, the DCM operation of the converter increases RMS and peak values of the series inductor which deteriorates the efficiency of the converter during CV charging phase.

References

- [1] X. Ruan and Y. Yan, "Soft-switching techniques for PWM full-bridge converters," in *Proc. 31st IEEE Power Electronics Specialists Conference (PESC)*, 2000, pp. 634-639.
- [2] X. Ruan, *Soft-switching PWM full-Bridge converters: topologies, control, and design*. Wiley, 2014.
- [3] J. Dudrik and J. Oetter, "High-frequency soft-switching dc-dc converters for voltage and current dc Power Sources," *Acta Polytechnica Hungarica*, vol. 4, no. 2, 2007.
- [4] P. Imbertson and N. Mohan, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," *IEEE Trans. Industrial Applications*, vol. 29, no. 1, pp. 121-125, Feb. 1993.
- [5] A. Fiedler and H. Grotstollen, "Investigation of asymmetrical phase-shifted full-bridge power converters," in *Proc. IEEE Annual Industrial Electronics Conference (IECON)*, 1995, pp. 434-439.
- [6] P. Imbertson and N. Mohan, "New directions in dc-dc power conversion based on idealized concepts leading ultimately to the asymmetrical duty-cycle power converter," *IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 722-727, Aug. 1997.
- [7] S. H. Ryu, D. H. Kim, M. J. Kim, J. S. Kim, and B. K. Lee, "Adjustable frequency-duty-cycle hybrid control strategy for full-bridge series resonant converters in electric vehicle chargers," *IEEE Trans. Industrial Electronics*, vol. 61, no. 10, pp. 5354-5362, Oct. 2014.
- [8] X. Xu, A. M. Khambadkone, T. M. Leong, and R. Oruganti, "A 1-MHz zero-voltage-switching asymmetrical half-bridge dc-dc converter: analysis and design," *IEEE Trans. Power Electronics*, vol. 21, no. 1, pp. 105-113, Jan. 2006.

- [9] D. J. Tschirhart and P. K. Jain, "A CLL resonant asymmetrical pulsewidth-modulated converter with improved efficiency," *IEEE Trans. Industrial Electronics*, vol. 55, no. 1, pp. 114-122, Jan. 2008.
- [10] B. C. Kim, K. B. Park, and G. W. Moon, "Asymmetric PWM control scheme during hold-up time for LLC resonant converter," *IEEE Trans. Industrial Electronics*, vol. 59, no. 7, pp. 2992-2997, Jul. 2012.
- [11] L. Wang, Z. Wang, and H. Li, "Asymmetrical duty cycle control and decoupled power flow design of a three-port bidirectional dc-dc converter for fuel cell vehicle application," *IEEE Trans. Power Electronics*, vol. 27, no. 2, pp. 891-904, Feb. 2012.
- [12] D. J. Tschirhart and P. K. Jain, "Design procedure for high-frequency operation of the modified series-resonant APWM converter to reduce size and circulating current," *IEEE Trans. Power Electronics*, vol. 27, no. 10, pp. 4181-4191, Oct. 2012.
- [13] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the dc bias condition based on steinmetz parameters," *IEEE Trans. Power Electronics*, vol. 27, no. 2, pp. 953-963, Feb. 2012.
- [14] I. O. Lee and G. W. Moon, "A new asymmetrical half-bridge converter with zero dc-ffset current in transformer," *IEEE Trans. Power Electronics*, vol. 28, no. 5, pp. 2297-2306, May 2013.
- [15] H. Daneshpajoo, A. Bakhshai, and P. Jain, "Design of dc-dc converter with phase shift and duty cycle control for full range soft switching," in *Proc. 33rd IEEE International Telecommunications Energy Conference (INTELEC)*, 2011, pp. 1-6.
- [16] H. Daneshpajoo, M. Pahlevaninezhad, P. Jain, and A. Bakhshai, "An efficient soft switched DC-DC converter for electric vehicles," in *Proc. 28th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 1798-1803.

- [17] M. Pahlevaninezhad, H. Daneshpajoo, A. Bakhshai, and P. Jain, "A multi-variable control technique for ZVS phase-shift full-bridge dc-dc converter," in *Proc. 28th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 257-262.
- [18] M. Mohammadi, J. Milimonfared, J. S. Moghani, and M. Taheri, "A high step-up current-fed phase-shift double-input dc-dc converter using asymmetrical PWM switching strategy," in *Proc. 6th Power Electronics, Drive Systems and Technologies Conference (PEDSTC2015)*, 2015, pp. 400-405.
- [19] D. S. Oliveira and I. Barbi, "A three-phase ZVS PWM dc-dc converter with asymmetrical duty cycle associated with a three-phase version of the hybrid rectifier," *IEEE Tran. Power Electronics*, vol. 20, no. 2, pp. 354-360, Mar. 2005.
- [20] D. D. Souza Oliveira and I. Barbi, "A three-phase ZVS PWM dc-dc converter with asymmetrical duty cycle for high power applications," *IEEE Trans. Power Electronics*, vol. 20, no. 2, pp. 370-377, Mar. 2005.
- [21] F. Liu, Y. Chen, G. Hu, and X. Ruan, "Modified three-phase three-level dc-dc converter with zero-voltage-switching characteristic-adopting asymmetrical duty cycle control," *IEEE Trans. Power Electronics*, vol. 29, no. 12, pp. 6307-6318, Dec. 2014.
- [22] L. Hitchcock, "Full bridge power converter circuit," US Patent 4860189, 22 Aug. 1989.
- [23] D. S. Gautam, F. Musavi, W. Eberle, and W. G. Dunford, "A zero-voltage switching full-bridge dc-dc converter with capacitive output filter for plug-in hybrid electric vehicle battery charging," *IEEE Trans. Power Electronics*, vol. 28, no. 12, pp. 5728-5735, Dec. 2013.

- [24] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Wiley-IEEE Press, Jun. 2015.
- [25] M. Pahlevani, S. Pan, and P. Jain, "A hybrid phase-shift modulation technique for dc-dc converters with a wide range of operating conditions," *IEEE Trans. Industrial Electronics*, vol. 63, no. 12, pp. 7498-7510, Dec. 2016.
- [26] H. Haga and F. Kurokawa, "Modulation method of a full-bridge three-level LLC resonant converter for battery charger of electrical vehicles," *IEEE Trans. Power Electronics*. (In Press)
- [27] C. Zhao, X. Wu, G. Zhang, and Z. Qian, "Variable frequency PWM controlled soft switched FB-PESI dc-dc converter," in *Proc. 6th IEEE International Power Electronics and Motion Control Conference (IPEMC)*, 2009, pp. 1378-1383.
- [28] O. Lucia, J. M. Burdio, I. Millan, J. Acero, and D. Puyal, "Load-adaptive control algorithm of half-bridge series resonant inverter for domestic induction heating," *IEEE Trans. Industrial Electronics*, vol. 56, no. 8, pp. 3106-3116, Aug. 2009.
- [29] M. Pahlevaninezhad, H. D. Pajooh, A. Bakhshai, and P. Jain, "A load/line adaptive zero voltage switching dc-dc converter used in electric vehicles," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, pp. 2065-2070.
- [30] M. Pahlevaninezhad, J. Drobniak, P. K. Jain, and A. Bakhshai, "A load adaptive control approach for a zero-voltage-switching dc-dc converter used for electric vehicles," *IEEE Trans. Industrial Electronics*, vol. 59, no. 2, pp. 920-933, Feb. 2012.

- [31] I. O. Lee, "Hybrid dc-dc converter with phase-shift or frequency modulation for NEV battery charger," *IEEE Trans. Industrial Electronics*, vol. 63, no. 2, pp. 884-893, Feb. 2016.
- [32] S. M. S. Shakib and S. Mekhilef, "A frequency adaptive phase-shift modulation control based LLC series resonant converter for wide input voltage applications," *IEEE Trans. Power Electronics*. (In Press)
- [33] S. Zong, H. Luo, W. Li, Y. Deng, and X. He, "Asymmetrical duty cycle-controlled LLC resonant converter with equivalent switching frequency doubler," *IEEE Trans. Power Electronics*, vol. 31, no. 7, pp. 4963-4973, Jul. 2016.
- [34] L. Gang, Y. Jang, M. Jovanovic, and J. Q. Zhang, "Implementation of a 3.3-kW dc-dc converter for EV on-board charger employing series-resonant converter with reduced-frequency-range control," *IEEE Trans. Power Electronics*. (In Press)
- [35] Y. Jang, M. M. Jovanović, J. M. Ruiz, M. Kumar, and G. Liu, "Implementation of 3.3-kW GaN-based dc-dc converter for EV on-board charger with series-resonant converter that employs combination of variable-frequency and delay-time control," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1292-1299.
- [36] G. V. Rodrigo and A. P. L. Joao, *Electric Vehicle Integration into Modern Power Networks*. Springer, 2013.
- [37] Y. C. Hsieh and C. S. Huang, "Li-ion battery charger based on digitally controlled phase-shifted full-bridge converter," *IET Power Electronics*, vol. 4, no. 2, pp. 242-247, Feb. 2011.
- [38] B. Y. Chen and Y. S. Lai, "New digital-controlled technique for battery charger with constant current and voltage control without current feedback," *IEEE Trans. Industrial Electronics*, vol. 59, no. 3, pp. 1545-1553, Mar. 2012.

- [39] M. Pahlevaninezhad, A. Bakhshai, and P. Jain, "A novel open loop control scheme for a current-driven full-bridge dc-dc converter used in electric vehicles," in *Proc. 28th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2052-2056.
- [40] C. Botting, R. Stockton, D. Gautam, M. Edington, and F. Musavi, "Designing and testing battery charger systems for California's new efficiency regulations," in *Proc. 29th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 2690-2693.
- [41] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high voltage, high power, full-bridge ZVS PWM converters," in *Proc. 5th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1990, pp. 275-284.
- [42] D. B. Dalal, "A 500 kHz multi-output converter with zero voltage switching," in *Proc. 5th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1990, pp. 265-274.
- [43] B. P. McGrath, D. G. Holmes, P. J. McGoldrick, and A. D. McIver, "Design of a soft-switched 6-kW battery charger for traction applications," *IEEE Trans. Power Electronics*, vol. 22, no. 4, pp. 1136-1144, Jul. 2007.
- [44] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An automotive on-board 3.3-kW battery charger for PHEV application," *IEEE Trans. Vehicular Technology*, vol. 61, no. 8, pp. 3466-3474, Oct. 2012.
- [45] A. Khaligh and S. Dusmez, "Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles," *IEEE Trans. Vehicular Technology*, vol. 61, no. 8, pp. 3475-3489, Oct. 2012.
- [46] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electronics*, vol. 28, no. 5, pp. 2151-2169, May 2013.

- [47] B. Whitaker *et al.*, “A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices,” *IEEE Trans. Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.
- [48] J. A. Sabate and F. C. Y. Lee, “Offline application of the fixed-frequency clamped-mode series resonant converter,” *IEEE Trans. Power Electronics*, vol. 6, no. 1, pp. 39-47, Jan. 1991.
- [49] S. H. Ryu, D. H. Kim, M. J. Kim, B. K. Lee, and J. S. Kim, “Operating optimization at light load of series resonant dc-dc converter with duty-adjusted frequency control in EVs on-board charger,” in *Proc. IEEE Vehicle Power and Propulsion Conference*, 2012, pp. 777-782.
- [50] S. Pan, M. Pahlevaninezhad, and P. K. Jain, “Adaptive hybrid primary/secondary-side digital control for series resonant dc-dc converters in 48 V VR applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 422-429, Jun. 2015.
- [51] D. S. Gautam and A. K. S. Bhat, “A comparison of soft-switched dc-dc converters for electrolyzer application,” *IEEE Trans. Power Electronics*, vol. 28, no. 1, pp. 54-63, Jan. 2013.
- [52] H. Wang and A. Khaligh, “Comprehensive topological analyses of isolated resonant converters in PEV battery charging applications,” in *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, 2013, pp. 1-7.
- [53] A. Safaee, K. Woronowicz, T. Dickson, B. Koushki, P. Jain, and A. Bakhshai, “A fixed-frequency soft switching series resonant converter with adaptive auxiliary circuit for transportation applications,” in *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, 2015, pp. 1-7.
- [54] B. K. Lee, J. P. Kim, S. G. Kim, and J. Y. Lee, “A PWM SRT dc-dc converter for 6.6-kW EV on-board charger,” *IEEE Trans. Industrial Electronics*, vol. 63, no. 2, pp. 894-902, Feb. 2016.

- [55] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electronics*, vol. 3, no. 2, pp. 174-182, Apr. 1988.
- [56] F. S. Tsai, J. Sabate, and F. C. Lee, "Constant-frequency, zero-voltage-switched, clamped-mode parallel-resonant converter," in *Proc. 11th International Telecommunications Energy Conference*, 1989, pp. 16.4.1-16.4.7.
- [57] A. K. S. Bhat, "Fixed-frequency PWM series-parallel resonant converter," *IEEE Trans. Industry Applications*, vol. 28, no. 5, pp. 1002-1009, Sep.-Oct. 1992.
- [58] Y. C. Chuang, Y. L. Ke, H. S. Chuang, and Y. M. Chen, "Analysis and implementation of half-bridge series-parallel resonant converter for battery chargers," *IEEE Trans. Industry Applications*, vol. 47, no. 1, pp. 258-270, Jan.-Feb. 2011.
- [59] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, and S. R. Motahari, "Analysis and implementation of a fixed-frequency LCLC resonant converter with capacitive output filter," *IEEE Trans. Industrial Electronics*, vol. 58, no. 10, pp. 4773-4782, Oct. 2011.
- [60] A. K. S. Bhat, "A fixed frequency LCL-Type series resonant converter," *IEEE Trans. Aerospace and Electronic Systems*, vol. 31, no. 1, pp. 125-137, Jan. 1995.
- [61] J. H. Kim, I. O. Lee, and G. W. Moon, "Analysis and design of hybrid-type converter for optimal conversion efficiency in electric vehicle chargers," *IEEE Trans. Industrial Electronics*. (In Press)
- [62] A. K. S. Bhat, "Analysis and design of LCL-type series resonant converter," *IEEE Trans. Industrial Electronics*, vol. 41, no. 1, pp. 118-124, Feb. 1994.

- [63] A. K. S. Bhat, "Analysis and design of a fixed-frequency LCL-type series-resonant converter with capacitive output filter," *IEE Proceedings - Circuits, Devices and Systems*, vol. 144, no. 2, pp. 97-103, Apr. 1997.
- [64] S. Chudjuarjeen, A. Sangswang, and C. Koompai, "An improved LLC resonant inverter for induction-heating applications with asymmetrical control," *IEEE Trans. Industrial Electronics*, vol. 58, no. 7, pp. 2915-2925, Jul. 2011.
- [65] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An LLC resonant dc-dc converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electronics*, vol. 28, no. 12, pp. 5437-5445, Dec. 2013.
- [66] N. Harischandrappa and A. K. S. Bhat, "A fixed-frequency LCL-type series resonant converter with a capacitive output filter using a modified gating scheme," *IEEE Trans. Industry Applications*, vol. 50, no. 6, pp. 4056-4064, Nov.-Dec. 2014.
- [67] F. Musavi, M. Craciun, D. S. Gautam, and W. Eberle, "Control strategies for wide output voltage range LLC resonant dc-dc converters in battery chargers," *IEEE Trans. Vehicular Technology*, vol. 63, no. 3, pp. 1117-1125, Mar. 2014.
- [68] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a full-bridge LLC-based PEV charger optimized for wide battery voltage range," *IEEE Trans. Vehicular Technology*, vol. 63, no. 4, pp. 1603-1613, May 2014.
- [69] J. Deng, S. Li, S. Hu, C. C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Vehicular Technology*, vol. 63, no. 4, pp. 1581-1592, May 2014.
- [70] H. Wang, S. Dusmez, and A. Khaligh, "Maximum efficiency point tracking technique for LLC-based PEV chargers through variable dc link control,"

- IEEE Trans. Industrial Electronics*, vol. 61, no. 11, pp. 6041-6049, Nov. 2014.
- [71] H. Wang, M. Shang, and A. Khaligh, "A PSFB based integrated PEV on-board charger with extended ZVS range and zero duty cycle loss," *IEEE Trans. Industry Applications*. (In Press)
- [72] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A SiC-based, high-efficiency, isolated on-board PEV charger with ultra-wide dc link voltage range," *IEEE Trans. Industry Applications*. (In Press)
- [73] J. H. Kim, C. E. Kim, J. K. Kim, J. B. Lee, and G. W. Moon, "Analysis on load-adaptive phase-shift control for high efficiency full-bridge LLC resonant converter under light-load conditions," *IEEE Trans. Power Electronics*, vol. 31, no. 7, pp. 4942-4955, Jul. 2016.
- [74] J. B. Lee, J. K. Kim, J. I. Baek, J. H. Kim, and G. W. Moon, "Resonant capacitor on-off control of half-bridge LLC converter for high-efficiency server power supply," *IEEE Trans. Industrial Electronics*, vol. 63, no. 9, pp. 5410-5415, Sep. 2016.
- [75] D. S. Gautham, "Investigation of high-performance DC-DC converters for plug-in hybrid electric vehicle battery chargers," *Ph.D. Thesis, The University of British Columbia, Canada*, 2014.
- [76] G. Moschopoulos and P. Jain, "ZVS PWM full-bridge converters with dual auxiliary circuits," in *Proc. 22nd International Telecommunications Energy Conference (INTELEC)*, 2000, pp. 574-581.
- [77] J. G. Cho, J. A. Sabate, and F. C. Lee, "Novel full-bridge zero-voltage-transition PWM dc-dc converter for high power applications," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1994, pp. 143-149.
- [78] X. Zhang, W. Chen, X. Ruan, and K. Yao, "A novel ZVS PWM phase-shifted full-bridge converter with controlled auxiliary circuit," in *Proc. 24th*

- IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 1067-1072.
- [79] Z. Chen, S. Liu, and L. Shi, "Improved zero-voltage-switching pulse width modulation full bridge converter with self-regulating auxiliary current," *IET Power Electronics*, vol. 6, no. 2, pp. 287-296, Feb. 2013.
- [80] A. F. Bakan, N. Altıntaş, and I. Aksoy, "An improved PSFB PWM dc-dc converter for high-power and frequency applications," *IEEE Trans. Power Electronics*, vol. 28, no. 1, pp. 64-74, Jan. 2013.
- [81] D. S. Wijeratne and G. Moschopoulos, "A ZVS-PWM full-bridge converter with reduced conduction losses," *IEEE Tran. Power Electronics*, vol. 29, no. 7, pp. 3501-3513, Jul. 2014.
- [82] G. N. B. Yadav and N. L. Narasamma, "An active soft-switched phase-shifted full-bridge dc-dc converter: analysis, modeling, design, and implementation," *IEEE Trans. Power Electronics*, vol. 29, no. 9, pp. 4538-4550, Sep. 2014.
- [83] G. N. B. Yadav and N. L. Narasamma, "A new active soft-switching technique for pulse-width modulated full-bridge dc-dc converters," *International Journal of Environmental Science and Development*, vol. 5, no. 1, pp. 20-25, Feb. 2014.
- [84] T. Mishima and M. Nakaoka, "Practical evaluations of a ZVS-PWM dc-dc converter with secondary-side phase-shifting active rectifier," *IEEE Trans. Power Electronics*, vol. 26, no. 12, pp. 3896-3907, Dec. 2011.
- [85] T. Mishima, K. Akamatsu, and M. Nakaoka, "A high frequency-link secondary-side phase-shifted full-range soft-switching PWM dc-dc converter with ZCS active rectifier for EV battery chargers," *IEEE Trans. Power Electronics*, vol. 28, no. 12, pp. 5758-5773, Dec. 2013.

- [86] F. S. Hamdad and A. K. S. Bhat, "A novel pulse-width control scheme for fixed-frequency zero-voltage-switching dc-to-dc PWM bridge converter," *IEEE Trans. Industrial Electronics*, vol. 48, no. 1, pp. 101-110, Feb. 2001.
- [87] S. Zeljkovic, T. Reiter, and D. Gerling, "Efficiency optimized single-stage reconfigurable dc-dc converter for hybrid and electric vehicles," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 496-506, Sep. 2014.
- [88] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1990, pp. 275-284.
- [89] G. Hua, F. C. Lee, and M. M. Jovanovic, "An improved full-bridge zero-voltage-switched PWM converter using a saturable inductor," *IEEE Trans. Power Electronics*, vol. 8, no. 4, pp. 530-534, Oct. 1993.
- [90] S. Hamada and M. Nakaoka, "Analysis and design of a saturable reactor assisted soft-switching full-bridge dc-dc converter," *IEEE Trans. Power Electronics*, vol. 9, no. 3, pp. 309-317, May 1994.
- [91] I. O. Lee and G. W. Moon, "Soft-switching dc-dc converter with a full ZVS range and reduced output filter for high-voltage applications," *IEEE Trans. Power Electronics*, vol. 28, no. 1, pp. 112-122, Jan. 2013.
- [92] I. O. Lee, S. Y. Cho, and G. W. Moon, "Improved phase-shift PWM converter for larger sized PDP slim sustain power module," *IEEE Trans. Power Electronics*, vol. 28, no. 2, pp. 945-958, Feb. 2013.
- [93] R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement. I. regulated-output applications," *IEEE Trans. Power Electronics*, vol. 16, no. 2, pp. 184-192, Mar. 2001.
- [94] R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full ZVS-range and reduced filter requirement. II. constant-input, variable-output

- applications,” *IEEE Trans. Power Electronics*, vol. 16, no. 2, pp. 193-200, Mar. 2001.
- [95] Z. Chen, S. Liu, and L. Shi, “A soft-switching full-bridge converter with reduced parasitic oscillation in a wide load range,” *IEEE Trans. Power Electronics*, vol. 29, no. 2, pp. 801-811, Feb. 2014.
- [96] P. K. Jain, Wen Kang, H. Soin, and Y. H. Xi, “Analysis and design considerations of a load and line independent zero voltage switching full bridge dc-dc converter topology,” *IEEE Trans. Power Electronics*, vol. 17, no. 5, pp. 649-657, Sep. 2002.
- [97] Z. Chen, B. Ji, F. Ji, and L. Shi, “A novel ZVS full-bridge converter with auxiliary circuit,” in *Proc. 25th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 1448-1453.
- [98] A. Safaee, P. K. Jain, and A. Bakhshai, “An Adaptive ZVS full-bridge dc–dc converter with reduced conduction losses and frequency variation range,” *IEEE Trans. Power Electronics*, vol. 30, no. 8, pp. 4107-4118, Aug. 2015.
- [99] A. Safaee, P. Jain, and A. Bakhshai, “A ZVS pulse-width modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit,” *IEEE Trans. Power Electronics*, vol. 31, no. 6, pp. 4031-4047, Jun. 2016.
- [100] Y. Jang, M. M. Jovanovic, and Y. M. Chang, “A new ZVS-PWM full-bridge converter,” *IEEE Trans. Power Electronics*, vol. 18, no. 5, pp. 1122-1129, Sep. 2003.
- [101] Y. Jang and M. M. Jovanovic, “A new family of full-bridge ZVS converters,” *IEEE Trans. Power Electronics*, vol. 19, no. 3, pp. 701-708, May 2004.
- [102] C. Zhou, X. Liu, and S. Xie, “A novel phase-shift full-bridge ZVS PWM dc-dc converter employing auxiliary circuit,” in *Proc. 23rd IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2008, pp. 1496-1501.

- [103] I. O. Lee and G. W. Moon, "Half-bridge integrated ZVS full-bridge converter with reduced conduction loss for electric vehicle battery chargers," *IEEE Trans. Industrial Electronics*, vol. 61, no. 8, pp. 3978-3988, Aug. 2014.
- [104] M. Borage, S. Tiwari, S. Bhardwaj, and S. Kotaiah, "A full-bridge dc-dc converter with zero-voltage-switching over the entire conversion range," *IEEE Trans. on Power Electronics*, vol. 23, no. 4, pp. 1743-1750, Jul. 2008.
- [105] B. Yang, J. L. Duarte, W. Li, K. Yin, X. He, and Y. Deng, "Phase-shifted full bridge converter featuring ZVS over the full load range," in *Proc. 36th Annual Conference on IEEE Industrial Electronics Society (IECON)*, 2010, pp. 644-649.
- [106] A. Safaee, K. Woronowicz, T. Dickson, B. Koushki, P. Jain, and A. Bakhshai, "A fixed-frequency soft switching series resonant converter with adaptive auxiliary circuit for transportation applications," in *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, 2015, pp. 1-7.
- [107] M. Borage, S. Tiwari, and S. Kotaiah, "A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range," *IEEE Power Electronics Letters*, vol. 3, no. 4, pp. 141-143, Dec. 2005.
- [108] X. Wu, J. Zhang, X. Xie, and Z. Qian, "Analysis and optimal design considerations for an improved full-bridge ZVS dc-dc converter with high efficiency," *IEEE Trans. Power Electronics*, vol. 21, no. 5, pp. 1225-1234, Sep. 2006.
- [109] Z. Chen, B. Ji, F. Ji, and L. Shi, "Analysis and design considerations of an improved ZVS full-bridge dc-dc converter," in *Proc. 25th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 1471-1476.
- [110] W. Chen, X. Ruan, and J. Ge, "A novel full-bridge converter achieving ZVS over wide load range with a passive auxiliary circuit," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 1110-1115.

- [111] S. Bhardwaj, M. Borage, and Tiwari, "Simplified loss analysis and comparison of full-bridge, full-range-ZVS dc-dc converters," *Sadhana*, vol. 33, no. 5, pp. 481-504, Oct. 2008.
- [112] Z. Chen, S. Liu, L. Shi, and F. Ji, "Power loss analysis and comparison of two full-bridge converters with auxiliary networks," *IET Power Electronics*, vol. 5, no. 9, pp. 1934-1943, Nov. 2012.
- [113] Z. Chen, L. Shi, and F. Ji, "Comparison of phase-shifted full-bridge converters with auxiliary networks," in *Proc. 7th International Power Electronics and Motion Control Conference (IPEMCC)*, 2012, pp. 1700-1706.
- [114] Z. Chen, S. Liu, L. Shi, and F. Ji, "A power loss comparison of two full-bridge converters with auxiliary networks," in *Proc. 7th International Power Electronics and Motion Control Conference (IPEMCC)*, 2012, pp. 1888-1893.
- [115] L. H. Mweene, C. A. Wright, and M. F. Schlecht, "A 1 kW 500 kHz front-end converter for a distributed power supply system," *IEEE Trans. Power Electronics*, vol. 6, no. 3, pp. 398-407, Jul. 1991.
- [116] S. Y. Lin and C. L. Chen, "Analysis and design for RCD clamped snubber used in output rectifier of phase-shift full-bridge ZVS converters," *IEEE Trans. Industrial Electronics Letters*, vol. 45, no. 2, pp. 358-359, Apr. 1998.
- [117] L. Diao, J. Chen, W. Lin, and Z. Liu, "Analysis and design for reducing voltage stress in output rectifier of LFLRV SIV DC-DC converter," in *Proc. IEEE International Symposium on Industrial Electronics*, 2009, pp. 1077-1080.
- [118] Y. D. Kim, K. M. Cho, D. Y. Kim, and G. W. Moon, "Wide-range ZVS phase-shift full-bridge converter with reduced conduction loss caused by circulating current," *IEEE Trans. Power Electronics*, vol. 28, no. 7, pp. 3308-3316, Jul. 2013.

- [119] J. H. Kim, I. O. Lee, and G. W. Moon, "Integrated dual full-bridge converter with current-doubler rectifier for EV charger," *IEEE Trans. Power Electronics*, vol. 31, no. 2, pp. 942-951, Feb. 2016.
- [120] Y. Jang and M. M. Jovanovic, "A New PWM ZVS full-bridge converter," *IEEE Trans. Power Electronics*, vol. 22, no. 3, pp. 987-994, May 2007.
- [121] K. M. Cho, Y. D. Kim, I. H. Cho, and G. W. Moon, "Transformer integrated with additional resonant inductor for phase-shift full-bridge converter with primary clamping diodes," *IEEE Trans. Power Electronics*, vol. 27, no. 5, pp. 2405-2414, May 2012.
- [122] J. A. Sabate, V. Vlatkovic, R. B. Ridley, and F. C. Lee, "High-voltage, high-power, ZVS full-bridge PWM converter employing an active snubber," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1991, pp. 158-163.
- [123] J. G. Cho, C. Y. Jeong, and F. C. Y. Lee, "Zero-voltage and zero-current-switching full-bridge PWM converter using secondary active clamp," *IEEE Trans. Power Electronics*, vol. 13, no. 4, pp. 601-607, Jul. 1998.
- [124] J. Dudrik, P. Spanik, and N. D. Trip, "Zero-voltage and zero-current switching full-bridge dc-dc converter with auxiliary transformer," *IEEE Trans. Power Electronics*, vol. 21, no. 5, pp. 1328-1335, Sep. 2006.
- [125] A. Mousavi, P. Das, and G. Moschopoulos, "A comparative study of a new ZCS dc-dc full-bridge boost converter with a ZVS active clamp converter," *IEEE Trans. Power Electronics*, vol. 27, no. 3, pp. 1347-1358, Mar. 2012.
- [126] J. G. Cho, J. W. Baek, C. Y. Jeong, and G. H. Rim, "Novel zero-voltage and zero-current-switching full-bridge PWM converter using a simple auxiliary circuit," *IEEE Trans. Industry Applications*, vol. 35, no. 1, pp. 15-20, Jan.-Feb. 1999.
- [127] Y. Xiaobo, W. Weiyang, and S. Hong, "Analysis and modeling of the ZVZCS full-bridge PWM dc-dc converter using a secondary auxiliary

- circuit,” in *Proc. 36th IEEE Power Electronics Specialists Conference (PESC)*, 2005, pp. 1018-1023.
- [128] C. Liu *et al.*, “High-efficiency hybrid full-bridge-half-bridge converter with shared ZVS lagging leg and dual outputs in series,” *IEEE Trans. Power Electronics*, vol. 28, no. 2, pp. 849-861, Feb. 2013.
- [129] I. O. Lee and G. W. Moon, “Phase-shifted PWM converter with a wide ZVS range and reduced circulating current,” *IEEE Trans. Power Electronics*, vol. 28, no. 2, pp. 908-919, Feb. 2013.
- [130] B. Gu, C. Y. Lin, B. Chen, J. Dominic, and J. S. Lai, “Zero-voltage-switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers,” *IEEE Trans. Power Electronics*, vol. 28, no. 10, pp. 4657-4667, Oct. 2013.
- [131] A. Mousavi and G. Moschopoulos, “A new ZCS-PWM full-bridge dc-dc converter with simple auxiliary circuits,” *IEEE Trans. Power Electronics*, vol. 29, no. 3, pp. 1321-1330, Mar. 2014.
- [132] H. Wang, M. Shang, and A. Khaligh, “A PSFB based integrated PEV on-board charger with extended ZVS range and zero duty cycle loss,” *IEEE Trans. Industry Applications*. (In Press)
- [133] E. S. Kim, K. Y. Joe, M. H. Kye, Y. H. Kim, and B. D. Yoon, “An improved soft-switching PWM FB dc-dc converter for reducing conduction losses,” *IEEE Trans. Power Electronics*, vol. 14, no. 2, pp. 258-264, Mar. 1999.
- [134] E. S. Kim and Y. Ho. Kim, “A ZVZCS PWM FB dc-dc converter using a modified energy-recovery snubber,” *IEEE Trans. Industrial Electronics*, vol. 49, no. 5, pp. 1120-1127, Oct. 2002.
- [135] H. Cha, L. Chen, R. Ding, Q. Tang, and F. Z. Peng, “An alternative energy recovery clamp circuit for full-Bridge PWM converters with wide ranges of

- input voltage,” *IEEE Trans. Power Electronics*, vol. 23, no. 6, pp. 2828-2837, Nov. 2008.
- [136] J. G. Cho, J. W. Baek, C. Y. Jeong, D. W. Yoo, and K. Y. Joe, “Novel zero-voltage and zero-current-switching full bridge PWM converter using transformer auxiliary winding,” *IEEE Trans. Power Electronics*, vol. 15, no. 2, pp. 250-257, Mar. 2000.
- [137] H. S. Choi, J. W. Kim, and B. H. Cho, “Novel zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converter using coupled output inductor,” *IEEE Trans. Power Electronics*, vol. 17, no. 5, pp. 641-648, Sep. 2002.
- [138] X. Wu, X. Xie, C. Zhao, Z. Qian, and R. Zhao, “Low voltage and current stress ZVZCS full-bridge dc-dc converter using center tapped rectifier reset,” *IEEE Trans. Industrial Electronics*, vol. 55, no. 3, pp. 1470-1477, Mar. 2008.
- [139] B. Gu, J. S. Lai, N. Kees, and C. Zheng, “Hybrid-switching full-bridge dc-dc converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers,” *IEEE Trans. Power Electronics*, vol. 28, no. 3, pp. 1132-1144, Mar. 2013.
- [140] I. O. Lee, “Hybrid PWM-resonant converter for electric vehicle on-board battery chargers,” *IEEE Trans. Power Electronics*, vol. 31, no. 5, pp. 3639-3649, May 2016.
- [141] I. D. Jitaru, “A 3 kW soft-switching dc-dc converter,” in *Proc. 15th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2000, pp. 86-92.
- [142] W. Song and B. Lehman, “Current-fed dual-bridge dc-dc converter,” *IEEE Trans. Power Electronics*, vol. 22, no. 2, pp. 461-469, Mar. 2007.
- [143] H. K. Yoon, S. K. Han, E. S. Choi, G. W. Moon, and M. J. Youn, “Zero-voltage switching and soft-commutating two-transformer full-bridge PWM

- converter using the voltage-ripple,” *IEEE Trans. Industrial Electronics*, vol. 55, no. 3, pp. 1478-1488, Mar. 2008.
- [144] C. Zhao, X. Wu, and Z. Qian, “Optimum design considerations for soft-switched phase-shift full-bridge converter with primary-side energy storage inductor,” in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, 2008, pp. 366-371.
- [145] C. Zhao, X. Wu, W. Yao, and Z. Qian, “Synchronous rectified soft-switched phase-shift full-bridge converter with primary energy storage inductor,” in *Proc. 23rd IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2008, pp. 581-586.
- [146] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain and A. Bakhshai, “A novel ZVZCS full-bridge dc-dc converter used for electric vehicles,” *IEEE Trans. Power Electronics*, vol. 27, no. 6, pp. 2752-2769, Jun. 2012.
- [147] D. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, “An interleaved ZVS full-bridge dc-dc converter with capacitive output filter for a PHEV charger,” in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2827-2832.
- [148] R. Li, H. Njiende, F. Schafmeister, and P. Ide, “A soft-switching interleaved dc-dc converter with integrated magnetics for high voltage battery charger,” in *Proc. International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1-8.
- [149] L. Sun, Y. Chen, X. Xia, L. Peng, and Y. Kang, “Design and optimization of parallel dc-dc system based on current-driven phase-shift full-bridge converter,” in *Proc. IEEE Applied Power Electronics Conference and Exposition(APEC)*, 2014, pp. 2048-2053.

Chapter 3*

ADFC Full-Bridge DC-DC Converter for PHEV Battery Charging with Reduced Auxiliary Magnetics Requirement

In this chapter, the steady-state operational analysis of auxiliary circuit with the proposed asymmetrical pulse width modulation (APWM) and trailing-edge pulse width modulation (TEPWM) is presented. Then asymmetrical duty cycle frequency control (ADFC) method is explained. The converter circuit parameters design considerations are also discussed. Finally, the experimental results are presented to validate the analysis and performance of the converter with the proposed PWM methods.

*Some content of this chapter is published substantially as V. R. K. Kanamarlapudi and P. L. So, "Analysis and implementation of pulse-width modulated dc-dc converter for electric vehicles with improved efficiency," in *Proc. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2016, pp. 1-6.

3.1 ADFC ZVZCS Full-Bridge DC-DC Converter

Figure 3.1 ZVZCS FB dc-dc converter with auxiliary inductor at both legs [1].

Figure 3.2 Theoretical operational waveforms of the auxiliary circuit with APWM.

Figure 3.3 Theoretical operational waveforms of the auxiliary circuit with TEPWM.

The passive auxiliary circuit assisted ZVZCS FB dc-dc converter is shown in Figure 3.1 [1]. The proposed asymmetrical pulse-width modulation (APWM) and trailing-edge pulse-width modulation (TEPWM) gating techniques are shown in Figures 3.2 and 3.3 respectively.

In APWM, the phase-shift between the gating signals of leading leg and lagging leg is fixed at 180° . The high-side switches/low-side switches are gated with a duty cycle D and their complementary signals are given to the low-side switches/high-side switches respectively. In TEPWM, the low-side switches/high-side switches are operated with a duty cycle of 50% and the high-side switches/low-side switches

are operated with a duty cycle D respectively. In Figures 3.2 and 3.3, the dotted-line gating signals represent the duty cycle control of low-side switches, and solid-line gating signals represent the duty cycle control of high-side switches, i.e., the output voltage of the FB converter is regulated through the duty cycle control of the switches.

All these control techniques result in similar controlled auxiliary circuit current by controlling the auxiliary capacitor voltages V_{ca1} - V_{ca4} . Therefore, the operational analysis of the auxiliary circuit using only the APWM with high-side switches S_1 & S_3 duty cycle control is presented here. The same analysis is equally valid for the other control methods.

3.1.1 Asymmetrical Duty Cycle Frequency Control

In the asymmetrical duty cycle frequency control (ADFC) method, the APWM is combined with variable operating switching frequency. The switching frequency is varied to optimally control the peak current value of two auxiliary inductors without losing ZVS. This approach increases the efficiency of the FB converter by reducing the switching loss, conduction loss, circulating loss, and auxiliary circuit losses. The power losses are mainly dependent on load current and switching frequency. The corresponding analytical equations are given in *Section 3.4*. The optimal switching frequency is also calculated using the loss analysis of the converter presented in *Section 3.4*.

3.2 Steady-state Analysis of Auxiliary Circuit

The steady-state analysis of the auxiliary circuit is explained in this section with reference to Figure 3.1. The following assumptions are considered for ease of analysis:

1. Equivalent capacitance across primary active switches is same $C_1 = C_2 = C_3 = C_4 = C$;
2. $C_{a1} = C_{a2} = C_{a3} = C_{a4} = C_a$ are large enough such that V_{ca1} , V_{ca2} , V_{ca3} , V_{ca4} are constant during the switching period;
3. Resistance and winding capacitance of T_r , L_{se} , L_{a1} and L_{a2} are neglected;
4. $L_{a1} = L_{a2} = L_a$ as symmetrical auxiliary circuit is required.

The theoretical waveforms of the voltage across auxiliary inductors and the current through auxiliary inductors are shown in Figure 3.2. The peak current value of two auxiliary inductors I_{La1P} , I_{La2P} with APWM is calculated from auxiliary capacitor voltages V_{ca1} and V_{ca2} , V_{ca3} and V_{ca4} respectively. In the converter, the dc input voltage V_{in} is split across C_{a1} and C_{a2} , C_{a3} and C_{a4} . So, $V_{ca1} + V_{ca2} = V_{in}$ and $V_{ca3} + V_{ca4} = V_{in}$. Under steady-state condition, using the voltage-time balance of auxiliary inductors,

$$V_{ca1}DT_s = (1-D)T_s V_{ca2}; V_{ca3}DT_s = (1-D)T_s V_{ca4} \quad (3.1)$$

The voltage across L_{a1} , L_{a2} during positive half-cycle and negative half-cycle are given by

$$V_{La1}^+ = V_{La2}^+ = V_{ca1} = V_{ca3} = (1-D)V_{in} \quad (3.2)$$

$$V_{La1}^- = V_{La2}^- = -V_{ca2} = -V_{ca4} = -DV_{in} \quad (3.3)$$

Therefore, the peak value of auxiliary inductor currents is given by

$$I_{LaP} = I_{La1P} = I_{La2P} = \frac{V_{in}D(1-D)}{2L_a f_s} \quad (3.4)$$

With the conventional phase-shift modulation (PSM) based control, all switches are operated with a duty cycle of 50% and the output voltage is regulated through the phase-shift between the gating signals of two legs [1]. Therefore, the voltage across

auxiliary inductors and the current through auxiliary inductors when gated with PSM are given by

$$V_{La1}^+ = V_{La2}^+ = V_{ca1} = V_{ca3} = V_{in}/2 \quad (3.5)$$

$$V_{La1}^- = V_{La2}^- = -V_{ca2} = -V_{ca4} = V_{in}/2 \quad (3.6)$$

$$I_{LaP} = I_{La1P} = I_{La2P} = \frac{V_{in}}{8L_a f_s} \quad (3.7)$$

Under constant input voltage conditions, it can be inferred from (3.2) and (3.3) that the voltage across auxiliary capacitors is dependent on the duty cycle of the switches and independent of the switching frequency with APWM/ADFC method. But from (3.5) and (3.6), the voltage across auxiliary capacitors is independent of the duty cycle or phase-shift and the switching frequency with PSM. The comparison of V_{ca1} and V_{ca2} with APWM/ADFC and PSM is shown in Figure 3.4.

Figure 3.4 Comparison of voltage across auxiliary capacitors with APWM/ADFC and PSM.

Under constant input voltage conditions, it can be inferred from (3.4) that the peak value of auxiliary inductors current is dependent on the duty cycle of the switches and the switching frequency with APWM/ADFC methods. But from (3.7), the peak

current value of auxiliary inductors is dependent on switching frequency with PSM method. The comparison of I_{LaP} with APWM and PSM under variable switching frequency for similar auxiliary inductances is shown in Figure 3.5. The controlled auxiliary inductor current with APWM combined with variable operating frequency increases the efficiency of the converter.

Figure 3.5 Comparison of peak value of auxiliary inductor's current with APWM and PSM under variable switching frequency.

Table 3.1 Design specifications of the ADFC converter

Parameter	Value
Input DC voltage	300V
Output DC voltage range	209V - 350V
Maximum output DC current	3.75A
Maximum output power	1.2 kW
Switching frequency	60 kHz – 220 kHz
Output voltage ripple	$< 3.5V_{pk-pk}$
Auxiliary capacitors voltage ripple	$< 6V_{pk-pk}$

Figure 3.6 Lithium-ion battery charging profile.

Table 3.2 Load points in Li-ion battery charging profile

Parameter	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}
V_{bat} [V]	209	240	260	280	320	320	320	320	320	320
I_{bat} [A]	3.75	3.75	3.75	3.75	3.75	3	2.25	1.5	0.8	0.375
R_{ebat} [Ω]	55.73	64	69.3	74.6	85.3	106.67	142.22	213.33	400	853.33
P_o [kW]	0.78	0.9	0.975	1.05	1.2	0.96	0.72	0.48	0.25	0.12

3.3 Circuit Parameters Design

The specification details of the converter for the main circuit parameters design are given in Table 3.1. The load characteristic of lithium-ion battery charging profile is shown in Figure 3.6. The voltage limits of the battery are based on Ford C-Max Hybrid EV battery specifications [2]. Different load points $P_1 - P_{10}$ are highlighted for verifying the performance of the converter and also given in Table 3.2.

3.3.1 Transformer Turns Ratio

The main power transformer T_r turns ratio n is designed for maximum output voltage at maximum duty cycle ratio of 0.95 which is given by

$$n = \frac{V_{omax}}{D_{max} V_{in}} = 1.23 \quad (3.8)$$

3.3.2 Series Inductor

The series inductance is estimated to ensure the critical conduction mode of the converter at the full-load condition at the corresponding operating switching frequency f_{smax} . The full-load condition corresponds to CC mode to CV mode transition point P_5 as shown in Figure 3.6. Therefore, the series inductance value is calculated as follows:

In case of ADFC FB ZVZCS FB dc-dc converter, the maximum operating switching frequency is 220 kHz. Therefore,

$$L_{se} = \left(1 - \frac{V_o}{nV_{in}}\right) \frac{V_o^2}{4n^2 f_{smax} P_o} = 8.5 \mu H \quad (3.9)$$

In case of APWM FB ZVZCS FB dc-dc converter, the operating switching frequency is fixed at 100 kHz. Therefore,

$$L_{se} = \left(1 - \frac{V_o}{nV_{in}}\right) \frac{V_o^2}{4n^2 f_s P_o} = 18.7 \mu H \quad (3.10)$$

3.3.3 Auxiliary Inductors

In this section, the design considerations to determine the value of auxiliary inductance L_a with the proposed APWM and ADFC methods and with the PSM method are discussed.

The auxiliary inductance should be selected to ensure that the available reactive energy during switching transitions guarantees ZVS for all MOSFETs over the battery charging range of the converter. It is assumed that the auxiliary inductor L_a acts as a constant current source during t_d with a magnitude of I_{Lap} . This current charges and discharges the capacitor C_2 and C_3 during switching transition.

Figure 3.7 Load points versus V_{C2} at different auxiliary inductance values with APWM.

Figure 3.8 Load points versus V_{C2} at different auxiliary inductance values with ADFC.

By using (3.11), the variation of voltage across capacitor C_2 during positive power to negative power transition on load conditions $P_1 - P_{10}$ at different auxiliary inductances is shown in Figure 3.7 for APWM gating technique. In APWM, the switching frequency is fixed at 100 kHz. To ensure ZVS, the capacitor voltage V_{C2} should be greater than the DC input voltage V_{in} over the entire battery charging

range within $t_d=300\text{ns}$. According to Figure 3.7, the voltage V_{C2} is minimum at the load point P_{I0} .

$$v_{C2}(t) = \frac{I_{LaP}}{2C}(t - t_4) = \frac{V_{in}D(1-D)}{4L_a f_s C}(t - t_4) \quad (3.11)$$

Another criterion to select the auxiliary inductance is that the energy balance equation for ZVS transition of switches should be satisfied which is given by

$$\frac{1}{2}L_a I_{LaP}^2 \geq C V_{in}^2 \quad (3.12)$$

Therefore, the condition to select auxiliary inductance from (3.4) and (3.12) is given by

$$L_a \leq \frac{D^2(1-D)^2}{8Cf_s^2} \quad (3.13)$$

Using Figure 3.7 and (3.13), the value of auxiliary inductance with APWM is chosen to be $60\mu\text{H}$.

Similarly, the variation of voltage across capacitor C_2 during positive power to negative power transition on load conditions $P_I - P_{I0}$ at different auxiliary inductances is shown in Figure 3.8 for ADFC gating technique. In ADFC, adaptive frequency control ranging from 60 kHz to 220 kHz is used. According to Figure 3.8, the voltage V_{C2} is minimum at the load point P_4 . Using Figure 3.8 and (3.13), the value of auxiliary inductance with ADFC is chosen to be $55\mu\text{H}$.

In the case of PSM, the auxiliary inductance should be selected such that the peak value of auxiliary inductor current is 3A. The switching frequency is fixed at 100 kHz similar to APWM. Using (3.7) the auxiliary inductance value is chosen to be $125\mu\text{H}$.

3.3.4 Auxiliary Capacitors

To ensure proper operation of the converter, the capacitors C_{a1} , C_{a2} , C_{a3} , and C_{a4} in the passive auxiliary circuit should behave as constant dc voltage sources over a single switching period. The auxiliary capacitances should be selected such that the peak to peak ripple voltage on each capacitor is small at the maximum auxiliary reactive current and the corresponding switching frequency condition. The minimum required capacitance allowing a ripple of $\Delta V_{Ca} = 6V$ is estimated by

$$C_{a1} = C_{a2} = C_{a3} = C_{a4} \geq \frac{V_{in}}{64L_a f_{smin}^2 \Delta V_{Ca}} \geq 4.34\mu F \quad (3.14)$$

Therefore, 4.7 μ F capacitance is selected for the auxiliary capacitors.

3.3.5 Output Filter Capacitor

The output filter capacitor is designed based on the allowable ripple in the output voltage [3]. The minimum filter capacitance required to maintain the voltage ripple within 1% at minimal switching frequency is given by

$$C_f \geq \frac{I_o}{8f_{smin} \Delta V_{cf}} \geq 2.24\mu F \quad (3.15)$$

Therefore, two parallel 2.2 μ F capacitors are selected for output filter capacitor.

3.4 Loss Analysis of Converter

Theoretical loss analysis of the converter is carried out in this section. The loss analysis is useful to optimally select the switching frequency for the improved performance of the converter. The advantage of the proposed ADFC gating method over APWM is also illustrated using this analysis. The key steady-state operating waveforms of the converter for the loss analysis are shown in Figure 3.9. Loss analysis of the main components MOSFETs, rectifier diodes and magnetics in the converter is given in the following sub-sections.

3.4.1 MOSFETs Switching Losses

MOSFETs turn-on switching loss is zero as the converter is designed to achieve ZVS for all active switches throughout the operating range of the converter. The turn-off loss of S_1 and S_3 [4] is given by

$$P_{S1,S3_off} = \frac{(I_{pP} + I_{LaP})^2 t_f^2 f_s}{12C} \quad (3.16)$$

The turn-off loss of S_2 and S_4 is given by

$$P_{S2,S4_off} = \frac{I_{LaP}^2 t_f^2 f_s}{12C} \quad (3.17)$$

where $I_{pP} = \frac{V_o}{2nL_{se}f_s}(\sqrt{D^2 + 4K} - D)$; $K = \frac{n^2 L_{se} f_s}{R_{ebat}}$

3.4.2 MOSFETs Conduction Losses

MOSFETs conduction losses are calculated from main channel and anti-parallel body-diode conduction losses. The main channel loss is calculated using the on-state drain-source resistance and RMS current through the switch.

Figure 3.9 Key steady-state operating waveforms for loss analysis of the converter.

The antiparallel body-diode conduction losses are calculated by the intrinsic diode forward voltage drop and the average diode current. As shown in Figure 3.9, the current through low-side switches and the corresponding body-diodes is the sum of transformer primary current and respective leg auxiliary circuit current. Therefore, the transformer primary current i_p in one-half switching cycle is given by

$$i_p(t) = \begin{cases} \frac{V_{in} - (V_o / n)}{L_{se}} (t - t_0) & t_0 < t < t_3 \\ I_{pP} - \frac{V_o}{nL_{se}} (t - t_3) & t_3 < t < t_4 \\ 0 & t_4 < t < t_5 \end{cases} \quad (3.18)$$

The current through auxiliary inductors i_{La1} , i_{La2} in one switching is given by

$$i_{La1}(t) = \begin{cases} -I_{La1P} + \frac{V_{in}(1-D)}{L_{a1}} (t - t_0) & t_0 < t < t_3 \\ I_{La1P} - \frac{V_{in}D}{L_{a1}} (t - DT_s) & t_3 < t < t_{10} \end{cases} \quad (3.19)$$

$$i_{La2}(t) = \begin{cases} -I_{La2P} + \frac{V_{in}(1-D)}{L_{a2}} (t - \frac{T_s}{2}) & t_5 < t < t_8 \\ I_{La2P} - \frac{V_{in}D}{L_{a2}} (t - \frac{T_s}{2} - DT_s) & t_8 > t < t_5 \end{cases} \quad (3.20)$$

The high-side switch's body-diode conduction loss is given by

$$P_{DS1,DS3_cond} = 2V_{SD} (f_s \int_{t_0}^{t_2} (i_p(t) + i_{La1}(t)) dt) \quad (3.21)$$

The high-side switch's conduction loss is given by

$$P_{S1,S3_cond} = 2(f_s \int_{t_2}^{t_3} (i_p(t) + i_{La1}(t))^2 dt) R_{ds(on)} \quad (3.22)$$

The total high-side MOSFET's conduction loss is given by

$$P_{MOS_Low-side_cond} = P_{DS1,DS3_cond} + P_{S1,S3_cond} \quad (3.23)$$

The low-side switches body-diode conduction losses are given by

$$P_{DS4,DS2_cond} = 2V_{SD} (f_s \int_{t_3}^{t_6} (i_p(t) + i_{La1}(t)) dt) \quad (3.24)$$

The low-side switch's conduction loss is given by

$$P_{S4,S2_cond} = 2(f_s \int_{t_6}^{t_{10}} (i_p(t) + i_{La1}(t))^2 dt) R_{ds(on)} \quad (3.25)$$

The total low-side MOSFET's conduction loss is given by

$$P_{MOS_High-side_cond} = P_{DS4,DS2_cond} + P_{S4,S2_cond} \quad (3.26)$$

The MOSFET's total conduction loss is given by

$$P_{MOS_cond} = P_{MOS_High-side_cond} + P_{MOS_Low-side_cond} \quad (3.27)$$

3.4.3 Gate Driver Losses

The gate driver loss [5] is the power dissipated due to the charging and discharge of the gate capacitance of MOSFET which is given by

$$P_{gdr} = 4C_g V_{dr}^2 f_s = 4Q_{gtot} V_{dr} f_s \quad (3.28)$$

where Q_{gtot} is the total gate charge of MOSFET, C_g is the gate capacitance, and V_{dr} is the MOSFET gate drive voltage value.

3.4.4 Rectifier Diodes Switching and Conduction Losses

The rectifier diode current i_D waveform from Figure 3.9 infers that they are naturally commutated with zero current when the current through series inductor current is zero as the converter is operated in DCM. This condition eliminates the reverse-recovery and switching losses in output rectifier diodes. The rectifier diode conduction losses are calculated by the intrinsic diode forward voltage drop and the average diode current which is given by

$$P_{D1,D2,D3,D4_cond} = 2V_F I_o \quad (3.29)$$

3.4.5 Transformer and Series Inductor Core and Winding Losses

The approximated piece-wise linear magnetic flux density waveform of the transformer and series inductor is shown in Figure 3.10(a).

Figure 3.10 Flux density waveforms. (a) Transformer. (b) Auxiliary inductor.

The core loss per unit volume of the transformer and series inductor using the improved general steinmetz equation (iGSE) [6] is given by

$$P_{v_Tr,Lse} = \frac{2K_i |\Delta B|^\beta}{T_s^\alpha} (D^{1-\alpha} + ((\frac{nV_{in}}{V_o} - 1)D)^{1-\alpha}) \quad (3.30)$$

where
$$K_i = \frac{K_c}{2^{\beta-1} \pi^{\alpha-1} (1.1044 + \frac{6.8244}{\alpha + 1.354})}$$

The peak magnetic flux density of the transformer is calculated from

$$\Delta B_{Tr} = \frac{DV_{in}}{f_s N_{p_Tr} A_{ce_Tr}} \quad (3.31)$$

The peak magnetic flux density the of series inductor is calculated from

$$\Delta B_{Lse} = \frac{V_o}{2nf_s N_{Lse} A_{ce_Lse}} (\sqrt{D^2 + 4K} - D) \quad (3.32)$$

The primary and secondary winding losses of the transformer and series inductor are calculated by using i_p waveform shown in Figure 3.9. The winding loss in the transformer is given by (3.33).

$$P_{cu_Tr} = \frac{2nDV_{in}I_{pP}^2}{3V_o} \left(R_{pri} + \frac{R_{sec}}{n^2} \right) \quad (3.33)$$

The winding losses in the series inductor is given by

$$P_{cu_Lse} = \frac{2nDV_{in}I_{pP}^2 R_{Lse}}{3V_o} \quad (3.34)$$

3.4.6 Auxiliary Inductors Core and Winding Losses

The approximated piece-wise linear magnetic flux density waveform of the auxiliary inductors is shown in Figure 3.10(b) where the flux density swings from $+\Delta B_{La}$ to $-\Delta B_{La}$. The core loss per unit volume of auxiliary inductors using iGSE is given by

$$P_{v_La} = \frac{2K_i |2\Delta B|^\beta}{T_s^\alpha} (D^{1-\alpha} + (1-D)^{1-\alpha}) \quad (3.35)$$

The winding loss in the auxiliary inductors is given by

$$P_{cu_La} = \frac{2I_{LaP}^2 R_{La}}{3} \quad (3.36)$$

Table 3.3 Optimal switching frequency details for converter

Parameter	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}
V_{bat} [V]	209	240	260	280	320	320	320	320	320	320
I_{bat} [A]	3.75	3.75	3.75	3.75	3.75	3	2.25	1.5	0.8	0.375
P_o [kW]	0.78	0.9	0.975	1.05	1.2	0.96	0.72	0.48	0.25	0.12
f_{sopt} (kHz)	100	130	150	180	220	210	190	160	110	60

3.4.6 Loss Analysis Results

The optimal switching frequency f_{sopt} is estimated such that the total losses are minimal over the battery charging profile range using the loss analysis presented in

Section 3.4.1 to Section 3.4.5. The determined switching frequency values at load points $P_1 - P_{10}$ are given in Table 3.3.

The peak current value of auxiliary inductors is calculated for the ADFC, APWM and PSM techniques and the results are compared in Figure 3.11. It can be seen from Figure 3.11 that the peak current value of auxiliary inductors with ADFC is less than that with APWM which results in reduced losses of the converter. It is equal to the peak current value of the auxiliary inductors with PSM. It can also be deduced that the required auxiliary inductance to ensure ZVS with ADFC is reduced approximately by a factor of 2.3 compared to PSM.

Figure 3.11 Peak value of auxiliary inductor's current with ADFC, APWM and PSM.

The comparison of the power losses of FB converter with PSM ($L_{a1} = L_{a2} = 60\mu H$ and $125\mu H$), APWM ($L_{a1} = L_{a2} = 60\mu H$), and ADFC ($L_{a1} = L_{a2} = 55\mu H$) gating techniques during CC charging mode and CV charging mode is shown in Figure 3.12. The losses are categorized into MOSFET's switching loss (turn-off loss), MOSFET's conduction loss, MOSFET's gate driver loss, rectifier diode's loss, high frequency transformer loss (core and winding losses) and series inductor loss (core and winding losses), and auxiliary inductor's loss (core and winding losses).

The corresponding losses are depicted in the bar-graphs as shown in Figure 3.12.

The following conclusions are drawn from the power loss analysis.

- ✓ The efficiency of the APWM FB converter with $L_a = 60\mu\text{H}$ is better than that of the PSM FB converter with same auxiliary inductors.
- ✓ Auxiliary inductor required to ensure ZVS with ADFC ($L_a = 55\mu\text{H}$) is reduced by a factor close to 2.3 compared to PSM ($L_a = 125\mu\text{H}$) without compromising on overall efficiency of the converter.
- ✓ The overall efficiency of ADFC FB converter with $L_a = 55\mu\text{H}$ is better than that of APWM FB converter with $L_a = 60\mu\text{H}$.
- ✓ The overall efficiency of ADFC FB converter with $L_a = 55\mu\text{H}$ is the same as PSM FB converter with $L_a = 125\mu\text{H}$.

The above conclusions are further verified with the experimental results presented in the following section.

Figure 3.12 Comparison of converter power losses with PSM, APWM and ADFC. (a) CC mode. (b) CV mode.

Table 3.4 Component list of ADFC converter

MOSFET Switches	IXFN60N80P
Rectifier diodes (D_1 – D_4)	C4D10120D
Main transformer (T_r)	E65 – 3C95, n: 1.23, Leakage inductance: 2μH
Series inductor (L_{se})	E32 – N87, 16.7μH (APWM), 6.5μH (ADFC)
Auxiliary inductors (L_{a1} , L_{a2})	RM12 – N97, 55μH (ADFC), 60μH (APWM, PSM), 125μH (PSM)
Auxiliary capacitors (C_{a1} , C_{a2} , C_{a3} , C_{a4})	4.7μF/300V
Output filter capacitor (C_f)	4.4μF/630V

Figure 3.13 Prototype of ZVZCS FB dc-dc converter with auxiliary inductor at both legs.

3.5 Experimental Results

A 1.2 kW laboratory converter prototype is developed to verify the advantages of the proposed APWM and ADFC methods compared to the PSM method. The components used in the development of the converter are listed in Table 3.4. The developed prototype is shown in Figure 3.13. The proposed methods are implemented on the TMS320F28335 controller using enhanced pulse-width modulators by the up-down counter method [7].

3.5.1 APWM ZVZCS Full-Bridge DC-DC Converter

The ZVS results for high-side switch S_3 and low-side switch S_4 are shown in Figures 3.14 and 3.15 respectively when gated with APWM at key load points P_1 , P_5 and P_{10} . The drain to source voltage v_{DS} of the switches attains zero before the respective gating signals are applied. This phenomenon confirms the ZVS turn-on of switches S_3 and S_4 with the proposed APWM gating technique.

The experimental results for the inverter output voltage v_{AB} and operating waveforms of T_r primary with the proposed APWM are shown in Figure 3.16. It can be observed from these results that the proposed APWM gating technique results in symmetrical inverter output voltage v_{AB} as discussed earlier.

The experimental results for the voltage across power transformer T_r secondary v_{sec} , and output rectifier diode v_{DI} at key load points P_1 , P_5 and P_{10} are shown in Figure 3.17. It is clearly evident from Figure 3.17 that the high voltage spikes across output rectifier diodes are eliminated due to the current-driven configuration of the converter.

(a)

(b)

(c)

Figure 3.14 ZVS waveforms of S_3 with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

(c)

Figure 3.15 ZVS waveforms of S_4 with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

(c)

Figure 3.16 Operating waveforms of T_r primary with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

(c)

Figure 3.17 Operating waveforms of T_r secondary with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

Figure 3.18 Auxiliary circuit waveforms with PSM ($L_a = 60\mu\text{H}$). (a) Auxiliary capacitor voltages. (b) Auxiliary inductors voltage and current.

(a)

(b)

(c)

Figure 3.19 Auxiliary circuit waveforms with APWM. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

The experimental results of the PSM auxiliary circuit are shown in Figure 3.18. In this case, the auxiliary capacitors voltage is 150V as the duty cycle of the switches is fixed at 50%. Therefore, it results in same auxiliary inductor peak current at all load conditions. The duty cycle dependent auxiliary capacitors voltage V_{Ca1} , V_{Ca2} with the proposed APWM technique at key load points P_1 , P_5 and P_{10} are shown Figure 3.19. The corresponding results of the controlled auxiliary inductor voltage v_{La1} and current i_{La1} results are also shown in Figure 3.19. The controlled auxiliary circuit current results in reduced switching, conduction and auxiliary circuit losses

in the converter thereby improving the efficiency when compared to PSM with similar auxiliary inductances. It is verified using efficiency comparison results of the converter with proposed gating techniques as shown in Figure 3.20(a) during CC charging mode and in Figure 3.20(b) during CV charging mode.

Figure 3.20 Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.

3.5.2 ADFC ZVZCS Full-Bridge DC-DC Converter

The experimental results are presented at key load points P_1 , P_5 and P_{10} for ADFC FB dc-dc converter. As discussed in *Section 3.3.3*, auxiliary inductances of $55\mu\text{H}$ are used for ADFC FB dc-dc converter. From loss analysis in *Section 3.4*, the optimal switching frequencies are calculated to be 100 kHz, 220 kHz and 60 kHz at the load conditions corresponding to P_1 , P_5 and P_{10} respectively.

The ZVS results for high-side switch S_3 and low-side switch S_4 are shown in Figures 3.21 and 3.22 respectively when gated with ADFC. The drain to source voltage v_{DS} of the switches attains zero before the respective gating signals are applied. This phenomenon confirms the ZVS turn-on of switches S_3 and S_4 with the proposed ADFC gating technique.

The experimental results for the symmetrical inverter output voltage v_{AB} and operating waveforms of T_r primary with the proposed ADFC and the corresponding optimal switching frequency are shown in Figure 3.23. The experimental results for the voltage across T_r secondary v_{sec} , and output rectifier diode v_{DI} at key load points P_1 , P_5 and P_{10} are shown in Figure 3.24. It is clearly evident from Figure 3.24 that the high voltage spikes across output rectifier diodes are eliminated due to the current-driven configuration of the converter.

The experimental results of the PSM auxiliary circuit with $L_{a1} = L_{a2} = L_a = 125\mu\text{H}$ are shown in Figure 3.25. The PSM FB converter is operated at a fixed switching frequency of 100 kHz. In this case, the auxiliary capacitors voltage is 150V as the duty cycle of the switches is fixed at 50%. Therefore, it results in same auxiliary inductor peak current at all load conditions.

(a)

(b)

(c)

Figure 3.21 ZVS waveforms of S_3 with ADFC. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

(c)

Figure 3.22 ZVS waveforms of S_4 with ADFC. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

Auxiliary inductors of $L_{a1} = L_{a2} = L_a = 55\mu\text{H}$ are used in ADFC FB dc-dc converter. The duty cycle dependent auxiliary capacitors voltage V_{Ca1} , V_{Ca2} results with the proposed ADFC technique at key load points P_1 , P_5 and P_{10} are shown Figure 3.26. The duty cycle controlled auxiliary inductor voltage v_{La1} , and the duty cycle and frequency controlled auxiliary inductor current i_{La1} results are also shown in Figure 3.26.

Figure 27 shows the efficiency of the converter over the battery charging profile under following scenarios:

1. APWM FB converter without auxiliary circuit (conventional converter);
2. PSM FB converter with auxiliary circuit, $L_{a1} = L_{a2} = L_a = 60\mu\text{H}$;
3. APWM FB converter with auxiliary circuit, $L_{a1} = L_{a2} = L_a = 60\mu\text{H}$;
4. PSM FB converter with auxiliary circuit, $L_{a1} = L_{a2} = L_a = 125\mu\text{H}$;
5. ADFC FB converter with auxiliary circuit, $L_{a1} = L_{a2} = L_a = 55\mu\text{H}$.

(a)

(b)

(c)

Figure 3.23 Operating waveforms of T_r primary with ADFC. (a) At load point P_1 (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

(a)

(b)

(c)

Figure 3.24 Operating waveforms of T_r secondary with ADFC. (a) At load point P_I (209V, 3.75A). (b) At load point P_5 (320V, 3.75A). (c) At load point P_{I0} (320V, 0.375A).

(a)

(b)

Figure 3.25 Auxiliary circuit waveforms with PSM ($L_a = 125\mu\text{H}$). (a) Auxiliary capacitor voltages. (b) Auxiliary inductors voltage and current.

(a)

(b)

(c)

Figure 3.26 Auxiliary circuit waveforms with ADFC. (a) At load point P_1 (209V, 3.75A).
 (b) At load point P_5 (320V, 3.75A). (c) At load point P_{10} (320V, 0.375A).

3.5.3 Comparative Analysis

The efficiency comparison between proposed ADFC and other gating techniques for converter with auxiliary circuit, and converter without auxiliary circuit are shown in Figure 3.27 and Table 3.5. From these results, it is observed that

- The efficiency of the APWM FB converter with $L_a = 60\mu\text{H}$ is greater than that of the PSM FB converter with same auxiliary inductors;
- The efficiency of the ADFC FB converter with $L_a = 55\mu\text{H}$ is greater than that of the APWM FB converter with $L_a = 60\mu\text{H}$ at light-load conditions (CV charging mode);
- The overall efficiency of the ADFC FB converter with $L_a = 55\mu\text{H}$ is the same as the PSM FB converter with $L_a = 125\mu\text{H}$.

Figure 3.27 Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.

Table 3.5 Efficiency comparison of converter with PSM, APWM and ADFC

Load point	Theoretical η (%)				Practical η (%)			
	PSM (60 μ H)	APWM (60 μ H)	PSM (125 μ H)	ADFC (55 μ H)	PSM (60 μ H)	APWM (60 μ H)	PSM (125 μ H)	ADFC (55 μ H)
P ₁	91.58	94.36	93.72	93.43	89.91	91.52	91.21	90.56
P ₂	93.06	94.95	94.48	94.55	90.46	92.43	91.91	92.60
P ₃	93.9	95.26	94.86	95.11	91.66	92.79	92.00	92.72
P ₄	94.64	95.5	95.14	95.64	92.82	93.29	92.91	93.69
P ₅	95.26	95.31	95.18	96.23	94.5	94.17	94.36	93.87
P ₆	95.02	95.27	95.09	96.16	94.04	92.98	93.24	93.15
P ₇	94.3	95.11	94.89	96.02	92.12	92.6	92.50	92.92
P ₈	92.33	94.75	94.37	95.76	88.65	90.65	89.73	91.15
P ₉	86.01	94.06	92.68	95.14	78.4	87.68	83.26	87.68
P ₁₀	72.88	93.25	88.19	93.78	62.64	80.86	72.43	81.39

Table 3.6 Comparison of FB dc-dc converters

Converter topology	Topology in [8]	Topology in [1]		
Modulation method	TEPWM	PSM [1]	Proposed APWM	Proposed ADFC
Switching frequency	100 kHz	100 kHz	100 kHz	60kHz – 220kHz
Series inductance	18.7 μ H	18.7 μ H	18.7 μ H	8.5 μ H
Auxiliary inductors size (volt-second)	Not applicable	$\frac{V_{in}}{8} \frac{1}{f_s}$	$\frac{V_{in}}{2} \frac{D_{min}(1-D_{min})}{f_s}$	$\frac{V_{in}}{2} \frac{D(1-D)}{f_{sopt}}$
Auxiliary circuit peak current rating	Not applicable	$\frac{V_{in}}{8L_a f_s}$	$\frac{V_{in}D(1-D)}{2L_a f_s}$	$\frac{V_{in}D(1-D)}{2L_a f_{sopt}}$
Auxiliary inductances	Not applicable	125 μ H	60 μ H	55 μ H
ZVS	Two switches (S_2, S_4)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)
ZCS	Two switches (S_2, S_4)	Two switches (S_1, S_4) – near ZCS	Two switches (S_2, S_4) – near ZCS	Two switches (S_2, S_4) – near ZCS

The comparative advantages of the proposed ADFC gating technique and the converter are highlighted in Table 3.6. From this table, theoretical analysis and

experimental results, it can be confirmed that the auxiliary inductance required to ensure ZVS with ADFC ($L_a = 55\mu\text{H}$) is reduced by a factor close to 2.3 compared to PSM ($L_a = 125\mu\text{H}$) without compromising on overall efficiency of the converter.

3.6 Conclusion

In this chapter, APWM, TEPWM and ADFC gating techniques have been proposed. Steady-state analysis of the auxiliary circuit in converter has been explained with the proposed gating techniques. The design considerations for circuit parameters design have been discussed. Theoretical comparative power loss analysis of the converter with the proposed APWM, ADFC and PSM gating techniques has been presented. ZVS and auxiliary circuit results from 1.2 kW laboratory converter type have validated the analysis of the converter. The experimental efficiency results have confirmed the advantage of the proposed gating techniques over the conventional PSM technique for the ZVZCS FB dc-dc converter with auxiliary inductor at both legs.

References

- [1] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, "A novel ZVZCS full-bridge DC-DC converter used for electric vehicles," *IEEE Trans. Power Electronics*, vol. 27, no. 6, pp. 2752-2769, Jun. 2012.
- [2] Ford C-Max8698 Hybrid – 2013, Advanced vehicle testing activity – HEV battery testing results, Idaho National Laboratory [Online]. Available: <http://energy.gov/sites/prod/files/2015/02/f19/batteryC-Max8698.pdf>.
- [3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd edition. Kluwer, 2001.
- [4] Turn-off snubber design for high frequency modules, Advanced Power Technology, Europe [Online]. Available: <http://www.microsemi.com>.

- [5] Z. Chen, S. Liu, L. Shi, and F. Ji, "Power loss analysis and comparison of two full-bridge converters with auxiliary networks," *IET Power Electronics*, vol. 5, no. 9, pp. 1934-1943, Nov. 2012.
- [6] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. Wiley, 2013.
- [7] Texas Instruments, "TMS320×2833, 2823× enhanced pulse-width modulator (ePWM) module," SPRUG04A, Oct. 2008 (Revised Jul. 2009).
- [8] D. S. Gautam, F. Musavi, W. Eberle, and W. G. Dunford, "A zero-voltage switching full-bridge DC-DC converter with capacitive output filter for plug-in hybrid electric vehicle battery charging," *IEEE Trans. Power Electronics*, vol. 28, no. 12, pp. 5728-5735, Dec. 2013.

Chapter 4*

APWM ZVS Full-Bridge DC-DC Converter for PHEV Battery Charging

In this chapter, a new zero-voltage switching full-bridge dc-dc converter for PHEV battery charger is proposed. The steady-state analysis of the converter is explained in detail with time intervals and respective governing analytical equations are provided. Experimental results on a 100 kHz, 1.2 kW converter prototype are presented to validate the performance of the proposed converter.

*Some content of this chapter is published substantially as V. R. K. Kanamarlaudi, B. F. Wang, K. N. Kumar and P. L. So, "A new ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range," in *Proc. IEEE India International Conference (INDICON)*, New Delhi, 2015, pp. 1-6.

4.1 APWM ZVS Full-Bridge DC-DC Converter Topology

Figure 4.1 Proposed APWM ZVS FB dc-dc converter. (a) Topology. (b) APWM gating technique.

The proposed ZVS full-bridge dc-dc converter topology is shown in Figure 4.1(a) and the APWM gating technique proposed in *Chapter 3* is shown in Figure 4.1(b). In this converter, the auxiliary circuit is comprised of one auxiliary transformer T_a , one auxiliary inductor L_a and two auxiliary capacitors C_{a1} , C_{a2} to achieve ZVS, and two clamping diodes D_{a1} , D_{a2} to mitigate the voltage spikes across output rectifier diodes.

4.2 Operating Principle of Converter

The steady-state analysis of the proposed APWM ZVS FB dc-dc converter over the operating range is explained in this section. The following assumptions are considered:

1. The switching elements are ideal;
2. Resistance and inter-winding capacitance of the main power transformer T_r and auxiliary transformer T_a are neglected;
3. Magnetizing inductance of both the transformers T_r and T_a is very high such that the magnetizing current is neglected;
4. Resistance and inter-winding capacitance of the series inductor and auxiliary inductor are neglected;
5. Equivalent capacitance across active switches is the same $C_1 = C_2 = C_3 = C_4 = C$;
6. $C_{a1} = C_{a2} = C_a$ are large enough such that V_{ca1} and V_{ca2} are constant during the switching period;
7. The filter inductor L_f is large enough such that the output current is constant;
8. C_f is large enough to assume that the output voltage is constant.

The proposed converter topology combined with APWM ensures ZVS for all main switches, reduced circulating and conduction losses over the operating range. In addition, the clamping diodes minimize the voltage spikes across output rectifier diodes. These phenomena can be explained through the operational analysis of the converter. The operation of the ZVS FB converter with APWM is divided into fourteen time intervals and the theoretical operational waveforms are shown in Figure 4.2. The time intervals are explained in detail and the respective governing analytical equations are provided as follows:

Figure 4.2 Theoretical operational waveforms of the converter with APWM.

Interval I ($t_0 < t \leq t_1$):

Figure 4.3 Interval I.

In this interval, the power is transferred from input source V_{in} to the load through the main switches S_1 and S_2 , and output rectifier diodes D_1 and D_2 as shown in Figure 4.3. During this interval,

$$v_{AB}(t) = V_{in}; v_{Tap}(t) = v_{Tas}(t) = \frac{V_{in}}{2} \quad (4.1)$$

$$i_{Lse}(t) = i_p(t) = nI_o \quad (4.2)$$

$$i_{La}(t) = I_{La}(t_0) + \frac{V_{in}(1-D)}{2L_a}(t-t_0) \quad (4.3)$$

$$i_{S1}(t) = nI_o + \frac{I_{LaP}}{4}; i_{S2}(t) = nI_o - \frac{I_{LaP}}{4} \quad (4.4)$$

where V_{in} is the input voltage, v_{AB} is the inverter output voltage, v_{Tap} and v_{Tas} are the voltages across the primary and secondary of T_a , i_{Lse} and i_p are the series inductor, and T_r primary currents respectively, I_o is the load current, I_{LaP} is the peak value of auxiliary inductor current, and i_{S1} and i_{S2} are S_1 and S_2 currents respectively. This interval ends when the gating signal to the main switch S_1 is turned off.

Interval II ($t_1 < t \leq t_2$):

Figure 4.4 Interval II.

When S_1 is turned off at t_1 , the current through the primary of the transformer i_p which was initially flowing through S_1 will now discharge C_4 and charge C_1 simultaneously as given by (4.5) and (4.6). The discharging of C_4 will also result in equal decay of v_{AB} . The output diodes D_1 and D_2 continue to conduct the load current I_o . S_1 is turned off with zero-voltage as the capacitors C_1 and C_4 limit the rising rate of voltage across S_1 . By the end of this interval, the capacitor C_4 is discharged completely and its body-diode D_{S4} becomes forward biased. The conduction of the body diode D_{S4} ensures ZVS turn-on for S_4 . The currents i_p and i_{La} can be considered constant as it is short time interval. The circuit conditions during this interval are shown in Figure 4.4.

$$v_{C4}(t) = V_s - \frac{1}{2C} (nI_o + \frac{I_{LaP}}{2})(t - t_1) \quad (4.5)$$

$$v_{C1}(t) = \frac{1}{2C} (nI_o + \frac{I_{LaP}}{2})(t - t_1) \quad (4.6)$$

The above equations also imply that the ZVS for low-side switch S_4 can be easily achieved because the total magnitude of discharging current at t_1 is more compared

to conventional ZVS FB converter. However, the passive auxiliary circuit results in extra conduction loss.

Interval III ($t_2 < t \leq t_3$):

Figure 4.5 Interval III.

In this interval, the reflected load current nI_o plus the auxiliary current i_{La} freewheel through the body-diode D_{S4} , and the reflected load current nI_o freewheels through the main switch S_2 . The voltage V_{AB} and T_r secondary voltage are zero, and the output rectifier diodes D_1 and D_2 continue to conduct the load current. The currents i_{Lse} and i_p are unchanged as the series inductor is shorted and D_{a1} is reverse biased in this interval. The circuit conditions during this interval are shown in Figure 4.5. In this interval,

$$i_{La}(t) = I_{La}(t_2) - \frac{DV_{in}}{2L_a}(t - t_2) \quad (4.7)$$

$$i_{DS4}(t) = nI_o + i_{La}(t); i_{S2}(t) = nI_o \quad (4.8)$$

This interval ends when the gating signal to the main switch S_2 is turned off.

Interval IV ($t_3 < t \leq t_4$):

Figure 4.6 Interval IV.

When S_2 is turned off with zero-voltage at t_3 because of C_2 and C_3 , the current $i_p(t_3)$ which was initially flowing through S_2 will now discharge C_3 and charge C_2 simultaneously as given by (4.10) and (4.11). The output rectifier diodes D_3 and D_4 also conduct the load current as the voltage v_{AB} becomes negative during this interval. The primary and secondary voltages of the main transformer T_r and auxiliary transformer T_a are zero as all the output rectifier diodes D_1 - D_4 conduct at the same time. The capacitor C_3 is completely discharged such that the body-diode D_{S3} starts conducting which ensures ZVS turn-on for S_3 by the end of this interval. The auxiliary current also reaches its maximum by the end of this interval but the change in $i_{La}(t)$ can be considered constant as it is a very short time interval. The circuit conditions during this interval are shown in Figure 4.6. During this interval,

$$i_{Lse}(t) = i_p(t) = (nI_o + \frac{I_{LaP}}{2}) \cos \omega_r(t - t_3) - \frac{I_{LaP}}{2} \quad (4.9)$$

$$v_{C3} = V_{in} - (nI_o + \frac{I_{LaP}}{2}) Z_r \sin \omega_r(t - t_3) \quad (4.10)$$

$$v_{C2} = (nI_o + \frac{I_{LaP}}{2})Z_r \sin \omega_r(t - t_3) \quad (4.11)$$

Interval V ($t_4 < t \leq t_5$):

Figure 4.7 Interval V.

At t_4 , the body-diode starts D_{S3} conducting which ensures ZVS turn-on for S_3 . The output rectifier diodes D_1 - D_4 continue to conduct during this interval, i.e., the primary and secondary voltages of the main transformer T_r and auxiliary transformer T_a are also zero. The clamping diode D_{a1} starts conducting and eliminates the voltage oscillation during this interval as the input voltage is fully applied on L_{se} . Therefore, the current i_{Lse} decays linearly. The current through D_{a1} is the difference between i_{Lse} and i_p . The circuit conditions during this interval are shown in Figure 4.7. This interval ends when i_{Lse} and i_p are equal and D_{a1} turns off naturally. During this interval,

$$i_{Lse}(t) = i_{Lse}(t_4) - \frac{V_{in}}{L_{se}}(t - t_4) \quad (4.12)$$

Interval VI ($t_5 < t \leq t_6$):

Figure 4.8 Interval VI.

D_{a1} turns off naturally at t_5 . In this interval, the T_r secondary voltage is zero as the output rectifier diodes D_1 - D_4 continue to conduct. The circuit conditions during this interval are shown in Figure 4.8. V_{in} is fully applied on L_{se} which causes i_{Lse} and i_p to decay linearly as given by

$$i_{Lse}(t) = i_p(t) = i_{Lse}(t_5) - \frac{V_{in}}{L_{se}}(t - t_5) \quad (4.13)$$

The body-diode ceases to conduct by the end of this interval as i_p decays to zero.

Interval VII ($t_6 < t \leq t_7$):

In this interval, i_p continues to increase in the negative direction which flows through S_3 and S_4 . The output rectifier diodes D_1 - D_4 continue to conduct as i_p is not sufficient to provide the load demand which implies that the T_r secondary voltage is zero during this interval. The circuit conditions during this interval are shown in Figure 4.9. The currents i_{Lse} and i_p decay linearly and are given by (4.14).

Figure 4.9 Interval VII.

$$i_{Lse}(t) = i_p(t) = -\frac{V_{in}}{L_{se}}(t - t_6) \quad (4.14)$$

This interval ends once the current i_p reaches the negative maximum to supply the required load current. At t_7 , the output rectifier diodes D_1 and D_2 turn-off, and the diodes D_3 and D_4 carry the entire load current.

Interval VIII ($t_7 < t \leq t_8$):

Figure 4.10 Interval VIII.

In this interval, the power is transferred from input source V_{in} to the load through the main switches S_3 and S_4 , and output rectifier diodes D_3 and D_4 as shown in Figure 4.10. During this interval, the currents through S_3 and S_4 are similar to (4.4). This interval ends when the gating signal to the main switch S_3 is turned off.

Interval IX ($t_8 < t \leq t_9$):

Figure 4.11 Interval IX.

When S_3 is turned off at t_8 , the current through the primary of the transformer i_p which was initially flowing through S_3 will now discharge C_2 and charge C_3 simultaneously similar to (4.5) and (4.6). The discharging of C_2 will also result in equal decay of v_{AB} and T_r secondary voltage. The output diodes D_3 and D_4 continue to conduct the load current. S_3 is turned off with zero-voltage as the capacitors C_3 and C_2 limit the rising rate of voltage across S_3 . By the end of this interval, the capacitor C_2 is discharged completely and its body diode D_{S2} becomes forward biased. The conduction of the body diode D_{S2} ensures ZVS turn-on for S_2 . The circuit conditions during this interval are shown in Figure 4.11.

Interval X ($t_9 < t \leq t_{10}$):

Figure 4.12 Interval X.

In this interval, the reflected load current nI_o plus the auxiliary current i_{La} freewheel through the body-diode D_{S2} achieving ZVS turn-on for S_2 . The clamping diode D_{a2} , output rectifier diodes D_1 and D_2 start conducting in this interval as the current i_p decreases in negative direction. The current i_{Lse} remains unchanged as L_{se} is shorted due to simultaneous conduction of D_{a2} and S_4 . The circuit conditions during this interval are shown in Figure 4.12. This interval ends when the gating signal to the main switch S_2 is turned on.

Interval XI ($t_{10} < t \leq t_{11}$):

The circuit conditions in this interval are similar to *Interval X* except that the gating signal to the main switch S_2 is ON and are shown in Figure 4.13. The current through the clamping diode D_{a2} is the difference between i_{Lse} and i_p . This interval ends when the gating signal to the main switch S_4 is turned off.

Figure 4.13 Interval XI.

Interval XII ($t_{11} < t \leq t_{12}$):

Figure 4.14 Interval XII.

When S_4 is turned off with zero-voltage at t_{11} because of C_1 and C_4 , the current $i_p(t_{11})$ which was initially flowing through S_2 will now discharge C_1 and charge C_4 simultaneously as given by (4.10) and (4.11). The primary and secondary voltages of the main transformer T_r and auxiliary transformer T_a are zero as all the output rectifier diodes D_1 - D_4 conduct at the same time. The capacitor C_1 is completely

discharged such that the body diode D_{S1} starts conducting which ensures ZVS turn-on for S_1 by the end of this interval. The voltage v_{AB} follows v_{C4} and reaches V_{in} by the end of this interval. D_{a2} continues to conduct and V_{in} is fully applied on L_{se} which causes i_{Lse} , i_p and i_{Da2} to decay linearly similar to (4.13). The circuit conditions during this interval are shown in Figure 4.14.

Interval XIII ($t_{12} < t \leq t_{13}$):

Figure 4.15 Interval XIII.

The conduction of D_{S1} ensures ZVS turn-on for S_1 . The currents i_{Lse} , i_p and i_{Da2} continue to decay linearly as the voltage V_{in} is fully applied on L_{se} . D_{a2} turns off naturally within this interval when i_{Lse} and i_p are equal. In this interval, the T_r secondary voltage is zero as the output rectifier diodes D_1 - D_4 continue to conduct.

The circuit conditions during this interval are shown in Figure 4.15. This interval ends when the sum of i_{Lse} and $i_{La}/2$ becomes zero.

Interval XIV ($t_{13} < t \leq t_{14}$):

Figure 4.16 Interval XIV.

In this interval, i_p continues to increase in the positive direction which flows through S_1 and S_2 . The output rectifier diodes D_1 - D_4 continue to conduct as i_p is not sufficient to provide the load demand which implies that the T_r secondary voltage is zero during this interval. The circuit conditions during this interval are shown in Figure 4.16. This interval ends once the current i_p reaches the negative maximum to supply the required load current. At t_{14} , the output rectifier diodes D_3 and D_4 turn- off, and the diodes D_1 and D_2 carry the entire load current.

4.3 Steady-state Analysis of Auxiliary Circuit

The operational waveforms of the voltage across the auxiliary inductor and the current through the auxiliary inductor are shown in Figure 4.17 when the converter is modulated with PSM and APWM. As mentioned, the auxiliary capacitors C_{a1} , C_{a2} act as constant dc voltage sources during a switching period. The voltage across the auxiliary capacitors when gated with PSM [1] is given by

$$V_{ca1} = V_{ca2} = V_{in}/2 \quad (4.15)$$

Figure 4.17 Auxiliary inductor voltage and current waveforms. (a) PSM. (b) APWM.

Figure 4.18 Comparison of voltage across auxiliary capacitors and peak current through auxiliary inductor with PSM and APWM.

The dc voltage given by (4.15) is present across L_a during $(1-D)T_s/2$ period of the switching cycle. Therefore, the peak value of auxiliary inductor current with PSM is given by

$$I_{LaP} = \frac{V_{in}(1-D)}{8L_a f_s} \quad (4.16)$$

Similarly, the voltage across auxiliary capacitors when gated with APWM is given by

$$V_{ca1} = \frac{(2-D)V_{in}}{2}; V_{ca2} = \frac{DV_{in}}{2} \quad (4.17)$$

Therefore, the peak value of auxiliary inductor current with APWM is given by

$$I_{LaP} = \frac{V_{in}D(1-D)}{8L_a f_s} \quad (4.18)$$

From Figure 4.17, the auxiliary inductor current waveform is trapezoidal in nature when gated with PSM and triangular when gated with APWM.

The comparison of the variation of voltage across auxiliary capacitors and peak current through auxiliary inductor with duty cycle is shown in Figure 4.18 using (4.15) to (4.18). The peak value of auxiliary inductor current with PSM is larger than that with APWM especially at low duty cycle operation. Therefore, APWM converter results in reduced switching, conduction, and auxiliary circuit losses of the converter compared to PSM converter. This analysis is further verified with the experimental results presented in next section.

It is to be noted that the filter inductor and filter capacitor design is similar to conventional PSM FB dc-dc converter [2], and the auxiliary circuit components design is similar to the procedure mentioned in [3]-[5].

Table 4.1 Design specifications of APWM ZVS converter

Parameter	Value
Input DC voltage	300V
Output DC voltage range	209V - 350V
Maximum output DC current	3.75A
Maximum output power	1.2 kW
Full-bridge switching frequency	100kHz

Figure 4.19 Lithium-ion battery charging profile.**Table 4.2** Main load points in Lithium-ion battery charging profile

Parameter	Nominal power point	Maximum power point	End power point
V_{bat} [V]	280	320	320
I_{bat} [A]	3.75	3.75	0.375
R_{ebat} [Ω]	74.67	85.33	853.33
P_o [kW]	1.05	1.2	0.12

Table 4.3 Component list of APWM ZVS converter

MOSFET Switches	IXFN60N80P
Diodes (D_1 – D_4 , D_{a1} , D_{a2})	C4D10120D
Main transformer (T_r)	E65 – 3C95, n: 1.23, $L_{lk} = 2\mu\text{H}$
Auxiliary transformer (T_a)	ETD54 – 3C90, turns-ratio: 1:1
Inductor (L_{se} , L_a)	E32 – N87, $10\mu\text{H}$, $6\mu\text{H}$
Auxiliary capacitors (C_{a1} , C_{a2})	$4.7\mu\text{F}/300\text{V}$
Output filter inductor (L_f)	1mH
Output filter capacitor (C_f)	$4.4\mu\text{F}/630\text{V}$
DSP controller	TMS320F28335

Figure 4.20 APWM ZVS FB dc-dc converter prototype.

4.4 Experimental Results

The specifications of the converter are given in Table 4.1 and the battery charging profile is shown in Figure 4.19. The voltage limits of the battery are based on Ford C-Max Hybrid EV battery specifications [6]. The key load points in the lithium-ion battery charging profile are listed in Table 4.2. A 1.2 kW converter prototype is developed in the laboratory to verify the performance of the proposed converter with PSM and APWM gating techniques. The components used in the development of the converter are listed in Table 4.3. The developed prototype is shown in Figure 4.20. The proposed methods are implemented on the TMS320F28335 controller using enhanced pulse-width modulators by the up-down counter method [7].

The ZVS results for high-side switch S_3 and low-side switch S_4 of the APWM ZVS converter are shown in Figures 4.21 and 4.22 respectively at the key load points: nominal power point, maximum power point and end power point. The drain to source voltage v_{DS} of the switches attains zero before the respective gating signals are applied. This phenomenon confirms the ZVS turn-on of switches S_3 and S_4 with the proposed APWM gating technique as explained in *Interval IV* and *Interval II* respectively. Similarly, ZVS for S_1 and S_2 can be achieved as explained in *Interval XII* and *Interval IX* respectively.

(a)

(b)

(c)

Figure 4.21 ZVS waveforms of S_3 with APWM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

(a)

(b)

(c)

Figure 4.22 ZVS waveforms of S_4 with APWM. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

(a)

(b)

(c)

Figure 4.23 T_r primary and secondary results without clamp diodes. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

(a)

(b)

(c)

Figure 4.24 T_r primary and secondary results with clamp diodes. (a) At nominal point (280V, 3.75A). (b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

(a)

(b)

(c)

Figure 4.25 Auxiliary circuit waveforms with APWM. (a) At nominal point (280V, 3.75A).

(b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

(a)

(b)

(c)

Figure 4.26 Auxiliary circuit waveforms with PSM. (a) At nominal point (280V, 3.75A).

(b) At maximum point (320V, 3.75A). (c) At end point (320V, 0.375A).

The experimental results for the voltage across T_r secondary v_{sec} , and output rectifier diode v_{DI} are shown in Figure 4.23 without clamping diodes, and in Figure 4.24 with clamping diodes at the key load points. The results indicate that the severity of voltage spikes across output rectifier diodes is lower in the proposed converter as explained in *Interval V and Intervals X, XI and XII*.

The auxiliary inductor voltage v_{La} and current i_{La} results of the converter with the proposed APWM and PSM techniques at key load points are shown in Figures 4.25 and 4.26 respectively.

Figure 4.27 Comparison of peak auxiliary inductor current with APWM and PSM over battery charging profile.

The experimental results for the peak values of i_{La} at different load conditions with APWM and PSM are compared in Figure 4.27. It can be observed from Figure 4.27 that the peak value of i_{La} with APWM is significantly lesser than that with PSM as explained in *Section 4.3*.

The total RMS MOSFET's current stress at different loads with APWM and PSM results are shown in Figure 4.28. The results show that the APWM is better than

PSM as the current stress is less which results in improved efficiency of APWM converter especially at load conditions during CC charging mode.

Figure 4.28 Comparison of total switch's current stress with APWM and PSM over battery charging profile.

Figure 4.29 Efficiency of the converter with APWM and PSM over battery charging profile

Table 4.4 Efficiency comparison of converter with PSM and APWM

Load point	Theoretical η (%)			Practical η (%)		
	PSM	APWM	Improvement	PSM	APWM	Improvement
P ₁	92.41	93.85	1.44	78.1	85.85	7.75
P ₂	93.86	94.82	0.96	84.25	88.33	4.08
P ₃	94.58	95.28	0.7	88.67	90.36	1.69
P ₄	95.3	95.7	0.4	91.85	91.88	0.03
P ₅	96.13	96.17	0.04	94.52	94.86	0.34
P ₆	96.18	96.33	0.15	93.9	93.4	-0.5
P ₇	95.93	96.3	0.37	93.2	93.1	-0.1
P ₈	94.98	95.84	0.86	90.93	90.13	-0.8
P ₉	91.9	93.99	2.09	86.37	87.56	1.19
P ₁₀	84.11	89.05	4.94	75.43	77.41	1.98

The theoretical and experimental efficiency results of the APWM and PSM operated converter over the battery charging profile are shown in Table 4.4 and Figure 4.29. From these results, it is evident that the proposed converter topology achieves similar efficiency in CV charging mode independent of gating technique. However, the proposed APWM operated converter achieves higher efficiency in CC charging mode when compared to the PSM operated converter. This is due to the reduced switching and conduction losses of main switches, auxiliary circuit losses, and low circulating currents.

4.5 Conclusion

In this chapter, an APWM ZVS FB dc-dc converter APWM gating technique has been proposed for battery charging applications in electric vehicles. Theoretical operation of the converter for achieving the ZVS turn-on of the main switches has been discussed. The experimental results verified the capability of the proposed converter to achieve ZVS condition over the entire battery charging range. The high voltage spikes on output rectifier diodes have been mitigated with the clamping diode circuit on the primary side of main transformer. The features have

been validated by the experimental results from the laboratory-scale 1.2 kW converter prototype. The efficiency results have proved the improved performance of the APWM gated proposed converter over the PSM gated proposed converter.

References

- [1] M. Borage, S. Tiwari, and S. Kotaiah, "A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range," *IEEE Power Electronics Letters*, vol. 3, no. 4, pp. 141-143, Dec. 2005.
- [2] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd edition. Kluwer, 2001.
- [3] Z. Chen, B. Ji, F. Ji, and L. Shi, "Analysis and design considerations of an improved ZVS full-bridge DC-DC converter," in *Proc. 25th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 1471-1476.
- [4] W. Chen, X. Ruan, and J. Ge, "A novel full-bridge converter achieving ZVS over wide load range with a passive auxiliary circuit," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 1110-1115.
- [5] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. Wiley, 2013.
- [6] Ford C-Max8698 Hybrid – 2013, Advanced vehicle testing activity – HEV battery testing results, Idaho National Laboratory [Online]. Available: <http://energy.gov/sites/prod/files/2015/02/f19/batteryC-Max8698.pdf>.
- [7] Texas Instruments, "TMS320×2833, 2823× enhanced pulse width modulator (ePWM) module," SPRUG04A, Oct. 2008 (Revised Jul. 2009).

Chapter 5*

APWM ZVZCS Full-Bridge DC-DC Converter for PHEV Battery Charging

In this chapter, a current-fed APWM ZVZCS full-bridge dc-dc converter is presented. APWM gating technique controls the auxiliary inductor current to minimize the auxiliary circuit losses and conduction losses on the primary side. This feature improves the overall efficiency of the proposed converter over the battery charging range compared to the PSM gating method. The operation principle and steady-state analysis of the converter is described. Converter circuit parameters design and magnetics design procedure are discussed. The experimental results are presented to validate the analysis and performance of the converter.

*This chapter is published substantially as V. R. K. Kanamarlapudi, B. F. Wang, P. L. So, and Z. Wang, "Analysis, design and implementation of an APWM ZVZCS full-bridge dc-dc converter for battery charging in electric vehicles," *IEEE Trans. Power Electronics*.

5.1 APWM ZVZCS Full-Bridge DC-DC Converter Topology

Figure 5.1 Proposed APWM ZVZCS full-bridge dc-dc converter.

The proposed ZVZCS FB dc-dc converter topology is shown in Figure 5.1(a) and the APWM gating technique proposed in *Chapter 3* is shown in Figure 5.1(b). In this converter, the auxiliary circuit is comprised of one auxiliary transformer T_a , one auxiliary inductor L_a and two auxiliary capacitors C_{a1} , C_{a2} . The inverter output voltage V_{AB} is symmetrical as S_1 and S_3 are gated with the same duty cycle as shown in Figure 5.1(b). This feature eliminates the dc-offset thereby reducing core loss compared to the configuration present in [2], [3]. The proposed APWM gating

signals can be applied to S_1 - S_4 in two methods to obtain the same output voltage. The first method is shown in Figure 5.1(b) where the duty cycle of the high-side switches D_{SWU} is controlled as $0 < D_{SWU} < 0.5$. The second method is that the duty cycle of the high-side switches is controlled as $0.5 < D_{SWU} \leq 1$. Both the methods can be used during the converter operation to achieve an optimal thermal profile [4]. In this chapter, the first gating method is analyzed. It is noted that the analysis presented in the following section is equally valid for the second method.

5.2 Operation Principle of Converter

The steady-state operation analysis of the converter over the entire battery charging range is explained here. The following assumptions are considered for ease of analysis:

1. All switching elements are ideal;
2. Resistance and inter-winding capacitance of T_r and T_a are neglected;
3. Magnetizing inductance of T_r and T_a is large enough to ignore the effect of magnetizing current during the switching period;
4. Resistance and inter-winding capacitance of L_{se} are neglected;
5. Equivalent capacitance across active switches is the same $C_1 = C_2 = C_3 = C_4 = C$;
6. $C_{a1} = C_{a2} = C_a$ are large enough such that V_{ca1} and V_{ca2} are constant during the switching period;
7. C_f is large enough to assume that the output voltage is constant.

The key operational waveforms of the converter are shown in Figure 5.2. The operation of the converter is divided into twelve-time intervals over one switching cycle. Time intervals t_0 - t_6 illustrates the positive power transfer operation and ZVS transition for S_3 and S_4 . Time intervals t_6 - t_{12} are similar to t_0 - t_6 except that it is negative power transfer operation and ZVS transition for S_1 and S_2 .

Figure 5.2 Key operational waveforms of the proposed converter.

Figure 5.3 Theoretical operational waveforms of converter when $D < D_{boundary}$.

The analysis for *Interval I-Interval VI* is discussed in this section. The analysis for remaining intervals, i.e., *Interval VI-Interval XII* is similar to *Interval I- Interval VI* with appropriate modifications. Therefore, it is not discussed separately.

Interval I ($t_0 < t \leq t_1$): The switch S_1 is turned ON with ZVS at the start of this interval. The body-diode D_{S1} , switch S_2 , and the output diodes D_1 and D_2 are in conduction during this interval. The circuit conditions during this interval are shown in Figure 5.4. The inverter output voltage V_{AB} is given by (5.1). The current

through the primary of the main transformer i_p rises linearly as the output rectifier diodes clamp the main transformer secondary voltage to the output voltage.

The voltage across the auxiliary inductor is constant given by (5.3). The current through L_a also rises linearly given by (5.4).

$$v_{AB}(t) = V_{in}; v_{Tap}(t) = v_{Tas}(t) = \frac{V_{in}}{2} \quad (5.1)$$

$$i_p(t) = \frac{V_{in} - V_o / n}{L_{se}}(t - t_0) \quad (5.2)$$

$$v_{La}(t) = V_{La}^+ = (1 - D) \frac{V_{in}}{2} \quad (5.3)$$

$$i_{La}(t) = I_{La}(t_0) + \frac{V_{in}(1 - D)}{2L_a}(t - t_0) \quad (5.4)$$

Figure 5.4 Interval I.

The current through the switches is given by

$$i_{S1}(t) - i_{DS1}(t) = i_p(t) + \frac{i_{La}(t)}{2} \quad (5.5)$$

$$i_{S2}(t) - i_{DS2}(t) = i_p(t) - \frac{i_{La}(t)}{2} \quad (5.6)$$

This interval ends at $t = t_1$. The switch current $i_{S1}(t) - i_{DS1}(t)$ is positive at the end of

this interval. The duration Δt_{1-0} of this interval is given by

$$\Delta t_{1-0} = \frac{I_{LaP}}{2\left(\frac{V_{in} - V_o / n}{L_{se}}\right) + \frac{V_{in}(1-D)}{2L_a}} \quad (5.7)$$

Interval II ($t_1 < t \leq t_2$): In this interval, the circuit conditions are dependent on load conditions. According to (5.6), the conduction of S_2 or D_{S2} is dependent on magnitudes of $i_p(t)$ and $i_{La}(t)$. It can be understood by examining the following cases. Case (i): Under constant current charging mode, $i_p(t)$ is always greater than $i_{La}(t)/2$, i.e., S_2 is in conduction. Case (ii): Under constant voltage charging mode, the power drawn from the charger is low especially when the battery is with higher state of charge (SoC). In this case, $i_p(t)$ will be less than $i_{La}(t)/2$, i.e., D_{S2} will be in conduction. A duty cycle $D_{boundary}$ is defined to differentiate the heavy-load and light-load conditions. $D_{boundary}$ corresponds to the same peak values of $i_p(t)$ and $i_{La}(t)/2$. Therefore, the duty cycle $D > D_{boundary}$ or $I_{pP} > I_{LaP}/2$ is treated as a heavy-load condition and $D < D_{boundary}$ or $I_{pP} < I_{LaP}/2$ is treated as a light-load condition. The $D_{boundary}$ can be calculated by

$$D_{boundary} = 1 - \frac{8L_a}{L_{se}} \left(1 - \frac{V_o}{nV_{in}}\right) \quad (5.8)$$

where I_{pP} is the peak value of main transformer primary current. Therefore, the circuit conditions under different load conditions are explained as follows:

Under heavy-load condition: The currents i_p and i_{La} continue to rise linearly similar to *Interval I*. The DC input source transfers power to the load through main switches S_1 and S_2 , and output diodes D_1 and D_2 . The corresponding circuit conditions are shown in Figure 5.5(a). The duration of this interval is approximated as follows:

$$\Delta t_{2-1} = \frac{DT_s}{2} - \Delta t_{1-0} \quad (5.9)$$

Figure 5.5 Interval II. (a) Heavy-load. (b) Light-load.

Under light-load condition: The currents i_p and i_{La} continue to rise linearly similar to in *Interval I* as shown in Figure 5.3. The dc input source transfers power to the load through main switches S_1 and S_2 , and output diodes D_1 and D_2 until $i_p(t) > i_{La}(t)/2$. The circuit conditions are same as shown in Figure 5.5(a) for $t_1 < t \leq t_1^1$. The duration Δt_{I^1-I} of this circuit condition is given by

$$\Delta t_{I^1-I} = \frac{I_{LaP}}{\frac{V_{in}(1-D)}{2L_a} - 2\left(\frac{V_{in}-V_o}{n}\right) \frac{1}{L_{se}}} - \Delta t_{I-0} \quad (5.10)$$

When $i_p(t) < i_{La}(t)/2$, the dc input source transfers power to the load through main

switch S_1 , body-diode D_{S2} , output diodes D_1 and D_2 . The circuit conditions during this period are shown in Figure 5.5(b) for $t_1^I < t \leq t_2$. The time Δt_{2-I}^I can be calculated using the following expression.

$$\Delta t_{2-I}^I = \frac{DT_s}{2} - \Delta t_{1-I}^I - \Delta t_{1-0} \quad (5.11)$$

This interval ends once the switch S_1 is turned OFF at t_2 . The currents i_p and i_{La} attain their peak values at t_2 . At the end of *Interval II*, i.e., $t = t_2$,

$$v_{C1}(t_2) = v_{C2}(t_2) = 0; v_{C3}(t_2) = v_{C4}(t_2) = V_{in} \quad (5.12)$$

$$i_p(t_2) = I_{pP}; i_{La}(t_2) = I_{LaP} = \frac{V_{in}D(1-D)}{8L_a f_s} \quad (5.13)$$

$$i_{S1}(t_2) - i_{DS1}(t_2) = I_{pP} + \frac{I_{LaP}}{2} \quad (5.14)$$

$$i_{S2}(t_2) - i_{DS2}(t_2) = I_{pP} - \frac{I_{LaP}}{2} \quad (5.15)$$

Interval III ($t_2 < t \leq t_3$): When S_1 is turned OFF at t_2 , the currents i_p and $i_{La}/2$ which were initially flowing through the switch S_1 will now flow through C_1 and C_4 . These currents charge the capacitor C_1 and discharge the capacitor C_4 simultaneously. The output diodes D_1 and D_2 continue to conduct the load current. The current i_{La} can be considered constant as the time duration of this interval is small and is given by

$$i_{La}(t) = I_{LaP} \quad (5.16)$$

In this interval, the charging and discharging of C_1 and C_4 depend on the load conditions which are described as follows:

Under heavy-load condition: The energy stored in L_{se} is sufficient to charge C_1 and discharge C_4 completely. The body-diode D_{S4} is forward-biased ensuring ZVS turn-on for S_4 by the end of this interval. The circuit conditions during this interval are shown in Figure 5.6(a).

Figure 5.6 Interval III. (a) Heavy-load. (b) Light-load.

During this interval, the current through series inductor i_p , the voltages v_{C1} and v_{C4} across capacitors C_1 and C_4 , and the output voltage of the inverter v_{AB} are given by

$$i_p(t) = \left(I_{pP} + \frac{I_{LaP}}{2}\right) \cos\left(\frac{t-t_2}{\sqrt{2L_{se}C}}\right) - \frac{I_{LaP}}{2} \quad (5.17)$$

$$v_{C1}(t) = \left(I_{pP} + \frac{I_{LaP}}{2}\right) \sqrt{\frac{L_{se}}{2C}} \sin\left(\frac{t-t_2}{\sqrt{2L_{se}C}}\right) \quad (5.18)$$

$$v_{C4}(t) = V_{in} - \left(I_{pP} + \frac{I_{LaP}}{2}\right) \sqrt{\frac{L_{se}}{2C}} \sin\left(\frac{t-t_2}{\sqrt{2L_{se}C}}\right) \quad (5.19)$$

$$v_{AB}(t) = v_{C4}(t); v_{Tap}(t) = v_{Tas}(t) = \frac{v_{AB}(t)}{2} \quad (5.20)$$

Equation (5.19) also implies that ZVS for low-side switch S_4 can be easily achieved because the magnitude of discharging current $i_{S1}(t_2)$ is greater than the conventional ZVS FB dc-dc converter [5]. Similarly, ZVS for switch S_2 can be achieved in second half of the switching cycle ($T_s/2 < t \leq T_s$). The duration Δt_{3-2} of this interval is given by

$$\Delta t_{3-2} = \sqrt{2L_{se}C} \sin^{-1}\left(\frac{2V_{in}}{2I_{pP} + I_{LaP}} \sqrt{\frac{2C}{L_{se}}}\right) \quad (5.21)$$

Under light-load condition: The energy stored in L_{se} alone is not sufficient to completely discharge the capacitor C_4 as I_{pP} is very small. The proposed auxiliary inductor L_a assists in discharging C_4 completely. The body-diode D_{S4} is forward-biased ensuring ZVS turn-on for S_4 by the end of this interval. Therefore, the transition from high-side switch S_1 to low-side switch S_4 results in two different slopes in inverter output voltage v_{AB} as shown in Figure 5.3. The first slope is determined by i_p and i_{La} during $t_2 < t \leq t_2^1$, and the second slope is mainly determined by i_{La} during $t_2^1 < t \leq t_3$. The circuit conditions during this interval are shown in Figure 5.6(b) where the body-diode D_{S2} conducts instead of switch S_2 as $I_{pP} < I_{LaP}/2$. The voltages v_{C1} , v_{C4} during this interval are given by

$$V_{C1}(t_2^1) = (I_{pP} + \frac{I_{LaP}}{2}) \sqrt{\frac{L_{se}}{2C}} \sin\left(\frac{t_2^1 - t_2}{\sqrt{2L_{se}C}}\right) \quad (5.22)$$

$$v_{C1}(t) = V_{C1}(t_2^1) + \frac{I_{LaP}}{4C} (t - t_2^1) \quad (5.23)$$

$$v_{C4}(t) = V_{in} - V_{C1}(t_2^1) - \frac{I_{LaP}}{4C} (t - t_2^1) \quad (5.24)$$

This interval ends when the voltage v_{AB} becomes zero. At the end of *Interval III*, i.e., $t = t_3$,

$$v_{C2}(t_3) = v_{C4}(t_3) = 0; v_{C1}(t_3) = v_{C3}(t_3) = V_{in} \quad (5.25)$$

Interval IV ($t_3 < t \leq t_4$): This interval starts when v_{AB} becomes zero and D_{S4} is forward-biased. During this interval, the output diodes D_1 and D_2 clamp secondary voltage of the main transformer to the output voltage. Thus, a net reflected output voltage V_o/n is applied across L_{se} which causes its current i_p to ramp down linearly with a slope of V_o/nL_{se} as given by

$$i_p(t) = I_p(t_3) - \frac{V_o}{nL_{se}}(t - t_3) \quad (5.26)$$

Figure 5.7 Interval IV. (a) Heavy-load. (b) Light-load.

During this interval, a net negative voltage is applied across L_a due to V_{ca1} . Therefore, the current i_{La} ramps down from $+I_{LaP}$ with a different slope $DV_{in}/2L_a$ compared to the rising slope $(1-D)V_{in}/2L_a$ in *Interval I*. The auxiliary inductor

current and voltage are given by

$$i_{La}(t) = I_{LaP} - \frac{DV_{in}}{2L_a}(t - t_3) \quad (5.27)$$

$$v_{La}(t) = V_{La}^- = -\frac{DV_{in}}{2} \quad (5.28)$$

The output diodes D_1 and D_2 continue to conduct the load current. The circuit conditions on the primary side during this interval are described as follows:

Under heavy-load condition: The circuit conditions during this interval are shown in Figure 5.7(a) where the main switch S_2 is in conduction as $i_p(t) > i_{La}(t)/2$. Under this load condition, i_{La} reaches zero and starts to rise in the negative direction before the current i_p reaches zero.

Under light-load condition: The circuit conditions during this interval are shown in Figure 5.7(b) where the body-diode D_{S2} conducts instead of the switch S_2 as $i_p(t) < i_{La}(t)/2$ during this interval as in Figure 5.3.

This interval ends when the decaying primary current i_p reaches zero. At the end of *Interval IV*, i.e., at $t = t_4$,

$$i_p(t_4) = 0; i_{D1}(t_4) = 0; i_{D2}(t_4) = 0 \quad (5.29)$$

The duration of this interval Δt_{4-3} is given by

$$\Delta t_{4-3} = \left(\frac{nV_{in}}{V_o} - 1\right) \frac{DT_s}{2} - \Delta t_{3-2} \quad (5.30)$$

Interval V ($t_4 < t \leq t_5$): This interval starts when the current through the primary of main transformer i_p becomes zero which indicates that the current through output diodes i_{D1} , i_{D2} is zero. The output capacitor C_f clamps the diode-bridge voltage to the output voltage and provides energy to the load during this interval. The auxiliary inductor current continues to ramp down with the same slope as observed in *Interval IV*. The circuit conditions on the primary side during this interval are described as follows:

Figure 5.8 Interval V. (a) Heavy-load. (b) Light-load.

Under heavy-load condition: The circuit conditions during this interval are shown in Figure 5.8(a). During this period, the auxiliary inductor current freewheels through S_2 and S_4 . The switch S_4 conducts instead of body-diode D_{S4} as the current i_{La} is negative. During this interval, the switches S_2 and S_4 , and body-diodes D_{S2} and D_{S4} currents are given by

$$i_{S2}(t) = \frac{i_{La}(t)}{2}; i_{DS2}(t) = 0 \quad (5.31)$$

$$i_{S4}(t) = \frac{i_{La}(t)}{2}; i_{DS4}(t) = 0 \quad (5.32)$$

The duration of this interval Δt_{5-4} is given by

$$\Delta t_{5-4} = (1-D) \frac{T_s}{2} - \Delta t_{4-3} - \Delta t_{3-2} - \Delta t_{6-5} \quad (5.33)$$

Under light-load condition: The current i_{La} ramps down to zero with a slope of $DV_{in}/2L_a$ and the respective circuit conditions are shown in Figure 5.8(b). During $t_4 < t \leq t_4^l$, the auxiliary inductor current freewheels through D_{S2} , D_{S4} as $i_{La}(t)$ is positive which is shown in Figure 5.3. During this interval, the switches S_2 and S_4 , and body-diodes D_{S2} and D_{S4} currents are given by

$$i_{S2}(t) = 0; i_{DS2}(t) = \frac{i_{La}(t)}{2} \quad (5.34)$$

$$i_{S4}(t) = 0; i_{DS4}(t) = \frac{i_{La}(t)}{2} \quad (5.35)$$

The duration of this interval Δt_{4^l-4} is given by

$$\Delta t_{4^l-4} = (1-D) \frac{T_s}{4} - \Delta t_{4-3} - \Delta t_{3-2} \quad (5.36)$$

During $t_4^l < t \leq t_5$, the circuit conditions are similar to the heavy-load condition as shown in Figure 5.8(a) as $i_{La}(t)$ becomes negative with the same slope $DV_{in}/2L_a$. The time duration Δt_{5-4^l} of this circuit condition is given by

$$\Delta t_{5-4^l} = (1-D) \frac{T_s}{4} - \Delta t_{6-5} \quad (5.37)$$

This interval ends when the current i_{La} attains its negative peak value $-I_{LaP}$ and switch S_2 is turned OFF. S_2 achieves near ZCS as the turn-off current ($I_{LaP}/2$) is smaller than the peak value of the series inductor current I_{pP} .

Interval VI ($t_5 < t \leq t_6$): This interval starts when S_2 is turned OFF at t_5 . The circuit conditions during this interval are shown in Figure 5.9. The auxiliary inductor current which was initially flowing through S_2 will flow through C_2 and C_3 during this interval. This current will charge the capacitor C_2 and discharge the capacitor C_3 simultaneously, and the respective voltages are given by (5.38) and (5.39).

Figure 5.9 Interval VI.

By the end of this interval, the capacitor C_3 is discharged completely and the body-diode D_{S3} is forward-biased ensuring ZVS turn-on for S_3 . The current i_{La} can be considered constant due to the short duration of this interval.

$$v_{C2}(t) = \frac{I_{LaP}}{4C} (t - t_5) \quad (5.38)$$

$$v_{C3}(t) = V_{in} - \frac{I_{LaP}}{4C} (t - t_5) \quad (5.39)$$

Equation (5.39) also implies that the ZVS for high-side switch S_3 can only be achieved with the auxiliary circuit current i_{La} . The ZVS mechanism for S_1 in the second half of switching period ($T_s/2 < t \leq T_s$) is similar to S_3 .

This interval ends when the voltage v_{AB} becomes V_{in} . At the end of *Interval VI*, i.e., $t = t_6$,

$$v_{C3}(t_6) = v_{C4}(t_6) = 0; v_{C1}(t_6) = v_{C2}(t_6) = V_{in} \quad (5.40)$$

$$v_{La}(t_6) = V_{La}^+ = (1-D) \frac{V_{in}}{2} \quad (5.41)$$

The duration Δt_{6-5} of this interval is given by

$$\Delta t_{6-5} = \frac{4CV_{in}}{I_{LaP}} \quad (5.42)$$

Table 5.1 Design specifications of APWM ZVZCS converter

Parameter	Value
Input DC voltage	300V
Output DC voltage range	209V - 350V
Maximum output DC current	3.75A
Maximum output power	1.2 kW
Full-bridge switching frequency	100kHz
Output voltage ripple	$< 3.5V_{pk-pk}$
Auxiliary capacitor voltage ripple	$< 3V_{pk-pk}$

Figure 5.10 Lithium-ion battery charging profile.**Table 5.2** Key load points in Li-ion battery charging profile

Parameter	Start point	Nominal point	Transition point	End point	Re-charge point
V_{bat} [V]	209	280	320	320	310
I_{bat} [A]	3.75	3.75	3.75	0.375	0.8
R_{ebat} [Ω]	55.73	74.67	85.33	853.33	387.5
P_o [kW]	0.78	1.05	1.2	0.12	0.25

Figure 5.11 Voltage gain characteristics of the converter.

5.3 Steady-state Analysis of Converter

The specifications given in Table 5.1 are considered for analyzing the converter. The converter operates under battery charging profile shown in Figure 5.10 [1]. The voltage limits of the battery are based on Ford C-Max Hybrid EV battery specifications [6]. The key load points in the battery charging profile are listed in Table 5.2. The steady-state analysis of the converter is given as follows:

5.3.1 Voltage Gain Analysis

The voltage gain of the proposed converter is determined using the volt-second balance of L_{se} and the average value of series inductance current i_p [7]. From *Interval I – Interval IV* operation analysis of the converter, it can be deduced as follows:

$$\frac{nV_{in} - V_o}{nL_{se}}(t_2 - t_0) = \frac{V_o}{nL_{se}}(t_4 - t_2) \quad (5.43)$$

$$\frac{(nV_{in} - V_o)(t_2 - t_0)(t_4 - t_0)f_s}{nL_{se}} = \frac{nV_o}{R_{ebat}} \quad (5.44)$$

where R_{ebat} is the equivalent load of the converter. The voltage gain of the converter can be obtained from (5.43) and (5.44), and is given by

$$g_v = \frac{V_o}{V_{in}} = \frac{2n}{1 + \sqrt{1 + \frac{4n^2 L_{se}}{f_s R_{ebat} (t_2 - t_0)^2}}} \quad (5.45)$$

The voltage gain g_v of the converter at different loads with respect to the duty cycle D is shown in Figure 5.11.

5.3.2 Auxiliary Circuit Voltage and Current

The auxiliary capacitors C_{a1} , C_{a2} act as constant DC voltage sources during a switching period. The respective voltages V_{ca1} , V_{ca2} when the converter is gated with APWM and PSM are given by

$$\begin{aligned} V_{ca1} &= \frac{(2-D)V_{in}}{2}; V_{ca2} = \frac{DV_{in}}{2}; APWM \\ V_{ca1} &= V_{ca2} = \frac{V_{in}}{2}; PSM \end{aligned} \quad (5.46)$$

The peak value of auxiliary inductor current when the converter is gated with APWM and PSM is given by

$$\begin{aligned} I_{LaP} &= \frac{V_{in} D(1-D)}{8L_a f_s}; APWM \\ I_{LaP} &= \frac{V_{in} (1-D)}{8L_a f_s}; PSM \end{aligned} \quad (5.47)$$

5.3.3 Soft-switching Analysis

Without Auxiliary Circuit: According to (5.19), the ZVS condition for low-side switches S_2 and S_4 depends on I_{pP} , I_{LaP} , and dead-time t_d . In this section, the ZVS analysis is carried out without considering the auxiliary circuit, i.e., the auxiliary

circuit current I_{LaP} is zero. A factor called α_{ZVL} given by (5.48) is defined to validate the ZVS range for low-side switches. The ZVS transition for low-side switches is achieved only when $\alpha_{ZVL} > 1$.

$$\alpha_{ZVL} = \frac{t_d}{2C} \left(\frac{V_o}{V_{in}} \sqrt{\left(1 - \frac{V_o}{nV_{in}}\right) \frac{1}{R_{ebat} L_{se} f_s}} \right) \quad (5.48)$$

As seen from (5.48), α_{ZVL} is a function of switch capacitance, input and output voltages, effective load resistance on the system, series inductance, switching frequency and dead-time. The effect of various parameters on α_{ZVL} is discussed next.

Figure 5.12 ZVS range of low-side switches over battery charging profile.

The ZVS range factor for low-side switches α_{ZVL} without the auxiliary circuit and with respect to the battery charging profile at different dead-times is shown in Figure 5.12. An equivalent capacitance of $C = 0.88nF$ and a series inductance $L_{se} = 18.72\mu H$ are considered for analysis. From Figure 5.12, it can be observed that a minimum t_d of 185ns is required to achieve ZVS turn-on for low-side switches over the entire battery charging range. However, an increase in t_d requires more

secondary turns to obtain the rated output voltage which translates to higher conduction losses on the primary side.

ZCS for low-side switches S_2 and S_4 can be achieved because the main transformer T_r operates in discontinuous conduction mode (DCM). For high-voltage battery charging applications, MOSFETs switching losses can be greatly minimized by operating them with ZVS rather than ZCS. The increased ZVS range for S_2 and S_4 and ZVS for S_1 and S_3 are achieved by integrating an auxiliary circuit as shown in the proposed converter Figure 5.1(a).

With Auxiliary Circuit: For the proposed passive auxiliary circuit assisted converter, a factor called α_{ZVLA} given by (5.49) is defined to validate the ZVS range for low-side switches using *Interval III* analysis. The ZVS transition for low-side switches can be achieved only when $\alpha_{ZVLA} > 1$.

$$\alpha_{ZVLA} = \frac{t_d}{2C} \left(\frac{V_o}{V_{in}} \sqrt{\left(1 - \frac{V_o}{nV_{in}}\right) \frac{1}{R_{ebat} L_{se} f_s}} + \frac{D(1-D)}{16L_a f_s} \right) \quad (5.49)$$

α_{ZVLA} is also plotted in Figure 5.12 with respect to battery charging profile at different dead-times. It can be inferred from Figure 5.12 that a minimum t_d of 85ns is required to guarantee ZVS turn-on for low-side switches S_2 and S_4 . The auxiliary inductance L_a is chosen to guarantee ZVS turn-on for high-side switches S_1 and S_3 . Hence, the proposed system results in ZVS turn-on for all active switches S_1 - S_4 over the entire battery charging range. The design considerations for the auxiliary inductor are explained in the next section.

The low-side switches S_2 and S_4 can also achieve near ZCS as their turn-off current ($I_{LaP}/2$) is smaller than the peak value of the series inductor current I_{pP} .

5.3.4 Features of Proposed APWM Converter

1. ZVS turn-on for all active switches over the entire battery charging range – from *Interval III* and *Interval VI* analysis and soft-switching analysis with the auxiliary circuit.
2. Near ZCS turn-off for low-side switches as the auxiliary circuit current is small during their turn-off transition – from *Interval V* analysis.
3. The circulating losses during the freewheeling period on the primary side are minimal due to the current-driven configuration, capacitive output filter and APWM gating technique – from *Interval V* analysis.
4. The secondary side freewheeling losses are completely eliminated as the main transformer T_r is operated in DCM; however, the DCM operation increases the peak current of the series inductor which may affect the efficiency at heavy loads – from *Interval V* analysis.
5. The reverse-recovery and the switching losses in the output rectifier diodes are minimal as they are naturally commutated when the series inductor L_{se} current reaches zero – from *Interval V* analysis.
6. The voltage spikes across the output rectifier diodes are mitigated due to the current-driven and the capacitive output filter configuration – from *Interval V* analysis.
7. Improved EMI due to mitigation of the high voltage spikes across the output rectifier diodes – from *Interval V* analysis.
8. The output power and voltage are regulated by controlling the duty cycle of the active switches.
9. The auxiliary inductance L_a required to achieve ZVS turn-on with APWM is 25% less when compared to PSM.
10. The peak value of current through active switches during ZVS transition with APWM is smaller than PSM. The switching current for active switches is given by

$$I_{S2,S4-ZVS-APWM} = V_o \sqrt{\left(1 - \frac{V_o}{nV_{in}}\right) \frac{1}{R_{ebat} L_{se} f_s}} + \frac{V_{in} D(1-D)}{16L_{aAPWM} f_s} \quad (5.50)$$

$$I_{S1,S3-ZVS-APWM} = \frac{V_{in} D(1-D)}{16L_{aAPWM} f_s} \quad (5.51)$$

The switching current for active switches when the converter is operated with PSM is given by

$$I_{S2,S3-ZVS-PSM} = V_o \sqrt{\left(1 - \frac{V_o}{nV_{in}}\right) \frac{1}{R_{ebat} L_{se} f_s}} + \frac{V_{in} (1-D)}{16L_{aPSM} f_s} \quad (5.52)$$

$$I_{S1,S4-ZVS-PSM} = \frac{V_{in} (1-D)}{16L_{aPSM} f_s} \quad (5.53)$$

Figure 5.13 Comparison of ZVS currents with APWM and PSM operated converter.

Theoretical comparison of ZVS currents with APWM and PSM at different loads using (5.50) – (5.53) is shown in Figure 5.13. It is evident that the ZVS current levels with PSM are greater than APWM operated converter. It can be concluded from this analysis that the switching and conduction losses on the primary side are substantial when the converter is operated with PSM. Therefore, the proposed

APWM gating technique results in increased efficiency compared to PSM gating technique. It is further verified with the experimental results.

5.4 Circuit Parameters Design

5.4.1 Transformer Turns Ratio

The main power transformer T_r turns ratio n is designed for maximum output voltage at maximum duty cycle ratio of 0.95. Turns-ratio n is given by

$$n = \frac{V_{o\max}}{D_{\max} V_{in}} = 1.23 \quad (5.54)$$

5.4.2 Series Inductor

The series inductance is estimated to ensure the critical conduction mode of the converter at the full-load condition. The full-load condition corresponds to the CC mode to CV mode transition point mentioned in Table 5.2. Therefore, the series inductance value is given by

$$L_{se} = \left(1 - \frac{V_o}{nV_{in}}\right) \frac{V_o^2}{4n^2 f_s P_{o\max}} = 18.72 \mu H \quad (5.55)$$

5.4.3 Auxiliary Inductor

The auxiliary inductance is selected to ensure that the available reactive energy during switching transitions guarantees ZVS for all MOSFETs over the battery charging range of the converter. The auxiliary inductor L_a acts as a constant current source during t_d with a magnitude of I_{Lap} . This current charges and discharges the capacitor C_2 and C_3 during *Interval VI*. By using (5.38), the variation of voltage

across capacitor C_2 during *Interval VI* with respect to different load conditions for various auxiliary inductances is shown in Figure 5.14.

Figure 5.14 Load versus V_{C2} for different values of L_a .

In order to ensure ZVS, the capacitor voltage V_{C2} should be greater than the DC input voltage V_{in} over the entire battery charging range within $t_d=250\text{ns}$. According to Figure 5.14, the voltage V_{C2} is minimum at the full-load condition. The duty cycle of the converter corresponding to full-load condition is given by

$$D = \sqrt{\frac{16n^2 L_{se} f_s / R_{ebat}}{(\frac{2nV_{in}}{V_o} - 1)^2 - 1}} = 0.86 \quad (5.56)$$

Then, the auxiliary inductance value is calculated by

$$L_a = \frac{D(1-D)t_d}{32Cf_s} = 10.7\mu H \quad (5.57)$$

5.4.4 Auxiliary Capacitors

To ensure proper operation of the proposed converter, the two auxiliary capacitors C_{a1} , C_{a2} in the passive auxiliary circuit should behave as constant DC voltage sources over a single switching period. The auxiliary capacitances are selected such that the peak to peak ripple voltage on each capacitor is small at the maximum auxiliary reactive current. The minimum required capacitance allowing a ripple of $\Delta V_{Ca} = 3\text{V}$ is estimated as

$$C_{a1} = C_{a2} \geq \frac{V_{in}}{256L_a f_s^2 \Delta V_{ca}} \geq 3.65\mu\text{F} \quad (5.58)$$

Therefore, $4.7\mu\text{F}$ capacitance is selected for auxiliary capacitors.

5.4.5 Output Filter Capacitor

The output filter capacitor is designed based on the allowable ripple in the output voltage. The minimum filter capacitance required to maintain the voltage ripple within 1% is given by

$$C_f \geq \frac{I_o}{8f_s \Delta V_{cf}} \geq 1.34\mu\text{F} \quad (5.59)$$

Therefore, a $2.2\mu\text{F}$ output filter capacitor is selected.

Figure 5.15 Voltage, current and flux density waveforms of L_a .

5.5 Magnetics Design

Magnetics design for the auxiliary circuit is one of the important parts of the converter to achieve improved efficiency. The proposed converter consists of one auxiliary inductor, one auxiliary transformer, one main transformer and one series inductor. The design steps for the auxiliary inductor are discussed as follows:

1. *Select core material:* Manganese-Zinc Ferrite core is chosen as it is characterized by low losses at high frequencies in the range of 100kHz – 300kHz.
2. *Set design constraint:* The design constraint for the auxiliary circuit is that the maximum loss should be less than 6W (0.5% of rated power). The maximum power loss $P_{tot_allowed}$ constraints for the auxiliary inductor and auxiliary transformer must be less than 2.5W and 3.5W respectively.
3. *Calculate maximum volt-second product:* The voltage, current and flux density waveforms of the auxiliary inductor are shown in Figure 5.15. The required inductor is a linear AC inductor as the corresponding flux density $B_{La}(t)$ is bipolar triangular. The maximum volt-second product λ across the auxiliary inductor is the main parameter required for the design. It is given by

$$\lambda = \frac{V_{in} D(1-D)}{4fs} = 187.5 \times 10^{-6} Vs \quad (5.60)$$

4. Calculate maximum RMS current and wire gauge: The maximum RMS current through the auxiliary inductor is given by

$$I_{LaRMS} = \frac{V_{in} D(1-D)}{8\sqrt{3}L_a f_s} = 5A \quad (5.61)$$

Table 5.3 Critical parameters of magnetic components

Parameter	Symbol	L_a	T_a	L_{se}	T_r
Core type	N/A	RM12 [8]	ETD54 [9]	EE32 [8]	EE65 [9]
Core material grade	N/A	N97	3C90	N87	3C95
Saturation flux (25°C)	B_{sat}	0.51T	0.47T	0.49T	0.53T
Relative core losses	P_{fe}	3.6 W (100kHz, 0.2T)	4.8 W (100kHz, 0.1T)	3 W (100kHz, 0.2T)	49.8 W (100kHz, 0.2T)
Core loss coefficient	K_c	$8.8896 \cdot 10^{-5} \text{W/Hz}^\alpha \text{T}^\beta$	$1.7967 \cdot 10^{-6} \text{W/Hz}^\alpha \text{T}^\beta$	$7.408 \cdot 10^{-5} \text{W/Hz}^\alpha \text{T}^\beta$	$1.8641 \cdot 10^{-5} \text{W/Hz}^\alpha \text{T}^\beta$
Core loss geometrical coefficient	K_{fe}	$19 \text{W/cm}^3 \text{T}^\beta$	$64.7162 \text{W/cm}^3 \text{T}^\beta$	$21.4552 \text{W/cm}^3 \text{T}^\beta$	$47.0806 \text{W/cm}^3 \text{T}^\beta$
Effective magnetic path length	l_e	5.7cm	12.7cm	7.4cm	14.7cm
Effective magnetic cross-section area	A_e	1.46cm^2	2.8cm^2	0.83cm^2	5.4cm^2
Effective magnetic volume	V_e	8.32cm^3	35.5cm^3	6.14cm^3	79cm^3
Core window area	A_w	0.73cm^2	3.16cm^2	1.08cm^2	3.94cm^2
Mean length turn	MLT	6.1cm	9.6cm	6.44cm	15cm
Winding fill factor	K_u	0.4	0.4	0.4	0.4
Number of turns	N	10	20:20	10	13:16
Air gap	l_g	1.7mm	N/A	0.7616mm	N/A

length					
Litz wire configuration	N/A	Six AWG22 twisted Litz	Three AWG22 twisted Litz	Six AWG22 twisted Litz	Six AWG22 twisted Litz
Litz wire area	W_a	2.0268mm ²	1.0134mm ²	2.0268mm ²	2.0268mm ²
Winding resistance	R	0.068Ω	0.196Ω/0.196Ω	0.068Ω	0.208Ω/0.256Ω

The Litz wire gauge for the auxiliary inductor is AWG14. It is calculated based on the maximum RMS current and current density $J = 2.5\text{A/mm}^2$. The AWG14 Litz wire is made of 6 strings of 40 strands of AWG38.

5. *Determine core size:* The core is selected to ensure that the core geometrical constant $K_{geometry}$ is greater than the electrical specification constant $K_{electrical}$ [7]. The constants are given by

$$K_{geometry} = \frac{A_w A_e^{(2(\beta-1)/\beta)}}{(MLT)(l_e^{2/\beta})} ((\beta/2)^{-\beta/(\beta+2)} + (\beta/2)^{2/(\beta+2)})^{-(\beta+2)/\beta} \quad (5.62)$$

$$K_{electrical} = \frac{\rho \lambda^2 I_{LaRMS}^2 K_{fe}^{2/\beta}}{4K_u P_{tot_allowed}^{(\beta+2)/\beta}} \quad (5.63)$$

The parameters required for (5.62) and (5.63) can be found in the datasheet of the core selected. RM12 core satisfies the inequality $K_{geometry} (1.5 \times 10^{-7}) > K_{electrical} (2.8 \times 10^{-9})$. The critical parameters of the core are given in Table 5.3.

6. *Select number of turns:* The selection of the number of turns for the auxiliary inductor depends on the peak to peak flux density ΔB_{La} , core winding area A_w and the winding fill factor K_u . The optimal flux density ΔB_{LaOpt} to minimize the total loss in the auxiliary inductor is calculated by (5.64). Then, the number of turns N_{La} for L_a is estimated from (5.65). The

number of turns selected should also satisfy the criterion that the core window area is large enough to accommodate Litz AWG calculated in *step 4* and is given by (5.66).

$$\Delta B_{LaOpt} = 2 \left(\frac{\rho \lambda^2 I_{LaRMS}^2 (MLT)}{2 K_u A_w A_e^3 l_e \beta K_{fe}} \right)^{1/(\beta+2)} \quad (5.64)$$

$$N_{La} = \frac{V_{in} D (1-D)}{4 \Delta B_{La} A_e f_s} \quad (5.65)$$

$$K_u A_w \geq N_{La} W_a \quad (5.66)$$

The ΔB_{LaOpt} has to be coarse adjusted if the inequality (5.66) is not satisfied with a good margin. Finally, ΔB_{La} is coarsely adjusted to 0.128T, and the number of turns is selected as $N_{La} = 10$.

7. *Total auxiliary inductor loss:* The core loss of L_a using improved General Steinmetz Equation (iGSE) [10] is given by

$$P_{Fe} = K_i |\Delta B_{La}|^\beta \left(\frac{2}{T_s} \right)^\alpha (D^{1-\alpha} + (1-D)^{1-\alpha}) \quad (5.67)$$

The coefficient K_i is calculated using $K_i = \frac{K_c}{2^{\beta-1} \pi^{\alpha-1} (1.1044 + \frac{6.8244}{\alpha + 1.354})}$

The peak to peak ΔB_{La} is calculated using the following equation:

$$\Delta B_{La} = \frac{2 L_a I_{LaP}}{N_{La} A_e} \quad (5.68)$$

The winding loss of L_a is given by

$$P_{winding} = \frac{I_{La}^2 R_{La}}{3} \quad (5.69)$$

The maximum auxiliary inductor loss is given by

$$P_{tot} = P_{Fe} + P_{winding} = 2.3\text{W} \leq 2.5\text{W} \text{ (power loss constraint)} \quad (5.70)$$

8. *Air-gap length:* The length of air gap l_g to obtain the required L_a is calculated from

$$l_g = \frac{\mu_o N_{La}^2 A_e}{L_a} = 1.7\text{mm} \quad (5.71)$$

Therefore, the presented design parameters satisfy the power loss constraint set for the auxiliary inductor. The auxiliary transformer is also devised in the same approach. The series inductor and main transformer are designed based on the constraint that the peak flux density $\Delta B_{max} \leq 0.25\text{T}$ to regulate the core loss and to avoid the core saturation. The final design parameters and the critical parameters of the selected cores are given in Table 5.3.

Table 5.4 Component list of APWM ZVZCS converter

MOSFET Switches	IXFN64N60P
Rectifier diodes (D_1 – D_4)	C4D10120D
Main transformer (T_r)	E65 – 3C95, n: 1.23, Leakage inductance: 5.06 μH
Auxiliary transformer (T_a)	ETD54 – 3C90, turns-ratio – 1:1
Series inductor (L_{se})	E32 – N87, 13.7 μH
Auxiliary inductor (L_{aAPWM}/L_{aPSM})	RM12 – N97, 10.7 $\mu\text{H}/14.2\mu\text{H}$
Auxiliary capacitors (C_{a1} , C_{a2})	4.7 $\mu\text{F}/300\text{V}$

Output filter capacitor (C_f)	2.2 μ F/630V
DSP controller	TMS320F28335
Gate driver IC	IXDN609SI
Optocoupler IC	ACPL-4800-300E

(a)

(b)

Figure 5.16 (a) Proposed APWM ZVZCS converter prototype. (b) Experimental setup of the system.

5.6 Experimental Results

A 1.2 kW converter prototype is developed in the laboratory to verify the theoretical analysis presented so far and validate the performance of the proposed converter and gating technique. The designed converter specifications are given in Table 5.1. The components used in the development of the converter are listed in Table 5.4. The developed prototype is shown in Figure 5.16(a) and the

experimental setup is shown in Figure 5.16(b). PSM and the proposed APWM are developed on the TMS320F28335 controller using enhanced pulse width modulators by the up-down counter control method [11].

Figure 5.17 ZVS waveforms for high-side switch S_3 . (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At re-charge point.

Figure 5.18 ZVS waveforms for low-side switch S_4 . (a) At start point. (b) At nominal point. (c) At transition point. (d) At end point. (e) At re-charge point.

The ZVS results for S_3 and S_4 are shown in Figures 5.17 and 5.18 at key load points given in Table 5.2. The drain to source voltage of the switches attains zero before the respective gating signals are applied. This phenomenon confirms ZVS turn-on of switches S_3 and S_4 . As explained in Section 5.2, the theoretical switch current i_{SW4} waveform in Figure 5.2 at heavy-load conditions, i.e., $I_{pP} > I_{LaP}/2$ is similar to the measured switch current result in Figure 5.17(a) - (c). The switch current i_{SW4} waveform in Figure 5.3 at light-load conditions, i.e., $I_{pP} < I_{LaP}/2$ is also similar to the switch current result in Figure 5.18(d) and 5.18(e). Therefore, the experimental results validate the theoretical analysis of the converter operation for heavy-load and light-load conditions.

Figure 5.19 T_r secondary operating waveforms. (a) At transition point. (b) At end point.

The experimental results for the voltage across main transformer secondary v_{sec} , and output rectifier diode v_{DI} at transition and end load points are given in Figure 5.19. It is clearly evident from Figure 5.19 that the high voltage spikes on rectifier diodes are mitigated in the proposed converter.

Figure 5.20 Auxiliary circuit waveforms with APWM. (a) At transition point. (b) At end point.

Figure 5.21 Auxiliary circuit waveforms with PSM. (a) At transition point. (b) At end point.

Figure 5.22 Comparison of peak current of auxiliary inductor with APWM and PSM over battery charging profile.

The auxiliary inductor voltage v_{La} and current i_{La} results of the converter with the proposed APWM and PSM techniques at transition and end load points are shown in Figures 5.20 and 5.21 respectively. The experimental results for the peak values of i_{La} at different load conditions with APWM and PSM are compared in Figure 5.22. It can be observed from Figure 5.22 that the peak value of i_{La} with APWM is significantly lesser than that with PSM especially at light-load conditions.

Figure 5.23 Comparison of ZVS switch's current with APWM and PSM over battery charging profile.

The measured switch's current during the ZVS transition with APWM and PSM at different load points are compared in Figure 5.23. It can be observed from this figure that the peak value of ZVS current with APWM is significantly lesser than PSM, especially at light-load conditions.

Figure 5.24 Efficiency of the converters over battery charging profile. (a) CC charging mode. (b) CV charging mode.

Figure 5.24 and Table 5.5 shows the efficiency of the converter over the battery charging profile under following scenarios:

1. APWM converter without auxiliary circuit (conventional converter);
2. PSM converter with auxiliary circuit, $L_a = L_{aPSM} = 14.2\mu\text{H}$;
3. APWM converter with auxiliary circuit, $L_a = L_{aAPWM} = 10.7\mu\text{H}$.

Table 5.5 Efficiency comparison of converter in with PSM and APWM

Load point	Theoretical η (%)			Practical η (%)		
	PSM	APWM	Improvement	PSM	APWM	Improvement
P ₁	91.41	94.36	2.95	89.91	92.38	2.47
P ₂	92.93	94.95	2.02	90.46	93.35	2.89
P ₃	93.80	95.26	1.46	91.66	94.01	2.35
P ₄	94.58	95.50	0.93	92.82	94.24	1.42
P ₅	95.25	95.31	0.06	94.5	94.95	0.45
P ₆	95.00	95.27	0.27	94.04	94.85	0.81
P ₇	94.25	95.11	0.86	92.12	94.06	1.94
P ₈	92.17	94.75	2.58	88.65	92.23	3.58
P ₉	85.85	94.08	8.23	78.4	88.57	10.17
P ₁₀	71.87	93.24	21.37	62.64	81.14	18.5

From Figure 5.24 and Table 5.5, it is evident that the proposed converter topology with the proposed APWM achieves superior efficiency when compared to the PSM and conventional converters. According to CV charging mode efficiency results, the APWM converter efficiency is higher especially at light-load conditions due to the reduced switching and conduction losses of main switches, auxiliary circuit losses, low circulating current, and elimination of reverse-recovery losses of output rectifier diodes.

Table 5.6 shows the comparison between the proposed APWM ZVZCS converter and the other converters [5], [12], [13]. The other converter systems are the half-bridge integrated full-bridge converter in [12], two symmetric auxiliary poles

assisted PSM converter in [13], trailing-edge PWM converter in [5], and the proposed PSM converter.

Table 5.6 Comparison of converters

Converter topology	Topology in [12]	Topology in [13]	Topology in [5]	Proposed topology	
Modulation method	PSM	PSM	Trailing-edge PWM	PSM	APWM
Number of auxiliary components	2	6	Not applicable	4	4
Total number of components	16	17	11	15	15
Auxiliary inductor size (volt-second)	$\frac{V_{in}}{8} \frac{D}{f_s}$	$\frac{V_{in}}{8} \frac{1}{f_s}$	Not applicable	$\frac{V_{in}}{8} \frac{(1-D_{max})}{f_s}$	$\frac{V_{in}}{8} \frac{D_{max}(1-D_{max})}{f_s}$
Auxiliary circuit peak current rating	$\frac{V_{in}D}{8L_{aux}f_s}$	$\frac{V_{in}}{8L_a f_s}$	Not applicable	$\frac{V_{in}(1-D)}{8L_a f_s}$	$\frac{V_{in}D(1-D)}{8L_a f_s}$
ZVS	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)	Two switches (S_2, S_4)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)
ZCS	Not applicable	Two switches (S_1, S_4) – near ZCS	Two switches (S_2, S_4)	Two switches (S_1, S_4) – near ZCS at full-load	Two switches (S_2, S_4) – near ZCS
Additional snubber circuit	Required	Not required	Not required	Not required	Not required
Voltage spikes across output rectifier diodes	Minimized	Mitigated	Mitigated	Mitigated	Mitigated

The converters [12] and [13] have more number of components compared to the proposed converter. The converter in [12] requires additional snubber circuit to mitigate the voltage spikes across the output rectifier diodes compared to the

proposed APWM ZVZCS converter. The converter in [5] can only achieve ZVS for two switches whereas the proposed APWM converter achieves ZVS for all (four) switches. In the case of AC inductor design, the volt-second product is the key design parameter to determine the physical size of the inductor core [14]. According to Table 5.6, it can be observed that the auxiliary inductor size (volt-second) required for ZVS in [12] and [13] is larger compared to the proposed APWM ZVZCS converter. The proposed PSM converter auxiliary inductor size is also greater than the proposed APWM ZVZCS converter.

5.6 Conclusion

In this chapter, a ZVZCS full-bridge DC-DC converter with APWM gating technique has been proposed for battery charging applications in electric vehicles. Theoretical operation of the converter for achieving the ZVS turn-on of the main switches has been discussed. The circuit parameters design and magnetics design have been presented. The results have verified the capability of the proposed converter to achieve ZVS condition over the entire battery charging range. The proposed converter showed significant reductions in switching losses, auxiliary circuit losses and required auxiliary inductance. The high voltage spikes on output rectifier diodes have been mitigated. The features have been validated by the experimental results from the laboratory-scale 1.2 kW converter prototype. The efficiency results have proved the improved performance of the proposed APWM converter over the proposed PSM converter and the conventional ZVZCS converter.

References

- [1] G. V. Rodrigo and A. P. L. Joao, *Electric vehicle integration into modern power networks*. Springer, 2013.
- [2] P. Imbertson and N. Mohan, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," *IEEE Trans. Industrial Applications*, vol. 29, no. 1, pp. 121-125, Feb. 1993.
- [3] P. Imbertson and N. Mohan, "New directions in DC-DC power conversion based on idealized concepts leading ultimately to the asymmetrical duty-cycle power converter," *IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 722-727, Aug. 1997.
- [4] Y. S. Lai, Z. J. Su, and Y. T. Chang, "Novel phase-shift control technique for full-bridge converter to reduce thermal imbalance under light-load condition," *IEEE Trans. Industry Applications*, vol. 51, no. 2, pp. 1651-1659, Apr. 2015.
- [5] D. S. Gautam, F. Musavi, W. Eberle, and W. G. Dunford, "A zero-voltage switching full-bridge DC-DC converter with capacitive output filter for plug-in hybrid electric vehicle battery charging," *IEEE Trans. Power Electronics*, vol. 28, no. 12, pp. 5728-5735, Dec. 2013.
- [6] Ford C-Max8698 Hybrid – 2013, Advanced vehicle testing activity – HEV battery testing results, Idaho National Laboratory [Online]. Available: <http://energy.gov/sites/prod/files/2015/02/f19/batteryC-Max8698.pdf>.
- [7] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd edition. Kluwer, 2001.
- [8] EPCOS, *Ferrites and Accessories - Data Book*, 2013.
- [9] FERROXCUBE, *Soft Ferrites and Accessories - Data Handbook*, 2013.
- [10] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. Wiley, 2013.

- [11] Texas Instruments, “TMS320×2833, 2823× enhanced pulse width modulator (ePWM) module,” SPRUG04A, Oct. 2008 (revised Jul. 2009).
- [12] I. O. Lee and G. W. Moon, “Half-bridge integrated ZVS full-bridge converter with reduced conduction loss for electric vehicle battery chargers,” *IEEE Trans. Industrial Electronics*, vol. 61, no. 8, pp. 3978-3988, Aug. 2014.
- [13] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, “A novel ZVZCS full-bridge DC-DC converter used for electric vehicles,” *IEEE Trans. Power Electronics*, vol. 27, no. 6, pp. 2752-2769, Jun. 2012.
- [14] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, “An automotive on-board 3.3-kW battery charger for PHEV application,” *IEEE Trans. Vehicular Technology*, vol. 61, no. 8, pp. 3466-3474, Oct. 2012.

Chapter 6

Conclusions and Future Works

In this chapter, the summary and overall conclusions of this thesis are discussed. The improved performance of the proposed converter topologies and gating control methods have been verified with laboratory converter prototypes. The experimental results have demonstrated that the proposed converters and control methods are effective for dc-dc conversion stage in PHEV/EV battery chargers. Moreover, areas for further research are presented as well.

6.1 Conclusions

In *Chapter 1*, the data on greenhouse gas emissions by sector from the Intergovernmental Panel on Climate Change group has been presented. The emission figures indicated that the transportation sector contributes to 14% of total greenhouse gas emissions. A research study from NREL on the usage of PHEV/EV in place of conventional vehicles has found that the total emissions are reduced by one-third of the total emissions in case of low carbon grid. The results motivated the use of renewable energy sources and battery operated vehicles as a solution for reducing the carbon emissions. Therefore, PHEVs/EVs are the promising solutions for nowadays transportation to have livable and sustainable environment.

One of the main concerns for wide adoption of PHEVs/EVs is the grid power quality issues associated with the integration of charging infrastructure. Another concern for consumers is the increasing utility costs and charging time, which requires the battery chargers to operate at higher efficiency throughout the battery charging range. As discussed in *Chapter 1*, the battery charger includes an ac-dc converter followed by an isolated dc-dc converter.

The main focus of this thesis is to develop a high efficiency and high power density isolated dc-dc converter for battery chargers. Therefore, the basic hard-switched and soft-switched power converters have been studied and the dc-dc converter requirements for battery charging application have been identified in *Chapter 1*.

In *Chapter 2*, a comprehensive review of the related research on gating techniques and adaptive control methods for dc-dc converters have been presented in detail. The power electronics literature related to full-load range soft-switched resonant full-bridge dc-dc converters and active auxiliary circuit assisted full-bridge dc-dc converters have been presented. Then, it was followed by the prior works on adaptive and non-adaptive passive auxiliary circuit assisted full-bridge dc-dc

converters. Special attention has been given to understand the state-of-the-art solutions for the voltage spikes across the output rectifier diodes in full-bridge dc-dc converters.

In *Chapter 3*, asymmetrical pulse width modulation (APWM) and trailing-edge pulse width modulation (TEPWM) gating techniques have been proposed. The adaptive frequency control combined with APWM called as ADFC has been presented. The steady-state analysis of the passive auxiliary circuit in the ZVZCS full-bridge dc-dc converter has been analyzed with the proposed gating techniques. The design considerations for the ADFC converter circuit parameters design have been discussed. The design for the auxiliary inductors has shown that the proposed ADFC can reduce the inductance by a factor close to 2.3 compared to the PSM technique. Then, a theoretical comparative power loss analysis of the converter with the proposed APWM, ADFC and PSM gating techniques has been presented to verify the advantages mentioned. The loss analysis results have indicated that the proposed ADFC converter achieves similar overall efficiency as that of the PSM converter. The experimental efficiency results of 1.2 kW converter prototype confirmed the advantages of the proposed gating techniques over the conventional PSM technique for the ZVZCS FB dc-dc converter with auxiliary inductor at both legs.

In *Chapter 4*, a ZVS FB dc-dc converter with APWM gating technique has been proposed for battery charging applications in electric vehicles. Theoretical operation of the converter for achieving the ZVS turn-on of the main switches has been discussed. The results have verified the capability of the proposed converter to achieve ZVS condition over the entire battery charging range. The high voltage spikes on output rectifier diodes are mitigated with the clamping diode circuit on the primary side of main transformer. The features have been validated by the

experimental results from the laboratory-scale 1.2 kW converter prototype. The efficiency results have proved the improved performance of the APWM gated proposed converter over the PSM gated proposed converter.

In Chapter 5, an APWM ZVZCS full-bridge DC-DC converter has been proposed for battery charging applications in electric vehicles. Theoretical operation of the converter for achieving the ZVS turn-on of the main switches has been discussed. The circuit parameters design and magnetics design have been presented. The results have verified the capability of the proposed converter to achieve ZVS condition over the entire battery charging range. The proposed converter showed significant reductions in switching losses, auxiliary circuit losses and required auxiliary inductance. The high voltage spikes on output rectifier diodes are mitigated. The features have been validated by the experimental results from the laboratory-scale 1.2 kW converter prototype. The efficiency results have proved the improved performance of the proposed APWM converter over the proposed PSM converter and the conventional ZVZCS converter.

The comparison of the proposed gating techniques and converter topologies are summarized in Table 6.1. In summary, ADFC ZVZCS FB dc-dc converter (proposed in *Chapter 3*) is better than PSM ZVZCS FB dc-dc converter as it achieves higher power density by reducing the auxiliary magnetics requirement.

APWM ZVS FB dc-dc converter (proposed in *Chapter 4*) is better than PSM ZVS FB dc-dc converter as it achieves better overall efficiency.

APWM ZVZCS FB dc-dc converter (proposed in *Chapter 5*) is better than APWM ZVS FB dc-dc converter (proposed in *Chapter 4*) as it eliminates the requirement of filter inductor and clamping diodes achieving high power density and low cost.

Finally, APWM ZVZCS FB dc-dc converter is better than other converter topologies (ADFC ZVZCS FB dc-dc converter, APWM ZVS FB dc-dc converter) because of less number of components and better efficiency.

Table 6.1 Comparison of the proposed dc-dc converters

Converter topology	$2L_a + \text{ZVZCS FB converter}$		$1L_a + 1T_a + \text{ZVS FB converter}$	$1L_a + 1T_a + \text{ZVZCS FB converter}$	
Modulation method	PSM	APWM	APWM	PSM	APWM
Number of auxiliary components	6	6	4	4	4
Total number of components	17	17	18	15	15
Auxiliary inductor size (volt-second)	$\frac{V_{in}}{8} \frac{D}{f_s}$	$\frac{V_{in}}{8} \frac{1}{f_s}$	$\frac{V_{in}}{8} \frac{D_{max}(1-D_{max})}{f_s}$	$\frac{V_{in}}{8} \frac{(1-D_{max})}{f_s}$	$\frac{V_{in}}{8} \frac{D_{max}(1-D_{max})}{f_s}$
Auxiliary circuit peak current rating	$\frac{V_{in}D}{8L_{aux}f_s}$	$\frac{V_{in}}{8L_a f_s}$	$\frac{V_{in}D(1-D)}{8L_a f_s}$	$\frac{V_{in}(1-D)}{8L_a f_s}$	$\frac{V_{in}D(1-D)}{8L_a f_s}$
ZVS	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)	All switches ($S_1 - S_4$)
ZCS	Two switches (S_1, S_4) – near ZCS	Two switches (S_1, S_4) – near ZCS	None	Two switches (S_1, S_4) – near ZCS at full-load	Two switches (S_2, S_4) – near ZCS
Additional snubber circuit	Not required	Not required	Required	Not required	Not required
Voltage spikes across output rectifier diodes	Eliminated		Minimized	Eliminated	

6.2 Future Works

The following future works can be carried out based on the works from this thesis:

1. It is found that the adaptive frequency control method has superior efficiency for FB converter with auxiliary inductor at both legs. Further work can be done on improving the efficiency of auxiliary inductor and transformer assisted FB dc-dc converter.
2. In general, the on-board chargers are designed to handle the power rating about 6.6 kW. In future, interleaved and non-interleaved topologies of the auxiliary inductor and transformer assisted FB dc-dc converter can be explored for higher charging power levels.
3. Performance evaluation of the proposed topologies when integrated with front-end ac-dc PFC stage of battery charger can be considered for further studies.
4. A detailed closed-loop control analysis is required to understand the dynamics of the proposed converters and interleaved/non-interleaved topologies for battery charging application.
5. With the evolution of integrated magnetics and planar transformers, new dc-dc converter topologies can be explored in view of reducing the number of magnetic cores.
6. Topologies can be further extended for solid-state transformer and power conditioning systems for interfacing solar PV, fuel cell and battery systems.

List of Publications

Journal/Transaction Publications

- [1] **V. R. K. Kanamarlapudi**, B. Wang, P. L. So, and Z. Wang, “Analysis, design and implementation of an APWM ZVZCS full-bridge DC-DC converter for battery charging in electric vehicles,” *IEEE Trans. Power Electronics*, vol. 32, no. 8, pp. 6145-6160, Aug. 2017.
- [2] B. Wang, **V. R. K. Kanamarlapudi**, L. Xian, X. Y. Peng, K. T. Tan, and P. L. So, “Model predictive voltage control for single-inductor multiple-output dc-dc converter with reduced cross regulation,” *IEEE Trans. Industrial Electronics*, vol. 63, no. 7, pp. 4187-4197, Jul. 2016.
- [3] **V. R. K. Kanamarlapudi**, B. Wang, K. N. Kumar, and P. L. So, “A new ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range: Analysis, design and implementation,” submitted to *IEEE Trans. Industrial Applications*. (2nd revision)
- [4] **V. R. K. Kanamarlapudi**, B. Wang, and P. L. So, “An ADFC ZVZCS full-bridge DC-DC converter with reduced auxiliary magnetics requirement for battery charging,” submitted to *IEEE Trans. Industrial Electronics*. (Under Review)
- [5] **V. R. K. Kanamarlapudi** and P. L. So, “Analysis and implementation of pulse-width modulated DC-DC converter for electric vehicles with improved efficiency,” submitted to *IEEE Trans. Industrial Applications*. (Under Review)

Conference Publications

- [6] **V. R. K. Kanamarlapudi**, N. Brahmendra, B. Sivaneasan, P. L. So, and C. C. Chan, “An APWM soft-switched DC-DC converter for PV and EV,” in *Proc. IEEE Photovoltaic Specialists Conference (PVSC)*, Jun. 2014.

- [7] B. Wang, **V. R. K. Kanamarlapudi**, and P. L. So, “Model predictive voltage control method for flyback converter,” in *Proc. IEEE India International Conference (INDICON)*, Dec. 2015.
- [8] **V. R. K. Kanamarlapudi**, B. Wang, K. N. Kumar, and P. L. So, “A New ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range,” in *Proc. IEEE India International Conference (INDICON)*, Dec. 2015. (Best Paper Award)
- [9] **V. R. K. Kanamarlapudi** and P. L. So “Analysis and implementation of pulse-width modulated DC-DC converter for electric vehicles with improved efficiency,” in *Proc. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec. 2016.

Appendix

1. Small-Signal Analysis of ZVS FB DC-DC Converter

The small-signal analysis of APWM ZVS FB converter shown in Figure 4.1 is carried out based on the assumption that the natural time constants of the storage elements are much larger than the switching period. This assumption coincides with the requirement of small switching ripple on output side. Another assumption is that the series inductance and leakage inductance of transformer are neglected compared to the output filter inductance. In addition, the battery is a nonlinear load for the converter system, but for small-signal variation around an operating point, the load can be approximated by an equivalent resistance $R = \partial v_{bat} / \partial i_{bat}$ where v_{bat} and i_{Bat} are small-signal ac components. The equivalent load resistance 'R' depends on the operating point. The state-space equations of the converter system using averaging technique are given by (A1)-(A3).

$$\begin{bmatrix} \frac{d \hat{i}_{Lf}}{dt} \\ \frac{d \hat{i}_{La}}{dt} \\ \frac{d \hat{v}_{Cf}}{dt} \\ \frac{d \hat{v}_{Ca1}}{dt} \\ \frac{d \hat{v}_{Ca2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & \frac{-1}{RC_f} & 0 \\ 0 & \frac{-1}{C_{a1} + C_{a2}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{a1} + C_{a2}} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} \frac{nD}{L_f} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} \frac{nV_{in}}{L_f} \\ \frac{V_{in}}{2L_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (A1)$$

$$\hat{v}_o = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (A2)$$

$$\hat{i}_{in} = \begin{bmatrix} D & \frac{1}{2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (A3)$$

Table A1. Comparison of transfer functions of APWM ZVS FB converter and conventional FB converter

Requirement	APWM ZVS FB dc-dc converter (Chapter 4)	Conventional FB dc-dc converter
Voltage control gain	$\frac{nV_{in}R}{L_f C_f R S^2 + L_f S + R}$	$\frac{nV_{in}R}{L_f C_f R S^2 + L_f S + R}$
Audio susceptibility	$\frac{nDR}{L_f C_f R S^2 + L_f S + R}$	$\frac{nDR}{L_f C_f R S^2 + L_f S + R}$
Input admittance	$\frac{nD^2(RC_f S + 1)}{L_f C_f R S^2 + L_f S + R}$	$\frac{nD^2(RC_f S + 1)}{L_f C_f R S^2 + L_f S + R}$
Output impedance	$\frac{R}{RC_f S + 1}$	$\frac{R}{RC_f S + 1}$
Current control gain	$I_o + \frac{V_{in}}{4L_a S} + \frac{nDV_{in}(RC_f S + 1)}{L_f C_f R S^2 + L_f S + R}$	$I_o + \frac{nDV_{in}(RC_f S + 1)}{L_f C_f R S^2 + L_f S + R}$

The transfer functions voltage control gain, audio susceptibility, input admittance, output impedance and current control gain of the passive auxiliary circuit assisted APWM ZVS FB dc-dc converter and conventional FB converter are given in Table A1. It can be inferred from

Table A1 that the transfer functions of the proposed passive auxiliary circuit assisted APWM ZVS FB dc-dc converter (Chapter 4) are same as conventional FB dc-dc converter except the current control gain transfer function. The proposed ZVS converter has additional component $V_{in} / 4L_a S$ due to the additional passive auxiliary circuit.

(a)

(b)

(c)

(d)

(e)

Figure A1. Estimated frequency response of APWM ZVS FB DC-DC converter. (a) Voltage control gain. (b) Audio susceptibility. (c) Input admittance. (d) Output impedance. (e) Current control gain.

The estimated frequency response of the proposed APWM ZVS FB dc-dc converter is shown in Figure A1. The voltage control gain frequency response has a gain margin of infinity and phase margin of 0.5 deg with a bandwidth of 23.28 kHz. The current control gain frequency response has a gain margin of infinity and phase margin of infinity with a bandwidth of infinity. The small-signal analysis and frequency response results shown above indicate that the converter is stable.

2. Small-Signal Analysis of ZVZCS FB DC-DC Converter

The small-signal analysis of APWM ZVZCS FB converter shown in Figure 5.1 is carried out based on the assumption that the natural time constants of the storage elements are much larger than the switching period. This assumption coincides with the requirement of small switching ripple on output side. And the battery is a nonlinear load for the converter system, but for small-signal variation around an operating point, the load can be approximated by an equivalent resistance $R = \partial v_{bat} / \partial i_{bat}$ where v_{bat} and i_{bat} are small-signal ac components. The equivalent load resistance ‘ R ’ depends on the operating point. The state-space equations of the converter system using averaging technique are given by (A4)-(A6).

$$\begin{bmatrix} \frac{d \hat{i}_{Lf}}{dt} \\ \frac{d \hat{i}_{La}}{dt} \\ \frac{d \hat{v}_{Cf}}{dt} \\ \frac{d \hat{v}_{Ca1}}{dt} \\ \frac{d \hat{v}_{Ca2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{DV_{in}}{L_{se} V_o} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{DV_{in}}{C_f V_o} & 0 & 0 & \frac{-1}{RC_f} \left(1 + \frac{1}{V_{in}}\right) & 0 \\ 0 & \frac{-1}{C_{a1} + C_{a2}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{a1} + C_{a2}} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} \frac{D}{L_{se}} \\ 0 \\ \frac{V_o}{RC_f V_{in}^2} \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} \frac{V_{in}}{L_{se}} \\ \frac{V_{in}}{2L_a} \\ \frac{V_o}{RC_f DV_{in}} \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (A4)$$

$$\hat{v}_o = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (\text{A5})$$

$$\hat{i}_{in} = \begin{bmatrix} D & \frac{1}{2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Lf} \\ \hat{i}_{La} \\ \hat{v}_{Cf} \\ \hat{v}_{Ca1} \\ \hat{v}_{Ca2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{d} \quad (\text{A6})$$

Table A2. Transfer functions of APWM ZVZCS FB dc-dc converter

Requirement	APWM ZVZCS FB dc-dc converter (Chapter 5)
Voltage control gain	$\frac{V_o (L_{se} V_o^2 S + RD^2 V_{in}^3)}{D(RC_f L_{se} V_{in} V_o^2 S^2 + (1 + V_{in}) L_{se} V_o^2 S + RD^2 V_{in}^3)}$
Audio susceptibility	$\frac{V_o (L_{se} V_o^2 S + RD^2 V_{in}^3)}{V_{in} (RC_f L_{se} V_{in} V_o^2 S^2 + (1 + V_{in}) L_{se} V_o^2 S + RD^2 V_{in}^3)}$
Input admittance	$\frac{D(1-D)}{4L_a S} + \frac{D^2 V_{in} V_o^2 (1 + RC_f S)}{RC_f L_{se} V_{in} V_o^2 S^2 + (1 + V_{in}) L_{se} V_o^2 S + RD^2 V_{in}^3}$
Output impedance	$\frac{R}{RC_f S + 1}$
Current control gain	$\frac{V_o I_o}{V_{in}} + \frac{V_{in}}{4L_a S} + \frac{DV_{in}^2 V_o^2 (1 + RC_f S)}{RC_f L_{se} V_{in} V_o^2 S^2 + (1 + V_{in}) L_{se} V_o^2 S + RD^2 V_{in}^3}$

The transfer functions voltage control gain, audio susceptibility, input admittance, output impedance and current control gain of the passive auxiliary circuit assisted APWM ZVZCS FB dc-dc converter are given in

Table A2. It can be inferred from

Table A2 that the passive auxiliary circuit has an effect on input admittance and current control gain transfer functions of the APWM ZVZCS FB dc-dc converter.

The estimated frequency response of the proposed APWM ZVZCS FB dc-dc converter is shown in Figure A2. The voltage control gain frequency response has a gain margin of infinity and phase margin of 0.17 deg with a bandwidth of 160 kHz.

(a)

(b)

(c)

(d)

(e)

Figure A2. Estimated frequency response of APWM ZVZCS FB dc-dc converter. (a) Voltage control gain. (b) Audio susceptibility. (c) Input admittance. (d) Output impedance. (e) Current control gain.

The current control gain frequency response has a gain margin of infinity and phase margin of infinity with a bandwidth of 34.85 kHz. The small-signal analysis and frequency response results shown above indicate that the converter is stable.

3. Control Block Diagram of ZVZCS Converter

Figure A3. Control block diagram for APWM ZVZCS FB dc-dc converter.

The control block diagram for APWM ZVZCS FB dc-dc converter is shown in Figure A3. The duty cycle D is calculated based on the battery charging characteristic and input voltage. The zeros would result in 180° phase boost, which increases the phase margin considerably. The transfer function of zero pair is given by

$$H_{Zero\,Pair}^{soft}(z) = 1 - \left(2 - \frac{1}{256}\right)z^{-1} + \left(1 - \frac{1}{512}\right)z^{-2} \quad (A7)$$

In order to have an infinite dc gain in the control loop, an Euler integrator is added to the control system. The transfer function of the Euler integrator is given by

$$H_{Integrator}^{Euler}(z) = \frac{1}{1 - z^{-1}} \quad (A8)$$