Switched-capacitor power converters for battery-powered and self-powered applications

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**SWITCHED-CAPACITOR POWER
CONVERTERS FOR BATTERY-POWERED
AND SELF-POWERED APPLICATIONS**

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Abstract

Today's portable electronic devices are becoming more feature-rich and yet power hungry. Designing the power management units to meet the increasing power consumption without sacrificing the battery life has never been more challenging. The design of power converters to interface with various types of energy harvesters is also gaining substantial attention due to the emerging Internet-of-Things devices.

This research explores the feasibility of using switched-capacitor (SC) power converters for both battery-powered and battery-less applications. Chapter 3 presents a lower boundary hysteretic control method for a SC DC-DC converter, which achieves optimal output voltage ripple by matching the output sampling frequency to the converter switching frequency. The converter responds instantly to step-up load transients that are smaller than six times the initial load current. When larger load steps occur, the sampling frequency jumps to its maximum value, resulting in small output voltage undershoots while using an output capacitance value on the same order as the flying capacitance. A 1/2 step-down SC DC-DC converter using on-chip flying capacitance is fabricated in 0.18 μm CMOS process, which achieves 86.4% peak efficiency and delivers a maximum output power of 5.6 mW.

Chapter 4 extends the use of hysteretic control technique to multiphase interleaved SC DC-DC converters. The proposed technique achieves both tight regulation in the steady state and fast response during the load transients with the aid of three control boundaries. In the steady state, the output voltage is regulated around a reference voltage, i.e. the first control boundary. The phase number is changed by a minimum step size from cycle to cycle to achieve tight regulation. To improve the load

transient response, a higher and a lower control boundary are introduced whereby the controller switches to a coarse operation mode whenever the output voltage crosses the higher or lower control boundaries. The converter achieves a peak efficiency of 81.5% and delivers a maximum output power of 7 mW.

In order to eliminate the output voltage ripple and improve the transient response. An in-phase output voltage regulation, which combines NMOS-LDOs with the power switches of the SC converter in both charging and discharging phases, is proposed. An adaptive gate slope technique is used to reduce the output glitches during phase transitions and a gate pre-charge technique assists the turn-on of the regulated transistor when the respective phase begins. The proposed converter, implemented in 0.18 μm CMOS technology, achieves a peak efficiency of 83.3% and achieves less than 0.5 mV output voltage ripple and less than 10 mV output glitches when delivering 100 mA output current.

To meet the demand for self-powered devices in the IoT era, a triple-topology reconfigurable SC DC–DC converter is proposed for indoor photovoltaic energy harvesting. To improve the overall energy efficiency, the first converter topology transfers the energy from the PV cell to the load in one conversion stage when the PV energy is available and the load is demanding energy. When the load demands no energy, the excess energy in the PV cell is stored in the buffer through the second topology. The third topology acts as the backup converter, which is enabled to deliver the stored energy to the load when the PV energy is not available. The proposed converter was fabricated in 0.18 μm CMOS process and achieves peak efficiencies of 87, 88 and 78% while delivering energy from the PV cell to the load, from the PV cell to the buffer and from the buffer to the load, respectively.

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Chapter 1 INTRODUCTION

This Chapter introduces the background and motivation of this thesis. A typical power management system in portable electronic devices is discussed and three types of DC-DC voltage regulators, namely linear regulators, switched-inductor DC-DC converters and switched-capacitor DC-DC converters are compared. These discussions lead to the objectives and scope of this thesis.

1.1 Background

The world has been increasingly connected over the past few decades due to the rapid growth of information and communications technologies. The Internet-of-Things (IoT) [1], emerged in recent years, has connected more than 10 billion devices today and the number will continue to grow at a rate of 15-20% per year in the near future, as forecasted by ABIresearch [2]. The connected devices require a minimum level of intelligence to collect, process and transmit data. Any intelligent device, however, consumes energy.

To meet the consumers' demand, today's portable electronic devices, such as cell phones, are becoming more and more feature-rich. For these devices, the battery life (i.e. the amount of time the device can work continuously before its battery must be re-charged) is a great concern. As more functions are incorporated, the power consumption also increases. To extend the battery life by simply using a larger battery is not an attractive solution because it increases the size, weight and cost of the device. Hence the development of low power circuit techniques, for example dynamic voltage frequency scaling (DVFS) [3], and more efficient power

management units (PMUs) that optimize the energy usage in battery operated devices are of utmost importance.

Besides the portable electronic devices, the growth of IoT has led to the demand for billions of wireless, intelligent devices which will be installed in a broad range of applications such as vehicles, smart homes, green buildings, health-care and etc [4-10] These devices, often come in large number or located remotely, need to function reliably over a long period of time (in years) with minimum maintenance cost including battery replacement. Energy autonomy is the key to overcome this challenge [11] by using ambient energy sources such as solar energy [12], vibration energy [13], heat energy [14], RF energy [15] and etc. Depending of the application, different types of ambient energies can be harvested. For example, a piezoelectric harvester is a natural choice for powering tire pressure monitoring sensors due to the abundant vibration energy [16]. On the other hand, solar cells can be used when natural or artificial light is available.

1.2 Power Management in Portable Devices and Choice of Power Converters

The increasing demand for more compact and power efficient portable devices has driven the development of system-on-chips (SoCs). Benefiting from the technology scaling, today's SoCs (e.g. Apple A9 SoC, Samsung Exynos SoC) integrate the central processing units (CPUs), graphic processing units (GPUs), memory, wireless communications modules (such as WIFI, 4G, Bluetooth, GPS) and most of the other key components that make the device function [17]. Reducing the power consumption in such complex SoCs is a challenging and on-going research topic.

1.2.1 Power Management in Portable Devices

The power management circuit in a battery powered devices should reduce both the dynamic and static power consumption. The PMUs save the overall power consumption of a system primarily by enabling efficient power delivery from the energy source to the various sub-systems which consume static (e.g. analog circuits) or dynamic power (e.g. digital circuits) or both (e.g. mixed signal circuits). Without power management circuits, especially switching regulators, efficient voltage conversion and power delivery would not be possible. One of the most well-established and widely used power reduction techniques today is the dynamic voltage frequency scaling (DVFS) for digital circuits. Specifically, The DVFS technique reduces the dynamic power consumption, which is given by [18]

$$P_{dynamic} = \sigma CV^2 f_{sw} \quad (1.1)$$

where σ is the activity factor, C is the collective switching capacitance, V is the supply voltage and f_{sw} is the switching frequency.

Different circuit blocks on the same SoC perform different functionalities, they often require different supply voltages to operate. In fact, using individual supply rails for different circuit blocks helps to optimize the overall SoC power consumption and performance by applying independent DVFS to each block. However, although most functional components can be fully integrated into a SoC, the power management units usually require bulky passive components, especially inductors and capacitors that remain hard to be integrated. Hence, as more functionalities continue to be integrated into a single chip, generating the increasing number of independent supply rails becomes more expensive as it requires more off-chip passive components as well as power supply pins.

A typical power management unit (PMU) for SoCs in battery-powered portable devices is shown in Figure 1.1 [19]. To cater to the need of different circuit blocks, the PMU generates multiple independent supply voltages, both higher and lower than the battery supply voltage. The supply voltage of each block may be adjusted dynamically (DVS) depending on its real-time performance requirement. Moreover, the battery supply voltage itself drops as the battery drains. Switching mode power converters are the only solution to achieve high power conversion efficiency in such systems. Since the DC battery is the main energy source, DC-DC converters (including switched-inductor and switched-capacitor DC-DC converters) are the predominant designs of switching mode power converters in portable devices. While the output of switching mode DC-DC converters can be used directly by some circuits (typically digital circuits) that can tolerate certain amount of supply voltage ripple, many analog and radio frequency (RF) circuits are sensitive to supply noise. Hence the output voltage of switching converters must be filtered by linear regulators [20] before they can be used to power the noise sensitive loads. Nowadays, both linear regulators and switching mode DC-DC converters can be found in almost every portable electronic device.

Figure 1.1 A typical Power Management Unit for SoCs [19].

1.2.2 Linear Regulators

Linear regulators, such as low drop-out regulators (LDOs [21-23]), have been widely used in portable devices to power the analog and RF circuits and other noise sensitive applications. As shown in Figure 1.2, a typical linear regulator consists of a pass transistor, an output capacitor, a feedback network consisting of R_{f1} and R_{f2} , and an error amplifier. The error amplifier senses the differences between the feedback output voltage with reference voltage, V_{ref} , and adjust the on-resistance of the pass transistor to regulate the output voltage at its desired value, given as

$$V_{out,desired} = (1 + \frac{R_{f1}}{R_{f2}})V_{ref} \quad (1.2)$$

The linear regulators draw continuous current from the input, resulting in much lower output noise as compared to switching mode DC-DC converters. Besides, linear regulators can be designed with high loop gain-bandwidth, which allows for faster transient response than that of switching converters. However, since the load current is drawn directly from the input supply, linear regulators can only generate

output voltages that are lower than the input voltage, and the maximum achievable efficiency is limited to

$$\eta_{max} = \frac{V_{out}}{V_{in}} \quad (1.3)$$

Therefore, the linear regulator technology does not lend itself to DVFS, which requires a wide range of output voltage.

Figure 1.2 A typical linear regulator [20].

Linear regulators do not require a bulky passive component for energy transfer, therefore, the size is usually much smaller than that of DC-DC converters. However, a conventional linear regulator still need sufficiently large output capacitance, in the order of μF , to ensure system stability as well as to reduce the overshoot and undershoot during load transients. The output capacitance limits the potential of fully integrating the linear regulators. Therefore, a new class of LDOs, output-capacitorless LDO (OCL-LDO), that do not require dedicated output capacitors are designed in recent years [24-26]. The OCL-LDOs can be fully-integrated, reducing the number of external components and supply pins. Compensating such OCL-LDOs, however, is challenging and is an on-going research topic.

1.2.3 Switched-inductor DC-DC Converters

To generate output voltages that can exceed the input voltage and maintain high power conversion efficiency over a wide output voltage range, switching mode power converters must be used. Inductor-based DC-DC converters with off-chip inductors have been the dominant designs of switching mode DC-DC converters [27-29]. A simplified architecture of a conventional boost DC-DC converter is shown in Figure 1.3. Pulse width modulation (PWM) is commonly used to regulate these inductor-based DC-DC converters. The boost converter has two operating phases. In the first phase, the switch M_N is turned ON, M_P is turned OFF, the current and the stored energy in the inductor increase. In the second phase, M_N is OFF and M_P is ON, the inductor releases the stored energy to the output. It can be shown that in steady state, the output voltage of the boost converter is given by

$$V_o = \frac{V_{in}}{1-D} \quad (1.4)$$

where $0 < D < 1$ is duty cycle, which defined as fraction of time that the converter operates in the first phase.

Figure 1.3 A simplified PWM switched-inductor boost DC-DC converter.

To regulate the output voltage, the error amplifier compares the output voltage with the reference voltage, and the PWM controller adjusts the duty ratio according to the sensed error signal. The desired value is set at

$$V_{out,desired} = (1 + \frac{R_{f1}}{R_{f2}})V_{ref} \quad (1.5)$$

Unlike linear regulators, the switched-inductor DC-DC converters are theoretically lossless, i.e.

$$\eta_{max} = \frac{V_o I_o}{V_{in} I_{in}} = 100\% \quad (1.6)$$

In reality, various loss mechanisms due to non-ideal passive and active components reduce the actual power conversion efficiency. Nonetheless, over 80% efficiency can be easily achieved.

However, the switching nature of switching mode DC-DC converters inevitably generates output voltage ripple and switching noise. Post-filtering by additional linear regulators is necessary when supplying critical analog or RF blocks. The passive components, including the power inductor and output capacitor, occupy large footprint and are hard to be integrated. Realizing high quality inductors (high energy density, low ESR) in CMOS technologies is especially difficult, which requires additional costly post-fabrication steps [30-32]. Moreover, to ensure the system stability, the control loop unity-gain frequency is typically limited to less than one-fifth of the switching frequency; hence the transient response of the converter is limited.

1.2.4 Switched-capacitor DC-DC Converters

Switched-capacitor (SC) DC-DC converters (also known as charge pumps) are another type of switching converters that use capacitors instead of inductors or transformers as the energy transfer devices [33-35]. SC DC-DC converters have been used in a variety of applications, such as memory circuits, to generate programmable high supply voltages [36, 37]. In recent years, there has been extensive research in using SC power converters as a replacement for linear regulators and switched-inductor power converters in both battery-powered portable devices and self-powered emerging devices, such as implantable medical devices and wireless sensor nodes [33, 38, 39].

A simplified switched-capacitor DC-DC converter with no-load voltage conversion ratio of 1/2 is shown in Figure 1.4. The power stage consists of four power transistors (M_{N1} - M_{N2} and M_{P1} - M_{P2}), and a flying capacitor (C_{fly}). The flying capacitor serves as the intermediate energy storage and transfer device. The SC power stage has two phases of operation. In phase one, M_{P1} and M_{P2} are turned ON, the voltage across C_{fly} is charged to $V_{in} - V_{out}$. In phase two, M_{N1} and M_{N2} are turned ON, the voltage across C_{fly} is discharged to V_{out} . Under no-load condition, the voltage ripple across C_{fly} is zero. Hence $\frac{V_{out}}{V_{in}} = \frac{1}{2}$ which is the ideal voltage conversion ratio of this particular SC DC-DC converter. As will be discussed in the following Chapters, the theoretical maximum efficiency of a SC DC-DC converter is given by

$$\eta_{max} = \frac{V_{out}}{M_{VCR,NL}V_{in}} \quad (1.7)$$

where $M_{VCR,NL}$ is the ideal no-load voltage conversion ratio. The efficiency is similar to that of a linear regulator except that the input voltage is scaled down by the converter's voltage gain. Therefore, the efficiency of a switched-capacitor DC-DC converter drops linearly as the actual load voltage V_{out} deviate from the ideal no-load voltage given by $M_{VCR,NL}V_{in}$. To overcome this problem, multi-ratio SC DC-DC converters using reconfigurable topologies have been proposed, making SC converters feasible for DVS systems [40, 41]. However, implementing multi-ratio SC converters requires multiple off-chip flying capacitors and large number of supply pins, which limits its practical usefulness. On the other hand, the key advantages of SC DC-DC converters over its inductive counterparts include higher energy storage density of capacitors than that of similarly scaled inductors and easier integration of high quality capacitors in CMOS technologies. Moreover, using on-chip capacitors allows for multiphase interleaved implementation which suppresses the output voltage ripple significantly while eliminating the need for a large external output capacitor [35, 42, 43].

Figure 1.4 A simplified PFM switched-capacitor DC-DC converter.

1.3 Objective and Scope

Based on the above discussions, a comparison of the linear regulators and both the switched-inductor and switched-capacitor DC-DC converters is summarized as shown in Table 1.1.

TABLE 1.1 COMPARISON OF TYPICAL LINEAR AND SWITCHING REGULATORS

Regulator	Linear Regulators	Switched-inductor DC-DC Converters	Switched-capacitor DC-DC Converters
Size	Small	Largest	Medium
V_{out}	$V_{out} < V_{in}$	$V_{out} \leq V_{in}$ or $V_{out} > V_{in}$	$V_{out} \leq V_{in}$ or $V_{out} > V_{in}$
Noise	Low	High	High
Transient Response	Fast	Slow	Slow
Typical Output Power	sub- μ W to hundreds of mW	>10 mW	<10 mW
Power Efficiency	$< V_{out}/V_{in}$	Highest	High
Integration Potential	Easiest	Hard	Easy

Clearly, each type of voltage regulator has its advantages and limitations. Linear regulators offer the smallest form factor, lowest output noise, fast transient response and fully integration potential. However, they are limited to applications where the output voltage is lower than the input voltage. Most importantly, the efficiency is fundamentally limited by $\frac{V_{out}}{V_{in}}$, hence scaling the output voltage results in significant efficiency loss unless their load circuits consume only a small fraction of the total power. Linear regulators can support several μ W to hundreds of mW output power.

Switched-inductor and switched-capacitors DC-DC are capable to generate output voltages that can be higher or lower than the input supply voltage. Both suffer from high output noise and slow transient response. The switched-inductor converters typically offer the highest power efficiency. However, they also occupy the largest footprint and are the most difficult to be integrated, primarily due to the need of inductors. To date, high power (>10 mW) switching regulators are still dominated by inductor-based DC-DC converters. On the other hand, the use of switched-capacitor DC-DC converters have traditionally been limited to deliver less than 10 mW output power. SC converters are getting more attention recently as they can be directly integrated in current CMOS technologies. Recent efforts to implement multi-phase interleaving have demonstrated the opportunity to eliminate the need for an external output capacitor. New technologies, such as trench capacitors, have enabled fully-integrated SC DC-DC converters that can achieve high power density of several W/mm^2 . These advantages have made SC DC-DC converters very promising solutions for low-cost, high efficiency on-chip power management. Improving the power density, power efficiency and reducing the output noise are the main challenges in SC DC-DC converter designs.

The objective of this research is to develop output voltage regulation techniques for switched-capacitor DC-DC converters to reduce the output voltage ripple, achieve high power conversion efficiency and fast transient response. SC DC-DC converters using on-chip flying capacitors are designed, which demonstrate the fully integration potential. With the increasing demand for self-powered intelligent devices in the IoT era, we extend the use of SC converters to energy harvesting

systems. Specifically, an on-chip SC DC-DC converter is designed for micro-power indoor photovoltaic (PV) energy harvesting.

The scope of this research includes:

- (i) Hysteretic control is popular for switched-capacitor (SC) DC-DC converters.

Conventional hysteretic controllers require either a large output capacitor or high speed output voltage detection for proper regulation. In this research, a lower boundary hysteretic control method is proposed to achieve optimal output voltage ripple by matching the output sampling frequency to the converter switching frequency across the entire load range. The converter responds instantly to step-up load transients that are smaller than six times the initial load current. To achieve small output voltage undershoot due to larger step-up load transients while using an output capacitance value on the same order as the converter's charge transferring capacitance, the sampling frequency jumps to its maximum value whenever the SC converter changes phase in two consecutive sampling cycles.

- (ii) The hysteretic control technique is extended to multiphase interleaved switched-capacitor DC-DC converters. Multiphase interleaving is an effective and popular technique to reduce the output voltage ripple of switched-capacitor DC-DC converters. This technique is especially useful for fully integrated SC converters, since the component count is no longer a serious concern and fragmenting capacitors does not introduce significant area or cost overhead. A conventional hysteretic controller uses a separate control loop for each converter core of the multiphase interleaved converter; hence it requires N comparators or one shared comparator that operates at $2N$ times the single phase switching frequency of a

N-phase interleaved converter. A hysteretic controller will be proposed, which uses three control boundaries, each of which is defined by a separate comparator. The first comparator compares the output voltage with a reference voltage, the output of which changes the phase number in the following clock cycle by a minimum step size to achieve tight regulation. The other two comparators enable the coarse operation mode for fast recovery whenever the output voltage crosses the higher or lower control boundaries due to load transients.

(iii) In order to provide clean supply voltages for noise sensitive applications, a LDO is commonly cascaded with a high efficiency switching mode DC-DC converter. The post-regulation architecture also benefits from the good line and load regulation and fast transient response of the LDOs. However, an additional buffer capacitor and power transistor are needed, which results in increased die area and additional external component. In this research, a step-down switched-capacitor DC-DC converter with in-phase output voltage regulation is proposed, which integrates a NMOS-LDO with the SC converter in both charging and discharging phases to suppress the output voltage ripple. An adaptive gate-slope technique is proposed to reduce the output glitches during phase transitions and a gate pre-charge technique is used to assist the turn-on of the regulated transistors when the respective phase begins.

(iv) Energy harvesting is a promising solution for miniaturized self-powered IoT devices. Conventional energy harvesting systems store the harvested energy in an intermediate energy buffer and use additional conversion stages to deliver the stored energy to the load. The energy conversions are commonly performed by inductive DC-DC converters with off-chip inductors, which are not favourable

for size constrained devices. In this project, a reconfigurable switched-capacitor (SC) DC–DC converter is proposed for indoor photovoltaic (PV) energy harvesting. To improve the overall energy efficiency, the first converter topology transfers the energy from the PV cell to the load in one conversion stage when the PV energy is available and the load is demanding energy. When the load demands no energy, the excess energy in the PV cell is stored in the buffer through the second topology. The third topology acts as the backup converter, which is enabled to deliver the stored energy to the load when the PV energy is not available.

1.4 Organization

This dissertation is organized as follows:

Chapter 1 introduces the power management in today's portable electronic devices and discusses the pros and cons of the three main types of voltage regulators for use in such devices. The need for energy-autonomous devices for IoT is also introduced.

Chapter 2 Reviews the fundamental operating principles of SC DC-DC converters and identifies the various power loss mechanisms. A DC model is introduced which provides a guidance for optimizing both passive and active component sizes and minimizing the switching losses. Various output regulation methods and noise reduction techniques in the literature are reviewed.

Chapter 3 presents the proposed hysteretic control with sampling frequency modulation to achieve optimal output voltage ripple and fast transient response.

Chapter 4 presents a multi-phase interleaved SC DC-DC converter with a proposed hysteretic control method.

Chapter 5 proposes the output ripple and noise suppression technique, which integrates a NMOS-LDO with the inherent switches of the SC power stage, in both converter switching phases.

In Chapter 6, an on-chip reconfigurable switched-capacitor DC-DC converter is proposed for indoor PV energy harvesting systems.

Chapter 7 concludes this thesis and provides discussion for future work direction.

Chapter 2 LITERATURE REVIEW

This Chapter starts with a brief discussion of the primary operating principles of switched-capacitor DC-DC converters. A generic model is introduced to further explain the behaviors and design tradeoffs of SC DC-DC converters. Various regulation techniques and output voltage ripple reduction techniques are reviewed.

2.1 Voltage Conversion Principle of Switched-Capacitor DC-DC

Converters

The voltage conversion ratio ($M_{VCR} = V_{out}/V_{in}$) of switched-inductor DC-DC converters, such as buck [27, 44], boost [28, 45] and buck-boost [29, 46] converters, can be varied continuously by simply changing the duty ratio while maintaining the same circuit topology. On the other hand, the voltage conversion ratio of a switched-capacitor (SC) DC-DC converter [37, 47] is determined by many factors, including primarily the circuit topology, the load current, the component sizing, the duty cycle and the switching frequency. The circuit topology determines the ideal no-load voltage conversion ratio of a SC DC-DC converter. For example, Figure 2.1 shows three different converter topologies which provide fixed no-load (i.e. $R_L = \infty$) voltage conversion ratios ($M_{VCR,NL}$) of 1/2, 1/3 and 2/3 respectively, regardless the switching frequency, duty cycle, capacitor or switch size. However, when a SC DC-DC converter is loaded, the actual voltage conversion ratio M_{VCR} will be less than $M_{VCR,NL}$ due to the inherent voltage drop to transfer charge to and/or from a capacitor through the switches. The theoretical maximum power efficiency of a SC DC-DC converter given by $\frac{V_{out}}{M_{VCR,NL}V_{in}}$ drops linearly with the output voltage, as will

be discussed in Section 2.3. Hence, a SC DC-DC converter with single topology is efficient only when V_{out} is close to the ideal no-load output voltage of $V_{out,NL} = M_{VCR,NL}V_{in}$. When high efficiency over a wide range of input or output voltage is required, multiple converter topologies must be used, giving rise to multi-ratio reconfigurable SC DC-DC converters [40, 47-49].

Without loss of generality, the fundamental voltage conversion principle of SC DC-DC converters is explained using the 1/2-converter in Figure 2.1 as an example. The typical 1/2-converter consists of a charge transferring capacitor (also called flying capacitor) C_{fly} , four power switches S_1 - S_4 and an output buffer capacitor C_{out} . The converter has two operating phases, Φ_1 and Φ_2 , corresponding to the charging and discharging phases of the flying capacitor.

The equivalent circuits of the 1/2-converter in both phases are shown in Figure 2.2(a) and Figure 2.2(b), respectively. During the charging phase (Φ_1), S_1 and S_3 are turned ON while S_2 and S_4 are OFF. The flying capacitor is connected in series between the input terminal and output terminal, therefore,

$$V_{Cfly,\Phi_1} = V_{in} - V_{out} \quad (2.1)$$

During the discharging phase (Φ_2), S_1 and S_3 are OFF while S_2 and S_4 are ON. The flying capacitor is connected in parallel with the output capacitor, therefore

$$V_{Cfly,\Phi_2} = V_{out} \quad (2.2)$$

Under no-load condition, no charge is transferred through the flying capacitor, the voltage across C_{fly} has no ripple. Hence

$$V_{Cfly,\Phi_1} = V_{Cfly,\Phi_2} \quad (2.3)$$

Equivalently

$$M_{VCR,NL} = \frac{V_{out}}{V_{in}} = \frac{1}{2} \quad (2.4)$$

Note that this no-load voltage conversion ratio is purely dependent on the circuit topology. Using the same method, the no-load voltage conversion ratio of any SC converter topology can be identified.

(a)

(b)

(c)

Figure 2.1 Switched-capacitor topologies with conversion ratios of (a) $M_{VCR,NL} = 1/2$;

(b) $M_{VCR,NL} = 1/3$; (c) $M_{VCR,NL} = 2/3$.

Figure 2.2 A 1/2-SC converter in (a) charging phase; (b) discharging phase.

While SC DC-DC converters with two operating phases are typical, it is possible to implement a SC converter with more operating phases, which potentially results in less number of flying capacitors needed for a specific voltage conversion ratio. This is especially beneficial if off-chip discrete capacitors are used [50]. Figure 2.3 shows a 3-phase SC DC-DC converter, which provides an ideal voltage conversion ratio of 1/4 using two flying capacitors [51]. The no-load voltage conversion ratio can be obtained by using the following three relationships:

In phase one (Φ_1):

$$V_{out} + V_{Cfly1} + V_{Cfly2} = V_{in} \quad (2.5)$$

In phase two (Φ_2):

$$V_{out} + V_{Cfly2} = V_{Cfly1} \quad (2.6)$$

In phase three (Φ_3):

$$V_{out} = V_{Cfly2} \quad (2.7)$$

Solving these three equations simultaneously results in

$$V_{out} = \frac{1}{4}V_{in} \quad (2.8)$$

$$\text{In } \Phi_1: V_{in} = V_{Cfly1} + V_{Cfly2} + V_{out}$$

$$\text{In } \Phi_2: V_{Cfly1} = V_{Cfly2} + V_{out}$$

$$\text{In } \Phi_3: V_{Cfly2} = V_{out}$$

Figure 2.3 A 3-phase SC converter with $M_{VCR,NL} = 1/4$ [51].

2.2 Current Delivery

A two-phase switched-capacitor DC-DC converter delivers current from the input to the output by charging the flying capacitor in one phase and discharging it in the other phase. The current delivery capability of a SC converter depends not only on the topology, but also on the size of the flying capacitor, the switch on-resistance, the switching frequency and duty cycle.

Consider the 1/2-SC converter in Figure 2.1 and assume that the equivalent resistance of all the power switches equals to R_{on} when they are conducting. Both the charging and discharging circuits of the converter are shown in Figure 2.4(a) and Figure 2.4(b), respectively. Figure 2.4(c) shows the corresponding waveforms of the charging and discharging currents and the voltage ripple across the flying capacitor. Typically the output capacitor is sufficiently large such that the output voltage ripple is relatively negligible compared to the voltage ripple across the

flying capacitor, hence the output voltage is assumed to be constant for the current delivery analysis.

Figure 2.4 (a) The 1/2-SC converter in charging phase; (b) The converter in discharging phase; (c) Operating waveforms.

The converter switching frequency is denoted as f_{sw} , which is the inverse of the switching period T_{sw} . The duty cycle which is defined as the fraction of time that the converter operates in the charging phase (Φ_1), is denoted as $D = \frac{t_{\Phi 1}}{T_{sw}}$. Conversely, $t_{\Phi 2} = (1 - D)T_{sw}$ is the time that the converter operates in the discharging phase (Φ_2) during each switching cycle. During the charging phase, the flying capacitor is connected between the input terminal and the output terminal. The voltage across C_{fly} is charged from $V_{Cfly,L}$ to $V_{Cfly,H}$ during this phase. The charging current is given by

$$I_{sc,\Phi 1}(t) = \frac{(V_{in} - V_{Cfly,L} - V_{out})}{2R_{on}} e^{-t/\tau} \quad (2.9)$$

where $\tau = 2R_{on}C_{fly}$. Therefore

$$V_{Cfly}(t) = V_{in} - V_{out} - 2R_{on}I_{sc,\Phi_1}(t) = V_{in} - V_{out} - (V_{in} - V_{Cfly,L} - V_{out})e^{-t/\tau} \quad (2.10)$$

At the end of phase one ($t = t_{\Phi_1} = DT_{sw}$),

$$V_{Cfly}(t_{\Phi_1}) = V_{Cfly,H} = V_{in} - V_{out} - (V_{in} - V_{Cfly,L} - V_{out})e^{-DT_{sw}/\tau} \quad (2.11)$$

During the discharging phase (Φ_2), the flying capacitor is connected in parallel with the output. In the equilibrium state, the voltage across C_{fly} must be discharged to $V_{Cfly,L}$ at the end of the discharging phase. The discharging current is given by

$$I_{sc,\Phi_2}(t) = \frac{V_{Cfly,H} - V_{out}}{2R_{on}} e^{-t/\tau} \quad (2.12)$$

Therefore

$$V_{Cfly}(t) = V_{out} + 2R_{on}I_{sc,\Phi_2}(t) \quad (2.13)$$

At the end of this phase ($t = t_{\Phi_2} = (1 - D)T_{sw}$),

$$V_{Cfly}(t_{\Phi_2}) = V_{Cfly,L} = V_{out} + (V_{Cfly,H} - V_{out})e^{-(1-D)T_{sw}/\tau} \quad (2.14)$$

Solving equations (2.11) and (2.14) yields

$$V_{Cfly,H} = \frac{\left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)}{1 - e^{-\frac{T_{sw}}{\tau}}} (V_{in} - 2V_{out}) + V_{out} \quad (2.15)$$

$$V_{Cfly,L} = \frac{e^{-\frac{(1-D)T_{sw}}{\tau}} \left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)}{1 - e^{-\frac{T_{sw}}{\tau}}} (V_{in} - 2V_{out}) + V_{out} \quad (2.16)$$

The voltage ripple across the flying capacitor is given by

$$\Delta V_{Cfly} = \frac{\left(1 - e^{-\frac{(1-D)T_{sw}}{\tau}}\right)\left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)}{1 - e^{-\frac{T_{sw}}{\tau}}} (V_{in} - 2V_{out}) \quad (2.17)$$

Hence the charge being delivered to the output in each switching period is given by

$$Q_{out} = 2C_{fly}\Delta V_{Cfly} \quad (2.18)$$

The average current delivered to the output is simply given by the charge delivered in each switching cycle multiplied by the switching frequency:

$$\begin{aligned} I_{out} &= 2C_{fly}\Delta V_{Cfly}f_{sw} \\ &= 4C_{fly}f_{sw} \left[\frac{\left(1 - e^{-\frac{(1-D)T_{sw}}{\tau}}\right)\left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)}{1 - e^{-\frac{T_{sw}}{\tau}}} \left(\frac{1}{2}V_{in} - V_{out}\right) \right] \end{aligned} \quad (2.19)$$

This equation (2.19) shows that the current delivery capability of the SC DC-DC converter is a function of the various design parameters including the size of the charge transferring capacitor C_{fly} , the switching frequency f_{sw} , the switch on-resistance R_{on} , and the duty cycle D . This equation also reveals an important trade-off between the current density and power efficiency when designing SC DC-DC converters. The converter is able to deliver more output current when the difference between the output voltage V_{out} and the ideal no-load voltage given by $\frac{1}{2}V_{in}$ is larger, which however reduces the power conversion efficiency.

When the switching frequency is slow such that $DT_{sw} \gg \tau$, and $(1-D)T_{sw} \gg \tau$, the output current is given by

$$I_{out}|_{f_{sw} \rightarrow 0} = 4C_{fly}f_{sw} \left(\frac{1}{2}V_{in} - V_{out}\right) \quad (2.20)$$

which increases linearly with the switching frequency and the flying capacitor size, and is independent of the duty cycle and the switch on-resistance. Intuitively, this is because given enough time, the flying capacitor will be completely charged and/or discharged regardless of the switch on-resistance. The switch resistance only affects the rate of charging and discharging processes, but not the amount of charge delivered to the flying capacitor and the output during the complete switching period. This operating region is referred to as the slow-switching limit (SSL) [52], as will be presented in Section 2.4.

On the other hand, when the switching frequency is fast, i.e. when $DT_{sw} \ll \tau$, and $(1 - D)T_{sw} \ll \tau$, using L'Hospital's rule, the output current is given by

$$I_{out}|_{f_{sw} \rightarrow \infty} = \frac{D(1-D)}{R_{on}} (V_{in} - 2V_{out}) \quad (2.21)$$

Equation (2.21) shows that at high switching frequency, the output current of the SC DC-DC converter is limited by the duty cycle and the switch on-resistance, and is independent of the switching frequency and the flying capacitor size. This operating region is referred to as fast-switching limit (FSL) [52].

With $C_{fly} = 1$ nF, $R_{on} = 0.1$ Ω , $V_{in} = 1.8$ V and $V_{out} = 0.85$ V, the output current I_{out} versus the switching frequency f_{sw} under different duty ratios D is plotted in Figure 2.5(a). It is seen that the output current increases linearly with switching frequency and is independent of the duty cycle when the low switching frequency is low, as equation (2.20) shows. However, at high switching frequency, the output current saturates and the maximum current delivery capability of the 1/2-converter is maximized when $D = 50\%$. This can be verified by solving

(a) $C_{fly} = 1 \text{ nF}$, $V_{out} = 0.85 \text{ V}$, $R_{on} = 0.1 \Omega$

(b) $R_{on} = 0.1$, $V_{out} = 0.85 \text{ V}$, $D = 0.5$

(c) $C_{fly} = 1 \text{ nF}$, $V_{out} = 0.85 \text{ V}$, $D = 0.5$

Figure 2.5 Output current vs switching frequency with (a) different duty ratios; (b) different flying capacitance; (c) different switch on-resistance.

$$\frac{\delta I_{out}|_{f_{sw} \rightarrow \infty}}{\delta D} = 0 \quad (2.22)$$

which results in $D = 0.5$. **Hence, it is desirable to operate this 1/2-SC converter with 50% duty cycle**, unless additional constraints preclude it.

Figure 2.5(b) shows the output current versus the switching frequency with different flying capacitor sizes. As expected, at low switching frequencies, a larger flying capacitor leads to higher output current delivery capability, since more charge is delivered to the output during each switching cycle. The output currents saturate at the same maximum value given by (2.21) when switching frequency increases due to the finite switch on-resistance, which limits the maximum output current delivery capability. Figure 2.5(c) shows that the output current is independent of the switch on-resistance at low switching frequency. However, as switching frequency increases, smaller switch on-resistance offers larger maximum output current delivering capability.

2.3 Power Efficiency and Loss Analysis

The power conversion efficiency and various loss mechanisms are discussed in this Section.

2.3.1 Intrinsic Power Efficiency

It is known that capacitive charge transfer through switches is an intrinsic lossy process even if the components are ideal [53]. Hence switched-capacitor DC-DC converters suffer from intrinsic energy loss when delivering current from the input to the output. Consider the same 1/2-converter as shown in Figure 2.1, the charge is extracted from the input only during the charging phase (Φ_1) and is given by

$$Q_{in} = C_{fly} \Delta V_{Cfly} \quad (2.23)$$

Therefore, the energy extracted from the input is

$$E_{in} = V_{in} Q_{in} = V_{in} C_{fly} \Delta V_{Cfly} \quad (2.24)$$

On the other hand, the total amount of energy delivered to the load during a complete switching cycle is given by

$$E_{out} = V_{out} Q_{out} = 2V_{out} C_{fly} \Delta V_{Cfly} \quad (2.25)$$

Therefore, the fundamental limit on the energy conversion efficiency of the 1/2-SC converter (excluding gate driving loss, parasitic bottom plate loss, leakage, control power and etc) is given by

$$\eta_{intrinsic} = \frac{E_{out}}{E_{in}} = \frac{V_{out}}{V_{in}/2} \quad (2.26)$$

This can be extended to any switched-capacitor DC-DC converter topologies. Given the converter topology (hence $M_{VCR,NL}$) and input voltage V_{in} , the intrinsic efficiency a SC DC-DC converters is given by

$$\eta_{intrinsic} = \frac{V_{out}}{V_{out,NL}} = \frac{V_{out}}{M_{VCR,NL} V_{in}} \quad (2.27)$$

where $V_{out,NL} = M_{VCR,NL} V_{in}$ is the ideal no-load output voltage.

Equation (2.27) shows that the intrinsic energy efficiency is only determined by the ratio of the actual output voltage to the no-load output voltage. Interestingly, the switching frequency, the duty cycle and the switch on-resistance play no role in determining the converter's intrinsic energy efficiency. However, this equation does not address the ability of the SC converter to achieve the particular output voltage

given from the topology, the input voltage and the required load current. Rearranging equation (2.19) gives

$$V_{out} = \frac{1}{2} V_{in} - I_{out} \frac{1 - e^{-\frac{T_{sw}}{\tau}}}{4C_{fly}f_{sw} \left(1 - e^{-\frac{(1-D)T_{sw}}{\tau}}\right) \left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)} \quad (2.28)$$

Figure 2.6 (a) plots the output voltage versus the switching frequency under different values of switch on-resistance with $C_{fly} = 1$ nF, $V_{in} = 1.8$ V, $D = 0.5$ and $I_{out} = 50$ mA. When the converter is delivering the constant output current, the output voltage increases with the converter switching frequency before it saturates at a maximum value when the switching frequency approaches the fast switching limit (FSL). The maximum achievable output voltage is given by

$$V_{out,max} = V_{out}|_{f_{sw} \rightarrow \infty} = \frac{1}{2} V_{in} - I_{out} \frac{R_{on}}{2D(1-D)} \quad (2.29)$$

which shows that higher maximum achievable output voltage is achievable with smaller switch on-resistance. Hence the maximum achievable intrinsic efficiency is higher when R_{on} is reduced, as shown in Figure 2.7(a). Equation (2.29) also shows that the maximum achievable output voltage is a function of the duty ratio D . Solving

$$\frac{\delta V_{out,max}}{\delta D} = 0 \quad (2.30)$$

gives $D = 0.5$. Figure 2.6(b) verifies that the maximum output voltage of this converter is the highest when the duty cycle is 50%. Figure 2.7(b) plots the maximum achievable intrinsic efficiency versus the duty ratio.

(a) $I_{out} = 50 \text{ mA}$, $C_{fly} = 1 \text{ nF}$, $D = 0.5$

(b) $I_{out} = 50 \text{ mA}$, $C_{fly} = 1 \text{ nF}$, $R_{on} = 0.1 \Omega$

Figure 2.6 Output voltage vs switching frequency with (a) different on-resistance;
(b) different duty ratio.

(a) $I_{out} = 50$ mA, $C_{fly} = 1$ nF, $D = 0.5$

(b) $I_{out} = 50$ mA, $C_{fly} = 1$ nF, $R_{on} = 0.5$ Ω

Figure 2.7 Maximum achievable intrinsic efficiency vs (a) switch on-resistance; (b) duty ratio.

The switching frequency of a SC converter does not affect the intrinsic efficiency, however, it affects the switching losses due to primarily the parasitic bottom plate capacitance of the flying capacitors and the gate capacitance of the power switches. This will be discussed in Section 2.3.3 and Section 2.3.4. Although a smaller R_{on} increases the maximum achievable intrinsic efficiency, it requires a larger switch size or gate overdrive voltage, both increase the associated switching loss.

2.3.2 Conduction Loss

The intrinsic power loss due to capacitive charge transfer through switches of a switched-capacitor DC-DC converter is dissipated in the power switches as conduction loss, which is the fundamental loss mechanism of SC DC-DC converters. The conduction loss is given by

$$P_{cond} = (E_{in} - E_{out})f_{sw} = (M_{VCR,NL}V_{in} - V_{out})I_{out} \quad (2.31)$$

Hence, having chosen the converter topology ($M_{VCR,NL}$), and the input voltage (V_{in}), the conduction loss is determined by the output voltage and the output current. It cannot be reduced by varying the switching frequency, the flying capacitor size, the switch on-resistance or any other design parameters. The only way to reduce the conduction loss and to improve the intrinsic efficiency $\eta_{intrinsic}$ is by choosing a topology that provides a no-load output voltage closer to the desired load voltage.

Multi-Ratio SC DC-DC Converters

In many applications, both the input and output voltages vary. For example, the output voltage of a Li-ion battery can drop from 4.2V to 2.6V as the battery drains. On the other hand, applications such as low power microprocessors using dynamic

voltage scaling (DVS) technique [54, 55] require the voltage regulators to provide a certain range of supply voltage.

Figure 2.8 (a) A reconfigurable 2/3, 1/2, 1/3 SC topology [49]; (b) Intrinsic efficiency versus output voltage.

To interface with a wide range of input voltage or generate a wide range of output voltage, reconfigurable switched-capacitor converter topologies that support multiple voltage conversion ratios are required [56, 57]. In [49], a reconfigurable SC converter that provides three no-load voltage conversion ratios of $2/3$, $1/2$ and $1/3$ was presented, as shown in Figure 2.8(a).

With $V_{in} = 1.8$ V, the intrinsic efficiency of this converter across the output voltage range of 0.35 V to 1.2 V is shown in Figure 2.8(b). Ideally, when V_{out} is in the range of [0.9V, 1.2V], the $2/3$ -configuration can be used, which gives an ideal no-load output voltage of 1.2 V. The intrinsic efficiency is 100% when $V_{out} = 1.2$ V, and drops to 75% when $V_{out} = 0.9$ V. The $1/2$ -configuration can be used to boost the intrinsic efficiency when the desired V_{out} drops below 0.9 V. Similarly, the $1/3$ -configuration can be used when V_{out} further drops below 0.6 V. When the converter is loaded, the actual V_{out} is always lower than the no-load output voltage, and the intrinsic efficiency will always be less than 100%.

It is usually not difficult to design a reconfigurable SC topology that support a small number of voltage conversion ratios. However, when more conversion ratios are needed, a systematic approach that allows one to construct a complex switched-capacitor configuration from some simple unit SC cells is highly desirable. In [58], a successive approximation (SAR) SC topology, which cascades several $1/2$ -SC unit cells to provide a large number of conversion ratios, was proposed. However, cascading the converter stages results in low overall conversion efficiency and current density is limited to that of a single stage. The capacitance utilization can be low for many conversion ratios. A recursive switched capacitor (RSC) DC-DC converter topology was proposed in [48]. As shown in Figure 2.9, each SC cell

generates an intermediate voltage V_{MID} between the high input voltage V_H and the low input voltage V_L :

$$V_{MID} = \frac{1}{2}(V_H + V_L) \quad (2.32)$$

Figure 2.9 Generating multiple conversion ratios from unit SC cells [48].

A voltage of $\frac{1}{2}V_{in}$ can be simply generated from a unit SC cell by connecting its two input ports to V_{in} and the ground, respectively. To generate a voltage of $\frac{1}{4}V_{in}$, a second SC cell can be used by connecting its higher input port and lower input port

to $\frac{1}{2}V_{in}$ and ground respectively. Similarly, connecting a SC cell between V_{in} and $\frac{1}{2}V_{in}$ produces an ideal no-load output voltage of $\frac{3}{4}V_{in}$. Note that each RSC unit cell must be at least two-phase interleaved to provide charge balance, otherwise, a buffer capacitor will be required at the output of each cell.

It can be shown that up to 2^N-1 voltage conversion ratios can be realized from N unit SC cells. The RSC approach is expected to be more efficient than the SAR approach since it allows connecting the unit SC cells in parallel, which maximizes the number of connections to V_{in} and ground, hence the charge transferred through the flying capacitors is maximized. The flying capacitors and power transistors of each SC cell can be optimally sized such that SC cells that carry the higher current are allocated with the proportionally larger capacitance and switch width. For example, when the converter is configured for $M_{VCR,NL} = 1/4$, one can find that the RSC cell 2 handles double the amount of charge than that handled by RSC cell 1. Hence, it is desirable to design cell 2 with double the size of cell 1.

2.3.3 Switching Loss Due to Bottom Plate Parasitic Capacitors

In addition to the conduction loss, a switched-capacitor DC-DC converter suffers from switching power losses due to the charging and discharging of the various parasitic capacitances in the SC converter in every switching cycle. These switching losses are directly proportional to the switching frequency. The first major contributor of the switching losses is the parasitic bottom plate capacitance of the flying capacitors. In Figure 2.10, the bottom plate parasitic capacitance of C_{fly} is denoted as $C_{bottom} = \alpha C_{fly}$ [33, 59]. The voltage across C_{bottom} is charged to V_{out} during the charging phase (Φ_1) and discharged to zero volt during the discharging

phase (Φ_2). The energy loss due to the bottom plate capacitor in every switching cycle is

Figure 2.10 A 1/2-SC converter with bottom plate parasitic capacitance.

$$E_{bottom} = C_{bottom} V_{out}^2 = \alpha C_{fly} V_{out}^2 \quad (2.33)$$

therefore

$$P_{bottom} = C_{bottom} V_{out}^2 f_{sw} \quad (2.34)$$

Since the C_{bottom} is charged by the output, the energy of which has already been transferred from the input with an efficiency of $\eta_{intrinsic}$, the switching power loss seen by the input is

$$P_{in,bottom} = \frac{C_{bottom} V_{out}^2 f_{sw}}{\eta_{intrinsic}} = \frac{\alpha C_{fly} V_{out} V_{in} f_{sw}}{2} \quad (2.35)$$

In general, the bottom plate power loss of a SC converter referred to the input can be expressed as

$$P_{in,bottom} = \sum_i \gamma_i C_{bottom,i} (\Delta V_{bottom,i})^2 f_{sw} \quad (2.36)$$

where $\Delta V_{bottom,i}$ is the voltage swing across the parasitic bottom plate capacitance ($C_{bottom,i}$) of the i^{th} flying capacitor, and γ_i is a constant that refers the bottom plate loss to the input and is determined by the converter topology.

2.3.4 Gate Switching Loss

Another major component of power losses in a SC DC-DC converter is associated with switching the power switches ON and OFF periodically. The loss originates from charging the and discharging of gate capacitances of the power MOSFETs and can be estimated as

$$P_{gate} = \sum_i C_{gate,i} V_{gate,i}^2 f_{sw} \quad (2.37)$$

where $C_{gate,i}$ is the total gate capacitance of the i^{th} MOS switch and $V_{gate,i}$ is the voltage swing at the gate of the switch. The gate switching loss can be referred to the input as

$$P_{in,gate} = \sum_i \rho_i C_{gate,i} V_{gate,i}^2 f_{sw} \quad (2.38)$$

where ρ_i is a constant determined by the gate driving mechanism.

While the conduction loss can't be reduced once the converter topology is chosen and the input and output voltages and the output current are fixed, the bottom-plate and gate-capacitor switching losses can be optimized by operating the SC converter at the corner frequency between the SSL and FSL. This will be discussed in Section 2.5 with the aid of the output impedance model, which is presented next in Section 2.4.

2.4 Modelling Switched-Capacitor DC-DC Converters

The design of a switched-capacitor DC-DC converter is a complex, multi-dimensional task involving various tradeoffs. A generic model is helpful to interpret the key common behaviors of SC DC-DC converters.

2.4.1 Output Impedance Model

The steady state operation of switched-capacitor DC-DC converters can be understood and analyzed using a DC model as shown in Figure 2.11 [52, 60-62]. A SC converter can be viewed as an ideal DC-transformer with turns ratio equal to the no-load voltage conversion ratio ($M_{VCR,NL}$), and a finite output impedance R_{out} . The voltage difference between the actual loaded output voltage and the ideal no-load output voltage is equivalent to the voltage drop across R_{out} . The output voltage can be expressed as:

$$V_{out} = M_{VCR,NL} V_{in} - I_{out} R_{out} = V_{out,NL} - I_{out} R_{out} \quad (2.39)$$

Considering the 1/2-SC converter in Figure 2.4, the output voltage derived in equation (2.3.6) is repeated below:

$$V_{out} = \frac{1}{2} V_{in} - I_{out} \frac{1 - e^{-\frac{T_{sw}}{\tau}}}{4C_{fly}f_{sw} \left(1 - e^{-\frac{(1-D)T_{sw}}{\tau}}\right) \left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)} \quad (2.40)$$

Fitting this equation into the model in Figure 2.11, one can find that the equivalent series output resistance of this converter is given by

$$R_{out} = \frac{1 - e^{-\frac{T_{sw}}{\tau}}}{4C_{fly}f_{sw} \left(1 - e^{-\frac{(1-D)T_{sw}}{\tau}}\right) \left(1 - e^{-\frac{DT_{sw}}{\tau}}\right)} \quad (2.41)$$

Figure 2.11 Output impedance model of SC DC-DC converters [52, 60-62].

Figure 2.12 plots R_{out} as a function of switching frequency on a log-log graph with different size of C_{fly} and switch on-resistance R_{on} when $D = 50\%$. It is seen that R_{out} has two asymptotic limits, namely the slow switching limit (SSL) and the fast switching limit (FSL) [52, 60, 61].

At low switching frequency (SSL), where $\tau = 2R_{on}C_{fly} \ll \frac{1}{2}T_{sw}$, the equivalent series output resistance of the 1/2-SC converter is given by

$$R_{out} = R_{SSL} = \lim_{\frac{T_{sw}}{2\tau} \rightarrow \infty} \left(\frac{1}{4C_{fly}f_{sw}} \frac{1+e^{-\frac{T_{sw}}{2\tau}}}{1-e^{-\frac{T_{sw}}{2\tau}}} \right) = \frac{1}{4C_{fly}f_{sw}} \quad (2.42)$$

The equivalent output resistance in SSL is only dependent on the switching frequency and the size of the flying capacitor, and is independent of the value of the switch on-resistance. As the switching frequency increases, the operation of the SC converter approaches the FSL, and the effect of the switch on-resistance becomes non-negligible. Eventually, when $\tau \gg \frac{1}{2}T_{sw}$,

$$R_{out} = R_{FSL} = \lim_{\frac{T_{sw}}{2\tau} \rightarrow 0} \left(\frac{1}{4C_{fly}f_{sw}} \frac{1+e^{-\frac{T_{sw}}{2\tau}}}{1-e^{-\frac{T_{sw}}{2\tau}}} \right) = 2R_{on} \quad (2.43)$$

Figure 2.12 Output impedance versus switching frequency.

The minimum output impedance is limited by the switch on-resistance and is independent of the switching frequency.

In [52], a systematic approach for calculating the equivalent output impedance in both asymptotic limits of a two-phase SC DC-DC converter is presented. Using this approach, the output impedance in the slow-switching limit (SSL) is given by

$$R_{SSL} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \quad (2.44)$$

where $a_{c,i} = q_{c,i}/q_{out}$ is defined as the ratio of the charge $q_{c,i}$ being processed by each capacitor, to the charge q_{out} being delivered to the output during the entire switching period.

The output impedance in the fast-switching limit (FSL) with 50% duty cycle is given by

$$R_{FSL} = 2 \sum_i R_{on,i} (a_{r,i})^2 \quad (2.45)$$

where $a_{r,i} = q_{r,i}/q_{out}$ is defined as the ratio of the charge $q_{r,i}$ that flows through the i^{th} switch during the phase when it is conducting to the charge q_{out} being delivered to the output during the full period.

Both $a_{c,i}$ and $a_{r,i}$ are switched-capacitor topology dependent. C_i and $R_{on,i}$ are the size of each flying capacitor and the resistance of each switch when it's conducting. The output impedance across the entire range of switching frequency can be approximated by [52, 61]

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (2.46)$$

This approach can be extended to find the output impedance of a general n-phase SC DC-DC converter [63]:

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^n \frac{(a_{c,i}^j)^2}{2C_i f_{sw}} \quad (2.47)$$

$$R_{FSL} = \sum_{i \in switches} \sum_{j=1}^n \frac{R_{on,i}}{D_j} (a_{r,i}^j)^2 \quad (2.48)$$

where $a_{c,i}^j$ is ratio of the charge being transferred by capacitor c_i during j^{th} operating phase to the charge being delivered to the output during the entire switching period; D_j is the duty cycle of the j^{th} phase; and $a_{r,i}^j$ is as the ratio of the charge that flows through i^{th} switch during j^{th} phase to the charge being delivered to the output during the complete switching cycle.

Example: Consider the two-phase voltage divider as shown in Figure 2.4, denote the charge being delivered to the output during the full period by q_{out} , then $q_{out}/2$ of charge is being transferred to the output through the flying capacitor in both phase one and phase two. We have

$$a_c = \frac{q_{out}/2}{q_{out}} = \frac{1}{2} \quad (2.49)$$

From equation (2.44), we have

$$R_{SSL} = \frac{(\frac{1}{2})^2}{C_{fly}f_{sw}} = \frac{1}{4C_{fly}f_{sw}} \quad (2.50)$$

which is identical to the equation (2.42).

The charge flowing through each of the four switches when they are conducting is also $q_{out}/2$, therefore we have

$$a_{r,i} = \frac{1}{2} \quad (2.51)$$

for $i = 1, 2, 3, 4$. From equation (2.45), if all switches have the same on resistance R_{on} , assuming 50% duty cycle, we have

$$R_{FSL} = 2 \sum_{i=1}^4 R_{on} \left(\frac{1}{2}\right)^2 = 2R_{on} \quad (2.52)$$

which is identical to equation (2.43).

2.4.2 Capacitor and Switch Size Optimization

Silicon area is one of the most critical constraints when designing SC DC-DC converters. For a fully on-chip SC DC-DC converter (excluding the output buffer capacitor), the largest portion of the area is occupied by the flying capacitors. On

the other hand, if discrete external flying capacitors are used, the power transistors typically occupy the largest portion of the die area. Therefore, in a capacitor-limited design, the capacitor utilization must be optimized to achieve the best converter performance with a given constraint on the total capacitor area, or equivalently, the total on-chip capacitance C_{tot} . Similarly, in a switch-limited design, the utilization of the switches must be maximized to obtain the best performance out of a given total switch area, or equivalently, the total switch conductance G_{tot} . One way to optimize the capacitor and switch utilization is through minimizing the output impedance of the SC DC-DC converter in the slow switching limit and fast switching limit, respectively.

According to [52], if all flying capacitors in a SC converter are rated for the same voltage, and the constraint on the total flying capacitance is C_{tot} , the output impedance of a two-phase SC DC-DC converter in the SSL can be minimized if the size of each individual capacitor is given by

$$C_i = \frac{|a_{c,i}|}{\sum_k |a_{c,k}|} C_{tot} \quad (2.53)$$

which results in the optimized SSL output impedance of

$$R_{SSL}^* = \frac{1}{C_{tot} f_{sw}} (\sum_i |a_{c,i}|)^2 \quad (2.54)$$

The switch utilization is maximized by minimizing the output impedance in the fast switching limit R_{FSL} . If all power switches are rated for the same voltage, then R_{FSL} can be minimized when the power transistors are sized such that the conductance of each power switch is

$$G_i = \frac{|a_{r,i}|}{\sum_k |a_{r,k}|} G_{tot} \quad (2.55)$$

The optimized FSL output impedance is

$$R_{FSL}^* = \frac{2}{G_{tot}} \left(\sum_i |a_{r,i}| \right)^2 \quad (2.56)$$

2.5 Switching Loss Minimization

Section 2.3 presents three dominant power losses in a switched-capacitor DC-DC converter, they are conduction loss, switching loss due to the bottom plate parasitic capacitance of the flying capacitors and switching loss due to driving the gate of the power switches. As shown in Section 2.3.2, once the conversion ratio ($M_{VCR,NL}$), the input voltage (V_{in}), the output voltage (V_{out}) and output current (I_{out}) are fixed, the conduction loss is also fixed. The conduction loss can only be reduced by changing the converter topology or $M_{VCR,NL}$.

On the other hand, the bottom plate loss and the gate switching loss can be minimized by operating the converter at an optimal operating point around the corner frequency at the crossing of the slow switching limit and the fast switching limit on the output impedance curve. Moreover, a specific voltage conversion ratio may be implemented by different converter topologies, which often result in different switching losses. Therefore proper topology selection is also important for switching loss minimization.

2.5.1 Topology Selection

A specific voltage conversion ratio can often be realized by different converter topologies, which can lead to different bottom plate losses [51]. For example, Figure 2.13 shows two alternative implementations to achieve the same voltage

conversion ratio of $M_{VCR,NL} = 1/2$. As discussed in Section 2.3.3, the first implementation shown in Figure 2.13(a) results in bottom plate loss of

$$P_{bottom,a} = \alpha f_{sw} C_{fly,a} V_{out}^2 \quad (2.57)$$

The bottom plate loss of the second implementation shown in Figure 2.13(b) is due to the bottom plate parasitic capacitor ($\alpha C_{fly,b1}$) of $C_{fly,b1}$. This parasitic capacitor is charged to $\frac{1}{2}V_{in}$ during the first phase (Φ_1), and discharged to ground during the second phase (Φ_2). Therefore, the bottom plate power loss of this topology is

$$P_{bottom,b} = \alpha f_{sw} C_{fly,b1} \left(\frac{1}{2}V_{in}\right)^2 \cong \alpha f_{sw} C_{fly,b1} V_{out}^2 \quad (2.58)$$

For fair comparison, the flying capacitors in both implementations must be sized such that both implementations result in the same current delivery capability. Using the output impedance model presented in Section 2.4, and use $C_{fly,b1} = C_{fly,b2} = C_{fly,b}$, the output impedances of the two implementations in SSL are given by

$$R_{SSL,a} = \frac{1}{4C_{fly,a}f_{sw}} \quad (2.59)$$

and

$$R_{SSL,b} = \frac{1}{2C_{fly,b}f_{sw}} \quad (2.60)$$

respectively. Hence $C_{fly,b} = 2C_{fly,a}$ for the same converter performance, which results in

$$P_{bottom,b} = 2P_{bottom,a} \quad (2.61)$$

Therefore, in order to reduce the bottom plate switching loss, the implementation shown in Figure 2.13(a) is preferred over that shown in Figure 2.13(b).

(a)

(b)

Figure 2.13 Alternative implementations of a 1/2-SC DC-DC converter.

2.5.2 Operating Point Optimization

Section 2.4 presents two asymptotic limits of equivalent series output impedance of a switched-capacitor DC-DC converter, namely R_{SSL} and R_{FSL} . The overall output impedance is approximated by [52, 61]

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (2.62)$$

Using this expression, the operating point of a SC DC-DC converter on the output impedance curve can be described using an output impedance balance factor β ($0 \leq \beta \leq 1$) [42], where

$$R_{SSL} = \sqrt{\beta} R_{out} \quad (2.63)$$

and

$$R_{FSL} = \sqrt{1 - \beta} R_{out} \quad (2.64)$$

The overall switching loss including the bottom plate loss and the gate driving loss can be minimized by choosing the optimal value of β . Intuitively, when the converter operates in the fast-switching limit, further increasing the frequency does not help to reduce the output impedance, however the switching loss increases, reducing the overall efficiency. On the other hand, if the converter is operating in the slow switching limit, the output impedance is independent of the switch on-resistance. In other words, it is desirable to reduce either the width or gate-to-source voltage (V_{gs}) of the power switches to reduce the gate driving loss without affecting the overall output impedance. Hence an optimized SC converter should operate around the corner frequency at the crossing of the SSL and the FSL asymptotic limits [42, 64]. The optimal value of β can be derived as follows.

When a SC converter is regulated, as will be discussed in Section 2.6, the desired value of R_{out} is determined by

$$R_{out,desired} = \frac{M_{VCR,NL} V_{in} - V_{out,desired}}{I_{out}} \quad (2.65)$$

which is fixed once the topology is chosen and the input voltage, output voltage and output current are specified. Substituting (2.63) into (2.54) gives

$$f_{sw} = \frac{(\sum_i |a_{c,i}|)^2}{\sqrt{\beta} R_{out,desired} C_{tot}} \quad (2.66)$$

Substituting (2.65) into (2.55) and (2.56) gives

$$G_i = \frac{|a_{r,i}|}{\sum_k |a_{r,k}| \sqrt{1-\beta} R_{out,desired}} \frac{2(\sum_i |a_{r,i}|)^2}{\sqrt{1-\beta} R_{out,desired}} \quad (2.67)$$

Since the power switches are expected to operate in the triode region while they are conducting, assume all power transistors have the length of same length L , this switch conductance value corresponds to a power transistor width of:

$$W_i = \frac{G_i L}{K_p (V_{gs,i} - V_{th})} = \frac{\frac{|a_{r,i}|}{\sum_k |a_{r,k}| \sqrt{1-\beta} R_{out,desired}} \frac{2(\sum_i |a_{r,i}|)^2}{\sqrt{1-\beta} R_{out,desired}} L}{K_p (V_{gs,i} - V_{th})} \quad (2.68)$$

where K_p is the technology constant, $V_{gs,i} - V_{th}$ is the gate overdrive voltage when the power transistor is ON. The gate capacitance can be expressed as:

$$C_{gate,i} = C_{sq} \frac{\frac{|a_{r,i}|}{\sum_k |a_{r,k}| \sqrt{1-\beta} R_{out,desired}} \frac{2(\sum_i |a_{r,i}|)^2}{\sqrt{1-\beta} R_{out,desired}} L^2}{K_p (V_{gs,i} - V_{th})} \quad (2.69)$$

where C_{sq} denotes the gate capacitance of a unit size transistor.

The bottom plate loss and gate switching losses can be expressed in terms of the output impedance balance factor β :

$$P_{bottom} = \frac{(\sum_i |a_{c,i}|)^2}{\sqrt{\beta} R_{out,desired} C_{tot}} \sum_i C_{bottom,i} V_{bottom,i}^2 = \frac{K_{bottom}}{\sqrt{\beta}} \quad (2.70)$$

and

$$\begin{aligned}
 P_{gate} &= \frac{(\sum_i |a_{c,i}|)^2}{\sqrt{\beta} R_{out,desired} C_{tot}} \frac{2(\sum_i |a_{r,i}|)^2}{\sqrt{1-\beta} R_{out,desired}} \sum_i V_{gate,i}^2 C_{sq} \frac{\frac{|a_{r,i}|}{\sum_k |a_{r,k}|} L^2}{K_p (V_{gs,i} - V_{th})} \\
 &= \frac{K_{gate}}{\sqrt{\beta} \sqrt{1-\beta}}
 \end{aligned} \tag{2.71}$$

The total switching loss is given by

$$P_{loss} = P_{bottom} + P_{gate} = \frac{K_{bottom}}{\sqrt{\beta}} + \frac{K_{gate}}{\sqrt{\beta} \sqrt{1-\beta}} \tag{2.72}$$

Therefore, the optimal value of β that minimizes the overall switching loss can be found by solving the differential equation:

$$\frac{\partial P_{loss}}{\partial \beta} = 0 \tag{2.73}$$

2.6 Regulation of Switched-Capacitor DC-DC Converters

Many applications require the DC-DC converters to provide stable supply voltages. Therefore, the switched capacitor DC-DC converters must be regulated to maintain the desired output voltage under varying line and/or load conditions. Using the output impedance model

$$V_{out} = M_{VCR,NL} V_{in} - I_{out} R_{out} \quad (2.74)$$

it is seen that the output voltage of a switched capacitor DC-DC converter can be controlled by adjusting either the conversion ratio $M_{VCR,NL}$ or the equivalent series output impedance R_{out} to compensate for any variations in the input voltage V_{in} or load current I_{out} . The $M_{VCR,NL}$ can be changed only by reconfiguring the switched-capacitor topology, and it can only take discrete values, resulting in coarse regulation of the output voltage [35, 65-69]. The purpose of reconfiguring the conversion ratio is mainly to provide reasonable efficiency over a certain range of input or output voltages. It is usually combined with regulation techniques that adjust the output impedance R_{out} continuously to achieve fine output voltage regulation. The expressions of R_{out} in both SSL and FSL are repeated below.

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^n \frac{(a_{c,i}^j)^2}{2C_i f_{sw}} \quad (2.75)$$

$$R_{FSL} = \sum_{i \in switches} \sum_{j=1}^n \frac{R_{on,i}}{D_j} (a_{r,i}^j)^2 \quad (2.76)$$

Various design parameters including the switching frequency f_{sw} , the flying capacitance C_i , the switch on-resistances $R_{on,i}$ and the duty cycle D_j can be used as the control variables to modify the equivalent output resistance of a SC DC-DC

converters. When the SC converter is operating in the slow switching limit (SSL), its equivalent output resistance can be controlled by varying the switching frequency or the size of the flying capacitance. When it's operating at fast switching limit (FSL), the output resistance can be controlled by varying the switch on-resistance or the duty cycle. When the converter is operating around the corner frequency at the crossing the SSL and FSL limits, all the above mentioned variables be used to adjust the output impedance. Adjusting these parameters regulates the SC converter directly. In noise sensitive applications such as analog and RF circuits, low noise supply rail is required. Therefore, it is often necessary to post-regulate a switched-capacitor DC-DC converter by cascading a low-dropout regulator (LDO) at the output of the converter to suppress the output voltage ripple and high frequency switching noise, and to improve the line and load regulation and transient response [70-72]. However, additional components are needed and the power efficiency is compromised.

2.6.1 Switching Frequency Modulation

Switching frequency is the most commonly used parameter to regulate the output voltage of a switched-capacitor DC-DC converter based on the dependence of the equivalent output impedance on the switching frequency in the slow-switching limit. Switching frequency modulation is preferred when high power conversion efficiency must be maintained over a wide range of load currents. However the switching frequency modulation suffers from the main drawback of generating noise with unpredictable spectrum [33].

2.6.1.1 Continuous Pulse Frequency Modulation

The switching frequency of switched-capacitor DC-DC converter can be controlled continuously using the conventional linear control method [73, 74]. An example implementation of the continuous PFM modulation is shown in Figure 2.14 [74]. The negative feedback regulation loop consists of the SC power stage, a feedback network consisting of R_{f1} and R_{f2} , an error amplifier with frequency compensation, a voltage controlled oscillator (VCO), and a non-overlap gate signal generator and driving circuit. The error amplifier senses the difference between feedback output voltage βV_{out} and the reference voltage V_{ref} . The output of the error amplifier V_e controls the switching frequency through the VCO, as shown in Figure 2.14(b). The negative feedback loop sets the desired output voltage at

$$V_{out,desired} = \left(1 + \frac{R_1}{R_2}\right) V_{ref} = \frac{1}{\beta} V_{ref} \quad (2.77)$$

When βV_{out} is smaller than V_{ref} , V_e increases and the switching frequency generated by the VCO is increased. As a result, more current is delivered to the output until V_{out} reaches the desired value. Similarly, when βV_{out} is larger than V_{ref} , the switching frequency is reduced.

The main drawback of the linear PFM modulation is that the unity-gain bandwidth of the regulation loop is typically limited to less than one fifth of the converter switching frequency to ensure the loop stability. Hence the dynamic response of the converter is slow. Due to this reason, the continuous time PFM method is not commonly used in regulated SC DC-DC converters.

(a)

(b)

Figure 2.14 (a) A 1/2-SC DC-DC converter with PFM control; (b) A voltage controlled oscillator [74].

2.6.1.2 Hysteretic Frequency Modulation

Most of the regulated switched-capacitor DC-DC converters in the literature adjust the switching frequency using hysteretic regulation technique [41, 42, 59, 65, 66, 69, 75, 76]. Hysteretic controller, also known as "bang-bang controller", is a comparator based control method. It enables the switching activity of the SC converter each time the output voltage falls below a certain control boundary.

Figure 2.15(a) shows the architecture of a dynamic comparator based single boundary hysteretic control [42]. The dynamic comparator operates with a sampling clock clk_{sample} with frequency of f_{sample} . At the rising/falling edge of the sampling clock, the output voltage V_{out} is sampled and compared to the reference voltage V_{ref} . When the sampled V_{out} is lower than V_{ref} , the comparator generates a pulse at the output which is identical to the sampling clock pulse, as shown in Figure 2.15(b). This comparator output acts as the clock to a T-latch with T input terminal tied to 1 (logic). Therefore, whenever a pulse is generated at the comparator output, the T-latch toggle the state of its output, V_{sw} , which is passed to the non-overlap gate signal generation and driving circuits to control the power switches. Hence whenever the sampled output voltage is smaller than the reference voltage, the SC power stage changes its phase to trigger charge transfer to the load in order to increase V_{out} until it is above V_{ref} . When the sampled V_{out} is greater than V_{ref} , no pulse is generated at the comparator output, hence the SC power stage does not change its phase during the sampling clock cycle. In other words, the sampling clock pulse is skipped for converter switching activity, therefore, hysteretic control is one type of pulse skipping modulation. As the load continuously draws current from C_{out} , the output voltage drops and when V_{out} becomes smaller than V_{ref} again, another phase change, hence charge transfer, of the power stage is triggered.

(a)

(b)

Figure 2.15 (a) A 1/2-SC DC-DC converter with hysteretic control architecture; (b) Operating waveforms [42].

Compared to the linear PFM method, hysteretic regulation provides inherent closed-loop stability for all loads without the need for a compensation circuit. Since the control loop reacts to any output voltage change due to load transients immediately after the propagation delay of the comparator, dead-time generator, and gate driver,

hysteretic SC converters can achieve fast load transient response. Therefore, hysteretic architecture is popular for regulation of SC DC-DC converters. However, without a high gain error amplifier, the DC set point of the output voltage is not as precise as can be achieved with continuous PFM architecture.

2.6.2 Pulse Width Modulation

Pulse width modulation (PWM), which is commonly used for regulation of inductor-based DC-DC converters [77], can also be used to regulate switched-capacitor DC-DC converters [78-84]. Compared to the switching frequency modulation, the PWM control strategy has the advantage of being constant frequency operation, hence it generates predictable EMI noise. Unlike the inductor-based DC-DC converters, the PWM method does not change the nominal conversion ratio ($M_{VCR,NL}$) of the SC converter. Instead, this method regulates the output voltage of a SC converter by terminating the charge transfer from the input to the flying capacitor prematurely during the charging phase. Hence the output voltage is regulated by controlling the amount of charge delivered to the output during each switching cycle.

A 1/2-SC DC-DC converter can be regulated using PWM control as shown in Figure 2.16. The operation of the converter in each switching cycle ($t = 0 \rightarrow T_{sw}$) can be divided into three phases. In the first phase, ($t = 0 \rightarrow T_{ON}$), M_{P1} and M_{P2} are turned on, the flying capacitor C_{fly} is being charged from the input supply. The duration of this phase, denoted by T_{ON} , is controlled by the negative feedback circuit. If the output voltage drops below the desired value $V_{out,desired} = \frac{1}{\beta} V_{ref}$, due to a drop in input voltage or increase in load current, the output of the error amplifier V_e increases. As a result, T_{ON} is increased such that more charge is delivered to C_{fly} and

the converter output during each switching cycle, increasing the output voltage. On the other hand, T_{ON} will be reduced when the output voltage increases due to, for example, an increase in input voltage or a decrease in the load current. In the second phase ($t=T_{ON} \rightarrow 0.5T_{sw}$), M_{P1} is turned OFF and the voltage across C_{fly} remains unchanged. In phase three ($t=0.5T_{sw} \rightarrow T_{sw}$), M_{N1} and M_{N2} are turned ON, C_{fly} is connected in parallel with the output, releasing the charge that is extracted from the input during phase one to the output.

One of the main problems of PWM method for SC DC-DC converters is the limited control width for proper regulation. In order to effectively control the amount of charge transferred to C_{fly} , T_{ON} must not be too large compared to the time constant (τ) of charging the flying capacitor. If $T_{ON} \gg \tau$, the flying capacitor is already being fully charged before the end of the charging process, varying T_{ON} will not change the amount of charge being delivered to the capacitor and therefore, the output voltage cannot be regulated properly. Hence achieving output voltage regulation across a wide range of load current is difficult due to the prohibitively small duty cycle (T_{ON}/T_{sw}) at low loads.

Since the switching frequency can be kept constant with PWM control, the EMI noise generated by the SC converter is predictable and easier to be filtered. However the constant switching frequency results in constant switching losses due to both the bottom plate parasitic capacitance of the flying capacitors and the gate capacitance. Therefore it results in low overall conversion efficiency of the power converter when the load current is small.

(a)

(b)

Figure 2.16 (a) A 1/2-SC DC-DC converter with PWM control; (b) Operating waveforms.

2.6.3 Capacitance and Switch Resistance Modulation

Variable frequency control methods helps to maintain high power conversion efficiency across a wide range of load current, however they introduce

unpredictable noise spectrum. The constant switching frequency PWM regulation method, as presented in Section 2.6.2, however suffers from low efficiency at small loads. In [85], a switch resistance control scheme is presented by segmenting the switches into multiple switch banks, and the total width of the MOS power transistors can be increased or decreased by digitally adjusting the number of switch banks that are used for charge delivery. However, since the same amount of flying capacitance is switched at all loads, the bottom-plate switching loss does not scale with load current.

In [33], a digital capacitance modulation (DCpM) control method is presented which implements output voltage regulation by controlling the flying capacitor size as well as the switch size that take part in the charge transfer. A simplified implementation of the DCpM is shown in Figure 2.17, where each switch and/or flying capacitor is divided into four different banks of sizes 1X, 2X, 4X and 8X. A 4-bit signal $EN_{<0:3>}$ is used to enable the corresponding switch and/or capacitor bank. Using this method, the flying capacitance can be adjusted in steps of $1C_B$ and the width of the power switch can be adjusted in steps of $1W$. By reducing the size of C_{fly} and the width of the power switches as load current decreases, the switching losses due to both the flying capacitor bottom plate parasitic and gate capacitance can be reduced while the switching frequency remains constant. In [33], a FINE switch-capacitor bank is used to further split the flying capacitance in steps of $C_B/7$ and split the switch size in steps of $W/7$ when fine regulation of output voltage is required. Nonetheless, only discrete values of capacitance are achievable, this method is not suitable when tight regulation is required.

Figure 2.17 A 1/2-SC DC-DC converter with capacitance and switch resistance modulation [33].

2.6.4 Post-Regulation using Series LDO

The regulation methods presented in Section 2.6.1 to 2.6.3 regulate the output voltage of the switched-capacitor DC-DC converters directly. These regulation methods do not suppress the output voltage ripple and switching noise during converter phase transitions, therefore low-dropout regulators (LDOs) with high power supply rejection are commonly cascaded with the SC DC-DC converters to provide the required supply voltages for analog and RF circuits [70-72, 86, 87].

Moreover, good load regulation and fast transient response can be achieved. Figure 2.18 shows an implementation of post-regulation using a conventional PMOS-LDO. Since the LDO is not coupled to the switching converter, the LDO requires sufficient drop-out voltage to ensure good ripple rejection under all load current conditions, which increases the power loss. In [72], A NMOS-LDO is used to suppress the switching noise of a SC DC-DC converter. The switching frequency and switch size are made adaptive to load current to improve the light load efficiency.

Figure 2.18 A 1/2-SC DC-DC converter with capacitance and switch resistance modulation.

2.6.5 Current Control Schemes and Switching Low Dropout Regulators

The post-regulation method in Section 2.6.4 requires an additional buffer capacitor and power transistor. To remove these additional components, there have been research efforts to control the operation of one or more of the inherent power transistors of the SC converters in both switching phases [57, 70, 88-93]. When connected in the charging path from the input, these regulated transistors can be used to re-shape the input current to reduce the conducted EMI noise generated to the input supply rail as well as to reduce the current stress on the switches [92, 93].

(a)

(b)

Figure 2.19 (a) A SC voltage doubler with current control scheme [92, 93]; (b)

Current waveforms.

A SC converter with current control scheme (CCS) is shown in Figure 2.19. Using the CCS control scheme, one of the power switches during the input charging phase is driven into the saturation region and functions as a current source that is controlled by a negative feedback controller. As shown in Figure 2.19, during phase one, the switch QS_1 (quasi-switch) functions as a constant current source that charges C_{fly1} linearly. At the same time, C_{fly2} discharges through the switch S_2 with finite on-resistance. During phase two, QS_2 act as the controlled current source to charge C_{fly2} , while C_{fly1} discharges. Theoretically, the constant input current waveform as shown in Figure 2.19(b) can be achieved. The output voltage is regulated by increasing the current through QS_1 and QS_2 when $V_{out} < \frac{1}{\beta} V_{ref}$, and decreasing the current when $V_{out} > \frac{1}{\beta} V_{ref}$. However, since the regulated transistors are not connected to the output, the controlled amount of charge that is stored in the flying capacitor during the charging phase can only be transferred to the output after half switching cycle when the output charge transfer phase begins. Moreover, the bandwidth of the negative feedback loop and the transient response are limited by the converter switching frequency. In order to improve the transient response, higher switching frequency must be used, which however leads to increased switching loss and degraded overall power efficiency.

To achieve in-phase output voltage regulation, the regulated transistors can be incorporated into the output charge transfer path, such designs are named switching low-dropout regulators [57, 70, 88-91]. Figure 2.20 shows a SC voltage doubler ($M_{VCR,NL} = 2$) using the switching LDO architecture for in-phase output voltage regulation. The error amplifier senses the difference between the scaled output voltage and the reference voltage. The error signal controls the V_{gs} of the power

transistors M_{r1} and M_{r2} during phase one ($\Phi_1 = 1$) and phase two ($\Phi_2 = 1$), respectively. Alternatively, a pseudo-continuous control (PCC) scheme is reported in [91], as shown in Figure 2.21, which controls M_{r3} and M_{r4} in phase one and phase two, respectively. With switching LDO or PCC architecture, the current flowing to the output during both phases is controlled continuously, hence the output voltage ripple can be suppressed on the condition that sufficient loop gain and bandwidth are achieved. Nonetheless, the switching nature of the converter inevitably generates switching noise (glitches) at the output voltage during phase transitions.

Figure 2.20 A SC voltage doubler with switching LDO architecture.

Figure 2.21 A SC voltage doubler with pseudo-continuous control [91].

2.7 Output Voltage Ripple Analysis and Reduction Techniques

The output voltage ripple of switched-capacitor DC-DC converters affects the performance of the load circuit, and must be minimized if the converter is used to power noise sensitive loads such as data converters, audio amplifiers and RF applications.

The output voltage ripple of SC DC-DC converters is due to the pulse like charging and/or discharging currents of the flying capacitors that flow to the output [49, 90, 94, 95]. Consider the 1/2-SC converter in Figure 2.22(a). Assume the load capacitance is sufficiently large so that the output voltage ripple is much smaller than the ripple across the flying capacitors and V_{out} can be assumed constant when analyzing the current delivery to the output. For simplicity, assume all power

switches have the same on-resistance R_{on} . As illustrated in Figure 2.22(b), the charging and discharging currents of the flying capacitor are high at the beginning of each phase due to small switch on-resistance. The currents decay exponentially with the time constant of $\tau = 2R_{on}C_{fly}$. The current flow to the output in both phases is given by

$$I_{sc}(t) = \frac{\Delta V}{2R_{on}} e^{-t/\tau} \quad (2.78)$$

where ΔV is the voltage across the power switches at the beginning of each phase, which is given by

$$\Delta V = V_{IN} - V_{Cfly,L} - V_{out} = V_{Cfly,H} - V_{out} \quad (2.79)$$

where $V_{Cfly,H}$ and $V_{Cfly,L}$ are obtained from equation (2.15) and equation (2.16).

As shown in Figure 2.22, the difference between the instantaneous charging/discharging current I_{sc} and the current drawn by the load circuit I_L causes an amount of charge Q_{out} being injected in the output capacitor in each switching phase, which causes the output voltage ripple of

$$\Delta V_{rpp} = \frac{Q_{out}}{C_{out}} \quad (2.80)$$

Q_{out} is given by

$$Q_{out} = \int_0^{t_1} [I_{sc}(t) - I_L] dt = \int_{t_1}^{0.5T_{sw}} [I_L - I_{sc}(t)] dt \quad (2.81)$$

where t_1 is the time when the charging/discharging current is equal to the load current, and is obtained from

$$I_{sc}(t_1) = \frac{\Delta V}{2R_{on}} e^{-t_1/\tau} = I_L \quad (2.82)$$

When the converter operates in the slow switching limit, the current delivery to the output can be approximated as an impulse (i.e. $t_1 \ll 0.5T_{sw}$). The output voltage ripple is given by

$$\Delta V_{rpp} = \frac{I_{out}}{2f_{sw}C_{out}} \quad (2.83)$$

Since the output current is proportional to the switching frequency in the SSL, the output voltage ripple remains relatively constant. Although larger output capacitor C_{out} can be used to reduce the output voltage ripple, this increases the die area or PCB footprint.

On the other hand, when the SC converter is designed to operate in the fast switching limit, the switching period becomes sufficiently small, compared to the charging/discharging time constant, such that the charging/discharging current is approximately constant and equals to the load current at all times. Theoretically, there's no charge injected in or extracted out of the output capacitor. As a result, the output voltage ripple disappears. However, as discussed in Section 2.5, for optimal conversion efficiency, a SC DC-DC converter must operate at the corner frequency between the SSL and the FSL. Hence the output voltage ripple must be suppressed through circuit techniques such as the post-regulation method presented in Section 2.6.4 or the in-phase regulation methods presented in Section 2.6.5.

(a)

(b)

Figure 2.22 Pulsive charging and discharging current and output voltage ripple.

2.7.1 Multiphase Interleaving

Multiphase interleaving is another attractive solution to mitigate the output voltage ripple of integrated SC DC-DC converters [34, 41, 43, 49, 69, 96-99]. It is implemented by fragmenting a single SC converter into multiple smaller ones and switch them with different phase shifted clocks. To avoid confusion, the SC

converters with interleaving technique are referred to as "multiphase-interleaved SC converters", while a "multi-phase SC converter" refers to a converter that has multiple circuit configurations within a switching cycle. For example, the converters of Fig 2.1 are two-phase converters since there are two converter configurations in every switching cycle associated with the charging phase and the discharging phase, respectively. Similarly the converter shown in Fig 2.3 is a three-phase converter since it has three different circuit configurations within a switching cycle. On the other hand, a N-phase interleaved SC converter consists of N identical SC converter cells that are switched with different phase shifted clocks. Each converter cell can have multiple configurations within a switching cycle.

By using multiphase interleaving, a single large SC DC-DC converter is fragmented into N smaller identical converter cells with the same circuit topology and the size of each flying capacitor and power switch is linearly scaled down by N times. The clock of each converter cell is shifted by an phase angle of $360^\circ/N$. The total amount of charge Q_{tot} delivered to the output in each switching cycle is the same as that of the converter without interleaving, but is equally divided among the N converter cells. Hence each converter cell delivers an amount of charge, Q_{tot}/N , to the output in every switching period. Since the charge transfer to the output occurs every T_{sw}/N seconds, the resulting output voltage ripple when the converter operates in SSL is given by

$$\Delta V_{rpp,NPhase} = \frac{I_{out}T_{sw}}{NC_{out}} = \frac{I_{out}}{Nf_{sw}C_{out}} \quad (2.84)$$

When the operation of the SC converter approaches the fast switching limit, the output voltage ripple is further reduced.

(a)

(b)

Figure 2.23 A four-phase interleaved 1/2-switched-capacitor DC-DC converter.

Besides the reduction of output voltage ripple, multiphase interleaving introduces additional benefit in reducing the size requirement of the output capacitor. Since only one SC converter cell is switched at a time, the flying capacitors of the other $N-1$ converter cells act as the output capacitor that helps to reduce the output voltage ripple. When sufficient numbers of interleaved converter cells are used, a dedicated output capacitor may be eliminated. Therefore, multiphase interleaving greatly increases the power density of the SC converter and makes it more feasible for monolithic integration. Figure 2.23 shows a four-phase interleaved 1/2-SC DC-DC converter. The phase shifted clocks can be generated as shown in Figure 2.24. Note that the first phase is the inverse of the third phase (i.e. $\overline{\Phi_1} = \Phi_3$), and the second phase is the inverse of the fourth phase (i.e. $\overline{\Phi_2} = \Phi_4$). Since each converter cell delivers the same amount of charge to the output during both switching phases of a switching cycle, the output voltage ripple of the 4-phase interleaved converter is half of that of a converter without interleaving. The peak input current ripple of the 4-phase converter is reduced to 1/4 of its single phase counterpart, since the input charges the flying capacitor only once in each switching cycle.

Figure 2.24 A four -phase clock generator.

Chapter 3 A HYSTERETIC SWITCHED-CAPACITOR DC-DC CONVERTER WITH OPTIMAL OUTPUT RIPPLE AND FAST TRANSIENT RESPONSE

Chapter 1 discussed the increasing demand for system-on-chips (SoCs) and the need to generate multiple independent supply rails to support the SoCs efficiently. Switched-capacitor (SC) DC-DC converters typically offer higher power efficiency than linear regulators and are easier to be integrated than SI DC-DC converters. Therefore, SC DC-DC converters are promising solutions to support the multiple voltage rails of SoCs without increasing the number of external components and supply pins [38, 49].

This Chapter investigates the output voltage ripple of a switched-capacitor DC-DC converter using the traditional single boundary hysteretic control (as discussed in Section 2.6.1.2); hence a sampling frequency modulation scheme is proposed which optimizes the output voltage ripple of a dynamic comparator based hysteretic SC DC-DC converter.

3.1 Introduction

Many of the SC converters in the literature are regulated by adjusting the switching frequency using hysteretic control methods (also referred to as bang-bang control) with one or more control boundaries[34, 41, 65, 66, 69, 75, 76]. Due to their inherent stability and fast transient response, the hysteretic control methods are often preferred over the traditional linear pulse-frequency modulation (PFM), which uses an error amplifier and a voltage controlled oscillator (VCO) to control the

switching frequency[73, 74]. A double-boundary hysteretic control is typically used when the output buffer capacitor is much larger than the charge transferring capacitors of the SC power stage [76].

(a)

(b)

Figure 3.1 (a) Double boundary control with large output capacitor [76]; (b) Lower boundary control with small output capacitor [34].

As shown in Figure 3.1(a), the converter clock is enabled when the output voltage falls below the lower control boundary. With large output capacitor, the converter needs multiple switching cycles to raise the output voltage above its higher control boundary, after which the converter clock is disabled, and the load current

discharges the output capacitor. In [34], a single (lower) boundary hysteretic control method is presented, which uses output capacitance on the same order of magnitude as the charge transferring capacitance. As shown in Figure 3.1(b), the control circuit triggers a phase transition of the SC converter to cause a packet of charge to be transferred to the output each time the sampled output voltage falls below the control boundary. With small output capacitance, the output voltage ripple due to a single phase transition is large enough to be used by the controller. When the output voltage is above the control boundary, the controller keeps the converter phase, and the load current discharges the output capacitor. The small output capacitance, however, raises concern about the output voltage droop during step-up load transients. Moreover, a conventional lower boundary hysteretic controller is typically clocked at fixed sampling frequency, while the converter switching frequency varies with load current. Since the converter is switched only at the sampling edge when the dynamic comparator detects that the output voltage is lower than the control boundary, the resulting switching frequency is non-uniform, which increases the output voltage ripple. Although the dynamic comparator can be clocked at high speed to avoid these issues [39, 75], this imposes more stringent requirements on the comparator design and increases the control power, degrading the overall conversion efficiency at low loads. Moreover, when the sampling period becomes smaller than the propagation delay in the hysteretic loop, sub-harmonic oscillation occurs which increases the output voltage ripple significantly [41].

In this Chapter, a modified hysteretic control technique is proposed, which locks the sampling frequency at an integer multiple of the converter switching frequency under all load conditions in steady state. As a result, optimal output voltage ripple is achieved and the comparator speed scales with the load current. Section 3.2

discusses the output ripple performance using lower boundary hysteretic regulation and shows that optimal output voltage ripple can be achieved by matching the sampling clock with the converter switching frequency. The architecture and implementation of the proposed control scheme are illustrated in Section 3.3. Section 3.4 presents the measurement results.

3.2 Single Boundary Hysteretic SC DC-DC Converters

The output voltage ripple of a 1/2 switched-capacitor DC-DC converter using the traditional single boundary hysteretic control is discussed in this Section.

3.2.1 A 1/2 Switched-Capacitor Power Stage

A two-phase switched-capacitor DC-DC converter with no-load voltage conversion ratio ($M_{VCR,NL}$) of 1/2 is shown in Figure 3.2. It consists of a charge transfer capacitor C_{fly} (also called flying capacitor) and four switches S_1 - S_4 . In this design, the output capacitance C_{out} is on the same order of magnitude as C_{fly} , therefore, the output voltage ripple must be taken into account in the current delivery analysis and the effect of C_{fly} on the output voltage ripple must be considered. During the charging phase, S_1 and S_3 are turned ON while S_2 and S_4 are turned OFF. The input delivers charge Q to both C_{fly} and the load. During the discharging phase, C_{fly} releases the same amount of charge to the load. In steady state

(a)

(b)

Figure 3.2 (a) A 1/2 step-down SC DC-DC converter; (b) Voltage ripple across C_{fly} and C_{out} assuming SSL operation.

$$Q = C_{fly} \Delta V_{cfly} \quad (3.1)$$

where ΔV_{cfly} is the voltage ripple across the flying capacitor. With converter switching at frequency of f_{sw} , the average current delivered to the output is given by

$$I_{out} = 2f_{sw} C_{fly} \Delta V_{cfly} \quad (3.2)$$

A SC DC-DC converter regulated via switching frequency operates in or near the slow switching limit (SSL), where the initial charge transfer to the output can be approximated as an impulse [52]. Assume the output voltage ripple is uniform over

time, as shown in Figure 3.2(b), at each switching instant, the output voltage steps from $V_{out,min}$ to $V_{out,max}$ due to the impulsive charge transfer. Meanwhile, the voltage across the flying capacitor is initially charged from $V_{cfly,L} = V_{out,min}$ to $V_{in} - V_{out,max}$ when the charging phase begins or discharged from $V_{cfly,H} = V_{in} - V_{out,min}$ to $V_{out,max}$ when the discharging phase begins. During both switching phases, the output voltage drops linearly from $V_{out,max}$ to $V_{out,min}$ due to the load current continuously draining the output capacitor. The output voltage ripple is given by

$$\Delta V_{out} = V_{out,max} - V_{out,min} = \frac{I_{out}}{2f_{sw}(C_{fly} + C_{out})} \quad (3.3)$$

The voltage across the flying capacitor is charged to $V_{in} - V_{out,min}$ at the end of the charging phase and discharged to $V_{out,min}$ at the end of the discharging phase, hence

$$\Delta V_{cfly} = V_{in} - 2V_{out,min} \quad (3.4)$$

Therefore, the output current is given by

$$I_{out} = 2f_{sw} C_{fly} (V_{in} - 2V_{out,min}) \quad (3.5)$$

3.2.2 Single Boundary Hysteretic Regulation

The architecture of a single boundary hysteretic control method, as shown in Figure 3.3, has been discussed in Section 2.6.1 [34]. Whenever the sampled output voltage falls below the reference voltage, the controller changes the phase of the converter, causing an amount of charge $Q = C_{fly}(V_{in} - 2V_{out,min})$ to be delivered to the output. The power stage reacts immediately after the propagation delay in the control loop whenever the comparator detects that the output voltage is below V_{ref} . Hence the transient response is mainly limited by the output voltage detection frequency. A fast comparator clock can be used to improve the transient response.

Figure 3.3 A Single boundary hysteretic control architecture [34].

However, to ensure the control loop stability, the maximum sampling frequency should be limited such that the propagation delay does not exceed the sampling clock period.

3.2.3 Output Voltage Analysis

The output voltage ripple of the 1/2 switched-capacitor DC-DC converter that is regulated using the single boundary hysteretic control method is examined here.

First, we assume that the converter operates with uniform switching frequency, as shown in Figure 3.4(a). Since the converter operates in the SSL and delivers the same amount of charge to the output once every half switching period, the peak-to-peak output voltage ripple is given by equation (3.3). However, since a conventional hysteretic controller uses a fixed sampling frequency, and the converter changes phase only when $V_{out} < V_{ref}$ is detected at the rising edge of the sampling clock.

(a)

(b)

Figure 3.4 (a) Optimal output ripple with uniform switching frequency when $T_d < T_{sample}$; (b) Simulated output voltage ripple vs sampling frequency.

The converter's instantaneous phase changing frequency f_{ph_change} can be expressed as

$$f_{ph_change} = f_{sample}/K \quad (3.6)$$

where K is an integer. Note that $f_{ph_change} = 2f_{sw}$ since there are two phase changes

within each converter switching period. On the other hand, the converter's average switching frequency is determined by the load current, and the size of the flying capacitor. Therefore, the switching frequency would not be uniform unless the sampling frequency of the hysteretic controller happens to be integer multiples of the converter's average phase changing frequency.

Figure 3.4(b) shows the simulated output voltage ripple of a 1/2 SC converter as a function of the sampling frequency when it delivers 1 mA output current with $V_{in} = 1.8$ V, $V_{ref} = 0.8$ V, using 1.5 nF flying capacitance and 2 nF output capacitance. The minimum output voltage ripple is obtained when the sampling frequencies are $2K$ times the average converter switching frequency. The non-optimal output ripple at other sampling frequencies is due to the mismatch between the sampling frequency and the converter switching frequency. Although the output voltage ripple approaches the optimal value when the dynamic comparator is clocked at a high sampling frequency, this increases the control power, hence reduces the overall efficiency especially when the converter is delivering low load power. Moreover, if the sampling period becomes smaller than the propagation delay in the control loop, sub-harmonic oscillation will happen which increases the output voltage ripple significantly. A general analysis of the output voltage ripple under these two cases is presented as follows.

1) Sampling frequency mismatches converter switching frequency

Since the output voltage is compared to the reference voltage once every sampling period, the effective frequency of the converter's phase change can be expressed as

$$f_{ph_change} = \frac{N}{M} f_{sample} \quad (3.7)$$

(a)

(b)

Figure 3.5 (a) Non-optimal output ripple when $T_d < T_{sample}$; (b) Non-optimal output ripple due to multiple enabling pulses when $T_d > T_{sample}$.

Equivalently,

$$NT_{ph_change} = MT_{sample} \quad (3.8)$$

i.e., the SC converter changes phase N times in every M sampling periods. Here N

and M are integers, and $N \leq M$ since the frequency of phase change cannot exceed the sampling frequency. Hence the remaining $M - N$ sampling clock pulses are skipped. If the propagation delay T_d in the control loop is smaller than one sampling period, as shown in Figure 3.5(a), then whenever the output voltage is detected to be lower than the reference voltage, the SC converter responds before the sampling edge of the subsequent clock pulse. The $M - N$ skipped pulses are distributed in between the N phase changing events. Uniform distribution of the phase changing events happens only when M equals integer multiple of N , which results in one phase change per M/N sampling periods. As shown in Figure 3.4(a), this results in uniform and optimal output voltage ripple of

$$\Delta V_{out,opt} = \frac{\frac{M}{N} T_{sample} I_{out}}{C_{fly} + C_{out}} = \frac{I_{out}}{f_{ph_change} (C_{fly} + C_{out})} \quad (3.9)$$

which is identical to (3.3) since $f_{ph_change} = 2f_{sw}$. On the other hand, when M does not equal to integer multiple of N , the $M - N$ skipped sampling pulses cannot be uniformly distributed. The number of skipped pulses between two adjacent phase changes takes either of the following two values:

$$N_{skip,1} = \frac{(M-N) - remainder(M,N)}{N} \quad (3.10)$$

and

$$N_{skip,2} = \frac{M - remainder(M,N)}{N} \quad (3.11)$$

where $remainder(M, N)$ is the remainder of M/N . The load current discharges the output capacitor during the period when no phase transition occurs, resulting in peak-to-peak output voltage ripple of

$$\Delta V_{out} \geq \frac{(N_{skip,z}+1)T_{sample}I_{out}}{C_{fly}+C_{out}} = \left(1 + \frac{N-\text{remainder}(M,N)}{N}\right) \frac{I_{out}}{f_{ph_change}(C_{fly}+C_{out})} \quad (3.12)$$

which is larger than the optimal output voltage ripple when switching frequency is uniform.

2) Sub-harmonic oscillation

Another scenario of non-uniform switching frequency is when the propagation delay T_d in the control loop is larger than the sampling period T_{sample} . This happens when high sampling frequency is used in order to achieve fast transient response. However, increasing the sampling frequency to the extent such that the sampling period becomes smaller than the delay in the regulating loop can cause significant oscillation of V_{out} around V_{ref} and large peak-to-peak output ripple. As depicted in Figure 3.5(b), when the comparator detects that the output voltage is below the reference at the rising edge of the sampling clock, an enabling pulse is generated which is expected to trigger a phase change in the power stage to bring the output voltage up immediately. However, due to the propagation delay in the control loop, the phase transition does not occur before the next sampling clock edge. The load current further drains the output capacitor, causing the output voltage to be even lower at the second sampling edge. Therefore, another phase transition enabling pulse is generated to produce stronger reverse action against the V_{out} drop. These consecutive enabling pulses cause intensive charge transfer to the output and increase the output voltage ripple significantly. In steady state, the output voltage contains significant frequency component in the sub-harmonics of the switching frequency. Hence this phenomenon is called sub-harmonic oscillation.

3.3 Proposed Hysteretic Regulation

To achieve the optimal output voltage ripple, a modified hysteretic regulation method is proposed. Instead of using a fixed sampling frequency, the proposed method locks the sampling frequency at an integer multiple of the converter's switching frequency for all varying load currents.

3.3.1 System Architecture

The architecture of the proposed system is illustrated in Figure 3.6. The hysteretic controller of the SC DC-DC converter comprises two feedback loops. The first loop performs the standard hysteretic output voltage regulation as discussed earlier in Section 2.6.1 and Section 3.2.2, whereas the second loop ensures a uniform converter switching frequency by adjusting the sampling frequency. The sampling frequency control loop monitors the time between adjacent phase changes by counting the number of skipped sampling pulses N_{skip} . The phase transitions, hence charge transfers, are distributed uniformly when N_{skip} remains constant over time. When N_{skip} is too large/small, the controller reduces/increases the sampling frequency by adjusting the control voltage of the voltage controlled oscillator (VCO) through a charge pump integrator. In this design N_{skip} is regulated at a value of six. This allows the converter switching frequency to be increased by up to six times without delay, hence the converter responds to any step-up load transient that is within six times the initial load current immediately by skipping less sampling pulses. During large load transients, N_{skip} becomes zero, the slow SC integrator control path is bypassed and the control voltage of the VCO is set to the maximum immediately to prevent significant output voltage droop.

Figure 3.6 System architecture of the proposed single boundary hysteretic DC-DC converter with sampling frequency control.

3.3.2 Power Stage

The 1/2 step-down switched-capacitor power stage is composed of two identical SC sub-modules operating in opposite phases, as shown in Figure 3.7(a). The switches $S_{1,1}$, $S_{1,3}$, $S_{2,1}$, and $S_{2,3}$ are implemented as p-type MOSFETs whereas $S_{1,2}$, $S_{1,4}$, $S_{2,2}$, and $S_{2,4}$ are implemented as n-type MOSFETs. The flying capacitors $C_{fly,1}$ and $C_{fly,2}$ are implemented as Metal-Insulator-Metal (MIM) capacitors for low bottom plate parasitic capacitance. Each flying capacitor has a size of 0.75 nF.

The anti-phase operation of the SC converter makes every switching event essentially the same, which includes one SC sub-module switching from the charging phase to the discharging phase and the other sub-module switching from the discharging phase to the charging phase. Hence the charge transfer to the output

becomes uniform if the two sub-modules are matched well and the phase transitions are distributed evenly over time.

Figure 3.7 (a) Anti-phase 1/2 step-down switched-capacitor DC-DC converter; (b) Non-overlap gate signals with reduced voltage swing.

Figure 3.8 (a) Anti-phase 1/2 step-down switched-capacitor DC-DC converter; (b) Non-overlap gate signals with reduced voltage swing.

To reduce the gate driving loss, the gate voltages of the low side transistors $S_{1,2}$, $S_{1,3}$, $S_{2,2}$, and $S_{2,3}$ swing from GND to V_{out} and the gate voltages of the high side transistors $S_{1,1}$, $S_{1,4}$, $S_{2,1}$, and $S_{2,4}$ swing from V_{out} to V_{in} . A capacitor-coupled level shifter can be used to generate the high side gate signals by adding the voltages across the level shifting capacitors C_{ls1} - C_{ls4} to the low side gate signals [34, 49, 100, 101]. To prevent shoot through current in the power stage, a dead-time is necessary when a SC sub-module switches from the charging phase to the discharging phase

and vice versa [34, 49, 89, 100]. Figure 7(b) shows the non-overlap gate signals with reduced voltage swing. The gate signal generation circuit including the dead-time generators, level shifters, gate drivers and a start-up circuit are shown in Figure 3.8(a). Here the gate drivers of the low side switches are inserted in the delay loop of the dead-time generator so that the delay mismatches of the drivers will not diminish the dead-time [49, 89]. The startup circuit is critical to ensure safe operation during the converter power-up phase. When the input voltage ramps up during the start-up phase, the output voltage is clamped to two diode voltages (approximately equal to V_{out} after start-up) below the input voltage. Meanwhile the power stage is forced to a known stage such that $C_{fly,1}$ is pre-charged to V_{out} and $C_{fly,2}$ is pre-charged to $V_{in} - V_{out}$. The level shifting capacitors C_{ls1} - C_{ls4} are also pre-charged to the appropriate voltages, so that the converter transitions from the start-up phase to the regulation phase smoothly, when V_{out} reaches 0.8 V. M_{DN} is added to help pull vp up and turn off the startup transistors M_X and M_Y immediately after vn goes low. This ensures that both the upper and lower voltage domains of the gate drivers are released from the start-up state simultaneously. Otherwise, the converter can be in an undefined state during the transition phase. Figure 3.8(b) shows the start-up waveforms.

3.3.3 Hysteretic Regulation with Sampling Frequency Modulation

The hysteretic controller uses a dynamic comparator [41] to compare the output voltage V_{out} with a reference voltage V_{ref} . As shown in Figure 3.9, the comparator has two complementary outputs, namely CMP and $CMPN$. When V_{out} becomes smaller than V_{ref} , a pulse is generated at the CMP terminal as shown in Figure 3.10, which triggers a phase change in the power stage. On the other hand, when V_{out} is

greater than V_{ref} , the comparator generates a pulse at the *CMPN* terminal while the voltage at *CMP* terminal remains low.

Figure 3.9 A dynamic comparator [41].

(b)

Figure 3.10 Output voltage detection operating waveform.

The number of pulses (N_{skip}) at the *CMPN* terminal between two *CMP* pulses indicates the time between two phase transitions. Hence uniform charge transfer to the output is achieved by regulating N_{skip} at a constant value. The value of N_{skip} is obtained from a 3-bit counter, as shown in Figure 3.9. The counter output is

initialized to 000 at the falling edge of each CMP pulse (i.e. after each phase transition is triggered) and starts to count the number of $CMPN$ pulses until the next phase transition is triggered by the next CMP pulse. When the output reaches the maximum value 111, the counter holds this value instead of returning back to 000 state. The counter output is read at the rising edge of the new CMP pulse and is stored as a three bit signal $B_3B_2B_1$ (the binary form of N_{skip}). N_{skip} is compared to a reference value N_{ref} , which is set to six in this design. When $N_{skip} > N_{ref}$, a one-shot decrement command is sent to decrease the output voltage of a charge pump integrator, which reduces the frequency of the sampling clock generated by the VCO, as shown in Figure 3.11. When $N_{skip} < N_{ref}$, the sampling frequency is increased.

Figure 3.11 Sampling frequency control through a charge pump integrator.

The sampling frequency control loop can be modeled as a phase locked loop, where the phase of the switching frequency is the reference signal, as shown in Fig. 3.12. In steady state, N_{skip} sampling pulses are skipped between two adjacent switching activities (i.e. during half-switching cycle), hence the phase of the sampling frequency is divided by $2(N_{skip} + 1)$, and compared to the phase of the switching

frequency. When the phase difference is larger than $\Delta\Phi_{\min} = \frac{\pi}{N_{\text{skip}}+1}$, skipped or redundant sampling pulses will be detected and the control voltage of the VCO will be adjusted. When the phase difference is less than $\Delta\Phi_{\min}$, N_{skip} sampling clock pulses are skipped during half switching cycle. As a result, the sampling frequency remains unchanged. When the one-shot increment/decrement pulse is enabled, the average output current of the CP integrator is given by

$$I_{\text{avg}} = I_{\text{CP}} t_{\text{CP}} f_{\text{sw}} \quad (3.13)$$

Therefore, the maximum gain from $\Delta\Phi$ to I in Figure 3.12 is given by

$$\frac{I_{\text{avg}}}{\Delta\Phi_{\min}} = \frac{(N_{\text{skip}}+1)I_{\text{CP}}t_{\text{CP}}f_{\text{sw}}}{\pi}. \text{ Since } f_{\text{sw}} = \frac{f_{\text{sample}}}{2(N_{\text{skip}}+1)} \text{ when the PLL is in lock, } \frac{I_{\text{avg}}}{\Delta\Phi_{\min}} =$$

$\frac{I_{\text{CP}}t_{\text{CP}}f_{\text{sample}}}{2\pi}$. The PLL consisting of two integrators, namely the CP-integrator and the VCO, can be compensated by introducing a zero at the output of the charge pump integrator.

Figure 3.12 PLL model of the sampling frequency control loop.

The current starved ring oscillator based VCO that is used to generate the sampling frequency is shown in Figure 3.13(a). V_{in} is used as the supply for the charge-pump

and the voltage-to-current (V-to-I) stage of the VCO to increase the output frequency tuning range. The voltage across the resistor R_{VCO} of the V-to-I is obtained by subtracting a V_{th} from the control voltage to ensure that the pull down current source of the charge-pump integrator does not go into the triode region at low frequencies. The VCO can be modeled as

$$\Phi_{sample}(s) = \frac{2\pi K_{VCO}}{s} v_{control} \quad (3.14)$$

Where K_{VCO} is given by $K_{VCO} = \frac{\partial f_{sample}}{\partial V_{Control}}$ in Hz/V. The overall loop transfer function of the PLL can be expressed as:

$$L(s) = \frac{I_{CP} t_{CP} f_{sample} K_{VCO} (1 + s R_z C_z)}{2(N_{skip} + 1) s^2 (C_z + C_p) (1 + s R_z (C_z / C_p))} \quad (3.15)$$

To ensure the stability, $C_p \ll C_z$ so that the extra pole due to C_p is placed far to the right of the unity-gain frequency, which is given by

$$\omega_u \approx \frac{I_{CP} t_{CP} f_{sample} K_{VCO} R_z}{2(N_{skip} + 1)} \quad (3.16)$$

The bandwidth is proportional to the product of f_{sample} and K_{VCO} . Here, the worst case stability happens at the lowest sampling frequency. By choosing $I_{CP} = 1 \mu A$, $t_{CP} = 10$ ns, $R_z = 670$ kOhm, and $C_z = 10$ pF, the zero is less than half the bandwidth for sampling frequencies larger than 3.6 MHz (control voltage > 0.3 V), which ensures more than 53 degree phase margin, as shown in Figure 3.14.

(a)

(b)

 Figure 3.13 (a) The voltage-controlled oscillator; (b) f_{sample} , K_{vco} and ratio =

ω_u/ω_{sw} vs VCO control voltage.

The bandwidth of the sampling frequency control loop must be sufficiently lower than the switching frequency so that it does not disturb the main hysteretic control loop. The ratio between the bandwidth and the switching frequency is given by

$$\frac{\omega_u}{\omega_{sw}} = \frac{\omega_u}{2\pi f_{sw}} = \frac{1}{2\pi} I_{CP} t_{CP} K_{vco} R_Z \quad (3.17)$$

Figure 3.14 Bode plots of the PLL model of the sampling frequency control loop model.

Figure 13(b) plots f_{sample} , K_{vco} and ω_u/ω_{sw} versus the control voltage across the entire tuning range of the sampling frequency. The bandwidth is kept lower than $1/5^{\text{th}}$ the switching frequency. A slow sampling frequency control loop means the output voltage ripple takes longer to reach the optimal value. This is tolerable as long as the output voltage remains regulated.

3.3.4 Transient Response Enhancement

By skipping N_{skip} , (which is set to six in this design) pulses between adjacent phase changes, the sampling frequency is given by $f_{sample} = (N_{skip} + 1)f_{ph_change}$. Theoretically, this allows the converter switching frequency to be increased by up to N_{skip} times when the load current increases. Hence it is able to respond instantly to a load current increase without output voltage droops if the load step is not larger

than N_{skip} times the initial load current. As illustrated in Figure 3.15(a), the step up load transient causes N_{skip} to become less than six initially, as a result, the control voltage of the VCO is increased slowly through the charge pump integrator, until N_{skip} becomes six. A larger load current step causes zero sampling pulses being skipped between adjacent phase transitions, as illustrated in Figure 3.15(b). Therefore, when $N_{skip} = 0$, a large step-up load transient is detected. The control voltage is set to the maximum value, bypassing the charge pump integrator. As a result, the sampling frequency jumps to its maximum value (~ 180 MHz) and the converter switching frequency can be increased to the required value quickly, preventing large output voltage undershoots. After that, the sampling frequency is reduced slowly until N_{skip} settles to its reference value. The choice of N_{skip} is a compromise between the transient response and the sampling frequency. Depending on the expected load steps, N_{skip} and the sampling frequency can be increased to speed up the load transient responses. On the other hand the maximum sampling frequency should be limited to prevent the sub-harmonic oscillation at high loads. Since the sampling frequency is set to the maximum when two consecutive *CMP* pulses are detected, the worst-case load transient response time is equal to one sampling period. On the other hand, the response to a step-down load transient of any step size is inherently instant since the switching frequency can be reduced immediately by automatically skipping more sampling pulses. Adjusting the sampling frequency slowly during small load transients ensures stability of the sampling frequency regulation loop, while bypassing the slow loop helps to speed up the output recovery during large load transients.

(a)

(b)

Figure 3.15 Sampling frequency control operating waveforms during (a) small load transients; (b) large load transients.

3.4 Measurement Results

The 1/2 switched-capacitor DC-DC converter with the proposed hysteretic regulation was implemented in 0.18 μ m CMOS technology with active area of 0.75 $\times$ 0.66 mm², as shown in Figure 3.16. The converter uses a total amount of 1.5 nF on-chip charge transferring capacitance implemented as dual-MIM capacitors. The

DC-DC converter provides a regulated output voltage of 0.8 V from a 1.8 V input supply. Table 3.1 summarizes the performance of the proposed converter.

The SC converter uses 2 nF off-chip output capacitance for testing purpose. The output reference voltage V_{ref} is set at 800 mV. Figure 3.17(a) shows the measured steady state operation of the SC converter when it is delivering a load current of 1 mA. The converter maintains a uniform switching frequency of 1.5 MHz is by skipping six sampling pulses (*CMPN* pulses) between adjacent phase transitions (triggered by *CMP* pulses). The output voltage ripple of 25 mV is observed. Figure 3.17(b) shows the waveforms at maximum 7 mA load current. The switching frequency is 10 MHz and the output voltage ripple is 10 mV.

Figure 3.16 Die microphotograph.

TABLE 3.1 PERFORMANCE SUMMARY OF THE MEASUREMENT RESULTS

Technology	0.18 μ m CMOS
No-load conversion ratio	1/2
Total flying capacitance	1.5 nF dual-MIM (on-chip)
Output capacitance	2 nF (off-chip)
V_{in}	1.8 V (measured)
	1.8 – 3.3 V (theoretical)
V_{out}	0.8 V (regulated)
	0.8 – 1.5 V (theoretical)
I_{out}	0.12 – 7 mA
f_{sw}	260 kHz - 10 MHz
Output voltage ripple	48 mV - 10 mV
Worst-case response time	1/ f_{sample}
V_{out} undershoot	50 mV
Max P_{out}	5.6 mW
Efficiency	68% - 86.4%
Peak efficiency	86.4% @ $I_{out} = 2$ mA
Control power	28 μ W
Active chip area	0.495 mm ²

The transient response of the DC-DC converter under different load conditions is tested. Figure 3.18 shows the transient response when the output current changes from 0.2 mA to 1 mA. The converter switching frequency is immediately increased by skipping less sampling clock pulses, resulting in zero output voltage droop. After that, the sampling frequency is increased gradually until N_{skip} recovers to 6.

(a)

(b)

Figure 3.17 Measured steady state operation with (a) $V_{ref} = 800$ mV and $I_{out} = 1$ mA;

(b) $V_{ref} = 800$ mV and $I_{out} = 7$ mA.

Figure 3.18 Measured step-up transient response when I_{out} changes from 0.2 mA to 1 mA.

Figure 3.19(a) demonstrates the transient response when I_{out} is increased from 0.2 mA to 2 mA. The transient step causes N_{kip} to drop to zero, hence the sampling frequency jumps to its maximum value to allow for sufficiently fast switching frequency to recover the output voltage quickly and prevent further output voltage droop. Figure 3.19(b) shows the response when the load current increases from 0.2 mA to the full load current of 7 mA. Since the slow sampling frequency control loop is bypassed, a small output voltage drop of 50 mV is observed and the output voltage recovers in less than 400 ns. The step-down load transient response is shown in Figure 3.20 when the output current drops from 1 mA to 0.2 mA. The switching frequency is reduced immediately by skipping more sampling pulses, therefore, no output voltage overshoot is observed. The sampling frequency is reduced gradually in order to maintain a constant N_{kip} of six. It is noted that the output voltage ripple is smaller at higher load currents. This is due to the converter

operation approaching the fast switching limit (FSL) as the switching frequency increases [52].

(a)

Figure 3.19 Measured step-up transient response when I_{out} changes from (a) 0.2 mA to 2 mA; (b) 0.2 mA to 7 mA.

Figure 3.20 Measured step-down transient response when I_{out} changes from 1 mA to 0.2 mA.

Figure 3.21 Steady state output voltage ripple and switching frequency vs load current.

The steady state output voltage ripple and switching frequency versus load current are shown in Figure 3.21. Figure 3.22 shows the breakdown of the power losses in

the proposed SC DC-DC converter under different load currents. The measured overall power conversion efficiency is shown in Figure 3.23. The converter achieves peak efficiency of 86.4% when $I_{out} = 2$ mA. The efficiency drops when I_{out} increases due to the rapid increase in switching loss. The control power and other losses do not scale with load current and dominate the overall power loss when load current is smaller than 0.3 mA.

Figure 3.22 Measured power loss components.

Figure 3.23 Measured overall power conversion efficiency.

TABLE 3.2 PERFORMANCE COMPARISON WITH PREVIOUS WORKS

Work	[57]	[33]	[102]	This Work
Technology	130 nm	45 nm	65 nm	0.18 μm
Regulation Method	Hysteretic	Digital Capacitance Modulation	Hysteretic	Hysteretic
Capacitor Type	Ferroelectric	Gate Oxide	MIM	MIM
Flying capacitance	8 nF	534 pF	0.675 nF	1.5 nF
f_{sw}	Up to 2 MHz	30 MHz	Up to 10 MHz	0.26 – 10 MHz
V_{out}	0.4 – 1.1 V	0.8 – 1 V	0.6 V, 0.8 V, 1 V	0.8 V (up to 1.5 V)
V_{in}	1.5 V	1.8 V	0.6 – 1.2 V	1.8 V (up to 3.3 V)
Conversion Ratios	1/1, 2/3, 1/2, 1/3	2/3	1, 4/3, 2/3	1/2
Max P_{out}	1.1 mW	8 mW	0.8 mW	5.6 mW
Efficiency	73% - 93%	48 - 69%	50 - 80%	68 - 86.4%
Control power	N.A.	40 μW	27 μW @ max P_{out}	28 μW
Active chip size (power stage)	** 0.2745 mm^2	0.16 mm^2	0.493 mm^2	0.495 mm^2
Output ripple	N.A.	50 mV	60 – 72 mV	10 – 48 mV
V_{out} drop	N.A.	100 mV (0.27 – 7.6 mA) Recover in 1.2 μs	50 mV (10 – 800 μA)	50 mV (0.2 – 7 mA) Recover in 400 ns
C_{out}	10 nF	0.7 nF	1.67 nF	2 nF

** Estimated from chip photo

Table 3.2 shows the performance comparison with some reported state-of-the-art designs using on-chip flying capacitors. For fair comparison, the selected works for comparison deliver similar amount of output power to the proposed design. The work in [57] achieves the highest peak efficiency by

using a special ferro-electric capacitor technology which allows for high capacitance density and very low bottom plate parasitic loss. Nonetheless, with the largest flying capacitance of 8 nF among the four designs, it delivers only 1.1 mW maximum output power. The design in [33] achieves higher output power by operating at much higher switching frequency than the other three designs; however, its power efficiency is traded off. The proposed design achieves better efficiency than [33] and [102] and comparable efficiency to [33]. It shows smallest steady state output voltage ripple, due to the use of the proposed sampling frequency control scheme. The output voltage undershoot and recovery time are smaller than those in [33] with similar load transient step size. [102] shows similar output voltage undershoot as the proposed design, however, the output voltage drop is not recovered due to the low sampling frequency.

3.5 Limitations and discussions

Although the conversion ratio of $\frac{1}{2}$ is used here to demonstrate the proposed ripple minimization technique, the technique can be extended to any other conversion ratios. The key is to ensure uniform charge transfers to the output. If a chosen topology does not transfer the same amount of charge to the output during the different switching phases, a symmetrical topology can be implemented by dividing the power stage into two identical units and operating them in opposite phases.

The maximum output current measured was 7 mA. This is because the test chip was designed for optimized efficiency at low power. Therefore, the power switches were not sized big enough to support higher load current, therefore the converter enters the fast switching limit early. If this converter were to support higher load current, the size of the power switches and the switching frequency can be increased.

Figure 3.24 Comparison of output voltage, output power and power conversion efficiency for different switch sizes and switching frequencies.

Figure 3.24 shows the comparison of the output power capability and the resulting efficiency for different power switch sizes and converter switching frequencies. It clearly shows that to optimize the efficiency at low load, small switch size and low switching frequency is desirable. But the efficiency drops fast as load current increases. On the other hand, larger switch size and higher switching frequency

allows for higher output power range, of course, the efficiency at low load is traded off.

Since the power stage is split into two voltage domains, each power transistor only blocks a fraction of the full input voltage. Hence the converter theoretically can support up to 3.6 V input voltage and 1.8 V output voltage, without using high voltage devices as the power transistors. Figure 3.25 shows the simulation results with input voltage of 3.3 V. To prevent device overstress issue, the output voltage must not be lower than 1.5 V. Hence, designing the converter at elevated input voltage needs addition care for circuit protection and reliability. This should be further explored in the future work.

3.6 Conclusion

A lower boundary hysteretic control technique with adaptive sampling frequency control is proposed for switched-capacitor DC-DC converters. The proposed technique is demonstrated on a 1/2 step-down SC DC-DC converter that was implemented in 0.18 μ m CMOS technology. By regulating the number of skipped sampling pulses (N_{skip}) between adjacent converter phase transitions at six in steady state, uniform output voltage ripple is achieved and the converter responses to step-up load transients that are within six times the initial load current immediately. When a larger load step occurs, the sampling frequency jumps to its maximum value within one sampling period to prevent significant output voltage drop. Step-down load transient does not cause output voltage overshoot since the switching frequency can be reduced to the required value immediately by skipping more sampling pulses. The proposed SC DC-DC converter achieves 86.4% peak power conversion efficiency and delivers a maximum output power of 5.6 mW.

Figure 3.25 Comparison of output voltage, output power and power conversion efficiency for different switch sizes and switching frequencies at $V_{in} = 3.3$ V.

Chapter 4 MULTIPHASE INTERLEAVED SWITCHED-CAPACITOR DC-DC CONVERTER

In this Chapter, a hysteretic control technique [41, 42, 59, 65, 66, 69, 75, 76] is proposed to regulate multiphase interleaved switched-capacitor DC-DC converters. As discussed in Section 2.7.1, multiphase interleaving is an effective and popular technique to reduce the output voltage ripple of switched-capacitor DC-DC converters [34, 41, 43, 49, 69, 96-99, 103]. This technique is especially useful for fully integrated SC converters, since the component count is no longer a serious concern and fragmenting capacitors does not introduce significant area or cost overhead. A multiphase SC converter can be regulated using the traditional pulse frequency modulation (PFM) method [73, 74], which uses an error amplifier to sense the difference between the output voltage and the reference voltage and controls the switching frequency through a voltage-controlled-oscillator (VCO), as discussed in Section 2.6.1. The PFM control loop requires frequency compensation and the transient response is limited since the unity-gain bandwidth is typically limited to less than one fifth of the converter switching frequency. On the other hand, a conventional hysteretic controller uses a separate control loop for each converter core of the multiphase interleaved converter. Hysteretic control method helps achieve fast transient response, but it uses N comparators or one shared comparator that operates at N times the single phase switching frequency of a N -phase interleaved converter. The proposed technique avoids these problems by using three control boundaries, each of which is defined by a separate comparator. The first comparator is used to compare the output voltage with a reference voltage,

the output of which changes the phase number (i.e. the number of converter cores to be switched in the next switching cycle) by a minimum step size of one to achieve tight regulation. The other two comparators enable the coarse operation mode for fast recovery whenever the output voltage crosses the higher or lower control boundaries.

4.1 Conventional Hysteretic Control for Multiphase SC Converters

The architecture of a conventional multiphase-interleaved switched-capacitor DC-DC converters with hysteretic control [34] is shown in Figure 4.1(a). The N-level interleaved converter is regulated by N identical control loops. Each loop comprises a comparator, a T-latch, a dead-time generator, a clock level shifter and a set of switch drivers to control the switching activity for the respective converter core. Interleaving is implemented by operating the comparators with phase shifted clocks so that different comparators sample and compare the output voltage with the reference voltage at different times. Hence the different converter cores will be switched at different times as well. The charge is delivered to the output at different times in packages that are N times smaller than that of a equivalent standard non-interleaved SC converter. Moreover, while one converter core delivers its charge to the output, the flying capacitors of the other converter cores act as the output buffer capacitor. As a result, the dedicated output capacitance C_L can be reduced or even removed, increasing the power density.

(a)

(b)

Figure 4.1 (a) Implementation of conventional multiphase hysteretic control with lower control boundary [34]; (b) Operating waveforms.

Figure 4.1(b) illustrates the operating waveforms for a 3-phase interleaved SC converter when the converter is operating at its maximum frequency (i.e. when each converter core change phase at every rising edge of its respective phase clock). As the clock Phase 1 goes high, the first comparator compares the output voltage V_{out} with its reference voltage V_{ref} . If $V_{out} < V_{ref}$, the first SC converter core will be switched in order to increase V_{out} . If $V_{out} > V_{ref}$, the first converter core would remain with the current configuration to avoid delivering excessive charges to the output. The same control sequence occurs to the rest of the converter cores when their associated clocks become high. As shown in Figure 4.1(b), within each switching period, $1/f_{sw,max}$, the output voltage is compared to the reference voltage $2N$ times, and is effectively being regulated at a frequency of $2N \times f_{sw,max}$. Meanwhile, each comparator operates at twice the maximum switching frequency of each converter core.

High level of interleaving reduces the output voltage ripple and saves the output capacitance, however, the use of separate control loop for each core results in control circuit complexity and area overhead that increases linearly with the level of interleaving [43]. The use of multiple comparators poses additional difficulties. Besides the increased area and power consumption, the multiple comparators are subjected to random offsets due to, for example, mismatches and PVT variations. Therefore, each comparator effectively define a reference level different from those of the other comparators. This limits the minimum achievable output voltage ripple of the converter. A solution to prevent the use of multiple comparators is to allow all converter cores to share a single comparator [41, 97, 104], as shown in Figure

4.2. However, this requires the comparator to operate at a frequency which is N times higher than that when multiple comparators are used.

Figure 4.2 (a) Alternative implementation of multiphase control using a single comparator [41]; (b) Operating waveforms.

4.2 Proposed Triple-Boundary Hysteretic Control for Multiphase SC DC-DC Converters

In this Chapter, a hysteretic regulation method with triple control boundaries is proposed that perform three comparisons within each switching cycle, while each comparator operates at twice the maximum switching frequency of each converter core. The proposed method prevents the need for N comparators or the need to operate a single comparator with N times faster speed.

4.2.1 System Architecture and Operating Principle

The architecture of the proposed multiphase interleaved SC converter with triple-boundary hysteretic control is shown in Figure 4.3.

Figure 4.3 Architecture of proposed multiphase SC converter with triple boundary hysteretic control.

The power stage comprises N identical SC converter cores. Three comparators compares the output voltage with the three control boundaries, namely V_{ref} , V_L and V_H . The comparison results are sent to an UP/DOWN counter, the output of which ($A_4A_3A_2A_1$) decides the number of converter cores to be switched (N_{phase}) in the following cycle. Each converter core has an individual set of non-overlap gate signal generation and driving circuit.

In order to minimize the output voltage ripple during the steady state and achieve fast output voltage recovery during load transients, two operation modes are implemented, namely coarse mode and fine mode operations. During the steady state, the output voltage has small ripple around the reference voltage, the controller employs the fine mode control. The output voltage V_{out} is sampled and compared to V_{ref} at the end of each sampling clock cycle (i.e. $1/(2f_{sw,max})$). When $V_{out} < V_{ref}$, the UP signal goes high, the counter output $A_4A_3A_2A_1$ (the binary form of N_{phase}) and hence the number of converter cores that will be switched (N_{phase}) in the following clock cycle will be increased by a minimum step size of one, unless N_{phase} has already reached its maximum value. Similarly, when $V_{out} > V_{ref}$, the DOWN signal goes high and the number of converter cores to be switched in the following cycle will be reduced by one, unless N_{phase} is already at its minimum value, 0. The minimum step size of one ensures tight regulation with small output voltage ripple around V_{ref} . In this design, the number of interleaved phases is chosen as 15. Hence the maximum number of converter cores that can change phase ($N_{phase,max}$) within each clock cycle is 15. The 15 phases are distributed over the whole clock cycle.

Figure 4.4 illustrates an example of N_{phase} going up and down between three and four from cycle to cycle during the steady state. The transient response of a

hysteretic controlled SC converter is mainly limited by the output voltage detection frequency. As discussed earlier in Section 4.1, the output voltage of a conventional multiphase phase interleaved is compared to V_{ref} at each phase instant. In the proposed design, the output voltage comparison is performed only once at the end of each clock cycle (note that there are 15 phases within each clock cycle). Therefore, the output voltage detection frequency is reduced by 15 times than that of conventional designs. Hence, in order to improve the output voltage recovery speed during large load transients, two additional control boundaries V_H and V_L are used, whereby the coarse operation mode will be enabled when the output voltage falls below V_L or rises above V_H .

Figure 4.4 Operation principle during steady state.

Figure 4.5(a) illustrates an example when the load current increases, which causes $V_{out} < V_L$. The UP_C signal goes high, causing the controller to switch from the fine operation mode to the coarse operation mode. The 4-bit counter output $A_4A_3A_2A_1$ is increased with a step size of five to quickly recover the output voltage back to around the reference level, after which the controller switches to the fine operation mode.

(a)

(b)

Figure 4.5 Operation principle during (a) step-up load transient; (b) step-down load transient.

If there is a sudden load decrease, as shown in Figure 4.5(b), V_{out} can rise above V_H , as a result, the $DOWN_C$ signal goes high and the number of converter cores that

will be switched in the next clock cycle is reduced by a step size large than one. The controller returns to the fine operation mode when the detected output voltage is smaller than V_H .

4.2.2 Implementation

The implementation of the whole system is shown in Figure 4.6. The 15 phase clocks with the same frequency are generated by a ring oscillator based VCO with 15 inverter stages. Each phase corresponds to a switched-capacitor converter core. The number of converter cores that are switched during a clock cycle is determined by the 4-bit counter output, $A_4A_3A_2A_1$. Here, A_1 , A_2 , A_3 and A_4 controls one, two, four and eight phases, respectively. As shown in the Figure 4.6, A_1 controls Phase 8, A_2 controls phase 4 and phase 12, A_3 controls phase 2, phase 6, phase 10 and phase 14, all the other eight phases are controlled by A_4 which is the most significant bit (MSB). It is noted that the different phases controlled by the same control bit are distributed over the whole clock period, hence the corresponding switching activities will also be distributed to minimize the output voltage ripple as much as possible.

Each converter core will change its phase only when the respective phase clock goes high, and the corresponding control bit is high. For example, the first converter core changes its phase (V_{sw1}) when phase 8 goes high while $A_1 = 1$. On the other hand, the if $A_1 = 0$, the corresponding converter core remains idle during the clock cycle.

Figure 4.6 Implementation of hysteretic control for multiphase SC converters.

The power stage of each switched-capacitor converter core is shown in Figure 4.7. Each SC converter core uses two 18 pF flying capacitors. The same dynamic comparator as presented in Chapter 3 is used in this multiphase implementation.

Figure 4.7 The power stage of each 1/2 converter core.

4.3 Simulation Results

The proposed regulation method is implemented in a 15-level interleaved voltage divider and is simulated in 0.35 μm CMOS process. A regulated output voltage of 1.35 V is generated from a 3 V input supply. The ring-oscillator based VCO generates 15 clock phases with frequency of 33 MHz. Without using a dedicated output capacitor, Figure 4.8 shows a peak to peak output ripple of 40 mV when the converter is delivering a constant output current of 3 mA. The number of phases ($A_4A_3A_2A_1$) changes by one from cycle to cycle.

Figure 4.8 Simulated steady state waveforms with $I_{out} = 3$ mA.

The conventional regulation method using 15 comparators is also simulated, which shows a slightly lower output voltage ripple of 35 mV using zero output capacitance, as shown in Figure 4.9. On the other hand, a non-interleaved SC converter results in 600 mV output ripple under the same load condition. Hence, the non-interleaved SC converter needs a dedicated output capacitor to reduce the output voltage ripple to an acceptable value. Figure 4.10 shows that the non-interleaved SC converter achieves similar output voltage ripple when 3 nF output capacitor is used. Such an output capacitor is often too large to be integrated in standard CMOS technology.

Figure 4.9 Simulated steady state waveforms with $I_{out} = 3$ mA, with standard multiphase interleaving.

The load transient response is simulated by switching the load current between 1.5 mA and 3.5 mA. Figure 4.11 shows that increasing the output current causes the output voltage to fall below the lower control boundary, which is set at 1.25 V. As a result, the signal UP_C goes high, causing the converter to switch from fine to coarse operation mode. The four-bit signal ($A_4A_3A_2A_1$) is increased from 0100 to 1001 by increasing both the two most significant bits (A_4A_3) and the two least significant bits (A_2A_1), therefore the number of switched converter cores increases from 4 to 9 to recover the output voltage quickly. And after that, the coarse operation mode is disabled. Similarly, during the step down load transient, the output voltage crosses the higher control boundary, which is set at 1.43 V and the number of active converter cores in the following cycle is reduced from 14 ($A_4A_3A_2A_1 = 1110$) to 9 ($A_4A_3A_2A_1 = 1001$) to bring the output voltage down quickly.

Then after the fine mode operation is enabled and the number of active SC cores increases/decreases by one from cycle to cycle.

Figure 4.10 Simulated steady state waveforms with $I_{out} = 3$ mA, with standard single-phase converter.

Figure 4.11 Transient response when I_{out} changes between 1.5mA and 3.5mA.

The simulated power conversion efficiency versus output current is shown in Figure 4.12. The converter peak efficiency of 81.5% when delivering 3.2 mA output current. Table 4.1 shows the comparison with some of the fully integrated switch cap DC-DC converters. The proposed converter achieves comparable efficiency and output power with the reported works. In [82], a single phase DC-DC converter is implemented, hence, it requires a large off-chip output capacitor to reduce the output voltage ripple. The proposed converter uses fifteen phase interleaving to achieve low output ripple without using a dedicated output capacitor, and each of the three comparators operates at a speed which is only twice the maximum switching frequency of the converter cores.

Figure 4.12 Simulated power conversion efficiency versus output current.

TABLE 4.1 COMPARISON WITH SOME OF THE MULTIPHASE SC CONVERTERS

Work	[57]	[82]	[43]	[51]	This Work
Technology	130 nm	0.35 μm	90 nm	65 nm	0.35 μm
Regulation Method	Hysteretic	Digital PWM	PFM	Open-loop	Triple-Boundary Hysteretic
Conversion ratio	1, 2/3, 1/2, 1/3	2/3	1/2, 2/3	1/4, 1/3	1/2
V_{in}	1.5 V	2.5 V	1.2 – 2V	1.5 – 2.5 V	3 V
V_{out}	0.4 -1.1 V	0.9 – 1.5 V	0.7 V	0.4 – 0.7 V	1.35 V
$P_{\text{out, max}}$	1.1 mW	7.5 mW	10 mW	26 mW	7 mW
Peak Efficiency	93%	66.7 %	81%	79.5% @ 0.6 V 63% @ 0.4 V	81.5 %
# of Phases	4	1	41	9	15
# of Comparators	1	N/A	N.A.	N.A.	3
SC Core Switching Frequency	Up to 2 MHz	1 MHz	50 MHz	100 MHz	16.5 MHz
Comparator Switching Frequency	8 MHz	N/A	N.A.	N.A.	33 MHz
Total C_{fly}	8 nF	6.72 nF	1.15 nF	4 nF (estimated)	540 pF
C_{out}	10 nF	External 470 nF	84 pF	N.A.	0
Output Ripple	N.A.	110 mV	3.8 mV	N.A.	40 mV

4.4 Conclusion

In this Chapter, a triple-boundary hysteretic regulation method is proposed for multiphase interleaved switched-capacitor DC-DC converters. The technique contains a total of three comparators, each defines a control boundary. Compared to the conventional implementations, which use N (level of interleaving) comparators or one shared comparator operating at N times higher frequency for output regulation, this technique uses three comparators that operate at only twice the maximum switching frequency of a the converter cores, therefore area overhead of the multiple comparators or the stringent requirement of a high speed comparator is

reduced. The mismatch issue of multiple comparators is also avoided. Besides the reference voltage, two additional control boundaries are introduced to enable coarse mode of operation to achieve fast output voltage recovery during load transients. During the steady state, the converter operates in the fine mode to ensure small output voltage ripple at constant load condition. Moreover, by controlling the number of SC cores that are being switched, the switching losses associated with the parasitic bottom-plate capacitance and the gate switching loss can be made to scale with the output current.

Chapter 5 PROPOSED SWITCHED-CAPACITOR DC-DC CONVERTER WITH INTEGRATED NMOS-LDOS

As illustrated in Section 2.6.4, in order to provide low noise supply rails (low ripple, low noise) for noise sensitive applications, such as data converters [105, 106], while achieving high conversion efficiency, a low-dropout regulator (LDO) is commonly cascaded with a high efficiency switching mode DC-DC converter (e.g. inductive DC-DC converter, switched-capacitor DC-DC converter) [70-72, 86, 87]. The post-regulation architecture also benefits from the good line and load regulation and fast transient response of the LDOs, which are more difficult to achieve using switching converters alone. This Chapter investigates the feasibility of combining the LDOs with the internal switches of the SC power stage to suppress the output voltage ripple without using additional power transistor and buffer capacitor.

5.1 Introduction

A PMOS-LDO is commonly used as the post filter to suppress the output voltage ripple and switching noise of a switching mode DC-DC converter [87, 107-109]. The LDO must be designed with sufficient headroom to stay away from the dropout region (hence large V_{ds} across the pass transistor) under all load current conditions, which however increases the power loss. A dropout voltage tracking circuit is presented in [86], which adjusts the drain-to-source voltage V_{ds} of the pass transistor dynamically to improve the power efficiency when load current decreases. In [72], A NMOS-LDO post filter with small dropout voltage of 50 mV is proposed to suppress the switching ripple/noise of a switched-capacitor DC-DC converter. However, the V_{ds} of the pass transistor can go as high as 220 mV which is a

significant drop when the output voltage is 1 V. Furthermore, an additional buffer capacitor and power transistor are always needed using the conventional cascaded structure, which results in increased die area and additional external component.

As presented in Section 2.6.5 and Section 2.6.6, in order to save these additional components, there have been research works that integrate the pass transistor of the LDOs with one or more of the inherent switches of the SC converter [57, 70, 88-93]. In [92], quasi-switched control (QSC) method is reported which regulates the output voltage of a SC DC-DC converter by controlling the charging current during converter's charging phase. The main purpose of the QSC method is to reduce the input current ripple of the SC converter, hence one of the power switches during the input charge transfer phase is regulated. However charge transfer during the discharging phase is not controlled, therefore the output voltage ripple is not suppressed and the load transient response is limited by the switching frequency. In [91], a pseudo-continuous control (PCC) scheme is reported which regulates the output voltage during both phases of a cross coupled SC doubler. However, the common source configuration of the regulated power transistors creates multi-pole loop response, which limits the loop unity-gain bandwidth. Hence significant output voltage ripple and slow transient response are observed. Moreover, the PCC control is not truly continuous due to the switching nature of the SC converter. Therefore, unlike the cascaded structure, the high frequency switching noise during converter phase transitions remains un-attenuated.

In this Chapter, a step-down switched-capacitor DC-DC converter with no-load voltage conversion ratio of $M_{VCR,NL} = 2/3$ is proposed. An NMOS-LDO [110] is integrated with the SC converter in both charging and discharging phases to

suppress the output voltage ripple. By monitoring the drain-to-source voltage across the regulated transistors, minimum drop-out voltage can be used to reduce the additional power loss while ensuring sufficient ripple rejection from the input of the integrated NMOS-LDOs to the output of the converter. A gate driving strategy is proposed which reduces the high frequency switching noise during phase transitions and assists the turn-on of the regulated transistors by using adaptive gate-slope technique and gate pre-charge technique, respectively.

5.2 Proposed SC Converter with Integrated NMOS-LDOs

The proposed SC converter with integrated NMOS-LDOs is presented in this Section.

5.2.1 Architecture

The architecture of the proposed SC DC-DC converter with embedded NMOS-LDOs is shown in Figure 5.1. As illustrated in Chapter 2, in a conventional switched-capacitor DC-DC converter, all the power transistors ($M_1 - M_7$) are operated as switches that are either OFF or ON. When ON, the power transistors typically operate in the triode region with finite on-resistance, giving rise to pulse-like charging and discharging currents that decay exponentially and resulting in output voltage ripple [49, 90, 94, 95]. In the proposed SC DC-DC converter, the power transistors M_3 and M_4 are controlled to function as NMOS-LDOs during the charging phase (Φ_1) and M_7 is operated as another NMOS-LDO during the discharging phase (Φ_2). Ideally, the negative feedback control loop forces a constant current that is equal to the load current through the regulated transistors in steady state, generating zero output voltage ripple. Unlike the traditional

PWM/PFM regulation methods, where the control loop bandwidth is practically limited to approximately 1/5 the switching frequency, as illustrated in Section 2.6, the control loop bandwidth of the proposed SC converter is no longer limited by the converter switching frequency, the in-phase regulation can achieve fast transient response similar to a conventional LDO.

M_1, M_2 : 6mm/180nm; M_3, M_4 : 5mm/180nm; M_5, M_6 : 3mm/180nm; M_7 : 10mm/180nm

Figure 5.1 System architecture of the proposed SC converter with integrated LDOs.

5.2.2 Design Considerations

Since the integrated LDOs are connected directly to the charging and discharging paths of the flying capacitors, they suffer from large input voltage ripple. Specifically, when turned ON (during the charging phase Φ_1), M_3 and M_4 are

connected to node NB and NC, respectively, as shown in Figure 5.1. Similarly, M_7 is connected to node NA when it is turned ON (during the discharging phase Φ_2). Hence large ripple rejection from the input of the LDOs to the output is needed. As will be discussed in Section 5.2.5, a NMOS-LDO results in better input rejection performance than that of a PMOS counterpart. Furthermore, using a PMOS-LDO requires a gate voltage swing approximately equal to its input (i.e. NB/NC in Φ_1 or NA in Φ_2) if constant currents (hence V_{GS}) were to be forced through the regulated transistors during the steady state. On the other hand, the source of the NMOS-LDO pass transistor is connected to the output, which is expected to be constant, hence the gate voltage would be approximately constant as well. Therefore, the use of NMOS-LDOs reduces the gate voltage swing of the regulated transistors within each switching phase significantly, which relaxes the swing and slew rate limitation of the error amplifier that drives the power transistors.

In order to ensure sufficient input ripple rejection, a minimum drain-to-source voltage $V_{ds,min}$ across the regulated transistors is ensured. The SC converter changes its phase whenever the drain-to-source voltage (V_{ds}) across the regulation transistors falls below the predefined minimum value ($V_{ds,min} = 80$ mV in this case). This minimum drain-to-source voltage can be defined by the built-in offset of the comparator which compares the drain and source voltages of the regulation transistors. This $V_{ds,min}$ of 80 mV translates to approximately 6.7% ($6.7\% = \frac{0.08 \text{ V}}{\frac{2}{3} \times 1.8 \text{ V}} \times 100\%$) efficiency loss, when the converter delivers an output voltage of 1 V from an 1.8 V input supply. By monitoring the V_{ds} across the regulated transistors during each phase and changing the phase when V_{ds} drops to $V_{ds,min}$, the SC converter is self-switched and a dedicated clock generator is not needed.

However, since the self-oscillation of the SC converter is established by monitoring its own inter node voltages (i.e. NA, NB/NC), a start-up circuit is required which charges the internal nodes and output node to proper voltages to make sure that the system starts up properly.

To prevent shoot through current, the charging and discharging phases are non-overlapped. To reduce the high frequency switching noise due to rapid changes of the current flowing to the output (large di/dt) during phase transitions, and to avoid excessive delay during phase transitions, adaptive ON/OFF gate slopes are used to when the power transistors are turned ON/OFF, as will be discussed in Section 5.2.6. Moreover, since the regulated transistors are turned ON and OFF periodically, when a converter phase begins, the respective integrated LDO must be restarted by charging the gate voltage of the pass transistor from zero volt to the desired voltage. However, the negative feedback loop takes time to settle the gate voltage to the desired value, during which period the output voltage ripple will be increased significantly. Therefore, a gate pre-charge technique is proposed whereby the gate voltage of a regulation transistor, when it is ON, is stored and used to pre-charge the gate of another regulation transistor when the subsequent phase begins. As a result, the gate voltage of the regulation transistors can be settled to the desired value much faster, resulting in much lower output voltage ripple. Moreover, the quiescent current of the error amplifier can be greatly relaxed, since it does not need to provide the large inrush current required to turn on the regulation transistors fast.

5.2.3 SC Power Stage and Switching Sequence

The switched-capacitor converter with no-load voltage conversion ratio ($M_{VCR,NL}$) of $2/3$ has five operating states including the main charging and discharging states and

three intermediate states during the converter phase transitions, as shown in Figure 5.2. The intermediate states are necessary for elimination of shoot through current in the power stage and reduction of switching noise due to the di/dt during the phase transitions [111]. Figure 5.3 shows the voltage ripple across the flying capacitors and the node voltages at NA, NB and NC during both switching phases. During the charging phase, both M_3 and M_4 are operated as the regulation transistors while M_1 and M_2 are operated as switches. Both M_3 and M_4 carry half of the output current which charges the flying capacitors C_1 and C_2 linearly. As the voltage across C_1 and C_2 ($V_{C1,2}$) increases, the drain-to-source voltage ($V_{ds3,4}$) across M_3 and M_4 reduces while the output voltage remains constant due to the negative feedback control loop. The charging process is ended when $V_{ds3,4} < V_{ds,min}$, where $V_{ds,min}$ is the predefined minimum drain-to-source voltage. Hence, neglecting the voltage drop across the switches M_1 and M_2 , both the voltages across C_1 and C_2 are charged to

$$V_{Cfly,H} = V_{in} - V_{out} - V_{ds,min} \quad (5.1)$$

at the end of the charging phase. Meanwhile, the voltages at node NB and NC drops linearly from

$$V_{NBC,max} = V_{in} - V_{Cfly,L} \quad (5.2)$$

to

$$V_{NBC,min} = V_{in} - V_{Cfly,H} \quad (5.3)$$

The drain-to-source voltage of the regulation transistors M_3 and M_4 drops from

$$V_{ds,max} = V_{in} - V_{Cfly,L} - V_{out} \quad (5.4)$$

to

$$V_{ds,min} = V_{in} - V_{Cfly,H} - V_{out} \quad (5.5)$$

Figure 5.2 The 2/3 SC power stage switching sequence.

Figure 5.3 SC node voltages and voltage ripple across flying capacitors.

The charging state is stopped by turning OFF M_3 and M_4 first, followed by the switches M_1 and M_2 . As will be shown in Section 5.2.6, the slope of the gate voltages of M_3 and M_4 are adjusted adaptively to reduce the ringing caused at the output without introducing excessive delay. The converter enters the discharging state by turning the switches M_5 and M_6 ON first followed by the regulation transistor M_7 . The gate voltage of M_7 is pre-charged to the desired value at a slope that turns ON M_7 fast without causing significant ringing at the output.

During the discharging state, C_1 and C_2 are connected in series and are discharged to the output. As C_1 and C_2 discharge, V_{ds7} reduces. The discharging phase ends when $V_{ds7} < V_{ds,min}$ by disconnecting M_7 first followed by M_5 and M_6 . At the end of the discharging phase, C_1 and C_2 are discharged to

$$V_{Cfly,L} = \frac{1}{2}(V_{out} + V_{ds,min}) \quad (5.6)$$

Meanwhile, the node voltage at NA drops from

$$V_{NA,max} = 2V_{Cfly,H} \quad (5.7)$$

to

$$V_{NA,min} = 2V_{Cfly,L} \quad (5.8)$$

The converter returns to the charging stage by turning M_1 and M_2 on followed by M_3 and M_4 . Similarly, the turn-off slope of M_7 and turn-on slope of M_3 and M_4 are designed carefully to reduce output ringing without increasing the delay significantly during the phase transition.

During no-load condition, the voltage across both C_1 and C_2 remains constant, hence

$$V_{Cfly,H} = V_{Cfly,L} \quad (5.9)$$

resulting in

$$V_{out} = \frac{2}{3}V_{in} - V_{ds,min} \quad (5.10)$$

Note that the no-load voltage conversion ratio is given by $\frac{2}{3}$ when all the power transistors are operated as switches and no minimum drain-to-source voltage is

applied across the regulation transistors. Operating M_3 , M_4 and M_7 as LDOs results in a DC offset in the output voltage by an amount equal to the predefined minimum drain-to-source voltage $V_{ds,min}$ across the regulation transistors.

In order to implement the above mentioned SC-converter switching sequence, a non-overlap gate signal generation circuit is used as shown in Figure 5.4(a). The gate drivers of the switches M_1 , M_2 , M_5 and M_6 are built into the delay line, which ensures that the respective switches are turned ON earlier than the regulated transistors when a phase begins and turned OFF later than the regulated transistors when the phase ends. Figure 5.4(b) illustrates the timing diagram of the associated gate signals of the power transistors M_1 - M_7 . When $V_{ds,3,4} < V_{ds,min}$, the SC-converter is required to change from charging phase to discharging phase, the input Φ of the non-overlap gate signal generator becomes one, at the same time Φ_1 becomes zero. The gate voltages ($V_{G3,4}$) of the regulation transistors M_3 and M_4 are discharged to ground first, disconnecting the current flow to the output. The switches M_1 and M_2 are turned OFF after a delay of T_{d1} . The converter enters the discharging phase by turning ON the switches M_5 and M_6 after another delay of T_{d2} . The regulation transistor M_7 is turned ON immediately after M_5 and M_6 are ON. Similarly, when the discharging phase ends, M_7 is turned OFF first. M_5 and M_6 are turned OFF after T_{d2} , M_1 and M_2 are turned ON after additional delay of T_{d1} and the regulation transistors M_3 and M_4 are turned ON last.

(a)

(b)

Figure 5.4 (a) Non-overlap gate signal generation circuit; (b) SC-converter switching sequence timing diagram.

Figure 5.5 Comparator with built-in offset.

To trigger a phase change when V_{ds} of the regulated transistors falls below the predefined value, a comparator with built-in offset is used to compare the drain and source voltages of the conducting regulated transistors. As shown in Figure 5.5, the input transistors of the comparator are designed with size ratio of $(W/L)_1 : (W/L)_2 = 1 : 5$, which generates an offset given by

$$V_{os} = \left(1 - \frac{1}{\sqrt{5}}\right) \sqrt{\frac{I_b}{\mu_n c_{ox} (W/L)_1}} \quad (5.11)$$

However, the offset of the comparator is subject to PVT variations. A practical and efficient way to compensate for this variation is to make the aspect ratio of the input transistors programmable.

5.2.4 Equivalent DC model of the SC DC-DC Converter

As illustrated in Section 2.4, a switched-capacitor DC-DC converter can be modeled using an ideal DC transformer and an equivalent series output impedance. A similar model is derived here for the proposed SC DC-DC converter to study the effect of operating the power transistors M_3 , M_4 and M_7 as LDOs on the current delivery performance of the SC DC-DC converter. Figure 5.3 shows the node voltages of NA, NB, NC and the voltage across the flying capacitors during both switching phases. The voltages across both flying capacitors are charged to $V_{Cfly,H}$ at the end of the charging phase (Φ_1) and discharged to $V_{Cfly,L}$ at the end of the discharging phase (Φ_2). For completeness, the on resistances of the switches (M_1 - M_2 , M_5 - M_6) are included here. Assume all the switches have the same on resistance R_{on} ,

$$V_{Cfly,H} = V_{in} - V_{out} - V_{ds,min} - \frac{1}{2}I_{out}R_{on} \quad (5.12)$$

$$V_{Cfly,L} = \frac{1}{2}(V_{out} + V_{ds,min} - 2I_{out}R_{on}) \quad (5.13)$$

The voltage ripples across the flying capacitors are given by

$$\Delta V_{Cfly} = V_{Cfly,H} - V_{Cfly,L} = V_{in} - \frac{3}{2}V_{out} - \frac{3}{2}V_{ds,min} - \frac{3}{2}I_{out}R_{on} \quad (5.14)$$

Hence the charge being delivered to the output in a complete switching cycle is given by

$$Q_{out} = 3C_{fly}\Delta V_{Cfly} = \frac{9}{2}C_{fly}(\frac{2}{3}V_{in} - V_{out} - V_{ds,min} - I_{out}R_{on}) \quad (5.15)$$

The average current delivered to the output is simply obtained by multiplying the charge delivered in each switching cycle with the switching frequency:

$$I_{out} = Q_{out} f_{sw} = \frac{9}{2} C_{fly} f_{sw} \left(\frac{2}{3} V_{in} - V_{out} - V_{ds,min} - I_{out} R_{on} \right) \quad (5.16)$$

Therefore,

$$V_{out} = \frac{2}{3} V_{in} - \left(\frac{1}{\frac{9}{2} C_{fly} f_{sw}} + R_{on} \right) I_{out} - V_{ds,min} \quad (5.17)$$

Note that $\frac{2}{3} V_{in}$ is the no-load voltage of the SC converter topology when all power transistors are operated switches and $\frac{1}{\frac{9}{2} C_{fly} f_{sw}}$ is the equivalent output impedance of the SC converter in the SSL, this term arises due to the fact that the converter relies on the voltage ripple of the flying capacitor to trigger phase transitions. Since constant currents flow through the switches, the on-resistance of the switches introduce additional constant IR voltage drop in the output voltage during constant load condition. Using equation (5.17), the proposed SC converter with M₃, M₄ and M₇ functioning as LDOs can be modeled using the circuit of Figure 5.6. Operating M₃, M₄ and M₇ as LDOs with a predefined minimum drain-to-source voltage $V_{ds,min}$ simply introduces an additional constant DC offset voltage drop of $V_{ds,min}$ in the output impedance model. This translates to series efficiency loss of $\eta_{loss} = \frac{V_{ds,min}}{M_{VCR,NL} V_{in}}$.

Figure 5.6 Equivalent DC model of proposed SC-converter with integrated LDOs.

5.2.5 Switching Integrated NMOS-LDOs

To implement the continuous in-phase regulation, M_3 and M_4 are regulated to behave like the regulated pass transistors of LDOs in the charging phase while M_7 is operated as the regulation transistor in the discharging phase. Since the inputs of the integrated LDOs are connected to the charging and discharging nodes (i.e. NA, NB and NC) of the switched-capacitor power stage, the input voltages varies significantly during both switching phases. As shown in Figure 5.3, the voltage at nodes NB and NC drops from $V_{in} - V_{cfly,L}$ to $V_{in} - V_{cfly,H}$ during the charging phase and the voltage at node NA drops from $2V_{cfly,H}$ to $2V_{cfly,L}$ during the discharging phase. With $V_{in} = 1.8$ V, $V_{out} = 1$ V and $V_{ds,min} = 80$ mV, $V_{cfly,L}$ and $V_{cfly,H}$ are obtained as 540 mV and 720 mV respectively, from equation (5.6), and (5.1). Hence the NMOS-LDO with M_3 and M_4 as pass element needs to suppress the input ripple of 180 mV in the charging phase and the LDO with M_7 as pass element needs to suppress 360 mV input ripple in the discharging phase. Large input rejection (from LDO input to output) is needed to achieve low output voltage ripple.

The pass element of a LDO is commonly implemented as PMOS transistor, as shown in Figure 5.7(a). The input ripple rejection (IRR) of the PMOS-LDO is given by

$$IRR_P = \frac{v_{out}}{v_{in}} = \frac{g_{mP}r_{oP}+1}{g_{mP}r_{oP}A(s)+1} \approx \frac{1}{A(s)} \quad (5.18)$$

where g_{mP} and r_{oP} are the transconductance and output resistance of the PMOS pass transistor and $A(s)$ is the gain of the error amplifier. When a NMOS transistor is used as the pass element, as shown in Figure 5.7(b), the input rejection of the NMOS-LDO is given by

Figure 5.7 Simplified circuit of (a) PMOS-LDO; (b) NMOS-LDO.

$$IRR_N = \frac{v_{out}}{v_{in}} = \frac{1}{1 + g_{mN}r_{oN}[A(s)+1]} \approx \frac{1}{g_{mN}r_{oN}A(s)} \quad (5.19)$$

where g_{mP} and r_{oP} are the transconductance and output resistance of the NMOS pass transistor. Note that the input rejection of the NMOS-LDO is better than that of the PMOS-LDO by the intrinsic gain of the NMOS power transistor. Moreover, when a PMOS pass transistor is used, the input ripple appears on the source of the power transistor, hence in order to maintain constant current, the gate voltage of the PMOS transistor must have the same voltage swing as the input node. On the other hand, if a NMOS pass transistor is used, the source voltage is connected to the regulated output node, hence the gate voltage remains constant during the entire switching phase. Due to these reasons, the regulated transistors M_3 , M_4 and M_7 are implemented as NMOS transistors.

The equivalent circuit of the SC-converter is shown in Figure 5.8. During the charging phase, node NB and NC are identical. The regulation transistors M_3 and

M_4 are designed with the same size $(W/L)_{3,4}$ and each carries half of the output current. The SC converter can be viewed as a NMOS-LDO with a single power transistor with size of $2(W/L)_{3,4}$ carrying the full output current. The node NB (or NC) is seen as the input of the LDO. In the discharging phase, the regulation transistor M_7 carries the full output current, hence M_7 is designed with twice the size of M_3 and M_4 . The equivalent NMOS-LDO in the discharging phase is the same as that of the charging phase except that node NA is now seen as the input.

Figure 5.8 Equivalent switching NMOS-LDOs.

An error amplifier with two gain stages provides the high loop gain and a switchable buffer drives the respective regulation transistors. The first gain stage utilizes a cascode current mirror as active load to improve the matching. An NMOS cascode amplifier is used as the second gain stage to achieve high loop gain. The switchable buffer with shunt feedback (super source follower) attenuates the impedance at the gate of the regulation transistors [22]. As a result, the pole at the gate of the regulation transistors can be pushed to a high frequency. Moreover, both the quiescent current and the transistor size of the source followers M_{sf1} and M_{sf2} can be reduced. With reduced size of M_{sf1} and M_{sf2} , the pole at the output of second gain stage can be designed as non-dominant pole despite the high output resistance

of the cascode. The output pole of the NMOS-LDO is designed to be another non-dominant pole. The dominant pole of the regulator is designed at the output of the first gain stage of the error amplifier by using a Miller compensation capacitor C_c .

Figure 5.9 (a) A super source follower (SSF) [22]; (b) small signal model of SSF.

The super source follower and its small signal model are shown in Figure 5.9.

Applying Kirchhoff's current law (KCL) at the output node gives

$$\frac{v_1}{r_{on1}} + g_{m2}v_1 + \frac{v_o}{r_{on2}/r_{op}} = 0 \quad (5.20)$$

Applying KCL at the drain of M_{sf} gives

$$\frac{v_1}{r_{on1}} + g_{msf}(v_i - v_o) + \frac{v_1 - v_o}{r_{osf}} = 0 \quad (5.21)$$

Substituting v_1 in (5.20) into (5.21) and rearranging gives

$$\frac{v_o}{v_i} = \frac{g_{msf}r_{osf}}{1 + g_{msf}r_{osf} + \frac{r_{osf} + r_{on1}}{(r_{on2}/r_{op})(1 + g_{m2}r_{on1})}} \quad (5.22)$$

The equivalent output resistance of the super source follower is obtained by setting

$v_i = 0$ and applying a test voltage at the output node. It can be shown that

$$R_o = r_{on2} // r_{op} // \frac{r_{osf} + r_{on1}}{(1 + g_{msf} r_{osf})(1 + g_{m2} r_{on1})} \quad (5.23)$$

If the current sources M_{N1} and M_P are ideal, $r_{on1} \rightarrow \infty$ and $r_{op} \rightarrow \infty$, and assume $g_{msf} r_{osf} \gg 1$, the output resistance is given by

$$R_o \approx r_{on2} // \frac{1}{g_{msf} r_{osf} g_{m2}} \approx \frac{1}{g_{msf} r_{osf} g_{m2}} \quad (5.24)$$

Compared to a conventional source follower, which gives output impedance of $\sim \frac{1}{g_{msf}}$, the output resistance of the super source follower is reduced by a factor of $\sim g_{m2} r_{osf}$. If both M_{N1} and M_P have finite output resistance on the same order of magnitude as that of M_{sf} , we assume $r_{on1} = r_{op} = r_{osf}$, the output resistance of the super source follower is given by

$$R_o \approx \frac{2}{g_{msf} r_{osf} g_{m2}} \quad (5.25)$$

which is smaller than that of the conventional source follower by a factor of $\sim \frac{1}{2} g_{m2} r_{osf}$.

Figure 5.10 Simulated frequency response of the super source follower.

Figure 5.10 shows the simulated frequency response of the super source follower, the -3 dB frequency (at 60 MHz) is well above the unity gain frequency of the equivalent NMOS-LDO (1.5 MHz), as shown in Figure 5.12. Figure 5.11 shows the small signal model of the equivalent NMOS-LDOs. Due to the impedance attenuated super source follower, the pole associated with the gate capacitance of the regulated transistors is neglected in the analysis [22]. In Figure 5.11, g_{m11} , g_{m24} , and g_{m1N} represent the transconductance of the differential input stage, the input transistor of second cascode gain stage and the pass transistor (M_3+M_4 , or M_7), respectively. The parasitic capacitances at the first and second gain stages of the error amplifier are denoted as c_1 and c_2 , respectively. r_{oN} represent the output resistance of the pass transistor. Let $R_x = R_L // r_{oN} // (R_{f1} + R_{f2})$. The loop gain transfer function of the equivalent NMOS-LDOs is given as

$$L(s) = \frac{\beta g_{m11} r_1 [s c_c R_x (1 + s c_2 r_2) - g_{mN} g_{m24} r_2 R_x]}{(g_{mN} R_x + 1)(1 + a s + b s^2 + c s^3)} \quad (5.26)$$

where

$$\beta = \frac{R_{f1}}{R_{f1} + R_{f2}} \quad (5.27)$$

$$a = r_1(c_1 + c_c) + c_2 r_2 + \frac{R_x(c_L + c_c)}{g_{mN} R_x + 1} + \frac{c_c r_1 g_{mN} g_{m24} r_2 R_x}{g_{mN} R_x + 1} \quad (5.28)$$

$$b = \frac{r_1 R_x(c_1 + c_c)(c_L + c_c)}{g_{mN} R_x + 1} + c_c r_2 + \frac{c_2 r_2 R_x(c_L + c_c)}{g_{mN} R_x + 1} - \frac{c_c^2 r_1 R_x}{g_{mN} R_x + 1} \quad (5.29)$$

$$c = \frac{r_1 c_2 r_2 R_x c_2(c_1 + c_c)(c_L + c_c)}{g_{mN} R_x + 1} - \frac{c_c^2 r_1 R_x c_2 r_2}{g_{mN} R_x + 1} \quad (5.30)$$

Writing the denominator as

$$D = (g_{mN} R_x + 1) \left(1 + \frac{s}{\omega_1}\right) \left(1 + \frac{s}{\omega_2}\right) \left(1 + \frac{s}{\omega_3}\right) \quad (5.31)$$

Assume $|\omega_1| \ll |\omega_2|, |\omega_3|$, and $g_{mN}R_x \gg 1$, the dominant pole is given by

$$\omega_1 \approx \frac{1}{a} \approx \frac{1}{r_1(c_1+c_c)+c_2r_2+\frac{(c_L+c_c)}{g_{mN}}+r_1c_cg_{m24}r_2} \quad (5.32)$$

Note that the Miller capacitance c_c is multiplied by the low-frequency gain of the second stage.

Figure 5.11 Small model of the equivalent NMOS-LDOs.

The simulated open-loop gain and phase of the NMOS-LDO under different load conditions are shown in Figure 5.12. The LDO achieves 75 dB DC loop gain and close to 90 degree phase margin when $I_{out} = 100$ mA. As the load current drops, the output pole moves towards the lower switching frequency, hence the phase margin drops. However, since the gain of the output stage also drops at very low loads, the phase margin is maintained above 51° across the entire load range, as shown in Figure 5.12(b). The minimum phase margin happens at $I_{out} = 100$ μ A, when the output pole equals the pole at the output of the second gain stage. The simulated worst-case (when $V_{ds} = V_{ds,min} = 80$ mV) input rejection performance of the LDO is shown in Figure 5.13. The maximum input rejection is 85 dB at low frequency and -

83 dB input ripple rejection is achieved at the converter switching frequency of 270 kHz when $I_{out} = 100$ mA.

(a)

(b)

Figure 5.12 (a) Simulated loop gain and phase of the equivalent NMOS-LDOs; (b) simulated gain margin and phase margin vs load current.

Figure 5.13 Simulated input ripple rejection of the equivalent NMOS-LDOs.

5.2.6 Gate Driving Strategy

As discussed in Section 5.2.3, the regulation transistors are turned OFF earlier than the switches when the respective phase ends and turned ON later than the switches when the phase begins. Hence the di/dt of the current flowing to the output is determined by the slope of the gate voltages of the regulation transistors. In order to reduce the switching noise and to assist the turn-on of the regulation transistors, a gate driving strategy implementing adaptive gate slope (AGS) and gate pre-charge is proposed, as shown in Figure 5.14. During the charging phase, the gates of M_3 and M_4 are continuously driven by the error amplifier to achieve in-phase regulation and suppress the output voltage ripple. Using NMOS source follower power stage, the gate voltage is expected to be constant during the steady state.

(a)

(b)

Figure 5.14 (a) Gate driving circuit; (b) gate switching waveform.

Therefore the gate voltage of M_3 and M_4 can be stored and used to pre-charge the gate of M_7 when the discharging phase begins. As a result, the error amplifier is not required to provide the large inrush current to turn ON the regulation transistors fast, hence the quiescent current of the can be greatly relaxed. When the charging phases ends, the gate voltage of M_3 and M_4 initially drops slowly to reduce di/dt . As the current drops, a larger gate slope can be used to further turn the transistor completely OFF fast to prevent unnecessary delay. A simple inverter is used to detect the gate voltage which turns the strong pull-down transistor on when the gate voltage drops below the trip point of the inverter. The same driving strategy is applied to M_7 during the discharging phase.

5.2.7 Start-up Circuit

Since the phase transition of the switched-capacitor power stage is determined by monitoring the internal node voltages (NA, NB and NC) and the output voltage, these voltages must be charged to proper values in order for the system start-up properly. The proposed start-up circuit is shown in Figure 5.15(a). A start-up comparator compares the output voltage with $1/2V_{in}$. When the output voltage is less than $1/2V_{in}$, the output capacitor is charged from the input through the transistors M_{s1} and M_{s2} . Meanwhile, a start-up reset signal resets the T-latch of the hysteretic controller ($\Phi = 0$), forcing the power stage to be connected in the charging configuration, hence the voltages at nodes NB and NC are charged together with V_{out} . The negative input of the main comparator is connected to V_{start} , as shown in Figure 5.15, which is more than 80 mV (the built-in offset of the comparator) larger V_{out} during the start-up. When V_{out} becomes larger than $1/2V_{in}$, the start-up reset signal

becomes low, hence the output of the T-latch changes state whenever a rising clock edge is detected. M_{s1} and M_{s2} are turned off and V_{start} is discharged to ground by M_{s3} .

(a)

(b)

Figure 5.15 (a) Start-up circuit of proposed SC-converter; (b) Start-up waveforms.

When $V_{start} < V_{out} + 80 \text{ mV}$, the main comparator output becomes high, the output of the T-latch toggles, hence Φ becomes 1 and the converter changes to the discharging phase. After that the start-up process is ended and the converter sustains self-oscillation by monitoring the V_{ds} of the respective regulation transistor in the both switching phases. A telescopic amplifier with PMOS input pair is used as the start-up comparator, as shown in Figure 5.16. The comparator is designed with hysteresis to prevent the system from going back to the start-up process due to any variation in the output voltage during the transition from start-up to self-oscillation mode.

Figure 5.16 Start-up comparator using telescopic amplifier with hysteresis.

5.3 Simulation Results

The proposed SC DC-DC converter with embedded NMOS-LDOs is designed in 0.18 μm CMOS process. Using two off-chip flying capacitors of 1 μF , the converter provides a regulated output voltage of 1 V from a 1.8 V input supply. The switching

frequency ranges from 0.9 kHz to 320 kHz corresponding to output current of 0.2 mA to 130 mA. Figure 5.17(a) shows the simulated load transient response when the output current switches between 10 mA and 100 mA with 100 ns rising and falling edges. Using an output capacitor of 2.2 μF , the ripple of the output voltage is less than 0.5 mV when the converter delivers 100 mA output current. Assuming the output capacitor has an ESL of 500 pH and ESR of 30 m Ω , small glitches of 10 mV are observed during the phase transitions. When the load current switches from 10 mA to 100 mA. The output voltage shows negligible undershoot and settles to a new steady state in 200 ns. This justifies the fast response of the NMOS-LDO. Similarly, no output voltage overshoot is observed when the output current switches from 100 mA to 10 mA. The output voltage settles to the new value within 150 ns. The response when the load current switches between the minimum load of 1 mA and the full load of 130 mA is shown in Figure 5.17(b). The steady state output voltage ripple at full load is less than 0.6 mV. The settling times are 1.7 μs and 1.4 μs for the loading and unloading transients, respectively. Nonetheless, the output voltage shows negligible undershoot and undershoot.

(a)

(b)

Figure 5.17 Simulated steady-state and transient response when (a) I_{out} switches between 10 mA and 100 mA; (b) I_{out} switches between 1 mA and 130 mA.

The simulated output spectrum of a conventional SC converter and proposed designs with and without adaptive gate slope (AGS) technique are shown in Figure 5.18. The proposed design suppresses the tones at switching frequency of 200 kHz and its harmonics since the output voltage ripple is suppressed by the embedded switching LDOs. The proposed AGS technique further reduces the high frequency noise due to the di/dt of the current flowing to the output during phase transitions, which causes the glitches in the output voltage. Figure 5.19 shows the simulated power conversion efficiency versus load current. Peak efficiency of 83.3% is achieved. Since the switching frequency is proportional to the load current, the efficiency is maintained above 80% over the load range of 5 mA to 130 mA.

Table 5.1 shows the comparison with prior DC-DC converters that suppress output ripple with cascaded LDO [72, 87], or pseudo-continuous control (PCC) [91]. The proposed design achieves the smallest output voltage ripple and load regulation. The load transient response is much faster than the design of [91] that used common-source PMOS as regulation transistor. Both the voltage undershoot and overshoot are smaller than those of the reported works. The design in [91] achieves higher conversion efficiency because its output voltage is higher, hence the efficiency overhead due to the dropout voltage across the regulated transistors is much smaller.

The proposed converter is sent for fabrication in 0.18 μ m CMOS technology. The layout is shown in Figure 5.20. However, the silicon measurement result is not available at this stage. The results should be included in the future.

(a)

(b)

(c)

Figure 5.18 Simulated output voltage spectrum of (a) Conventional design; (b) SC converter with in-phase regulation; (c) SC converter with in-phase regulation and adaptive gate slope.

Figure 5.19 Simulated power efficiency versus load current.

TABLE 5.1 COMPARISON WITH PRIOR DESIGNS WITH OUTPUT RIPPLE SUPPRESSION

Reference	[72]	[105]	[91]	This Work
Process	90 nm	0.25 μm	0.6 μm	0.18 μm
Architecture	Cascaded CP+LDO	Cascaded Buck+LDO	Integrated CP+PCC	Integrated CP+LDO
V_{out}	1 V	1.8 V	3.3 V	1 V
V_{in}	2.5 V	2.4-5.5 V	1.5-3.2 V	1.8 V
Max I_{out}	30 mA	400 mA	150 mA	130 mA
C_{fly}/L	0.54 nF	1 μF	1 μF (off chip)	1 μF (off chip)
C_{out}	0.26 nF	4 μF	2.2 μF	2.2 μF
Quiescent Current	10 μA	N.A.	N.A.	40 μA
Peak Efficiency	76.2%	86.5%	90%	83.3%
V_{out} Ripple	2 mV	1 mV	20 mV	< 0.6 mV
Load Regulation	0.2 mV/mA	N.A.	0.16 mV/mA	0.02 mV/mA
Settling Time	500 ns @ $\Delta I_{out}=20\text{mA}$ $t_{edge} = 200\text{ps}$	15 μs @ $\Delta I_{out}=160\text{mA}$	25 μs @ $\Delta I_{out}=100\text{mA}$ $t_{edge} = 1\mu\text{s}$	200 ns @ $\Delta I_{out}=90\text{mA}$ $t_{edge} = 100\text{ns}$
				1.7 μs @ $\Delta I_{out}=130\text{mA}$ $t_{edge} = 100\text{ns}$
V_{out} undershoot	195 mV	90 mV	50 mV	8 mV
V_{out} overshoot	195 mV	15 mV	50 mV	Negligible

Figure 5. 20 Layout of the proposed SC converter with integrated NMOS-LDOs.

5.4 Conclusion

In this Chapter, a $2/3$ step-down switched-capacitor DC-DC converter with integrated NMOS-LDOs is presented to achieve low output voltage ripple, good load regulation and fast load transient response. Since the LDO is coupled to the SC converter, a minimum drop-out voltage can be used which minimizes the additional power loss while ensuring sufficient ripple rejection. The switching noise due to converter phase transitions is reduced by adaptive gate slope. To minimize the quiescent current of the error amplifier, a gate pre-charge technique is used to assist the turn-on of the regulation transistors. The converter achieves peak efficiency of 83.3% and more than 72% across the load current range of 1 mA to 130 mA.

Chapter 6 ON-CHIP RECONFIGURABLE SWITCHED-CAPACITOR DC– DC CONVERTER FOR INDOOR PV ENERGY HARVESTING

Energy harvesting is an important application of low power switching converters. The feasibility of using SC converters for energy harvesting was studied in this thesis. The lack of input supply range is one of the known major limitations of SC converters as compared to traditional inductor based converters. This can be seen from the intrinsic efficiency of a SC DC-DC converter of $V_{out}/(M*V_{in})$. Obviously, to increase the input or output voltage range, multi-ratio (reconfigurable) topologies must be used, which however increases the circuit complexity. Nonetheless, for scenarios where the input voltage does not vary significantly (such as PV cell outputs under indoor condition), the SC converters are viable solutions.

In this Chapter, a reconfigurable switched-capacitor DC–DC converter is presented for indoor photovoltaic energy harvesting. A uniform hysteresis controller regulates the PV cell voltage at 1.5 V to extract the maximum power from the PV cell and regulates the load voltage at 0.9 V. To minimise the conversion loss, the energy is transferred from the PV cell to the load directly whenever energy is available in the PV cell. When the load voltage is high, the excess energy in the PV cell is stored in the buffer of 1.8 V. The load draws energy from the buffer when energy is not available in the PV cell. The proposed converter was fabricated in 0.18 μm CMOS process and achieves peak efficiencies of 87, 88 and 78% while delivering energy from the PV cell to the load, from the PV cell to the buffer and from the buffer to the load, respectively.

6.1 Introduction

Typical energy harvesting systems store the harvested energy in an intermediate energy buffer (such as rechargeable battery and super capacitor) and use additional conversion stages to deliver the stored energy to the load [112-114]. The energy conversions are commonly performed by inductive DC–DC converters with off-chip inductors, which are not favourable for size constrained smart nodes [113, 115, 116]. The additional energy processing stage to power the load causes additional energy loss and reduces the overall energy efficiency. In this Chapter, a reconfigurable switched-capacitor (SC) DC–DC converter is proposed for indoor photovoltaic (PV) energy harvesting. To improve the overall energy efficiency, the first converter topology transfers the energy from the PV cell to the load in one conversion stage when the PV energy is available and the load is demanding energy [11, 115]. When the load demands no energy, the excess energy in the PV cell is stored in the buffer through the second topology. The third topology acts as the backup converter, which is enabled to deliver the stored energy to the load when the PV energy is not available.

6.1.1 PV Cell Electrical Model

One of the most commonly used energy scavengers is photovoltaic (PV) cells which converts the light energy into electrical energy [115, 117-119]. A simplified single-diode model which entails the most important parameters of a PV cell is shown in Figure 6.1(a) [120]. Here I_{PH} is the induced electric current due to the separation and drift of electron–hole pairs which are generated when photons hit the solar cell. The diode D_{PV} represents the p-n junction of the PV cell, while R_S and R_P account

for the intrinsic resistance of the semiconductor material and the leakage current across the p-n junctions, respectively.

(a)

(b)

Figure 6.1 (a) Electrical model of PV cells [120]; (b) I-V and P-V characteristics of PV cells.

The current-voltage and power-voltage characteristics of a PV cell are illustrated in Figure 6.1(b). I_{SC} represents the current delivered by the PV cell when the output terminals of the PV cell are shorted (i.e. $V_{PV} = 0$ V). V_{OC} is the output voltage of the PV cell when output of the PV cell is open (i.e. $I_{PV} = 0$ A). When the cell voltage (V_{PV}) is low, the output current of the PV cell (I_{PV}) is close to the I_{PH} . As V_{PV} increases, the diode current and the leakage current through R_P increases, hence the

current delivered by the PV cell drops. By multiplying V_{PV} with I_{PV} , the power supplied by the PV cell is obtained. It can be shown that at any light intensity, there is a unique optimum value of V_{PV} (V_{MPP}) that results in maximum power extraction from the PV cell. Maximum power point tracking (MPPT) techniques, such as fractional open circuit [121], perturb and observe and incremental conductance techniques [122], are often implemented to ensure maximum power extraction under varying light conditions. For indoor photovoltaic systems, the lighting conditions can be well controlled and remain relatively constant. Hence the maximum power point of a PV cell can be determined prior to installation and a MPPT circuit can be eliminated. The small variation of V_{MPP} makes switched-capacitor power converter [112] a suitable candidate for indoor PV harvesting systems.

6.2 Proposed Switched-Capacitor PV Energy Harvesting System

6.2.1 System Architecture

The architecture of the proposed energy harvesting system is shown in Figure 6.2(a). The energy harvester extracts electric energy from a commercial PV cell which has a V_{MPP} of 1.5 V under typical indoor lighting conditions. Here, a uniform hysteresis controller regulates both the PV cell voltage V_{PV} and the load voltage V_{Load} . The PV cell voltage regulation ensures maximum power extraction while the load voltage regulation provides the desired supply voltage to the load. The SC converter has three different configurations to realize the energy flow from the PV cell to the load, from the PV cell to energy buffer and from the energy buffer to the load, respectively.

(a)

(b)

Figure 6.2 (a) Architecture of proposed PV energy harvesting system; (b) Operating waveforms.

Figure 6.2(b) illustrates the operating waveforms of the uniform hysteresis controller. The PV voltage regulation is implemented by adaptively comparing V_{PV} with V_{MPP} (the voltage corresponding to maximum power extraction) and $V_{MPP} - \Delta V_{MPP}$, where ΔV_{MPP} defines the size of the hysteresis band. The comparison result PV_High decides whether the PV energy is available. When $PV_High = 0$, no energy is extracted from the PV cell, hence V_{PV} increases due to the photovoltaic current I_{PV} . When V_{PV} crosses V_{MPP} , PV_High becomes 1. As a result, the SC converter draws energy from the PV cell and delivers the energy to the load or the energy buffer depending on the load condition. When V_{PV} falls below the lower threshold $V_{MPP} - \Delta V_{MPP}$ due to the energy extraction, PV_High returns to 0 and the energy extraction is stopped, allowing C_{PV} to be re-charged.

The load is regulated by comparing the reference voltage with two different scaled versions of the load voltage, $\beta_1 V_{Load}$ and $\beta_2 V_{Load}$. The comparison result V_{Load_High} indicates the load condition. When $V_{Load_High} = 1$, no energy is delivered to the load, hence V_{Load} drops. When V_{Load} crosses its lower threshold, V_{Load_High} becomes 0. The power required by the load will be drawn from the PV cell when $PV_High = 1$ or from the energy buffer when $PV_High = 0$. The energy in the PV cell will be transferred to the energy buffer when $PV_High = 1$, and $V_{Load_High} = 1$.

In another scenario, when $PV_High = 0$, and $V_{Load_High} = 1$, the SC converter enters the idle mode, since there is no excess energy in the PV cell and the load is not demanding power.

Figure 6.3 Proposed reconfigurable SC DC-DC converter power stage.

6.2.2 Reconfigurable switched-capacitor DC-DC converter

The proposed switched-capacitor DC-DC converter is shown in Figure 6.3. It provides three voltage conversion ratios of $2/3$, $4/3$ and $3/5$, corresponding to the power transfer from the PV cell to the load, from the PV cell to the energy buffer and from the energy buffer to the load, respectively.

TABLE 6.1 CONDUCTING SWITCHES FOR DIFFERENT GAIN SETTINGS IN EACH SWITCHING PHASE

Gain = 2/3		Gain = 4/3		Gain = 3/5	
Φ_1	Φ_2	Φ_1	Φ_2	Φ_1	Φ_2
S2, S22, S5, S24, S7, S27, S9, S30, S12, S33, S14, S36	S3, S16, S25, S10, S18, S28, S15, S20, S34	S2, S16, S17, S28, S14, S20, S19, S31	S1, S21, S4, S23, S6, S26, S8, S29, S11, S32, S13, S35	S1, S16, S24, S8, S18, S27, S13, S20, S33	S3, S16, S17, S28, S15, S20, S19, S31

Table 6.1 shows the conducting switches in each switching phase for the different converter topologies. In order for the multiple configurations to share the total amount of on-chip capacitance, the capacitance is equally divided into six capacitors, denoted by C1–C6.

A. 2/3-Converter Topology

When transferring energy from the PV cell to the load, the PV voltage of 1.5 V is converted to a regulated load voltage of 0.9 V. The topology with nominal voltage conversion ratio of 2/3 is selected. The equivalent circuit of the topology in both switching phases (Φ_1 and Φ_2) are shown in Figure 6.4. In the first phase, the voltages across the capacitors C1–C6 are charged from $(1/2)V_{Load}$ to $V_{PV} - V_{Load}$. In the second phase, C1 and C2 are connected in series, each capacitor is discharged from $V_{PV} - V_{Load}$ to $(1/2)V_{Load}$, releasing the charge to the load. Similarly, C3–C6 are discharged. The current delivered to the load is given by

$$I_{out,PV_L} = 9Cf_{sw,PV_L}(V_{PV} - \frac{3}{2}V_{Load}) \quad (6.1)$$

where C is the size of each charge transferring capacitor and f_{sw,PV_L} is the switching frequency when this converter topology is enabled. The current drawn from the PV cell is given by

$$I_{in,PV_L} = 6Cf_{sw,PV_L}(V_{PV} - \frac{3}{2}V_{Load}) \quad (6.2)$$

To implement the hysteresis PV voltage regulation, the switching frequency f_{sw,PV_L} must be sufficiently fast to ensure $I_{in,PV_L} > I_{PV}$ so that the converter is able to bring V_{PV} down whenever V_{PV} hits its higher threshold V_{MPP} . Similarly, I_{out,PV_L} must be greater than the load current for proper load voltage regulation.

Figure 6.4 2/3-converter topology in both switching phases.

B. 4/3-Converter Topology

When $PV_High = 1$ and $V_{Load}High = 1$, there is available energy in the PV cell and the load is not demanding power, the excess energy in the PV cell is delivered to the energy buffer through the 4/3-converter topology, which converts V_{PV} of 1.5

V to V_{Bat} of 1.8 V. The equivalent circuits in both charging and discharging phases are shown in Figure 6.5. The voltage across each flying capacitor is charged to $(1/3)V_{PV}$ in phase one and discharged to $V_{Bat} - V_{PV}$ in phase two. The current delivered to the battery is given by

$$I_{out,PV_Bat} = 6Cf_{sw,PV_Bat}(\frac{4}{3}V_{PV} - V_{Bat}) \quad (6.3)$$

where f_{sw,PV_Bat} is the switching frequency when this 4/3-topology is enabled. The current extracted from the PV cell is given by

$$I_{in,PV_Bat} = 8Cf_{sw,PV_Bat}(\frac{4}{3}V_{PV} - V_{Bat}) \quad (6.4)$$

Similar to the 2/3 converter topology, the f_{sw,PV_Bat} must be sufficiently fast to ensure $I_{in,PV_Bat} > I_{PV}$ so as to regulate the PV voltage properly.

C. 3/5-Converter Topology

When $PV_High = 0$ and $V_{Load_High} = 0$, the load voltage is low and the PV energy is not available, 3/5-topology is selected to convert the buffer voltage of 1.8 V to the load voltage of 0.9 V, as shown in Figure 6.6. The energy is delivered from the buffer to the load. The voltage across each flying capacitor is charged to $(1/2)(V_{Bat} - V_{Load})$ in phase one and discharged to $(1/3)V_{Load}$ in phase two. The current delivered to the battery is given by

$$I_{out,PV_Bat} = 5Cf_{sw,Bat_L}(\frac{1}{2}V_{Bat} - \frac{5}{6}V_{Load}) \quad (6.5)$$

where f_{sw,Bat_L} is the switching frequency when converter topology is enabled. To achieve proper load voltage regulation, I_{out,Bat_L} must be greater than the load current.

Figure 6.5 4/3-converter topology in both switching phases.

Figure 6.6 3/5-converter topology in both switching phases.

6.3 Measurement Results

The proposed SC DC-DC converter was fabricated in 0.18 μm CMOS technology with active area of $0.8 \times 0.78 \text{ mm}^2$, as shown in Figure 6.7. The converter uses a total amount of 2.5 nF on-chip capacitance implemented as dual-MIM capacitors.

The PV energy harvester was tested with a commercial PV cell featuring a 2.5 cm^2 size.

Figure 6.7 Die microphotograph of proposed reconfigurable SC DC-DC converter.

Figure 6.8(a) shows the transient waveforms of the regulated PV cell voltage and the load voltage across a $100 \text{ k}\Omega$ load resistance under 400 lx light intensity. Both C_{PV} and C_{Load} used 100 nF off-chip capacitance in the test. Figure 6.8(b) shows the waveforms at 200 lx light intensity. Since less power is extracted from the PV cell, more energy is transferred from the battery to the load, as indicated by the increased number of Bat-to-Load pulses.

Figure 6.9 shows the measured output power of the three converter topologies and the power conversion efficiencies versus switching frequency. When enabled, the 2/3-converter topology delivers $26 \text{ }\mu\text{W}$ of power from the PV cell to the load with peak efficiency of 87% at 100 kHz switching frequency. The 4/3-converter topology is designed to operate at the same switching frequency as the 2/3-topology, 88% peak efficiency is achieved while delivering $50 \text{ }\mu\text{W}$ of power from the PV cell to the energy buffer.

(a)

(b)

Figure 6.8 Measured transient waveforms at (a) 400 lx light intensity; (b) 200 lx light intensity.

The 3/5-converter topology is designed with switching frequency of 300 kHz, at which the converter achieves a peak efficiency of 78% while delivering 32 μ W of power from the energy buffer to the load when the PV energy is not available.

The Bat-to-Load efficiency is lower than other two topologies due to two reasons. Firstly, the intrinsic efficiency of a SC converter is given by $V_{out}/(M \cdot V_{in})$. According to this formula, the intrinsic efficiency of the Bat-to-Load topology is given by $0.9/1.08 = 83.3\%$, which is smaller than that of the PV-to-Load topology ($0.9/1 = 90\%$) and that of the PV-to-Bat topology ($1.8/2 = 90\%$). Secondly, the topology result in higher equivalent output resistance, which is given by $6/(25Cf_{sw})$ in SSL. The PV-to-Load topology gives equivalent SSL output resistance of $1/(6Cf_{sw})$ while the PV-to-Bat topology gives equivalent SSL output resistance of $2/(27Cf_{sw})$.

Figure 6.9 Measured output power and efficiency versus switching frequency.

Table 6.2 shows that the efficiency of each topology is comparable with state-of-the-art PV harvesters. The harvested energy in [112] and [113], and is stored in the battery requiring additional conversion stages to power the load, hence the overall efficiencies after the power is subsequently delivered to the load are expected to be lower than the values shown in the table. More over [113] uses a bulky 1 mH off-chip inductor which prevent the harvester from being integrated. The design in [115] interfaces the PV cell to the load directly, however an off-chip inductor is used similar to[113].

TABLE 6.2 COMPARISON WITH OTHER DC-DC CONVERTERS FOR PV ENERGY HARVESTING

Reference	[112]	[115]	[113]	This Work
Process	0.18 μm	0.18 μm	0.25 μm	0.18 μm
Architecture	PV-to-Battery	PV-to-Battery PV-to-Load Battery-to-Load	PV-to-Battery	PV-to-Battery PV-to-Load Battery-to-Load
Converter Topology	Reconfigurable SC-Boost	Inductive Buck-boost	Inductive Boost	Reconfigurable SC-Buck-Boost
C_{fly}/L	0.5 nF	10 μH	1 mH	2.5 nF
V_{out}	3.3 V	1.1V, 1.8V, 2.5 V	0-5 V	0.9V(PV/Bat-to-Load) 1.8V(PV-to-Bat)
V_{in}	0.45-3 V	1.5 V, 2.5 V	0.5-2 V	1.5V(PV-to-Load/Bat) 1.8V(Bat-to-Load)
f_{sw}	27 kHz – 1.05 MHz	312 Hz - 20 kHz	100 kHz	100kHz(PV-to-Load/Bat) 300kHz(Bat-to-Load)
Control circuit power consumption	0.4 – 3.84 μW	400 nW	2.4 μW @ $P_{\text{in}}=8.6\mu\text{W}$ 3.5 μW @ $P_{\text{in}}=1.66\text{mW}$	0.35 μW @ $P_{\text{PV_Load}}=26\mu\text{W}$ 0.6 μW @ $P_{\text{PV_Bat}}=50\mu\text{W}$ 0.9 μW @ $P_{\text{Bat_Load}}=32\mu\text{W}$
Throughput power	<50 μW	1-10 mW	<10 mW	<80 μW (PV-to-Load) <160 μW (PV-to-Bat)
Peak Efficiency	89%	83% (with MPPT)	87%	87% (PV-to-Load) 88% (PV-to-Bat) 78% (Bat-to-Load)
Active chip area (power stage)	0.8 mm^2 (estimated from chip photo)	4.6 mm^2	13 mm^2	0.62 mm^2

6.4 Conclusion

In this Chapter, an on-chip reconfigurable SC DC–DC converter for indoor PV energy harvesting is presented. Both the PV cell voltage and the load voltage are regulated by a uniform hysteresis controller for maximum power extraction and providing stable supply for the load circuit. To improve the overall efficiency, the harvested energy is delivered to the load in one conversion stage whenever PV energy is available and the load voltage is low. The excess energy from the PV cell is stored in the energy buffer, which powers the load circuit when PV energy is absent. The $2/3$, $4/3$ and $3/5$ converter topologies achieve peak efficiencies of 87, 88 and 78% while processing powers of 26, 50 and 32 μW , respectively.

Chapter 7 SUMMARY AND FUTURE WORK

Power management for today's SoC is challenging since the switching converters need passive components, especially inductors that occupy large PCB footprint and are hard to be integrated. Switched-capacitor DC-DC converters, which offer higher efficiency than linear regulators and lower cost than switched-inductor DC-DC converters, are promising solutions to compact, efficient and low-cost power management for SoCs. Switched-capacitor DC-DC converters are also promising solutions self-power devices that harvest ambient energies for operation.

This Chapter summarizes the contributions of this thesis and gives the future work directions of this research.

7.1 Summary of Contributions

This research reviews the voltage conversion and current delivery principles of switched-capacitor DC-DC converters and identifies the various power loss mechanisms. Different output regulation methods and noise reduction techniques in the literature are discussed. Four switched-capacitor DC-DC converters are developed to achieve different objectives.

In Chapter 3, a lower boundary hysteretic control method is proposed which achieves optimal output voltage ripple by matching the output sampling frequency to the converter switching frequency across the entire load range. The converter responds instantly to step-up load transients that are smaller than six times the initial load current. When larger load transient steps occur, the sampling frequency jumps to its maximum value to recover the output voltage quickly. Small output

voltage droop can be achieved while using an output capacitance value on the same order as the converter's charge transferring capacitance. A $1/2$ step-down SC DC-DC converter using on-chip MIM flying capacitance with the proposed control technique is fabricated in $0.18\text{ }\mu\text{m}$ CMOS process. The converter achieves a peak efficiency of 86.4% and delivers a maximum output power of 5.6 mW.

The hysteretic control technique is extended to multiphase interleaved switched-capacitor DC-DC converters. The proposed technique achieves both tight regulation in the steady state and fast response during the load transients by using three control boundaries. In the steady state, the output voltage is compared to a reference voltage, i.e. the first control boundary. The comparison result changes the phase number in the following clock cycle by a minimum step size to achieve tight regulation. To achieve fast output voltage recovery during load transients, a higher and a lower control boundary are introduced whereby the controller switches to a coarse operation mode whenever the output voltage crosses the higher or lower control boundaries. The converter achieves a peak efficiency of 81.5% and delivers a maximum output power of 7 mW

In order eliminate the output voltage ripple of a switched-capacitor DC-DC converter and improve the line and load regulation and transient response without post-filtering by cascaded LDOs. In Chapter 5, a $2/3$ step-down SC DC-DC converter with in-phase output voltage regulation is proposed. A NMOS-LDO is combined with the power switches of the SC converter in both charging and discharging phases. By monitoring the drain-to-source voltage across the regulated transistors, minimum drop-out voltage can be used to reduce the additional power loss while ensuring sufficient ripple rejection from the input of the integrated

NMOS-LDOs to the output of the converter. An adaptive gate slope technique is used to reduce the output glitches during phase transitions and a gate pre-charge technique assists the turn-on of the regulated transistor when the respective phase begins. The proposed converter, implemented in 0.18 μm CMOS technology using off-chip flying capacitors, achieves peak efficiency of 83.3% and achieves less than 0.5 mV output voltage ripple and less than 10 mV output glitches when delivering 100 mA output current.

To meet the demand for self-powered devices in the IoT era, a triple-topology reconfigurable switched-capacitor DC–DC converter is proposed for indoor photovoltaic (PV) energy harvesting. To improve the overall energy efficiency, the first converter topology transfers the energy from the PV cell to the load in one conversion stage when the PV energy is available and the load is demanding energy. When the load demands no energy, the excess energy in the PV cell is stored in the buffer through the second topology. The third topology acts as the backup converter, which is enabled to deliver the stored energy to the load when the PV energy is not available. The proposed converter was fabricated in 0.18 μm CMOS process and achieves peak efficiencies of 87, 88 and 78% while delivering energy from the PV cell to the load, from the PV cell to the buffer and from the buffer to the load, respectively.

7.2 Future Work

The sampling frequency control technique in Chapter 3 and the multiphase interleaving technique in Chapter 4 are meant to reduce the ripple of a SC DC-DC converter. The sampling frequency control technique reduces the output voltage

ripple while using the same amount of output capacitance, while the main purpose of interleaving technique is to further reduce or eliminate the output capacitance. However, multiphase interleaving suffers from similar problem of non-uniform output voltage ripple, which limits the effectiveness of interleaving. One of the future work directions of this thesis is to combine the sampling frequency and the multiphase interleaving technique to further optimize the output voltage ripple of a multiphase SC converter. Alternatively, the number of phases can be reduced while achieving the same output voltage ripple, which reduces the circuit complexity and implementation cost.

Power density, power efficiency and output voltage ripple are important considerations when designing power management circuits for portable electronic devices. This thesis has demonstrated the capability of SC DC-DC converters to achieve >80% power efficiency. Different output voltage ripple reduction techniques such as multi-phase interleaving and in-phase output voltage regulation have been proposed. However, achieving high power density and high power efficiency simultaneously is still a major challenge. While multiphase interleaving offers the opportunity to eliminate the bulky output capacitor, the flying capacitance must be further reduced in order for the SC DC-DC converter to be fully integrated without causing significant area overhead to the overall SoC. High on-chip capacitance density and high switching frequency are the keys to increase the power density. Today's on-chip SC DC-DC converters typically use MOScaps and MIM capacitors as the flying capacitors. MOPcaps usually possess the highest capacitance density in CMOS technologies, however, they also suffer most from the bottom plate parasitic capacitances [64]. Increasing the switching frequency

improves the power density, however, this also leads to increased switching losses due to both the bottom plate parasitic capacitance and the gate capacitance of the power switches. New technologies, such as deep trench capacitors, have enabled fully-integrated SC DC-DC converters that achieve 85% power efficiency while delivering 2.5 W/mm^2 output power [75]. However, in order to co-integrate the power management circuits with the functional blocks in low-cost CMOS technologies, circuit techniques, such as bottom-plate charge recycling, can be further investigated.

Chapter 6 demonstrates the feasibility of SC DC-DC converter for indoor PV energy harvesting systems. As we know from Chapter 2, switched-capacitor DC-DC converters are efficient only when the actual output voltage to input voltage ratio is close to the nominal no-load conversion ratios. Since the indoor lighting condition can be well defined, the V_{MPP} of the PV cell is relatively constant; hence the SC converter needs few gain settings to interface the PV cell under constant lighting condition. However, in order to extend the use of SC converters to more general outdoor PV harvesting and other types of energy harvesting systems, such as piezoelectric and thermal energy harvesting, switched-capacitor DC-DC converters with large number of gain configurations must be employed. However, to generate a large number of voltage conversion ratios, the number of flying capacitors, I/O pins and circuit complexity increases rapidly. To reduce the external components and number of I/O pins further necessitates integrating the flying capacitors. Switched-capacitor DC-DC converters with multiple phases of operation (not multiphase-interleaved SC converter), as exemplified in Section 2.1, is also a

promising solution to generate different voltage conversion ratios using less flying capacitors.

Publications

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- **Z. Xiao**, A. K. Bui, and L. Siek, "On-chip reconfigurable switched-capacitor DC-DC converter for indoor PV energy harvesting," *Electronics Letters*. Available: <http://digital-library.theiet.org/content/journals/10.1049/el.2016.3018>.
- **Z. Xiao**, A. K. Bui, and L. Siek, "A Switched-Capacitor DC-DC Converter with Embedded Fast NMOS-LDOs Achieving Low Noise, Low Output Voltage Ripple and Fast Response," in 15th Int. Symp. Integrated Circuits (ISIC), 2016.
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