Piezoelectric energy harvesting interface circuits for energy autonomous sensors

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**PIEZOELECTRIC ENERGY HARVESTING
INTERFACE CIRCUITS FOR ENERGY
AUTONOMOUS SENSORS**

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2017

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INTERFACE CIRCUITS FOR ENERGY
AUTONOMOUS SENSORS**

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**A thesis submitted to the Nanyang Technological
University in partial fulfilment of the requirement for
the degree of
Doctor of Philosophy**

2017

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

20/1/2017

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Date

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Arish Shareef Kootungal Paramba

Abstract

The Internet of Things (IoT) era has unlocked a new dimension for interconnected devices. Numerous sensors are being deployed around us for applications such as environmental, structural health and human health monitoring. These sensors are sometimes expected to work in a deploy-and-forget mode, in which accessing them for replacing their power source might not be a feasible option. Though energy harvesting has been in existence for a long time, it is only in the recent past that they have been increasingly applied for powering miniature sensor nodes, mainly due to the ultra-low power nature of the contemporary sensors.

Harvesting energy from ambient sources such as light, heat, motion and radio waves is an attractive alternative to perishable batteries. Though energy from light has the highest power density, the availability of the same cannot be guaranteed for all environments. Harvesting energy from motion, especially vibration, has garnered much research interest due to their ubiquitous nature. Vibrational energy is often harvested using three methods viz. Electromagnetic, Electrostatic and Piezoelectric, the latter being the focus of this thesis.

Harvesting vibrational energy using Piezoelectric Transducers (PET) is highly desirable owing to their higher power density amongst the three methods. However, in space-constrained designs, it becomes imperative to harvest the last bit of energy left in the tiny transducer. MEMS based transducers subjected to ambient vibrations typically produce low voltages, which are not efficiently harvested using conventional diode based rectifier circuits. Moreover, the voltage output of a PET is highly susceptible to the rapidly varying frequency of ambient vibrations, causing the voltage to drop during off-resonant conditions. Impedance matching is essential to maximize the power output from any energy source and performing the same in low power environments is a challenge due to the power overhead involved. Non-linear processing techniques have been proposed in the past, which

aim to enhance the power output from a PET. The work in thesis is based on Synchronous Electric Charge Extraction (SECE), which is one of the many non-linear techniques available.

This thesis introduces three rectifier-less topologies based on the SECE technique. The rectifier-less feature in all the three topologies is implemented using a bi-directional switching converter. The first topology is capable of harvesting energy from a single PET with a measured peak efficiency of 73 % in the input voltage range of 0.5 V – 1.75 V. The second topology achieves a peak efficiency of 80 % and targets the same voltage range, but combines multiple PET sources in an inductor-sharing configuration. The combination of multiple PETs operating at different resonant frequencies widens the operating frequency range of the Piezoelectric Energy Harvesting (PEH) system. The third topology has a slightly wider input voltage range of 1.1 – 3.5 V and achieves efficiencies up to 79 % in simulations.

Two complete PEH systems have been developed using the proposed rectifier-less, SECE topologies. The first PEH system is for a single PET, whereas the second is for multiple PETs. The efficacy of the multiple input PEH system is verified using three commercially available piezoelectric cantilevers. The PEH systems are implemented on a PCB using discrete components. Performance data from the PCB prototype demonstrate a peak power-conversion efficiency of 80 % in agreement with simulations. The PEH systems are self-powered, battery-less, and self-starting. The start-up circuit kick-starts the system from a zero-energy state with an input voltage of 650 mV. During the harvesting process, the control circuits consume an intrinsic power of 7 μ W at 2.7 V. In the absence of vibrations, the system draws a standby power of only 2.6 μ W at 2.7 V. In comparison to other state-of-the-art PEH systems, the proposed system achieves comparable or better power conversion efficiencies by using a small sized inductor.

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Abbreviations

AD	Active Diode
AVD	Active Voltage Doubler
BSC	Bi-directional Switching Converter
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductors
DBR	Diode Bridge Rectifier
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCP	Dickson Charge Pump
DCR	Direct Current Resistance
DLC	Digital Logic Controller
DLS	Dual Level Shifter
DSP	Digital Signal Processor
DSSC	Dye Sensitized Solar Cells
DSSH	Double Synchronized Switch Harvesting
ECM	Equivalent Circuit Model
EDLC	Electric Double Layer Capacitors
EMG	Electromagnetic Generators
ERI@N	Energy Research Institute @ NTU
FOCV	Fractional Open Circuit Voltage
FOM	Figure of Merit
GSM	Global System for Mobile Communications
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
JFET	Junction Field-effect Transistor

LDO	Low Dropout
LS	Level Shifter
LV	Low Voltage
MEMS	Micro-Electro-Mechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
N-Ch	N-Channel
NMOS	N-Channel Metal Oxide Semiconductor
NTU	Nanyang Technological University
NVC	Negative Voltage Converter
PCB	Printed Circuit Board
P-Ch	P-Channel
PEH	Piezoelectric Energy Harvesting
PET	Piezoelectric Transducer
PFM	Pulse Frequency Modulation
PKD	Peak Detection
PMOS	P-Channel Metal Oxide Semiconductor
P-SSHI	Parallel Synchronized Switch Harvesting on Inductor
PWM	Pulse Width Modulation
PZT	Lead Zirconate Titanate
RCI	Residual Charge Inversion
RF	Radio Frequency
RFID	Radio Frequency Identification
SECE	Synchronous Electric Charge Extraction
SoC	System on Chip
SOI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis

SR	Set-Reset
SSHI	Synchronized Switch Harvesting on Inductor
S-SSHI	Series Synchronized Switch Harvesting on Inductor
TEG	Thermoelectric Generators
UVLO	Under Voltage Lock Out
WSN	Wireless Sensor Network
ZCD	Zero Crossing Detection

Chapter 1

Introduction

This chapter provides an insight into the need for low power energy harvesting and the motivation for this research. Various transduction mechanisms used for energy harvesting are compared and the rationale for choosing a piezoelectric transducer is explained. The work undertaken aims to design a highly efficient interface circuit for piezoelectric transducers, addressing some of the existing limitations. A detailed list of original contributions of this thesis are presented at the end of the chapter.

1.1 Energy storage and Miniaturization

With integrated circuit technology rapidly moving towards low voltage process nodes, portable electronic products have experienced tremendous reduction in power consumption. The goal of miniaturization has been pursued rigorously in the past and the recent development of connected devices such as wearable electronics and smart sensors, collectively called Internet of Things (IoT) is an outcome of the

Figure 1.1 Human Health Monitoring Systems (a) Google's smart contact lens [7] (b) Psikick's heartrate monitor, powered by body heat [8].

same. With the onset of the IoT era, an ever increasing number of wireless sensors are deployed around us [1]. These sensors often form an interconnected network, transmit information remotely to a central unit and is referred to as a Wireless Sensor Network (WSN) [2]. A WSN is expected to function autonomously in a variety of scenarios such as environmental sensing [3], [4], structural health [5] and human health [6] monitoring systems. Figure 1.1(a) shows a smart contact lens prototype [7] from Google Inc., capable of monitoring and transmitting insulin level for diabetic patients and Figure 1.1(b) shows a heartrate monitoring device from Psikick [8] capable of operating from body heat. None of the devices were commercially available during the time this thesis was written. Presently a great

Figure 1.2 Comparison of various technology trends over the years [16]

number of the implantable devices [9], wearables and WSNs are powered using a conventional battery which limits their long-term use. The limited lifespan of batteries when compared to the much longer operational period of the sensor, calls for frequent battery replacements. As more of such sensors are deployed, accessing them individually for maintenance will be counter-productive and in some cases, prohibitive, for e.g. the surgical procedure required for a battery replacement in a pacemaker can lead to post-operative complications such as infections [10] and also cosmetic issues like scarring. Batteries that can last for the lifetime of the device being powered is therefore the ideal solution. However, upon inspecting the evolution of battery technology over the years (see Figure 1.2), one can observe that the improvement in energy density of batteries has been rather linear when compared to the exponential development of semiconductor technology, which is known to follow Moore's law. The longer lifespan of modern batteries can be attributed mainly to the lower power consumption of the semiconductor devices

Figure 1.3 A Ragone plot showing the power density vs. energy density of different energy storage technologies [42].

used rather than the battery technology itself. In addition to the energy density limitations already mentioned, batteries pose a challenge in the form of waste disposal [11]. Moreover, wireless sensors generally operate in burst mode during wireless transmission and consume high power, which is not easily provided by batteries. Electric Double Layer Capacitors (EDLC) or supercapacitors have power densities superior to and energy densities comparable to that of batteries, which can be observed from the Ragone plot shown in Figure 1.3. Supercapacitors tend to maintain their capacities even after 1,000,000 charge/discharge cycles [12], which is orders of magnitude higher than a lithium-ion battery having an average of 300 charge/discharge cycles, though higher self-discharge rate [13] of a super-capacitor is still a concern which needs to be addressed. Nevertheless, supercapacitors are a viable alternative to conventional batteries given the above benefits. To account for the lower energy density and higher self-discharge rate, supercapacitors are often used in conjunction with energy harvesting techniques. Though ubiquitous, the

intermittent nature of ambient energy sources is one of the main drawbacks which has limited their widespread use. However, since state-of-the-art wireless sensors draw power in the microwatts range [14], energy harvesting from ambient sources has become a viable option. These sensors remain in their idle or standby state up to 99% of their operational lifetime [15] and enter active mode of operation only when the storage element has accumulated sufficient energy for a ‘measure-and-transmit’ event.

1.2 Energy Harvesting and its applications

Energy harvesting refers to the tapping of ambient energy present in the environment. The process of harvesting energy from the environment has been in existence for a long time, dating back to the use of the ancient water wheel [16] and the more recent solar panels. Majority of the research in the past has focused on harnessing energy from renewable sources such as solar, wind and geothermal for powering medium-high power applications which are important for achieving a lower carbon footprint. However, it is only recently that energy harvesting has been increasingly applied for powering ultra-low power devices such as wireless sensors and wearables [17] which consume power in the range of microwatts to milliwatts. Energy harvesting techniques combined with supercapacitor technology can greatly reduce the solution size of WSNs. The increased power density of supercapacitors provides the power needed for wireless transmissions and their lower energy density can be compensated by harvesting from ambient sources of energy. Light, heat, motion and Radio Frequency (RF) are the most commonly harvested sources of energy in the microwatts-milliwatts power range [18]. A comparison between the various sources of energy is given in Table 1.1, where it can be observed that out of the four ambient sources mentioned, the energy obtained from light and heat has the highest power density, in outdoor and industrial conditions respectively,

Table 1.1 Power Density of commonly harvested sources of energy

SOURCE	SOURCE POWER	HARVESTED POWER
Ambient Light		
Indoor	0.1 mW/cm ²	10 μW/cm ²
Outdoor	100 mW/cm ²	10 mW/cm ²
Vibration/Motion		
Human	0.5 m/s ² at 1 Hz	4 μW/cm ²
	1.0 m/s ² at 50 Hz	
Industrial	1.0 m/s ² at 5 Hz	100 μW/cm ²
	10 m/s ² at 1 kHz	
Thermal energy		
Human	20 mW/ cm ²	30 μW/cm ²
Industrial	100 mW/cm ²	1 – 10 mW/cm ²
Radio Frequency		
GSM Base Station	0.3 μW/cm ²	0.1 μW/cm ²

Adapted from [18]

followed by motion and RF. An overview of the above-mentioned sources of energy i.e. light, heat, motion and RF is provided in the following section.

- **Light:** Till date, light energy harvesting remains to be the most popular method of energy harvesting owing to its high energy density. Photovoltaic cells made of monocrystalline and polycrystalline silicon are widely used for light energy harvesting owing to their high efficiency. More recently, Dye Sensitized Solar Cells (DSSC) [19] have emerged which use a process similar to photosynthesis, however, the efficiency of the same is still far behind [20] that of its silicon counterparts. The photovoltaic cell has an optimal point in its I-V characteristic, where it provides the highest power output, referred to as the Maximum Power Point (MPP) and is dependent on both the temperature and illuminance. The power output of solar cells can drop considerably if operated away from their MPP. This could happen under indoor conditions where there is comparatively

less amount of light falling on the photovoltaic cell. Care should be taken during installation to ensure that the solar cells receive enough illumination [21] even when indoors. In order to operate at their MPP, energy harvesting circuits are often equipped with a Maximum Power Point Tracking (MPPT) circuit [22]–[24] which keep track of the MPP and maximize power. Despite the power overhead incurred, MPPT circuits have become an indispensable building block when designing circuits which harvest light energy.

- **Heat:** ‘Seebeck Effect’ is the phenomenon in which a temperature gradient between two metals or semiconductor produces a voltage difference between them. This voltage difference causes a current flow when an external load is connected across them. Thermoelectric Generators (TEG) use the heat flow from a hot to cold surface to drive current through the external load [25]. The voltage V generated by the TEG due to the temperature difference T across its plates is given by $V = \alpha \Delta T$, where α is the ‘Seebeck coefficient’. The Figure of Merit (FOM), ‘ zT ’ of a TEG is given by $\alpha^2 T / \rho \kappa$, where ρ is the electrical resistivity and κ is the thermal conductivity. From the definition of the FOM we understand that a good TEG should have low electrical resistivity and low thermal conductivity, which is a challenging requirement since majority of the good conductors of electricity are good conductors of heat as well. Due to this contradictory requirement, TEG material research is challenging [26]. The electrical model of a TEG consists of a DC voltage source in series with a resistance. Impedance matching techniques similar to photovoltaic cells need to be applied to harvest maximum power from TEGs [27]. Furthermore, in order to maintain the temperature difference, heat should be continuously removed from the cold side using a heat sink [28]. This requirement increases the size of a TEG, which is not desirable for volume constrained solutions. Nevertheless,

solid-state TEGs have been employed successfully in the past to power space missions [25] like the *Voyager*.

- **Radio Frequency:** Despite the fact that RF energy harvesting provides the lowest power density when compared to other harvesting methods, there is growing research interest around the topic due to the widespread availability of Wi-Fi hotspots and GSM towers around us. Antenna design in an RF energy harvester is as important as the power conversion circuit [29] itself. RF energy harvesting from a short range has already been successfully applied to passive RFID tags [30] using power transmitted from the reader unit, though far field [31] RF energy harvesting is still evolving.

- **Motion:** The main advantage of harvesting energy from motion is its omnipresent nature, for e.g. vibrational motion of industrial machines and automobiles, walking, flexing of muscles [32] and even pumping of the heart [33], [34]. Vibrational energy can be harvested using three mechanisms [35] viz. electrostatic, electromagnetic and piezoelectric, the latter being the focus area of this thesis.

Electrostatic harvesters use a capacitor having a movable plate set in motion by external vibrations. There are two modes of operation for electrostatic harvesters i.e. charge constrained case and voltage constrained case. When the charge is constrained in the capacitor, C and the plate distance increases due to the vibration, there is a reduction in the capacitance and increase in the voltage, V . The net energy stored in the capacitor increases according to $E = 1/2 CV^2$. The voltage increase due to the charge constrained case makes it less compatible with standard CMOS processes and calls for high voltage options [36] or other special processes like Silicon on Insulator (SOI) which drives up the cost [37]. On the other hand, in the voltage constrained case, the net energy

flows out of the electrostatic harvester as a current. However, constraining the voltage needs an initial voltage even before the harvesting starts, which discourages zero energy/battery-less start-up.

Electromagnetic Generators (EMG) use the principle of electromagnetic induction to generate power. The principle of electromagnetic induction has been used extensively in dynamos for large scale power generation. However, in the realm of energy harvesting, EMGs use vibrational motion instead of rotational motion. Due to the large number of turns required, the volume occupied by EMG is considerably large compared to other motion based transducers. When the size is confined to an acceptable limit, their open circuit voltages drastically reduce to the range of few hundred millivolts or less. Hence in most cases voltage boosting techniques [38], [39] are required to provide the load with an acceptable voltage level.

In the work presented in this thesis, vibrational energy is harvested using piezoelectric transducers (PETs) and the same is discussed below.

1.3 Rationale for choosing Piezoelectric Transducer

The piezoelectric effect is the phenomenon in which certain materials develop electric charge within them when strained due to an external force. The charge developed is extracted out from the surface of the material using electrodes and used for powering low power devices and also for sensing. Another phenomenon called the inverse piezoelectric effect exists in which a voltage supplied to the material causes it to strain. The inverse piezoelectric effect is often used in the production of ultrasonic waves and actuation. Lead Zirconate Titanate abbreviated as PZT is widely used for energy harvesting applications and is the constituent of the transducer used in this thesis. The underlying theory of the transduction process is not discussed here, but has been extensively reviewed in [40]. There is an ever-increasing interest in developing energy harvesting interface circuits exploiting the

Figure 1.4 Plot showing the Power density of various energy source vs their respective voltage outputs.

Piezoelectric effect. This could be mainly attributed to the relatively high power density of PETs compared to other transducers targeting kinetic energy which can be seen in Figure 1.4. The power density of EMGs can also be seen overlapping with PETs, however, due to low output voltages and the challenges involved in miniaturization, PETs are preferred. PETs are also compatible with MEMS process [41] which helps to shrink their size further.

1.4 Motivation

Prima facie piezoelectric transducers (PET) seem to be an attractive option for micro-power harvesting. However, they come with a few limitations. Unlike other sources of energy, PETs have a dependence on the frequency of mechanical vibration. There is a particular frequency at which PETs deliver the highest output power, called the resonant frequency, and the same depends upon the structure of the PET. Ambient vibrations are known to vary in amplitude and frequency over

time (aperiodic), and any deviation from their resonant frequency can significantly affect the power output of the PET. At resonance, macroscale PETs are known to produce voltages in the order of tens of volts, whereas microscale MEMS-based PETs often produce voltages ranging from a few hundred millivolts to a few volts. Under off-resonant conditions, the above voltages are expected to drop further for macroscale and microscale PETs alike. Moreover, a harvesting system capable of generating power at a unique frequency alone is not very meaningful. Device fabricators are in efforts to broaden the harvestable frequency range through smart structural and material modifications. There are very few works in literature which have focused on this problem from a circuit design perspective, and there is immense scope for advancement. Since voltage output of PETs decreases during off-resonant conditions, it is highly desirable to have an energy harvesting circuit providing high efficiency at low voltage levels.

1.5 Contribution of the Thesis

The work undertaken as part of this Ph.D. programme attempts to bridge the gap between existing piezoelectric energy harvesting systems and a system capable of scavenging vibrational energy under realistic environmental conditions. This thesis introduces a series of circuit design improvements for achieving high efficiency at low voltages and for broadening the frequency range of operation. Some of the major contributions of this work are listed below:

- A circuit implementation of a rectifier-free piezoelectric energy harvesting system which is self-powered, self-starting and suitable for PETs which generate low voltages, when operating under off-resonant conditions. The low voltage compatibility is achieved through a bi-directional switching converter.
- A circuit implementation of an energy harvesting system which is capable of harvesting energy from multiple low voltage PETs. The low voltage compatibility is achieved using a bi-directional power converter different from

the above, due to limitations in handling multiple PETs in the former design . The converter here uses a new topology and gate driver design to cater to multiple PETs. The proposed topology uses a single inductor shared among multiple PETs, which reduces the solution size significantly. Since the multiple PETs are tuned to different resonant frequencies, the operational bandwidth of the system is widened. Besides, the self-powered, self-starting features of the single PET version are preserved.

- A new topology for a rectifier-free, piezoelectric energy harvesting system capable of harvesting energy from a wider input voltage range compared to the above two topologies. The proposed solution uses a new design of a bi-directional converter. The functionality and efficiency of the converter are validated through circuit simulations.
- The trade-offs considered as part of the device selection process has enabled an ultra-low power design which will be discussed in detail. It will serve as a general guideline for designing ultra-low-power control circuits for energy harvesting systems.

1.6 Organization of the Thesis

Following the introduction provided here, a comprehensive literature review of existing piezoelectric energy harvesting techniques will be presented in Chapter 2. The motivation for selecting Synchronous Electric Charge Extraction (SECE) as the technique of choice in this thesis will be provided in the context of existing literature. Chapter 3 will present first of the three topologies providing a rectifier-free operation for single low-voltage PETs. The trade-offs considered as part of the component selection process will be discussed in detail followed by functional simulation of the sub-circuits. Finally, the design will be validated experimentally using a commercially available piezoelectric transducer. In Chapter 4, a rectifier-free topology targeting multiple PETs will be presented. Since the topology utilizes

certain sub-circuits from its single-PET version, only the sub-circuits which are different from the previous topology will be discussed in detail. Simulations will be performed to validate the effectiveness of the topology and the functionality of its sub-circuits. Experimental results showing the multi-PET capability of the system will be provided at the end. Chapter 5 will present the third rectifier-free topology targeting medium-voltage PETs. The challenges involved in the implementation of the sub-circuit blocks will be discussed and guidelines for implementing the same will be provided. Finally, the efficacy of the topology will be validated through simulations. Chapter 6 will draw the conclusion by emphasizing the achievements of the present work and will provide possible means of improving the designs further.

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Chapter 2

Literature Review

This chapter aims to provide a comprehensive overview of the prior arts and the state-of-the-art in piezoelectric energy harvesting. Various interface circuits used for harvesting energy from piezoelectric transducers are reviewed, highlighting the advantages and disadvantages of each technique. Finally, the desirable features of an energy harvesting system are examined, which is particularly useful when conceptualizing an improved design, addressing some of the drawbacks associated with the state-of-the-art circuits.

2.1 Equivalent Circuit Model of a Piezoelectric Transducer

The piezoelectric principle and materials used were introduced in section 1.3. Before delving into the literature on interface circuits for piezoelectric energy harvesting, the Equivalent Circuit Model (ECM) of a PET is briefly presented here. There are two configurations [1] in which a PET can be attached to the host structure – (i) surface mount and (ii) base excited as shown in Figure 2.1. The effect of the harvesting techniques on each configuration is different. Since in this thesis the base excited (cantilever) configuration is used, only the literature related to those will be reviewed.

Figure 2.1 A piezoelectric patch (a) directly attached to a host structure (b) mounted on a cantilever beam. The former relies on surface deformation and the latter relies on the base movement of the host structure.

A piezoelectric transducer is an electromechanical device having an electrical as well as a mechanical domain. A PET vibrating in a cantilever configuration (see Figure 2.2(a)) when subjected to an external force, F , is often modelled as a second-order Mass-Spring-Damper system as shown in Figure 2.2(b). The internal forces consist of a restoring force, F_e due to the piezoelectric element, restoring force due

Figure 2.2 (a) Structure of a piezoelectric cantilever beam with an attached tip mass (b) Second-Order Mass-Spring-Damper model of a piezoelectric bimorph in a cantilever configuration.

Figure 2.3 Coupled Equivalent Circuit Model [51] of a Piezoelectric Transducer vibrating in a cantilever configuration. The equivalent parameters in the mass- spring-damper model are listed on the right side.

to the stiffness of the spring and viscous force of the damper. u represents displacement of the mass, whereas structural stiffness of the system is represented by k , and mechanical losses are represented by d . The work done by the mass, m against F_e is converted into electrical energy and V_P is the voltage produced across the piezoelectric transducer. The ECM of the Mass-Spring-Damper system is shown in Figure 2.3. The inductance L_m represents the dynamic mass (m), resistance

Figure 2.4 Uncoupled (a) Thevenin and (b) Norton Equivalent Circuit Model of a Piezoelectric Transducer vibrating in a cantilever configuration.

R_m represents the mechanical damping (d) and C_m represents the compliance ($1/k$). Compliance is the inverse of stiffness and refers to the ease with which a body deforms. C_{PET} and R_{PET} are the intrinsic piezoelectric capacitance and resistance. R_{PET} is a large value and is often ignored. α is the electromechanical coupling factor, which determines the amount of mechanical energy converted into electrical energy. The dependent current source, αI_m represents the piezoelectric current flowing in the electrical domain. The dependent voltage source, αV_P represents the inverse piezoelectric effect or the backward coupling, which acts against V_m and damps the vibrational motion of the mass and is called electrically induced damping. For a given mechanical damping, the maximum power is harvested when the mechanical damping is equal to the electrically induced damping. A simplified, uncoupled ECM of a PET is widely used for circuit simulation and is shown in Figure 2.4, V_{OC} is the open circuit voltage. The Thevenin ECM is used in this thesis for verification of the various topologies presented.

It is known from maximum power transfer theorem that a voltage source V_s with an internal complex impedance of Z_s transfers maximum power to a load Z_L , when $Z_s = Z_L^*$, where Z_L^* represents the complex conjugate impedance. Similarly, to match the complex impedance of the PET, which is predominantly capacitive,

Figure 2.5 (a) Schematic showing the Diode Bridge Rectifier charging an RC load (b) Capacitor charging waveform. The maximum achievable voltage at the output is $V_{IN} - 2V_F$.

Henries of inductance would be needed [2] at low frequencies (typical of ambient vibrations). Since using a large inductor would be prohibitive in a miniaturized system, research has focused on using sub-optimal impedance matching and other non-linear techniques which will be discussed in the following section.

2.2 Interface circuits for piezoelectric energy harvesting

Conventionally, research focus has been on the structural design of PETs for improving the power output, with little emphasis on the interface circuit. It was only in the past decade that the focus shifted to improving the efficiency of the interface circuit, which provides the necessary power conversion for the load electronics. Unlike photovoltaic and thermoelectric generators, motion based transducers like PETs mandate an additional AC-DC rectification stage due to the alternating nature of the source. The requirement of an additional rectification stage contributes to efficiency loss in the interface circuit; the extent of which depends on the rectification technique pursued. Numerous interface circuits have been proposed for harvesting energy from PETs, the most basic one being the Diode Bridge Rectifier (DBR). If one observes the charging waveform (see Figure 2.5(b))

of a capacitor connected to a DBR circuit (see Figure 2.5(a)), it can be understood that the simplicity advantage associated with the circuit diminishes when the load voltage approaches the PET's output voltage. The DBR circuit is commonly used for benchmarking the power gain achieved by newly reported interface circuits.

Interface circuits used for PETs can be widely classified into three categories, though this classification is not strict by any means. The first group of interface circuits strives to improve the efficiency of the rectifier block by using methods to mitigate the forward voltage drop associated with the diode. The inherent limitation of the DBR circuit i.e. output voltage cannot surpass the input, is applicable to this group as well. The second group of circuits tries to overcome the limitations of a DBR circuit, by employing a switching converter across the energy storage element. The switching converter provides a matched impedance to the PET and optimizes the power flow. The third category of circuits uses non-linear techniques which exploit the predominantly capacitive nature of the PETs for enhancing the energy extraction. Compared to the previous categories of interface circuits, the third group can harvest a significant portion of the available energy. The literature on interface circuits reviewed here is exclusively on piezoelectric energy harvesting, though some circuits could function with other kinds of vibration based transducers as well. The focus of this literature review is to highlight the various techniques employed and covers both discrete and integrated implementations.

2.2.1 Interface circuits based on variants of the conventional diode

Early interface circuits used conventional Schottky diodes with a low forward voltage drop for the purpose of AC-DC conversion and were often employed in discrete circuits. Schottky diodes with low forward voltage drops have high reverse leakage current, which is not desirable due to the rapid discharge of the storage element. Moreover, in an integrated circuit implementation, fabrication of the

Figure 2.6 Schematic of the AVD circuit. The comparators CMP_1 and CMP_2 drive the MOSFET MN_1 and MP_1 , respectively based on the voltage across the MOSFETs.

Schottky diode in a CMOS process raises the production costs [3], [4]. Le *et al.* in [5] introduced an Active Voltage Doubler (AVD) circuit, which replaced the passive diodes with a MOSFET, drastically reducing the voltage drop. It was found that with the Active Diodes (AD), the peak efficiency of the circuit was 37% higher than its passive counterpart. However, the reported efficiency was with the comparator powered externally. In [6], Dallago *et al.* demonstrated a self-powered AVD circuit in which the control circuits drew a quiescent current of only 500 nA while the ADs achieved efficiencies greater than 90% for a wide range of load values. The design used a supply independent bias circuit for powering the control circuits which helped achieve the higher efficiency reported. The schematic of an AVD circuit is shown in Figure 2.6. Marinkovic *et al.* in [7] presented an AVD circuit which used a trigger circuit instead of a continuous time comparator, reducing the power drawn during standby. An additional diode connected PMOS transistor was used to expedite the start-up process. In [8], the authors demonstrated a floating gate technique to reduce the threshold voltage of the MOSFETs used in the AD. The authors in [9] presented an AD bridge rectifier circuit, replacing all four passive diodes with ADs. The design is self-powered and reported a peak power efficiency of 90% with a lower voltage drop across the ADs.

Figure 2.7 Schematic of the NVC. An AD comprising of a P-Ch MOSFET and a comparator is used at the output for blocking reverse current from the capacitor.

Compared to previously reported AD implementations, the control circuits draw power from the PET, rather than the energy storage, which ensured that the control circuits do not draw power during standby. More recently, Liempd *et al.* [10] reported an AD bridge rectifier within a System on Chip (SoC). The rectifier achieved a peak power conversion efficiency of 94% and could work with input power in the range of 1 μ W to 1 mW.

A Negative Voltage Converter (NVC) circuit, shown in Figure 2.7, originally used for rectification in RFID-based power circuits [11], has been widely used in many PEH applications, due to its simple structure. MOSFET pairs $MP_1 - MN_1$ and $MP_2 - MN_2$ turn on during positive and negative half-cycles, respectively. The MOSFETs are turned on by the input voltage and do not need sophisticated comparators. During conduction, the circuit exhibits only $2V_{DS}$ drop at the output, where V_{DS} is the drain to source voltage when the transistor is turned on. However, the MOSFETs need at least one threshold voltage, V_{TH} at the input to turn on. The NVC is incapable of blocking reverse current from the output capacitor. For the same reason, the authors in [12] used an additional second stage consisting of an

Figure 2.8 Simplified block diagram of a switched converter based on a Perturb and Observe MPPT scheme. PWM and PFM stands for Pulse Width Modulation and Pulse Frequency Modulation, respectively.

AD (see Figure 2.7). The measured voltage efficiency exceeded over 90% for a wide input voltage range, indicating the effectiveness of the NVC circuit.

2.2.2 Interface circuits based on a switching converter

The AD-based circuits, except the AVD, have an inherent limitation of not being able to charge the storage element beyond the maximum input voltage. To bypass this limitation, switched DC-DC power converters are used as a second stage, to regulate the voltage across the output of the rectifier, V_{RECT} . This ensures continuous outflow of power from the PET into the final storage element. The regulation of V_{RECT} is done in such a way that maximum power flows into the power converter.

Ottman *et al.* applied the dynamic resistive impedance matching principle to PETs in [13] and used a buck converter to regulate the voltage across C_{RECT} as shown in Figure 2.8. The system used an externally powered DSP to implement the duty cycle control of the converter, by measuring the current flowing into the battery. The system effectively maintains the V_{RECT} at $V_{oc}/2$ which coincides with maximum power transfer. A modified version of [13] which used a buck converter in Discontinuous Conduction Mode (DCM) was implemented in [14] by the same authors. The new design used a fixed duty cycle mode when the input voltage

crossed a predefined threshold, reducing the complexity of the control circuit and hence reducing the power overhead. While [13] harvested 400% more power compared to a DBR, [14] harvested only 325% more, but facilitated a self-powered operation. Lefeuvre *et al.* designed a sensor-less buck-boost converter [15] based on the resistive impedance matching principle. The drawback of the circuit was that prior knowledge of the source resistance was required for designing the converter, which removes the flexibility in the circuit. In [16], Tabesh *et al.* reported a PEH system based on a voltage doubler with an adaptive MPPT circuit. The circuit indirectly tracked the V_{OC} of the PET using an analog controller without using a current sensor, which helped to lower the power consumption. In [17] Kong *et al.* demonstrated a self-powered, self-starting, dynamic impedance matching, discrete interface circuit capable of adjusting its impedance over a range of values around the resonant frequency. A microcontroller onboard implemented the Hill Climbing algorithm (a.k.a. perturb and observe) to track the MPPT and the inbuilt ADC sensed the current using a sense resistor. Sankman *et al.* [18] reported an integrated version of a PEH using resistive impedance matching which consumed 450 nA of quiescent current with a peak efficiency of 79 %. The design features an on-chip adaptive impedance matching circuit for tracking the MPP by maximizing the current into the boost converter. The current is measured using a current sense resistor and a differential amplifier, whereas the boost converter is controlled using an adaptive pulse skipping controller. Gao *et al.* [19] used an NVC rectifier in combination with a reconfigurable boost/buck-boost converter to aid system start-up from an input voltage as low as 0.3 V. A body-bias control was used to lower the V_{TH} of the MOSFETs used. The peak rectifier efficiency was 98%, however, the overall power efficiency was only 70%, losing much of the power to the reconfigurable converter. In [20], Darmayuda *et al.* presented an interface circuit based on a buck-boost converter with the NVC as the first stage. The diode needed for blocking reverse current, generally present immediately after the NVC, was

Figure 2.9 Simplified block diagram of a switched converter based on Fractional Open Circuit Voltage MPPT scheme. The switch S is opened for a brief period to sense the V_{OC} of the PET.

merged into the buck-boost converter to reduce diode drop. Moreover, the intermediate capacitor was removed reducing component count. It has to be noted that the circuits in [19] and [20] do not offer dynamic impedance matching. In [21], Lu *et al.* incorporated a low power, Fractional Open Circuit Voltage (FOCV) based MPPT circuit into the PEH to track the MPP. A simplified block diagram of an FOCV based MPPT converter is shown in Figure 2.9. The control circuit disconnects the PET from the rest of the circuit for a brief period (2 cycles) when the vibration tracking unit tracks the V_{OC} . The circuit efficiency was above 90% and the control circuit consumed ultra-low power which made it suitable for micropower operation. Although the MPPT circuit presented in [21] is suitable for slowly varying signals, it might not be a good fit for rapidly varying vibrations which are more predominant in the environment. Shim *et al.* later introduced the faster ‘one cycle MPPT’ circuit in [22], however, for rapid changes in the vibration profile, the circuit still faces limitations.

2.2.3 Interface circuits based on non-linear processing techniques

Figure 2.10 Schematic of (a) Synchronous Switched Harvesting on Inductor circuit and (b) Synchronous Electric Charge Extraction circuit

All the methods discussed thus far do not alter the shape of the voltage waveform significantly and can be considered linear. The methods discussed below take into account the predominantly capacitive nature of PETs and modify the voltage wave shape by using either a switch or a switch-inductor pair. Non-linear techniques try to harvest more energy which is closer to the theoretical limit achieved through a complex conjugate matching technique. The non-linear processing techniques applied to energy harvesting were originally developed for the problem of vibration damping in mechanical structures by Richard *et al.* in [23], [24]. The most popular among the non-linear techniques are Synchronized Switch Harvesting on Inductor (SSHI) [25] and Synchronous Electric Charge Extraction (SECE) [26]. There are numerous other techniques which have sprouted from the former two techniques and have focused on either impedance matching [27] or energy enhancement [28]. The characteristics of most non-linear techniques have been extensively reviewed in [29], by Guyomar *et al.*

The basic principle behind the SSHI technique is to invert the voltage across the intrinsic piezo capacitance, C_{PET} by forming an LC tank circuit with an external inductor, L . The SSHI circuit is shown in Figure 2.10(a). A switch, S connects C_{PET} to L at the extremum (positive and negative peak) of the alternating voltage for a short period of time, t_{SSH} given by (2.1).

$$t_{SSH} = \pi \sqrt{LC_{PET}} \quad (2.1)$$

Figure 2.11 (a) Simulated voltage and current waveforms of (a) an SSHI circuit (b) an SECE circuit.

t_{SSH} is half of the LC oscillation period of the tank circuit and is also the time required for C_{PET} to discharge into L and to recharge itself in the opposite direction (voltage reversal). This quasi-instantaneous phase reversal of the voltage sets the current flow (velocity) and voltage (force) of the PET in phase and enhances the power delivered to the load. Characteristic waveforms of an SSHI circuit fed with a V_{OC} of 1 V is shown in Figure 2.11(a). The figure shows the V_{OC} , the input waveform during the SSHI process (V_{SSH}) and the associated inductor current, i_L .

Differently, in the SECE technique, S is closed for a short duration, t_{SECE} , given by (2.2) which is equal to one quarter of the LC oscillation period.

$$t_{SECE} = \left(\frac{\pi}{2}\right) \sqrt{LC_{PET}} \quad (2.2)$$

The SECE circuit is shown in Figure 2.10(b). The closing of the switch, S causes the voltage across the PET to fall to zero, the current in the inductor to peak. At this

instance S is opened and the falling inductor current is discharged into the external load. Characteristic waveforms of an SECE circuit fed with a VOC of 1 V is shown in Figure 2.11(b). The figure shows the VOC, the input waveform during the SECE process (VSECE) and the associated inductor current, i_L . The characteristic voltage doubling associated with SECE can be observed, which is an indication of the higher amount of energy extracted from the PET.

The initial SSHI based interface circuits developed by Lefeuvre *et al.* [30] were not self-powered and required external displacement sensors to monitor the displacement peaks. A self-powered SSHI technique was presented by Liang *et al.* in [31], however the power output was significantly less compared to the theoretical predictions. In [32], Ramadass *et al.* developed an integrated solution based on the SSHI technique which used a time multiplexed inductor for a buck, a boost and a bias-flipping stage. The DC-DC buck converter achieved a peak efficiency of 85% and delivered power to a 1.8 V rechargeable battery at the output. Few of the drawbacks associated with this design were the lack of a start-up circuit and battery-free operation. Also, the timing of the bias-flip stage had to be administered externally, which shunned autonomous operation. Krihely *et al.* [33] presented a discrete, self-powered, SSHI interface circuit which consumed a quiescent current of 4 μA and harvested 2.3x times power compared to a DBR circuit. Improving the design in [33] further, Shaohua *et al.* [34] developed a self-powered SSHI circuit for the micropower range which used a simple and efficient strategy to control the timing of the switch, which lead to a power gain of 5.8x compared to a DBR circuit.

Different from previous implementations, an AD-based switch-only interface circuit was designed by Sun *et al.* in [35] which did not employ an inductor. The removal of the inductor does reduce the amount of energy extracted from the PET but is suitable for applications where volume is a constraint. Do *et al.* [36] improved the former switch-only technique by adding an adaptive timing control

for the switch. Aktakka *et al.* [37] demonstrated an integrated system combining a custom fabricated MEMS-based PET and an integrated CMOS-based PEH system using the SSHI technique. Besides being self-powered, the system could start up from an initially depleted storage source with an input vibration of 0.1g ($1\text{ g} = 9.8\text{ m/s}^2$) in amplitude. Du *et al.* [38] developed an SSHI interface circuit, which addresses some of the start-up issues associated with the technique and introduced design optimizations to harvest from low voltages. Lastly, Sanchez *et al.* [39] introduced an SSHI interface circuit which could harvest from periodic and shock vibrations efficiently. In addition to an NVC, the PEH also incorporates an impedance matching buck converter, leading to an improvement of 6.8x compared to a DBR circuit. The inductor is shared between the bias-flip stage and the buck converter, leading to a reduced form factor. The design also incorporates a Low Dropout Regulator (LDO) on-chip, to provide a stable 2.5 V output to the load.

Synchronous Electric Charge Extraction was experimentally demonstrated for the first time by Lefeuvre *et al.* in [26]. However, the control circuits used external sensors for peak detection, which were not self-powered. Xu *et al.* [40] developed an integrated interface circuit based on SECE which achieved a peak efficiency of 70%. The input rectifier circuit used two bridge rectifiers suitable for operation with high and low voltages, which occupied the largest area on the chip. The design did not provide battery-less operation, and hence the start-up issue was not addressed. Kwon *et al.* [41] developed a rectifier-free, SECE circuit which could harvest from input voltage as low as 0.35 V with a peak power conversion efficiency of 50%. The timing for controlling the switches need to be set externally and the design required an external negative supply, giving away autonomy. Also, the lack of a start-up circuit limited its practical use. Tan *et al.* [42] reported a discrete implementation based on SECE using a flyback transformer with a peak efficiency of 63.3%. The maximum power output of the circuit was 5.6 mW, with the control circuits consuming 300 μW @ 5V, which is suitable only for operation

in the milliwatts range.

In [43], Hehn *et al.* presented a modified version of SECE which reduced the effect of parasitic resistance on the efficiency. The modified technique allowed them to use smaller inductors compared to previously used methods and still achieve a high-power efficiency of 85%. The design was also notable due to the presence of a start-up circuit and self-powered operation. Gasnier *et al.* designed an SECE circuit for harvesting energy from high voltage PETs > 100 V, by using a step-down transformer. The circuit used a multi-shot technique which supports the use of a smaller inductor for efficient energy transfer to the load. However, the optimum number of shots required for the transfer had to be set externally, and hence, the circuit was not completely autonomous. Romani *et al.* [44] presented a discrete, SECE based topology capable of harvesting energy from multiple PETs. Multiple PETs allowed the broadening of the harvestable frequency range. The design was scalable and achieved a peak efficiency of 74% for the input voltage up to 20 V. The design applied aggressive micropower design optimization to limit quiescent power consumption to $10 \mu\text{W}$ per source. However, the design used a microcontroller unit and needed to be reprogrammed with the t_{SECE} values for different L - C_{PET} combinations. Dini *et al.* [45] demonstrated an SECE based circuit with residual charge inversion (RCI). The RCI method used an additional smaller inductor to flip the charge left in C_{PET} . The charge left in C_{PET} is due to the incapability of an NVC circuit to conduct below V_{TH} . The SECE, RCI combination is particularly useful in improving power efficiency of low voltage PETs.

2.3 Broadband Energy Harvesting

Most of the works discussed so far have focused on improving the efficiency of the power transfer from the PET to the load, neglecting the fact that PETs working in cantilever configuration can only provide the highest possible power when operating at its resonant or natural frequency. Ambient vibrations are aperiodic

Figure 2.12 Power vs frequency plot of three individual PETs (b) Power vs frequency plot of three PETs combined. The bandwidth improvement is visible in the latter.

which negatively impacts the power output of a PET. Figure 2.12(a) shows the power vs frequency relationship of three PETs operating at different resonant frequencies. To broaden the frequency range of the PETs, various methods are in use for e.g. resonance tuning, multimodal harvesting, frequency up-conversion and non-linear oscillations [46]. Out of the aforementioned methods, multimodal energy harvesting is the easiest to implement with no continuous resonance tuning needed. The broadening of the operational bandwidth of three-PET system can be seen in Figure 2.12(b). In [47], Liu *et al.* demonstrated a MEMS prototype of an array of PETs. Multiple groups of cantilevers were fabricated with varying resonant frequencies, which achieved a broadband operation. The mathematical model and design procedure for such a wide band system was presented by Shahruz *et al.* in [48]. One drawback for the multimodal technique is that energy storage policy [46] needs to be optimized when multiple sources are present. To that extent, the authors in [44], [49] presented an SECE based, multiple PET technique to harvest the peak energy from each transducer.

2.4 Rationale for choosing SECE

Synchronous Electric Charge Extraction has been selected as the technique of choice in this thesis to implement a PEH system. Although the working of the

SECE technique was introduced in section 2.2.3, the rationale needs further explanation and is elaborated here. SSHI technique yields high output power compared to SECE, but the efficiency of the process is highly affected by the variation of the output capacitor's voltage. There is a particular load voltage at which the SSHI technique achieves the highest efficiency and needs impedance matching [39]. Compared to SSHI, the inductor in an SECE circuit acts as an intermediate storage bank which isolates the PET from the load. This gives the technique a unique advantage of being immune to the output load voltage variations [26], which removes the need for complex impedance matching or MPPT circuits. SECE inherently works at its optimum power point, lowering the control circuit power consumption and increasing the power delivered to the load. Also, it was shown by Lefeuvre *et al.* in [50] that SECE is suitable for random vibrations which are more predominant in nature. Moreover, since a PET utilizes the inductor for a brief period of time, the same inductor can be shared among multiple PETs facilitating a broadband operation with a reduced form factor.

2.5 Desirable features of a PEH system

In this section, the desirable characteristics of an interface circuit are chalked out from the study of prior arts and the state-of-the-art PEH systems. The features are listed below:

- **High efficiency operation:** The amount of energy available from ambient vibrations is limited and since WSNs generally operate in volume constrained environments, it becomes imperative that an interface circuit be highly efficient and capable of extracting the maximum energy from the source. This implies that control circuits should draw only a small portion of the harvested energy (quiescent power) while employing maximum power point schemes. Though ubiquitous, ambient vibrations are highly unpredictable. During periods of inactivity, it is required that the PEH system consumes minimal

standby power. This ensures that the load does not run out of power during normal operation.

- **Autonomous operation:** Energy harvesting is often applied in situations where the system is inaccessible for maintenance. Under such conditions, feeding signals or power externally is not a viable option and the PEH system should work reliably from the harvested energy and without external intervention. Moreover, removal of batteries from wireless sensor nodes helps to save maintenance costs, mitigate waste disposal issues and reduce the solution size. Supercapacitors are a good alternative as discussed in Chapter 1. However, using a supercapacitor adds an additional requirement of zero-energy start-up. The SECE technique requires the control circuits to be powered first in order to harvest energy.
- **Broadband operation:** An interface circuit operating at a particular frequency is not of much practical significance. The circuit should be capable of operating from a wide range of frequencies with acceptable power consumption. This requirement is of utmost importance when multiple PETs with different resonant frequencies are interfaced with the PEH system. An additional requirement which emerges from broadband operation is the ability of the system to have high efficiency at low voltages. PETs under off-resonant conditions produce significantly low voltages which can affect the efficiency of power conversion. Under such conditions, it is highly desirable to have a circuit which can harvest energy efficiently even under such low levels of voltage.

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Chapter 3

Rectifier-less Topology for Single Low-Voltage Piezoelectric Transducers

This chapter introduces an SECE based rectifier-less topology suitable for harvesting energy from low-voltage piezoelectric transducers. The block level details of the topology are introduced followed by the detailed circuit level implementation. The design methodology, including the criteria for component selection is discussed in detail and validated through circuit simulations. Experimental results are also presented to verify the effectiveness of the topology.

3.1 Introduction

The topology presented here is based on the classic SECE approach introduced in section 2.2.3. However, different from most of the conventional approaches, the interface circuit presented here does not employ an input rectifier and targets PETs generating low output voltages. A PET's output voltage drops significantly when it is subjected to vibrations away from its resonant frequency. Even at their resonant frequency, MEMS [1] based PETs generate very low voltages. The drawbacks of using conventional NVC based SECE circuits for low-voltage PETs have been discussed previously and the work presented here serves to eliminate them and improve upon them by incorporating a start-up circuit and a truly autonomous control circuitry. A Piezoelectric Energy Harvesting (PEH) system for single low-voltage PETs is discussed in this Chapter. The proposed system is based on the split-capacitor topology originally introduced for electromagnetic generators, by Dayal *et al.* in [2]. The former split-capacitor topology employed a conventional boost converter in which the inductor is continuously engaged, whereas the method used here is based on the SECE technique. Moreover, the system introduced in [2] required a pre-charged battery for start-up, unlike the design presented here, which is battery-free and kick-starts the system from a completely depleted energy storage. Since the control circuits are self-powered and the control signals required for reliable operation of the circuit are generated internally, the proposed PEH system is truly autonomous.

3.2 Architecture

A basic overview of the architecture and the functions of the individual blocks are presented here. The block diagram of the interface circuit for a single low-voltage PET is shown in Figure 3.1. The architecture of the SECE based, rectifier-free PEH system for low-voltage PETs comprises of the following sub-circuit blocks:

Figure 3.1 Block diagram of the rectifier-free, SECE based, PEH system for low-voltage PETs. The shaded area represents the BSC block. The dashed lines connecting the blocks indicate control signals and the solid lines indicate power flow..

1. Bi-directional Switching Converter (BSC)
2. Level Shifter (LS)
3. Peak Detector (PKD)
4. Zero Crossing Detector (ZCD)
5. Digital Logic Controller (DLC)
6. Under Voltage Lock Out
7. Start-up

SECE technique mandates the transfer of charge from the piezo capacitance, C_{PET} , into an inductor, L during the peak excursions (both positive and negative) of the PET's output voltage v_{PET} . C_{PET} is connected to L using a bi-directional switch, SW_{Bi} . Once the charge in C_{PET} is removed, v_{PET} falls to zero. At this instance, C_{PET} needs to be disconnected from L . A Bi-directional Switching Converter (BSC) is used for power conversion in the proposed PEH system. The PKD block is used for

detecting the voltage peaks in the v_{PET} waveform and responds to both positive and negative peaks. The ZCD block detects the zero-crossing events of the v_{PET} waveform i.e. positive to negative transition and vice-versa. The ZCD block has a shutdown feature to save power during inactivity. The voltage outputs of the PKD and ZCD blocks i.e. V_{PKD} and V_{ZCD} are fed to the Digital Logic Controller (DLC) which generates the control signals for SW_{Bi} . An additional gate driver stage comprising of a simple Level Shifter (LS) and an inverting buffer is used for driving SW_{Bi} , which consists of MOSFETs with large input capacitance (C_{iss}). The Start-up block serves the purpose of kick-starting the circuit when C_{STO} has zero energy or when depleted below the minimum voltage (under-voltage condition) required for normal operation. Such an under-voltage condition could lead to erroneous functioning of the sub-circuit blocks and cause excessive current drain from C_{STO} . To avoid such a scenario, the Under Voltage Lock Out (UVLO) block cuts off the power supply to the PKD, ZCD, DLC blocks and the load. Simultaneously, the UVLO block enables the Start-up block to charge C_{STO} back to the threshold voltage required for normal operation.

3.3 Circuit implementation of the sub-circuit blocks

The sub-circuit blocks used in the PEH system are implemented using discrete components and incurs more real estate than an IC solution. However, it gives the designer the liberty to choose from a broad spectrum of off-the-shelf devices and facilitates rapid prototyping. The details of the circuit implementation of the proposed system is presented here, along with the trade-offs considered as part of the component selection process. Since the target power range of the design is within a few hundred microwatts, circuit elements were carefully chosen to limit the circuit's intrinsic power consumption up to few tens of microwatts. Due to the intermittent nature of the ambient vibration, special emphasis is given to limit the standby power consumption of the circuit. Circuit design also ensures that the

Figure 3.2 Schematic of the single PET Bi-directional Switching Converter using ideal switches.

selected devices can function reliably within the VSTO range of 2.7 V – 5 V. It is worth mentioning that whenever a device has comparable parameters with another, the one with a simulation model is given preference.

3.3.1 Bi-directional Switching Converter (BSC)

The rectifier-free operation is achieved by incorporating a Bi-directional Switching Converter (BSC) in the system. The switching elements and the different stages of operation of the converter are elaborated here. The basic schematic of the BSC block using ideal switches is shown in Figure 3.2 and it consists of a bi-directional switch, SW_{Bi} , unidirectional switches S_1 , S_2 , inductor L , capacitors C_1 - C_2 and C_{STO} . For ease of implementation, S_1 and S_2 are implemented using Schottky diodes D_P and D_N as shown in Figure 3.3. An active diode implementation would improve the converter's power efficiency; however, a discrete solution is complicated and might not achieve optimal performance in this case. The bi-directional switch, SW_{Bi} is implemented using a series combination of P-Ch and N-Ch MOSFETs as in [2].

Figure 3.3 Schematic of the single PET Bi-directional Switching Converter using Schottky diodes and MOSFETs.

The two MOSFETs MP_1 and MN_1 are connected as shown in Figure 3.3, such that their internal body diodes do not conduct when the MOSFETs are blocking.

3.3.1.1 Stages of operation

There are four stages of operation in the BSC block and are shown in Figure 3.4. Description of the different stages of operation is provided in the following section.

- **Positive half-cycle**

When the sinusoidal voltage v_{PET} reaches a positive peak value, V_{PET} , SW_{Bi} is closed, and the charge in C_{PET} starts to discharge into the inductor L . When C_{PET} is completely discharged, the current i_L in the inductor reaches a positive peak value, and SW_{Bi} is opened. Charge recycling takes place among the three capacitors at the output. This is to balance the charge imbalance from the previous operating stage (stage 4). In stage 2, the inductor tries to maintain the flow of current through it by lowering the voltage at V_{L+} node, facilitating i_L to flow through $L-D_N-C_2$ path and charging C_2 in the process. Since the output capacitor C_{STO} and C_1 are in parallel to C_2 , they also get charged in the process.

Figure 3.4 Stages of operation of the single-PET BSC. Stages 1 and 2 are part of the positive half-cycle, whereas stage 3 and 4 are part of the negative half-cycle. Dashed lines with arrows indicate direction of current flow.

- **Negative half-cycle**

When the sinusoidal voltage v_{PET} reaches a negative peak value, $-V_{PET}$, SW_{Bi} is closed and the charge in C_{PET} starts to discharge into the inductor L . When C_{PET} is completely discharged, the current i_L in the inductor reaches a negative peak value and SW_{Bi} is opened. Charge recycling takes place among the three capacitors at the output. This is to balance the charge imbalance from the previous stage (stage 2). This completes Stage 3 of the converter operation. In stage 4, the inductor tries to maintain the flow of current through it by raising the voltage at V_{L+} node,

Figure 3.5 Plot showing the $R_{DS(ON)}$ versus Q_g values of (a) N-Ch MOSFETs and (b) P-Ch MOSFETs. The MOSFETs closest (red) to the origin were selected from each plot.

facilitating i_L to flow through L-D_P-C₁ path and charging C₁ in the process. Since the output capacitor C_{STO} and C₂ are parallel to C₁, they also get charged in the process. Charge recycling takes place in the next stage, i.e. stage 1.

3.3.1.2 Device Selection

The rationale behind choosing the components of the BSC block has been presented here. Selection of critical components such as the MOSFET, diode, inductor and capacitor are discussed.

- **MOSFETs:** SW_{BI} needs both MP₁ and MN₁ to effectively block and conduct current in either direction. Choosing MOSFETs with a low $R_{DS(ON)}$ value would reduce the conduction losses, but at the expense of higher switching losses in the gate-driver circuit. The switching losses in the gate-driver circuit is proportional to the total gate charge, Q_g of the MOSFETs used. Q_g has been used as a measure of the switching losses incurred, instead of the input capacitance, C_{iss}, since Q_g gives a realistic estimate of the charge required to turn on the MOSFETs. For selecting the MOSFETs, a parametric search was

Figure 3.6 Plot showing the reverse leakage currents of (a) PMEG4002 and (b) BAT754 extracted from their respective datasheets.

done on an electronic component supplier's website to shortlist the MOSFETs with the lowest $R_{DS(ON)}$ and Q_g values. Also, it was ensured that the MOSFETs have extremely low values of drain to source leakage current ($I_{DSS} < 100$ nA) and can withstand the voltage stress encountered when the MOSFETs are off ($V_{DSS} > 8$ V). An $R_{DS(ON)}$ vs Q_g plot for the shortlisted MOSFETs is shown in Figure 3.5. The MOSFETs closest to the origin were chosen in this design.

- **Diodes:** The diodes D_P and D_N are Schottky diodes (NXP PMEG4002) with a forward voltage drop (V_F) of 320 mV at a forward current (I_F) of 10 mA. The maximum reverse leakage current (I_R) of the selected diodes is 500 nA at a reverse voltage (V_R) of 25V. Schottky diodes with even lower V_F values were available; however, the I_R value increased drastically in those cases. For e.g., BAT754 Schottky diode has a lower V_F compared to the selected diode. However, upon comparing the I_R values of both diodes, shown in Figure 3.6, it can be observed that the I_R value of BAT754 is four times that of the selected diode, which leads to significant losses during standby.

- Inductor and Capacitor:** A 1 mH surface mount inductor with a DC Resistance (DCR) of 3.4Ω and a volume of 150 mm^3 is used for testing the prototype. The inductors were chosen as a trade-off between an acceptable efficiency and size. Simulations done earlier in OrCAD PSpice provided an estimate of the value of inductance needed. Increasing the inductance by keeping the resistance minimal will improve power efficiency. However, an important point to note here is that, increasing the size of the inductor increases the time t_{SECE} needed for charge transfer. This causes the control circuits to operate longer accompanied by an increase in power consumption. There is a critical inductance value beyond which, increasing the same would adversely affect the efficiency. In discrete implementations, the critical value would be reached at a lower value of inductance due to the relatively higher intrinsic power demand. A value of $2.2 \mu\text{F}$ was used for C_1 and C_2 , whereas a much higher capacitance of $100 \mu\text{F}$ was used for the storage capacitor, C_{STO} . A large capacitance reduces the ripple across the split-capacitors and eliminates issues during start-up. During the transition phase from start-up to SECE, there is a slightly higher current draw from C_{STO} causing V_{STO} to drop. If C_{STO} were a small value, the drop in V_{STO} would be large and this would lead to oscillations around the point and the system would fail to start up.

3.3.2 Level Shifter (LS)

In the single low-voltage PET topology, the control signals for SW_{Bi} are referenced to the PET ground. Switching on SW_{Bi} requires voltages above (for N-Ch) and below (for P-Ch) the PET ground which is readily available across the split-capacitors, C_1 and C_2 . The control signals to SW_{Bi} originate from the DLC block which is powered by a 2.5 V LDO, referenced to V_{SS} . To increase the voltage drive to SW_{Bi} , a logic level shifter (ADG3301) is used to shift the control signals with $V_{OH(MAX)} = 2.5 \text{ V}$ and $V_{OL(MIN)} = V_{SS}$ to $V_{OH(MAX)} = V_{STO}$ and $V_{OL(MIN)} = V_{SS}$. A non-

inverting buffer (SN74LVC1G34) used in the following stage, guarantees the driving current necessary for fast switching.

3.3.2.1 Device Selection

ADG3301 was selected for consuming the lowest quiescent power ($< 500 \text{ nA}_{\text{typ}}$ at 5 V) and lowest leakage power ($< 1 \text{ }\mu\text{A}_{\text{max}}$ at 5 V) amongst level translators which can work across the entire power supply range of 2.7 V to 5 V. Similarly, the non-inverting buffer, SN74LVC1G34 had the lowest quiescent power ($< 1 \text{ }\mu\text{A}_{\text{max}}$ at 5 V) and leakage power ($< 1 \text{ }\mu\text{A}_{\text{max}}$ at 5 V) with the ability to drive $> 32 \text{ mA}$ of current at 5 V into SW_{Bi} 's gate, enabling fast switching.

3.3.3 Peak Detector (PKD)

The circuit shown in Figure 3.7 is used for peak detection and employs a comparator, U_1 which compares the scaled version of v_{PET} with a delayed version of v_{PET} itself [3]–[5]. Comparing a sinusoidal signal with a delayed version of itself forces the comparator to toggle at the voltage peaks. The PKD block connects to the BSC block as shown in Figure 3.8. Ideally, connection to the $V_{\text{L+}}$ node would be sufficient to sense the voltage peaks, if the ground connection to the PET was continuous. However, since in this case, the ground side of the PET is disconnected from the system ground when SW_{Bi} is off, the PKD block monitors the node voltage above SW_{Bi} as shown in Figure 3.8. The PKD output, V_{PKD} toggles from high to low ($\text{H} \rightarrow \text{L}$) when v_{PET} reaches a positive peak and vice-versa at the negative peak. An inverter, U_{28} is connected at the output of the PKD block to make the logic compatible with the DLC block. In addition to the logic, U_{28} also performs down-translation of the V_{PKD} voltage to the voltage level at which the DLC block operates. The inverter is powered by the voltage level of the DLC block, but can handle input voltages up to 5V. Hence the output of the comparator is fed directly to the inverter, which down-translates the voltage to DLC's level.

Figure 3.7 Schematic of the peak detector for single low-voltage PETs with an inverting buffer at the output.

Figure 3.8 Schematic showing the node (blue arrow) at which the peak is monitored in a single PET system

3.3.3.1 Device Selection

An RC low-pass filter using a 330 k Ω resistor and a 100 pF capacitor creates a delayed version of v_{PET} . The RC delay (33 μ s) is small enough for accurate peak-detection and at the same time sufficiently large to prevent erroneous triggering due to noise. Since PKD is an always-on block, a low power comparator, TS881 consuming a quiescent current of 220 nA at 2.7 V has been selected for U₁. Comparator selection should guarantee that the power gain obtained by choosing a fast comparator should be more than the quiescent power losses in the comparator. The power-loss, $P_{peak-loss}$ due to an inaccurate peak detection is given by (3.1)

$$P_{peak-loss} = CV_{PET}^2 (1 - \cos^2 \omega_{VIB} t_{dly}) / T_{VIB} \quad (3.1)$$

where V_{PET} is the peak value of the v_{PET} waveform, T_{VIB} is the time-period of v_{PET} , ω_{VIB} is the angular frequency of vibration and t_{dly} is the delay in peak detection. t_{dly} in this configuration is about 400 μ s, which is the sum of the RC delay and the propagation delay, t_{PD} (7 μ s at 2.7V) of TS881. Dynamic hysteresis provided by a 36 pF capacitor, prevents oscillations at the output of U₁, occurring due to parasitic coupling in the PCB. A voltage divider using resistors 5.6 M Ω and 2.2 M Ω scales the voltage and sets the minimum v_{PET} to 500 mV for peak detection. The chosen voltage division ensures that the harvesting process is not triggered by a signal which is unable to provide a positive power budget.

3.3.4 Zero Crossing Detector (ZCD)

The circuit shown in Figure 3.9 is used for zero-crossing detection and utilizes a comparator, U₂ which is faster than the PKD circuit's comparator by an order of magnitude. The ZCD circuit should be quick enough to respond to the zero-crossing events and justifies the need for a fast comparator. Since U₂ consumes a high quiescent current, it is enabled only when a peak detection event has occurred and is immediately disabled after the zero-crossing event. The shutdown signal

Figure 3.9 Schematic of zero crossing detector in the single-PET topology. Signal A originates from the DLC block.

($\overline{SD}$) for the comparator is generated by the DLC block. and uses a level translator, U_{27} is a non-inverting level-shifter for raising the voltage to the level at which U_2 is operated. U_{26} is a non-inverting buffer used for down-translation of U_2 output to the DLC block's voltage level. Two 100 k Ω resistors generate a scaled version of the V_{L+} node voltage at the non-inverting terminal of the comparator and is compared with the PET ground connected to the inverting terminal. The output of the comparator, V_{ZCD} toggles from high to low ($H \rightarrow L$) when V_{L+} crosses zero to become negative and vice-versa when V_{L+} crosses zero to become positive.

3.3.4.1 Device Selection

During the design phase, it was observed that options for a low power (< 500 μA at 5 V) comparator with a shutdown feature were limited to a few, such as the MAX9030 from Maxim Integrated and LMV761 from Texas Instruments (TI). Though MAX9030 is rated to consume lower power, LMV761 was chosen due to the lower input offset voltage and the availability of a simulation model. LMV761 is a fast comparator with a maximum t_{PD} of 120 ns (at $V_{DD} = 5$ V) with 50 mV

Figure 3.10 Schematic of the control circuit. The SR latch is implemented using two NOR gates as shown inside the dashed box (shaded).

overdrive at its inputs. Since the output of U_2 is tri-stated when shut down, a 100 K Ω resistor is added at the output pin, to connect the CMOS input of the following stage to supply ground. U_{27} uses ADG3301 as the level translator, whereas U_{26} uses SN74LVC1G34 as the buffer and were selected due to reasons explained in section 3.3.2.1.

3.3.5 Digital Logic Controller

The circuit shown in Figure 3.10 is the Digital Logic Controller (DLC) that generates the control signals for SW_{Bi} . The circuit consists of two sections, each handling the signal generation in one half-cycle. The circuit comprising of D flip-flops U_5 , U_6 , inverters U_{11} , U_{12} and SR latch, U_9 controls the generation of signal A_x , whereas the circuit consisting of D flip-flops U_7 , U_8 , inverters U_{13} , U_{14} and SR latch, U_{10} control the generation of signal A_y . The OR gate, U_{16} ensures that the switch control signal A is high (i.e. SW_{Bi} is closed), when either of the signals A_x or A_y is high. All the flip-flops used are positive edge triggered and have a CLEAR

Figure 3.11 Waveform showing the output, A of the DLC block and its effect on the input waveform.

and PRESET input. Initially, when both A_x and A_y are low, U_6 is cleared ($Q = 0$) and only U_5 is enabled. The V_{PKD} signal toggles from $L \rightarrow H$ when a positive peak is detected, which causes the Q output of U_5 to go high, which sets ($S = 1, R = 0$) the Q output ($A_x = 1$) of U_9 . Since A_x remains high, the output of U_{11} becomes low, forcing U_5 to enter and U_6 to exit CLEAR state. However, the output of U_9 remains unchanged ($A_x = 1$) since $S = R = 0$. The V_{ZCD} signal toggles from $H \rightarrow L$ when V_L+ crosses zero to become negative. Inverter U_{12} is used to convert the $H \rightarrow L$ transition of the V_{ZCD} signal to a $L \rightarrow H$ transition, which sets U_6 . The output Q of U_6 goes high which resets ($S=0, R=1$) the Q output ($A_x = 0$) of U_9 , opening SW_{Bi} . The operation mentioned above repeats in the negative half-cycle, when the V_{PKD} signal toggles from $H \rightarrow L$ (negative peak), setting $A_y = 1$ and closing the switch. The switch is opened again when $A_y = 0$ due to the $L \rightarrow H$ transition of the V_{ZCD} signal at D input of U_8 . The output waveform of the DLC block and its effect on the input waveform can be seen in Figure 3.11.

3.3.5.1 Device Selection

All the logic devices used for implementing the DLC block has been picked from TI's Advanced Ultra-Low Power (AUP) family of devices, mainly owing to their ultra-low dynamic power and quiescent current consumption. However, the operating voltage range of the AUP family of logic devices is 0.8 – 3.3 V, whereas the operating range of the PEH system is 2.7 – 5 V. The logic devices in the DLC block would be damaged if directly powered by the above voltage. To avoid damage to its logic devices, the DLC block is powered using a Low Dropout Regulator (LDO), U₂₄ (refer Figure 3.13) which provides a fixed voltage output from an input voltage as low as 2.7 V. The LDO selected here is Intersil's ISL60002 which provides a stable output of 2.5 V for the DLC block and doubles as a regulated power supply for the load, consuming a quiescent current of only 350 nA at 3 V, the least current among other design choices.

3.3.6 Start-up

The storage capacitor, C_{STO} is initially charged through a start-up circuit connected to the PET, which consists of a DBR followed by a four-stage Dickson Charge Pump (DCP) as shown in Figure 3.12. A diode implementation was chosen in lieu of MOSFETs for the DCP, to avoid the use of complex control circuitry. To facilitate start-up, two normally-on switches viz. J₁ and J₂ are used to provide the initial conduction path which is later cut-off by the UVLO block when SECE circuit starts operation. A filter capacitor, C_{STA} is connected at the output of the DBR and is continuously monitored by a supply voltage monitoring chip, U₂₀, with a preset upper threshold, V_{PRE+} = 975 mV and lower threshold, V_{PRE-} = 900 mV. When V_{STA} > V_{PRE+}, the output of U₂₀ closes a PMOS switch MP₇, which connects C_{STA} to DCP. If the input power is not high enough to maintain V_{STA} > V_{PRE-}, MP₇ is disabled and is re-enabled only when V_{STA} > V_{PRE+}, gradually charging C_{STO} to

Figure 3.12 Schematic of the start-up circuit.

the desired voltage level (2.66 V in this design). The clock signal required to drive the switching capacitors in the DCP is generated using a resistor-tuned CMOS oscillator, U_{19} . An inverter, U_{18} generates the 180° degree out of phase signal needed for the DCP. U_{19} has an operating voltage range of 0.9 V – 2 V; hence is protected against any over-voltage condition using a Zener diode, D_Z , which regulates the supply voltage of U_{19} to 1.8 V. A JFET stores charge in its intrinsic junction capacitance, even when its gate drive is removed. Such a situation applies for J_1 alone since its gate is left in a high impedance state when the gate drive of 0 V is removed. The JFET would fail to turn on the second time, due to the charge build-up and the start-up circuit will fail. To overcome such a scenario, a 10 M Ω bleed-off resistor is added between the gate and the source of J_1 to remove the charge stored in the junction capacitance. However, such a resistor is not required for J_2 since the gate is always driven high or low and is never in a high impedance

state. The start-up circuit is disabled by driving J_1 's gate to the lowest and J_2 's gate to the highest potential available in the system. J_1 has a typical V_{GS-OFF} value of 0.8 V, which causes the drain end of J_1 to be at 0.8 V when turned off. If the drain end of J_1 needs to be at 0V, the gate needs to be pulled down further by $-0.8V$, which is not feasible without additional circuitry. However, the start-up circuit is not activated by the 0.8 V at C_{STA} because U_{20} needs a minimum voltage of 975 mV to enable MP_7 .

3.3.6.1 Device Selection

Diodes $D_{R1} - D_{R4}$ and D_S use NXP PMEG4002EB, and were selected for having the lowest V_F within an acceptable I_R limit of < 200 nA at < 5 V (V_R). BF862 (N-Ch) is used for JFET J_1 , whereas MMBFJ177 (P-Ch) is used for JFET J_2 . JFETs were selected to have the lowest V_{GS-OFF} voltage among available options. TPS3839A09 (U_{20}) is a voltage monitoring chip with a threshold setting of 0.9 V and an ultra-low current consumption of 150 nA at 5 V. U_{17} and U_{18} are low-power Schmitt-trigger inverters for logic-level inversion and are implemented using SN74AUP1G14 from TI's AUP family of logic devices. NX3008P (MP_7) is a P-Ch MOSFET with a low gate-source turn-on voltage, $V_{GSth} = 0.9$ V, ideal for starting up from low voltages. TS3001 (U_{19}) is a resistor tuned CMOS oscillator which produces a 25 kHz, 50% duty cycled, clock signal, chosen mainly because of its lowest current consumption of 1 μ A at 1 V. The 1.8 V Zener diode (MMSZ4678) used for limiting the voltage supply to U_{19} was chosen owing to its low value of leakage current.

3.3.7 Under Voltage Lock Out

In the absence of ambient vibrations, V_{STO} could fall below the working voltage of the control circuits, which could further accelerate the discharge of C_{STO} . To prevent such a scenario, the load and control circuits are disconnected from C_{STO} when $V_{STO} < V_{PRE-} = 2.63V$ and is re-enabled only when $V_{STO} > V_{PRE+} = 2.66$ V.

Figure 3.13 Schematic of the Under Voltage Lock Out circuit. Signals for controlling JFETs, J_1 and J_2 are generated from this block.

This is accomplished using an Under-Voltage Lock Out (UVLO) circuit shown in Figure 3.13, which deactivates MP_8 . Additionally, the UVLO circuit disables the JFETs, J_1 and J_2 , when $V_{STO} > V_{PRE+}$ and re-enables the same when V_{STO} falls below V_{PRE-} , hence enabling the start-up circuit. The UVLO circuit comprises of a voltage monitoring circuit U_{21} , a tristate buffer, U_{22} , and an inverter, U_{23} . If the gate of J_1 were driven using a CMOS output from the UVLO block during an under-voltage condition, a high voltage at J_1 's gate would cause excessive current flow through its gate and cause the start-up circuit to fail. Hence a tristate buffer, U_{22} is used for driving the gate of J_1 , keeping the gate of J_1 tri-stated when required to be off.

3.3.7.1 Device Selection

U_{21} is implemented using TI's TPS3839L30, which is a voltage monitoring chip with a lower voltage threshold of 2.63 V and an ultra-low current consumption of 150 nA at 5 V. The chip has an upper voltage threshold of 2.66 V at which other

Table 3.1 List of components for the low-voltage single PET topology

Reference Designator	Part Number / Value	Reference Designator	Part Number / Value
U ₁	TS881	U ₂₅₋₂₆	SN74LVC1G34
U ₂	LMV761	U ₂₇	ADG3301
U _{3-4, 16}	SN74AUP3G32	D _Z	MMSZ4678
U ₅₋₈	SN74AUP1G74	D _{P, N, R1-R4, S}	PMEG4002EB
U ₉₋₁₀	SN74AUP2G02	J ₁	BF862
U ₁₁₋₁₅	SN74AUP2G04	J ₂	MMBFJ177
U ₁₇₋₁₈	SN74AUP1G14	MN ₁	BSS806N
U ₁₉	TS3001	MP _{1,2}	NX2301P
U ₂₀	TPS3839A09	MP ₃	NX3008P
U ₂₁	TPS3839L30	R _{SET}	4.32 M Ω
U ₂₂	SN74AHC1G126	L	LPS6235-105MR
U _{23, U28}	SN74AHC1G14	C _{STO}	100 μ F
U ₂₄	ISL60002-25	C _{STA}	1 μ F

sub-circuits commence operation due to the turn-on of MP₈, a P-Ch MOSFET. MP₈ is implemented using NX2301P which has a very low $R_{DS(ON)}$ of 155 m Ω at a V_{GS} of 2.7 V. U₂₂ uses a non-inverting buffer, SN74AHC1G126 with a 3-state output and an ENABLE input, whereas U₂₁ uses an inverting buffer, SN74AHC1G14. Both the above buffers were chosen due to their wide operating range (2 – 5.5 V) and low quiescent current consumption of 1 μ A at 5 V.

Table 3.1 provides a list of all the components used for implementing the single low-voltage PEH system.

3.4 Simulation Results

Simulations were carried out in OrCAD PSpice v16.6 and the PSpice models of the components used were obtained from their respective manufacturer websites. Devices such as buffers, clock generators, voltage monitors etc. lacked a simulation model; and hence, simulations of sub-circuits containing such devices were not carried out. The sub-circuits for which simulation models for all the components were available are the BSC, PKD and ZCD blocks.

3.4.1 Bi-directional Switching Converter (BSC)

Figure 3.14 Simulated voltage and current waveforms of the SECE based BSC circuit. Arrows point to the enlarged version of i_L and V_{SW} waveforms.

Besides verifying the basic functionality of the BSC block, simulations were done to find the BSC's power conversion efficiency. The Thevenin equivalent model (see Figure 2.4) of the PET has been used in the simulation, since adjusting the

Figure 3.15 Simulated voltage waveform across the split-capacitors, C_1 (bottom) and C_2 (top).

amplitude of the voltage source directly gives the open-circuit voltage (V_{OC}), unlike the Norton equivalent, where the amplitude of the current source needs to be calculated each time for a new V_{OC} value. At the output end, the capacitor, C_{STO} is replaced by a DC voltage source, V_{STO} which helps to calculate the efficiency at different storage/load voltages. The V_{OC} of the PET is varied from 0.5 V – 1.75 V and storage voltage, V_{STO} is varied from 2.7 V – 5 V. All the simulations were done by keeping the input frequency (f_{VIB}) at 65 Hz.

Figure 3.14 shows the simulated characteristic voltage and current waveforms of the BSC circuit. The waveforms were obtained with the following parameters: $C_{PET} = 530$ nF, $L = 1$ mH (DCR = 3.4 Ω), $C_{1,2} = 2.2$ μ F, $V_{STO} = 5$ V, $V_{OC} = 1$ V_{PK}. It can be observed that the input voltage, V_{PET} is twice the V_{OC} , which confirms the SECE operation. The timing of the switch pulse, V_{SW} was calculated based on equation (2.2). In Figure 3.14, the inductor current, i_L can be seen rising and falling when SW_{Bi} is turned on and off, respectively. Figure 3.15 shows the

Figure 3.16 Plot showing simulated power conversion efficiency of the single PET BSC circuit corresponding to input voltages ranging from 1 V to 3.5 V.

voltage across the split-capacitors, C_1 and C_2 . It needs to be noted that, though there is a voltage variation across individual capacitors, $V_{C1} - V_{C2}$ will be a constant.

The simulated efficiency, η_{sim} , of the BSC circuit is plotted in Figure 3.16. It was found that the input power, P_{in} remained constant irrespective of the output voltage, which is again a characteristic of SECE circuits. A peak efficiency of 73.7 % was observed during simulations. For a specific input voltage, the efficiency shows an improving trend as the output voltage increases. This is because, for the same amount of P_{in} , when V_{STO} increases, the inductor needs to push current into the output capacitor at a higher voltage ($V_{STO} + V_F$). This reduces the duration of current flow in the output path. Reduction in time, reduces the conduction losses (E_{cond}) as given by (3.2).

$$E_{cond} = I^2 R t \quad (3.2)$$

Where, R is the resistance, I is the current and t is the duration of current flow.

Figure 3.17 Simulated waveforms of the Peak Detector circuit.

3.4.2 Peak Detector

The Peak Detector circuit has been simulated using a sine wave signal at its input. The sine wave has a frequency of 65 Hz and an amplitude of 3.5 V_{PK}. The PKD comparator, TS881 has been supplied using a dual voltage power supply of +/- 2.5 V such that the output swing of the comparator would be 5 V centered around the PET ground. The sine wave passes through the voltage divider and undergoes scaling. The scaled voltage and the delayed version of the scaled voltage are supplied to the VIN- and VIN+ terminals of the comparator, respectively. The simulated output of the PKD block, V_{PKD} can be seen toggling at the voltage peaks in Figure 3.17. A delay of 400 μ s was observed before the comparator output toggles after the detection of a voltage peak. The voltage divider is designed to minimize the leakage current through it and uses resistors in the Mega Ohms range.

However, this adds to the RC delay at the input of the PKD comparator and increases the delay. It's worth noting that, the voltage spike observed on top of the scaled and delayed (also scaled) versions of the input signal is due to the dynamic hysteresis created by the addition of the 36 pF capacitor between the comparator output and VIN+ input. Hysteresis became a requirement after the PCB prototype was tested and unwanted parasitic oscillations were observed at the output of the comparator. The simulations were repeated to include the hysteresis effect. Hysteresis could be added to a comparator by positive feedback using a resistive network. However, a capacitive hysteresis approach used fewer components and consumed zero static current, compared to a resistor based method.

3.4.3 Zero Crossing Detector

The Zero Crossing Detector circuit has been simulated with the sine wave input used previously for the PKD block. A dual voltage power supply of +/- 2.5 V is used to supply the ZCD comparator, LMV761. The sine wave is applied to the VIN+ input of LMV761 through a voltage divider and the system's circuit ground is applied to the VIN- input. The physical comparator IC has an active-low SHUTDOWN pin to disable the device and reduce the supply current, but the available simulation model did not include a SHUTDOWN pin. Nevertheless, the functionality of the ZCD block is simulated without using the SHUTDOWN pin and the resulting waveforms are shown in Figure 3.18. The output of the comparator can be seen toggling, when the sine wave crosses the circuit ground. A delay of approx. 300 ns is observed due to the propagation delay of the comparator and resistance of the voltage divider. The resistors used for the voltage divider are in the Kilo Ohms range. This reduces the delay encountered by the ZCD block, but would also increase the leakage current through them. However, the amount of time for which a voltage is present at the VL+ node is when SW_{Bi} is closed and this amounts to a fraction of the time-period of the sinusoidal signal and leads to very

Figure 3.18 Simulated waveforms of the Peak Detector circuit.

low leakage power in the voltage divider. Unlike the PKD comparator, no hysteresis is provided for the ZCD comparator to avoid parasitic oscillations. This is because, the DLC block of the PEH system is designed in such a way that, the ZCD block is disabled, during the first transition (rise or fall) of the comparator output, removing the subsequent transitions caused by parasitic coupling in the PCB.

3.5 Measurement Results

The sections to follow provide details on the implemented PCB prototype, the measurement setup and the experimental results.

3.5.1 PCB Prototype and Experimental Setup

A double layer Printed Circuit Board (PCB) measuring 50 x 100 mm² in area was

Figure 3.19 PCB prototype of the single low-voltage PEH system.

fabricated and assembled using off-the-shelf components listed in Table 3.1. The PCB prototype of the single low-voltage PEH system is shown in Figure 3.19. To demonstrate the functionality of the proposed system, an off-the-shelf PET measuring $90 \times 16.8 \times 0.8 \text{ mm}^3$ in size was used. The two active piezoelectric layers on either side of the bimorph cantilever were connected in parallel configuration and wires were soldered to its terminals for connection to the PEH system. The PET was drilled with an M5 sized hole for fixing nuts and bolts, so that the harvester could be tuned to the desired frequency by adding metal washers in between as shown in the inset of Figure 3.20. The PET was mounted using two screws on an 8-mm thick aluminium platform and the platform was mounted on an electromagnetic shaker (Sentek Dynamics VT-20) driven by a power amplifier (Sentek Dynamics LA-100). The sinusoidal signal was provided by a vibration controller (Dynatronic Corp. VENZO-820), which received feedback from an accelerometer (Briel & Kjaer 4519-003) mounted on the aluminium platform. The

Figure 3.20 Experimental setup used for measurements.

experimental setup is shown in Figure 3.20.

3.5.2 Start-up mechanism and transition to SECE

In Figure 3.21, the start-up circuit can be seen charging a $100\ \mu\text{F}$ capacitor from 0 V to 2.66 V. In the same figure, the UVLO circuit can be seen disabling the start-up circuit and enabling the SECE circuit simultaneously. The activation of SECE can be verified by the characteristic voltage enhancement associated with the technique shown in the inset of Figure 3.21. The start-up circuit starts to harvest energy from a voltage as low as 650 mV across the PET device. When $V_{\text{PET}} = 650\ \text{mV}$, C_2 is charged to a voltage of about 325 mV (w.r.t V_{SS}) through diode D_{R3} which increases the DC level of v_{PET} by 325 mV, making $V_{\text{STA}} = 975\ \text{mV}$ and activating U_{20} . The V_F of diodes D_{R1} - D_{R4} drops to a very low value when I_F (C_{STA} 's charging current) is weak, which enables starting up from 650 mV, but takes about 427 seconds to charge C_{STO} to the required voltage threshold (2.66 V in this design).

Figure 3.21 Waveform acquired using an oscilloscope during start-up. The transition from start-up phase to SECE is visible in the zoomed waveform at the bottom.

Figure 3.22 Plot showing the variation of start-up time with input voltage amplitude. The vibration frequency was set to 70 Hz.

Figure 3.23 Characteristic voltage and current waveforms of the SECE technique in the single low-voltage PEH system. Channel 4 (pink) shows the SW_{Bi} 's gate control signal.

Figure 3.22 shows the variation of start-up time with input voltage amplitude. As expected, start-up time improves with increasing input voltages.

To verify successful operation of the PEH system, characteristic waveforms associated with the SECE technique were acquired using an oscilloscope as shown in Figure 3.23. A $10\ \Omega$ resistor was added in between the inductor and PET ground to capture the inductor current waveform, i_L . At the V_{L+} node, oscillations (ringing) are visible, which is due to the energy left in the inductor due to the V_F of the output diode. In [6], an oscillation cancellation switch is used to prevent unwanted triggering of the control circuitry. However, since the control circuit in this work uses an edge based triggering, the circuit will only respond to the first voltage transition of the ZCD block and will not cause any unwanted triggering.

Ideally, upon commencement of SECE, the voltage across the PET should be twice the open circuit voltage, for transducers having a low electromechanical coupling factor (α) or for transducers operating at off-resonance. The coupling

Figure 3.24 Voltage across capacitors C_1 (Channel 1) and C_2 (Channel 2) measured using an isolated channel oscilloscope.

factor of the PET was not estimated, but it was observed that the open circuit voltage, V_{OC} was magnified only by 1.6x and 1.78x under resonance and off-resonance conditions, respectively. Authors in [7] have studied the effectiveness of using SECE for PETs with different values of α and it was concluded that SECE is most suitable for weakly coupled PETs and for PETs with medium coupling, operating at off-resonance. Hence, it may be fairly concluded that the PET used in this work falls in the medium coupling regime. The inability of the circuit to achieve 2x voltage magnification during off-resonance could be attributed to the delay in peak detection and the non-ideal zero-crossing detection. The non-ideal zero crossing is a result of the comparator's input-offset error, aggravated by voltage scaling.

Figure 3.24 shows the voltage across the split capacitors C_1 and C_2 , which was measured using an isolated channel oscilloscope (TPS2014B) to avoid shorting of the supply grounds. The voltage across the split capacitors can be seen varying

when charge is deposited on them, but the voltage difference, $V_{C1}-V_{C2}$ is fixed, due to the large value of C_{STO} .

3.5.3 Intrinsic Power Consumption and Converter Efficiency

The power consumed by individual blocks were calculated by taking the product of the voltage and current supplied by a Keithley 2400 source meter. The intrinsic power consumption of all the sub-circuits is only dependent on the V_{STO} voltage. Energy stored in C_{PET} is given by $1/2 C_{PET} V_{PET}^2$, and since the harvesting circuit extracts this energy twice during a vibration period, T_{VIB} , the input power, P_{in} into the harvester is given by $CV_{PET}^2 f_{VIB}$. The output power, P_o is calculated as $V_{STO} I_{OUT}$, where I_{OUT} is measured using the arrangement shown in Figure 3.25. The Keysight 34461A bench multimeter displays the current, I_{OUT} flowing into the power supply, which is set at a specific voltage (V_{STO}). Power conversion efficiency, η of the bi-directional switching converter is given by (3.3)

$$\eta = \frac{V_{STO} I_{OUT}}{CV_{PET}^2 f_{VIB}} \quad (3.3)$$

The control circuits were powered externally when calculating the power conversion efficiency, as shown in Figure 3.25. All the measurements reported below were taken at an input frequency of 65 Hz. Figure 3.26 shows the intrinsic power consumption of the various sub-circuits in the single-PET system. Miscellaneous power consumption shown in the figure consists of the LDO which consumes 350 nA of quiescent current. Besides, the voltage monitoring circuit inside the UVLO block and the fly-back diodes, D_P and D_N also contributes to miscellaneous power consumption. Majority of the control circuit losses are in the ZCD block, which is a fast comparator with a quiescent current of approx. 300 μA . The power consumption of the DLC block is constant since it is powered by the 2.5 V LDO. The maximum intrinsic power consumption of the single-PET system is 14.7 μW at 5 V.

Figure 3.25 Experimental setup for measuring the voltage and current in the circuit. The Keithley 2400 source meter measures the quiescent current consumption of the control circuits, and the Keysight 34461A measures the output current.

Figure 3.26 Measured intrinsic power consumption of the sub-circuit blocks in the single-PET system. An inductor of 1 mH (DCR = 3.4 Ω) was used during the measurement.

Figure 3.27 Measured standby power consumption of the sub-circuit blocks in a single-PET system.

Figure 3.28 Experimental (bottom) vs. simulated (top) efficiency of the single-PET BSC block using $L = 1$ mH, $DCR = 3.4 \Omega$. The efficiency is plotted for different input voltages, ranging from 1.0 V to 3.5 V

When no vibrations are present, there is no switching activity in the system and the power consumption is minimum, which is due to the standby current flowing in the system. The variation of the standby power w.r.t the supply voltage, V_{STO} is shown in Figure 3.27. It can be observed from the figure that the PKD block and the miscellaneous section consume the highest standby power.

Both experimental, η_{exp} and simulated efficiency, η_{sim} of the single low-voltage PEH system are plotted in Figure 3.28. The experimental efficiency is in good agreement with the simulated efficiency. For a specific input voltage, the input power, P_{in} is almost constant and does not depend on other circuit parameters, which is one of the characteristics of the SECE technique. Since P_{in} is constant at a specific V_{PET} , the efficiency increases with an increase in V_{STO} , due to reasons explained in section 3.4.1. The reduction in efficiency for higher input voltages, predicted earlier through simulations, can be observed in the experimental results as well. The single-PET BSC block achieved a peak efficiency of 73 % with a 1 mH surface mount inductor.

3.6 Comparison with State-of-the-art

Important results from the single low-voltage PEH system are compared with other state-of-the-art systems in Table 3.2. It's worth noting that many interface circuits optimized for low voltage operation are fabricated on chip and hence their power handling capability is generally low. While [3] uses the smallest inductor among all the circuits compared, it lacks a start-up circuit and also requires external tuning of the timing resistors. The topology also mandates an external negative power supply for improving the Input Common Mode Range (ICMR) of its PKD comparator and hence is not truly autonomous. [8] presents an SECE based integrated solution and incorporates a self-start feature and adaptive timing. However, input voltage range is smaller compared to the proposed topology and uses a larger inductor to achieve

Table 3.2 Comparison with Existing Piezoelectric Energy Harvesting Circuits

Parameters	[3]	[8]	[9]	This work
Technology	Integrated	Integrated	Discrete	Discrete
Technique	Rectifier-free SECE	SECE, NVC + NMOS bridge	SSHI	Rectifier-free SECE
Inductance, DCR [volume]	160 μ H, 3.4 Ω [27 mm ³]	0.1 mH, 0.1 Ω [665 mm ³]	1 mH, 1 Ω [>1020 mm ³]	1 mH, 3.4 Ω [150 mm³]
Self-Start	No	Yes	Yes	Yes
Startup voltage	n.a.	1.7 V	n.a.	650 mV
Input voltage	Up to 2.4 V	1.2 V – 2.4 V	1.75 V – 6 V	1 V – 3.5 V
Output power ¹	30 μ W	25 μ W	3.16 mW	300 μW
Intrinsic power	n.a.	600 nW @ 2V	35 μ W @ 4V	10 μW @ 3V
Timing	Preset	Adaptive	Adaptive	Adaptive
Efficiency	50%	70%	80%	73%

¹Experimentally demonstrated output power. n.a = not available.

a power conversion efficiency of 70 %. Moreover, the circuit in [8] has a higher startup voltage compared to this work. [9] uses the SSHI technique and is implemented using discrete components. However, the circuit caters to the milliwatt power range and uses a large sized inductor to achieve a power conversion efficiency of 80%. In conclusion, the proposed single low-voltage PET topology introduced here provides high efficiency even at low input voltages. The efficiency improvement is not by the use of a large sized inductor, but by employing a rectifier-free approach.

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Chapter 4

Rectifier-less Topology for an array of Low-Voltage of Piezoelectric Transducers

This chapter introduces the SECE based, rectifier-free circuit topology for multiple low-voltage piezoelectric transducers. The block level details of the topology are presented followed by the circuit implementation. The concept is verified through circuit simulations followed by the fabrication of a PCB prototype. The prototype is tested using commercially available piezoelectric transducers and the experimental results are discussed.

4.1 Introduction

The rectifier-less SECE topology introduced in Chapter 3 was designed for handling low-voltage PET devices. Often, practical scenarios might arise where combining two or more PETs would become a requirement. Examples of such scenarios are when (1) higher power output or (2) broadband operation is needed.

Figure 4.1 Schematic showing the single-PET topology extended for multi-PET operation. The red arrows show the nodes at which the peaks are monitored.

The single low-voltage PET topology introduced previously should have been sufficient for harvesting energy from multiple PETs and has been verified to do so successfully during simulations when switching signals are directly provided to SW_{Bi} . However, the motivation for a new SECE based, low-voltage multi-PET topology is the difficulty in implementing a peak detector circuit for monitoring the peaks in such a system. Figure 4.1 shows the single-PET topology extended for

Figure 4.2 Simulated waveform of the peak detector outputs, $V_{PKD1,2}$ and their respective inputs, $V_{PET1,2}$. The above waveforms are from the single-PET topology which is extended for multi-PET operation. Green arrows highlight the glitch in the output.

multi-PET operation. The circuit was simulated to test the functionality of the PKD blocks in a multi-PET system. Figure 4.2 shows the simulated waveform of the two PKD outputs, monitoring two PET sources. It is observed that the switching activity in one PET is affecting the peak detection in the other PET. The reason for this behavior is that in the single low-voltage PET topology, the PET is floating and is not referenced to a specific voltage. This floating nature makes it susceptible to fast, transient signals due to the switching activity from other PETs. When working with multiple PETs, it needs to be ensured that the harvesting process in one PET does not affect the other PETs. The above method of peak detection is suitable only for a single PET and hence the multi-PET topology is introduced here. Owing to

the short duration of t_{SECE} when compared to the time-period of mechanical vibration, T_{VIB} , it is possible that multiple PETs can share a single inductor, which is often the bulkiest component in a system. The sharing of the inductor results in a significantly smaller solution size. The concept of inductor sharing has been demonstrated in conventional switching converters [1], [2] which work in the Discontinuous Conduction Mode (DCM) and in SECE based switching converters [3], [4]. However, none of the above are suited for high-efficiency operation in low-voltage PETs.

4.2 Architecture

A basic overview of the architecture and the functions of the individual blocks are presented here. The block diagram of the architecture of the interface circuit for multiple, low-voltage PETs is shown in Figure 4.3. The architecture comprises of the following sub-circuit blocks:

1. Bi-directional Switching Converter (BSC)	5. Digital Logic Controller (DLC)
2. Dual Level Shifter (DLS)	6. Under Voltage Lock Out
3. Peak Detector (PKD)	7. Start-up
4. Zero Crossing Detector (ZCD)	

In a single-PET topology there will only be a single instance of the sub-circuit blocks. However, in the multi-PET topology with j number of PETs, there would be j instances of SW_{Bi} , PKD, DLS and DLC blocks. The rest of the blocks will be shared among multiple PETs. Besides the inductor, L , the ZCD block is also shared among multiple PETs to reduce the component count. ZCD block monitors the V_{L+} node, which starts following the j^{th} PET's output voltage node, when the respective switch, SW_{Bi-j} is closed.

Figure 4.3 Block diagram of the rectifier-free, SECE based, PEH system for multiple low-voltage PETs. The shaded area represents the BSC block. The dashed lines connecting the blocks indicate control signals and the solid lines indicate power flow. The cascaded boxes represent the blocks replicated for each PET.

4.3 Circuit implementation of the sub-circuit blocks

The details of the circuit implementation of the proposed system is presented here, along with the trade-offs considered as part of the component selection process. The underlying principle (SECE) of the multi-PET topology is identical to the single-PET case and hence most of the sub-circuit blocks used by the multi-PET topology are functionally similar to the former. Only the sub-circuits which are designed differently for the multi-PET system are discussed in detail below.

4.3.1 Bi-directional Switching Converter (BSC)

The switching elements and the different stages of operation of the converter are elaborated here. The basic schematic of the BSC block using ideal switches is

Figure 4.4 Schematic of the multi-PET BSC using ideal switches. The greyed-out PET shown in the schematic is representative of how the additional PETs can be connected.

Figure 4.5 Schematic of the multi-PET Bi-directional Switching Converter using Schottky diodes and MOSFETs. For simplicity, only one PET source is shown.

shown in Figure 4.4 and it consists of a bi-directional switch, SW_{Bi} , unidirectional switches S_1 , S_2 , inductor L , capacitors C_1 - C_2 and C_{STO} . Unlike the former topology, the bi-directional switch here is not referenced to the PET ground. However, it can conduct and block current in both directions. S_1 and S_2 are implemented using

Figure 4.6 Stages of operation of the multi-PET BSC. Stages 1 and 2 are part of the positive half-cycle, whereas stages 3 and 4 are part of the negative half-cycle. Dashed lines with arrows indicate direction of current flow.

Schottky diodes D_P , D_N whereas SW_{Bi} is implemented using a parallel combination of series connected N-Ch and P-Ch MOSFETs as shown in Figure 4.5. The back-to-back configuration of the MOSFETs ensures that the internal body-diodes do not conduct inadvertently. Both P-Ch and N-Ch MOSFETs are required to complement each other, since none of the MOSFETs conduct efficiently in both half-cycles.

4.3.1.1 Stages of operation

The working of the multi-PET BSC is same as the single-PET, except for the difference in the bi-directional switch used. Hence, the stages of operation are not

Figure 4.7 Schematic of the dual level shifter. The section of the circuit in the dashed boxes requires replication for each additional PET.

explained here in detail and can be found in section 3.3.1.1. Figure 4.6 shows the various stages of operation of the BSC. Stages 1 and 2 are part of the positive half-cycle, whereas stages 3 and 4 are part of the negative half-cycle.

4.3.2 Dual Level Shifter (DLS)

In the multi-PET topology, the switch SW_{Bi} is not referenced to circuit ground. After the start of the SECE process, when steady-state is achieved, the PET ground is more positive compared to V_{SS} by a voltage magnitude of $|(V_{STO} - V_{SS})/2|$. Hence, even if the switch control signals from the DLC block had a voltage level of $V_{OH(MAX)} = V_{STO}$ and $V_{OL(MIN)} = V_{SS}$ V, it would not have been sufficient to completely turn-off the P-Ch and N-Ch MOSFETs inside SW_{Bi} , when condition (4.1) is encountered.

$$|V_{PET}| \geq \left[(V_{STO} - V_{SS}) / 2 \right] + |V_{TH}| \quad (4.1)$$

where V_{PET} is the peak voltage across the PET and V_{TH} is the threshold voltage of the MOSFETs used. The dual level shifter (DLS) shown in Figure 4.7 serves two purposes: (i) level shifts the output from the DLC block to a higher voltage magnitude in both positive and negative direction, for e.g. -2.5 V – +2.5 V is level shifted to -3.5 V – +3.5 V (ii) chooses the most positive and negative voltage from the two available sources i.e. PET and C_{STO} .

The DLS uses cross-coupled PMOS transistors in the first stage to shift the voltage level in the positive direction and uses cross-coupled NMOS transistors in the second stage to shift the voltage level in the negative direction. Diodes D_0 - $D_{(2j-1)}$ and D'_0 - $D'_{(2j)}$ select the most positive and negative voltages respectively between V'_{STO} and v_{PET} voltages. A 100 Ω resistor is used for limiting the short-circuit current in each branch of the driver circuit when both PMOS and NMOS transistors conduct during a switching event. In the DLS circuit, the MOSFETs are required to switch fast enough to minimize shoot through current and hence low values of Q_g were preferred over $R_{DS(ON)}$ for MOSFETs MP_3 – MP_6 and MN_3 - MN_6 . Besides, MOSFETs with low V_{TH} were selected for complete turn-on at low gate-source voltages (V_{GS}).

4.3.3 Peak Detector (PKD)

An instance of the PKD block shown in Figure 3.7 is used for each PET in the multi-PET topology. The design of the PKD block for the multi-PET architecture is identical to the single-PET case; however, unlike the single-PET topology, the PKD block in this configuration monitors the voltage node shown in Figure 4.9, which provides information regarding the voltage peaks of individual PETs. A non-inverting buffer, U_{25} is used at the output of the PKD block i.e. V_{PKDj} and the buffered output is sent to the DLC block. The change in logic level at the output of

Figure 4.8 Schematic of the peak detector for multiple low-voltage PETs with a non-inverting buffer at the output. The circuit inside the dashed box is replicated for each PET.

Figure 4.9 Schematic showing the node (blue arrow) at which the peak is monitored in a multi-PET system.

Figure 4.10 Schematic of zero crossing detector. An instance of the circuit in the dashed box is required for each additional PET. The signals A_{1-j} originate from the DLC block.

the PKD comparator allows the design of the DLC block to be unaltered from the single-PET version. Sections 3.3.3 and 3.4.2 should be referred to for information related to device selection and simulation of the PKD circuit.

4.3.4 Zero Crossing Detector (ZCD)

The circuit shown in Figure 4.10 is used for zero crossing detection and is identical to the ZCD block used in the single-PET topology; and like the inductor, is shared among multiple PETs in the system. Since the ZCD block needs to be disabled every time a PET is served, shutdown signals from individual PET's DLC block passes through an OR logic before being connected to the ZCD's $\overline{SD}$ pin. The 3-input OR gate shown in Figure 4.10 is implemented using the two 2-input OR gates as shown inside the dashed box (shaded). The OR gates used for the ZCD block are selected from TI's AUP family of logic devices due to the ultra-low standby and switching power needed for operation. Sections 3.3.4 and 3.4.3 should be referred to for information related to device selection and simulation of the ZCD circuit.

4.4 Simulation Results

The simulation setup used for verifying the functionality of the multi-PET BSC block is identical to that of a single-PET BSC topology mentioned in section 3.4.1. However, to simulate a multi-PET BSC, two additional sources with $V_{OC} = 1\text{ V}_{PK}$ were added to the circuit.

Figure 4.11 Plot showing the simulated voltage and current waveforms of the multi-PET BSC circuit. The control signal for SW_{Bi} , i.e. V_{SW} is not shown in the figure.

Figure 4.12 Plot showing simulated power conversion efficiency of the multi-PET BSC circuit corresponding to input voltages ranging from 1 V to 3.5 V

4.4.1 Bi-directional Switching Converter (BSC)

Besides verifying the basic functionality of the BSC block, simulations were done to find the BSC's power conversion efficiency. Figure 4.11 shows the simulated characteristic voltage and current waveforms of the SECE based multi-PET BSC. The waveforms were obtained with the following parameters: $C_{PET} = 530$ nF, $L = 1$ mH ($DCR = 3.4 \Omega$), $C_{1,2} = 2.2 \mu F$, $V_{STO} = 5V$, $V_{OC} = 1 V_{PK}$, and $f_{VIB} = 65$ Hz. Multiple PET operation can be verified by observing the inductor current, which has 3 charge/discharge events in every half-cycle, clearly visible in the zoomed-in plot. The simulated efficiency, η_{sim} of the multi-PET BSC is plotted in Figure 4.12. Only a single PET source was used for plotting the efficiency. The efficiency plot of the multi-PET BSC circuit shows a trend similar to its single-PET counterpart. A peak efficiency of 74.2 % was observed during simulations, which is slightly

Figure 4.13 Plot showing simulated power conversion efficiency of the multi-PET BSC circuit corresponding to input voltages ranging from 1 V to 3.5 V with a 3.3 mH, DCR = 3.2 Ω inductor

higher efficiency compared to the low-voltage BSC case. The higher efficiency can be attributed to the parallel connection of P-Ch and N-Ch MOSFETs in the multi-PET BSC, which lowers the resistance in the path when compared to the series connection of P-Ch and N-Ch MOSFETs in single-PET BSC.

Another set of simulated efficiency curves were plotted with a higher value of inductance i.e. $L = 3.3$ mH (DCR = 3.2 Ω). This is to study the improvement in efficiency obtained when using a large inductance. The simulated efficiency, η_{sim} of the multi-PET BSC using a 3.3 mH inductor is plotted in Figure 4.13. The peak efficiency with a larger inductor has increased to 81 % which is due to the lower conduction losses due to the reduction in peak currents.

The two topologies discussed thus far were optimized for low voltage energy harvesting. It can be observed from their efficiency plot that; the efficiency drops

rapidly when the input voltage increases. Generally, this could be attributed to the increased conduction losses in the input side due to the increase in current. Another reason for the decrease in efficiency can be explained as follows. If the magnitude of the input voltage, $|V_{PET}|$ (after voltage doubling) is greater than $|V_{STO}/2| + V_F$, and the bi-directional switch, SW_{Bi} is turned on, there are two paths for the capacitor, C_{PET} to discharge i.e. (i) directly into the split-capacitors (ii) into the inductor. When part of the charge in C_{PET} discharges into the split capacitor, the charging current is very high, which causes conduction losses in the output diodes. This theory was verified by placing ideal switches in series with the diodes D_P and D_N which helped channel the current into the inductor alone. An efficiency improvement up to 5% was noted. Nevertheless, without the ideal switches, the efficiency was good at low input voltages and at higher input voltages, the efficiency improved as V_{STO} increased.

4.5 Measurement Results

4.5.1 PCB Prototype and Experimental Setup

A double layer Printed Circuit Board (PCB) measuring $50 \times 100 \text{ mm}^2$ in area was fabricated and assembled using off-the-shelf components listed in Table 3.1. The PCB prototype of the smultiple low-voltage PEH system is shown in Figure 4.14. To demonstrate the functionality of the multi-PET system, three off-the-shelf PETs (viz. PET1, PET2, PET3) measuring $90 \times 16.8 \times 0.8 \text{ mm}^3$ in size were used. For the single PEH system, only PET₁ was used for testing. The two active piezoelectric layers on either side of the bimorph cantilever were connected in parallel configuration and wires were soldered to its terminals for connection to the PEH system. Individual PETs were drilled with an M5 sized hole for fixing nuts and bolts, so that the harvester could be tuned to the desired frequency by adding metal washers (refer Figure 3.20). In this way, PET_{1,2,3} were tuned to resonant frequencies of 65, 68 and 70 Hz, respectively. The measured C_{PET} values of

Figure 4.14 PCB prototype of the multi-PET energy harvesting system. The two inductors used for testing are highlighted in red.

Figure 4.15 Waveform acquired using an oscilloscope during start-up. The transition from start-up phase to SECE is visible in the zoomed waveform in the inset.

PET_{1,2,3} were 532 nF, 566 nF and 561 nF, respectively. The experimental setup used for multi-PET topology is similar to that of single-PET (section 3.5.1).

4.5.2 Start-up mechanism and transition to SECE

In Figure 4.15, the start-up circuit can be seen charging a completely depleted 100 μ F capacitor to 2.66 V. The start-up voltage starts to harvest energy from an input voltage as low as 650 mV across the PET. Since the start-up block is similar to the single-PET topology, the principal of operation is not discussed again.

To verify successful operation of the multi-PET PEH system, characteristic waveforms associated with the SECE technique were acquired using an oscilloscope and is shown in Figure 4.16. A 10 Ω resistor was added in between the inductor and PET ground to capture the inductor current waveform, i_L . Oscillations (ringing) are visible at the V_{L+} node of the inductor due to the LC circuit formed between the inductor and the parasitic capacitances at the node.

Figure 4.16 Characteristic voltage and current waveforms of the SECE technique in the multi-PET topology. Channel 4 (pink) shows the SW_{Bi}'s gate control signal.

4.5.3 SECE operation with multiple PETs

The ability of the system to handle multiple PETs is demonstrated here. For testing purposes, each PCB was designed such that more number of PETs can be easily added to the system by stacking one on top of the other as shown in . Only the first PCB was assembled completely with all the components of the system, including

Figure 4.17 Oscilloscope capture showing multiple-PET operation. The frequency of vibration was set to 65 Hz.

the blocks which do not need replication, for e.g. inductor, ZCD, start-up etc. while the remaining two PCBs consists of the components which needed replication, for e.g. SW_{Bi} , PKD, DLS etc. Figure 4.21 shows the input waveforms of the multiple PETs functioning simultaneously. Since the frequency of vibration (65 Hz) used for testing matches the resonant frequency of PET_1 (yellow waveform), it has the highest power output. To demonstrate the merits of the SECE technique when combining multiple PETs, Table 4.1 shows the actual combined power output ($P_{O(1+2+3)}$) of the three-PET system vs expected power output ($P_{O1} + P_{O2} + P_{O3}$). It can be observed that the combined power output is almost equal to the expected power output, which demonstrates the efficiency of combination. The worst-case

Table 4.1 Power Output from Multiple PETs

V_{STO} (V)	P_{O1}	P_{O2}	P_{O3}	Expected $P_{O1}+P_{O2}+P_{O3}$	Actual $P_{O(1+2+3)}$	*Combining Efficiency (%)
2.7	128.8	37	158.5	324.3	322.7	99.5
3.0	132.9	37.8	166.5	337.2	336	99.6
3.5	133	38.5	174.3	345.8	345.5	99.9
4.0	134	38.8	176.8	349.6	348.8	99.8
4.5	135.9	39.2	176.9	352	351	99.7
5.0	137.5	39.5	179	356	350	98.3

*Combining efficiency is the ratio of actual power output to the expected power output. All the values of power given in the above table are in μW .

combining efficiency was found to be 98.3%. The combining efficiency is given by (4.2)

$$\eta_{comb} = \frac{P_{O(1+2+3)}}{P_{O1} + P_{O2} + P_{O3}} \quad (4.2)$$

Combining multiple PETs in this manner is beneficial for broadband operation, however there are certain limits which need to be considered. The maximum number of PETs, j_{max} which can be combined in this manner is given by (4.3), approximated to the lower integer.

$$j_{max} \leq \frac{T_{VIB}}{2(t_{SECE-max} + t_{store-max})} \quad (4.3)$$

where $t_{SECE-max}$ is the maximum time taken for C_{PET} to discharge into L , $t_{store-max}$ is the maximum time taken for L to discharge into C_1 or C_2 . Equation (4.3) does not take into account the delay associated with the control circuits when responding to a peak or zero crossing event and if considered, will further reduce j_{max} .

4.5.4 Intrinsic Power Consumption and Converter Efficiency

The input power, P_{in} into the harvester and the output power, P_o of the BSC block are calculated the same way it was done for the single-PET case. The experimental setup used for measuring output current, I_o in the former topology is reused here and the control circuits were externally powered when calculating the power

Figure 4.18 Measured intrinsic power consumption of the sub-circuit blocks in a multi-PET system. An inductor of 1 mH (DCR = 3.4 Ω) was used during the measurement. The power consumption has been normalized to three sources.

conversion efficiency. All the measurements reported below were taken at an input frequency of 65 Hz.

The major difference between the single-PET and multi-PET system lies in the gate driver circuit used. Single-PET system uses a simplified gate drive and uses off-the-shelf ICs to get the level translation task done. Also, the gate driver needs to drive only two MOSFETs. The multi-PET topology uses the DLS block

Figure 4.19 Standby power consumption of the DLS and LS blocks.

for level shifting and driving the gate of SW_{Bi} . The power consumption of the discretely designed DLS circuit is expected to be high compared to the off-the-shelf level shifter used in the single-PET case. Figure 4.18 shows the intrinsic power consumption of the various sub-circuits in the multi-PET system. The power consumption of the DLS block was found to be 2.5 times that of the level shifter in the single-PET case. However, it can be observed that the power consumption per source in a multi-PET topology is slightly lower than the single-PET case since the miscellaneous power consumption is normalized to three sources. The maximum intrinsic power consumption of the multi-PET system is $13.9 \mu W$ at an output voltage of 5 V. The above value is with the DLS circuit operating at 5 V. However, the power consumption of the DLS circuit is also dependent on the input voltage amplitude. If the input voltage amplitude is more than the V_{STO} voltage, then the DLS circuit draws power from the input. This translates to lower available power

Figure 4.20 Experimental (bottom) vs. simulated (top) efficiency of the multi-PET BSC block. An inductor of 1 mH (DCR = 3.4 Ω) was used during the measurement. The efficiency is plotted for different input voltages, ranging from 1.0 V to 3.5 V.

for harvesting. The standby power consumption of the multi-PET topology is similar to the single-PET case, except for the DLS block which consumes much higher standby-power compared to LS as shown in Figure 4.19. The standby current of the multi-PET system varied from 1.65 μ A to 1.9 μ A when V_{STO} was swept from 2.7 V to 5 V. When the standby-current of the multi-PET system is normalized to the number of sources, the same translates to 550 nA/PET at 2.7 V, which is, to the best of the author's knowledge, one of the lowest reported [5] so far for any discrete SECE implementation.

Both experimental, η_{exp} and simulated efficiency, η_{sim} of the multi-PET BSC block are plotted in Figure 4.20. The efficiency of only a single PET was measured, since the worst-case combining efficiency of the multi-PET system is about 98.3 % and the net efficiency will be constant even with higher number of sources. The calculated peak efficiency of the BSC converter based on voltage and current

Figure 4.21 Experimental (bottom) vs. simulated (top) efficiency of the multi-PET BSC block. An inductor of 3.3 mH (DCR = 3.2 Ω) was used during the measurement. The efficiency is plotted for different input voltages, ranging from 1.0 V to 3.5 V.

Figure 4.22 Measured intrinsic power consumption of the sub-circuit blocks at different output voltages, in a multi-PET system ($L = 3.3$ mH and DCR = 3.2 Ω)

Figure 4.23 Plot showing the variation of efficiency (experimental) w.r.t. the input voltage. The multiple curves are the various efficiency values at different storage voltages.

measurements is about 74.5 %, which is slightly higher than the single PET topology as predicted by simulations.

To understand the effect of the inductance on the power conversion efficiency and intrinsic power consumption, a 3.3 mH inductor with a DCR of 3.2 Ω was used for taking measurements. Both experimental, η_{exp} and simulated efficiency, η_{sim} of the multi-PET BSC block with the new inductor are plotted in Figure 4.21. As expected, the efficiency improves and reaches a peak value of 80%, coherent with simulations. A higher inductance also influences the control circuit's power consumption since the circuits need to stay awake for a longer period of time (t_{SECE}). The power consumption of the control circuit for the multi-PET case with a 3.3 mH inductor is shown in Figure 4.22 and is normalized to three sources. The power consumption of the control circuits increased to 18.5 μ W at $V_{STO} = 5$ V. The 3.3 mH inductor had a volume of 1990 mm³ whereas the 1 mH inductor occupied

Table 4.2 Comparison with Existing Piezoelectric Energy Harvesting Circuits

Parameters	[6]	[7]	[8]	[3]	This work
Technology	Integrated	Integrated	Integrated	Discrete	Discrete
Technique	Rectifier-free SECE	SECE, NVC	SECE, eNVC ^{1,2}	SECE	Rectifier-free SECE
No. of PETs	1	1	5	3	3
Inductance [volume]	160 μ H [27 mm ³]	10 mH [8478 mm ³]	10 mH, 560 μ W [7085 mm ³]	10 mH [2448 mm ³]	3.3 mH [1990 mm³]
Self-Start	No	Yes	Yes	Yes	Yes
Input voltage	Up to 1.2 V	Up to 20 V	Up to 5 V	Up to 20 V	Up to 3.5 V
Output power ³	30 μ W	477 μ W	13.4 μ W	300 μ W	350 μW
Intrinsic power	n.a.	3 μ W @ 3V	144 nW @ 3V	10 μ W @ 3V	10 μW @ 3V
Timing	Preset	Adaptive	Adaptive	Preset	Adaptive
LV Efficiency ⁴	50%	69%	85.3%	62%	80%

¹eNVC stands for Enhanced Negative Voltage Converter. ²Uses two inductors. ³Experimentally demonstrated output power.

⁴Low Voltage Efficiency. n.a = not available.

only 150 mm³. The choice of the inductor in an energy harvesting system is often restricted by space constraints in the end application.

The efficiency vs. V_{STO} plot in Figure 4.21 can also be plotted to show the efficiency variation with the input voltage, V_{PET} and is shown in Figure 4.23. The decrease in efficiency with higher input voltages is due to the higher conduction losses encountered. Since the efficiency of the designed converter is high at low voltages, the proposed converter is suitable for working with low-voltage PETs.

4.6 Comparison with State-of-the-art

The important results of the multi-PET design are compared with state-of-the-art circuits and is consolidated in Table 4.2. The performance results with the 3.3 mH inductor will be used to compare with other state-of-the-art techniques. Also, 0 – 5 V has been set as the ‘low voltage (LV) range’ to compare with the reported works. Efficiency of the state-of-the-art circuits in the low voltage range is compared with the efficiency of the proposed circuit.

The integrated SECE circuit reported in [6] uses the smallest inductor amongst all the compared designs and achieves a peak efficiency of 50 %. However, the design lacked a start-up circuit and required the use of an external negative voltage supply. The timing control for the switches had to be externally fed. The authors in [7] report a self-powered SECE circuit with a peak efficiency of 85 % across its input range of operation which was 0 – 20 V. The design used a 10 mH inductor which was bulky due to the lower DCR. The peak efficiency of the above circuit in the LV range was found to be 69 % [7] at 5 V, corresponding to a P_{in} of 85.3 μ W. The PET used in this thesis provided an equivalent amount of power at 1.6 V. The proposed design has an efficiency of 78 % at 1.6 V with a smaller 3.3 mH inductor, which shows the advantage of using a rectifier-free design. The authors in [8] demonstrate a multi-PET compatible IC with 85.3 % peak efficiency, using a Residual Charge Inversion (RCI) method. However, the design used a 560 μ H inductor for RCI in addition to the 10 mH inductor for the SECE converter. In [3], the authors demonstrate a discrete implementation of an SECE circuit, capable of handling multiple PETs. The design uses a 10 mH inductor. The peak efficiency of the circuit in the LV range was 62 % at 5V, corresponding to a P_{in} of 52 μ W. The PET used in this thesis provided an equivalent amount of power at 1.2 V. The proposed design has a peak efficiency of 78 % at 1.2 V. The volume of all the inductors used in the above works are provided in Table 4.2.

From the above discussion, it can be concluded that the proposed design achieves a high efficiency of 80% in the low voltage range. The efficiency improvement is not by using a larger inductor, but by reducing the conduction losses in the circuit, by using a rectifier-less topology.

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Chapter 5

Rectifier-less Topology for Medium-Voltage Piezoelectric Transducers

This Chapter introduces an SECE based, rectifier-free circuit topology optimized for single medium-voltage piezoelectric transducers. The block level details of the topology are presented followed by the circuit implementation. Simulations are performed to provide an insight into the applicability of the topology for medium-voltage PETs and to arrive at the maximum efficiency achievable using the selected components.

5.1 Introduction

The previous two topologies were focused on low-voltage PETs, and demonstrated a high-power efficiency in the low voltage range ($0.5 \text{ V} < V_{OC} < 1.75 \text{ V}$). The topology presented in this section targets PETs with V_{OC} in the range of $1 - 4 \text{ V}$, which is referred to as ‘medium-voltage range’ in this thesis. The voltage range of the design presented here is only limited by the device breakdown limits, however, high-voltage PETs will not benefit significantly in terms of efficiency by using a rectifier-less scheme.

Figure 5.1 Schematic of charge flow when a medium-voltage PET is connected to a low-voltage PET architecture. Width of the lines with an arrow head (red) is proportional to the current. Only current flow in the positive half-cycle is shown.

The SECE technique requires the inductor, L to be the temporary storage and the output capacitor, C_{STO} to be completely isolated from the PET source. If a PET generates a voltage, V_{SECE} when connected to the SECE circuit shown in Figure 5.1 and the switch, SW_{Bi} is closed, there are three paths through which current flows when condition (4.1) is encountered. Current flowing through the flyback diode directly into the output capacitor leads to lower efficiency of power conversion as discussed previously. The architecture introduced in this Chapter eliminates the above problem through the inclusion of an additional switch.

A basic description of the architecture and its sub-circuit blocks are presented here. The block diagram of the interface circuit for medium-voltage PETs is shown in Figure 5.2. The architecture consists of the following sub-circuit blocks:

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One of the notable differences in this topology is the additional Bi-directional Switch used in the BSC block. While switch SW_{Bi-3} is controlled by a dedicated output from the DLC block, switches SW_{Bi-1} and SW_{Bi-2} are controlled together. An LS block is used for each Bi-directional switch in the BSC block. The proposed architecture is also based on the conventional SECE technique; and hence, the sub-circuits used here are similar, except for the Dead-Time Generator (DTG) block, which is used in this design to avoid shorting of the PET or inductor terminals during normal operation. The PKD and ZCD block serves the same purpose of providing information to the DLC block to determine switching instances of the three switches. Unlike previous topologies, a Start-up block connected between v_{PET} and ground node provides the initial charging path for C_{STO} . The Start-up block is disabled by the Under Voltage Lock Out (UVLO) block once the SECE circuit takes over.

5.3 Circuit implementation of the sub-circuit blocks

Circuit implementation of the sub-circuit block are detailed in this section. Only the sub-circuit blocks which are designed differently for the rectifier-less medium-voltage PET system are discussed in detail below. While the BSC block is drastically different from former topologies, the circuit elements of certain blocks such as the ZCD, PKD and Start-up have been modified for use with the higher input voltage range. Additional glue-logic such as latches are added between certain blocks to enhance the reliability during operation.

5.3.1 Bi-directional Switching Converter

Figure 5.3 shows the schematic of the BSC block used in the medium-voltage PET topology. The output side of the proposed topology consists of the split capacitors – C_1 , C_2 , unidirectional switches – S_1 and S_2 and switches – SW_{Bi-1} , SW_{Bi-2} , SW_{Bi-3} . All the bi-directional switches used in this design are referenced to the PET

Figure 5.3 Schematic of the medium voltage BSC using ideal switches.

Figure 5.4 Schematic of the medium voltage BSC using Schottky diodes and MOSFETs.

ground. Switches, S_1 and S_2 are implemented using Schottky diodes D_P and D_N . Bi-directional switches, $SW_{Bi-1,2,3}$ are implemented using series connected N-Ch and P-Ch MOSFETs as shown in Figure 5.4.

5.3.1.1 Stages of operation

There are four stages of operation in the medium-voltage BSC block as shown in Figure 5.5. Following section describes the different stages of operation of the BSC circuit.

Figure 5.5 Stages of operation of the medium-voltage BSC. Stages 1 and 2 are part of the positive half-cycle, whereas stages 3 and 4 are part of the negative half-cycle. Dashed lines with arrow heads indicate direction of current flow.

- **Positive half-cycle**

When the sinusoidal voltage v_{PET} reaches a positive peak value, SW_{Bi-1} and SW_{Bi-2} are closed, and the charge in C_{PET} starts to discharge into the inductor, L . When C_{PET} is completely discharged, the current i_L in the inductor reaches a positive peak value, and SW_{Bi-1} , SW_{Bi-2} are opened. Charge recycling takes place among the three capacitors at the output. This is to balance the charge imbalance from the previous operating stage (stage 4).

In stage 2, the inductor tries to maintain the flow of current through it by lowering the voltage at V_{L+} node, facilitating i_L to flow through L - D_P - C_1 path and charging C_1 in the process. Since the output capacitor C_{STO} and C_2 are in parallel to C_1 , they also get charged in the process.

- **Negative half-cycle**

When the sinusoidal voltage v_{PET} reaches a negative peak value, SW_{Bi-1} and SW_{Bi-2} are closed and the charge in C_{PET} starts to discharge into the inductor L . When C_{PET} is completely discharged, the current i_L in the inductor reaches a negative peak value and SW_{Bi-1} , SW_{Bi-2} are opened. Charge recycling takes place among the three capacitors at the output. This is to balance the charge imbalance from the previous stage (stage 2). This completes Stage 3 of the converter operation.

In stage 4, the inductor tries to maintain the flow of current through it by raising the voltage at V_{L+} node, facilitating i_L to flow through L - D_N - C_2 path and charging C_2 in the process. Since the output capacitor C_{STO} and C_1 are parallel to C_2 , they also get charged in the process. Charge recycling takes place in the next stage, i.e. stage 1.

5.3.2 Dead-Time Generator

The time required to turn on and turn off a MOSFET is determined by the driving capability of its preceding gate driver stage and the MOSFET's Total Gate Charge, Q_g . The higher the value of Q_g , longer is the time spent in charging/discharging the MOSFET's gate capacitance and hence turning it on/off. In the proposed topology, Bi-directional switches, $SW_{Bi-1,2}$ need to be turned on and SW_{Bi-3} needs to be turned off simultaneously. However, there is a certain amount of time during which neither of the switches are completely turned on or off due to the gate charging delay and other delay elements in the signal path. A single control signal and its inverted version from the DLC block could lead to the turning on of $SW_{Bi-1,2}$ and SW_{Bi-3} at the same instance. The PET source and the inductor could get short-circuited momentarily, at the onset of the inductor charging phase and the inductor discharging phase, respectively, losing energy in the process. To avoid such a

Figure 5.6 Schematic showing the Dead-Time Generator circuit.

scenario, a certain amount of ‘dead-time’ is embedded in the control signal from the DLC block, during which none of the MOSFETs conduct. The dead-time is used during the turn-on and turn-off of the switches and is generated using a non-overlapping clock generator circuit shown in Figure 5.6. The delay is determined by the RC delay of resistor, R_{DT} and capacitor, C_{DT} used in the circuit. The control signal (INP) from the DLC block is fed to the input of the inverter, I_1 and the AND gate, A_1 . The inverted signal, X , passes through the $R_{DT}C_{DT}$ network and is delayed at node Y . Schmitt trigger inverter, I_2 , generates a delayed version of the original control signal at node Z . The Schmitt trigger allows to have a dead-time for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions at the input. Assuming an initial output of $OUT2 = OUT1 = 0$ and an input transition from $0 \rightarrow 1$, $OUT1$ switches state to 1, only after the arrival of the delayed control signal, whereas $OUT2$ switches state earlier, when INP toggles from $0 \rightarrow 1$. However, for a $1 \rightarrow 0$ input transition, a more delayed version is produced at $OUT2$ and a less delayed version at $OUT1$.

5.3.3 Peak Detector

The principle of peak detection used in the proposed topology is the same as the low-voltage case i.e. using a delayed version of the input voltage. The node, v_{PET} used for monitoring the voltage peak is shown in Figure 5.7. Node V_{L+} cannot be

Figure 5.7 Schematic showing the node (blue arrow) at which the peak is monitored in a medium-voltage PET system.

used for monitoring the peak, since the ground path to the PET is cut-off by SW_{Bi-1} when the switch is open. For reliable peak-detection when PET is in open-circuit condition, SW_{Bi-3} needs to be normally closed. SW_{Bi-3} is opened after a peak is detected and before $SW_{Bi-1,2}$ are closed to avoid short circuiting the PET source. In comparison to the previous two topologies, the peak detection in the medium-voltage topology is challenging due the floating PET source during the dead-time when none of the switches conduct. The floating voltage at the v_{PET} node causes the output of the PKD comparator to toggle inadvertently, affecting the reliability of the SECE operation. To eliminate this problem, a gated latch was added to the output of the comparator to hold its state when the DTG block issues a turn-off signal to SW_{Bi-3} . The latch becomes transparent again when a turn-on signal is issued to SW_{Bi-3} after the charge in C_{PET} is completely discharged into the inductor L . Since the PKD block connects to the BSC block at node v_{PET} , an inversion in logic is required at its output to maintain compatibility with the input of the DLC block. The inversion is achieved by using $\bar{Q}$ of the latch as the output of the PKD block.

Figure 5.8 Schematic of the peak detector for medium-voltage PETs with a gated latch at the output.

Figure 5.9 Schematic of the zero-crossing detector for medium-voltage PETs with a gated latch at the output.

5.3.4 Zero Crossing Detector

The ZCD block used in the proposed design has a shutdown ($\overline{SD}$) input which is asserted for most part of the circuit's operation causing the output of the circuit to be in a high impedance state, most of the time. However, during the short duration when ZCD is enabled, node V_{L+} experiences voltage swings above and below the

Figure 5.10 Schematic showing the (a) current flow in the positive half-cycle through the start-up JFET (b) Under Voltage Lock Out circuit.

PET ground, when the node comes out of a floating state, causing the output of the ZCD comparator to oscillate. A gated latch is used at the output of the ZCD block to prevent the oscillating signals from reaching the DLC block. The output signal, OUT2 from the DTG block is used for controlling SW_{Bi-1,2} and is also used for enabling the comparator and the latch. Though the ZCD comparator is enabled instantaneously when OUT2 goes high, the latch is made transparent only after a certain delay to allow settling of the voltage at the V_{L+} node. A delay of 100 ns was chosen in this design based on simulations. A Schottky diode, D_{FD} is connected in parallel to the 100 Ω resistor for fast discharge at the inputs of gates A₄ and A₅, facilitating rapid shutdown of the ZCD comparator, saving power.

5.3.5 Start-up and Under Voltage Lock Out

The Start-up block consists of a P-Ch JFET, J₁ in parallel with SW_{Bi-1} for providing the initial conduction path when C_{STO} is discharged below the threshold voltage required for SECE operation. The P-Ch JFET is a normally-ON device and is turned off by a positive voltage between its gate and source terminals. If the gate of the P-Ch JFET were directly driven by a CMOS output, the gate would experience a voltage lower than its source voltage causing excessive leakage through the gate.

Hence, the gate is driven by a 3-state buffer with an OE signal instead of a CMOS output. Figure 5.10(a) shows the current flowing through the Start-up JFET and charging C_{STO} during the positive half-cycle.

Figure 5.10(b) shows the schematic of the Under Voltage Lock Out block. The UVLO block consists of a Voltage Monitoring (VM) IC which disables the rest of the sub-circuit blocks when $V_{STO} < V_{PRE-} = 2.63V$ and enables them when $V_{STO} > V_{PRE+} = 2.66V$. The OE signal generated by the VM IC is used to enable or disable the buffer driving J_1 's gate.

5.4 Simulation Results

Simulations were done using OrCAD PSpice v16.6 using device models obtained from their respective manufacturers. Simulation models for all the circuit elements used in the BSC and Start-up blocks were available; however, simulation models for components such as logic gates, flip-flops, VM ICs etc. used in other blocks were unavailable. OrCAD's in-built library includes 74ACT series logic gates and flip-flops which were used in lieu of the intended low-power gates (TI's AUP logic family) for simulating the overall circuit. It needs to be noted that, only the functionality of the sub-circuits can be verified using the 74ACT logic gates and an estimation of the power consumption will lead to exaggerated values, typical of the ACT family when powered by a 5 V supply. Simulations have been done based on the device parameters of Mide Technologies' PPA-1001 piezoelectric transducer with $C_{PET} = 100$ nF, $f_{VIB} = 65$ Hz and V_{OC} varying between 1.15 V and 4 V ($V_{PET} = 2.3$ V – 8 V).

5.4.1 Bi-directional Switching Converter

Simulations are performed to verify the functionality and to understand the power conversion efficiency of the BSC block. Input power, P_{in} which goes into the PEH system is given by (5.1),

Figure 5.11 Plot showing the simulated efficiency of the medium-voltage PET BSC circuit. The efficiency is plotted for input voltages ranging from 2.3 V_{PK} to 8.0 V_{PK} with a 1 mH, DCR = 3.4 Ω inductor.

$$P_{in} = C_{PET} V_{PET}^2 f_{VIB} \quad (5.1)$$

A PET with $C_{PET} = 100$ nF feeds the same amount of power into the PEH system at a $V_{PET} = 2.3$ V and $f_{VIB} = 65$ Hz, which a PET with $C_{PET} = 530$ nF would feed at a $V_{PET} = 1$ V and $f_{VIB} = 65$ Hz. The range of 1.15 V to 4 V was chosen as a means of comparison between the power conversion efficiencies of the medium-voltage topology and the low-voltage topology. The simulated efficiency, η_{sim} of the medium-voltage BSC is plotted in Figure 5.11. It can be observed that, compared to the other two topologies, the medium-voltage topology does not have an efficiency drop for input voltages above $(V_{STO} - V_{SS})/2 + |V_{TH}|$ since the current does not split when C_{PET} is connected to L . A peak efficiency of 79% was achieved at an input voltage, $V_{PET} = 2.3$ V with a 1 mH (DCR = 3.4 Ω) inductor. It is worth noting that for the same amount of P_{in} , the medium-voltage BSC shows a higher peak efficiency of 79 % compared to the efficiencies achieved by the other two topologies for the same inductance value. The reason for this behavior can be

Figure 5.12 Plot showing the input, outputs and intermediate signals of the DTG block for a (a) 0 → 1 transition of the INP signal (b) 1 → 0 transition of the INP signal.

attributed to the lower conduction losses incurred when the same input power is supplied at a higher input voltage (lower current). The general trend of efficiency improvement with an increment of the V_{STO} voltage can be observed in the medium-voltage plot as well.

5.4.2 Dead-Time Generator

The simulated waveform of the DTG circuit (Figure 5.6), when INP transitions from 0 → 1 and 1 → 0 is shown in Figure 5.12(a) and Figure 5.12 (b), respectively. The input signal to the circuit was generated using a pulse generator with a rise/fall time = 100 ns, frequency = 130 Hz and pulse width = 16 μ s. A frequency of 130 Hz

Figure 5.13 Plot showing the start-up waveforms in the medium-voltage PET topology.

was selected for this purpose since the Bi-directional switches are triggered twice during a signal period. The dead-time with $R_{DT} = 200 \, \Omega$ and $C_{DT} = 1 \, \text{nF}$ was found to be 400 ns (T_{ON-DT}) when INP toggles from $0 \rightarrow 1$ and 100 ns (T_{OFF-DT}), vice-versa. The best power conversion efficiency of 79 % was achieved with the above configuration. The efficiency deteriorated with decreasing dead-time values. The dead-time is strong function of the propagation delay of the logic gates, which in turn is dependent on the supply voltage. However, in the proposed design, since logic gates are powered by the output of a 2.5 V LDO, the dead-times can be expected to stay within acceptable bounds.

5.4.3 Start-up

The Start-up circuit in Figure 5.10 was simulated using a 1.75 V_{PK} voltage at the PET output. The capacitors C1-C2 were set to 100 nF and C_{STO} was set to 1 μF to reduce the simulation time. The gate of J₁ was left floating at the start of the simulation and could charge the output capacitor to 3.3 V at simulation the end of 1 s simulation time. The drain current through the JFET, I(J1) and the V_{STO} voltage can be observed in the waveform shown in Figure 5.13. The gate of J₁ was driven to the V_{STO} voltage of 3.3 V externally at 1 s to cut-off the start-up circuit. I(J1) is

Figure 5.14 Plot showing the simulated characteristic SECE waveform of the medium-voltage PET system. The voltage is measured across the PET device.

instantaneously cut-off and the V_{STO} voltage starts to drop. During the off period of the JFET, the ac voltage can be seen across its Drain-Source terminals. $I(J1)$, at this instance was measured to be less than 40 nA. J1's gate is left in its initial floating condition at the end of 2 s of simulation time and after a slight delay of 200 ms, current starts to flow through the J1, bringing the voltage across its Drain-Source terminals to less than 200 μ V. In a practical implementation, the driving signal for J1 would originate from the UVLO block.

5.4.4 PEH System

The functionality of the BSC block was simulated previously using ideal gate drive signals and externally set timing pulses. The circuit achieved a power conversion efficiency of 79 % with a 1 mH inductor. In this section, the entire PEH system is simulated using the sub-circuits for which device models are available. The simulation parameters are as follows: $V_{STO} = 5$ V, $V_{PET} = 3.5$ V, $f_{VIB} = 65$ Hz, $T_{ON-DT} = 400$ ns and $T_{OFF-DT} = 100$ ns. The characteristic voltage waveform of the SECE circuit can be seen in Figure 5.14 along with the outputs of the latched PKD and ZCD sub-circuits. INP is the output of the DLC block and sets the turn-on time of the bi-directional switches in the system. For the present system, the turn-on

time was found to be 16 μ s with $L = 1$ mH and $C_{PET} = 100$ nF which is approximately equal to the value provided by (2.2).

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Chapter 6

Conclusion and Future Work

This chapter collates the most important outcomes of this research work and discusses its effectiveness in meeting the qualities of a desirable piezoelectric energy harvesting system. Certain general points to consider when evaluating the merits of a design are provided. The chapter ends by suggesting a few plausible improvements to the system as a future work.

6.1 Conclusion

The rectifier-less, SECE based technique presented here focuses on reducing the power losses in the input rectifier and achieves better efficiency even when using a small sized inductor. The other technique proposed in this thesis, aims to combine multiple transducers to harvest energy from broadband vibrations.

Chapter 1 began by introducing the need for incorporating energy harvesting into the electronic devices of the future. The power density and the various issues related to ambient energy sources such as light, heat, and motion were discussed, which pointed to the need for highly efficient interface circuits. The motivation for choosing piezoelectricity as the transduction mechanism for harvesting vibrational energy was explained.

An exhaustive literature review of the conventional and state-of-the-art systems was presented in Chapter 2. Desirable features of a piezoelectric energy harvesting system were deduced based on existing literature. Some of the key features are high efficiency with low standby power consumption, autonomous and battery-free operation. Besides, it's also desirable to have a system which can operate from a wide range of vibrations. SECE, which is one of the many non-linear processing methods, was identified as a potential technique, capable of achieving the above objectives.

Chapter 3 introduced an SECE based rectifier-free architecture targeting single piezoelectric transducers. The trade-offs considered during the device selection process have been explained in detail. The functionality of the sub-circuit blocks and the efficacy of the topology were validated through simulations and was found to have a peak power conversion efficiency of 74 %. The measured efficiency of 73 % obtained using a commercial piezoelectric transducer with the fabricated PCB prototype corroborates the simulation results obtained.

Chapter 4 extended the single low-voltage PET topology to multiple PETs with the objective of broadband operation. The multi-PET operation was verified by combining three commercially available PETs tuned to different but close resonant frequencies. The system achieved a peak power conversion efficiency of 81 % and 80 % during simulations and experiments, respectively.

Chapter 5 introduced a medium-voltage PET topology for devices generating slightly higher voltages than the low-voltage devices. The topology was validated through circuit simulations and was found to have a peak power conversion efficiency of 79 % even with a 1 mH inductor (3.4Ω DCR).

A few things to consider while comparing the merits of a particular topology is the tradeoff between power efficiency, intrinsic power consumption and solution size. Efficiency which comes at the expense of increasing the inductance affects the size of the solution adversely. Techniques which focus on maximizing the power conversion efficiency by keeping the solution size at a minimum are pragmatic, when considering the fact that target application of most energy harvesting circuits are tiny sensor nodes. When using techniques such as SECE, where the circuits are only awake during the period when energy is transferred, a large inductance leads to higher intrinsic power consumption. There is a critical point of inductance beyond which, increasing the same would adversely affect the efficiency. In discrete implementations, the critical value would be reached at a lower value of inductance due to the relatively higher intrinsic power consumed.

The main considerations during component selection were the tradeoffs between speed and power consumption for comparators, conduction losses and switching losses for MOSFETs, reverse leakage current and forward voltage drop for Schottky diodes. Emphasis was given on reducing the standby power consumption of the control circuits, which will go a long way in ensuring that the load does not run out of power, when ambient vibrations are absent. The system

design is notable by the presence of a start-up circuit which provides battery-free operation.

When compared to other discrete implementations which report high efficiencies with large inductors [1], [2] or more than one inductor [3], the circuit presented here offers superior power conversion efficiency using small inductors. The standby power consumption was measured to be only around 550 nA/PET for the multi-PET topology and to the best of the author's knowledge, it is one of the lowest reported thus far [4]. All the measurements were taken using commercially available PETs. The multi-PET based PEH system was able to harvest the peak energy from individual transducers. Careful system-design ensured that the harvesting process in one PET did not affect the other PETs in the array.

In conclusion, the three autonomous PEH systems with peak efficiencies in the range of 73 – 80 % for low to medium voltages have been demonstrated. Due to the SECE technique employed, the system operates at its maximum power point without the need for impedance matching. The PEH systems draw an ultra-low standby power and the multi-PET version is capable of broadband operation as well. Hence, this work has been successful in meeting the desirable features of a PEH system mentioned in section 2.5.

6.2 Future Work

Besides SECE, there are other non-linear techniques such as S-SSHI, P-SSHI, DSSH and the recent energy injection schemes can extract much higher energy from the PET source. Though there are discrete implementations of the same, the present designs not suitable for low voltage PETs. This area can be explored further since higher energy extraction from tiny PETs is particularly attractive.

The system presented here used only PETs. However, combining the same with a different type of source such as a Radio Frequency (RF) harvesting coil would lead to a heterogeneous system which opens new avenues for harvesting energy. Since

voltage generated in the RF coil is alternating in nature, it could benefit from the same rectifier-free design. This could be a potential research direction. Due to the low levels of energy available from RF coils, a thorough study needs to be done to ensure that a self-powered discrete system would still lead to a positive power budget. Alternatively, an integrated solution may be pursued.

A discrete implementation offers several advantages over an integrated solution in terms of development time and cost. However, integrated solution reduces the PCB real estate and is more economical in volume production. MEMS based PETs are known to generate low voltage outputs [5] and are compatible with CMOS processes. The rectifier-free topologies presented here are very generic and a chip implementation can benefit PETs fabricated using MEMS process.

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List of Publications

Conference Publications

- [1] **A. Shareef**, W. L. Goh, Y. Gao, S. Narasimalu, “Synchronous Electric Charge Extraction for Low Voltage Piezoelectric Energy Harvester Array,” *2016 International Symposium on Integrated Circuits (ISIC)*, Singapore. (Dec 2016)

Journal Publications

- [2] **A. Shareef**, W. L. Goh, S. Narasimalu, Y. Gao, “A Rectifier-less AC-DC Interface Circuit for Ambient Energy Harvesting from Low Voltage Piezoelectric Transducer Array”, *IEEE Trans. Power Electron.* (Submitted, Oct 2017)
- [3] **A. Shareef**, W. L. Goh, S. Narasimalu, Y. Gao, “Synchronous Electric Charge Extraction based Rectifier-less AC-DC topologies for low-voltage Piezoelectric Transducers”, *IEEE Trans. Circuits Syst. II* (In Submission)