A study on complementary resistive switching characteristics in resistive random access memory for next-generation non-volatile memory technology

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**NANYANG
TECHNOLOGICAL
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SINGAPORE

**A STUDY ON COMPLEMENTARY RESISTIVE
SWITCHING CHARACTERISTICS IN RESISTIVE
RANDOM ACCESS MEMORY FOR NEXT-
GENERATION NON-VOLATILE MEMORY
TECHNOLOGY**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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GENERATION NON-VOLATILE MEMORY
TECHNOLOGY**

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ABSTRACT

Resistive random access memory (RRAM) has shown the potential to become the future universal memory. The novel concept of complementary resistive switching (CRS) provides the promise of a high-density, selector-less RRAM crossbar array implementation, free of the sneak-path current problem. This thesis mainly focuses on the device fabrication and investigations of the CRS mechanism, the CRS current-conduction mechanism, the self-compliance set switching (SCSS) mechanism, the CRS stability, as well as the CRS read voltage window in HfO_x -based RRAM devices, for the implementation of high-performance RRAM devices with stable and reliable CRS.

CRS has been demonstrated in the $\text{TiN}/\text{HfO}_x/\text{IL}/\text{TiN}$ device, where a bottom interfacial layer (IL) resulted from the oxidation of TiN during the device fabrication. No CRS was observed in the $\text{TiN}/\text{HfO}_x/\text{Pt}$ device where the formation of the bottom IL was suppressed by the inert Pt metal. It is found that the IL between the metal electrode and switching oxide plays an important role in enabling stable CRS in the HfO_x -based single memory device. The physical switching model, based on oxygen-ion exchange between the bottom/top IL and the conductive path in HfO_x , is proposed to be the cause of the CRS observed in the $\text{TiN}/\text{HfO}_x/\text{IL}/\text{TiN}$ device.

The current-conduction mechanism analysis reveals that Schottky emission is a dominant conduction mechanism of the high resistance state (HRS) in both bipolar resistive switching (BRS) and the CRS mode due to the same top/bottom TiN/HfO_x interface in the symmetric $\text{TiN}/\text{HfO}_x/\text{TiN}$ resistive memory device. Low resistance state (LRS) current conduction can change from semiconducting (at low voltages) to metallic (at high voltages) conduction. In the former regime, conduction may be described by a

farthest-neighbor tunneling process, characterized by a trap spacing of ~ 8.3 Å along the conduction path. On the other hand, the latter is characterized by a metal-like mechanism with a positive temperature coefficient like that of a sputtered Hf metal film. Field-induced lowering of the tunneling barrier (~ 77 meV due to the collapsed HfO_x conduction band edge and the small trap spacing) is proposed to have caused the transition to a metal-like conduction. Due to the opposite temperature dependence of the two conduction regimes, existence of a zero temperature-coefficient of LRS resistance has been observed.

A complementary switch exhibiting SCSS can provide a pathway towards an implementation of truly selector-less crossbar memory array. SCSS has been realized in resistive memory devices with a series oxide layer incorporated into the memory stack. The series oxide acts as an in-built resistor, limiting the increase of the current during set transition. In this study, we show that SCSS is also present in the $\text{TiN}/\text{HfO}_x/\text{Pt}$ device without a series oxide layer. However, substitution of the TiN electrode by Pt eliminates the SCSS behavior. We propose that oxygen ions drifting from the ruptured part of the filament towards the TiN anode tend to accumulate at the TiN interface during set transition due to a low density of nitrogen vacancy in our nearly stoichiometric TiN electrode. Oxygen accumulation can give rise to an increase in the resistance of HfO_x at the TiN interface, which can partially compensate for the decrease of the filament resistance, and an increase in the effective work function of TiN, which can offset part of the applied electric field, resulting in a lower net electric field across the filament.

Our study on the CRS of $\text{TiN}/\text{HfO}_x/\text{TiN}$ memory devices found an unusually high occurrence of a self-reset behavior, i.e. the device is automatically programmed into the high resistance state during forming. This is observed in the following opposite-polarity voltage sweep, in which the device exhibits a set behavior (instead of a reset typically

observed in bipolar switching mode). However, the self-reset behavior is (1) suppressed in devices with a thin Al_2O_3 layer inserted in-between the TiN and HfO_x ; (2) completely eliminated in devices where the TiN cathode is replaced by Pt. It is shown that the IL at the HfO_x/TiN interface plays a crucial role in enabling CRS, via an oxygen exchange process with the adjacent conducting filament formed in the HfO_x . The self-reset behavior can be ascribed to the migration of oxygen ions from the cathode interfacial oxide into the conducting filament in the HfO_x during the forming transient, thus resulting in the disruption of the filament. With the reduction in “voltage loading” across the cathode interfacial oxide during the forming transient in devices with the Al_2O_3 interlayer and the elimination of interfacial oxide in devices with the Pt cathode, the occurrence of the self-reset behavior is reduced or eradicated.

Our study also shows that a large percentage of the TiN/ HfO_x /TiN RRAM device fails to exhibit CRS after forming. These devices exhibit a large non-polar reset loop in the first post-forming voltage-sweep measurement. It is proposed that breakdown of the TiN/ HfO_x interfacial oxide layers (crucial in enabling CRS) and the accompanied formation of Ti filaments (due to Ti migration from the TiN cathode into the breakdown path) take place, resulting in CRS failure and the observed non-polar reset behavior. Our proposition is supported by the significant reduction or complete elimination of the large non-polar reset and the CRS failure in devices with a thin Al_2O_3 layer incorporated at the TiN-cathode/ HfO_x or both TiN/ HfO_x interfaces. The higher breakdown field of the thin Al_2O_3 enables it to withstand the forming voltage (upon filament formation in the main oxide) until the forming process is interrupted. With the integrity of the barrier oxide layer ensured, stable CRS can be achieved.

An approach that may lead to a significantly improved CRS voltage window and read margin is presented. The approach is leveraged on the inherent asymmetry in the

O-ion exchange process between interfaces involving different reactive metal electrodes to enlarge the difference between the set and reset voltages. The proof-of-concept is successfully demonstrated for the ITO/HfO_x/TiN resistive memory structure, yielding a positive CRS voltage window of 1.6 V and a read margin of 1.1 V. These results represent a significant improvement over the respective window and margin of 0.5 V and 0.1 V achieved on the TiN/HfO_x/TiN stack and other single devices reported to-date, and address a major challenge of array-level CRS implementation using HfO_x RRAM on both rigid and flexible substrates. The improvement may be attributed to a decreased set voltage due to the greater tendency for O ion to migrate from the adjacent ruptured filament into the ITO and an increased reset voltage due to an opposing Volta potential arising from the larger work function of ITO.

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LIST OF ABBREVIATIONS

ALD	atomic layer deposition
BE	bottom electrode
BRS	bipolar resistive switching
BSE	backscattered electrons
CBRAM	conductive bridging RAM
CC	current compliance
CCD	charge-coupled device
CF	conductive filament
CMOS	complementary metal-oxide semiconductor
CRS	complementary resistive switching
DUT	device under test
DRAM	dynamic random access memory
EBL	electron-beam lithography
ECM	electrochemical metallization
EDX	energy dispersive X-ray spectroscopy
EELS	electron energy-loss spectroscopy
FESEM	field emission Scanning electron microscope
FeRAM	ferroelectric random access memory
HRS	high resistance state
IL	interfacial layer
ITO	indium tin oxide
LRS	low resistance state
MIM	metal-insulator-metal
MRAM	magneto-resistive random access memory
NVM	non-volatile memory
PCRAM	phase-change random access memory

RIE	reactive ion etching
RRAM	resistive random access memory
SCSS	self-compliance set-switching
SE	secondary electrons
SEM	scanning electron microscope
SMU	source monitor unit
SRAM	static random access memory
TCM	thermochemical metallization
TCR	temperature coefficient of resistance
TE	top electrode
TEM	transmission electron microscopy
TEOS	tetraethyl orthosilicate
VCM	valence change memory
XPS	x-ray photoelectron spectroscopy

LIST OF SYMBOLS

d	trap spacing
ξ	applied electric field
μ	micro
q	electronic charge
qn	electronic charge density
β	temperature coefficient
ρ_{sh}	sheet resistance
$\emptyset$	work function
φ	work function
φ_{B}	barrier height
E_{a}	activation energy
E_{a0}	zero-field activation energy
E_{f}	Fermi level
E_{B}	binding energy
E_{K}	kinetic energy
E_{p}	X-ray photons energy
I - V	current-voltage characteristic
J - V	current density-voltage characteristic
R	probe-contact resistance
T_0	reference temperature
V_{o}	oxygen vacancy
ν	thermal vibration frequency

Chapter 1 INTRODUCTION

1.1 Background

1.1.1 Emerging non-volatile memory technology

Advancement in modern information technology requires the development of faster, denser and less energy-consuming non-volatile memory (NVM). Over the past decades, Si-based flash-memory technology has dominated the NVM industry due to its high density and low fabrication costs. However, the main disadvantage of flash memory is its severe performance degradation with the further scaling of tunnel oxide [1]. Since stored electrons in the floating gate can tunnel through thin tunnel oxide more easily via the traps-assisted-tunneling process after a considerable number of program/erase cycles, which can create traps in the tunnel oxide, this leads to deteriorative data loss. To overcome the problems of current NVM concepts, the development of non-charge-based next-generation NVM is therefore essential for the extension of Moore's law over the next few decades [2]. Although a variety of novel memory concepts have been recently explored, most of the proposed memory concepts cannot compete with current flash-memory technology [3-6]. The emergence of new technology for industry applications, the scalability of the technology, the speed of the devices, power consumption, endurance, densities better than existing memories, and most importantly the costs, have to be taken into consideration. If the emerging technology possesses only one or two of these attributes, then it can, at most, be used for some niche applications. Some emerging non-volatile memory technologies are introduced in the following part.

Magneto-resistive random access memory (MRAM) or magnetic RAM was first developed by IBM in the 1970s [7], but was not greatly developed. MRAM stores data

using magnetic-storage elements instead of the electrical charges used by dynamic random access memory (DRAM) and static random access memory (SRAM) technologies [8]. The storage elements consist of two ferromagnetic plates separated by a thin insulating tunnel barrier, shown in Fig. 1.1 [9]. One of the two plates is a permanent magnet set to a particular polarity, but the other one is changeable to match that of an external field to store memory. The different memory states can be realized by changing the orientation of the magnetic moments, and hence the resistance in the magnetic layer upon application of a magnetic field. The memory state of the cell is sensed by measuring the electrical resistance while passing a current through the cell. Because of the magnetic tunnel effect [10], if both magnetic moments are parallel to each other, then the electrons will be able to tunnel and the cell will be in a low resistance state. However, if the magnetic moments are antiparallel, the cell resistance will be high. The memory characteristics of MRAM for writing and erasing are shown when a current is passed through the write line to induce a magnetic field across the cell. MRAM has a high read/write speed, unlimited endurance, and low power usage when compared with DRAM. However, the device requires a large unit cell size, and has big problems with size reduction. Additionally, the power consumption required to write data is three to eight times higher than that required to read data. Currently, as one of the emerging non-volatile memory technologies, MRAM has attained some level of commercial success in niche applications. Spin-transfer torque RAM, or STT-RAM, is an MRAM, but with better scalability than traditional MRAM [11, 12]. The STT is an effect where the orientation of a magnetic layer in a magnetic tunnel junction or spin valve can be modified using a spin-polarized current. Spin-transfer torque technology has the potential to be incorporated into MRAM devices, combining low current requirements

and reduced cost. However, the amount of current needed to reorient the magnetization is, at present, too high for most commercial applications.

Fig. 1.1: (a) A schematic MRAM cell array structure. (b) A typical single-cell structure of MRAM, where different memory states are denoted by the orientation of the magnetic moments in the two ferromagnetic plates. “0”: magnetic moments are parallel to each other; “1”: magnetic moments are antiparallel to each other [9].

Ferroelectric random access memory (FeRAM), which is similar to DRAM in terms of device structure and operation, but uses a ferroelectric layer, instead of a dielectric layer, to achieve the non-volatile memory characteristic. In a DRAM cell, the data need to be refreshed periodically due to the discharging of the capacitor, whereas FeRAM can maintain the data without any external power supply [13]. It achieves this by using a ferroelectric material in the place of a conventional dielectric material between the plates of the capacitor. When an electric field is applied across the ferroelectric material, it will be polarized, and when that field is removed, the material will be depolarized. But the ferroelectric material can retain its polarization, exhibiting the polarization hysteresis. A typical FeRAM cell structure and its polarization hysteresis characteristic are illustrated in Fig. 1.2 [8]. FeRAM is the most common type of personal computer memory, with the ability to retain data when the power is turned off, similar to other non-volatile memory devices such as ROM and flash memory.

FeRAM has attained a level of commercial success, with the first devices released in 1993 [14]. FeRAM exhibits the very promising characteristics of a fast switching speed (< 20 ns) and a very robust switching endurance ($> 10^{14}$) [15]. It is expected to have many applications in small consumer devices such as personal digital assistants, handheld phones, power meters, smart cards, and security systems. However, the read operation of the FeRAM cell is destructive. The device also has inherent problems in terms of scalability.

Fig. 1.2: A schematic of the typical cell structure of FeRAM and its polarization hysteresis characteristic [8].

Phase-change random access memory (PCRAM) is also a type of nonvolatile random access memory. The resistance switching property of PCRAM is based on reversible phase conversion between the amorphous and crystalline state of chalcogenide glass [16, 17], which is accomplished using localized joule heating and heat quenching processes. A low resistive crystalline state or high resistive amorphous state is obtained by controlling the stress duration. This utilizes the unique behavior of chalcogenide, whereby the heat, produced by the passage of an electric current, causes the material to switch between two states. The different states have different electrical resistances which can be used to store data. However, the device suffers from fatigue

failure due to the frequent expansion and contraction of the switching material during the heating and quenching process. Also, the heating requires a high power consumption. A typical PCRAM structure is shown in Fig. 1.3 [18]. One cell is in a low resistance crystalline state, while the other in a high resistance amorphous state.

Fig. 1.3: A schematic cross-sectional diagram of two PRAM memory cell: a low resistance crystalline state (the left cell), and a high resistance amorphous state (the right one) [18].

In recent years, resistive random access memory (RRAM), that utilizes electrically switchable resistance of a metal-insulator-metal (MIM) structure, has attracted considerable research attention due to its simple MIM structure, good complementary metal-oxide-semiconductor (CMOS) compatibility, and ease of scalability [19-23]. Transitions between resistance states in RRAM devices are achieved by adjusting the applied external electrical field, due to the hysteretic resistance behavior of the switching material. Considering the competition with current mainstream memory technology, the ultimate RRAM for next-generation NVM applications should exhibit a number of good electrical characteristics [21]: (1) High resistance ratio: If RRAM devices can be cost-competitive with flash memory, a R_{OFF}/R_{ON} ratio of larger than 10 is required for a small and highly efficient sense amplifier; (2) Fast write/read operation: It is desirable

for the write voltage pulse (t_{wr}) to be less than 100 ns in order to outperform flash memory. The length of read voltage pulses (t_{rd}) should be shorter as compared to t_{wr} or at the least in the order of t_{wr} ; (3) Low energy consumption: Write voltages (V_{wr}) should be smaller than a few volts to outperform the current flash memory which suffers from a high programming voltage. A significantly smaller read voltage (V_{rd}), when compared to V_{wr} , is required so as to prevent a change in the resistance during the read operation; (4) Good endurance and retention: RRAM should provide at least 10^7 write/read cycles in order to outperform the current flash memory, which has a maximum number of write cycles of around 10^7 . A data retention time (t_{ret}) of more than 10 years, normally examined during an accelerated stress condition with a thermal stress of up to 85 °C and a small constant voltage stress, is required for a universal NVM.

In fact, Hickmott et al. first reported the hysteretic resistance switching in Al/Al₂O₃/Al MIM structure in 1962 [24]. A first period of high research activity was up to the mid-1980s. During this period, the resistance switching behavior was observed in a variety of materials such as BeO, TiO, and NbO, in their MIM configuration [25-27]. The current period of the research activity was started by Asamitsu et al. in the late 1990s [28-30]. After being intensively researched, RRAM showed great promise to be a universal NVM. Continuous improvements and in-depth investigations in both the materials and electrical switching mechanisms have demonstrated a breakthrough in the performance of RRAM [2, 19, 23, 31-50]. Some very promising switching materials such as HfO_x, TaO_x, widely used in modern CMOS fabrication technology, have been intensively studied in RRAM memory structures [35, 41, 42, 51-54]. A conductive-filament (CF) RRAM device with a cell size of 10 nm x10 nm (further dimension scaling of the RRAM device is possible because resistive switching is based on the connection and rupturing of a localized CF) and a switching energy per bit of less on 0.1 pJ has

been reported [55]. Although many studies have shown a slower reset speed than set speed, an average transition time of around 1 ns has been achieved [56]. A cycling number of greater than 10^{12} cycles has been successfully demonstrated by some researchers [35]. All these advantages show that RRAM is the most promising candidate for the next-generation NVM. When compared with the current main memory products, shown in Table 1.1 below, RRAM has shown great potential for commercialization and production.

Table 1.1 Performance comparison of RRAM with current main memory products [57].

	SRAM	DRAM	Flash NAND	Flash NOR	<u>RRAM</u>
Non-volatile	No	No	Yes	Yes	Yes
Cell size (F^2)	≈ 50	≈ 6	≈ 6	≈ 10	≈ 4
Multi-Level-Cell (MLC)	No	No	Yes	Yes	Yes
Write/Erase time	1 ns to 100 ns	50 ns / 50 ns	1 μ s / 0.1 μ s	1 μ s / 10 μ s	< 1 ns
Endurance (number of Write/Erase cycles before failure)	10^{16}	10^{16}	10^5	10^5	$> 10^{13}$
Write current	low	low	very high	very high	low (< 10 mA)
Voltage required	1 V	1.35 V to 1.5 V	3.3 V to 5 V	1.7 to 3.6 V	< 1.5 V
Complexity of 3d integration	high	high	high	high	low

1.1.2 Sneak-path current problem in the crossbar RRAM array

There is much hope that RRAM can be used for crossbar memory array implementations via back-end-of-line interconnect integration, enabling the fabrication of higher-density memory fabrication. However, a major issue for RRAM application in crossbar memory arrays is the sneak-path current [58]. Parasitic currents flowing through neighboring cells in the LRS can interfere with the read/write operation performed on a designated cell, leading to data corruption.

A common method by which this problem may be circumvented is to connect a rectifying selector device, such as oxide diode, a threshold switch, or transistor, in series with the RRAM cell to block the parasitic current [54, 59-64]. However, this comes at

the expense of increased front-to-back-end integration complexity and reduced memory density.

An alternative approach is found in the concept of complementary resistive switching (CRS) [58]. In the CRS approach, two RRAM cells are connected anti-serially such that when one of the RRAM cells is programmed into the LRS, the other will be programmed into the HRS. In this way, the parasitic current associated with a cell in the LRS is suppressed. As the integration of a different rectifying element is not required, this approach is deemed more attractive and has attracted considerable interest lately. But the CRS proposed requires a complex fabrication process and has a common active internal electrode that quickly degrades.

The integration complexity may be reduced by the introduction of CRS in a single memory device. Good results have been obtained by testing a single RRAM cell [41, 65-72], providing a promising outlook that the sneak-path problem may eventually be solved based on the study of just a single RRAM cell.

1.2 Motivation

When compared with flash memory, which is the most widely used NVM nowadays, but consumes more power due to current leakage and requires a complex fabrication process, RRAM is regarded as an ideal candidate for the next-generation NVM due to its simple MIM structure, good CMOS compatibility, and ease of scalability. The advantages of the RRAM cell are: (a) low transition power consumption; (b) high operation speed; (c) good repeatability and endurance; and (d) superior scalability.

There is much promise for RRAM to be used in crossbar memory array via back-end-of-line interconnect integration. CRS offers the promise of a high-density selector-less RRAM crossbar array implementation free of the sneak-path current problem. As

the integration of a selector is not required, CRS in RRAM devices has been intensively investigated. Good results have been obtained in a single RRAM cell, which provide the promising outlook that the sneak-path problem may eventually be solved based on just a single RRAM cell.

However, the underlying mechanism of CRS in oxide-based RRAM devices is not clear. Although different resistive switching models have been proposed to explain the observed CRS in oxide-based RRAM devices based on different oxide-stacks, there is a lack of a universal physical model. The understanding of the mechanism is necessary for the creation of a high-performance RRAM with stable and controllable CRS.

Numerous studies on the nature of the conduction mechanisms of traditional bipolar resistive switching in oxide-based RRAM devices have been performed. There has been a lack of investigation on the current-conduction mechanism of CRS in oxide-based RRAM devices. In addition, there still has been a lack of studies on stability of CRS. Moreover, CRS in reported RRAM devices shows a narrow read voltage window, limiting its real-life applications in next-generation NVMs. A study on improving the CRS voltage window and read margin is needed.

1.3 Objectives

The aim of this research paper is to study the CRS characteristics in the HfO_x -based RRAM device for next-generation NVM technology applications. The objectives are listed below:

- To study the physical mechanism of CRS in the HfO_x -based RRAM device, and to propose a universal physical model to clarify the underlying mechanism of CRS in the oxide-based RRAM device.

- To study the current-conduction mechanism of CRS in the oxide-based RRAM device.
- To reveal the origin of self-compliance set-switching (SCSS) in the RRAM device without a series oxide layer.
- To reveal the self-reset behavior, and to study the CRS stability in the oxide-based RRAM device. The interface-engineering method is explored to achieve a stable and controllable CRS.
- To explore an approach that improves the narrow read voltage window of CRS in the oxide-based RRAM device.

1.4 Organization of thesis

This thesis is divided into seven chapters, organized as follows:-

- *Chapter One* highlights the background, motivation, objectives and original contributions of the research.
- *Chapter Two* presents the literature review of the resistive switching mode and mechanism, and the traditional methods and different implementations of CRS to solve the sneak-path current problem in the RRAM crossbar memory cell array.
- *Chapter Three* presents the device fabrication for the CRS study, and the physical and electrical characterizations of the HfO_x-based RRAM device.
- *Chapter Four* presents a study of the physical mechanism of CRS. The role of the interfacial layer in CRS is investigated. The current-conduction mechanism of CRS is also studied. In addition, the physical mechanism of SCSS in the RRAM device without a series oxide layer is investigated.
- *Chapter Five* investigates the self-reset behavior during forming. A set behavior, instead of a reset typically observed in bipolar resistive switching is observed in the following

opposite-polarity voltage sweep after forming. A large, non-polar reset and the subsequent failed CRS after forming are also studied. CRS performance improvement by interface engineering optimization is presented.

- *Chapter Six* presents a new approach, leveraging on the inherent asymmetry in the O-ion exchange process, between the switching layer and the different reactive metal electrodes, to enlarge the difference between the set and reset voltages, which may lead to a significantly improved CRS voltage window and read margin.
- *Chapter Seven* presents the conclusion of this thesis and makes recommendations for future research works.

1.5 Original contributions

The major contributions of this research paper lie in a systematic study of CRS in HfO_x-based RRAM device in terms of resistive switching mechanism, current conduction mechanism, interface engineering, and the switching operation voltage window. The study offers a very promising outlook for the implementation of a high-density selector-less RRAM crossbar array, free of the sneak-path current issue. The original contributions are listed below:

- We show that CRS is observed in the TiN/HfO_x/TiN device, while no CRS is observed in the TiN/HfO_x/Pt device. The role of the IL between the metal electrode and switching oxide in enabling CRS in the HfO_x-based RRAM device is revealed. The physical switching model, based on an oxygen-ion exchange between the conductive path in the HfO_x switching layer and the bottom/top IL, is proposed to have caused the CRS observed in the TiN/HfO_x/TiN device.
- The current-conduction mechanism study demonstrates that Schottky emission is a dominant conduction mechanism of HRS in both the BRS and CRS mode. On the

other hand, we reveal a transition from semiconducting (at low voltages) to metallic (at high voltages) conduction in the LRS for the BRS for the first time. Semiconducting conduction may be attributed to a farthest-neighbor, trap-assisted tunneling process in the low-voltage regime. Field-induced lowering of the tunneling barrier is proposed to have caused the transition to a metal-like conduction in the high-voltage regime. A near-zero temperature-coefficient of the LRS resistance is revealed because of the opposite temperature dependence of the two conduction regimes.

- We show the SCSS in the TiN/HfO_x/Pt device without a series oxide layer. However, no self-compliance behavior is observed when the TiN electrode is replaced by Pt or when it is enriched with Ti. A new mechanism is proposed that oxygen accumulation at the TiN interface during set transition, due to a low density of nitrogen vacancy in our nearly stoichiometric TiN electrode, creates a barrier, which self-arrests the increase of the set switching current. Our results show interface engineering as a possible route for enabling SCSS in a RRAM device without the need for a complicated stack structure. This finding may be useful to the development of selector-less oxide-based RRAM device for flexible and/or transparent electronics applications.
- A new self-reset behavior during forming is reported in this research paper. After forming, the device shows a set behavior, instead of a reset one typically observed in the bipolar resistive switching. This behavior may be attributed to the migration of oxygen ions from the cathode IL into the conducting filament in HfO_x during the forming transient, thus resulting in the disruption of the filament. This hypothesis is supported by the fact that self-reset behavior is suppressed in devices with a thin Al₂O₃ layer inserted in-between the TiN and HfO_x due to the reduction in “voltage

loading” across the cathode interfacial oxide during the forming transient, and completely eliminated in devices with the TiN cathode replaced by Pt because of the elimination of interfacial oxide.

- Our study shows the majority (70%) of TiN/HfO_x/TiN devices exhibits a large, non-polar reset loop in the first post-forming voltage-sweep measurement, and following the failed CRS. This abnormal resistive switching behavior is ascribed to the breakdown of the TiN/HfO_x interfacial oxide layer and the accompanied formation of Ti filaments due to Ti migration from the TiN cathode into the breakdown path. This proposition is supported by the significant reduction or complete elimination of the large non-polar reset and the CRS failure in devices with a thin Al₂O₃ layer incorporated at the TiN-cathode/HfO_x or both TiN/HfO_x interfaces.
- We present a new approach that may result in a significantly improved CRS voltage window and read margin. This approach is leveraged on the inherent asymmetry in the O-ion exchange process between the HfO_x switching layer and the top/bottom reactive metal electrodes to enlarge the difference between the set and reset voltages. We successfully demonstrate a positive CRS voltage window of 1.6 V and a read margin of 1.1 V in the ITO/HfO_x/TiN RRAM device. These results represent a significant improvement over the respective window and margin of 0.5 V and 0.1 V achieved by the TiN/HfO_x/TN stack and other single devices reported to-date. This demonstration addresses a major challenge of array-level CRS implementation using HfO_x RRAM on both rigid and flexible substrates.

Our research works have been published in peer reviewed journals and established international conferences, such as the *Applied Physics Letters (APL)*, *IEEE Electron Device Letters (EDL)*, *Journal of Physics D: Applied Physics (JPD)*, *Solid States*

Devices and Materials (SSDM) symposium, and International Memory Workshop (IMW).

Chapter 2 LITERATURE REVIEW

2.1 Introduction

This chapter is divided into three main sections, excluding the introduction and summary sections, to systematically review the different types of resistive switching, past efforts and current methods to address the sneak-path current issue, faced in the crossbar RRAM cell arrays, by various research groups. Section 2.2 reviews the classification of RRAM device operation, in particular the resistive switching mechanism of RRAM devices. Section 2.3 reviews the traditional solutions to the sneak-path current issue in the crossbar memory cell array. Section 2.4 reviews the new CRS concept to solve the sneak-path current issue in RRAM cells.

2.2 Resistive random access memory (RRAM)

The ultimate NVM should exhibit characteristics such as high density, low cost, fast write/read speed, low energy operation, and high performance in terms of endurance (write/read cycles) and retention. Today, Si-based flash-memory devices represent the most dominant NVM because of their high density and low fabrication costs. However, flash memories suffer from low endurance and low write speed, and require a high voltage for write operations. In addition, further scaling in the cell size to increase the density of flash memory, is expected to be approaching the physical limits in the near future. To overcome the obstacles of current NVM technology, a large number of alternative memory concepts are proposed. MRAM [10] and FeRAM [13] supply only niche markets for some special applications due to an inherent problem in their scalability, i.e., achieving the same density as flash memories today. RRAM has shown

the potential to become the future universal memory, due to its fast switching time ($\sim$ ns), low switching energy ($\sim$ pJ), and high write endurance ($\sim 10^{12}$ cycles) [19, 21, 35, 36, 73-76]. This section will cover the classification of RRAM device operation, in particular the interesting resistive switching mechanism of RRAM device.

2.2.1 Classification of resistance switching mode

Before we provide an overview of the different resistive switching mechanisms of RRAM devices, we need to distinguish between the two resistance switching modes with respect to the operating electrical polarity, by which RRAM can be classified into four types: unipolar, bipolar, nonpolar, and complementary.

The physical mechanism of unipolar switching is usually regarded as the Joule heating effect, and thus the switching procedure is independent of the polarity of the operating voltage. A typical unipolar resistive switching of RRAM devices is shown in Fig. 2.1.

Fig. 2.1: A typical unipolar resistive switching of Pt/HfO_x/Pt RRAM device. During the forming/set operation, a current compliance (CC) is generally required to prevent the hard breakdown of the device. Reset happens at a higher current.

Immediately after electroforming, a positive voltage can reset the device to a HRS from the previous LRS. A subsequent voltage-sweep with the same polarity as that in the reset can switch the device to the LRS again. During the set operation, a current

compliance (CC) is generally required to prevent the hard breakdown of the device. A reset happens at a higher current, but a lower voltage below the set voltage.

In contrast, the physical mechanism of bipolar switching is usually interpreted as the redox reaction and electrochemical migration. In our work, bipolar resistive switching is interpreted as the redox-reaction process where the set and reset processes occur at the opposite operating voltage polarity. The resistive switching is totally dependent on the operating voltage polarities. An electroforming process is normally required so that the subsequent resistive switching effect can be observed. Fig. 2.2 shows the typical current-voltage characteristics of bipolar resistive switching: either negative-voltage reset/positive-voltage set (Fig. 2.2(a)) or positive-voltage reset/negative-voltage set (Fig. 2.2(b)).

Fig. 2.2: A typical bipolar resistive switching of TiN/HfO_x/TiN RRAM device. (a) negative-voltage reset/positive-voltage set; (b) positive-voltage reset/negative-voltage set.

Nonpolar resistive switching [77, 78] is the coexistence of unipolar and bipolar switching, as presented in Fig. 2.3. Nonpolar resistive switching, in effect, can be referred to as a particular unipolar switching, which occurs symmetrically under both positive- and negative- voltage polarities. In the nonpolar-switching mode, set-reset processes can be achieved by positive-positive (Fig. 2.3(a)), positive-negative (Fig. 2.3(b)), negative-positive (Fig. 2.3(c)), and negative-negative (Fig. 2.3(d)) voltage

polarities. Similar to unipolar switching, the reset always happens at a higher current, but a lower voltage below the set voltage.

Fig. 2.3: Nonpolar resistive switching behavior of Pt/MgO/Pt RRAM device: the coexistence of unipolar and bipolar resistive switching. (a) Unipolar (positive set/positive reset), (b) bipolar (positive set/negative reset), (c) bipolar (negative set/positive reset), and (d) unipolar (negative set/negative reset) resistive switching [78].

Additionally, a new resistive switching mode is proposed as CRS [58]. In this switching mode, set-reset processes can occur at the same or opposite voltage polarity. Repeatable bipolar switching can occur, however, unipolar set-reset process can happen only one time. CRS is triggered once unipolar set-reset process is finished by extending the voltage sweep for the set process, as shown in Fig. 2.4 [79]. The negative reset/positive set bipolar switching mode can be switched to the positive reset/negative set bipolar switching mode by extending the positive-set voltage. The switching mode can be changed back to previous one only by extending the negative-set voltage sweep.

Fig. 2.4: Current-voltage curves depicting (a) bipolar set/reset; (b) CRS. The latter is triggered by extending the voltage sweep for the set process. Arrows show the directions of the voltage sweep [79].

2.2.2 Resistive switching mechanism

A large number of physical phenomena can induce the non-volatile resistive switching memory effects, as summarized in Fig. 2.5 [21]. Only three main memory effects related to the redox processes in the memory cell are covered in this section. The first one is the electrochemical metallization memory effect (ECM) [80], which relies on an electrochemically active metal electrode. The conductive filaments are formed by the drift of the highly mobile metal cations in the ion-conducting layer upon the application of an external voltage, setting the memory cell to the “ON” state. The dissolution of these filaments can happen when the opposite polarity of the voltage is applied to the memory cell, resetting the cell to the “OFF” state. The second class is the thermochemical memory effect (TCM) [81]. The unipolar resistive switching characteristic is usually observed based on this effect which relies on current-induced temperature change. The third class is the valence change memory effect (VCM) [82], which is based on the migration of anions, and takes place in some specific transition metal oxides. The section will provide a detailed introduction to these three memory effects.

Fig. 2.5: Classification of the resistive switching effects for non-volatile memory applications [21].

2.2.2.1 Electrochemical metallization memory effect (ECM)

RRAM based on the ECM effect is also well known for being a conductive bridging (CB) RAM. An ECM memory cell typically involves an electrochemically active metal such as Ag or Cu, an electrochemically inert counter-electrode such as Pt or Au, and a solid-electrolyte thin-film such as amorphous selenide and sulfide, sandwiched between both electrodes. The resistive switching relies on the electrochemically active metal's electrodeposition and dissolution. Fig. 2.6 shows a typical current-voltage (I-V) characteristic of an Ag/Ag-Ge-Se/Pt ECM cell and the basic operation principle [83]. The migration of active metal cations takes place when a positive voltage is applied to the active metal electrode. These metal cations drift through the solid-electrolyte thin film towards the inert counter-electrode. A subsequent cathodic electrodeposition reaction of the metal cations occurs at the inert counter electrode. Metal filaments grow towards the direction of the active metal electrode (Fig. 2.6A) until a conductive path is generated, and the cell is switched to an "ON" state (Fig. 2.6B). The cell remains in the

“ON” state unless an opposite voltage polarity is applied and the electrochemical dissolution of the metal filament occurs (Fig. 2.6C), resetting the cell to its initial “OFF” state (Fig. 2.6D).

Fig. 2.6: Typical current-voltage (I-V) characteristic of an Ag/Ag-Ge-Se/Pt electrochemical memory cell. Resistive switching processes in the different stages are shown in the insets (A to D). During the set switching, a current compliance of 25 mA (a dashed line) is applied to the cell [83].

In another ECM system, an electroforming process is typically required before the reproducible resistive switching can be obtained. A typical system is the Cu/SiO₂/Pt ECM cell where the Cu-doped amorphous SiO₂ thin film is created by an electroforming process [84]. In this case, the insulating amorphous SiO₂ thin film for the fast ion transport does not contain any electrochemically active metal cations. The electroforming procedure is required to incorporate mobile metal ions into the insulating thin film. The electroforming process may also induce the nano-morphological changes in the insulating thin-film matrix due to the formation of the first metallic filament, which may play a role of a transport channel for all the subsequent resistive switching.

2.2.2.2 Thermochemical memory effect (TCM)

Several types of electrically controlled resistive switching rely on thermal memory effects. In this section, we only cover thermochemical switching that shows a unipolar switching characteristic. This phenomenon is usually observed in some specific transition metal oxides. Resistive switching is initiated by a filamentary thermal breakdown of the switching oxide leading to the formation of a conductive channel between the electrodes. During the set switching, a weak conductive filament with a controlled resistance is created by supplying a set current compliance. The current compliance is released during the reset process, so that the rupture of the conductive filament takes place thermally again. One of the prominent candidate materials is NiO [81]. Fig. 2.7 exhibits a typical unipolar I-V characteristic of a Pt/NiO/Pt memory device [21, 85]. A forming process with a current compliance of 1 mA is required to enable the subsequent resistive switching. A following voltage sweep can lead to the occurrence of a reset at a lower voltage but at a higher current, by releasing the current compliance. The set process occurs at a voltage far below the forming voltage, with a current compliance of 0.5 mA lower than that in the forming process.

Fig. 2.7: Unipolar current-voltage (I-V) characteristics of a Pt/NiO/Pt memory device with a current compliance of 1mA, and 0.5 mA for the forming, and all subsequent set processes, respectively [21, 85].

2.2.2.3 Valence change memory effect (VCM)

Resistive switching of a memory cell based on the valence change memory effect can be classified as filamentary-type or interface-type, in terms of the type of conducting path, as distinguished in Fig. 2.8 [34, 86-89]. Filamentary-type resistive switching can be attributed to the formation and rupture of conductive filaments in an insulating switching oxide (Fig. 2.8 A). This resistive-switching mechanism can be related to both unipolar and bipolar switching behavior. For unipolar resistive switching, thermal redox at the metal electrode/switching oxide interface is regarded as the driving mechanism behind the formation and rupture of the filaments. In contrast, the electrochemical migration of oxygen ions (or oxygen vacancies) is considered to be the driving mechanism behind bipolar resistive switching [34]. Interface-type resistive switching originates from the field-induced change of the Schottky-barrier at the interface between the metal electrode and the oxide (Fig. 2.8 B). This resistive-switching mechanism is usually associated with the bipolar resistive switching observed in semiconducting perovskite oxides [88, 89].

Fig. 2.8: Proposed models for resistive switching, based on the valence change memory effect, can be classified as either (a) a filamentary conducting-type [86, 87], or (b) an interface-type [88, 89].

The difference between the filamentary- and interface-type resistive switching can be understood by studying the area dependence of the cell resistance. Interface-type switching cells usually show an obvious dependence of the device resistance on the

electrode area, because this switching happens homogeneously over the entire electrode area.

2.3 Conventional solutions to the sneak-current issue in crossbar memory cell arrays

The sneak-path current is considered to be a major problem for the RRAM application in crossbar memory arrays. A variety of methods have been utilized to solve this problem by connecting a rectifying selector device, such as oxide diode [54], a transistor [59], or a threshold switch in series with the RRAM cell to block the sneak current. Also, self-rectifying RRAM [90] has been developed to suppress this parasitic current. In the subsequent section, we will give a detailed introduction to these common methods.

2.3.1 One diode/one RRAM (1D/1R) method

The oxide diode was first proposed as the select device to suppress the sneak-path current in crossbar memory arrays. Lee et al. [54] reported a 2-stack one-diode/one-RRAM (1D/1R) cross-point structure for high-density RRAM applications, as shown in Fig. 2.9, where oxide diodes are used as switch elements. However, the demonstrations have been essentially limited to the single-device level, and actual array-level operations where many cells are written then read out together have remained elusive. Even though a number of approaches have been proposed to address the sneak-current problem using diodes as the select device, diodes made from crystalline materials are not suitable for low-temperature fabrication, while those made from low-temperature materials suffer from performance and reliability issues. In terms of memory performance, the increase

of read/write voltage and the degradation of memory stability are considered key concerns for future 1D/1R structure. Also, the current density of the diode is an important factor affecting its scaling limitation due to the dependence of current transport of many resistive switching materials on area. Furthermore, integrating a rectifying diode increases the complexity of the fabrication process and, thus, the cost. Besides performance and integration issues, it has been noted that nanoscale diodes may lose their rectifying behavior below 50 nm due to the increased tunnelling current. In addition, the 1D/1R structure is only compatible with unipolar switches that can be turned on or off using just positive programming voltages. In this case, the serially connected diode can remain forward-biased during programming to prevent voltage loss for the resistive memory device. The 1D/1R approach is inapplicable for bipolar resistive switches, which require a negative bias voltage to switch off the device. These disadvantages of the 1D/1R approach make addressing crosstalk a difficult challenge particularly for the proposed high-density memory and logic systems.

Fig. 2.9: Schematic diagram of a 2-stack 1D-1R memory cell with totally reversed layers. Two cells share the same bit line [54].

2.3.2 One Transistor/one RRAM (1T/1R) method

The sneak-current problem can be addressed by integrating a select transistor at each node of the memory cell, which can decouple those memory cells if they are not addressed. Wang et al. [59] demonstrated a 1T/1R architecture consisting of TiN/Ni/HfO₂/n⁺ Si RRAM cells built on vertical gate-all-around (GAA) Si nano-pillar transistors, as illustrated in Fig. 2.10. However, this 1T/1R approach also came at the expense of increased front-to-back-end integration complexity and reduced memory density.

Fig. 2.10: (a) Schematic diagram of 1T-1R architecture. RRAM (TiN/Ni/HfO₂/n⁺ Si) device is directly built on top of the vertical gate-all-around Si nano-pillar (NP). (b) A high-resolution TEM image showing the 1T-1R device structure. The inset is a TEM image of the memory cell [59].

2.3.3 Self-rectifying RRAM

Self-rectifying RRAM has been proposed to have a pronounced rectifying effect in the LRS, so sneak-current issue can be alleviated without serially connecting an external diode. Tan et al. [90] demonstrated a self-rectifying RRAM based on NiSi/HfO_x/TiN device structure, as shown in Fig. 2.11. The device shows a high forward/reverse rectifying ratio of more than 10³ (reading voltage of ± 0.5 V) in the LRS. Because of the self-rectifying effect, the memory cell can significantly minimize misreading in the matrix crossbar memory, without extra rectifying diodes. But, similar to the 1D/1R structure, the self-rectifying RRAM can only exhibit unipolar switching behaviour,

which can be a difficult challenge for high-density memory and logic systems applications.

Fig. 2.11: (a) Schematic self-rectifying RRAM structure. (b) Typical current-voltage (I-V) curves of NiSi/HfO_x/TiN RRAM device [90].

2.4 Complementary resistive switching (CRS) concept to solve sneak-current issue in RRAM cell

A new concept of complementary resistive switching (CRS) [58] in RRAM devices was proposed where memory states are distinguished by two different high resistance states (HRS), i.e. all the memory cells are in the HRS, so that no sneak-path current issue takes place in the RRAM crossbar array. CRS offers the promise of a selector-less crossbar array, free of the sneak-path problem. CRS was first implemented in a RRAM device with two anti-serially back-to-back connected conductive bridging memory cells sharing a common electrode where memory cell A, consisting of a Pt top electrode, a GeSe solid electrolyte, and an oxidizable Cu bottom electrode, is merged with a memory cell B with a totally reversed material order and current-voltage characteristic, such that when one of the RRAM cells is programmed into the LRS, the other will be programmed into the HRS [58]. After a program operation, the overall device always shows a high resistance, thus avoiding the presence of parasitic current during the successive reading

operation. Fig. 2.12 [58] shows the schematic device structure and typical CRS characteristics of this memory device. Such a device can be switched from HRS (1) to the HRS (2) upon an application of sufficiently large positive-voltage (V_{reset}) to the top Pt electrode, and switches back from HRS (2) to the HRS (1) under an opposite voltage-bias ($-V_{\text{reset}}$). For the reading operation a voltage higher than the set voltage is needed to turn on both cells.

As the integration of a different rectifying element is not required, this approach is deemed more attractive and has attracted considerable interest. CRS characteristics also have been widely reported in oxide-based RRAMs. In the following section, we will introduce different ways that this kind of memory device can be realized.

Fig. 2.12: (a) Schematic device structure of a complementary switch and (b) CRS characteristics of this memory device [58].

2.4.1 CRS in two symmetric memory-cell-integrated RRAM device

Lee et al. [91] reported CRS in the oxide-based RRAM device with two symmetric memory cells with the inverse material order, i.e. Pt/ZrO_x/HfO_x/metal/HfO_x/ZrO_x/Pt. Fig. 2.13 shows the conventional bipolar resistive switching characteristics of each memory cell before the back-to-back connection, and the complementary resistive-switching of the merged RRAM device after the back-to-back connection of two

memory cells. The switching mechanism was attributed to oxygen exchange between the ZrO_x and HfO_x oxides.

Fig. 2.13: (a) Bipolar resistive-switching characteristics of Pt/ZrO_x/HfO_x/BE (the left one) and BE/HfO_x/ZrO_x/Pt (the right one) memory cells before back-to-back connection. (b) Typical complementary resistive switching of merged RRAM device after back-to-back connection of these two memory cells [91].

2.4.2 CRS in two asymmetric memory-cell-integrated RRAM device

A RRAM device integrating two of the same type of memory cells usually exhibits the fixed operation voltages, thus limiting the operation voltage windows. Daeseok et al. [92] reported CRS in a RRAM device, consisting of two asymmetric memory cells, i.e. a W/ZrO_x/HfO_x/TiN and TiN/Ir/TiO_x/TiN memory cell, which can enlarge the operation voltage window. Fig. 2.14 schematically shows the CRS concept of this RRAM device. The HfO_x-based memory device shows a positive-set and negative-reset resistive-switching characteristic; in contrast, the TiO_x-based memory device exhibits a negative-set and positive-reset resistive-switching characteristic. Moreover, both memory devices have a larger reset voltage than the set voltage. In this way, an asymmetric CRS behavior in the merged RRAM device can be achieved due to the superimposed current-voltage characteristics of the two memory cells, leading to a wide voltage-operating window in the positive-bias region.

The voltage-operating window refers to the read voltage region where both memory cells are in the LRS. A dramatic current change usually happens when the erasing operation is performed in a symmetric RRAM device. However, the current does not decrease dramatically in the asymmetric RRAM device due to the significant difference between the set and reset voltages of each memory cell (i.e. the set voltage of the HfO_x -based ReRAM is obviously smaller than the reset voltage of the TiO_x -based ReRAM), so that the operation voltage window is enlarged.

Fig. 2.14: (a) Bipolar (positive set and negative reset) resistive switching characteristics of HfO_x -based RRAM device. (b) Bipolar (negative set and positive reset) resistive switching characteristics of TiO_x -based RRAM device. (c) Typical complementary resistive switching of merged RRAM device after back-to-back connection of these two memory cells [92].

2.4.3 CRS in a single memory device

The realization of CRS in the RRAM device with two anti-serially connected memory cells requires a complex device-fabrication process. These devices also suffer

from the fast degradation of their common active internal electrode. The integration complexity may be reduced by the introduction of CRS in a single memory device. Nardi et al. [71] have showed CRS in the single memory device with the TiN/HfO_x/TiN structure (Fig. 2.15 (a)). The temperature- and field-accelerated ion migration mechanism was proposed to explain the observed CRS behaviour, as shown in Fig. 2.15(c). In this mechanism, excess Hf and oxygen vacancies are considered as conductive species to form CF within the HfO_x layer after forming (A). These conductive species are accumulated near the top electrode (TE) to generate a depleted gap close to the bottom electrode (BE) after a negative reset (A → B). Under a small positive voltage sweep with a current compliance, ions migrate from the TE side towards the BE side to replenish the depleted gap, inducing the CF reconnection (B → C or B → A). The extension of the positive voltage sweep results in the formation of a depleted gap near the TE, due to ions further migrating toward the BE, finally leading to the reset (C → D). A reverse transition happens, upon the application of a subsequent negative voltage sweep (D → C). The researchers suggested that the necessity of the symmetric device structure enables CRS behavior. CRS behavior could only be observed in devices with a uniform Hf concentration profile within the HfO_x active layer, which allows for a fully symmetric nonpolar-RRAM device. No CRS could be observed in devices with a non-uniform Hf concentration profile, which breaks the symmetry of the device structure. As a result, the CRS operation disappeared.

Fig. 2.15: (a) Current-voltage (I-V) characteristics of symmetric TiN/HfO_x/TiN RRAM device with a uniform Hf concentration across the HfO_x layer, showing a complementary resistive switching (CRS). (b) Asymmetric TiN/HfO_x/TiN RRAM device with non-uniform Hf concentration across the HfO_x layer (Hf-rich, close to the bottom electrode, see inset) shows no complementary resistive switching behavior. The necessity of a symmetric structure for CRS is evidenced. (c) Schematic explanation of the switching transition from bipolar switching (BS) to unipolar switching (US) through CRS [71].

However, Yang et al. [65] also have reported the CRS in Pd/Ta₂O_{5-x}/TaO_y/Pd memory cells, where the functional layer was purposely designed with two different stoichiometric TaO_x layers: an oxygen-rich layer and an oxygen-deficient layer. Fig. 2.16 shows the CRS behavior and schematic resistive switching process of this device. The researchers attributed the CRS to the exchange of oxygen vacancies between the two layers with the different oxygen composition upon application of external electric field.

Fig. 2.16: (a) Complementary resistive switching (CRS) characteristics of the single Pd/Ta₂O_{5-x}/TaO_y/Pd RRAM device. (b)-(e) Schematic illustration of CRS processes of this device, corresponding to the four different resistance states (1-4) in (a), respectively. The different resistance states are determined by the internal V_O distributions in the Ta₂O_{5-x} and TaO_y layers [65].

In an earlier study [93], CRS was also observed in the Pt/TiO₂/TiO_{2-x}/Pt device with an asymmetric distribution of oxygen vacancies in the active layer. The CRS was attributed to the transformation of electrical transport behavior between the Pt and switching oxide, due to the changing of concentration of oxygen vacancies at the interfaces. The accumulation of oxygen vacancies at the interface transforms the wide bandgap oxide into an electrically conductive doped semiconductor, which in turn transforms the interface contacts from Schottky-like (low oxygen vacancy concentration) to Ohmic (high oxygen vacancy concentration) upon the application of a negative voltage to the TE, and vice-versa, as shown in Fig. 2.17.

Fig. 2.17: Schematic illustration of complementary resistive switching (CRS) of Pt/TiO₂/TiO_{2-x}/Pt RRAM device. Positively charged V_Os drift toward or away from the Pt/TiO_{2-x} interface, resulting in CRS, which depends on the V_O distribution and the applied voltage polarity. A high concentration of vacancies at the metal-semiconductor interface (Pt/TiO_{2-x}) produces an essentially Ohmic contact, whereas a low concentration of vacancies yields a Schottky-like contact (Pt/TiO₂) [93].

2.5 Summary

Flash memory, which is dominating the current NVM industry, suffers from severe performance degradation with the scaling-down of memory cells. Emerging memory concepts compete with the current flash memory. RRAM has shown the potential to become the future universal memory. The typical resistive switching behavior and resistive switching mechanism behind the oxide-based RRAM device were briefly introduced.

An overview of the traditional methods and the new concept of CRS to suppress the sneak-path current in the RRAM crossbar array for high-density memory integration was presented in detail. CRS shows the promise for a selector-less crossbar array, free of the sneak-path current problem. Different implementation methods of CRS were reviewed in this chapter. Recent results showed promise that the sneak-path problem may eventually be solved, based on just a single RRAM cell. Several CRS mechanisms

have been proposed to explain the observed CRS. In fact, the underlying mechanism of CRS is not clear, and there is an absence of a universal physical model. CRS in the reported RRAM devices showed a narrow read voltage window, limiting real-life applications. A systematic study on complementary resistive switching in oxide-based RRAM devices is needed.

Chapter 3 EXPERIMENTS

3.1 Introduction

This chapter is divided into three main sections, excluding the introduction and summary sections. Section 3.2 presents the details of the samples fabrication for the CRS mechanism, CRS stability, and CRS read voltage margin studies. Section 3.3 introduces the basic working principles of physical characterization methods such as X-ray photoelectron spectroscopy (XPS), scanning electron microscope (SEM), transmission electron microscopy (TEM), and energy dispersive X-ray spectroscopy (EDX). Section 3.4 gives an introduction of the 200 mm Cascade Microtech wafer probe station, the Keithley SCS4200 semiconductor parameter analyzer, 300 mm Cascade Microtech wafer probe station, and the Agilent Technologies B1500A Semiconductor Device Analyzer, which were used to perform electrical measurements.

3.2 Samples preparation

3.2.1 Samples for the CRS mechanism study

In order to study the CRS mechanism in oxide-based RRAM devices, TiN/HfO_x/TiN and TiN/HfO_x/Pt memory cells based on only single-stack HfO_x were fabricated. Except for the different bottom electrodes, both samples underwent identical processing. The processing flow (left) and schematic cross-sectional diagram (right) of the test device are presented in Fig. 3.1. The test devices were fabricated on SiO₂/p-Si substrates. Physical vapor deposition of a 160 nm TiN bottom electrode with a Ti to N ratio of 1.1

to 1 [94] was first carried out by DC reactive magnetron sputtering of a Ti target in a mixture of N_2 and Ar gases at 375 °C. The flow rate of N_2 and Ar were 30 and 8 sccm, respectively. Or a 50 nm Pt bottom electrode was deposited by DC reactive magnetron sputtering of a Pt target in the Ar gas. The flow rate of Ar was 8 sccm. Then, the deposition of SiO_2 serving as the passivation layer was carried out using tetraethyl orthosilicate (TEOS) via a chemical vapor deposition process. This was followed by standard photolithography and reactive ion etching (RIE) for active area definition. Wafer was loaded into a Cambridge Nanotech Savannah S200 atomic layer deposition (ALD) system for HfO_x growth at a temperature of 250 °C and a pressure of 0.2 Torr. The precursor was tetrakis (dimethylamino) hafnium and the oxidizing agent was H_2O . After the ALD process, a top TiN electrode (80 nm in thickness) was deposited under the same conditions as the bottom TiN electrode. This was followed by lithography and RIE to complete the metal-insulator-metal structures (Fig. 1(a)). To minimize the etching time, a thinner top TiN electrode was used. No post-deposition annealing was carried out.

Fig. 3.1: Processing flow (left) and schematic cross-sectional diagram (right) of the test device.

A TiN/ HfO_x /TiN sample was also used for the current conduction mechanism investigation of CRS. Besides the TiN/ HfO_x /Pt samples, the sample with the top TiN electrode also replaced by Pt (i.e. Pt/ HfO_x /Pt) was fabricated for self-compliance

resistive switching mechanism analysis. The same process was used for the deposition of the top Pt electrode as the deposition of the bottom Pt electrode, and top metal patterning was achieved by lift-off.

3.2.2 Samples for the CRS stability study

For the analysis of the observed self-reset behavior in the TiN/HfO_x/TiN resistive memory devices, the TiN/HfO_x/TiN control sample, prepared using the same process introduced in Section 3.2.1, test samples with a thin Al₂O₃ layer inserted at the top or bottom TiN interface (i.e. TiN (top)/Al₂O₃/HfO_x/TiN, TiN/HfO_x/Al₂O₃/TiN (bottom)), and the TiN/HfO_x/Pt device with the bottom TiN electrode replaced by Pt were fabricated.

Another batch of test devices with different oxide stack configurations, TiN/HfO_x/TiN, TiN (top)/Al₂O₃/HfO_x/TiN, and TiN/Al₂O₃/HfO_x/Al₂O₃/TiN, were fabricated for the CRS performance study. The Al₂O₃ layer was also grown by ALD at the same temperature of 250 °C; the precursor was trimethyl aluminum. The thickness of the HfO_x layer remains the same in all cases.

3.2.3 Samples for the CRS read voltage margin study

To solve the narrow read voltage issue existing in the CRS of oxide-based RRAM devices, the device with top TiN replaced by indium tin oxide (ITO) (ITO/HfO_x/TiN) was prepared. First, electron-beam lithography (EBL) was performed on a pre-cleaned SiO₂/Si substrate, followed by DC reactive magnetron sputtering for the TiN deposition (Ti:N ratio of 1.1:1 [94]) and a lift-off to form the bottom electrode. ALD of the HfO_x layer at 250 °C was then carried out with tetrakis (dimethylamino) hafnium as the precursor and H₂O as the oxidizing agent. After the second EBL patterning step, the ITO

deposition (via physical sputtering of a commercial ITO target with ~5 wt. % Sn in an argon-only ambient) followed by the lift-off were carried out to complete the top-electrode formation.

3.3 Physical Characterization

A variety of physical-characterization techniques was utilized in our work, such as XPS, SEM, TEM, and EDX. The basic principles of these techniques are introduced in this section.

3.3.1 XPS

XPS, as a typical surface-sensitive quantitative spectroscopic technique, can examine the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material [95]. A typical XPS spectrum is a plot of the number of electrons, emitted by irradiating an analyzed material with a beam of X-rays (Al K_{α} X-rays or Mg K_{α} X-rays), against the binding energy of the electrons detected. Each element in a material produces a characteristic set of XPS peaks, corresponding to the configuration of electrons within the atoms, at characteristic binding-energy values that directly identify each element present in the analyzed material. The number of detected electrons in each of the characteristic peaks is directly related to the amount of each element within the analyzed material.

A typical XPS system is illustrated in Fig. 3.2. The number of emitted electrons per unit of time can be detected by an electron detector. The binding energy of each of the emitted electrons can be determined by measuring the kinetic energy which is based on the conservation-of-energy equation:

$$E_B = E_P - (E_K + \phi)$$

where E_B is the binding energy of the electron, E_P is the energy of the X-ray photons being used, E_K is the kinetic energy of the electron measured by the instrument, and ϕ is the work function that is a tunable instrumental correction factor, depending on both the spectrometer and the material. The energy of an X-ray with a particular wavelength is known, and the emitted electrons' kinetic energies are measured. The work function ϕ is a constant that usually does not need to be adjusted in practice.

XPS can only detect electrons that have actually escaped from the sample and reached the detector. However, electrons need to travel a long distance from the material irradiated with X-rays to the electron counting detectors. In order to improve the intensity of electron signal, the XPS system should be operated in a high or ultra-high vacuum condition. In addition, photoelectrons will undergo inelastic collisions, recombination, recapture or trapping in various excited states within the material before escaping from the analyzed material into the vacuum. These effects can lead to much stronger electron signals detected from the surface than the signals detected from the deeper surface [96] so that the XPS system is, in effect, sensitive mainly to the electrons that escape from the top 0 -10 nm of the analyzed material.

As a non-destructive technique, XPS can analyze most materials such as semiconductors, inorganic compounds, metal alloys, polymers, biomaterials, glasses, ceramics, and human implants. In our research, the composition of the resistive switching HfO_x layer was examined by XPS.

Fig. 3.2: Basic components of a monochromatic XPS system [95].

3.3.2 SEM

The SEM is a powerful tool for examining and interpreting the microstructures of materials because it provides a higher resolution than the optical microscope, and is widely used in the field of material science.

The SEM, developed in the 1930s to overcome the limitations of optical microscopy, provides enhanced magnification and resolution, which is far superior to optical systems. The principle of the SEM is based on the interaction between the incident electron beam and the analyzed specimen. Electron bombardment can produce a wide variety of emissions from the specimen, including secondary electrons, backscattered electrons, Auger electrons, X-rays, and visible photons. The most commonly used signals for SEM topographical imaging are low-energy secondary electrons (SE) and high-energy backscattered electrons (BSE). SEs are the electrons ejected from the orbital shell of the specimen atoms via inelastic-scattering interactions with the injected beam electrons. Due to their low energy, SEs, generated only within a few nanometers from the specimen's surface, can escape to be collected by the detector. As a result, SEs are usually used to examine the sample's surface topography. However, BSE are high-energy back-scattered electrons that escape from the specimen when the injected electron beam undergoes elastic interaction with the positively

charged nucleus of the specimen atoms. BSE imaging tends to be used to examine the contrast between areas with different chemical compositions [97]. Since heavy atoms in the specimen have a much stronger backscattering interaction with the beam electrons when compared with light atoms, this generates a brighter image.

The spatial resolution of the SEM is strongly dependent on the spot size of the electron probe beam at the specimen's surface. In a SEM system, the diameter of the incident-electron beam is de-magnified using two or more electron lenses before it reaches the specimen's surface. At the same time, the effective diameter of the electron source is a key factor in determining the resolution of the SEM. Two types of electron guns are used to provide the beam electrons in the current SEM system. One is the tungsten or Lanthanum hexaboride (LaB6) thermionic electron gun, which is based on thermionic emission. The thermionic electrons are emitted from the tip of the tungsten or Lanthanum hexaboride emitter filament, heated by a current to the high temperature of 2000-2700 K. The emitted electron beam is accelerated and focused towards the sample where it interacts with the sample. Another electron gun is the cold-cathode field emission electron gun. The diameters of the electron beam, emitted from the thermionic electron gun and the cold-cathode field emission electron gun, are about 20-50 μm and 10 nm, respectively. Thus, the field emission SEM (FESEM) is a good choice for obtaining high-resolution SEM images. Also, FESEM has a higher beam density (brightness), and longer tip life than thermal tungsten filament SEMs.

Fig. 3.3: (a) A typical SEM system. (b) Basic components of a SEM system.

In our research, the top view of the ITO/HfO_x/TiN crossbar memory device is characterized by using the FESEM 6340F system, which has a resolution of 3.0 nm, an accelerating voltage of 0.5 to 30 keV, and a magnification of 50x to 200,000x [98].

3.3.3 TEM

The TEM is one of the most powerful microscopy techniques in which beam electrons are transmitted through an ultra-thin specimen, interacting with the specimen as the beam passes through. An image is formed from the interaction of the electrons transmitted through the specimen, then is magnified and focused onto an imaging device or to a sensor that detects it, such as a charge-coupled device (CCD) camera. TEMs can produce imaging with a significantly higher resolution than optical microscopes due to the much smaller de Broglie wavelength of electrons compared to that of photons, which enables the user to examine things as small as a single column of atoms, which is thousands of times smaller than the smallest resolvable object in an optical microscope. Modern TEM can even examine lattice defects, atoms, and their movements. TEM, as a major analysis method, has been widely used in a wide range of scientific fields, such as the physical and biological sciences, cancer research, materials science, semiconductor research, nanotechnology, virology, and pollution [99].

The first transmission electron microscope was developed by Max Knoll and Ernst Ruska in 1931, and the first commercial transmission electron microscope was developed in 1939 [100]. A typical TEM system is illustrated in Fig. 3.4 [101], and is composed of an electron emission source for producing the electron beam, accelerating electrodes that accelerate the electrons emitted from the filament to a high energy, a high vacuum system, a series of electromagnetic lenses, a sample chamber, and a CCD camera. The electron emission source in a TEM system mainly consists of either a thermionic filament that emits

electrons by thermal heating or a field-emission filament that ejects electrons upon an application of a high electric field to the metal filament tip. The field-emission filament is a lot more expensive and requires a much higher vacuum than the thermionic filament, but it offers a very stable source with a greater resolution and a longer tip life-time. TEM operates in a very high vacuum maintained by a vacuum system in which the electrons travel. Electromagnetic lenses, including the condenser lens, objective lens, projective lens, and intermediate lens, help produce the small spot size of the electron beam by focusing the electrons, and improve the resolution of the TEM system. The CCD camera is used to capture a TEM image. With its advanced design, the analysis capacity of TEM has been significantly enhanced by the integration of several advanced techniques into the instrument. These techniques involve spectrometers, such as EDX and electron energy-loss spectroscopy (EELS). The TEM technique requires the area of interest of a specimen to be thin enough (mostly less than 100 nm) to allow electrons to penetrate it. It is not only difficult to thin the bulk of the sample down to the required thickness, but false information may also arise from a large number of artifacts that may be created in the sample during the sample preparation process (mechanical/electrochemical polishing and ion sputtering) .

Fig. 3.4: (a) A typical TEM system. (b) Basic components of a TEM system [101].

The high-resolution cross-sectional transmission electron microscopy (HRTEM) technique was used to study the different properties of the HfO_x/TiN and HfO_x/Pt interfaces. Details of the thickness of the resistive switching HfO_x layer were characterized using the TEM technique.

3.3.4 EDX

Being a type of spectroscopy, EDX also relies on the interactions of an incident electron beam and the solid specimen for investigation, similar as the SEM. As an analytical tool, EDX is extensively used for chemical characterization. As mentioned before, electron bombardment can produce a wide variety of emissions from the specimen, including SEs, BSEs, Auger electrons, X-rays, and visible photons. The SEM technique analyzes the SEs and BSEs, but the EDX technique analyzes emitted X-rays. Different elements of the analyzed sample have a unique electronic structure and, thus, have a unique response to X-rays, which is used to identify and analyze the elemental composition of the specimen's surface. EDX spectra can be acquired over a short period of time and be displayed almost simultaneously, providing a nearly instant visual representation of the chemical analysis. Qualitative analysis determines what elements are present in a sample by identifying the peaks in the spectrum, and is also used to obtain the relative abundance of the elements by identifying their corresponding peak intensities [102].

In this study, EDX analysis was mainly used to determine the Ti element distribution in the different devices ($\text{TiN}/\text{HfO}_x/\text{TiN}$, $\text{TiN (top)}/\text{Al}_2\text{O}_3/\text{HfO}_x/\text{TiN}$, and $\text{TiN}/\text{Al}_2\text{O}_3/\text{HfO}_x/\text{Al}_2\text{O}_3/\text{TiN}$) to aid the study of CRS stability.

3.4 Electrical Characterization

3.4.1 Prober system

The electrical characterization of HfO_x -based RRAM devices was carried out using either a 200 mm Cascade Microtech wafer probe station and a Keithley 4200 Semiconductor Characterization System (SCS) or a 300 mm Cascade Microtech wafer probe station and an Agilent Technologies B1500A Semiconductor Device Analyzer with a high precision (i.e. sub-femto amp) resolution, as shown in Fig. 3.5.

The wafer probe station, a platform for holding the device under test (DUT), primarily consists of (i) a thermal chuck, which serves as a stage for holding an eight inch or smaller wafer, (ii) an air-leg stabilizer, which isolates the thermal chuck from external vibrations, (iii) four probe heads, which are connected to the source-monitor units (SMUs) of the Keithley 4200-SCS (or Agilent Technologies B1500A) via 1.5 m low leakage tri-axial cables. Each probe head holds a sharp and conductive Au-coated tungsten probe with a radius of 7 μm . Two remote pre-amps are installed at the rear panel of the Keithley 4200-SCS (or Agilent Technologies B1500A) to extend the system's measurement resolution from 100 fA to 0.1 fA by effectively adding five current ranges to the SMU (10 nA, 1 nA, 100 pA, 10 pA, and 1 pA) for accurate low leakage measurements. The Keithley Interactive Test Environment (KITE) characterization program of the Keithley 4200-SCS (Agilent Technologies B1500A) provides the user with an interface for advanced test definition, parameter analysis, and graphing that is required for all the related electrical measurements. The voltage-bias was applied to the top electrode (TE) and the bottom electrode (BE) was always grounded.

Fig. 3.5: (a) Cascade Microtech 200 mm wafer probe station. (b) Keithley 4200-SCS, a test environment for controlling the various electrical measurements. (c) Cascade Microtech 300 mm wafer probe station. (d) Agilent Technologies B1500A Semiconductor Device Analyzer, a test environment for controlling the various electrical measurements.

3.4.2 Resistive switching measurement (DC/AC)

The resistive switching behavior of HfO_x -based RRAM devices is mainly characterized during the DC voltage sweep. All DC voltage-sweep testing was performed on $50 \times 50 \mu\text{m}^2$ devices at room temperature (if there was no special statement) by directly contacting the top and exposed area of the bottom electrodes using Au-plated probe tips. A positive (negative) set/reset/forming thus refers to a positive (negative) voltage-sweep applied to the TE. Forming was always needed to create the conductive paths within the dielectric stack, so that the subsequent resistive switching effect could be observed.

Under the DC voltage-sweep mode, current-voltage characteristics are obtained by applying a gradually changed voltage-bias with a constant step (0.01 V) to measure the change in the current. A typical DC bipolar resistive switching of $\text{TiN}/\text{HfO}_x/\text{TiN}$ is presented in Fig. 3.6.

Fig. 3.6: Bipolar switching characteristics of the TiN/HfO_x/TiN device. (a) Positive set/negative reset; (b) negative set/positive reset. Also shown are the current-voltage curves for the forming steps. Numbers denote the measurement sequence.

Numbers denote the measurement sequence. Bipolar resistive switching behavior can be realized under both forming polarities, by virtue of the symmetrical electrode configuration. For the case of positive forming (Fig. 3.6 (a)), the device shows the conventional negative reset (step 1), post-negative-reset (step 2), subsequent positive set (step 3), and post-positive set (step 4) measurements. Consistent DC resistive switching behavior can be observed for the negative forming (Fig. 3.6 (b)).

The HfO_x-based RRAM device was developed to replace the currently widely used flash memories for next-generation NVM applications. Programming/erasing time and voltage are important specifications. The write/erase time of flash memories is normally in the range of microseconds. The RRAM device should have better performance or comparable performance to those of flash memories. To examine the switching speed and voltage of our RRAM devices, AC resistive switching was implemented using the Agilent B1530A WGF MU module in a B1500A parameter analyzer.

3.4.4 Retention and endurance measurement

Data retention and switching endurance are also key performance indicators of nonvolatile memory. RRAM should have a data-retention time (t_{ret}) of more than ten years, which is generally required for a universal NVM. It is impossible to perform the

retention measurements over such a long period of time. Retention time is practically evaluated based on the accelerated stress condition (i.e. thermal stress up to 85°C and small constant electrical stress) and the Arrhenius plot. The RRAM device should have at least a comparable or better endurance when compared with flash memory. In our work, the retention and endurance performances of CRS under the DC- and plus-voltage operation were measured. The results are shown in the following sections.

3.5 Summary

In summary, the sample fabrication, physical and electrical characterization techniques, and prober system were discussed. HfO_x-based RRAM devices, employing different metal electrodes, with varied oxidation properties and different oxide stacks, were prepared for the study of the physical mechanism of CRS, current conduction mechanism of CRS, physical mechanism of self-compliance resistive switching, CRS stability, and CRS read-voltage window. The typical physical characterization techniques of XPS, SEM, TEM, and EDX were used to support this research. The Keithley 4200 SCS and Agilent B1500A were used to measure DC and AC current-voltage characteristics of our RRAM device respectively.

Chapter 4 COMPLEMENTARY RESISTIVE SWITCHING BEHAVIOR IN OXIDE-BASED RRAM DEVICES

4.1 Introduction

CRS offers the promise of a selector-less crossbar array free of the sneak path problem [58]. The current issues faced in the CRS in the RRAM device were reviewed in the previous chapter. One of major issues is that the underlying mechanism of CRS is not clear [65, 71, 93]. Although different resistive switching models have been proposed to explain the observed CRS in oxide-based RRAM devices based on different oxide stacks, there is an absence of a universal physical model.

In addition, numerous temperature-dependence studies on the nature of the conduction mechanisms of resistive switching in oxide-based RRAM devices have been made to-date. In the low-resistance state, conduction has been found to be either metallic [103, 104], typically characterized by a positive temperature coefficient of resistance (TCR), or semiconducting [104-106], usually marked by a negative TCR, depending on the density of vacancy defects in the filament. In the high-resistance state, which has a lower vacancy density, conduction is always semiconducting in nature and has been generally modeled using barrier-limited conduction models. To date, there has not been any investigation of the current-conduction mechanism of CRS in oxide-based RRAM devices. In this chapter, the current conduction mechanism of CRS in HfO_x -based

RRAM devices is investigated. In particular, we reveal a transition from semiconducting to metallic conduction in the low-resistance state of a single TiN/HfO_x/TiN resistive memory device.

Besides that, memory bits are represented using two distinct high resistance states in a complementary switch, thus eliminating the parasitic current associated with the low resistance state. However, the read operation for one of the high resistance states still involves a set transition and thus requires a mechanism to limit the current increase. A typical way to ensure the proper operation of a crossbar memory array would be to connect each RRAM cell in series to a selector (typically a transistor or bi-directional diode) [54, 59] that eliminates the advantages of CRS for the implementation of a selector-less crossbar array. In this regard, a complementary switch that can exhibit SCSS (i.e. the increase in current during a set transition is automatically limited by the RRAM itself without the need of a selector) should provide a pathway towards a truly selector-less crossbar memory [107]. A typical approach for achieving SCSS is to embed a “series resistor” into the RRAM cell [107-109]. The resistor may take the form of an additional oxide layer situated next to the switching layer [107-109]. Upon formation of a conducting filament in the switching layer, the series oxide serves to limit the increase of the current. The series oxide can be intentionally incorporated into the memory stack during fabrication [107-109] or unintentionally formed due to oxidation of the reactive metal electrode [68, 110]. This paper reports the existence of SCSS in the TiN/HfO_x/Pt device. An important distinction here is that there is no series oxide layer in this memory stack. Yet, SCSS is still observed indicating that another mechanism is causing such a behavior. A possible explanation is proposed below.

4.2 The role of the interfacial layer on complementary resistive switching in the TiN/HfO_x/TiN resistive memory device

4.2.1 Experiments

TiN/HfO_x/TiN and TiN/HfO_x/Pt samples, based on only single-stack HfO_x, were fabricated to study the CRS mechanism. Since TiN can be readily oxidized in an oxygen-rich ambient at relatively low temperatures, the bottom interfacial layer was expected to generate in the TiN/HfO_x/TiN sample. However, Pt is usually considered as an inert metal, thus no bottom interfacial layer should form in the TiN/HfO_x/Pt sample. To facilitate later discussion, the former sample will be referred to as the TiN sample, while the latter sample will be the Pt sample.

4.2.2 Physical analysis

4.2.2.1 XPS results of the HfO_x switching layer

The composition of our HfO_x layer was studied by XPS measurement using an Al K α (1486.6 eV) source. Photoelectrons were sampled at a direction perpendicular to the sample surface (i.e. detection angle $\theta = 0^\circ$). The measured Hf 4f and O 1s core-level spectra were curve-fitted with component spectra each comprising a combination of Gaussian (70%) and Lorentzian (30%) line shapes, as depicted in Fig. 4.1. The secondary background electron was subtracted away using the Shirley function. The full-width-half-maximum of a component spectrum was varied within a narrow range only (± 0.1 eV). The lowest number of component spectra was used to achieve

acceptably low residual values. The binding energy of Hf 4f_{7/2} and 4f_{5/2} are located at 17.0 eV and 18.6 eV, respectively (based on the C 1s reference binding energy of 285.0 eV). The O 1s spectrum comprises two different chemical states. The main component at 530.2 eV is ascribed to hafnium oxide. The smaller component at 531.0 eV may be attributed to non-lattice oxygen atoms. Analysis revealed a Hf:O ratio of 1:1.4 for the HfO_x layer, which confirmed our HfO_x layer is oxygen deficient [68]. The Hf:O ratio was determined as $\frac{A_{Hf}}{SF_{Hf}} : \frac{A_O}{SF_O}$ [111], where SF_{Hf} = 2.05 and SF_O = 0.66 are the sensitivity factor for the Hf 4f and O 1s photoelectrons, respectively; A_{Hf} and A_O are the corresponding area under the Hf 4f and O 1s XPS spectra. For the latter, only the spectrum for Hf-O bonds (with peak binding energy of 530.2 eV) is considered. The error of this method is $\sim \pm 5\%$.

Fig. 4.1: (a) Hf 4f and (b) O 1s XPS spectra of the HfO_x layer.

4.2.2.2 Cross-section TEM analysis

Results from HRTEM study on the TiN and Pt samples are shown in Fig. 4.2. The HfO_x is ~ 6 -7 nm thick in both samples, in agreement with the targeted value. A distinctive feature of the TiN sample is the presence of a region of lighter contrast, between the HfO_x layer and the bottom TiN electrode. This observation implies that an IL of ~ 4 nm thick is formed between the HfO_x and the bottom TiN electrode (Fig. 4.2(a)). However, no IL formation can be seen in the Pt sample (Fig. 4.2(b)). The clear

observation of a bottom IL in the TiN sample may be attributed to the oxidation of the exposed TiN electrode during the device fabrication. Studies have shown that TiN can be readily oxidized in an oxygen-rich ambient at relatively low temperatures [112]. Thus, during the initial cycles of the ALD process where only a few monolayers of HfO_x were formed, the oxidizing species might have penetrated the HfO_x and oxidized the underlying TiN. The growth of a GaO_x IL was similarly observed during the ALD process of Al_2O_3 on a GaN substrate [113]. For non-ALD cases, the formation of a bottom IL may still occur due to the higher thermal budget experienced by the bottom TiN electrode interface. On the other hand, bottom IL formation in the Pt sample is clearly suppressed by the relatively inert Pt metal in accordance to the known oxidation-resistant property of Pt.

Fig. 4.2: High resolution cross-sectional transmission electron micrograph of (a) the TiN/ HfO_x /TiN, and (b) TiN/ HfO_x /Pt RRAM device.

4.2.3 CRS characteristic of TiN/ HfO_x /IL/TiN resistive memory device

Due to the formation of IL at the bottom HfO_x /TiN interface, the symmetrical TiN/ HfO_x /TiN device becomes an asymmetrical TiN/ HfO_x /IL/TiN structure. Forming was necessary to create minute conductive filaments within the dielectric stack so that subsequent resistive switching effect could be observed. Forming was achieved using a voltage-ramp, until an abrupt increase of current was detected. The current at the instant of forming was limited by a preset compliance enforced by the parameter analyzer. Fig. 4.3 shows the typical bipolar resistive switching characteristics of the TiN/ HfO_x /TiN

device under both forming polarities, by virtue of the symmetrical electrode configuration. The order of the measurements performed after forming (0) is denoted by the numbers as shown. Device was switched from LRS after positive forming to HRS under negative voltage sweep, and switched back to the LRS under positive voltage sweep (Fig. 4.3(a)). Device also could be reset to a HRS from a LRS (after negative forming) under positive voltage sweep, and set to a LRS again under negative voltage sweep (Fig. 4.3(b)). Consistent switching characteristics are achieved by repeatedly ‘toggling’ the device between the two bipolar modes (Fig. 4.4).

Fig. 4.3: Current-voltage curves for forming and subsequent bipolar set and reset operations on the TiN/HfO_x/IL/TiN RRAM device. (a) Positive forming with the current compliance set at 0.5 mA; (b) Negative forming with the current compliance set at 10 μ A.

Fig. 4.4: Current-voltage curves for first 50 bipolar set/reset cycles. Consistent resistive switching behavior can be observed for each mode: (a) positive set/negative reset; (b) negative set/positive reset.

Interestingly, CRS was also observed in the TiN/HfO_x/IL/TiN memory device, as demonstrated in Fig. 4.5. The alphanumerical labels denote the sequence of

measurements. Curves 1a, 1b and 2a depict the typical negative-reset/positive-set bipolar switching behavior following the positive forming. After the positive-set step (curve 2a), a positive voltage-sweep to larger voltages yielded a subsequent reset at $\sim +1.3$ V. The ensuing positive-voltage sweep confirms the reset (curve 2c). It should be emphasized that in curve 2c, the set transition seen previously in curve 2a is no longer observed. Instead, the device can now only be set using a negative voltage-sweep (curves 3a, 3b) and reset by a positive voltage-sweep (curves 4a, 4b). Clearly, the previous bipolar switching mode comprising positive set/negative reset has been changed to a complementary mode involving negative set/positive reset.

Fig. 4.5: A set of current-voltage curves illustrating the existence of a dual-mode resistive switching behavior after positive forming. The order of measurements is as indicated by the numbers. (a) Curve 1a, 1b and 2a show the conventional negative reset, post-negative-reset and positive set measurements. Extending the voltage range during the post-positive-set induces a reset at $\sim +1.3$ V (curve 2b). The reset is confirmed by the lower current seen in curve 2c, for which the set previously present in curve 2a is now absent. (b) The set can now only be induced by a negative voltage sweep (curves 3a, 3b) and positive voltage sweep only produces a reset (curves 4a, 4b). The results clearly show a changeover from a positive set/negative reset to a negative set/positive reset mode. Extending the negative voltage sweep (after the negative set) induces a reset (curves 5a, 5b) and a change back to the positive set/negative reset mode. Also shown are curves 1a and 1b (dashed lines) from (a).

The absence of a set transition following the prior reset in the same polarity domain (cf. curves 2b, 2c) distinguishes the dual-mode switching behavior from the non-polar behavior of the Pt/HfO₂/Pt device. Moreover, the reset voltage is smaller than the set

voltage in the latter whereas it is the reverse for the TiN/HfO_x/IL/TiN device. Extending the negative voltage sweep (after the negative set) induces a reset (curves 5a, 5b) and a change back to the positive set/negative reset mode. Clearly, the asymmetrical TiN/HfO_x/IL/TiN device can exhibit CRS.

4.2.4 Electrical characteristic of Pt/HfO_x/TiN resistive memory device

No CRS behavior is observed in the Pt sample, in which the bottom IL is not present (Fig. 4.2(b)). As can be seen in Fig. 4.6, only the usual bipolar switching behavior is observed. After the positive forming step, a typical negative reset followed by a positive set can be readily achieved. Extending the positive voltage sweep beyond the set did not lead to any apparent reset (Fig. 4.6(a)). Further increasing the positive voltage sweep sets the device to a lower resistance state, which in turn requires a more negative voltage to reset it (Fig. 4.6(b)).

Fig. 4.6: Current-voltage curves for the TiN/HfO_x/Pt RRAM device formed under a positive forming. The order of measurements is as indicated by the numbers. In contrast to TiN/HfO_x/IL/TiN RRAM device, only single mode bipolar resistance switching (i.e., negative reset (step (1)) and positive set (step (2))) is evident. Increasing the positive-voltage sweep beyond the first set does not lead to any apparent reset (step (3)). A subsequent negative-voltage sweep yields the usual reset (step (4)). (b) Current-voltage curves of another TiN/HfO_x/Pt RRAM device. Likewise, the device only shows single mode bipolar resistance switching (i.e., negative reset (step (1)) and positive set (step (2))). When the positive-voltage sweep is extended to higher value (step (3)), the device is only set to a lower resistance state, which, in turn, requires a more negative voltage to reset it (step (4)).

Since the main difference of the Pt sample as compared to the TiN sample lies in the absence of the bottom IL in the former, the corresponding absence of CRS implies that the bottom IL plays a crucial role in enabling the CRS behavior seen in the TiN sample.

4.2.5 CRS model of TiN/HfO_x/TiN resistive memory device

The need for a bottom IL to be present in order to exhibit stable CRS for the HfO_x RRAM implies that the underlying mechanism may be similar to that in the Ta₂O_{5-x}/TaO_y [65], TiO₂/TiO_{2-x} devices [93]. In the latter devices, oxygen ions or vacancies can be alternately transferred between the Ta₂O_{5-x} or TiO₂ layer and the respective TaO_y or TiO_{2-x} layer, depending on the applied voltage polarity, causing either of the two layers to be driven to a high resistance state. A possible mechanism based on the conductive filaments model was proposed. The formation of localized conductive paths during forming is supported by the lack of dependence of LRS conduction on the device area, as shown in Fig. 4.7. Comparable resistance in LRS is obtained for devices with area ranging from 400-40000 μm^2 .

Fig. 4.7: Areal dependence of LRS conduction of the TiN/HfO_x/TiN memory device.

CRS mechanism in the TiN sample is schematically illustrated in Fig. 4.8. Although it may not be as apparent as the bottom IL, a top IL comprising Hf sub-oxide is expected to be formed during device fabrication, due to the oxygen scavenging property of TiN

[114]. During positive-voltage forming or set, oxygen ions are drawn from the HfO_x layer towards the top TiN electrode, leading to the formation of a conductive path (comprising oxygen vacancies) in the HfO_x layer (Fig. 4.8(a)). As a result, the overall oxide resistance decreases, setting the RRAM device to the LRS. Some of the oxygen ions may be captured by vacancies present in the top IL, reducing the vacancy density in the IL region above the conductive path. During a subsequent negative-voltage sweep, these oxygen ions in the top IL are transported back to the conductive path [115], causing the conductive path near the top IL to be partially reoxidized, and hence, the device is switched to HRS (Fig. 4.8(b)). The process is reversed during a subsequent positive-voltage set (Fig. 4.8(a)). The role of the top IL in bipolar resistive switching is corroborated by improved performance achieved via the incorporation of either a thin Ti or Hf cap layer in between the top TiN electrode and the HfO_x layer [116]. It should be noted that the top IL in the TiN sample plays an important role opposite to that of the top $\text{Ta}_2\text{O}_{5-x}$ layer in the $\text{Ta}_2\text{O}_{5-x}/\text{TaO}_y$ sample [65]. In the latter, a negative voltage drives oxygen ions from the relatively oxygen-rich $\text{Ta}_2\text{O}_{5-x}$ to the oxygen-deficient TaO_y layer, setting the device to LRS during forming, and a positive voltage is needed to reset the device to HRS.

A further extension of the positive-voltage sweep following the set may draw oxygen ions from the bottom IL into the HfO_x layer, and, in turn, cause the conductive path next to the bottom IL to be partially reoxidized, and the device to be reset to HRS (Fig. 4.8(c)). It is worth noting that the internal configuration of the conductive path is now different from that after negative reset (Fig. 4.8(b)). The reoxidized part of the conductive path is now situated near the bottom IL, as opposed to case of negative reset, where the reoxidized part is situated near the top IL. It is here where the role of the bottom IL is crucial to realizing stable CRS. Without it, such as in the case of the Pt

sample, no supply of oxygen ions to the conductive path can occur.

Fig. 4.8: Schematic illustration of the proposed mechanism for complementary resistive switching in the TiN/HfO_x/IL/TiN RRAM device. (a) Formation of conductive path in the HfO_x either after positive-voltage forming or set, where oxygen ions from the HfO_x are drawn towards the top electrode, with some captured by the vacancies in the IL. (b) During negative voltage sweep, oxygen ions captured in the top IL are driven back to the vacancy-filled conductive path. This partially reoxidizes the conductive path next to the top IL and resets the device. Alternating between a positive and negative voltage sweep repeatedly drives the device between low resistance state (Fig. 4.8(a)) and high resistance state (Fig. 4.8(b)), respectively. (c) A further increase of the positive voltage after the set (Fig. 4.8(a)) draws in oxygen ions from the bottom IL, causing the conductive path next to it to be partially reoxidized and resetting the device (arrow 1). This changes the position of the reoxidized part of the conductive path to the bottom IL. (d) A subsequent negative-voltage sweep drives the oxygen ions in the partially reoxidized part of the conductive path back to the bottom IL, reforming the conductive path and setting the device. A further increase of the negative voltage after the reset in (Fig. 4.8(d)) drives oxygen ions from the top IL into the underlying conductive path, partially reoxidizing this region of the conductive path and resetting the device (arrow 2). This changes the position of the reoxidized part of the conductive path back to the top IL, as shown in Fig. 4.8(b).

Increasing the positive voltage sweep would lead to more oxygen ions being drawn towards the top IL, further depleting the oxygen content in the conductive path and increasing the current (Fig. 4.6(b)). Following the positive reset in the TiN sample (Fig. 4.8(c)), the device now can no longer be set using a positive-voltage sweep, since a moderate positive voltage could not deplete the oxygen ions in the conductive path near the bottom IL. However, a negative-voltage sweep could cause a set (Fig. 4.8(d)) since

this voltage polarity could drive the oxygen ions back to the bottom IL, making the adjacent conductive path oxygen-deficient again. Due to the absence of the bottom IL in the Pt sample, alternate partial reoxidization and reformation of the conductive path cannot readily happen in this region. Only partial reoxidation/reformation of the conductive path near the top IL can occur, yielding only a single bipolar switching mode. Sweeping the voltage to more negative values after the negative set (Fig. 4.8(d)) would drive oxygen ions from the top IL into the conductive path, causing the top part of the conductive path to be partially reoxidized and the device to be reset. When this happens, the internal configuration of the conductive path is changed back to that shown in Fig. 4.8(b), and the device can now only be set and reset under positive and negative voltages, respectively.

The consistently larger reset voltage, as compared to the set voltage, may suggest that it is more difficult to move oxygen ions from the IL to HfO_x during reset than to move oxygen ions from HfO_x to the IL during set. The difference may be explained as follows. Once the device is reset, most of the applied voltage during a subsequent set measurement will be dropped across the narrow, partially reoxidized part, as this is the most resistive part of the conductive path. Hence, a relatively low voltage is enough to generate the electric field needed to move the oxygen ions from HfO_x to IL. After set, however, the applied voltage during a subsequent reset operation would be more evenly distributed throughout the entire conductive path, and thus, a higher voltage is needed to produce the required electric field to move oxygen ions from IL to HfO_x .

The explanation in Fig. 4.8 attributes CRS to the alternate exchange of oxygen ions between the HfO_x conductive path and the top and bottom IL. The absence of bottom IL is believed to have caused the CRS behavior to disappear in the Pt sample. To further validate the importance of the bottom IL on CRS, negative-voltage forming was carried

out on the Pt sample to determine if the positive reset/negative set switching behavior can happen. Since the Pt would be the anode during forming/set, much poorer switching behaviour should result as there is no IL at the Pt electrode interface. This inference is indeed borne out by Fig. 4.9. Unlike the case of positive-voltage forming, only a very marginal reset is obtained during the positive voltage sweep after negative voltage forming. Extending the positive voltage sweep to higher values would trigger a set (not shown), and subsequently, the device can be reset by a negative voltage and set by a positive voltage. In this case, it is believed that the partial reoxidation and reformation of the conductive path happen at the top IL interface, similar to the case of positive voltage forming (Fig. 4.6). The poor resistive switching behavior after negative forming further supports the proposed crucial role of the bottom IL in determining CRS behavior.

Fig. 4.9: Evolution of current-voltage characteristics of the TiN/HfO_x/Pt RRAM device under negative voltage forming for successively higher current compliance (as indicated). After the negative voltage forming (symbol), a negative voltage sweep (red dashed line) reveals a higher current, confirming the transition to a lower resistance state. However, only very marginal reset can be observed under positive voltage sweeps (dashed lines denote a second positive-voltage sweep after the first (solid lines)).

It should be noted that although CRS has been observed in RRAM stacks using Pt as the electrode (e.g., Pt/ZrO_x/HfO_x/ZrO_x/Pt [91]), the two dissimilar oxide materials (ZrO_x and HfO_x) are believed to have played a role similar to the two layers of the same material but of different oxygen contents (e.g., Ta₂O_{5-x}/TaO_y [65] and TiO₂/TiO_{2-x} [93]), allowing oxygen-ion exchange to occur alternately between them. Hence, CRS could

still occur even though the Pt electrode is used, so long as another oxide region exists for oxygen-ion exchange to take place.

4.2.6 Retention and endurance characteristics of the TiN/HfO_x/TiN resistive memory device

The retention and endurance characteristics of both bipolar and complementary resistive switching in the TiN/HfO_x/TiN resistive memory device were also measured (Fig. 4.10). The retention test was performed at 125 °C with a read voltage of 0.1 V, and the endurance test was read at 0.1 V. The device shows a good data retention after 10,000 seconds for both negative reset/positive set and positive reset/negative set modes. It should be noted that the difference in the HRS I-V curves (Fig. 4.5) either between V_{+set} and V_{+reset} or V_{-set} and V_{-reset} may be used to denote two distinct memory states, with the read voltage set in between (V_{+set} , V_{+reset}) or (V_{-set} , V_{-reset}). The read operation is destructive for one of the two HRS's. For instance, if the re-oxidized filament region is near the top IL, a read voltage between V_{+set} and V_{+reset} would result in a set to the LRS but this can be rectified with the subsequent application of a voltage more negative than V_{-reset} . If the re-oxidized filament region is near the bottom IL, the same read voltage would give a lower current, with no change to the filament configuration.

Fig. 4.10: Data retention (measured at 125 °C) for (a) negative reset/positive set, (b) positive reset/negative set, and endurance property for (c) negative reset/positive set, and (d) positive reset/negative set of the TiN/HfO_x/TiN resistive memory device at a read voltage of 0.1 V.

4.3 Current conduction mechanism investigation of complementary resistive switching in oxide-based RRAM device

4.3.1 Experiments

Numerous temperature dependence studies on the nature of the conduction mechanisms of either unipolar or bipolar switching in the HfO_x-based RRAM have been made to-date. For the low-resistance state, conduction has been found to be either metallic or semiconducting, depending on the density of vacancy defects in the filament. As for the high-resistance state which has a lower vacancy density, conduction is always semiconducting in nature and has been generally modeled using barrier-limited conduction models. In this work, the current conduction mechanism of CRS in a single TiN/HfO_x/TiN resistive memory device is investigated.

Test devices, of area $50 \times 50 \mu\text{m}^2$, were fabricated following a standard procedure. The device structure and fabrication details were introduced in chapter 3. The HfO_x layer was formed by atomic-layer deposition. The thickness is 7 nm and the Hf:O ratio is 1:1.7. Current-voltage measurements were made via a Keithley SCS4200 parameter analyzer, on a Cascade Microtech probe station equipped with a thermal stage. Direct contact of the top electrode and exposed bottom electrode was made by Au-plated probe needles. Temperature setting of the chuck was maintained within ± 0.1 K.

4.3.2 Electrical characteristic of $\text{TiN}/\text{HfO}_x/\text{TiN}$ resistive memory

Fig. 4.11 shows the complementary switching behavior of the $\text{TiN}/\text{HfO}_x/\text{TiN}$ resistive memory. Numbers denote the measurement sequence. A traditional bipolar negative-reset (step 1 and 2) and positive-set (step 3) switching was observed after positive forming (not shown). After that, the switching mode could be switched to complementary positive-reset (step 4 and 5) and negative-set (step 6) switching mode.

Fig. 4.11: CRS characteristics of the $\text{TiN}/\text{HfO}_x/\text{TiN}$ device. (a) BRS mode: positive set/negative reset; (b) CRS mode: negative set/positive reset. Numbers denote the measurement sequence.

4.3.2 Current conduction mechanism analysis

The current conduction mechanism of the HRS and LRS was analyzed in both the BRS mode and CRS mode. Fig. 4.12 shows the current conduction mechanism of the

HRS in BRS mode (curve 2 in Fig. 4.11). Temperature-dependent I-V measurement results (i.e. HRS resistance decreases with the temperature from 300 K to 400 K in Fig. 4.12(a)), the linear fit of $\ln(I/T^2)$ versus $1/T$, as shown in Fig. 4.12(b), and the linear relationship between $\ln(I)$ versus $V^{1/2}$ from 0.1 V to 0.5 V (Fig. 4.12(c)) indicate that Schottky emission is the dominant conduction mechanism in the HRS [117, 118], and the extracted barrier height (ϕ_B) is 0.34 eV (Fig. 4.13(a)).

Fig. 4.12: Carrier transport mechanism in HRS of the TiN/HfO_x/TiN device. (a) Typical I-V characteristics at different temperatures. (b) The linear fit of $\ln(I/T^2)$ versus $1/T$. (c) The linear relationship of $\ln(I)$ versus $V^{1/2}$.

A study was also made on the HRS in the CRS mode (curve 5 in Fig. 4.11). Similarly, the Schottky conduction model [117, 118] yields the best fit (Fig. 4.13(b)) with an extracted barrier height of 0.33 eV, indicating a barrier-limited conduction mechanism. Clearly, Schottky emission is considered a dominant conduction mechanism of the HRS in both the BRS and CRS mode due to the same top/bottom TiN/HfO_x interface in the symmetric TiN/HfO_x/TiN resistive memory device.

Fig. 4.13: (a) and (b) are respective $\ln(I)$ versus $V^{1/2}$ plots in HRS for BRS and CRS mode in Fig. 4.11. The linear relationship implies Schottky-limited conduction; ϕ_B is the extracted barrier height. The linear best-fit lines are as shown.

Investigation on the temperature dependent LRS in the BRS mode found a transition from semiconducting to metallic current conduction. Existence of a near-zero temperature-coefficient of LRS resistance has been observed. Fig. 4.14(a) shows the LRS current-voltage (I - V) curves for two temperatures. To ensure that the LRS was not perturbed by the measurement, the voltage-bias was limited to 0.5 V. LRS stability was checked by applying the voltage sweep several times at a given temperature. Negligible differences among the current-voltage curves (not shown) confirmed the LRS stability. The crossover of the two curves around 0.25 V should be noted. Below 0.25 V, a higher current is obtained when the temperature is increased. The reverse holds true above 0.25 V. Variation in the LRS resistance R with temperature for different voltages are shown in Fig. 4.14(b). At 0.1 V, R decreases with increase in temperature. On the other hand, R @0.5 V increases with temperature. At 0.25 V (crossover point; Fig. 4.14(a)), R is approximately independent of temperature. Although Fig. 4.14 shows only the results for the TiN/HfO_x/TiN device, similar observations are obtained on other HfO_x devices (e.g. TiN/HfO_x/Pt, ITO/HfO_x/TiN).

Fig. 4.14: (a) Current versus voltage (I - V) curves of the low-resistance state (LRS) at two temperatures. The applied voltage was limited to 0.5 V to avoid the influence of a reset due to oxygen-ion migration from the opposite electrode interface [68, 79]. (b) LRS resistance R as a function of temperature for different voltages. Dashed lines are eye guides.

As the temperature-induced variation of R is relatively small (Fig. 4.14(b)), contributions from the TiN and probe contact resistances to the variation should be

clarified. To ascertain the TiN resistance, blanket-deposition (via reactive sputtering) of a 70-nm thick TiN (same thickness as the electrodes of the test device) was made on a 6-inch SiO₂/Si substrate and the sheet resistance ρ_{sh} measured at various positions via the four-point probe method (Fig. 4.15(a)). The deposition was carried out under the same conditions as those used for the electrodes of the test device. The resultant TiN is nearly stoichiometric, with a Ti to N ratio of 1.1:1, as determined by x-ray photoelectron spectroscopy (not shown). Fig. 4.15(b) shows the distribution of ρ_{sh} , ranging from 3.68 to 4.63 $\Omega/\square$. The average $\rho_{sh} = 4.17 \Omega/\square$, which corresponds to a resistivity of 29 $\mu\Omega\text{-cm}$, is in very good agreement with the reported value of 25 $\mu\Omega\text{-cm}$ for stoichiometric TiN formed by reactive sputtering [119]. Based on the temperature-coefficient of resistance of 900 ppmK⁻¹ for stoichiometric TiN [119], the resistance increase from 300-400 K is $\sim 0.4 \Omega$.

Fig. 4.15: (a) Four-point probe measurement of the sheet resistance ρ_{sh} of a 70-nm thick, reactively sputtered TiN layer (Ti:N = 1.1:1) at different positions on a 6-inch SiO₂/Si substrate. (b) The measured ρ_{sh} appears to follow a normal distribution with minimum, maximum and average values as indicated.

To assess the probe-contact resistance R_c , the probes were positioned at the opposite ends of a $50 \times 50 \mu\text{m}^2$ top TiN electrode (Fig. 4.16(b) inset) and the current-voltage curve recorded. Fig. 4.16(a) shows the distribution of the as-measured resistance $R_m (= R_{TiN} + 2R_c)$. The average R_m is 9.7 Ω , giving an average $2R_c$ of $\sim 5.5 \Omega$. From these tests, we conclude that the much larger as-measured LRS resistance ($\sim 70\text{-}100 \Omega$) in Fig. 4.14(b) consists of a major contribution from the cell resistance. The temperature dependence

of R_m is also examined in Fig. 4.16(b), showing an increase of 1.9Ω for a temperature change from 300 to 400 K. This positive temperature dependence should be contrasted against the opposite dependences and larger resistance changes seen in Fig. 4.14(b), indicating a non-negligible role of the cell resistance in the observed behaviors.

Fig. 4.16: (a) Distribution of the as-measured resistance $R_m (= R_{TiN} + 2R_c)$ between two probes spaced $\sim 50 \mu m$ apart on the top TiN electrode as shown in the inset in (b) (not drawn to scale). R_{TiN} and R_c denote the TiN and probe-contact resistances, respectively. (b) Temperature dependence of $R_{TiN} + 2R_c$, showing an increase of 1.9Ω from 300 to 400 K.

The positive dependence of R (@ 0.5 V) on temperature (Fig. 4.14(b)) implies a metal-like behavior of the filament [103]. In Fig. 4.17(a), we examine the variation of as-measured R with temperature, for voltages ranging from 0.35-0.5 V, in steps of 0.01 V (open circle). In this voltage range, the spread in R is relatively narrow ($< 5 \Omega$), indicating that the conduction is largely Ohmic. The averages for different temperatures are denoted by the filled circles. The open triangles show the temperature dependence of R' , after correcting for the TiN and probe-contact resistances. Evidently, R' varies almost linearly with temperature and their relationship may be given by the standard equation of a metallic conductor, as follows

$$R'(T) = R_0'[1 + \beta(T - T_0)] \quad (1)$$

where R_0' is resistance at reference temperature T_0 (300 K) and β is temperature coefficient. Least-squares fitting (line) gives $\beta = 3.1 \times 10^{-4} \text{ K}^{-1}$, which compares favorably with the range ($8 \times 10^{-4} - 1.6 \times 10^{-3} \text{ K}^{-1}$) obtained for sputtered Hf films [120].

This implies that conduction in this regime is determined by a Hf-like filament embedded in the HfO_x , consistent with the view that oxygen ions were being extracted from the HfO_x layer during the forming process, thus giving rise to a Hf-rich filament. The lower β may be explained by the fact that the filament still comprises Hf sub-oxide and is not pure Hf. The density of a sputtered Hf film was shown to affect β , with β decreasing to $8 \times 10^{-4} \text{ K}^{-1}$ for a 50% film density (relative to bulk) [120].

On the other hand, the negative dependence of R (@ 0.1 V) on temperature (Fig. 4.14(b)) implies a semiconducting behavior, where conduction is generally limited by charges having to overcome some energy barrier. To shed more light on the nature of the conduction mechanism, a $\log_{10} R'$ versus $(kT)^{-1}$ (k is Boltzmann constant) is constructed for numerous voltages $< 0.25 \text{ V}$ (Fig. 4.17(b)). An Arrhenius relationship is evident and the activation energy E_a at different voltages can thus be extracted. The extracted E_a is relatively small, only on the order of several tens of meV, similar to those reported in earlier studies [104-106, 121]. This implies that in this voltage regime, conduction through the filament may be limited by a tunneling process between traps [121]. The resultant current density may be expressed as [117]:

$$J = qn \cdot d \cdot \nu \cdot \exp\left(\frac{qd\xi}{kT} - \frac{E_{a0}}{kT}\right) \quad (2)$$

where qn is electronic charge density, d is trap spacing, ν is thermal vibration frequency of electrons at the trap sites, ξ is applied electric field and E_{a0} is zero-field activation energy between two traps. Since conduction is a sequential process, the current would be limited by the tunneling step involving two traps spaced farthest apart along the conduction path. In past studies [117], E_{a0} is usually ascribed as the effective activation energy level referenced from the dielectric's conduction band edge (for electron transport). Here, we caution against a similar interpretation. This is because as compared to the pre-forming resistance ($\sim 1 \text{ T}\Omega$), the much smaller value of R ($\sim 100 \Omega$) implies

that a high density of traps is present at the filament location. *Ab-initio* simulation has shown that the bandgap of HfO_x having ~ 10 at. % of oxygen vacancies is significantly reduced, due to a “lowering” of the conduction band edge towards the valence band edge [105]. Thus, it is reasonable to assume that at the filament location, the TiN/HfO_x band offset is significantly reduced and conduction occurs primarily through a band of defect states formed by the large number of oxygen vacancies there (cf. Fig. 4.18) [122, 123]. A more logical interpretation of E_{a0} would be the average level of the two farthest spaced traps referenced from the collapsed conduction band edge or top of the defect band.

Fig. 4.17: (a) Left axis: 1) As-measured LRS resistance R as a function of temperature T for the metallic-like conduction regime. At a given T , the open circles denote R obtained at different voltage biases, ranging from 0.35-0.5 V in steps of 0.01 V. The filled circle denotes the average R . 2) R' (average R after the correction of probe-contact and TiN resistances) as a function of T . Right axis: $R_{\text{tunnel}} @ 0.25 \text{ V}$ ($= R @ 0.25 \text{ V} - R_{\text{Ohmic}}$) as a function of T . R_{tunnel} is the resistance of the rate-limiting tunneling between two farthest spaced traps along the conduction path; R_{Ohmic} comprises the probe-contact and TiN resistances and the Ohmic resistance of the rest of the conducting path. Lines are least-square linear regression fitting. (b) Arrhenius plot for R' in the semiconductor-like conduction regime with the voltage bias as the parameter. Activation energy (E_a) for selected voltage biases are as shown. (c) Arrhenius plot for R_{tunnel} at different voltage biases. (d) Plot of E_a of R_{tunnel} and of R' versus electric field, estimated as the ratio of the applied voltage bias (0.02-0.25 V) to the HfO_x thickness or filament length.

The decreasing E_a ($38 \rightarrow 23$ meV) obtained for increasing voltage bias ($20 \rightarrow 130$ mV) indicates a field-induced barrier lowering effect which gives rise to a weakened temperature dependence of the tunneling current. This suggests the possibility that as the voltage bias is increased, the temperature dependence of the rate-limiting tunneling step may be weakened to an extent comparable to the opposite temperature dependence of the Ohmic conduction due to the rest of the conduction path. When this happens, the temperature dependence of the two processes compensate each other, resulting in a near-zero TCR (Fig. 4.14(b)). A further increase in the voltage bias would then see a changeover to a metallic conduction. To check the above explanation, the temperature and electric field dependence of E_a of the rate-limiting tunneling step are examined. To enable an accurate analysis, the Ohmic resistance component R_{Ohmic} (comprising $R_m = 2R_c + R_{\text{TIN}}$ and the resistance arising from Ohmic conduction in the rest of the breakdown path) must be excluded from the overall resistance R . As can be seen from Fig. 4.16(a), the average for $2R_c + R_{\text{TIN}}$ is 9.7Ω (at 300 K) whereas the corresponding average for R in the metallic regime (Fig. 4.17(a)) is 69Ω , indicating that there is a non-negligible Ohmic resistance contribution from the breakdown path itself. In the metallic regime, the relative independence of R on the voltage bias over the range 0.35-0.5 V (Fig. 4.17(a), open circles) shows a predominantly Ohmic conduction, which implies that the voltage bias is large enough to suppress the expectedly stronger exponential voltage dependence of the resistance arising from the rate-limiting tunneling step, due to the field effect overcoming a large part of the tunneling barrier (Eqn. (2)). This enables us to make use of the average R obtained in the voltage range (0.35-0.5 V) as a good estimate for R_{Ohmic} in the semiconducting regime. Fig. 4.17(c) shows the Arrhenius plot for R_{tunnel} , the resistance due to the rate-limiting tunneling step, obtained after subtracting R_{Ohmic} from R in the semiconducting regime. The extracted E_a is larger than that obtained for R' at

each voltage bias in Fig. 4.17(b); the difference may be ascribed to the weaker temperature dependence of R' due to the inclusion of the relatively temperature-independent R_{Ohmic} . R_{tunnel} (at 0.25 V) is plotted as a function of temperature in Fig. 4.17(a). A quasi-linear, negative dependence on temperature can be observed with a slope almost identical in magnitude to that of R_{Ohmic} . This validates our proposition that the near-zero TCR of R (at 0.25 V) is a consequence of the compensation of the Ohmic and tunneling conduction mechanisms having opposite but equal temperature dependence. A plot of E_a (for R_{tunnel}) versus ξ (estimated as the ratio of the applied voltage to the HfO_x thickness) yields a linear relationship (Fig. 4.17(d)), validating Eqn. (2). E_{a0} and d are determined as 77 meV and 8.3 Å, respectively from least-squares fitting. Also shown is the ξ -dependence of the E_a of R' . Least-squares fitting of low voltage-bias data points (0.01-0.08 V) yields a straight line (dashed) having an almost identical slope as that obtained for the E_a of R_{tunnel} . Deviation from linearity at higher voltage biases may be ascribed to the increasing effect R_{Ohmic} (which has a positive TCR) on the E_a of R' , as the negative TCR of R_{tunnel} gets weakened by the increasing voltage bias. At $E_a = 0$, $\xi \approx 398$ kV/cm, which corresponds to a voltage bias of 0.28 V, in good agreement with the zero-TCR voltage (0.25 V) for the as-measured resistance R (Fig. 4.14(b)). The latter voltage is slightly smaller due to the positive TCR of $R_{\text{TiN}} + 2R_c$ (Fig. 4.16(b)), resulting in the transition from semiconducting to metallic conduction occurring at a lower voltage bias during actual measurement.

Based on the above analysis, we propose in Fig. 4.18 an explanation for the observed transition from semiconducting to metallic conduction. The generation of a high density of vacancy defects at the filament location leads to the formation of a defect band [122, 123] and the “collapse” of the TiN/ HfO_x conduction band offset (Fig. 4.18(a)) [105]. Atomic-scale spectroscopic studies [124-127] have found that the breakdown oxide

region is deficient in oxygen. Thus, it is reasonable to presume that oxygen vacancy defects populate the breakdown region. As shown by *ab-initio* simulation study [128] and spectroscopic ellipsometry measurement [129], a vacancy defect gives rise to an energy state at ~ 1 eV below the HfO_2 conduction band edge. Considering the random orientations of the Hf dangling bonds and the high density of vacancy defects at the filament location, a defect band would be formed instead of a single defect level. The formation of this defect band significantly lowers the TiN/HfO_x conduction offset (~ 1.9 eV) [121], giving rise to a highly conductive path connecting the two electrodes. However, conduction is not metallic as the extracted trap spacing of ~ 11 Å implies that at a certain position along the path, the electron wave functions of two traps, presumably spaced farthest apart, do not completely overlap (the electron wave function localization length ~ 3 Å in HfO_x [121]), unlike in a pure Hf metal. Hence, conduction is limited by electron tunneling from one trap to another. (Fig. 4.18(b)) The relatively low tunneling barrier (~ 43 meV) may be attributed to the small trap spacing and the collapsed HfO_x conduction band edge. An increase of the voltage bias reduces the tunneling barrier, making it easier for electron tunneling to happen. When the tunneling barrier is overcome by a sufficiently large voltage bias (Fig. 4.18(c)), conduction becomes metal-like and electron transport is scattering-limited just like in a metal film. Good agreement between the β extracted in this regime and that for the Hf metal film [120] lends strong support (Fig. 4.17(a)). At the crossover point, the opposite temperature dependence of the two transport mechanisms result in a zero temperature-coefficient of the LRS resistance.

Fig. 4.18: Schematic energy band illustration of transition from trap-assisted tunneling conduction to metal-like conduction as the applied voltage is increased. (a) Formation of a defect band comprising oxygen vacancy defects after forming. Dashed line depicts the TiN/HfO_x conduction band offset before forming. (b) Exaggerated view of low-voltage electron transport, limited by tunneling between two farthest-spaced traps along the conduction path within the defect band. Each short dash depicts an energy level arising from a vacancy defect. (c) Conduction becomes metal-like when the tunneling barrier is overcome by a stronger applied electric field.

Since the near-zero TCR point stems from the compensation of two conduction mechanisms having different temperature dependence (linear for R_{Ohmic} whereas exponential for R_{tunnel}), a pertinent question would be the temperature range over which the near-zero TCR behavior remains valid. A check could be made by simulating the variation of R_{Ohmic} and R_{tunnel} over a broader temperature range than that accessible during the experimental work, based on the parameters extracted from Fig. 4.17(a) and (c), respectively. The results are shown in Fig. 4.19 for temperatures ranging from 80 to 500 K (left axis). As can be seen, R approaches a “quasi-plateau” around 300-400 K, where $dR/dT \sim 0$ by virtue of the comparable but opposite temperature dependence of R_{Ohmic} and R_{tunnel} . As expected, the quasi-plateau is shifted towards higher temperatures for lower voltage biases. Above 400 K, $dR/dT \sim 0.026 \text{ } \Omega/\text{K}$, smaller than the $0.036 \text{ } \Omega/\text{K}$ value for R_{Ohmic} due to the continued presence of the negative dR_{tunnel}/dT . Below ~ 270 K, dR/dT goes negative rapidly due to the stronger exponential temperature dependence of R_{tunnel} .

Fig. 4.19: Left axis: Simulated temperature dependence of R_{Ohmic} , R_{tunnel} and $R (= R_{\text{Ohmic}} + R_{\text{tunnel}})$ over a broad temperature range (80-500 K) based on parameters extracted from the experimental data (Figure 5(a) and 5(c)). Right axis: Derivative of R with respect to temperature. Arrows indicate the shift in the curves as the voltage bias is reduced from 0.25 V to 0.2 V.

The analysis and explanation presented above imply that a critical vacancy defect density should exist for the transition from semiconducting to metallic conduction to be observed in a single device. Below this critical defect density, trap spacing and the corresponding tunneling barrier become relatively large. Whether the transition to metal-like conduction could be observed is determined by the largest voltage that can be applied before further breakdown occurs. On the other hand, if the defect density is far above the critical threshold, trap spacing and tunneling barrier become exceedingly small such that conduction is metal-like even at low voltages. The above may explain why some past studies observed a semiconducting LRS conduction behavior [104-106] while others only observed a metallic conduction behavior [103, 104]. For instance, De Stefano *et al.* [105] reported a semiconducting LRS conduction in the TiN/HfO_x(10 nm)/TiN device having a relatively large resistance ($\sim 2.5 \text{ k}\Omega$ @0.1 V, 313 K), which implies a low vacancy defect density. A similar semiconducting LRS conduction was also observed in a TiN/HfO_x(5 nm)/TiN device formed with a higher resistance of $\sim 1 \text{ M}\Omega$ @0.1 V, 298 K. However, metal-like LRS conduction was observed in the TiN/Hf/HfO_x(10 nm)/TiN device formed to a lower LRS resistance ($\sim 300 \Omega$ @0.1 V,

298 K [104]). The change in conduction behavior was ascribed to an increase of the defect density in the filament due to the “oxygen-scavenging” effect of the Hf interlayer (which increased the pre-forming vacancy defect density in the HfO_x) and the higher forming current compliance used on the latter device. Our inference that a critical defect density should exist for the conduction-transition to be observed in a single device is consistent with the findings of ref.[104].

At this juncture, a quantitative study on how the near-zero TCR point is impacted by forming-current compliance, stack thickness and stoichiometry, etc. is, however, challenging due to the randomness nature of filament formation. Nonetheless, the observed transition from a semiconducting LRS conduction behavior in the $\text{TiN}/\text{HfO}_x/\text{TiN}$ device [104] to a metallic conduction in the $\text{TiN}/\text{Hf}/\text{HfO}_x/\text{TiN}$ device implies that there should exist an intermediate set of conditions (i.e. stack thickness and stoichiometry, forming-current compliance, etc.) that would enable such conduction transition to be consistently observed in a single RRAM cell. On the other hand, one may regard an intermediate resistance state (one that is between a low resistance state that is always metallic and a high resistance state that is always semiconducting in nature) as an alternative route to realizing the zero-TCR point. As our analysis has shown, the transition from semiconducting to metallic conduction is controlled by two farthest spaced defects along the breakdown path. In principle, one may leverage on the gradual set or reset transition behavior to incrementally adjust the resistance of the breakdown path, through varying the defect distribution inside the path. It may then be possible to arrive at an intermediate conduction state limited by two defects, separated by a distance slightly larger than the electron wave-function localization length. In this case, one should be able to observe a voltage-driven semiconducting-to-metallic transition, with a zero-TCR point at the transition voltage. The approach should in principle also allow

adjustment of the zero-TCR voltage through varying the separation of the two defects. It is also worthwhile to point out the possibility of generalizing the conceptual understanding attained in this study to other metal-oxide RRAM devices having similar properties as the HfO_x RRAM device examined in this study.

4.4 Physical mechanism investigation of self-compliance resistive switching characteristic of oxide-based RRAM device

4.4.1 Experiments

Our earlier study on the $\text{TiN}/\text{HfO}_x/\text{TiN}$ device has shown a self-compliant complementary resistive switching behavior (Fig. 4.11). In this device, however, there is an unintentional TiO_xN_y interfacial layer (IL), of ~ 4 nm thickness, present between the bottom TiN electrode and HfO_x , as can be seen from the high-resolution cross-sectional TEM result (Fig. 4.2(a)). The formation of a bottom IL has also been observed in past studies and has been ascribed to the unintentional oxidation of the bottom electrode during processing [112]. In our test samples, it was determined that the plasma-ashing process used to ensure complete photoresist removal after active region definition was the major contributing factor. During the processing, the bottom TiN in the active area was exposed to the oxygen plasma, resulting in the growth of a TiO_xN_y layer. As previous reports [107-109] have shown that a series oxide layer may limit the current increase during set transition, bottom IL formation was avoided in the $\text{TiN}/\text{HfO}_x/\text{Pt}$ device (device A) by replacing the bottom TiN with an inert Pt electrode. The TEM result in Fig. 4.2(b) confirmed the absence of a bottom IL in device A. As a

comparison, a test device with the top TiN electrode also replaced by Pt was fabricated, i.e. Pt/HfO_x/Pt (device B). A forming step is needed to initiate resistive switching operation in our test devices as no focus was made to optimize the HfO_x stoichiometry for forming-free operation. Nonetheless, forming-free operation of HfO_x RRAM devices has already been demonstrated and may therefore be incorporated.

4.4.2 Self-compliance resistive switching characteristics of HfO_x-based RRAM device

Fig. 4.20(a) shows the bipolar resistive switching behavior of device A after positive forming. The increase in current during the set transition at ~0.5 V is also self-arrested, like the TiN/HfO_x/TiN device in Fig. 4.11. However, unlike the TiN/HfO_x/TiN device, there is no series oxide layer in device A (Fig. 4.2(b)). This implies that a different mechanism must be responsible for the self-compliance set-switching (SCSS) behavior in the latter. It should be mentioned that device A exhibits positive set/negative reset switching only, in contrast to the TiN/HfO_x/TiN device which exhibits complementary switching. Attempts to form the conducting filament in device A using a negative-voltage sweep results in either a poor or no positive reset (Fig. 4.6 of ref. [68]). The absence of negative set/positive reset switching in this device is a consequence of the inert Pt replacing TiN as the bottom electrode and is consistent with the common view that TiN serves as an oxygen “reservoir” which enables bipolar resistive switching [68]. It is believed oxygen ions that drift from the filament are stored in the TiN anode. Under a reverse-polarity sweep, oxygen ions in TiN are moved back to the filament, thus causing a reset. Pt, on the other hand, is permeable to oxygen as shown in past studies [130]. For instance, the exposure of a Pt/Si stack to air led to the growth of a SiO_x interfacial oxide [130], indicating that oxygen could easily penetrate the Pt layer,

probably via grain boundaries, to oxidize the underlying Si. Oxygen diffusing through the Pt layer and piling-up at the Pt/TiN interface were also observed after exposure of the PZT/Pt/TiN/Si stack to air [131]. Thus, upon filament formation, it is likely that oxygen ions entering the Pt anode are quickly dispersed into the bulk of the electrode (i.e. the Pt acts as a “sink” for oxygen). The lack of oxygen at the Pt interface may explain the absence of positive reset switching in device A.

Fig. 4.20: (a) Current-voltage curves of the TiN/HfO_x/Pt device showing self-compliance positive set and negative reset switching. (b) Current-voltage curves of the Pt/HfO_x/Pt device showing unipolar resistive switching. In this case, a current compliance (CC) setting is needed to limit the current increase during the set transition.

However, SCSS is not observed in device B, as shown in Fig. 4.20(b). Set switching requires an externally imposed compliance to limit the surge in current. In addition, the type of resistance switching is changed. Unipolar switching is observed, in contrast to the bipolar switching seen in device A. Past reports [81] have attributed unipolar switching to the formation or annihilation (by Joule heating) of a metal filament. We therefore ascribe the unipolar switching in device B to Hf filament formation/annihilation. During forming or set operation, oxygen ions are drawn from the HfO_x towards the Pt electrode. Since Pt is permeable to oxygen [130], it cannot function as an oxygen reservoir, unlike TiN. The oxygen ions can easily run away through the grain boundaries of Pt in the Pt/HfO_x/Pt device, leading to possible formation of a stronger conductive filament comprising of metallic Hf. For the RESET

process, we suggest that local Joule heating may assist the rupture of Hf filaments, resulting in the device from the LRS to the HRS. The lack of SCSS in device B indicates that the besides the enablement of bipolar switching, the TiN electrode is also a necessary condition for the occurrence of SCSS in device A.

The absence of SCSS in the Pt/HfO_x/Pt device confirms that the SCSS behavior of the TiN/HfO_x/Pt device is a consequence of an interfacial interaction between the TiN and the vacancy-rich breakdown path. However, it is important to point out that the TiN electrode itself is not a sufficient condition for realizing the SCSS behavior. The stoichiometry of the TiN electrode is found to play an important role. Fig. 4.21 shows the bipolar switching behavior of the TiN/HfO_x/Pt device with a Ti-rich TiN electrode. Interestingly, SCSS is not observed and the current increase during the set transition needs to be capped by a preset current compliance in the parameter analyzer to prevent catastrophic breakdown of the device. Clearly, the Ti content in the TiN electrode is an important factor determining the occurrence of SCSS. Study is not made on a N-rich TiN electrode due to its highly resistive nature.

Fig. 4.21: Current-voltage curves of the Ti-rich TiN/HfO_x/Pt device. Unlike the device which has a near-stoichiometric TiN electrode, this device requires a preset current compliance in the parameter analyzer to limit the current increase during set transition.

4.4.3 Proposed Mechanism of SCSS

To shed more light on the above difference, the properties of near-stoichiometric TiN/HfO_x and Ti-rich TiN/HfO_x interfaces were probed by XPS measurement. The test samples consisted of HfO_x blanket-deposited over TiN/SiO₂/Si substrates, where the Ti composition in the TiN was adjusted to correspond to those in the test devices. The chemical composition of TiN was checked, which confirms that one sample has an almost stoichiometric TiN (Ti:N = 1:1.2, within experimental error) (Fig. 4.22(a)) while the other has a Ti-rich TiN (Ti:N = 2.4:1) (Fig. 4.22(b)).

Fig. 4.22: (a) Ti 2p core-level spectrum of (a) near-stoichiometric TiN; (b) Ti-rich TiN. Valence band spectrum of (c) near-stoichiometric TiN/HfO_x interface; (d) Ti-rich TiN/HfO_x interface. Band alignment of (e) near-stoichiometric TiN/HfO_x interface; (f) Ti-rich TiN/HfO_x interface.

Band alignment of the TiN_{1.2}/HfO_x and Ti_{2.4}N/HfO_x interfaces were also extracted from the XPS data. The valence band maximum (VBM) was determined from the intercept of the leading edge of the valence band spectrum of HfO_x with the base line. The Fermi position of TiN, determined by the binding energy at the middle of the leading Fermi edge of TiN, is assigned as 0 eV. The valence band offset of HfO_x, extracted from the difference between the VBM of HfO_x and the Fermi edge of TiN is

~2.0 eV for the near-stoichiometric TiN (Fig. 4.22(c)). and ~3.5 eV for the Ti-rich TiN (Fig. 4.22(d)). samples. The corresponding TiN to HfO_x conduction barrier height (ΔE_C) is 3.5 eV (Fig. 4.22(e)) and 2.0 eV (Fig. 4.22(f)).

Properties of the HfO₂/TiN interface have also been studied by others via *ab-initio* simulation. Of particular relevance is the work of Bradley *et al.* [133], who studied the TiN to HfO₂ conduction barrier height as a function of oxygen chemical potential at the TiN/HfO₂ interface. The authors reported a barrier height of 2.3 eV for an interface with a high oxygen chemical potential and a barrier height of 1.3 eV for an interface with a low oxygen chemical potential. The oxygen chemical potential reflects the concentration of oxygen interstitials at the interface. A decrease in oxygen chemical potential is marked by the interface transiting from an interstitial oxygen-rich one to an oxygen vacancy-rich one. Simulation study has shown that an energy gain of 0.9 eV results from the movement of an interstitial oxygen into a N vacancy site. A high concentration of N vacancies is present in the Ti-rich TiN. Oxygen in the adjacent oxide layer may thus tend to migrate into these vacancy sites. However, to move an interstitial oxygen from HfO₂ into an interstitial site in TiN would need at least 4.6 eV of energy. Hence, oxygen would tend to accumulate at the TiN interface in the event that there is a lack of vacancy sites they can occupy within the TiN. The larger barrier height of 3.5 eV for the near-stoichiometric TiN interface in our work may have stemmed from an accumulation of oxygen at the interface.

Based on the above analysis, we propose a physical explanation for the SCSS behavior for the near-stoichiometric TiN/HfO_x/Pt device. During the set transition, the positive voltage, applied to the TiN electrode, draws oxygen anions from the re-oxidized part of the breakdown path towards the TiN interface. As the TiN electrode is almost stoichiometric and therefore has a negligible concentration of N vacancies, these oxygen

anions would tend to pile-up at the TiN interface. The accumulation of oxygen creates a barrier and limits the conduction between the TiN electrode and the breakdown path. On the other hand, in the Ti-rich TiN/HfO_x/Pt device, the oxygen anions are likely to migrate into the TiN electrode due to the high concentration of N vacancies there. As a consequence, there is no piling up of oxygen at the TiN interface. The set current, could continue to increase as the breakdown path is further depleted of oxygen since the N-vacancy-laden TiN electrode functions as an infinite “sink” for the oxygen anions. It should be mentioned that the insights obtained from this study are not only applicable to the TiN/HfO_x interface but should also be applicable to other metal/oxide interfaces.

4.5 Summary

The role of the IL between the metal electrode and switching oxide in enabling stable CRS in the HfO_x-based single memory device was revealed. Stable CRS was enabled in the TiN/HfO_x/IL/TiN device, where a bottom IL, comprising Hf and Ti sub-oxides, resulted from the oxidation of TiN during device fabrication. In the TiN/HfO_x/Pt device where formation of the bottom IL was suppressed by the inert Pt metal, no CRS was observed. Physical switching model, based on oxygen-ion exchange between the bottom/top IL and the conductive path in HfO_x, was proposed to have caused the CRS observed in the TiN/HfO_x/IL/TiN device.

Current conduction mechanism analysis revealed that Schottky emission is a dominant conduction mechanism of the HRS in both the BRS and CRS mode due to the same top/bottom TiN/HfO_x interface in the symmetric TiN/HfO_x/TiN resistive memory device. LRS current conduction can change from semiconducting (at low voltages) to metallic (at high voltages) conduction. In the former regime, conduction may be described by the farthest-neighbor tunneling process, characterized by a trap spacing of

~ 8.3 Å along the conduction path. On the other hand, the latter regime is characterized by a metal-like mechanism with a positive temperature coefficient like that of a sputtered Hf metal film. Field-induced lowering of the tunneling barrier (~ 77 meV due to the collapsed HfO_x conduction band edge and the small trap spacing) was proposed to have caused the transition to a metal-like conduction. Due to the opposite temperature dependence of the two conduction regimes, existence of a zero temperature-coefficient of LRS resistance was observed.

An interface-controlled self-compliance set switching behavior is revealed in the TiN/ HfO_x /Pt device. In contrast to other reported devices in which an additional oxide layer is incorporated into the RRAM stack to serve as an in-built resistor for limiting the set switching current, no such oxide layer is used in the device studied here. Experimental results show that the TiN/ HfO_x interface and the stoichiometry of the TiN electrode both play a determining role. No self-compliance behavior is observed when the TiN electrode is replaced by Pt or when it is enriched with Ti. In both cases, the electrode becomes more permeable to oxygen. XPS analysis shows that the conduction barrier height at the Ti-rich TiN/ HfO_x interface is significantly reduced as compared to that at the near-stoichiometric TiN/ HfO_x interface. These observations consistently indicate that the self-compliance behavior in a single-oxide RRAM device is possible if oxygen anions pile up at the anode interface during the set evolution. The accumulation of oxygen creates a barrier, which self-arrests the increase of the set switching current.

Chapter 5 COMPLEMENTARY RESISTIVE SWITCHING PERFORMANCE IMPROVEMENT BY INTERFACE ENGINEERING OPTIMIZATION

5.1 Introduction

The observation of CRS in the TiN/HfO_x/TiN structure is particularly important as both TiN and HfO_x are already widely deployed in mainstream manufacturing. Study on complementary resistive switching of TiN/HfO_x/TiN memory device has shown that the device is highly susceptible to self-reset, i.e. the device is automatically programmed into the high resistance state during forming [79]. This is observed in the following opposite-polarity voltage sweep, in which the device exhibits a set behavior (instead of a reset as typically observed in bipolar switching mode). In the previous work, it is shown that the IL at the HfO_x/TiN interface plays a crucial role in enabling CRS, via an oxygen exchange process with the adjacent conducting filament formed in the HfO_x [68]. This mechanism allows the position of the re-oxidized filament to be alternated between the two TiN electrode interfaces, giving two distinct HRSs. The critical role of the IL is supported by the observation that CRS ceases to exist when formation of one of the ILs is prevented by replacing the TiN electrode with an inert Pt metal. The self-reset may be attributed to the migration of oxygen ions from the cathode IL into the conducting filament in HfO_x during the forming transient.

This study also has shown that a majority (70%) of TiN/HfO_x/TiN devices exhibit a large non-polar reset loop in the first post-forming voltage-sweep measurement, and

failed CRS after forming [69]. It is proposed that breakdown of the TiN/HfO_x interfacial oxide layers (crucial in enabling CRS) and the accompanied formation of Ti filaments (due to Ti migration from the TiN cathode into the breakdown path) take place, resulting in CRS failure and the observed non-polar reset behavior. Observations underscore the impact interface engineering may have on CRS performance.

5.2 Observation of self-reset during forming of the TiN/HfO_x/TiN resistive switching device

5.2.1 Experiments

Besides TiN/HfO_x/TiN control sample, test samples with a 3-nm or 6-nm Al₂O₃ layer inserted at the top or bottom TiN interface (i.e. TiN/Al₂O₃/HfO_x/TiN or TiN/HfO_x/Al₂O₃/TiN labelled as T-AIO or B-AIO, respectively), and TiN/HfO_x/Pt sample labelled as B-Pt were fabricated. Fig. 5.1 shows the high-resolution cross-sectional transmission electron micrographs for the T-AIO and B-AIO samples. The HfO_x is ~6-7 nm thick in all cases, in agreement with the targeted value.

Fig. 5.1: High-resolution cross-sectional transmission electron micrograph for the (a) T-AIO (TiN/Al₂O₃/HfO_x/TiN); and (b) B-AIO (TiN/HfO_x/Al₂O₃/TiN) devices.

As mentioned in Section 4.2.2.1, a 4-nm thick bottom IL is formed in devices with a bottom TiN electrode due to TiN oxidation during the device fabrication process. The

rationale behind the choice of different Al_2O_3 thicknesses will be elaborated later.

5.2.2 Electrical characteristic of different resistive memory device

Fig. 5.2(a) depicts the current-voltage (I - V) curves obtained during the positive-voltage forming sweep and the first negative-voltage sweep measurements made on a control device. After forming, the negative-voltage sweep should yield a reset as is commonly seen on this RRAM device (Fig. 5.2(b)).

Fig. 5.2: Current-voltage (I - V) curves (circle) of two control devices ($\text{TiN}/\text{HfO}_x/\text{TiN}$) measured during the first negative-voltage sweep after positive-voltage forming. The corresponding forming I - V curves are as shown. A majority ($\sim 90\%$) of the devices exhibit the unusual behaviour depicted in (a), as opposed to the conventional bipolar reset shown in (b). Solid lines denote I - V curve segments used for conduction mechanism analysis (cf. Fig. 5.3).

However, an initially lower current followed by an obvious increase at ~ -0.7 V is observed, denoting a set-like behavior. This is then followed by a current decrease when the voltage sweep is extended to -1 V. About 90% of control devices (> 30 tested) exhibit such a behavior during the first post-forming negative-voltage sweep measurement. The remaining devices display the conventional bipolar reset behavior (Fig. 5.2(b)). The large switching current ($\sim \text{mA}$) may be ascribed to the high forming-current compliance and non-negligible current overshoot encountered in big area devices [134], resulting in a large filament size. A smaller filament (hence lower switching current) may be achieved via device area scaling [55, 135, 136], which allows for forming at reduced compliance level and overshoot (by virtue of a

background lesser leakage current and parasitic capacitance).

5.2.3 Current conduction mechanism analysis

To shed light on the unusual behavior depicted in Fig. 5.2(a), study was made on the conduction mechanism responsible for the I - V characteristic before the increase of the current at -0.7 V (bold line). For all devices examined, the Schottky conduction model [117] yields the best fit (e.g. Fig. 5.3(a)), indicating a barrier-limited conduction mechanism. $q\phi_B$ is Schottky barrier (in eV). The extracted average barrier height is 0.34 ± 0.02 eV. This barrier height refers to a potential energy barrier at the top TiN/HfO_x interface for electrons movement from the TiN electrode to the oxygen-deficient HfO_x layer. Study was also made on the HRS I - V curve after the traditional bipolar reset in Fig. 5.2(b) (bold line). Similarly, the Schottky model gives the best fit (e.g. Fig. 5.3(b)), with an extracted average barrier height of 0.34 ± 0.05 eV. The good agreement between the conduction mechanism in devices exhibiting the unusual behavior (Fig. 5.2(a)) and the HRS conduction mechanism in devices displaying conventional bipolar reset (Fig. 5.2(b)) implies that in the former case, the devices had experienced a self-reset during the forming process. During the post-forming negative-voltage sweep, the current increase at ~ -0.7 V may be ascribed to a set switching. The subsequent current decrease, similar to that seen in Fig. 5.2(b), is a result of reset switching as is also confirmed by the good match between the forward- and reverse-sweep curves in the low voltage regime. For devices formed under a negative-voltage sweep, this set-then-reset behavior would occur during the post-forming positive-voltage sweep (not shown).

Fig. 5.3: (a) and (b) are respective $\ln I$ versus $V^{1/2}$ plots for the segments of the I - V curves marked in bold in Fig. 5.2(a) and 2(b). The linear relationship implies Schottky-limited conduction; $q\phi_B$ is the extracted barrier height. The linear best-fit lines are as shown.

The set-then-reset behavior shown in Fig. 5.2(a) is similar to the CRS behavior reported by others [65, 71]. Both bipolar and complementary switching are also observed in our devices (Fig. 5.4) regardless whether the devices first displayed the behavior shown in Fig. 5.2(a). Bipolar switching is achieved as long as the range of the voltage sweep is restricted (Fig. 5.4(a)). Extending the positive-voltage sweep after the set will trigger CRS (Fig. 5.4(b)). Here, we draw the similarity between the HfO_x/TiON stack in our control devices and the $\text{Ta}_2\text{O}_{5-x}/\text{TaO}_y$ stack shown to exhibit a CRS behavior [65]. CRS in the latter was attributed to the interchange of oxygen vacancies between the two oxide layers, which resulted in the part of the filament situated in one of the oxides being disrupted at any one time.

Fig. 5.4: Current-voltage curves of $\text{TiN}/\text{HfO}_x/\text{TiN}$ device depicting (a) bipolar set/reset; (b) CRS. The latter is triggered by extending the voltage sweep for set. Arrows show the directions of voltage sweep.

5.2.4 Physical mechanism analysis of self-reset

Following this idea, a possible mechanism for the self-reset is proposed in Fig. 5.5(a). Before forming occurs, the current is limited by the thicker HfO_x layer. Upon filament formation in the HfO_x , the bulk of the forming voltage would be instantaneously transferred across the sub-stoichiometric TiON interfacial oxide. The resultant large electric field may then draw oxygen ions from this layer into the filament in the HfO_x , disrupting the filament before the forming process can be interrupted.

Results from electrical testing made on the T-AIO and B-AIO devices support this hypothesis. With the inclusion of a 3-nm Al_2O_3 layer at the top electrode interface (T-AIO), the percentage of devices exhibiting the self-reset behavior is visibly reduced to ~50% for both forming voltage polarities (Fig. 5.5(b)). Lesser improvement is obtained for the thicker 6 nm Al_2O_3 interlayer. These outcomes may be ascribed to the relatively high electrical breakdown field (E_b) of the Al_2O_3 [137]. Dependence of E_b on Al_2O_3 thickness has been observed, with E_b exceeding 15 MV/cm for Al_2O_3 thinner than 3 nm [138]. Hence, we have chosen two Al_2O_3 thicknesses (3 and 6 nm) for hypothesis validation. By virtue of the lower dielectric constant (~9) as compared to that of TiON (~28) [139] and the relatively high E_b , the Al_2O_3 interlayer would be able to sustain the bulk of the forming voltage (once filament formation takes place in the HfO_x) with a lesser probability of suffering a breakdown before the forming process is interrupted. This in turn lowers the voltage loading on the TiON interfacial oxide and reduces oxygen migration into the adjacent filament. To support the above analysis and to understand the different results obtained for devices with 3- and 6-nm Al_2O_3 interlayers, the forming voltage distributions for the different devices are examined in Fig. 5.5(c). For positive voltage forming, the average forming voltage is ~5.5 V for the T-AIO device (with a 3-nm Al_2O_3 interlayer). Based on the dielectric constant for Al_2O_3 (9) and

TiON (28) [139], it may be estimated that ~ 3.85 V would appear across the 3-nm Al_2O_3 upon filament formation in the HfO_x . As the resultant electric field of ~ 12.8 MV/cm $< E_b$ (~ 15 MV/cm) [138], the Al_2O_3 layer would be able to sustain this voltage before the forming process is interrupted. This reduces the voltage across the TiON interfacial oxide and thus oxygen migration into the adjacent filament region. For negative voltage forming, the lower average forming voltage (-4.5 V) consistently results in the better suppression of self-reset (Fig. 5.5(b)).

Fig. 5.5: (a) Schematic diagram showing the surge in current during forming transient. With the formation of the conducting filament in HfO_x , the forming voltage is developed across the cathode interfacial oxide. The resultant large electric field drives oxygen ions into the adjacent filament, leading to filament disruption (dashed line). (b) Percentage of devices that do not show self-reset after forming for different forming polarities and device types. (c) The corresponding forming voltage distributions. Forming polarities are as shown.

However, with a thicker 6-nm Al_2O_3 interlayer (B-AIO), an increase in the occurrence of self-reset is observed. This may be ascribed to two factors: (1) the decrease in E_b , which is now ~ 9 MV/cm at this thickness [138]; (2) the increase in the forming voltage due to the larger physical thickness of the overall dielectric stack. For negative voltage forming, the average forming voltage is -8.5 V. Upon filament

formation in the HfO_x , the resultant electric field across the 6-nm Al_2O_3 layer is ~ 11.7 MV/cm, exceeding the E_b (~ 9 MV/cm) [138]. Consistently, self-reset is nearly always observed in the B-AIO devices under negative voltage forming. It is worth noting that the current conduction during forming is determined by the top TiN/ Al_2O_3 interface in the T-AIO sample. A positive (negative) voltage applied to the top TiN with respect to the bottom TiN increases (decreases) the Schottky barrier height, so a larger positive forming voltage was needed in the T-AIO device. While the current conduction during forming is determined by the Al_2O_3 /bottom TiN interface in the B-AIO sample. A positive (negative) voltage applied to the top TiN with respect to the bottom TiN decreases (increases) the Schottky barrier height, so a smaller positive forming voltage was needed in the T-AIO device.

Electrical testing of the B-Pt devices provides a further confirmation that the self-reset behavior is caused by the migration of oxygen ions from the cathode interfacial oxide into the adjacent filament in the HfO_x during forming transient. With the replacement of the bottom TiN by Pt, formation of the interfacial oxide is suppressed, as shown by the TEM result in Fig. 1(b). Consistently, self-reset is completely suppressed under positive voltage forming (Fig. 5(b)). It should be noted that testing was not performed for negative voltage forming (i.e. Pt as the anode) as no reliable resistive switching can be achieved due to the absence of a reactive anode for oxygen “storage” under this forming polarity (Fig. 5 of ref. [68]).

The mechanism for self-reset depicted in Fig. 5.5(a) should be distinguished from that proposed in Ref [71]. In the latter, the authors attributed self-reset to the continued movement of positive ions (which made up the filament) towards the cathode, leading to a disruption of the filament at the anode. The main difference thus lies in the location of the filament rupture. According to ref. [71], the B-Pt device should also display self-

reset; this is, however, clearly not the case (Fig. 5.5(b)). The results for the B-Pt devices tend to favor Fig. 5.5(a).

5.3 Complementary resistive switching performance improvement by interface engineering optimization

5.3.1 Experiments

The test devices with different oxide stack configurations: TiN/HfO_x/TiN, TiN/Al₂O₃/HfO_x/TiN with a 3-nm Al₂O₃ on top of HfO_x, and TiN/Al₂O₃/HfO_x/Al₂O₃/TiN with a 3-nm Al₂O₃ on both top and bottom HfO_x were fabricated. All test devices have a same HfO_x thickness of ~6-7 nm and a ~4 nm thick IL on the bottom TiN electrode. Fig. 5.6(a) shows the HRTEM for the TiN/Al₂O₃/HfO_x/Al₂O₃/TiN devices. The HRTEMs of TiN/HfO_x/TiN and TiN/Al₂O₃/HfO_x/TiN devices refer to Fig. 4.2(a) and Fig. 5.1(a), respectively.

Fig. 5.6: (a) High-resolution cross-sectional transmission electron micrograph for the TiN/Al₂O₃/HfO_x/Al₂O₃/TiN device. (b) Energy-dispersive X-ray analysis of the Ti element concentration within the HfO_x layer of the TiN/HfO_x/TiN, TiN/Al₂O₃/HfO_x/TiN, and TiN/Al₂O₃/HfO_x/Al₂O₃/TiN devices after positive-voltage forming. The evidently lower Ti element concentration, especially for the device with a thin Al₂O₃ incorporated at both TiN/HfO_x interfaces.

EDX analysis of Ti element concentration within the HfO_x layer was carried out on the test devices after positive-voltage forming, as shown in Fig. 5.6(b). The EDX result

is discussed in the later part.

5.3.2 Electrical characteristic of different resistive memory device

CRS in the single TiN/HfO_x/TiN device is characterized by the two sets of HRS I-V curves, each comprising two curves (symbol and thick line), in the positive- and negative-voltage regimes (Fig. 5.7). The CRS behavior may be attributed to the exchange of O between the top and bottom IL and the respective adjacent filament regions, as explained in Fig. 4.8 of Chapter 4. After forming using a positive-voltage ramp (not shown), the device is in the LRS and a negative-voltage sweep yields curve 1. A sufficiently negative voltage ($\leq V_{n,pk}$) resets the device to HRS as shown by curve 2. The process can only be reversed by a positive-voltage sweep, which gives curve 3. When a sufficiently positive voltage ($\sim V_{p1}$) is developed, setting the device back to the LRS. More importantly, a further increase of the positive voltage ($\geq V_{p,pk}$) would reset the device again to HRS. Repeating the positive-voltage sweep yields curve 4, with a lower current level between V_{p1} and V_{p2} . A subsequent negative-voltage sweep would yield curve 5.

Fig. 5.7: CRS in the TiN/HfO_x/TiN device after positive-voltage forming. The order of the voltage-sweep measurements is denoted by the numbers shown.

However, only a small fraction (less than 30%) of the tested devices (>30) exhibit the stable CRS (that can last several thousands of voltage-sweep cycles) shown in Fig.

5.7. The initial post-forming I-V curves for the rest of the devices are similar to the examples shown in Fig. 5.8, which evolve quickly to a switching failure. But a noteworthy feature should be mentioned. In every such device, a large reset loop (curve 1) can always be observed during the immediate sweep measurement made after forming, regardless of the voltage polarity. The switching ratio, defined as (I_{LRS}/I_{HRS} @ ± 0.2 V), is typically > 100 , much larger than the ratio of ~ 10 -20 for devices that display stable CRS. This large reset loop is only seen once and it is reproduced again in later sweep measurements. An ensuing inverted-polarity sweep would typically yield a small current increase followed by a decrease (curve 2), which may appear similar to the set-then-reset feature of CRS. However, this behavior is also observed once only at the initial stage. Subsequent alternating sweeps would no longer yield any switching (curve 3).

Fig. 5.8: Examples of large non-polar reset and failed complementary resistance switching seen in a majority ($\sim 70\%$) of the TiN/HfO_x/TiN devices. The order of measurements is indicated by the numbers. Both devices were formed by a positive-voltage sweep.

5.3.3 Physical mechanism analysis

It should be mentioned that the large non-polar reset seen in Fig. 5.8(a) and 5.8(b) is atypical of the TiN/HfO_x/TiN device, which commonly displays a bipolar switching behavior [140]. On the other hand, a large non-polar reset is usually found in devices

with a Ni or Pt electrode (e.g. Ni/HfO₂/p⁺-Si [140], Pt/HfO_x/Pt [141]) and is often associated with the formation of a metal filament in the oxide. It is believed that such a filament may be melted by Joule heating, and therefore a reset to the HRS can occur, during a voltage sweep involving either polarity [19]. The observation of a large non-polar reset in Fig. 5.8(a) and 5.8(b) thus suggests that Ti filaments (since the test device has TiN electrodes) were generated during forming.

In an earlier study [68], it is shown that the IL's at the TiN/HfO_x interfaces play a crucial role in enabling CRS. Eliminating the bottom IL by replacing the TiN with an inert Pt electrode also disables CRS; the resultant TiN/HfO_x/Pt structure only displays the conventional bipolar resistance switching. The failed CRS in the majority of the TiN/HfO_x/TiN devices thus suggests that the IL's might also have suffered a breakdown during forming. It has been reported that the average breakdown field E_b of a 10-nm TiO₂ film, reactively sputtered on a metal electrode and annealed at 600 °C is ~3 MV/cm [142]. Considering the thickness t_{ox} dependence of E_b ($\propto t_{ox}^{-\alpha}$; $\alpha \sim 0.5-1$) [143], the breakdown field (voltage) of the 4-nm IL is likely to be < 7.5 MV/cm (< 3 V), given that it is a sub-stoichiometric TiO_x formed at a lower temperature (250 °C). Thus, it is likely to also suffer a breakdown following the breakdown of the HfO_x (the average forming voltage is 4.4 V). After the IL has suffered a breakdown, O exchange with the adjacent filament region can no longer happen. In addition, as the breakdown of the IL's leads to a direct shorting of the TiN electrodes, the resultant current surge may cause the migration of Ti from the cathode into the breakdown path (supported by later results). *Ab-initio* simulation has shown that the energy barrier for metal-ion migration in an oxide is reduced in a region with a high vacancy defect concentration [132]. Thus, Ti migration into the breakdown path, aided by the electron “wind”, may easily occur. A large non-polar reset loop (Figs. 5.8(a) and 5.8(b)) then occurs during a post-forming

voltage sweep when the Ti filament is ruptured by a local heating effect [19]. Thus, to ensure CRS functionality, the IL's must be able to withstand the forming voltage, upon filament formation in the main oxide layer, until the forming process is interrupted.

To check our proposition, test devices with a thin layer of Al_2O_3 (~3 nm) incorporated at either one or both TiN/HfO_x interfaces (i.e. $\text{TiN}/\text{Al}_2\text{O}_3/\text{HfO}_x/\text{TiN}$, $\text{TiN}/\text{Al}_2\text{O}_3/\text{HfO}_x/\text{Al}_2\text{O}_3/\text{TiN}$) were fabricated and tested. The primary purpose of the Al_2O_3 is two-fold: 1) To “absorb” the forming voltage upon filament formation in the HfO_x . This would help reduce the electric field across the filament and the surge in the current. 2) To subsequently serve as a “reservoir” for O exchange with the adjacent filament region for enabling CRS. To fulfill these roles, the Al_2O_3 must not breakdown during forming and this constitutes the main consideration in its choice as elaborated below. With a lower permittivity, the E_b of Al_2O_3 is inherently higher than that of HfO_2 ; the theoretical E_b of Al_2O_3 is ~13 MV/cm whereas that of HfO_2 is ~5 MV/cm [137]. In addition, it has been shown that the E_b of ALD Al_2O_3 is increased as its thickness is decreased; for a 3 nm Al_2O_3 , its E_b ~14 MV/cm which corresponds to a breakdown voltage of ~4.2 V [138]. In addition, Al_2O_3 has a larger oxygen-vacancy formation energy and migration barrier energy as compared to HfO_2 [144]. In these regards, it is expected that the thin Al_2O_3 layer would be able to sustain the forming voltage upon filament formation in the HfO_x , until the forming process is interrupted.

The testing results support our proposition. The percentage of devices, with a 3-nm Al_2O_3 layer inserted between the TE and HfO_x , which exhibits a large reset loop and failed CRS is reduced to 50% and 20%, respectively, for positive- and negative-voltage forming. More importantly, with the inclusion of a 3-nm Al_2O_3 layer at both TiN/HfO_x interfaces, devices displaying a large reset loop and failed CRS are totally eliminated. With two Al_2O_3 layers, a smaller voltage load appears across each layer, reducing the

probability of Al_2O_3 breakdown. For devices with a Al_2O_3 layer included at the TE interface only, the significantly fewer cases of large non-polar reset and failed CRS under negative-voltage forming, as compared to positive-voltage forming, implies that Ti migration into the breakdown path originates from the cathode during the forming transient. This is because under negative-voltage forming, the Al_2O_3 layer is situated directly next to the TiN cathode and could therefore effectively suppress the surge in current and Ti migration. However, the sub-stoichiometric TiO_x interfacial layer is a much poorer barrier against the electron wind and Ti migration under positive-voltage forming [132]. These observations are consistent with the results from energy-dispersive X-ray analysis carried out on the test devices after positive-voltage forming. As shown in Fig. 5.6(b), Ti concentration in the HfO_x is marginally reduced in the device that has the Al_2O_3 layer included at the TE interface but a much greater reduction is obtained in the device that has Al_2O_3 layers incorporated at both interfaces.

Based on the experimental results, a possible explanation for the high percentage of TiN/ HfO_x /TiN devices that fail to display CRS after forming is proposed (Fig. 5.9). Because of the higher permittivity of the TiO_x IL's, the major portion of the applied voltage is initially developed across the thicker HfO_x layer [142]. When the formation of a low-resistance path occurs in the HfO_x due to the build-up of vacancy defects to a critical level, the bulk of the applied voltage would now be transferred to the TiO_x IL's. Owing to the relatively low breakdown field of the TiO_x [137], the IL's may breakdown before the forming process can be interrupted. Coupled with the surge in electron "wind", the presence of a region of a high concentration of vacancy defects next to the TiN cathode would in turn facilitate the migration of Ti into the breakdown path (Fig. 5.9(a)) [132]. Due to the random nature of oxide breakdown and ion migration, breakdown regions comprising filaments complete Ti filaments (Fig. 5.9(b)) and composite Ti-

vacancy filament (Fig. 5.9(c)) may be formed within the device area.

Fig. 5.9: The direct short between the top and bottom TiN electrodes, due to breakdown of the HfO_x and ILs, triggers a surge in electron wind (arrows) and accompanying migration of Ti ions from the cathode into the breakdown path, resulting in the formation of (b) a complete Ti filament and (c) a Ti-vacancy composite filament.

During a subsequent voltage sweep, Joule heating causes the melting (rupture) of the Ti filaments [19], when the local temperature exceeds the melting point. Although the melting point of bulk Ti is relatively high (1668 °C), a remarkable dependence on size and structure have been observed [145]. From molecular dynamics simulation, a significant decrease of the melting point to <450 °C is found for Ti nanowires [145]. It has been estimated that the local filament temperature due to Joule heating may approach hundreds of degree Celsius for several milliamperes of current [146]. It is thus possible for the Ti filaments to melt during the post-forming voltage-sweep measurement, resulting in the large reset loop observed (Figs. 5.8(a); 5.8(b)). The gradual reset behavior may be ascribed to the size (hence melting temperature) distribution of the Ti filaments. Since the range of the applied voltage during post-forming measurement is restricted, reformation of the Ti filaments does not occur and therefore the large reset loop is not obtained again. With the IL's also suffered breakdown during forming, CRS is not observed since O exchange with the adjacent filament region in the HfO_x now cannot occur. Possible redistribution of Ti ions and

remnant O ions in the Ti-vacancy composite filaments during the inverted-polarity sweep following the large reset may account for the minor current hysteresis seen in Figs. 5.8(a) and 5.8(b).

5.4 Summary

Study on complementary resistive switching of TiN/HfO_x/TiN memory device showed an unusually high occurrence of a self-reset behavior during post-forming opposite- voltage-polarity sweep measurement. The similarity between this behavior and complementary resistive switching implies that the formed filament is at the same time disrupted during the forming process. Interestingly, the self-reset behavior was (1) suppressed in devices with a thin Al₂O₃ layer inserted in-between the TiN and HfO_x; (2) completely eliminated in devices with the TiN cathode replaced by Pt. These results are consistent with a hypothesis that ascribes the self-reset to the migration of oxygen ions from the cathode interfacial oxide into the conducting filament in the HfO_x during the forming transient, thus resulting in the disruption of the filament. With the reduction in “voltage loading” across the cathode interfacial oxide during forming transient in devices with the Al₂O₃ interlayer and the elimination of interfacial oxide in devices with the Pt cathode, the occurrence of self-reset is reduced or eradicated.

Our study also showed that a large percentage of the TiN/HfO_x/TiN RRAM device fails to exhibit CRS after forming. These devices exhibited a large non-polar reset loop typical of devices for which the resistance reset is driven by Joule-heating induced dissolution of metal filaments. IL (crucial in enabling CRS) breakdown is proposed as the cause of the metal (Ti) filament formation and CRS failure in the TiN/HfO_x/TiN device. Our proposition is supported by the significant reduction or complete elimination of the large non-polar reset and CRS failure in devices with a thin Al₂O₃

layer incorporated at the TiN-cathode/HfO_x or both TiN/HfO_x interfaces. The higher breakdown field of the thin Al₂O₃ enables it to withstand the forming voltage (upon filament formation in the main oxide) until the forming process is interrupted. With the integrity of the barrier oxide layer ensured, stable CRS can be achieved.

Chapter 6 SINGLE ITO/HFO_x/TiN COMPLEMENTARY SWITCH WITH A WIDE READ MARGIN FOR SELECTOR-LESS CROSSBAR RRAM APPLICATION

6.1 Introduction

Two major issues faced in the CRS in the RRAM device are 1) the fact that the underlying mechanism of CRS is not clear; 2) a narrow read voltage window of CRS, i.e. the difference between the set and reset voltages (V_{set} and V_{reset}) is small, and in conjunction with the inherent variations in V_{set} and V_{reset} , an unacceptably small read margin would result [19, 65, 67, 70, 71, 91, 92]. The underlying mechanism of CRS has been clarified in our work. This chapter will mainly cover the narrow read margin issue existing in CRS.

Fig. 6.1(a) exhibits the CRS characteristics of TiN/HfO_x/TiN device [68]. After write operation (V_{reset}), the device always remains one of two distinct high resistance states (HRS1 or HRS2), enabling the elimination of sneak current problem. However, a narrow “voltage window” (~ 0.3 V in this device) is observed. Considering the inherent variations in V_{set} and V_{reset} , an unacceptably small read margin (~ 0.1 V) would result (Fig. 6.1 (b)), which in turn not only would result in a wrong read-out but also a change in the stored bit. A worst-case scenario in a selector-less crossbar array (Fig. 6.1(c)) where memory bits are denoted by either HRS1 or HRS2 is considered that a cell, in HRS1, selected for reading has the minimum V_{reset} (Fig. 6.1(d)). A small positive

variation in the read voltage pulse, instead, would write the selected cell to HRS2, i.e. change the stored bit from HRS1 to HRS2.

Fig. 6.1: (a) Complementary switching characteristics of the TiN/HfO_x/TiN resistive memory device. Two distinct high resistance states are evident (HRS1 – read-destructive, and HRS2 – non-destructive for the positive-voltage reading). The device read window is generally small (~ 0.3 V in this example). (b) Inherent distribution of the set and reset voltages, V_{set} and V_{reset} , respectively, makes the array read window unacceptably narrow (~ 0.1 V). (c) Schematic diagram of a selector-less crossbar array where memory bits are denoted by either HRS1 or HRS2. A cell in HRS1 is selected for reading. (d) Worst-case scenario where the selected cell in (c) has the minimum V_{reset} . A small positive variation in the read voltage pulse (dotted line) not only would result in a wrong read-out as HRS2 but also a change in the stored bit from HRS1 to HRS2.

To our best knowledge, reported RRAM devices with CRS characteristics generally give a narrow read margin (~ 0.5 V), as listed in Table I [19, 65, 67, 68, 70, 71, 91, 92]. Complex stack engineering [147] has been attempted to enlarge the voltage window. In this work, we demonstrate the CRS capability in the single-stack ITO/HfO_x/TiN RRAM device with a large read window.

Table 6.1: Resistive memory devices displaying complementary switching and their respective voltage windows (i.e. difference between V_{set} and V_{reset}) reported to-date. (* no voltage distribution data available; ** original definition based current “plateau” erroneous.)

Stack	Voltage Window (V)	Read Margin (V)
Pt/SiO ₂ /GeSe/Cu/GeSe/SiO ₂ /Pt [19]	0.7	< 0.7*
Pd/Ta ₂ O _{5-x} /TaO _y /Pd [65]	0.6	< 0.6*
W/Nb ₂ O _{5-x} /NbO _y /Pt [67]	0.7	< 0.7*
TiN/HfO _x /TiN [71]	0.5	< 0.5*
Pt/ZrO _x /HfO _x /TiN/HfO _x /ZrO _x /TiN [91]	0.4	< 0.4*
W/ZrO _x /HfO _x /TiN/Ir/TiO _x /TiN [92]	0.4**	< 0.4*
Al/Ni/NiAlO _x /Al ₂ O _{3-x} /ITO [147]	1.9	< 1.9*
ITO/HfO _x /TiN(<i>this work</i>)	1.6	1.1

6.2 Fabrication of ITO/HfO_x/TiN nano-crossbar RRAM device

Electron-beam lithography (EBL) was first performed on a pre-cleaned SiO₂/Si substrate, following by TiN deposition by DC reactive magnetron sputtering and lift-off to form the TiN electrode. Atomic layer deposition of the HfO_x layer at 250 °C then proceeded with tetrakis (dimethylamino) hafnium as the precursor and H₂O as the oxidizing agent. After the second EBL patterning step, ITO deposition (via physical sputtering of a commercial ITO target with ~5 wt. % Sn in an argon-only ambient) followed by lift-off were carried out to form the ITO electrode. For comparison, symmetric TiN/HfO_x/TiN devices, only substituting the top ITO electrode by TiN, were also fabricated. To facilitate later discussion, the former will be referred to as the ITO device, while the latter as the TiN device.

6.3 Physical analysis

6.3.1 SEM analysis

Fig. 6.2 shows a low- and high-magnification scanning electron microscopy image of the ITO/HfO_x/TiN crossbar memory device with a dimension of 300 nm (TiN bottom electrode) by 200 nm (ITO top electrode).

Fig. 6.2: (a) Low- and (b) high-magnification scanning electron micrographs of the ITO/HfO_x/TiN crossbar resistive memory device. Dimensions of the TiN bottom electrode and ITO top electrode are as indicated.

6.3.2 Cross-sectional TEM and EDX analysis

High-resolution cross-sectional transmission electron microscopy showed a ~6-7 nm thick HfO_x (Fig. 6.3(a)). The bright shade between the HfO_x and TiN may refer to an interfacial oxide formed by the oxidation of the exposed TiN surface during initial ALD cycles. Element distributions across the stack obtained from energy dispersive spectroscopy (Fig. 6.3(b)).

Fig. 6.3: (a) High-resolution cross-sectional transmission electron micrograph of the ITO/HfO_x/TiN stack. (b) Element distributions across the stack obtained from energy dispersive spectroscopy. The finite beam size has resulted in artificial broadening of the interfacial layers (ILs).

6.3.3 XPS analysis

XPS measurement, using an Al $K\alpha$ (1486.6 eV) source, was made on samples having a 7-nm HfO_x (Fig. 6.3(a)) blanket-deposited on either a bottom TiN or ITO electrode to check the impact of the electrode material on the HfO_x stoichiometry (Fig. 6.4). °). The XPS test samples were fabricated under the same conditions as those of the crossbar devices. The Hf $4f$ and O $1s$ core-level spectra, and their corresponding constituent component spectra, are shown in Fig. 6.5. Analysis revealed a Hf:O ratio of 1:1.4 for the HfO_x layer in the HfO_x /ITO stack, as compared to a ratio of 1:1.7 in the HfO_x /TiN stack. The lower oxygen ratio for the HfO_x /ITO stack indicates that oxygen in the HfO_x may have been “scavenged” by the bottom ITO layer.

Fig. 6.4 Schematic cross-sectional diagram of (a) HfO_x /ITO and (b) HfO_x /TiN stacks used in the XPS measurement.

A check on the XPS sampling depth was also made with reference to the inelastic mean free path (IMFP) of the Hf $4f$ photoelectrons. The kinetic energy of Hf $4f$ photoelectrons is ~1469 eV (photon energy (1486.6 eV) minus the binding energy of Hf $4f$ (~18 eV)), giving an IMFP of ~2.9 nm (based on the TPP-2M (Tanuma-Powell-Penn) method [148] adopted in the NIST database [149]). The XPS sampling depth, typically taken as $3 \times \text{IMFP}$, is ~8.7 nm for a 0° detection angle. Hence, the extracted stoichiometry is indicative of the entire 7-nm HfO_x film.

Fig. 6.5: Hf 4f and O 1s core-level spectra of the (a) ITO/HfO_x/TiN and (b) TiN/HfO_x/TiN stacks. The respective Hf:O ratios are 1:1.4 and 1: 1.7. Symbol denotes experimental data and lines denote component spectra and best fit curve.

6.4 Complementary resistance switching characteristics in the ITO/HfO_x/TiN nano-crossbar memory device

DC voltage-sweep testing was performed at room temperature (27 °C) using a Keithley SCS4200 parameter analyzer. The voltage-bias was applied to the top ITO or TiN electrode with the bottom TiN electrode always grounded. Pulsed read/write testing was also carried out using the Agilent B1530A WGF MU module in a B1500A parameter analyzer.

Fig. 6.6 shows typical CRS behaviors of the ITO and TiN devices. Forming was carried out using a positive-voltage sweep (not shown) to create a conductive filament within the HfO_x layer so that subsequent resistive switching effect could be observed. For the ITO device (Fig. 6.6(a)), a positive-voltage sweep triggers a high to low resistance (HRS1→LRS) or set transition @ $V_{\text{set}}^+ \sim 0.2$ V. If the voltage sweep is stopped after this set transition, the device can only be reset by a negative-voltage sweep (@ $V_{\text{reset}}^- \sim -1$ V), i.e., it exhibits a typical positive set/negative reset bipolar switching behavior. However, if the positive-voltage sweep is further extended, a reset subsequently happens @ $V_{\text{reset}}^+ \sim 1.5$ V, bringing the device to a different high-resistance

state (HRS2). Following this reset, the device can no longer be set again using a positive-voltage sweep. Instead, it can only be set by a negative-voltage sweep ($@V_{\text{set}}^- \sim -0.4$ V), and reset by a positive-voltage sweep ($@V_{\text{reset}}^+ \sim 1.5$ V), i.e., the device now operates in a complementary switching mode (negative set/positive reset). An extension of the negative-voltage sweep yields a reset $@V_{\text{reset}}^- \sim -1$ V to HRS1, after which the device is changed back to the positive set/negative reset mode. The device may be alternated between the two switching modes by extending the voltage sweep beyond the initial set transition (Fig. 6.7). A similar behavior is obtained for the TiN device (Fig. 6.6(b)).

Fig. 6.6: Typical complementary resistive switching behavior of the (a) ITO/HfO_x/TiN, and (b) TiN/HfO_x/TiN RRAM devices. “TE” denotes top (ITO) electrode.

Fig. 6.7: Current-voltage curves of the ITO/HfO_x/TiN crossbar RRAM device. The device can be toggled between the positive set/negative reset and negative set/positive reset switching mode by extending the respective set voltage-sweep beyond the initial set voltage.

A comparison of the CRS characteristics of the ITO and TiN devices reveals two

major differences. First, for most of the ITO devices tested, the resistance of HRS1 is significantly higher than that of HRS2 (cf. Fig. 6.6(a)). The respective resistance distributions differ by a factor of $>10^3$ at the median value (Fig. 6.8(a)). This is in contrast to the comparable HRS1 and HRS2 of the TiN device (Fig. 6.8(b)). However, both devices can be set to nearly the same LRS regardless of the set-voltage polarity and the initial HRS. It is pertinent at this juncture to clarify that the significantly lower HRS2 resistance (or higher current) of the ITO device would not pose any problem for array level CRS operation. Electrically, HRS1 and HRS2 are not distinguished by the difference in their current or resistance values, but by their different responses to a read voltage bias. A positive voltage larger than V_{set}^+ would trigger a HRS1→LRS transition (Fig. 6.6(a)), since the ruptured filament next to the ITO interface is reconnected to the ITO (via oxygen migration from the ruptured filament to the ITO (cf. Fig. 6.10)). However, it has no effect if the device is in the HRS2 state, since the voltage polarity does not favor oxygen migration from the ruptured filament back to the adjacent TiN electrode. Similarly, a read voltage more negative than V_{reset}^- would trigger a HRS2→LRS transition but has no effect if the device is in the HRS1 state.

Fig. 6.8: Distributions of the low-resistance state, and high-resistance state (HRS1 and HRS2) resistances in the positive- and negative-voltage regimes for the (a) ITO/HfO_x/TiN, and (b) TiN/HfO_x/TiN RRAM devices.

Second, the V_{set} and V_{reset} of the ITO device show a larger difference of 1.6 V (median) in the positive-voltage regime as compared to the 0.7 V in the negative-voltage

regime (Fig. 6.9(a)), whereas they differ comparably (0.5 V) in both voltage regimes for the TiN device (Fig. 6.9(b)). After accounting for the spread in voltages, the difference between the upper end of V_{set}^+ and the lower end of V_{reset}^+ distributions (defined as the read margin) in the positive-voltage regime is 1.1 V for the ITO device, substantially larger than the 0.13 V for the TiN device. On the other hand, the read margin in the negative-voltage regime is comparable for both devices (0.2 V versus 0.15 V).

Fig. 6.9: Distribution of the set and reset voltages in the positive- and negative-voltage regimes for the (a) ITO/HfO_x/TiN and (b) TiN/HfO_x/TiN RRAM devices. As indicated are the respective read windows and margins in both voltage regimes.

6.5 CRS model of ITO/HfO_x/TiN resistive memory device

An oxygen-exchange mechanism between the oxygen vacancies in the conducting filament formed in the HfO_x and the ITO or TiN electrode, adopted from our earlier study on the CRS behavior of the TiN/HfO_x/TiN device [68], may also be used to explain the CRS behavior in the ITO device (Fig. 6.10). A conducting filament, comprising oxygen vacancies, is generated in the HfO_x after forming [2, 124, 126, 150-152] (center). A negative-voltage sweep drives oxygen from the top ITO interface region to the adjacent vacancy sites in the filament, rupturing the filament (center→right) and causing a reset to HRS1. A subsequent positive-voltage sweep reconnects the filament (right→center) and causes a set by reversing the oxygen migration process. An extended

positive-voltage sweep would draw oxygen from the bottom TiN interface region into the adjacent filament and in turn ruptures the filament there (center→left), resetting the device to HRS2. The change in the position of the filament rupture distinguishes this HRS2 from the previous HRS1 (right), giving this device its CRS capability.

Fig. 6.10: Schematic illustration of oxygen-ion exchanges between the vacancy-filled conducting filament and ITO and TiN interfacial layers (ILs). Center – Fully formed filament gives rise to a low resistance path between the two electrodes. Right – A negative voltage applied to the ITO electrode drives oxygen ions within the IL down to the filament; recombination with the vacancies there disrupts the filament, causing a reset. A positive voltage draws oxygen ions from the ruptured part of the filament back to the ITO IL and reforms the filament. Left – An extension of the positive voltage sweep draws oxygen ions from the TiN IL into the adjacent filament region, rupturing the filament. After this, only a negative voltage could reform the filament and the device is thus switched to the complementary state. The two high resistance states are distinguished by the different locations of the filament rupture.

Table 6.2 summarizes the median V_{set} and V_{reset} values for the positive- and negative-voltage regimes, together with the filament change that occurred for each voltage, and a notation denoting the direction of oxygen transfer between the filament and the electrode for both devices. Take the V_{set}^+ of the ITO device for instance, which corresponds to the reconnection of the ruptured filament next to ITO (Figs. 6.6(a); Fig.10). This change arises from the migration of oxygen from the ruptured filament (HfO_x) to the ITO, and the process is denoted as $\text{O}_{\text{HfO}_x} \rightarrow \text{ITO}$. At V_{reset}^+ , the filament next to TiN is ruptured and the oxygen transfer process is denoted as $\text{O}_{\text{TiN}} \rightarrow \text{V}_\text{O}$ (V_O

denotes vacancy sites of the filament). It is clear from Table 6.2 that the enlarged positive read window of the ITO device is due to the reduction in V_{set}^+ and the increase of V_{reset}^+ , relative to those of the TiN device. The analysis implies 1) it is easier for oxygen to migrate from the ruptured filament to ITO ($V_{\text{set}}^+ = 0.2$ V) than to TiN ($V_{\text{set}}^+ = 0.6$ V); 2) it is more difficult for oxygen to migrate from the bottom TiN to adjacent vacancy sites of the filament in the ITO device ($V_{\text{reset}}^+ = 1.8$ V) than in the TiN device ($V_{\text{reset}}^+ = 1.1$ V).

Table 6.2: Summary of CRS voltages, location of filament change and direction of oxygen transfer between filament and electrode.

Device	Median Switching Voltage	Filament Change	Oxygen transfer
ITO/HfO _x /TiN	$V_{\text{set}}^+ = 0.2$ V	reformed @ITO	O _{HfO_x} →ITO
	$V_{\text{reset}}^+ = 1.8$ V	ruptured @TiN	O _{TiN} →V _O
	$V_{\text{set}}^- = -0.3$ V	reformed @TiN	O _{HfO_x} →TiN
	$V_{\text{reset}}^- = -1.1$ V	ruptured @ITO	O _{ITO} →V _O
TiN/HfO _x /TiN	$V_{\text{set}}^+ = 0.6$ V	reformed @TiN _{top}	O _{HfO_x} →TiN _{top}
	$V_{\text{reset}}^+ = 1.1$ V	ruptured @TiN _{bot}	O _{TiNbot} →V _O
	$V_{\text{set}}^- = -0.6$ V	reformed @TiN _{bot}	O _{HfO_x} →TiN _{bot}
	$V_{\text{reset}}^- = -1.1$ V	ruptured @TiN _{top}	O _{TiNtop} →V _O

6.6 Physical mechanism of enlarged CRS voltage window and read margin

Since both devices have the same bottom TiN electrode, the above differences may be ascribed to the different top electrodes. In our device, ITO electrode was prepared in an argon-only ambient. Studies [153, 154] have found that an ITO film sputter-deposited in an argon-only (i.e. oxygen-absent) ambient has a high concentration of oxygen vacancies, which give the film an n-type conductivity. An oxygen deficient ITO layer in turn promotes the migration of oxygen from the HfO_x layer [155], thus making the latter also more oxygen deficient. The XPS analysis (Fig. 6.5) shows that the ITO electrode has a stronger affinity for oxygen than the TiN electrode. This may explain

the smaller V_{set}^+ of the ITO device.

To shed light on point (2), It should be noted that the V_{reset}^+ of the TiN device (1.1 V) is smaller than that of the ITO device (1.8 V), despite in both cases, the reset involves the rupture of filament due to oxygen migration from the bottom TiN electrode. The large difference between HRS1 and HRS2 of the ITO device provides a clue on the effect of the ITO electrode on electrical conduction through the stack.

6.7 Current conduction mechanism analysis

A study on the current conduction mechanism was made to understand the above mentioned point (2). Among the various transport models (Poole-Frenkel, Schottky, space-charge limited, and quantum point contact) proposed for RRAM current conduction in HRS, the Schottky model is found to give the best fit to the experimental data. According to the Schottky conduction model, the current density J may be expressed as [117, 118]:

$$J = A^* T^2 \exp \left[\frac{-q(\phi_B - \sqrt{qE/4\pi\epsilon})}{kT} \right] = C_1 \exp \left(-\frac{q\phi_B}{kT} + C_2 \sqrt{V} \right) \quad (1)$$

where $C_1 (= A^* T^2)$, $C_2 \left(= \frac{1}{kT} \sqrt{\frac{q}{4\pi\epsilon d}} \right)$ are constants for a given interface structure and temperature T ($A^* = 120 \text{ A cm}^{-2} \text{ K}^{-2}$ is Richardson constant [156]; k is Boltzmann constant; q is electronic charge; d is the effective barrier thickness; ϵ is permittivity) and $q\phi_B$ is Schottky barrier (in eV). As is apparent in Fig. 6.11, a very good least-square linear regression fit ($R^2 > 0.98$) to the experimental data can be obtained on a $\ln I$ versus $V^{1/2}$ plot, implying that conduction in HRS1 and HRS2 are limited by Schottky emission. The extracted Schottky barrier is 0.49 eV and 0.17 eV for the ITO/HfO_x and HfO_x/TiN interface, respectively. The substantially lower current (or higher resistance) for HRS1 may thus be explained by the larger Schottky barrier at the ITO/HfO_x interface. Studies

on the tunneling current characteristics of ITO/HfO₂/Si and TiN/HfO₂/Si structures have also found a larger ITO/HfO₂ Schottky barrier [157, 158].

Fig. 6.11: $\ln I$ versus $V^{1/2}$ plot showing a good fit of the Schottky conduction model to the current-voltage characteristic of the (a) HRS1 and (b) HRS2 states of the ITO/HfO_x/TiN device. The extracted Schottky barrier $q\phi_B$ for each case is as indicated. (c) Schematic energy band diagram of the ITO/filament/TiN configuration, showing the presence of a Volta potential $\Delta\psi$ arising from the different work functions of the ITO and TiN electrodes. The band structure of the filament is omitted due to uncertainties on its chemical composition and shape. Variation in $\Delta\psi$ across the structure is represented by a simplified linear variation of the vacuum level E_{Vac} . $E_{F,ITO}$ and $E_{F,TiN}$ denote the Fermi level of the ITO and TiN electrode, respectively.

The larger Schottky barrier at the ITO/HfO_x interface implies that the ITO electrode has a larger work function than the TiN electrode. This inference is in general agreement with the work function of ITO and TiN reported elsewhere; e.g. 5.3 eV for ITO [159] and 4.5 eV for TiN [160]. Due to the work function difference, a Volta potential, $\Delta\psi$ exists between the ITO and TiN electrodes in both the high- and low-resistance states (Fig. 6.11(c)). Because of the larger ITO work function, the polarity of $\Delta\psi$ is such that it opposes (reinforces) a positive (negative) voltage applied to the ITO with respect to the TiN. The opposition between the $\Delta\psi$ and positive applied voltage means that a more positive voltage is needed to cause a reset, which explains the increase in V_{reset}^+ of the ITO device. An increase in V_{set}^+ should also be expected but the stronger oxygen affinity of ITO may have offset the increase, resulting in an overall decrease relative to the TiN

device. A comparison of V_{set}^- and V_{reset}^- of the two devices (Table 6.2) also consistently reflects the possible role of $\Delta\psi$ in the resistive switching voltages of the ITO device in the negative-voltage regime. The V_{set}^- of the ITO device is -0.3 V, less negative than that of the TiN device (-0.6 V), despite in both cases, the set involves reconnection of the ruptured filament at the TiN interface, by oxygen migration from the ruptured filament to TiN. But this difference in V_{set}^- of the two devices is smaller than the difference in V_{reset}^+ . The reason for this discrepancy is not clear and is a subject of further investigation. As for V_{reset}^- , a more negative value should be expected for the ITO device, in view of the stronger oxygen affinity of ITO and hence a greater difficulty for oxygen to migrate from ITO back to the filament. However, the V_{reset}^- of both devices are similar (1.1 V), implying that the Volta potential in the ITO device may have helped reduce the reset voltage (as it reinforces the negative applied voltage). On the other hand, no Volta potential should exist in the symmetrical TiN/HfO_x/TiN stack and thus the TiN device shows identical set and reset voltages in both voltage regimes (Table 6.2). Our explanation on the effect of electrode work-function difference on the switching operation of the ITO device is supported by the study of Hadi *et al.* [161], who reported a set-voltage increase for the W/CeO_x/SiO₂/n⁺Si stack relative to the W/CeO_x/SiO₂/p⁺Si stack, arising from a decrease of the work function of the n⁺ Si electrode relative to the top W electrode.

On the other hand, conduction in the LRS is ohmic (Figs. 6.12), with similar average resistances regardless of the set-voltage polarity and initial HRS (Fig. 6.8(a)).

Fig. 6.12: The LRS after (c) positive and (d) negative set both show ohmic conduction. Symbol denotes experimental data and line shows the best linear fit.

6.8 Memory (resistance) window

The smaller difference between LRS and HRS2 in the positive regime limits the memory window. The difference in the median resistances of $\sim 85\times$ (Fig. 6.13) is relatively narrow, typical of the HfO_x/TiN stack. Statistical variations in LRS and HRS2 further degrade the ratio, resulting in a worst-case value of $\sim 6\times$. Nonetheless, the insight that HRS2 conduction is limited by the HfO_x/TiN Schottky barrier (Figs. 6.11(b), 6.10(left)) offers the prospect for further memory window enlargement via interface engineering (e.g. the inclusion of a thin layer of a wide bandgap oxide for barrier tuning) [162]. This subject needs to be further studied.

Fig. 6.13: The difference in the median resistance of the low and high states is $85\times$. With statistical variations, the worst-case array-level memory window becomes $\sim 6\times$ in this study.

6.9 AC electrical characteristics characterization

Single pulse read-destructive and write-back operation can be successfully induced down to a pulse timing of 1 μs for a wafer-level set-up (Fig. 6.14). A further decrease in pulse timing would require larger voltages (which may cause premature failure) or multiple read/write pulses.

Fig. 6.14: Single-pulse destructive read and write-back of ITO/HfO_x/TiN device are achieved down to a pulse timing of 1 μs . (a) shows the positive-read and negative write-back voltage waveforms; (c) shows the negative-read and positive write-back voltage waveforms. Voltage levels shown are the minimum needed to cause a resistance change at a 1 μs pulse timing. In between the read and write voltage pulses, a low-voltage measurement was performed to check the resistance of the device. (b) and (d) show changes in the resistance recorded under alternating read (R) and write (W) pulses.

6.10 Summary

An approach that may lead to a significantly improved CRS voltage window and read margin is presented. The approach is leveraged on the inherent asymmetry in the O-ion exchange process between interfaces involving different reactive metal electrodes to enlarge the difference between the set and reset voltages. The proof-of-concept was successfully demonstrated for the ITO/HfO_x/TiN resistive memory structure, yielding a positive CRS voltage window of 1.6 V and a read margin of 1.1 V. These results represent a significant improvement over the respective window and margin of 0.5 V

and 0.1 V achieved on the TiN/HfO_x/TiN stack and other single devices reported to-date, and address a major challenge of array-level CRS implementation using HfO_x RRAM on both rigid and flexible substrates. The improvement may be attributed to a combination of two effects: 1) a reduced set voltage due to the greater oxygen affinity of ITO; 2) an increased reset voltage due to an opposing Volta potential arising from the larger work function of ITO.

Chapter 7 CONCLUSION & RECOMMENDATION

7.1 Conclusion

A systematic investigation, comprising device level electrical characterizations as well as physical analysis (via TEM, SEM, EDX and XPS), of CRS in HfO_x-based RRAM devices, using fully compatible materials with current mainstream CMOS technology, provides very useful insight into the implementation of a high-density, selector-less RRAM crossbar array for next-generation NVM applications. The key findings achieved in this research paper are summarized as follows:

- A study revealed a key role of the interfacial layer (IL) between the switching oxide and reactive metal electrode in enabling CRS in HfO_x-based RRAM devices. The physical switching mechanism, based on oxygen-ion exchange between ILs and the conductive path in HfO_x, was clarified to have caused the observed CRS in the RRAM device.
- A study on the current conduction mechanism of HfO_x-based RRAM devices revealed that Schottky emission is a dominant conduction mechanism of the HRS in both the bipolar resistive switching and complementary resistive switching modes. A current conduction transition from semiconducting (via the farthest-neighbor trap-assisted tunneling process) to metallic conduction in the LRS was proposed for the first time. A zero temperature-coefficient of LRS resistance was revealed.
- Self-compliance set-switching behavior was observed in the TiN/HfO_x/Pt RRAM device without a series oxide layer. No self-compliance behavior is

observed when the TiN electrode is replaced by Pt or when it is enriched with Ti. Studies show that the TiN/HfO_x interface and the stoichiometry of the TiN electrode both play a determining role. A new mechanism, based on pile-up of oxygen at the metal/oxide interface and its modulation of the interface barrier (increase the Schottky barrier of the interface) as the key requirements for a RRAM device to display the SCSS behavior, was proposed to have caused this behavior. The insights obtained from this study are not only applicable to the TiN/HfO_x interface but should also be applicable to other metal/oxide interfaces. Our study provides important insights into the governing mechanism of SCSS and a pathway towards the implementation of truly selector-less crossbar memory arrays.

- A study on CRS in the TiN/HfO_x/TiN RRAM device revealed an unusual self-reset behavior. Analysis of the current conduction mechanism in devices exhibiting this behavior shows a good agreement with the HRS conduction mechanism in devices displaying a conventional bipolar reset, indicating that the formed filament is simultaneously disrupted after the forming process. We propose that the bulk of the forming voltage would be instantaneously transferred across the sub-stoichiometric TiON interfacial oxide upon filament formation in the HfO_x. The resultant large electric field may then draw oxygen ions from this layer into the filament in the HfO_x, disrupting the filament before the forming process can be interrupted. This hypothesis is supported by the fact that this behavior is suppressed in devices with a thin Al₂O₃ layer inserted in-between the TiN and HfO_x, and is completely eliminated in devices with the TiN cathode replaced by Pt, because of the reduction in “voltage loading” across the

cathode's interfacial oxide during forming transient in devices with the Al_2O_3 interlayer and the elimination of interfacial oxide in devices with the Pt cathode.

- A study on CRS also revealed an unusually large, non-polar reset loop (irrespective of post-forming switching voltage), and failed CRS behavior. We proposed that the IL (key in enabling CRS) breakdown and the metal (Ti) filament formation induce this behavior, which is supported by the significant reduction or complete elimination of the large non-polar reset and CRS failure in devices with a thin Al_2O_3 layer incorporated at the TiN-cathode/ HfO_x or both TiN/ HfO_x interfaces. This is because the higher breakdown field of the thin Al_2O_3 enables it to withstand the forming voltage (upon filament formation in the main oxide) until the forming process is interrupted. With the integrity of the barrier oxide layer ensured, stable CRS could be achieved. The findings reported here provided a possible route for CRS performance optimization via electrode/oxide interface engineering.
- We revealed a new approach to solve another major issue of the narrow read voltage window faced in the CRS in oxide-based RRAM devices. This approach is leveraged on the inherent asymmetry in the O-ion exchange process between interfaces, involving different reactive metal electrodes, to enlarge the difference between the set and reset voltages. We successfully demonstrated an improved positive CRS voltage window of 1.6 V and a read margin of 1.1 V in the ITO/ HfO_x /TiN resistive memory structure, representing a significant improvement over the respective window and margin of 0.5 V and 0.1 V achieved in the TiN/ HfO_x /TiN stack and other single devices reported to date. The improvement may be attributed to the greater tendency for O ions to migrate from the adjacent ruptured filament into the ITO (hence a small set voltage) and

the increased reset voltage due to an opposing Volta potential arising from the larger work function of the ITO. These findings addressed the real challenge of array-level CRS implementation using HfO_x RRAM on both rigid and flexible substrates for solving the sneak-path current problem in the selector-less RRAM crossbar array structure.

7.2 Recommendations

Although RRAM has been extensively studied for several decades, the concept and application of complementary resistive switching for the implementation of the high-density, selector-less RRAM crossbar array is deemed relatively new, and therefore the fundamental understanding of the reliability of the physics of CRS is still lacking. The performance of array-level CRS also needs to be investigated. More research could be done to achieve stable and reliable CRS in the oxide-based RRAM device. Possible future studies are listed as follows:

- Studies have found the crucial key of interfacial layer between the reactive metal electrode and resistive switching oxide in enabling CRS. However, a detailed study on the dependence of CRS reliability on the thickness and composition of the IL is still lacking.
- An improvement of CRS stability, by incorporating an oxide with a high breakdown electrical-field into the RRAM stack, has been demonstrated in this research. Interface-engineering optimization with the aid of physical and electrical characterization is still needed to achieve high-performance CRS.
- CRS offers great promise for the implementation of a high-density selector-less RRAM crossbar array, free of the sneak-path current issue. The achievement of CRS in forming-free RRAM device is very important so that a study on the dependence

of forming voltage on the stoichiometry and thickness of switching oxide is desirable.

- CRS behavior has been successfully observed in the HfO_x -based RRAM device under pulse read-destructive and write-back operation with the pulse timing down to 1 μs for a wafer-level set-up. A further decrease in the pulse timing of CRS is required. The use of larger pulse voltages or multiple read/write pulses can be studied.
- It is necessary to fabricate the high-density, nano-crossbar RRAM array structure to examine the functionality of CRS in a circuit-level system. It is also worthy to explore the CRS in a full-transparent and flexible RRAM device for potential flexible electronic device applications.

LIST OF PUBLICATIONS

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