Modelling of gallium nitride half-bridge converter

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**NANYANG
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UNIVERSITY**

**MODELLING OF GALLIUM NITRIDE HALF-BRIDGE
CONVERTER**

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SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**

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Abstract

Gallium nitride high electron mobility transistors (GaN HEMTs) have been commonly cited to significantly improve the efficiency and power density of power electronic converters like battery chargers, laptop adapters and motor drives. The potential for size reduction was proven during the Google little box challenge where GaN HEMTs were used for the construction of the winner's converter. The size of the magnetics components are significantly reduced due to the high switching frequencies. This has enabled the use of more advanced hardware design techniques like integration of magnetics and packaging. However, as they are relatively new to the field of power electronics, their characteristics are not well understood by many power electronics engineers. Hence, many developed simulation models for GaN HEMTs do not accurately reflect the device behaviour when they are used in power electronic applications.

In present thesis work, the majority of models for GaN HEMTs are proposed for radio frequency applications. Relatively few models have been proposed for power electronic applications and the few that have been proposed use simplistic equations that do not accurately capture the device's behaviour. In this thesis, the unique device physics associated with the GaN HEMT is reviewed and compared with that of other devices like the silicon MOSFET. Unlike other power transistors, the i - v characteristic of GaN HEMTs is significantly augmented by the piezoelectric effect. Also, unlike the body diode of silicon MOSFETs, the body diode of GaN HEMTs is affected by the applied gate bias. Hence, in this work, a device model is proposed with an i - v characteristic that is approximated using the equation of a charge sheet in a GaN HEMT under the effect of piezoelectric polarisation. An i - v characteristic equation for the body diode that reflects the effect of different gate biases is also proposed for the model. In order to capture the dynamic behaviour of the device, the capacitances have been modelled behaviourally using sigmoid functions.

It is also well-known that parasitic inductances in a power electronic circuit hinder the performance of fast-switching devices. Many authors propose ways of minimising the parasitic inductances without regards to the implications this would have on other aspects of converter design such as the thermal resistance of the thermal path from the device's junction to the ambient air. Hence, the implications of the trade-off in between a low parasitic inductance design and a low thermal-resistance is examined with respect to the volume and efficiency of a buck converter.

This is done by examining the performance of GaN converters with different printed circuit board (PCB) layouts.

As GaN switches are known to switch very quickly, it is very difficult to accurately observe their switching behaviour under practical conditions due to limitations in the bandwidth of current equipment. Consequently, this makes deducing the actual switching loss of a GaN switch difficult. Hence, in order to determine what method is useful for extracting the switching loss of GaN HEMTs, a review of loss measurement methods is conducted and two commonly used electrical methods are compared against each other in terms of accuracy.

Lastly, two boost converters, one developed using silicon MOSFETs and the other developed using GaN HEMTs, are both constructed and tested for use as a bidirectional battery charger in a home energy storage system. The two are compared against each other in terms of volume, cost and efficiency to assess the benefit of GaN HEMTs.

In the concluding chapter, findings are summarised and potential future work is proposed.

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List of symbols

Symbol	Description	Units
A	Cross-sectional area of p-n junction	m^2
a_1	Fitting parameter	F
a_2	Fitting parameter	F
A_c	Effective area due to convection	m^2
A_{jb}	Cross-section of thermal path due to conduction	m^2
A_{rad}	Effective area due to radiation	m^2
b_1	Fitting parameter	V^{-1}
b_2	Fitting parameter	V^{-1}
B_{ac}	Magnetic flux density through core	T
BW	Bandwidth	Hz
c_1	Fitting parameter	V
C_1	Rated capacitance	F
c_2	Fitting parameter	V
C_{ds}	Drain-source capacitance	F
C_{gs}	Gate-source capacitance	F
C_i	Capacitance per unit area	F/m^2
C_{oss}	Output capacitance	F
d	Barrier layer depth	m
d_1	Fitting parameter	F
d_2	Fitting parameter	F
d_{AlGaIn}	Thickness of AlGaIn layer	m
d_d	Depletion depth of doped portion of semiconductor	m
d_{GaN}	Thickness of GaN layer	m
d_i	Depletion depth of intrinsic portion of semiconductor	m
E	Electric field across depletion region	VC^{-1}
E_1	Sum of $E_{\text{on-T}}$, $E_{\text{off-T}}$, $E_{\text{on-bd}}$ and $E_{\text{on-bd}}$ for first part of opposition method	J
E_2	Sum of $E_{\text{off-T}}$ and $E_{\text{on-bd}}$ for second part of opposition method	J
E_{2h}	Sum of $E_{\text{off-T}}$ and $E_{\text{on-bd}}$ corresponding to maximum value of inductor ripple	J
E_3	Sum of $E_{\text{on-T}}$ and $E_{\text{off-bd}}$ for opposition method	J
E_{3l}	Sum of $E_{\text{on-T}}$ and $E_{\text{off-bd}}$ corresponding to minimum value of inductor ripple	J
E_c	Critical breakdown electric field	VC^{-1}
E_c	Conduction band energy level	eV
E_f	Fermi level of semiconductor	eV
E_{fm}	Fermi level of metal	eV
E_m	Magnetic energy	J
E_{max}	Magnitude of maximum electric field across depletion region	VC^{-1}
$E_{\text{off-bd}}$	Turn-off energy of body diode	J
$E_{\text{off-T}}$	Turn-off energy of power transistor	J
$E_{\text{on-bd}}$	Turn-on energy of body diode	J
$E_{\text{on-T}}$	Turn-on energy of power transistor	J
ESL_1	Equivalent series inductance of film capacitor	H
ESL_2	Equivalent series inductance of electrolytic capacitor	H
ESR_1	Equivalent series resistance of film capacitor	Ω
ESR_2	Equivalent series resistance of electrolytic capacitor	Ω
E_v	Valence band energy level	eV
f	Frequency of applied magnetic field in core	Hz
f_{sw}	Switching frequency	Hz
g_m	Transconductance	Ω^{-1}
h	Heat transfer coefficient	$\text{W}/(\text{K}\text{m}^2)$
I_{ds}	Drain-source current	A
I_g	Fitting parameter	A
I_{gs}	Gate-source leakage current	A
i_L	Current through a generic inductance	A
I_{lrms}	RMS current through inductor	A
I_{osc}	Oscillation current	A
I_{sd}	Reverse conduction current	A
J_n	Electron current density	C/m^2

K_1	Temperature dependent constant	A
K_2	Temperature dependent constant	V ⁻¹
K_3	Material and geometrically dependent constant	V
K_4	Temperature dependent constant	A
K_5	Fitting parameter	
k_{gs}	Fitting parameter	V ⁻¹
L	Generic inductance	H
L	Channel length	m
l'	Generic closed loop	
l_c	Mean current path	
L_{com}	Total parasitic inductance of commutation loop	H
L_{d_l}	Drain inductance of lower switch	H
L_{d_u}	Drain inductance of upper switch	H
L_{gate}	Total parasitic inductance of gate driver loop	H
l_{jb}	Length of thermal path due to conduction	m
L_{par}	Parasitic inductance	H
l_{PCB}	Length of PCB trace	m
l_s	Path enclosing S_{ex}	
L_{s_l}	Source inductance lower switch	H
L_{s_u}	Source inductance of upper switch	H
L_{sh}	Shunt parasitic inductance	H
L_{trace}	Parasitic inductance of PCB track	H
L_{trace}	Trace Inductance	H
n	Negative charge carrier concentration	m ⁻³
N_a	Acceptor carrier concentration	m ⁻³
N_d	Donor carrier concentration	m ⁻³
N_d	Dopant concentration	m ⁻³
n_e	Effective negative charge carrier concentration	m ⁻³
n_s	Charge sheet concentration	m ⁻²
n_{s0}	Sheet carrier concentration under equilibrium conditions	m ⁻²
p	Positive charge carrier concentration	m ⁻³
p_e	Effective positive charge carrier concentration	m ⁻³
P_i	Input power	W
P_l	Power loss	W
P_o	Output power	W
P_{sw}	Switching loss	W
P_t	Total power loss of opposition method	W
P_v	Core loss per unit volume	W/m ³
q	Electron charge	C
Q_{gd}	Miller charge	C
Q_{leak}	Leakage charge	C
Q_m	Charge entering gate during miller plateau	C
R_{hs_conv}	Thermal resistance due to convection	K/W
R_{hs_rad}	Thermal resistance due to radiation	K/W
R_{jb}	Thermal resistance due to conduction	K/W
R_n	Resistance at n th harmonic of current	Ω
r_{on}	On-resistance of p-n junction	Ω
$r_{on,sp}$	Specific on-resistance of p-n junction	Ωm ²
R_{trace}	Trace resistance	Ω
S	Open surface	
S_{ex}	Open loop portion external to conductor	
S_{in}	Open surface portion within conductor	
t	Time	S
T	Temperature	K
t_{PCB}	Thickness of PCB trace	m
t_r	Generic rise time	s
tr_{probe}	Probe rise time	s
tr_{scope}	Scope rise time	s
t_{sys}	System rise time	s
V	Reverse-biased voltage across depletion region	V

V_{Br}	Breakdown voltage of device	V
V_c	Volume of conductor	m ³
V_c	Channel voltage	V
V_{driver}	Gate driver IC voltage	V
V_{ds}	Drain-source voltage	V
V_{gd}	Gate-drain voltage	V
V_{gd1}	Fitting parameter	V
V_{gs}	Gate-source voltage	V
V_{gs1}	Fitting parameter	V
v_L	Voltage across a generic inductance	V
V_{osc}	Oscillation voltage	V
v_{over}	Voltage overshoot	V
V_p	Built-in potential	V
V_{sd}	Source-drain voltage	V
V_{sp}	Volume of space occupied by magnetic field	m ³
V_{th}	Threshold voltage	V
W	Width of depletion region	m
W_N	Displacement of depletion region into the n ⁺ region	m
w_{PCB}	Width of PCB trace	m
x	Displacement	m
X_c	Reactance of capacitor	Ω
Z	Channel width	m
α_I	Fitting parameter	V ⁻¹
ϵ_0	Permittivity of free space	m ⁻³ kg ⁻¹ s ⁴ A ²
ϵ_r	Relative permeability	
η	Efficiency	
μ	Carrier mobility	cm ² /(Vs)
μ_0	Permeability of free space	H/m
μ_n	Electron mobility	cm ² /(Vs)
μ_p	Hole mobility	cm ² /(Vs)
μ_r	Relative permeability	
ρ	Charge per unit volume	C/m ³
σ	Conductivity	Ω ⁻¹ m ⁻¹
$\vec{A}$	Vector magnetic potential	Wb/m
$\vec{J}$	Current density	A/m ²
$\vec{H}$	Magnetic field strength	A/m
$\vec{B}$	Magnetic flux density	T
θ	Angle in between current density and vector magnetic potential	rad
$\phi_{m,ex}$	Flux passing through S _{ex}	
ϕ_{bn}	Schottky barrier voltage	V
ϵ_s	Permittivity of semiconductor	m ⁻³ kg ⁻¹ s ⁴ A ²
ϕ_b^{eff}	Effective schottky barrier potential	V
ΔE_C	Discontinuity in the conduction band	eV
ω_{res}	Angular frequency for resonance	rad s ⁻¹
σ_t	Thermal conductivity	W/(Km)
ϵ_{hs}	Emissivity of heatsink	
σ_b	Stefan Boltzmann constant	W/(K ² m ⁴)

CHAPTER 1 : INTRODUCTION

1.1 : Motivation

Power electronics occupies a category of circuits used for the processing and control of electric power by supplying voltages and currents in a form that is optimal for user loads [1]. These circuits, also known as converters, are required to process electric power in a wide variety of applications like transport, renewable energy and data centres. In many of these applications, the power electronics is expected to meet a set of requirements imposed on size, efficiency, cost, reliability and electromagnetic compatibility. The power transistor, which is a key component in power electronics, plays a critical part in meeting these requirements.

In the past decade or so, power transistors realised from wide bandgap semiconductors like gallium nitride (GaN) and silicon carbide (SiC) have been gaining much popularity as they are often cited to be able to improve efficiency [2, 3, 4] and power density [5, 6, 7, 8, 9]. It is expected that GaN transistors will eventually find their niche in low-power, low-voltage applications whilst SiC transistors will find their niche in medium-power, medium-voltage applications.

Although GaN power transistors have been used for radio frequency (RF) applications for about a decade [10, 11, 12, 13], they are a relatively new addition to the field of power electronics and are hence not well understood by many power electronics engineers. Power semiconductor textbooks published as recently as 2011 [14] and 2008 [15] do not dedicate chapters to explain the device physics of GaN switches. It is hence difficult for new adopters of this technology to utilise it to its full potential. Suitable device models for GaN switches could hence prove useful for power electronics engineers when they need to predict the performance of converters realised using GaN switches.

The need for device models has also been driven by another trend. In the past decade or so, design of converters through multi-objective optimisation techniques [16, 17, 18, 19] which use genetic algorithms and detailed component models has been gaining popularity. An accurate and fast model for GaN transistors could help speed up development time and is expected to be adopted by proponents of multi-objective optimisation.

In order to verify the correctness of these models, suitable measurement techniques must be developed. One of the key challenges of working with GaN devices is their high di/dt s [20, 21] which can easily lead to overvoltages and destruction of the device. The high di/dt s and dv/dt s also impose high bandwidth requirements on both the oscilloscope and probes needed to measure the switching waveforms of the GaN HEMT [22]. This makes verification of device models under practical operating conditions, when the device is expected to switch fast, very difficult and costly. Rough estimates for the voltage rating and bandwidth of a voltage probe needed to measure the fast transients of GaN switches are above 100V and about 1GHz respectively. To date, no such commercial probe exists.

GaN transistors have seen usage in various low power applications ranging from a few watts to a few kilowatts like point-of-load converters [23, 24], LLC converters for data centres [6] and motor drives [3, 4]. High power densities [6, 23] and efficiencies [3] as a result of utilisation of GaN transistors have been consistently reported.

The circuit-level benefits of GaN transistors are a point of interest for power electronic engineers as these switches are significantly more expensive than their silicon counterparts but offer efficiency improvements as well as volume reduction and cost savings on the cooling system and passive components. The high switching frequencies of GaN converters allow magnetic components to be shrunk to such an extent that integration is possible [5, 25].

1.2: Objectives

The objectives of this work are as follows:

1) Propose a model for the GaN power transistor

Since GaN transistors are relatively new to the field of power electronics, power device models for GaN transistors often do not fully reflect its device physics or its implications on the performance of the converter. At present, most authors and manufacturers rely on “black box” models [26, 27]. Physics-based models are often too complicated for practical use and involve device parameters that are not easily assessable to the power electronics engineer. Hence, one of the objectives of this work is to propose an accurate model that has basis in device physics while being simple enough for power electronics engineers to use. In Chapter 3, the model is presented along with its associated parameter extraction technique.

2) Find and investigate suitable verification techniques

Due to the fast transients of GaN switches under practical conditions, conventional oscillographic techniques are not as suitable for finding the switching losses. Therefore, alternative switch loss measurement techniques must be investigated in order to verify the switching losses predicted by the models under practical conditions. In Chapter 5, two such techniques are presented and compared in detail.

3) Investigate the circuit-level suitability of GaN transistors

GaN transistors are more expensive than their silicon counterparts. Hence, care must be exercised when evaluating when GaN transistors should be used over silicon ones so that the overall circuit design is better. In Chapter 6, the circuit-level benefit of GaN transistors is investigated using a bidirectional boost converter that acts as the first stage of a modular home energy storage system.

Due to their fast switching speeds, it is often cited that the parasitic inductances of circuits involving GaN transistors must be kept low. However, keeping these parasitic inductances low can come at the expense of reduced thermal dissipation capability. Hence, Chapter 4 aims to investigate if it is worthwhile to slightly increase the parasitic inductance in return for better thermal dissipation capability. The investigation is done using half-bridges with slight variations in their printed circuit board (PCB) layout. The half-bridges are simulated as a 48V to 12V buck converter which are the typical input and output voltages of brick converters that are connected in between a 48V lead-acid battery and electronics that run on a 12V rail.

1.3: Major contributions of the thesis

The major contributions of this thesis are as follows:

1) A novel power transistor model for GaN transistors is proposed and investigated.

This model approximates the device physics used for deriving the i-v characteristic of GaN transistors and makes use of behavioural models for the device capacitances. The accuracy of this model is investigated in Chapter 5 for a variety of fast and slow switching conditions.

2) A detailed comparison between two techniques for measuring the switching loss of GaN transistors under practical conditions is performed.

Recommendations are made for which technique to use under those conditions. Sources of error are also identified.

3) The efficiency, cost and volume benefits of GaN transistors over silicon transistors are investigated and quantified for the case of a bidirectional boost converter.

In Chapter 6, a silicon switch was selected and used as part of a half-bridge to benchmark against another half-bridge realised from GaN transistors. The resulting volume, efficiency and cost of the converters are presented.

1.4: Outline

In Chapter 1, the motivation, objectives, major contributions and outline are presented.

In Chapter 2, typical applications of GaN transistors are listed and the concept of the half-bridge as a basic building block of various topologies is introduced. A literature review of power device technology is presented and the underlying physical factors that give rise to GaN's superiority over silicon switches is presented. This is followed by a review of transistor modelling techniques, parasitic inductance extraction techniques and verification techniques for power transistor models.

In Chapter 3, the power transistor model is presented along with the associated parameter extraction technique.

In Chapter 4, the trade-off in between a low parasitic inductance design and a low thermal resistance design is investigated.

In Chapter 5, verification techniques for extraction of switching loss predicted by the power transistor model is investigated.

In Chapter 6, a comparison in between GaN and silicon transistors for an example application is made.

In Chapter 7, the conclusions and future work are presented.

CHAPTER 2 : LITERATURE REVIEW

2.1: Chapter overview

In this chapter, the applications of GaN power transistors are first reviewed. This is followed by a review of power semiconductor devices and parasitic inductances of power converters. In addition, the concept of the half-bridge converter as a building block is discussed to emphasise the importance of having accurate half bridge models. It is also important that appropriate measurement techniques be employed for verification of the model. Hence, a literature review of verification and modelling techniques is also conducted.

2.2: Applications of GaN Power Transistors

GaN power transistors are suited for applications with a power range within about 10W to 10kW. Some of these applications are listed in Table 2.1. The primary benefits of GaN in these applications are a reduction in size and losses.

Table 2.1: Variety of applications of GaN power transistors

Power range	10W to 1kW	1kW to 10kW
Applications	<ul style="list-style-type: none">- Point-of-load converters (POL) [5, 23, 24]- Micro-inverters [28, 29, 30]- Brick converters [31]- Class D amplifiers [32, 33]- Gate drivers [34]	<ul style="list-style-type: none">- Data centres [6]- Motor drives [4, 3, 35]- Battery chargers [36, 37]- PV inverters [38, 39]

2.3: The Half-Bridge converter as a Building Block

The switching behaviour of power transistors is affected by the parasitic inductance of the current paths in the converter. It is therefore important to choose the topology in which the switches will be modelled so that the parasitic inductance can be accounted for. For this work, the half-bridge was chosen since it was the simplest of the topologies and it can be considered as a building block for other topologies. In Figure 2.1(a), the half-bridge is depicted using two ideal switches, S1 and S1!, which work in complement with each other to step down voltage from V1 to V2. The half-bridge is also depicted as part of various converters in Figure 2.1(b) to (d) in order to show that it can be seen as a building block for various other topologies.

Figure 2.1: Examples of present topologies

It should be noted that not all topologies can be physically realised by using the half-bridge as a building block. Examples of this include neutral-point clamped (NPC) converters and flyback converters. Due to differences in circuit topology, the current paths in these converters differ from that in a typical half-bridge. In order to better illustrate this, the current path of the commutation loop of a typical half-bridge is depicted beside one of the possible current paths of an NPC leg as seen in Figure 2.2.

Figure 2.2: Comparison of current paths in half-bridge leg and NPC leg

The half-bridge model derived in this work is hence useful only for topologies which can be realised using several half-bridges as building blocks. However, the switch model itself can be used for simulating other topologies provided if the parasitics of the current paths in those topologies are accounted for.

2.4: Power Device Review

Power semiconductor devices are very important parts of a converter. Their performance impacts the size of the cooling system required as well as the size of the passive components that the converter requires. A power device's performance is a function of both the material that is used to build it as well as its physical structure which is also known as its device geometry. In the case of GaN transistors, a unique combination of both material and device geometry has led to good performance. This unique combination also causes the physics of the GaN transistor to be significantly different from other types of transistors. In the next sections, a review of materials and the device geometry of GaN transistors is conducted to examine why GaN transistors are so unique amongst other power devices.

2.4.1: Materials Review

Many semiconductors are available for designing power transistors. Power transistors fashioned from these materials are expected to exhibit desired traits like low power losses and the ability to withstand high operating temperature. The ideal semiconductor for this application should therefore possess traits like high carrier mobility, wide bandgap, high thermal conductivity and low cost. However, in practice, it is difficult to find a material that embodies all these traits. It is therefore necessary to define a set of figures of merit (FOMs) to assess the suitability of these materials. These FOMs must reflect how the traits of the material are related to the desired traits of the power transistor.

Not all materials can be used to make any type of power device. In the case of GaN, which is a direct bandgap semiconductor, it has been reported [41] that the minimum carrier lifetime in GaN is very short. This makes it a very poor material for realising bipolar devices. In addition to this, hole mobility in p-type GaN is known to be very poor at typically around $10 \text{ cm}^2/\text{Vs}$. Hence, it is not worthwhile to create a bipolar GaN device. Therefore, if one were to compare GaN to another material for making power devices, the implicit assumption is that the comparison is being done for the case of a unipolar device. Hence, the FOMs involved for such a comparison will be for unipolar devices.

The chosen FOMs in this work are Huang's material figure of merit (HMFOM) [42] and Baliga's figure of merit (BFOM). HMFOM is an indicator of how much combined switching and conduction loss that a unipolar device made using that material will exhibit. A higher number indicates a better material. As HMFOM is

reflective of the combined switching and conduction loss, it is more suitable for assessing materials which will be used to make transistors for hard-switched converters where both loss components exist. BFOM is an indication of how much on-resistance that a unipolar device made using that material will exhibit. A higher number indicates that the material has a lower specific on-resistance. BFOM is more suitable for assessing materials which will be used to make transistors for soft-switched converters where the conduction loss of the switch is expected to predominate more. HDFOM is defined in

$$\text{HMFOM} = E_c \sqrt{\mu} \quad (2.1)$$

where E_c represents the critical breakdown electric field, μ represents the carrier mobility.

BFOM is defined in

$$\text{BFOM} = \varepsilon_0 \varepsilon_r \mu E_c^3 \quad (2.2)$$

where ε_0 and ε_r represent the permittivity of free space and relative permittivity of the material respectively.

As seen in (2.2), E_c is a very important factor when it comes to the on-resistance due to the fact that BFOM is proportional to its cube. Doubling the value of E_c improves the on-resistance by a factor of eight. E_c is known to increase with bandgap of the material. This is the reason why wide bandgap semiconductors are known to have a higher performance.

Using these FOMs, various materials can be evaluated as seen in Table 2.2. It should be noted that for the GaN, the highest reported electron mobility is 2000 cm²/Vs [43] which is the value used for the comparison. It should also be noted that such high mobility has only been reported in the high electron mobility transistor which will be covered in the next section. Other values for the electron mobility, critical field and relative permittivity have been taken from various sources [42, 44].

Table 2.2: Material Comparison

Material	Electron mobility / cm^2/Vs	Critical field / kV/cm	Relative permittivity	BFOM (normalised against silicon)	HMFOM (normalised against silicon)
Silicon	1400	300	11.7	1.0	1.0
Silicon carbide (4H-SiC)	700	3180	9.7	493.7	7.5
Silicon carbide (6H-SiC)	330	2400	9.66	99.6	3.9
Gallium nitride	2000	3000	9	1098.9	12.0
Gallium arsenide	8500	400	13.1	16.1	3.3
Gallium phosphate	250	1000	11.1	6.3	1.4
Gallium oxide (Beta type)	300	8000	10	3473.1	12.3
Germanium	3900	100	16	0.1	0.6
Diamond	2200	5700	5.7	5251.0	23.8

It can be seen from Table 2.2 that a material may not be better than another just because it possesses one desirable characteristic. For instance, gallium arsenide has the highest electron mobility but in terms of both HMFOM and BFOM, it loses out to 6H-SiC which has a significantly lower electron mobility. Likewise, a high critical field by itself is not a deciding factor for a good material. For instance, silicon 4H-SiC has a higher critical field than gallium nitride but still loses out in terms of HMFOM and BFOM.

Based on Table 2.2, diamond appears to be the best semiconductor for constructing a unipolar device. To-date however, the cost of such devices is high and the manufacture of diamond devices is difficult. Hence, diamond devices are not commercially available and are typically the subject of academic literature [45, 46, 47, 48, 49].

Based on HMFOM and BFOM, the second best candidate for realising a unipolar device is gallium oxide. This material is a new wide bandgap semiconductor and its

potential has been reported in a few pieces of literature [44, 50]. However, as it is still very new, it has yet to be widely adopted.

The third best candidate based on HMFOM and BFOM is gallium nitride. It is seen that this material possesses both a high critical field due to its wide bandgap as well as a high mobility. Both of these factors combined yield a superior material compared with silicon and silicon carbide. Unlike diamond, GaN transistors are more easily created and unlike gallium oxide, GaN transistors have had more time to mature.

Through this material comparison, it can be seen that from a technological perspective, gallium nitride is a good material because it simultaneously possesses high mobility and a wide bandgap. It should be noted however, that the high electron mobility of GaN is only possible in monocrystalline substrates that are highly pure. So in order to create a good power transistor from GaN, the material must be paired with a suitable device geometry – one in which the layer where the current channel is formed consists of a very pure monocrystalline GaN material.

2.4.2: Power Device Geometry

In this section, the various device geometries are reviewed to check which geometries can be suitably used with the GaN material. The chosen device geometry must also allow for high electron mobility which implies that the current channel must be formed in a region that is ideally monocrystalline.

The first device geometry to be reviewed is that of the p-i-n diode. Its symbol and device geometry are presented in Figure 2.3. The p-i-n diode is a bipolar device. Its device geometry consists of a lightly doped drift region engineered in between two highly doped regions as depicted in Figure 2.3(b). When the device blocks, this drift region is depleted and serves as a dielectric for blocking reverse voltages.

It can be deduced upon examination that the p-i-n device geometry is not a suitable candidate for realising a GaN device. Since it is a bipolar device, both holes and electrons are involved in the conduction of current. GaN does not possess a high hole mobility and thus is unsuitable for use with this geometry.

Another reason this geometry is unsuitable is the presence of doped regions in the path of the device current. Due to high levels of doping in two of the regions, the

crystal structure of these regions is no longer highly monocrystalline. Hence, the electron mobility within these regions is no longer high.

(a) Diode symbol

(a) Device geometry of p-i-n diode

Figure 2.3: p-i-n diode symbol and device geometry

Another type of diode is the Schottky diode and its device geometry is presented in Figure 2.4. Unlike the p-i-n diode, the Schottky diode is a unipolar device. As seen in Figure 2.4, the difference in between a p-i-n diode structure and a Schottky diode is that there is no highly doped p-region. The metal contact is instead directly connected to the drift region. As the device is unipolar, it is slightly more suitable than the p-i-n diode in terms of its compatibility with the GaN material. However, the highly doped n+ region still causes the electron mobility of GaN to drop. Hence it is not a highly suitable geometry for realising a GaN device.

Figure 2.4: Schottky diode device geometry

The third device geometry to be reviewed is that of the metal oxide semiconductor field effect transistor (MOSFET). Its device geometry and symbol are presented in Figure 2.5. When the device is on, a current channel is formed in the channel region under the gate. Current flows from the drain contact through the n+ and n- regions and then through the channel region which is p-doped and eventually to the source contact via the n+ region. When the device is off and in the blocking state, the n- region is depleted and serves as a dielectric just like in the case of the p-i-n diode.

It is also seen from Figure 2.5(b) that there exists a region of the MOSFET that resembles the structure of a p-i-n diode. This region is known as the body diode and is typically unoptimised with poor reverse recovery characteristics. When the channel is in the cutoff regime, and a reverse voltage is applied across the drain and source terminals, the body diode conducts. In a converter, a dead-time interval is introduced in between complementary switches and during this dead-time, the body diode conducts. The losses resulting from body diode operation is significant and is the reason why MOSFETs are sometimes connected in parallel with a more optimised diode with better characteristics.

It can again be seen that the current flows through several highly doped regions. Hence the mobility of charge carriers is expected to degrade in these regions, making this device geometry unsuitable for use with the GaN material. As the body diode is actually a p-i-n diode, use of GaN to realise a MOSFET will result in a device with a very poor body diode behaviour and lead to greater device losses. Hence, the MOSFET geometry is not suitable for realising a GaN device.

Figure 2.5: MOSFET symbol and device geometry

The next device geometry to be considered is that of the bipolar junction transistor (BJT). Its symbol and structure are presented in Figure 2.6. The BJT is a bipolar device. In its on-state, a continuous base current is supplied to keep the device on and the main load current flows from collector to emitter. In order for the BJT to work, the carrier lifetime must be sufficiently large enough so that the majority of the charge carriers can make it through the base region. Only when this condition is met can current amplification be achieved. As the carrier lifetime of a GaN device is short, a GaN-based BJT will not have enough current amplification to be usable as a power device. Also, since the BJT is bipolar and the load current travels through doped regions, this geometry is unsuitable for realising GaN transistors.

Figure 2.6: BJT symbol and device geometry

The next device geometry to be considered is that of the insulated gate bipolar transistor (IGBT). Its symbol and structure are presented in Figure 2.7. As seen by Figure 2.7(b), the device structure is very similar to that of a MOSFET except that the highly doped n+ region at the drain end has been replaced by a p region. The p-n-p region forms a pnp transistor with the p region near the collector of the IGBT acting as the emitter and the p and the n- region acting as the base. When a current channel is formed under the gate, the base-emitter junction of the pnp transistor is forward biased and the collector-base junction of the pnp transistor is reversed. The collector-base junction eventually becomes forward biased once the device fully turns on.

Similar to the case of the BJT, the device geometry is not suitable for realising GaN transistors because the device is bipolar, the carrier lifetime of GaN is small and the regions that the load current travels through are doped and hence reduces carrier mobility.

Figure 2.7: IGBT symbol and device geometry

The next device geometry to be considered is that of the thyristor. The device geometry and symbol are presented in Figure 2.8. In order to turn the device on, a gate current is applied. Once the gate current rises above the latching current, the gate signal can be removed and the device is in the on-state. Many variations of the

thyristor exist such as the gate turn-off thyristor (GTO) or the MOS-controlled thyristor (MCT) but they operate on similar principles. Just like in the case of the BJT, the device is bipolar and the load current flows through doped regions where the electron mobility of GaN transistors is significantly impaired. Hence this device geometry is not suitable for realising GaN transistors.

(a) Thyristor symbol

(b) Device geometry of thyristor

Figure 2.8: Thyristor symbol and device geometry

Of all known device geometries, the only device whereby the conducting current travels through a pure monocrystalline layer is the high electron mobility transistor (HEMT). In other power devices, the current flows through regions that have already been doped. Hence the structure of those regions are no longer monocrystalline and the impurities cause scattering which reduces the mobility of the charge carriers.

(a) HEMT symbol

(b) Device geometry of HEMT

Figure 2.9: HEMT device symbol and device geometry

The HEMT is a very recent device geometry in the field of power electronics. Originally, it was a device geometry employed for RF applications. As seen by the device geometry in Figure 2.9(c), the HEMT is a lateral device unlike vertically diffused MOSFETs (VDMOS) or thyristors. Current flows along a 2-D surface instead through the body of the device. Hence, the current-carrying capability of a typical HEMT is quite low. In GaN HEMTs however, piezoelectric polarisation at the heterojunction increases the carrier concentration of the charge sheet and as a result, the current-carrying capability is significantly increased to a point that is comparable to silicon power MOSFETs. This piezoelectric polarization can only occur if the crystal structure of both the channel and barrier layer are closely matched with very similar lattice constants. In addition to this requirement, the barrier layer must possess a bandgap that is significantly wider than GaN so that carrier confinement can be ensured. For GaN HEMTs, the channel layer consists of GaN of a wurzite crystal structure with a bandgap of 3.4 eV. The barrier layer consists of Al_mGa_{1-m}N which is a mixture of GaN and aluminium nitride. This material possesses a bandgap in between 3.4 eV to 6.2 eV depending on the mole fraction, m . In Figure 2.10, a plot of bandgap of different materials against the lattice parameter is presented to better illustrate the requirements on the lattice parameter as well as the bandgap of the material used for the barrier layer. The red line represents the bandgap and lattice parameters of Al_mGa_{1-m}N for different mole fractions.

Figure 2.10: Plot of bandgap of various materials against lattice parameter [51]

Since this unique combination of wide bandgap, high carrier mobility and high current-carrying capability only occurs with this combination of structure and materials, authors [52, 53] typically do not vary the structure of the HEMT much. In Figure 2.11, the structure of a GaN gate injection transistor (GIT) and a GaN Schottky diode are presented. It can be seen that the structures are very similar to that depicted in Figure 2.9 despite the differences in device operation.

(a) GaN GIT [52]

(b) GaN Schottky diode [53]

Figure 2.11: Structure of GaN GIT and GaN Schottky diode

As the piezoelectric effect is unique to the GaN HEMT and alters the concentration of the charge sheet, it is expected that the i-v characteristics of the GaN HEMT will be significantly different from that of a typical HEMT. This has implications on how the device is modelled which are discussed in more detail in Chapter 3.

The switching speed of GaN HEMTs are well-known to be very fast and can reach speeds of as high as 400V in 1.4ns [54]. The switching frequency of GaN HEMTs can easily approach 1MHz under the right circumstances [55].

2.4.3: Power device operating ranges for voltage, current and switching frequency

In this section, the underlying reason for the trade-off in between voltage, current and switching frequency is reviewed to highlight why GaN HEMTs typically outperform silicon MOSFETs.

There is a fundamental trade-off in between the voltage rating, current rating and switching frequency of a power device. All of these device properties are influenced by the size of the drift region of the device. In general, a power device can be optimised for two of this quantities at the expense of the third. It is important to have a general sense of what ranges of voltage rating, current rating and switching frequency that a type of device can be operated at so that GaN can be benchmarked fairly against the right kinds of devices and proposed for the right applications. In this section, the impact of the size of drift region on the fundamental trade-off is discussed using a basic p-n junction structure illustrated in Figure 2.12.

The drift region is a lightly doped region in power devices. In Figure 2.12, the drift region is the n^- doped region. When it is depleted, it forms a dielectric which allows the power device to block when it is in the off-state. The voltage rating of the device increases with the thickness of this region. When the device is in the conducting state, charges are stored in this region so that current may flow. However, because this region is lightly doped, it is in the interest of the designer to not incorporate a drift region that is too thick so that the on-resistance of the device is not too high.

The relationship between electric field and reverse-biased voltage across the depletion region is given by

$$E = -\frac{dV}{dx} \quad (2.3)$$

where E , V and x are the electric field, reverse-biased voltage and displacement respectively.

Reverse-biased voltage can be further expressed as

$$V = \frac{1}{2} E_{max} W \quad (2.4)$$

where E_{max} and W are the magnitude of the maximum electric field across the depletion region and the width of the depletion region.

Figure 2.12: pn junction with plot of electric field distribution

In optimised devices, the doping level of the lightly doped region is adjusted such that when it is totally depleted, E_{max} is approximately equal to the critical field, E_c . Assuming doping level of the p region is very high compared with the n⁻ region, the width of the part of the depletion region in the p-doped region can be approximated as zero.

The relationship between breakdown voltage and critical field can be derived by substituting terms in (2.4). to yield

$$V_{Br} = \frac{1}{2} E_c W_N \quad (2.5)$$

where V_{Br} is the breakdown voltage and W_N is the displacement of the depletion region into the n^- region. W_N is the required width of the depletion region to block the rated voltage. The part of the p-n junction corresponding to W_N is also called the drift region.

(2.5) can also be rewritten as

$$W_N = 2 \frac{V_{Br}}{E_c} \quad (2.6)$$

At this point, Poisson's equation is required in order to establish a link in between breakdown voltage and specific on resistance. Poisson's equation is given by

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon_0\epsilon_r} \quad (2.7)$$

where ρ represents charge per unit volume.

The charge per unit volume is given by

$$\rho = q(p - n + N_d - N_a) \quad (2.8)$$

where q , p , n , N_a and N_d represent electron charge, intrinsic p-type carrier concentration, intrinsic n-type carrier concentration, acceptor and donor carrier concentration respectively.

By substituting (2.8) and (2.3) into (2.7), a generic relationship in between the rate of change of electric field with respect to displacement and the various carrier concentrations may be derived as shown

$$-\frac{dE}{dx} = -\frac{q(p - n + N_d - N_a)}{\epsilon_0\epsilon_r} \quad (2.9)$$

In the n^- region, p , n and N_a are negligibly small. As electric field is expected to vary linearly in this region, (2.9) can be rewritten as shown

$$\frac{E_c}{W_N} = \frac{qN_d}{\epsilon_0 \epsilon_r} \quad (2.10)$$

(2.10) may be further rearranged to yield

$$qN_d = \frac{\epsilon_0 \epsilon_r E_c}{W_N} \quad (2.11)$$

Next, the conductivity of the n^- region is considered as shown in

$$\sigma = q(\mu_n n_e(x) + \mu_p p_e(x)) \quad (2.12)$$

where σ , μ_n , μ_p , n_e and p_e represent conductivity, electron mobility, hole mobility, effective electron concentration and effective hole concentration respectively.

In unipolar devices like schottky diodes or MOSFETs, the current flowing through the drift region predominantly consists of only one type of charge carrier. However in bipolar devices like p-i-n diodes or IGBTs, high injection of minority carriers into the drift region significantly increases the conductivity. This phenomenon is known as conductivity modulation and is the reason why bipolar devices can typically carry more current than unipolar devices of the same active area.

When the p-n junction is on, the depletion region shrinks and allows for carriers to cross. The on resistance across the p-n junction corresponding to width W , formerly occupied by the depletion region, can be given by

$$r_{on} = \frac{W}{\sigma A} \quad (2.13)$$

where r_{on} and A are the on-resistance and the cross-sectional area of the p-n junction respectively. Once again, due to the high doping of the p region relative to the n^- region, it can be assumed that $W \approx W_N$. In other words, most of the resistance arises from the lightly doped n^- region. Applying this assumption and substituting (2.12) into (2.13) will yield

$$r_{on} = \frac{W_N}{Aq(\mu_n n_e(x) + \mu_p p_e(x))} \quad (2.14)$$

In the case of unipolar devices, the amount of minority carriers injected into the drift region is negligible. Hence, (2.14) may be re-written as

$$r_{on} = \frac{W_N}{AqN_d\mu_n} \quad (2.15)$$

Specific on resistance is a parameter that is independent of device cross-sectional area and is defined as

$$r_{on,sp} = r_{on}A \quad (2.16)$$

where $r_{on,sp}$ is specific on resistance.

To derive a relationship in between $r_{on,sp}$ and V_{Br} , we start by substituting (2.11) into (2.15) to yield

$$r_{on} = \frac{W_N^2}{A\varepsilon_0\varepsilon_r\mu_n E_c} \quad (2.17)$$

(2.6) may then be substituted into (2.17) to eliminate W_N . The resulting expression for r_{on} may be substituted into (2.16) to yield

$$r_{on,sp} = \frac{4V_{Br}^2}{\varepsilon_0\varepsilon_r\mu_n E_c^3} \quad (2.18)$$

As seen in (2.18), the specific on-resistance varies with square of breakdown voltage. However, in practice, the exponent is higher due to doping dependencies of μ_n and E_c . As a result, the exponent value is typically approximated as 2.5. At this point, it is important to note that (2.18) is only valid for unipolar devices and not bipolar devices as it was assumed in (2.15) that the concentration of minority carriers injected into the drift region is negligible.

(2.18) presents a few implications. First, it shows that a device with a higher blocking voltage will possess a higher on-resistance and hence be able to carry less current. It also suggests that for a low on- resistance, it is beneficial for the p-n

junction to be made using materials with a high E_c , μ_n and ϵ_r . A high E_c , in particular, is of great value as $r_{on,sp}$ is inversely proportional to the cube of E_c . This explains why wide bandgap devices like GaN HEMTs possess such good potential because they have high critical fields.

In addition to the trade-off in between a device's rated blocking voltage and current ratings, one must also understand the trade-off in between these two quantities and switching frequency. When the p-n junction transits from a conducting to a non-conducting state, additional free carriers must be swept out from the drift region so that the depletion region may widen to block the voltage. When the p-n junction transits from a non-conducting to a conducting state, charges must be placed back into the drift region for conduction. The switching time depends on how fast the charges can be placed into and taken out of the drift region as well as the amount of charge in the drift region. A larger drift region translates to more charge and hence a larger switching time. With a longer switching time, more switching losses will be incurred and hence switching frequency must be reduced to ensure the device does not overheat. For a high switching frequency, it is ideal to keep the drift region small but for high current rating, the A must be increased and for a high voltage rating, W_N must be increased. Hence, there is a trade-off in between the voltage rating, current rating and switching frequency. Due to this trade-off different switches have different operating ranges as depicted in Figure 2.13.

Figure 2.13: Operating ranges of different switches [14]

2.4.4: Advantage of GaN HEMTs over silicon MOSFETs

After critically examining the operating ranges of different power transistors, it can be seen that the only other power transistor that operates in a similar low power high frequency range as the GaN HEMT is the silicon MOSFET. It is for this reason that most papers tend to compare GaN HEMTs with silicon MOSFETs as they can both be used for the same applications. As GaN HEMTs have a higher critical field, a smaller drift region may be engineered for the same amount of blocking voltage. Hence GaN HEMTs have lower switching losses and can be operated at higher frequencies than silicon MOSFETs.

2.4.5: Availability, ratings and cost of GaN HEMTs

In Table 2.3, the availability, ratings and cost of commercial GaN HEMTs are shown. Focus is placed upon GaN HEMTs from commercial companies as it is expected that the devices are in a higher level of maturity. In [56], the authors give a more detailed summary pertaining the availability of GaN HEMTs which includes GaN HEMTs from research organisations like HRL. As seen by Table 2.3, GaN HEMTs with a voltage rating of up to 650V are easily available online. 1200V GaN HEMTs are beginning to emerge but require more time to mature as the performance of high voltage GaN HEMTs are limited due to the current collapse phenomenon [57].

Table 2.3: Availability cost and ratings of various GaN HEMTs

Manufacturer	Voltage (V)	Current (A)	Availability	Cost (USD)
Transphorm	600	9	Online	10.56
		17		12.87
		70		196.71
	650	16		12.10
		20		11.88
		35		23.01
		50		31.46
GaN systems	100	45	Online	5.64
		90		7.60
	650	7.5		9.35
		15		12.14
		22.5		17.17
		30		16.25
		60		54.78
EPC	15	3.4	Online	1.67
	30	16		3.49
		60		4.94
	40	10		0.92
		53		2.43
		90		5.00
	60	1		0.36
		23		5.22
		90		5.06
	80	6.8		1.90
		48		4.36
		90		5.15
	100	6		0.98
		48		4.45
		90		5.25
	200	11		7.58
		22		4.11
		48		5.52
Exagan	650	100A [58]	Custom-made wafer directly from manufacturer	Depends on customer specifications
	1200	Unknown		
Powdec	1200	Unknown	Custom-made wafer directly from manufacturer	Depends on customer specifications

2.5: Simulation requirements of power transistors

Power transistor models are useful for predicting the following:

- 1) Power loss
- 2) Temperature rise
- 3) di/dt and dv/dt
- 4) Voltage and current overshoots
- 5) Switching times

For unipolar devices like the HEMT and the metal-oxide semiconductor field effect transistor (MOSFET), the above quantities are linked to a few aspects of the power transistor. These are namely the following:

- 1) I-V characteristics of the channel
- 2) Device capacitances and charges
- 3) I-V characteristics of the body diode
- 4) Gate leakage current
- 5) Thermal characteristic of the package
- 6) Package parasitics

In the next few sections, the significance of these aspects is elaborated upon.

2.5.1: I-V characteristics

The I-V characteristics influence the switching losses as well as the conduction losses of the device. Hence it is important to model this aspect correctly so that the power loss predicted by the switch is correct. In addition, the i-v characteristics have an influence on the switching trajectory of the model as seen in Figure 2.14(b) and hence is expected to influence the di/dt and dv/dt .

I-V characteristics also exhibit a temperature dependence which is reflected by a change of on-resistance as seen in Figure 2.15. This change significantly impacts the conduction losses of the GaN HEMT at elevated temperatures.

(a) Gate charge plot of unipolar device

(b) I-V characteristic of unipolar device with superimposed switching trajectory

Figure 2.14: Gate charge plot and corresponding i-v characteristics as seen in [59]

Figure 2.15: Variation of on-resistance with junction temperature [60]

2.5.2: Device capacitances and charges

Power transistors can be thought of as charge-controlled switches. By injecting varying amounts of charge into the gate, charge is redistributed amongst the capacitances of the device and change the characteristics of the power transistor dynamically. The speed at which power transistors switch is dependent on how fast charges can be injected into or taken out of the gate. Hence it is important to model the various capacitances within the device so as to accurately determine the switching losses, di/dt , dv/dt and switching times.

Under slow switching conditions, gate charge plots like the one seen in Figure 2.14(a) can be made. The gate charge can be segregated into portions that can be attributed to the charges of different capacitances on the device. As seen in Figure 2.16, the device capacitances of a unipolar device are illustrated. As the gate-voltage rises from 0V to miller plateau voltage, V_{GP} , the C_{gs} capacitance is charged up. Hence the dv/dt of the red portion labelled 'A' of the gate charge plot is limited by the value of C_{gs} . During the miller plateau corresponding to region 'B', the miller capacitance is being discharged, hence the dv/dt of that portion is limited by the miller capacitance, C_{gd} . As the gate voltage rises above the miller plateau, the transistor's operation transits from the saturation region to the linear region. Further increase of gate voltage enhances the channel.

Figure 2.16: Generic power transistor model

2.5.3: I-V characteristics of the body diode

The body diode is responsible for the reverse recovery behaviour of the device as well as the conduction of the current during the dead-time. The body diodes of MOSFETs and HEMTs are not well optimised. Hence, the power loss contribution of the body diode is not negligible. Unlike MOSFETs, the HEMT does not possess an integrated p-i-n diode as its body diode. Instead, for the reverse conduction that occurs during the dead-time, the gate-drain contacts act as the control terminals instead of the gate-source contacts in the case of forward conduction. When the voltage across the gate-drain contacts increases beyond the threshold voltage, the HEMT turns on and allows current to flow in the reverse direction. The gate-drain voltage influences the i-v characteristic of the HEMT unlike the case of MOSFETs. By varying the voltage at the gate during the dead-time, the HEMT will exhibit more or less losses depending on the level of applied gate voltage.

The body diode also exhibits a temperature dependence as seen in Figure 2.17 which can be used to predict the junction temperature of the device. This dependence implications on electro-thermal modelling.

Figure 2.17: Body diode i-v characteristics of HEMT at different temperatures [60]

2.5.4: Gate leakage current

Unlike the MOSFET, the gate leakage current of the GaN HEMT is significantly larger. In various MOSFETs [61, 62, 63], the gate leakage currents are typically in the order of a few μA whereas in GaN HEMTs [64, 65, 66], the gate leakage currents are typically in the order of a few mA. This high level of leakage current is caused by the structure of the gate of a GaN HEMT. In a GaN HEMT, the gate contact typically consists of either metal or a highly doped polysilicon material. Hence, the gate and the barrier layer form a Schottky junction with i-v characteristics similar to that of a Schottky barrier diode as seen in Figure 2.18. It can also be seen through this figure that the i-v characteristics of this schottky diode varies with temperature. By contrast, the gate of a silicon MOSFET is isolated from the substrate layer by silicon dioxide which has been known to be a very effective insulator. The significantly higher gate leakage currents have implications on both gate drive design and gate charge extraction procedure.

Figure 2.18: Gate leakage current i-v characteristics

In terms of gate driver design, engineers would typically opt for the bootstrap gate driver to save costs. In these gate drivers, the bootstrap capacitor must supply the current to turn the top transistor of the half-bridge on. Since GaN HEMTs draw a leakage current continuously while they are on, the bootstrap capacitor discharges more quickly over time compared with a silicon MOSFET. Hence, a larger bootstrap capacitor may be required depending on design requirements.

In order to characterise the device capacitances, knowledge of how the voltage of these capacitances varies with their respective charge is required. This information can be extracted from a gate charge plot. In terms of gate charge extraction procedure, the significantly high gate leakage currents can result in an error when accounting for the actual amount of charge that is required to charge and discharge the capacitances. The amount of leakage charge that goes across the Schottky diode in the gate must be accounted for and subtracted from the total gate charge in order to obtain the amount of charge that enters the capacitances.

2.5.5: Thermal characteristic of the package

In order to determine the temperature rise of the power transistor, the thermal resistance of the thermal path in between the junction of the power transistor and the ambient air must be known. The value of thermal resistance for the power transistor is typically given in datasheets. For converters operating in steady state, knowledge of only the thermal resistances is sufficient for sizing the cooling system.

In some instances, converters may be designed to process high amounts of power for very short millisecond or microsecond durations rather than continuously. In such cases, it is necessary to consider the thermal capacitances associated with the thermal path in order to avoid over-sizing the cooling system. In this regard, Foster and Cauer

thermal networks like the ones depicted in Figure 2.19 may be used to model the thermal impedance associated with the transistor package. Of the two networks, the Foster network is typically used as its associated parameters are more easily extracted from datasheets.

Figure 2.19: Thermal networks

2.5.6: Package parasitics

The parasitic inductances of a typical power transistor are depicted in Figure 2.20. These inductances are undesirable as they limit the switching speed of the power transistor and hence lead to more device losses. In cascode-driven devices, these inductances have been reported [67, 68, 20] to lead to unwanted oscillations that eventually destroy the device. Hence, minimising the parasitic inductances of the transistor package has been one of the focuses of manufacturers of GaN transistors. The packages that have resulted from the efforts of these manufacturers are different from those that have been typically employed by slower silicon-based devices. In Table 2.4, the packages typically used as part of silicon transistors are placed beside those used by GaN transistors. Due to the importance of parasitic inductances and the wide range of newly-emerging device packages for GaN transistors, it is important to be able to accurately reflect these parasitic inductances in the simulation.

Figure 2.20: Transistor with package inductances

Table 2.4: Comparison of packages for silicon and GaN transistors

	Packages for silicon transistors	Packages for GaN transistors
Low power applications	<p>(a) PQFN package</p>	<p>(b) LGA package</p>
Medium power applicatoins (through-hole)	<p>(c) TO-220 package for silicon</p>	<p>(d) TO-220 package for GaN</p>
Medium power applications (surface mounted)	<p>(e) D2-Pak</p>	<p>(f) GaN_{PX} packaging</p>

2.6: Power Transistor Modelling Review

There are a few different physical phenomena of power transistors that authors focus on in order to describe their behaviour. These physical phenomena and the techniques required to model them accurately were briefly presented in [69] and are re-examined here in order to identify what physical phenomena in GaN HEMTs to focus modelling efforts on and how to model these physical phenomena.

2.6.1: Physical phenomena in power transistors

Based on [69], there are five physical phenomena that are the focus of modelling:

- 1) Resistivity modulation
- 2) Charge storage
- 3) Metal-insulator-semiconductor (MIS) capacitances
- 4) Electro-thermal behaviour
- 5) Breakdown

Resistivity modulation refers to the variation of a device's resistance due to the presence of both electron and hole charge carriers. It is also known as conductivity modulation. Since this physical phenomena involves both types of charge carriers, it primarily plays a part in bipolar devices like p-i-n diodes, bipolar junction transistors (BJTs), thyristors, gate turn-off thyristors (GTOs), insulated gate bipolar transistors (IGBTs) and MOS-controlled thyristors (MCTs). In MOSFETs, this phenomena is important as the parasitic body diode is a p-i-n diode. Resistivity modulation does not play a part in unipolar devices like Schottky diodes or HEMTs.

Charge storage refers to a phenomenon that occurs in bipolar devices. When these devices conduct, some charges are stored in the lightly doped region also known as the drift region. In order for the device to block voltages when it is off, the stored charge in this region must first be removed. The removal of this charge during switching results in reverse recovery and translates to increased device losses and electromagnetic emissions. This physical phenomena is relevant for bipolar devices but not relevant for the HEMT which is a unipolar device.

The third physical phenomenon to be covered is the MIS capacitances. The switching of voltage-controlled devices like MOSFETs, IGBTs and HEMTs is done through the use of a MIS capacitor which serves as the gate of the device. In order for these devices to switch properly, certain amounts of charge must either be accumulated at or depleted from different regions of the device. These regions can be modelled electrically as non-linear capacitances. For voltage-controlled devices, the most important capacitance that must be modelled is that in between the gate and anode of the device. This capacitance is also known as the miller capacitance. This capacitance is very significant as most of the device losses typically occur during the discharging or charging of this capacitance.

The fourth physical phenomenon is electro-thermal behaviour. The behaviour of semiconductors changes with temperature. For a power device in operation, the temperature of the device increases over time due to self-heating. As a result of this self-heating, device properties such as the on-resistance and i-v characteristics are expected to change. This physical phenomenon is relevant for all devices but the extent of its influence on the device behaviour varies depending on which device is in question.

The fifth physical phenomenon is breakdown. Modelling this physical phenomenon is important for predicting the reliability and expected lifetime of power devices. Common mechanisms involved in breakdown include impact ionisation, zener breakdown and punchthrough. In the case of GaN HEMTs, especially those designed for high voltages, there is an interest in the phenomenon of dynamic on-resistance [70, 71, 72], also known as current collapse [73, 57]. This phenomenon is caused by the formation of electron traps that occur at the heterojunction and is more prevalent at higher blocking voltages.

The influence of the presented physical phenomena on power device behaviour varies depending on the device geometry. In [69], a table reflecting the relevance of different physical phenomena for different power devices was presented. The table is reiterated in Table 2.5 with an additional column for the HEMT and an additional row for the physical phenomena of piezoelectric polarisation.

Table 2.5: Relevance of different physical phenomena for different power transistors (++ very important, + important, 0 to be included, - less important, -- not applicable)

	Diode	BJT	Thyristor/GTO	MOSFET	IGBT, MCT	HEMT
Resistivity modulation	++	++	++	++	++	--
Charge Storage	++	++	++	-	++	--
MIS capacitances	--	--	--	++	++	++
Electro-thermal behaviour	+	+	+	+	+	+
Breakdown	0	0	+	0	0	0
Piezoelectric polarization	--	--	--	--	--	++*

* Only in GaN HEMTs

2.6.2: Power transistor modelling techniques

In order to model these physical phenomena, a few techniques are available as mentioned below:

- 1) Functional model
- 2) Approximate solution

- 3) Transformation
- 4) Lumped model
- 5) Numerical solution

The functional modelling approach involves treating the device as a “black box”. Functional models [74, 75, 76] describe the externally observed behaviour of the device without regard for its internal device physics. Functional modelling approaches include use of low-power device models to simulate the behaviour of high power device models, lookup tables and empirical expressions. The functional approach to modelling is generally easier than the other approaches but the resulting models also typically lack accuracy.

The second approach is the approximate solution. In this approach, the model equations are based on physics but since the exact solutions to these equations are hard to obtain or valid only for a few special cases, an approximate solution is proposed by assumption [77], substitution using a time derivative [78] or neglecting of terms [79].

The third approach is transformation. Physics-based equations, like the Fick’s law diffusion equation are typically differential equations that can be solved through the application of Laplace transformation [80, 81] or Green’s functions [82]. This approach is generally more exact compared with the functional approach but can get significantly more tedious depending on the boundaries of the problem.

The fourth approach is the lumped model [83, 84, 85] which involves dividing the device into several charge storing regions. The charge of each region is assigned to a node and the charge difference in between each node determines the current that flows in between each region.

The final approach is the numerical solution which involves the discretization of the region into a finite number of mesh points. This method is the most accurate but requires the most computation time and resources to execute. Under this category of approaches is the method of finite differences [86, 87] and the finite element method [88].

2.6.3: Review of existing GaN Transistor models

As GaN HEMTs were initially introduced for RF applications before being adopted in the power electronics field, a vast majority of device models for GaN HEMTs

were designed for RF applications [89, 90, 91, 92, 93] rather than power electronics applications. RF models focus mainly on parameters like gain and s-parameters which are not relevant parameters for power electronics applications.

For power electronics applications, authors often adopt simple behavioural models to describe parameters like the transconductance [26], the capacitances [27, 94]. As these models have no basis in device physics, their accuracy is questionable. A few authors have attempted to describe the i-v characteristics as well as the capacitances by employing approximate solutions [95, 96]. These physics-based models are in general accurate but require prior knowledge of device parameters like doping and gate length to use and are hence impractical to the power electronics engineer. In order to create an accurate yet practical GaN power transistor model, a hybrid model involving both the functional and approximate solution approaches may be a viable model.

Hence, for the power transistor model developed in this work, a functional approach was used for describing the device capacitances and an approximate solution approach was adopted for describing the i-v characteristics of the device under the influence of the piezoelectric effect.

2.7: Parasitics

It has been noted by numerous authors [24, 97, 20, 98, 99, 100] that parasitic inductance degrades the performance of the switch and must be accounted for during simulation and design. Two such critical inductances are those in the commutation loop and the gate driver loop. In Figure 2.21, these loops are presented along with their respective equivalent inductances, L_{com} and L_{gate} and their effects on switching performance will be covered in the subsequent paragraphs.

The voltage, of an inductor is related to the rate of change of current and its inductance according to (2.19).

$$v_L = L \frac{di_L}{dt} \quad (2.19)$$

where v_L represents voltage across the inductor, L represents inductance, i_L represents current and t represents time.

During switching of the lower switch, changes in gate driver current cause a voltage to be imposed across L_{gate} which opposes the charging or discharging of the gate.

This slows down the switching speed of the power transistor and hence results in more losses. L_{gate} also forms a series RLC circuit which must be sufficiently damped to prevent voltage overshoots. Using piece-wise linear plots for the gate-source voltage, V_{gs} , drain-source voltage, V_{ds} , and drain-source current, I_{ds} , Figure 2.22, L_{com} causes voltage overshoots across the lower switch during turn off, hence increasing turn-off energy of the lower switch. During turn-on, the voltage across L_{com} causes the drain-to-source voltage to decrease, hence reducing turn-on energy of the lower switch. L_{com} also simultaneously causes the voltage of the upper upper switch to spike during turn-on of the lower switch. This voltage spike increases the turn-off losses across the body diode during the dead-time. By varying L_{com} , the switching losses are redistributed in between the top and bottom switches.

Figure 2.21: Half-bridge with commutation and gate driver loops

Figure 2.22: Effect of commutation inductance on turn-on and turn-off behaviour of switch

The inductance of both the commutation and gate driver loops is dependent on the geometry of the traces through which the current in these loops flow. It is therefore important to review the various ways of how to calculate the parasitic inductance so that a relationship can be drawn in between the inductance and geometrical parameters of the PCB. In general, expressions for inductance may be derived through the use of physics principles and vector calculus or approximated by assuming that the structure in question possesses the same inductance to another simplified but similar structure. The approaches for deriving expressions for inductance through the use of physics principles and vector calculus is reviewed first. Then the inductance of various structures is examined to find a relation in between the inductance and geometrical parameters of the PCB.

(a) Lateral commutation current loop

(b) Vertical commutation current loop

Figure 2.23: Examples of commutation current loops [24]

First, the possibility of deriving the inductance associated with the gate driver and commutation loops through the use of physics principles is explored. As these loops are usually rectangular as depicted in Figure 2.23 and the forward and return paths are typically placed on adjacent layers to minimise the parasitic inductance. An expression must therefore be derived involving thickness of the PCB, t , width of the trace, w , and length of the overall loop, l . For a generic current loop depicted in Figure 2.24, there are a few ways of defining the stored magnetic energy, E_m and the associated inductance L .

Figure 2.24: Generic current loop

The definitions of self-inductance and stored magnetic energy can be classified into two broad categories as detailed in [101]. The first category involves vector magnetic potential, $\vec{A}$, and current density, $\vec{J}$, integrated throughout the volume of the conductor. This category of equations is frequently used by computer programs like ANSYS to extract the parasitic and partial inductances of three dimensional structures. The second category involves magnetic field strength, $\vec{H}$, and the flux density, $\vec{B}$, integrated throughout the entirety of space. Since the boundary of the second category is theoretically at infinity, computer programs typically do not employ these equations for computation as an accurate calculation will in theory last forever. However, the equations derived in this category are typically used by engineers to understand the nature of the inductances as the physical quantities involved are more relatable.

The first category of equations are reviewed and for this purpose, the concept of vector magnetic potential must be explained. Vector magnetic potential is a purely mathematical construct. It is related to the magnetic field as defined in (2.20).

$$\vec{B} = \vec{\nabla} \times \vec{A} \quad (2.20)$$

where flux density and vector magnetic potential are given by $\vec{B}$ and $\vec{A}$ respectively. Vector magnetic potential has no physical significance and its purpose is to make the derivation of quantities easier.

The energy stored in a magnetic field generated by a generic conductor is

$$E_m = \iiint_{V_c} \left[\int_0^{A_f} \vec{j} \cdot d\vec{A} \right] dv \quad (2.21)$$

where E_m , V_c and A_f represent magnetic energy volume of the conductor and final value of the vector magnetic potential respectively.

Over time, current density is built up in the conductor. Correspondingly, vector magnetic potential builds up from 0 to its final magnitude, A_f . The internal integral is therefore the integration of $J dA \cos \theta$ where θ is the angle in between $\vec{A}$ and $\vec{j}$.

For a linear magnetic environment, where $\vec{A}$ is linearly proportional to $\vec{j}$ at any point in the conductor, (2.21) can be rewritten as

$$E_m = \frac{1}{2} \iiint_{V_c} \vec{j} \cdot \vec{A} dv \quad (2.22)$$

Since $\vec{A}$ is linearly proportional to $\vec{j}$, it can be expected that the energy is directly proportional to the square of the current through the inductor. Hence, E_m may also be expressed as (2.23) where L is the self-inductance of the loop.

$$E_m = \frac{1}{2} L i_L^2 \quad (2.23)$$

By equating (2.22) and (2.23), the inductance can be found as shown in.

$$L = \frac{1}{i_L^2} \iiint_{V_c} \vec{J} \cdot \vec{A} dv \quad (2.24)$$

(2.24) does not allow the user to easily relate the geometry of the traces to the self-inductance.

For a linear magnetic environment in free space, $\vec{A}$ is related to $\vec{J}$ through,

$$\vec{A}(u_1, u_2, u_3) = \iiint_{V_c} \frac{\mu_0 \vec{J}'(u'_1, u'_2, u'_3)}{4\pi R} dv' \quad (2.25)$$

where μ_0 represents the permeability of free space, u_1, u_2 and u_3 are coordinates of the field point of $\vec{A}$ whereas u'_1, u'_2 and u'_3 are the coordinates of the source point. R is the distance from the field point to the source point and dv' is an infinitesimally small volume containing a current of current density, $\vec{J}'$.

By substituting (2.25) into (2.24), we obtain

$$L = \frac{1}{i_L^2} \iiint_{V_c} \iiint_{V_c} \frac{\mu_0 \vec{J}' \cdot \vec{J}}{4\pi R} dv' dv \quad (2.26)$$

This form still does not relate the geometrical parameters to the self-inductance easily.

The second category of equations is reviewed next. In general, the magnetic energy stored in an inductor can be found as shown in (2.27)

$$E_m = \iiint_{V_{sp}} \left[\int_0^{B_f} \vec{H} \cdot d\vec{B} \right] dv \quad (2.27)$$

where B_f is the final value of the magnitude of the magnetic flux density at a specific point in space and V_{sp} is the volume of the space occupied by the magnetic field that has been chosen for integration.

In a linear magnetic environment, $\vec{B}$ is linearly proportional to $\vec{H}$. Hence, (2.27) may be rewritten as

$$E_m = \frac{1}{2} \iiint_{V_{sp}} \vec{B} \cdot \vec{H} dv \quad (2.28)$$

Inductance may be found by substituting (2.23) into (2.28) to obtain ..

$$L = \frac{1}{i_L^2} \iiint_{V_{sp}} \vec{B} \cdot \vec{H} dv \quad (2.29)$$

This equation still does not relate the geometrical parameters of the PCB trace with the self-inductance easily

The energy stored in the magnetic field may be thought of as consisting of two components. These are the energy stored by the field inside the conductor and the energy field stored outside of the conductor. This information is reflected in

$$E_m = \frac{1}{2} \iiint_{V_i} \vec{B} \cdot \vec{H} dv + \frac{1}{2} \iiint_{V_e} \vec{B} \cdot \vec{H} dv \quad (2.30)$$

where V_i refers to the volume inside of the conductor and V_e refers to the volume outside of the conductor.

(2.30) implies that the self-inductance of the loop may also be decomposed into the internal and external components as reflected in

$$E_m = \frac{1}{2} L_i i_L^2 + \frac{1}{2} L_e i_L^2 \quad (2.31)$$

where L_i and L_e are the inductance component arising from the field within the conductor and inductance component arising from the field outside the conductor.

Based on the derivation given in [101], (2.28) may be decomposed to yield

$$E_m = \frac{1}{2} \iint_S \oint_{l'} (\vec{H} \cdot \hat{b}) B dl' ds \quad (2.32)$$

where $\hat{b}$ is a unit vector in the direction of the magnetic field, B is the magnitude of the magnetic field, dl' represents an infinitesimally small element on a generic closed loop l' and ds represents an infinitesimally small element on an open surface S which is perpendicular to $\vec{B}$. (2.32) may be further rearranged to yield

$$E_m = \frac{1}{2} \iint_S \oint_{l'} \vec{H} \cdot \overrightarrow{dl'} B ds \quad (2.33)$$

At this point, it can be seen that ampere's law can be applied to give

$$E_m = \frac{1}{2} \iint_S i_L(l') B ds \quad (2.34)$$

where i_L is the current enclosed by l' contributing to the magnetic field strength at a point on S . For a generic conductor such as the toroid depicted in Figure 2.25, S may be constructed such that all flux generated by the conductor passes through it. At this point, S may be further partitioned into two parts – S_{in} , which is the part in the conductor and S_{ex} , which is the part out of the conductor. This partitioning implies that E_m may once again be split into two components – one internal to the conductor and another external to the conductor as seen in

$$E_m = \frac{1}{2} \iint_{S_{in}} i_L(l') B ds + \frac{1}{2} i_L \iint_{S_{ex}} B ds \quad (2.35)$$

Figure 2.25: Toroid cross section with open surfaces S_{in} and S_{ex} [101]

(2.35) can be further simplified to yield

$$E_m = \frac{1}{2} \iint_{S_{in}} i_L(l') B ds + \frac{1}{2} i_L \phi_{m,ex} \quad (2.36)$$

where $\phi_{m,ex}$ represents the flux passing through S_{ex} .

Equating (2.36) with (2.23), the following can be derived

$$L = \frac{1}{i_L^2} \iint_{S_{in}} i_L(l') B \, ds + \frac{\phi_{m,ex}}{i_L} \quad (2.37)$$

The second term of (2.37) corresponds to the external inductance. When the conductor wire is very thin, the self-inductance of the wire can be approximated as the external inductance as shown in

$$L \approx L_e = \frac{\phi_{m,ex}}{i_L}, \quad S_{in} \ll S_{ex} \quad (2.38)$$

(2.38) is the typical formula for inductance that is presented in physics textbooks [102].

Figure 2.26: Current loop distribution

The external flux can also be re-expressed in terms of vector magnetic potential as depicted in (2.39).

$$\phi_{m,ex} = \iint_{S_{ex}} \vec{B} \cdot d\vec{s} = \iint_{S_{ex}} (\vec{\nabla} \times \vec{A}) \cdot d\vec{s} = \oint_{l_s} \vec{A} \, dl_s \quad (2.39)$$

where l_s represents a closed path encircling open surface S . For the case of linear magnetic environment in free space, (2.25) and (2.39) may be substituted into (2.38) to yield

$$L_e = \frac{1}{i_L} \oint_{l_s} \iiint_{V_c} \frac{\mu_0 \vec{J}'}{4\pi R} dv' \, dl_s \quad (2.40)$$

For the case of thin wires, the current may be assumed as being concentrated on a closed path l_c as depicted in Figure 2.26 (2.40) may be re-written as

$$L_e = \oint_{l_s} \oint_{l_c} \frac{\mu_0}{4\pi R} dl_c dl_s \quad (2.41)$$

which is also known as Neumann's inductance formula. This formula is useful for deriving the mutual inductance expressions associated with various structures [103, 104, 105]. However, the derivation is typically very long and complicated even for simple structures [106]. The complexity of these equations make it hard for the user to see the effect of varying various aspects of the PCB geometry.

It can be seen at this point that deriving expressions for the inductance of these rectangular loops through the use of physics principles is not a feasible strategy. Hence, the second approach of approximating these rectangular loops with simpler structures is considered. There are a few such structures used in PCBs as shown in Figure 2.27. As lateral loops have been shown to reduce efficiencies significantly [24], edge-coupled traces are not suitable for approximating the inductances of the gate driver and commutation loops. For this work, the expression for the broadside-coupled traces was chosen for its relative simplicity. The expression is presented in

$$L = \frac{\mu_0 \mu_r l_{PCB} t_{PCB}}{w_{PCB}}, \quad w_{PCB} \gg t_{PCB} \quad (2.42)$$

where l_{PCB} , t_{PCB} and w_{PCB} represent, the length, thickness and width of the PCB trace respectively. The implications of (2.37) on the inductance geometry is discussed further in Chapter 4.

Figure 2.27: Cross sections of various PCB structures

2.8: Verification techniques

In order to verify the accuracy of the developed half-bridge model, experimental techniques must be developed to extract the following quantities:

- 1) Power loss
- 2) Waveforms
- 3) Junction temperature

The power loss of a converter can be measured through either electrical or thermal methods as reviewed in various papers [107, 108]. In general, electrical methods are easier and faster but less accurate whereas thermal methods are harder and slower but more accurate. Thermal methods require a high amount of development effort to custom-make the calorimeter and measurements often take a few hours [109, 110, 111] as the setup needs time to reach thermal equilibrium. Hence for this work, it was decided that a suitable electrical method be used. Based on [108], the following electrical methods are identified:

- 1) Input and output power measurement
- 2) Measurement of instantaneous voltage and current
- 3) Opposition method

The simplest electrical way to measure power loss is to subtract the output power, from the input power as seen in (2.43)

$$P_l = P_i - P_o \quad (2.43)$$

where P_o , P_i and P_l represent output power, input power and power loss respectively.

However, this method is very inaccurate and the relative uncertainty of P_l increases with converter efficiency according to (2.44).

$$\frac{\Delta P_l}{P_l} = \frac{1}{1 - \eta} \frac{\Delta P_i}{P_i} + \frac{\eta}{1 - \eta} \frac{\Delta P_o}{P_o} \quad (2.44)$$

where η represents converter efficiency.

Hence, this method is not suitable for measuring the power losses of highly efficient converters. For instance, if the relative uncertainty on both the input and output power is 0.1 percent and the converter efficiency is 99 percent, a relative error of 19.9 percent can be expected for the power loss.

The second electrical way to measure power loss is to measure instantaneous voltage and current. This is done through the use of the oscilloscope along with appropriate voltage probes and current sensors which are incorporated into the circuitry. It has

been noted however, that when this method is used for measuring fast-switching devices, large errors may occur [112, 113, 114]. This is caused by propagation delays in between the voltage and current probes [115]. It has also been noted [116] that parasitics associated with the probes like the probe capacitance can interfere with the accuracy of the measurement and have to be compensated for with accurate probe models. In addition, the scope and probes have minimum rise times. This translates to a minimum combined system rise time which limits the speeds of transients that the system can accurately measure. The relation in between these times is given in (2.45)

$$t_{sys} = \sqrt{tr_{probe}^2 + tr_{scope}^2} \quad (2.45)$$

where t_{sys} , tr_{probe} and tr_{scope} are the rise times associated with the measurement system, the probe and the oscilloscope respectively. The rise times of individual components in the measurement chain are related according to their bandwidths according to

$$t_r = \frac{0.35}{BW} \quad (2.46)$$

where t_r and BW represent the rise time and bandwidth of a generic component in a measurement chain.

It was suggested in [115], that in order to maintain an accurate measurement of the rise time, the ratio of the system to source bandwidths must be about three to five. This place a very high requirement on equipment used to measure GaN transistors which typically have switching times in the order of a few nanoseconds. It has been estimated [22] that in order to accurately measure the switching times of GaN transistors, both the probe and the oscilloscope must possess a bandwidth in the range of a few GHz.

The third electrical method to consider is the opposition method. It uses the setup shown in Figure 2.28. The setup consists of an electrical source with two copies of the system to be characterised. The first of the copies, system 1, acts as a generator whilst the second one, system 2, acts as a receptor. The aim of the setup is to circulate a high power, P_I , through the circuit whilst only supplying the losses of both systems, P_{lo1} and P_{lo2} , through the use of the electrical source.

Figure 2.28: Generic setup of opposition method depicting flow of power losses

Compared with the previous two methods, there are three advantages:

- 1) The power source is minimised as the source only supplies the load.
- 2) There is no need for a dissipative load
- 3) The total power losses can be extracted directly with a high degree of accuracy

In order for the opposition method to work, the system under test must have the following properties:

- 1) Reversibility
- 2) Symmetry of operating modes

The system is considered reversible if it is able to function as both a generator and as a receptor. In addition to this, the operating conditions of both systems have to be chosen such that the losses in each system are the same. That is to say, that the systems generate the same losses whether they are in generator mode or receptor mode. In other words, the operating modes of the systems must be symmetrical.

A simple example of such a system is a half-bridge which is depicted in Figure 2.29 as two transistors with a bus capacitor. Two such half-bridges can be linked together as depicted in Figure 2.30 as part of the opposition method setup. In Figure 2.30, it is assumed that the additional passives added are purely reactive. In practice these components consume minute amounts of power.

Compared with the instantaneous power measurement method, the opposition method has an additional advantage in that it does not require an oscilloscope for measurement and is hence not affected by instrument bandwidth or parasitics of probes. This makes it more suitable for measuring the losses of a GaN converter under more practical, fast-switching conditions.

Figure 2.29: Half-bridge

Figure 2.30: Opposition setup for characterising switching losses of half-bridge

The waveforms of the current and voltage that appear across the device during switching are of interest to the power electronics engineer as the di/dt and dv/dt of the waveforms are related to the EMC requirements of the filter. Hence, it is desirable to be able to observe these waveforms under operating conditions that closely resemble those in the actual converter. The typical way of observing switching waveforms is the double pulse test method which has been used by various authors [117, 118, 119, 97, 120]. This method uses the circuit of Figure 2.31 and is typically used for extraction of switching energies for the purposes of loss characterisation of converters. Since the waveforms are observed using an oscilloscope, the method suffers from the same problems associated with instantaneous power measurement like probe parasitics and limited instrument bandwidth. These factors cause the observed waveforms to be distorted compared to the actual ones. In addition, the current measurement is done with a current shunt which increases the parasitic inductance of the commutation loop and limits the speeds at which the device under test (D.U.T.) can be switched. Due to the fast switching speeds of GaN HEMTs, it is not advisable to use this method to extract the switching energies for the purposes of loss characterisation of a GaN-based power converter. However, if the switches are switched slowly, the waveforms can still be used for modelling the switch.

Figure 2.31: Double pulse tester schematic

The third quantity that must be extracted for transistor modelling is the junction temperature. Many methods exist for this purpose as detailed in survey papers [121, 122]. The methods can be divided into three main categories which are electrical, optical and physically contacting. Optical methods such as measurement by thermal camera involve the measurement of temperature-dependent optical parameters like infra-red radiation [123, 124, 125], luminescence and laser deflection [126, 127, 128]. Physically contacting methods involve direct contact of the measurement instrument with the semiconductor die. Examples of these methods include thermocouples [129, 130, 131], thermistors or solutions using liquid crystals or thermographic phosphors [121]. Last but not least are electrical methods which involve the measurement of thermo-sensitive electrical parameters (TSEPs) like body diode forward voltage [132, 133, 134] or gate threshold voltage [135, 136, 137]. A brief summary of the advantages and disadvantages of each method was presented in [121].

In a practical converter, it is very difficult to apply electrical or physically contacting methods as the circuit consists of components other than the semiconductor itself and the device is already packaged. Typically, authors measure the temperature using an infra-red camera [138, 139, 140]. This data can then be used to approximate the value of the junction temperature assuming that the thermal circuit in between the measurement point and the junction is known.

2.9: Chapter summary

In this chapter, the semiconductor devices were reviewed and it was seen that a unique combination of device geometry and material gave rise to the good performance of GaN transistors. In addition, the effect of parasitic inductance and equations that relate this quantity to the geometry of the PCB were reviewed. The verification techniques associated with power transistors were also reviewed.

CHAPTER 3 : GaN POWER TRANSISTOR MODELLING

3.1: Chapter overview

In this chapter, the physics of the GaN HEMT is reviewed. Special attention is given to the phenomenon of piezoelectric polarisation and its effect on the i-v characteristic. In subsequent sections, the equations used to describe the i-v characteristics and the capacitances of the device are described. This is followed by the extraction procedure. It should be noted that for this work, enhancement-mode GaN HEMTs were explored and that the equations and extraction procedure may not apply to depletion-mode GaN HEMTs driven using a MOSFET in cascode.

The model parameters are derived by observing key features of the switching waveforms under slow-switching conditions where the behaviour of the switch is expected to be predominated by the semiconductor and not the parasitics. Hence it is expected that the derived model will be specific to the power transistor and is not dependent on surrounding circuitry.

3.2: Physics of the GaN HEMT

GaN HEMTs are different from typical HEMTs due to the phenomenon of piezoelectric polarisation. As a result of the piezoelectric polarisation, the threshold voltage, i-v characteristics and device charges are different. In this section, the device physics of a typical HEMT is reviewed followed by the physics of a GaN HEMT.

The high electron mobility transistor (HEMT) is also known as the heterojunction field effect transistor (HFET), two-dimensional electron gas field effect transistor (TEGFET) or modulation doped field effect transistor (MODFET). The device primarily consists of two layers of different materials that make up the heterojunction as depicted in Figure 3.1. These layers are known as the barrier layer and channel layer. Formation of the current channel in between drain and source contacts is done through the application of a gate bias which shrinks the depletion region under the gate and consequently connects both drain and source contacts to turn the device on. During operation, carriers from the doped barrier layer diffuse into the channel and are confined at the heterojunction due to the structure of the conduction band as depicted in Figure 3.2(b).

It can be seen from Figure 3.2(b) that a discontinuity in the conduction band, ΔE_c , caused by the difference in bandgaps of the barrier layer material and the channel material help to confine the carriers in the channel during operation. This carrier confinement is further assisted by the built-in potential, V_p , which is a result of the doping. A schottky barrier with barrier height $q\phi_{bn}$ is formed in between the highly-conductive gate and the barrier layer as depicted in Figure 3.2(b). At the threshold voltage V_{th} , as depicted in Figure 3.2(b), the channel begins to conduct. Threshold voltage of a typical HEMT is therefore given by (3.1). Using poisson's equation, (3.2) can be derived for V_p in terms of the dopant concentration, N_d , the thickness of the barrier layer, d , the permittivity of the barrier layer, ϵ_s , and the charge of an electron, q .

$$V_{th} = \phi_{bn} - \frac{\Delta E_c}{q} - V_p \quad (3.1)$$

$$V_p = \frac{qN_d d^2}{2\epsilon_s} \quad (3.2)$$

In literature [141], the typical expression for the charge sheet carrier concentration, n_s , of a MODFET is given by (3.3) where V_c is the channel voltage along the y-direction in the channel and C_i is the capacitance per unit area. (3.4) is derived from the current density equation with the assumption that the diffusion component is small compared with the drift component. By substituting the expression for n_s in (3.3) and (3.4) and then integrating the resulting expression with respect to y , a set of equations which have the same form as that of a silicon MOSFET can be derived as seen in (3.5) where Z and L are the channel width and channel length respectively. It should be noted that for GaN HEMTs, the expression for n_s is significantly different due to the piezoelectric polarisation. As such, the i-v characteristic will differ greatly from that seen in (3.5).

$$n_s(y) = \frac{C_i[V_{gs} - V_{th} - V_c(y)]}{q} \quad (3.3)$$

$$I_{ds} = Zq\mu_n n_s \frac{dV_c}{dy} \quad (3.4)$$

$$I_{ds} = \begin{cases} 0, V_{gs} < V_{th} \\ \frac{Z}{L} \mu_n C_i (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2}, V_{gs} \geq V_{th} \text{ and } V_{ds} > V_{gs} - V_{th} \\ \frac{Z}{2L} \mu_n C_i (V_{gs} - V_{th})^2, V_{gs} \geq V_{th} \text{ and } V_{ds} \leq V_{gs} - V_{th} \end{cases} \quad (3.5)$$

Piezoelectric polarisation is a very important phenomenon in $\text{Al}_m\text{Ga}_{1-m}\text{N}/\text{GaN}$ HEMTs as it increases the carrier concentration of the current channel and consequently, the current-carrying capability of the device to a level higher than HEMTs utilising other material combinations. Due to augmentation of the channel brought about by this effect, the i-v characteristic of a GaN HEMT is significantly different compared with that of a typical silicon MOSFET. Hence, it is important to understand the origin and implications of the piezoeffect.

Figure 3.3: GaN heterojunction under piezoelectric polarisation

The simplified structure of the heterojunction of a GaN HEMT is depicted in Figure 3.3. Due to the slight lattice mismatch in between the GaN and $\text{Al}_m\text{Ga}_{1-m}\text{N}$ layers, a strain is exerted on the $\text{Al}_m\text{Ga}_{1-m}\text{N}$ layer which causes piezoelectric polarization in it. A polarization field exists within the $\text{Al}_m\text{Ga}_{1-m}\text{N}$ layer and consists of both a piezoelectric polarization component, P_{pz}^{AlGa} , and a spontaneous polarization component, P_{sp}^{AlGa} . Likewise, a polarization field exists within the GaN layer consisting of both piezoelectric (P_{pz}^{GaN}) and spontaneous (P_{sp}^{GaN}) polarization component. The polarization-induced charge sheet density, σ , is related to these components according to

$$\sigma = P_{pz}^{AlGa} + P_{sp}^{AlGa} - P_{pz}^{GaN} - P_{sp}^{GaN} \quad (3.6)$$

Due to the fact that the GaN layer is significantly thicker than the $\text{Al}_m\text{Ga}_{1-m}\text{N}$ layer, the piezoelectric polarization in the GaN layer is relatively weak. σ is also a function of the Al mole fraction, m . Hence, (3.6) can be re-written as

$$\sigma(m) = P_{pz}^{AlGa}(m) + P_{sp}^{AlGa}(m) - P_{sp}^{GaN} \quad (3.7)$$

σ is related to the charge sheet density, n_s . Presently, many different proposed expressions for n_s exist [95, 96, 142, 143]. Two such expressions from [142] and [143] relating σ to n_s are presented in (3.8) and (3.9) respectively. d_{AlGaN} and d_{GaN} are the thicknesses of the $Al_mGa_{1-m}N$ and GaN layers respectively. q is the charge of an electron. ϵ_0 is the permittivity of free space whilst $\epsilon_r(m)$ is the relative permittivity of the $Al_mGa_{1-m}N$ layer. ϕ_b and ϕ_b^{eff} are the schottky and effective schottky barrier heights respectively. E_F refers to the Fermi level and ΔE_C refers to the discontinuity in the conduction band. In many physics-based models [95, 96, 142, 143], expressions like (3.8) and (3.9) are used as the basis for deriving the device's behaviour. These models typically yield very good accuracy. However, it can be seen that these expressions involve parameters like mole fraction and layer thickness which are not readily available on data sheets. The resulting expressions for i-v characteristic also tend to be very complicated and not suitable for use in a circuit simulator like SPICE or Saber. A practical model of the GaN HEMT must not only be accurate but simple enough to be simulated with parameters that can be extracted by a typical power electronics engineer.

$$n_s = \frac{\sigma(m)}{q} - \left(\frac{\epsilon_0 \epsilon_r(m)}{d_{AlGaN}}\right) \left[\phi_b + \frac{E_F}{q} - \frac{\Delta E_C}{q}\right] \frac{1}{q} \quad (3.8)$$

$$n_s = \left\{1 + \frac{\epsilon_r(m)}{\epsilon_r(0)} \frac{d_{GaN}}{d_{AlGaN}}\right\}^{-1} \left\{\frac{\sigma(m)}{q} - \left(\frac{\epsilon_0 \epsilon_r(m)}{d_{AlGaN}}\right) \left[\phi_b^{eff} + \frac{E_F}{q} - \frac{\Delta E_C}{q}\right] \frac{1}{q}\right\} \quad (3.9)$$

The piezoeffect also causes the expressions for device charges, and consequently, the device capacitances to be significantly different from that of a typical HEMT. Authors [95, 144, 145] have attempted to take this into consideration when creating physics-based models. However, to date these models were developed for use in RF applications where the GaN HEMT operates in linear mode rather than switchmode as is the case for power electronics applications. A practical model of the device charges must be created in order to describe the GaN HEMT's behaviour under more practical conditions.

3.3: Proposed GaN HEMT model

The structure of the model is seen in Figure 3.4. Behavioural sources b1 and b2 are used to simulate the i-v characteristics of both the forward conduction and reverse conduction of the device when it is on. b3 is used to simulate the i-v characteristics

of the body diode. b4 is used to simulate the gate leakage current. C_{gs} , C_{gd} and C_{ds} are the device capacitances and have been modelled behaviourally using modified sigmoid functions.

Figure 3.4: Model structure

3.4: Modelling of I-V characteristics

The i-v characteristics of a typical unipolar device are derived starting with the continuity equation as seen in (3.10) where J_n is the current density, μ_n is electron mobility, n is charge carrier concentration, E is the applied electric field, T is the temperature of the semiconductor, x is the distance along the current channel, q is the charge of an electron and k is the Boltzmann constant.

$$J_n = \mu_n n q E + k T \mu_n \frac{dn}{dx} \quad (3.10)$$

For a HEMT, (3.10) may be re-written as (3.11) where I_{ds} is the drain-to-source current, n_s is the sheet carrier concentration at position x in the channel. V_c is the channel voltage at position x in the channel and Z is the channel width.

$$I_{ds} = Z q \mu_n \left(n_s(x) \frac{dV_c(x)}{dx} + \frac{k T \mu_n}{q} \frac{dn_s(x)}{dx} \right) \quad (3.11)$$

During switching the channel transits in between strong inversion and depletion regimes which correspond to the on-state and off-state of the device respectively. However, during transition, the device is expected to transit through the weak and moderate inversion regimes. During this transition, the device's i-v characteristic

equation is expected to greatly deviate from that in the strong inversion regime. Also, due to the piezoelectric polarization effect in GaN HEMTs, the expression for the charge sheet carrier concentration is augmented as mentioned in numerous papers [146, 147, 43]. For this paper, the following expression in (3.12), taken from [96], is used for the charge sheet carrier concentration. In (3.12), n_{s0} refers to the sheet carrier concentration under equilibrium conditions. ϵ refers to dielectric constant of the barrier layer. d_d is the depth of the doped portion of the barrier layer. d_i is the depth of the intrinsic portion of the barrier layer. V_{th} is the threshold voltage of the device.

$$n_s = n_{s0} \exp\left(\frac{q\epsilon(V_{gs} - V_c(x) - V_{th} - \frac{q(d_d + d_i)n_{s0}}{\epsilon})}{q^2(d_d + d_i)n_{s0} + \epsilon kT}\right) \quad (3.12)$$

Substituting (3.11) into (3.12), and following through with the derivation mentioned in the appendix section A1, an expression can be written for I_{ds} as shown in (3.13) where K_1 and K_2 are temperature dependent constants and K_3 is a material and geometrically dependent constant.

$$I_{ds} = K_1 \left[\exp\left(K_2(V_{gs} - V_c - V_{th} - K_3)\right) \right] \frac{dV_c}{dx} \quad (3.13)$$

(3.13) can be integrated with respect to x with the upper and lower bounds being 0 and the channel length, L . In order to simplify the resulting equation for use in a simulator, the contact resistances are ignored. The resulting expression from the integration is given in (3.14).

$$I_{ds} = K_4 \left[\exp\left(K_2(V_{gs} - V_{th})\right) \right] [1 - \exp(-K_2 V_{ds})] \quad (3.14)$$

Based on the derivation in the appendix, it is seen that K_4 and K_2 are temperature-dependent constants. This has implications on electrothermal modelling of GaN HEMTs which are not explored in this paper. (3.14) is the i-v equation for the moderate inversion regime of the GaN HEMT. Strictly speaking, expressions for both the weak and strong inversion regimes must be derived through a similar process to get the full static characteristics. In order to model the weak inversion regime and ensure a smooth transition in between both the weak and moderate inversion regions, another factor is introduced as shown in (3.15). (3.15) is a concave up equation. Its curvature is adjusted by fitting parameters, α_I and V_{gs1} . V_{gs1} is the

gate-source voltage at which the device transits from weak inversion to moderate inversion.

$$K_5 = \frac{\exp(\alpha_1(V_{gs} - V_{th})) - 1}{\exp(\alpha_1(V_{gs1} - V_{th})) - 1} \quad (3.15)$$

In addition, it has been observed in experiments for the turn-on of the device that the gate-source voltage curves upward during the fall of the drain voltage. In order to capture this characteristic, an additional fitting parameter, α_2 , is used to modify (3.14). Hence, the complete i-v characteristic equation used for the model in this paper is written as seen in (3.16). (3.16) is used to model the equations for sources b1 and b2.

$$I_{ds} = \begin{cases} 0, & V_{gs} < V_{th} \\ K_5 K_4 \left[\exp(K_2(V_{gs} - V_{th})) \right] [1 - \exp(-\alpha_2 K_2 V_{ds})], & V_{th} \leq V_{gs} < V_{gs1} \\ K_4 \left[\exp(K_2(V_{gs} - V_{th})) \right] [1 - \exp(-\alpha_2 K_2 V_{ds})], & V_{gs1} \leq V_{gs} \end{cases} \quad (3.16)$$

Unlike a MOSFET, the HEMT does not physically possess a body diode. However, during dead-time of a half-bridge, the load current can still freewheel through the HEMT in the reverse direction as if the device actually possesses one. When in this mode of operation, the device may thought of as HEMT working in the reverse direction with V_{gd} taking the role of V_{gs} as the gate signal. Hence, (3.16) can be modified to model the behaviour of the device when the current is freewheeling through it in the reverse direction during dead-time using (3.17). This equation has been used to describe b3. (3.17) suggests that the “body diode” of the GaN HEMT is affected by the applied gate-voltage. This observation is corroborated by [148, 149] where this aspect has been exploited to improve the reverse conduction losses of GaN HEMTs.

$$I_{sd} = \begin{cases} 0, & V_{gd} < V_{th} \\ K_5 K_4 \left[\exp(K_2(V_{gd} - V_{th})) \right] [1 - \exp(-\alpha_2 K_2 V_{sd})], & V_{th} \leq V_{gd} < V_{gs1} \\ K_4 \left[\exp(K_2(V_{gd} - V_{th})) \right] [1 - \exp(-\alpha_2 K_2 V_{sd})], & V_{gs1} \leq V_{gd} \end{cases} \quad (3.17)$$

b4 is modelled using a form similar to the typical Shockley equation. The governing equation for b4 is seen in (3.18). Leakage current is modelled using (3.18) and as seen in datasheets [60], the leakage current is typically significantly higher compared

with silicon MOSFETs. This gate leakage current is sensitive to temperature and hence has implications on electrothermal modelling.

$$I_{gs} = I_g(\exp(k_{gs}V_{gs}) - 1) \quad (3.18)$$

3.5: Modelling of device charges and capacitances

C_{gs} is extracted from gate charge plots and modelled as a constant capacitance whereas C_{gd} and C_{ds} are modelled using sigmoid functions. C_{gd} and C_{ds} are described using (3.19) to (3.21).

$$C_{gd}(V_{gd}) = \frac{a_1}{1 + e^{(-b_1(V_{gd} + c_1))}} + d_1 \quad (3.19)$$

$$C_{oss}(V_{sd}) = \frac{a_2}{1 + e^{(-b_2(V_{sd} + c_2))}} + d_2 \quad (3.20)$$

$$C_{ds}(V_{sd}) = C_{oss}(V_{sd}) - C_{gd}(V_{sd}) \quad (3.21)$$

Fitting parameters a_1 , b_1 , c_1 , d_1 , a_2 , b_2 , c_2 and d_2 can be used to adjust the shape of the functions. In order to match the behavior of the C_{gd} capacitance in the model with the miller capacitance of the actual device, graphs of miller charge, Q_{gd} , plotted against V_{gd} must be obtained experimentally and fitted based on the integral of (3.19). This integral is shown in (3.22).

$$Q_{gd}(V_{gd}) = \frac{a_1}{b_1} \ln(1 + e^{b_1(x + c_1)}) + d_1x + k_1 \quad (3.22)$$

k_1 is a constant offset resulting from the integration that does not influence the behavior of the capacitances in the model. It can be adjusted to fit the simulated and experimental $Q_{gd} - V_{gd}$ curves. C_{ds} is determined by first fitting (3.20) to datasheet values of C_{oss} and then using (3.22).

3.6: Parameter extraction procedure

The switching behaviour of the power transistor is influenced by both the semiconductor as well as the parasitics of the gate driver loop and the commutation loop. When a high gate resistance is used in the gate driver circuit, the switching speed can be limited such that effects caused by the parasitics such as the ringing and the current and voltage overshoots are no longer present. Under such slow-switching conditions, the switching behaviour and consequently, the switching

waveforms, will be predominated by the semiconductor. This allows for easier extraction of device parameters like miller plateau voltage and gate charge. An added benefit of using observed slow-switching waveforms to extract these parameters is that errors arising due to bandwidth of the measurement are significantly reduced. Hence, the extracted waveforms are more accurate and suitable for parameter extraction and experimental verification.

The double pulse tester shown in Figure 3.5(b) was used for extracting the waveforms under slow-switching conditions. The double pulse tester module portion depicted in Figure 3.5(b) is a tester that was designed by a commercial company to test 600V through-hole devices. In order to make this portion more suitable for testing GaN switches, the module of Figure 3.6 was designed by the candidate. The module aims to better emulate the conditions experienced by GaN switches in a practical circuit by incorporating a layout that more closely resembles that of a practical GaN half-bridge and using an LM5113 gate driver which is the typical gate driver used to drive the GaN HEMT used in this work. The gate resistance used was set to $1\text{k}\Omega$ to limit the switching speed.

(a) Double pulse tester schematic

(b) Double pulse tester

Figure 3.5: Double pulse tester and schematic

Figure 3.6: GaN double pulse tester module

3.6.1: I-V Characteristics

Figure 3.8 was obtained by the candidate using the setup of Figure 3.5. The driver circuitry was modified into that of a constant current gate drive such as the one in

[150] which is used for obtaining gate charge plots. The schematic of the gate driver is seen in Figure 3.7. In order to ensure slow-switching during turn-on and turn-off, a current regulator diode with a small current rating of 0.5mA was selected along with a 1k Ω resistor, R_g . In Table 3.1, the key components of the gate driver are listed. The graph was obtained under the following conditions in Table 3.2. Gate current is measured by measuring the voltage across R_g .

Figure 3.7: Gate driver used for parameter extraction under slow-switching conditions

Table 3.1: Components of constant current gate driver

Component	Model
Gate driver IC	IR2110
Diode, D	1N4148
Resistor, R_g	1k Ω through-hole
Current regulator diode	E501

Table 3.2: Experimental conditions for obtaining Figure 3.8

Parameter	Value
Applied DC voltage	90V
Applied inductor current	25A
Positive rail voltage of gate driver	5V
Negative rail voltage of gate driver	-4V
Temperature	25°C

During the miller plateau period, the device is in saturation. While in the saturation regime, the device current is expected to be constant at its saturation current, I_{sat} , over a large range of drain-to-source voltage. While in this regime, the device's gate-to-source voltage will be clamped at the corresponding miller voltage, V_m . Miller voltage and the corresponding saturation current can therefore be read from slow-switching waveforms like those seen in Figure 3.8. For large V_{ds} values, (3.14) can be approximated as (3.23) so that K_2 and K_4 can be easily extracted using two pairs of values for V_m and I_{sat} . V_{th} is extracted from the datasheet of the device. After

extracting K_4 and K_2 , the remaining fitting parameters, α_1 , α_2 and V_{gs1} are tuned in SPICE.

$$I_{ds} = K_4 \left[\exp \left(K_2 (V_{gs} - V_{th}) \right) \right] \quad (3.23)$$

Figure 3.8: Slow-switching waveforms

3.6.2: Device capacitances

In order to parameterize the device capacitances, the miller charge, Q_{gd} , must be found. By measuring the gate current during the miller plateau period as depicted in Figure 3.8, the total gate charge that enters the gate during this period, Q_m , can be found using MATLAB scripts. Unlike silicon MOSFETs, GaN HEMTs have a significantly higher gate leakage current that can be modelled using source b4. The amount of leakage charge, Q_{leak} , must be subtracted from Q_m in order to obtain Q_{gd} as seen in (3.24).

$$Q_{gd} = Q_m - Q_{leak} \quad (3.24)$$

Q_{leak} can only be accurately found if b4 is modelled correctly. Hence, (3.18) is fitted to the extracted values of the data sheet first as seen in Figure 3.9. Since voltage is constant during the miller plateau period, it can be assumed that the leakage current is roughly constant for that interval. Hence, Q_{gd} can be more easily found and plotted against V_{gd} and fitted using (3.22) as seen in Figure 3.10. C_{oss} c-v curves are also extracted from the datasheet and fitted using (3.20) as seen in Figure 3.11. The parameters of the GaN HEMT model used in this work can be summarised in Table 3.3. The accuracy of the model is verified in Chapter 5.

Figure 3.9: Modelling of gate leakage current

Figure 3.10: Plot of charges vs V_{gd}

Figure 3.11: Plot of C_{sd} vs V_{sd} with curve fitting

Table 3.3: Consolidated parameters of chosen model

Parameter	Value	Units
K_2	2.28	V^{-1}
K_4	8.96	A^{-1}
V_{th}	1.4	V
V_{gs1}	3	V
α_1	0.01	V^{-1}
α_2	0.1	V^{-1}
I_b	0.2	A
k_b	2	V^{-1}
I_g	1.76×10^{-12}	A
k_{gs}	3.76	V^{-1}
a_1	0.72×10^{-9}	F
b_1	0.3	V^{-1}
c_1	0	V
d_1	0.015×10^{-9}	F
a_2	1×10^{-9}	F
b_2	0.3	V^{-1}
c_2	10	V
d_2	0.4×10^{-9}	F
C_{gs}	0.9×10^{-9}	F

3.7: Simulation circuits for verification

The double pulse tester module of Figure 3.6 can be simulated in LTSPICE for both slow and fast-switching conditions. Experimental results extracted from this GaN module can then be compared against simulation. Under slow-switching conditions, the parasitic inductances of the module can be neglected and the circuit of Figure 3.12 can be used to simulate the module. Under fast-switching conditions, the parasitic inductances must be included and the circuit of Figure 3.13 can be used to simulate the module.

The model was simulated in LTSPICE under both slow switching and fast switching conditions in order to verify its performance under both conditions. The results of this verification are presented in Chapter 5. Under slow switching conditions, the circuit of Figure 3.12 is used to simulate the power transistor. I_{load} and V_s are used to adjust the applied voltage and current for the turn-on or turn-off of the switch. For Figure 3.12, all diodes used are assumed to be ideal and the internal resistances of the gate driver were calculated using datasheet values. V_{drive} is a pulsed signal used to control the turn-on and turn-off of the switch. Under fast switching conditions, parasitic inductances in the circuit must be considered. Hence the circuit of Figure 3.13 is used to simulate the power transistor's behaviour under such conditions.

Figure 3.12: Simulated circuit for slow switching condition

Figure 3.13: Simulation circuit for fast switching conditions

The parasitic inductances of each various components have to be approximated. For the MLCC capacitors, the frequency response resembles that of a notch filter. Hence the equivalent series circuit can be found by examining the magnitude and frequency of the impedance at resonant frequency. The equivalent series resistance, ESR_l , has the same magnitude as that of the impedance at resonant frequency. The equivalent series inductance, ESL_l , can be calculated by using (3.25) where ω_{res} is the angular frequency at which resonance occurs and C_l is the rated capacitance. For the electrolytic capacitors, ESR_2 was calculated using (3.26) where $\tan \delta$ is the loss tangent found in the datasheet and X_c is the reactance at the rated frequency of the capacitor. ESL_2 is estimated. For the gate resistors, the parasitic inductance is approximated as 1 nH. The shunt resistor's parasitic inductance, L_{sh} , is measured using an impedance analyser. The parasitic inductance of the remaining printed circuit board (PCB) track, L_{trace} , is approximated based on the frequency of observed oscillations in the experiment and can be regarded as a fitting parameter. The package inductance of the GaN HEMTs were read from an application note [151] and it was assumed that it is distributed evenly among the drain and source contacts. The consolidated simulation parameters are seen in Table 3.4.

$$ESL_1 = \frac{1}{\omega_{res}^2 C_1} \quad (3.25)$$

$$ESR_2 = X_c \tan \delta \quad (3.26)$$

Table 3.4: Simulation parameters for slow and fast-switching conditions

Slow switching conditions		
Simulation parameters	Value	Units
R_{on}	4.2	Ω
R_{off}	1	Ω
Shunt resistance	0.1	Ω
R_g	1000	Ω
Fast switching conditions		
Simulation parameters	Value	Units
R_{on}	4.2	Ω
R_{off}	1	Ω
R_{g_l}	5.1	Ω
L_{g_l}	1	nH
L_{d_l}	0.2	nH
L_{s_l}	0.8	nH
Shunt resistance	0.1	Ω
L_{sh}	4	nH
L_{trace}	5.4	nH
L_{load}	2.5	mH
R_{g_u}	6.1	Ω
L_{g_u}	1	nH
L_{d_u}	0.2	nH
L_{s_u}	0.2	nH
ESL_1	1	nH
ESR_1	0.1	Ω
$C1$	4.7	μF
ESL_2	20	nH
ESR_2	6	Ω
$C2$	47	μF

3.8: Modelling effect of temperature on GaN HEMT

transconductance for small signal applications

In the proposed GaN model, an expression for the i-v characteristic was derived based on the assumption that the transistor mainly transits through the moderate inversion regime during switching. Based on (3.14), an expression can be derived for the transconductance, g_m , which is a crucial parameter for small signal applications where the transistor operates in the linear mode. g_m is not as crucial for power electronics applications where the switch operates in switch-mode and was hence not considered in the proposed model. However, the effect of temperature on g_m is of great interest to those working in the RF field since this parameter influences

the gain of linear-mode amplifiers. This interest is evident in several papers [152, 153, 154, 155] and hence, an expression relating g_m to temperature is derived from (3.14) and presented here should there be a need for it in future work.

Starting from (3.14), its partial derivative can be taken with respect to V_{ds} to yield (3.27) which is an expression for transconductance. In (3.27), K_2 and K_4 are temperature-dependent parameters. By taking the partial derivative of (3.27) with respect to T , (3.28) can be derived. The expressions for the partial derivatives of K_2 and K_4 can be found in A8 and A9 of the appendix. (3.28) requires prior knowledge of the device parameters to be used effectively and is hence not suitable for circuit design. However, it can help device designers to better minimise the effect of temperature on the gain of an amplifier realised from GaN HEMTs.

$$g_m = \frac{\partial I_{ds}}{\partial V_{ds}} = K_2 K_4 \exp(K_2(V_{gs} - V_{th})) \exp(-K_2 V_{ds}) \quad (3.27)$$

$$\begin{aligned} \frac{\partial g_m}{\partial T} = \exp(K_2(V_{gs} - V_{th})) \exp(-K_2 V_{ds}) & \left[\frac{\partial K_2}{\partial T} K_4 + K_2 \frac{\partial K_4}{\partial T} \right. \\ & \left. + K_2 K_4 (V_{gs} - V_{th}) \frac{\partial K_2}{\partial T} - K_2 K_4 \frac{\partial K_2}{\partial T} V_{ds} \right] \end{aligned} \quad (3.28)$$

3.9: Chapter summary

In this chapter, the i-v characteristics and capacitances of a GaN HEMT have been modelled. The equations of the model may be inputted into LTSPICE and any other variants of SPICE such as PSPICE, HSPICE and CoolSPICE for simulation. The i-v characteristics of the GaN HEMT while it is in forward conduction were derived starting with a charge-sheet expression that takes into account the effect of piezoelectric polarisation. The equation for the forward i-v characteristics were then extended to model the reverse i-v characteristics of the GaN HEMT. The resulting reverse i-v characteristic equation also captures the fact that the reverse-conduction behaviour of the GaN HEMT is dependent on the applied gate-bias. The simulation method for a half-bridge realised using GaN HEMTs has also been outlined. The simulation circuits for slow-switching and fast-switching conditions have been presented along with their respective simulation parameters. These circuits will be used as part of verification in Chapter 5 and can be employed by other researchers in future works.

CHAPTER 4 : A STUDY OF TRADE-OFF IN BETWEEN PARASITIC INDUCTANCE AND THERMAL RESISTANCE

4.1: Chapter overview

It is desirable to design a converter with low parasitic inductances so that it can run more efficiently and be at less risk of failure due to voltage overshoot. It is also desirable to incorporate thermal paths with low thermal resistances so that the semiconductor components can stay cool. It is commonly known amongst engineers that there exists a trade-off in between the parasitic inductances and thermal resistances of a power converter. In general, minimisation of parasitic inductances is achieved by placing components closer to each other or by using smaller components. However, it is also generally true that in order to minimise thermal resistances, one should space out the components and use larger components. The same holds true for GaN HEMTs. Authors [156, 24, 157] often focus on minimisation of parasitic inductances to reduce voltage overshoot and power losses. However, little attention has been given to assessing the trade-off in between the parasitic inductances and thermal resistances in the design of GaN HEMTs. In some instances, authors [156] trade off thermal dissipation capability entirely in favour of minimising parasitic inductance which result in circuit layouts that are unsuitable for use in a practical converter.

In this chapter, the theory behind parasitic inductances and heat sinks is reviewed. The trade-off in between minimisation of inductances and heatsink volume is illustrated using four PCB layout designs for a 250W, 48V to 12V buck converter operating at a switching frequency of 600 kHz.

4.2: Parasitic inductances

For the commutation and gate driver loops, authors [24, 4, 97] typically route the forward and return paths of the loops close to each other to form differential pairs and reduce the parasitic inductance. The trace widths of the forward and return paths are also enlarged to further reduce the parasitic inductance. Therefore, in order to gain a qualitative understanding of how geometric parameters affect the parasitic inductances, the forward and return paths of the commutation loop can be approximated as broadside coupled traces. The inductances of both loops has been approximated with (2.42) and is presented again in (4.1) for easy reference. μ_0 is

permeability of free space, μ_r is relative permeability, l_{PCB} is the length of the trace, t_{PCB} is the thickness of the dielectric in between the traces and w_{PCB} is the width of the trace.

$$L = \frac{\mu_0 \mu_r l_{PCB} t_{PCB}}{w_{PCB}}, \quad w_{PCB} \gg t_{PCB} \quad (4.1)$$

Figure 4.1: Broadside coupled traces

As seen by (4.1), the inductance is linearly proportional to the area in between the forward and return paths as depicted in Figure 4.1. This observation is supported by [24] where the high frequency commutation loop inductance for a vertical layout was simulated and it was found that the relation in between the inductance of the commutation loop and the thickness of the PCB was highly linear. (4.1) also suggests that the inductance is inversely proportional to the width of the trace, indicating that wider traces are good for reducing parasitics.

4.3: Heat sinks

There are three mechanisms involved in the dissipation of heat. These are conduction, convection and radiation. Conduction is the primary heat transfer mechanism involved in between the junction of the switch to the base plate of the heatsink. Heat is then transferred to the ambient air primarily through convection and radiation. For forced-cooled designs, convection will predominate over radiation. The thermal resistances for a typical power electronics assembly is shown in Figure 4.2 (a).

(a) Typical power electronics assembly

(b) Thermal resistance circuit

Figure 4.2: Typical power electronics assembly with thermal resistance circuit

As seen in Figure 4.2 (b), thermal resistances, R_{jb} , R_{hs_conv} and R_{hs_rad} represent the junction-to-base plate thermal resistance as well as the thermal resistances for the convection and radiation paths respectively. The primary mechanism behind R_{jb} is conduction. Hence, R_{jb} can be described using (4.2) where l_{jb} is the effective length of the thermal path from junction to the base-plate, A_{jb} is the effective cross sectional area of the thermal path and σ_t is the thermal conductivity of the materials in between.

$$R_{jb} = \frac{l_{jb}}{\sigma_t A_{jb}} \quad (4.2)$$

R_{hs_conv} is related to the effective area available for convection, A_c , and the heat transfer coefficient, h , as depicted in (4.3). h is dependent on various fluid-related parameters like the flow rate, viscosity and thermal conductivity.

$$R_{hs_conv} = \frac{1}{h A_c} \quad (4.3)$$

R_{hs_rad} is related to the geometrical parameters of the heat sink as depicted in (4.4) where A_{rad} is the effective area available for radiation, ϵ_{hs} is the emissivity of the heatsink, σ_b is the stefan-boltzmann constant. T_s and T_a are the surface temperature and ambient temperature of the heatsink respectively.

$$R_{hs_rad} = \frac{\Delta T}{\epsilon_{hs} A_{rad} \sigma_b (T_s^4 - T_a^4)} \quad (4.4)$$

As seen by (4.3) and (4.4), the thermal resistance of the heatsink improves with greater exposed area. Consequently, this means that a larger heatsink is required for a lower thermal resistance.

The overall thermal resistance of the thermal path is also affected by the position of the heat source on the heatsink. In order to illustrate this, the setup of Figure 4.3 was simulated in ANSYS ICE-pak with a pair of heat sources to simulate the switches in contact with the heatsink. Heat sources positioned closer to the centre of the heatsink will experience a lower thermal resistance than the same heat source at the side of a heatsink as illustrated in Figure 4.4. This is caused by the increased spreading resistance of the heat source when it is at the edge of the heatsink.

Figure 4.3: Simulated thermal dissipation system

Figure 4.4: Thermal simulations for examination of effect of heat source position on temperature

4.4: Examination methodology

For typical GaN HEMTs, surface mounted components are typically used to minimise the parasitics associated with the package. Hence, GaN HEMTs can either be top-cooled or bottom cooled. The cross sections of a converter for both cases of top-cooled and bottom-cooled GaN HEMTs is presented in Figure 4.5. For a top-cooled converter, heat is conducted from the switch junction to the heatsink and then dissipated into the ambient air through convection and radiation. For the case of a bottom-cooled converter, the heat must first be conducted through thermal vias in the PCB and then dissipated into the air through the heatsink. In between the two designs, it can be seen that for the case of a top-cooled converter, the heat takes a more direct path into the ambient air. Hence, for surface-mounted GaN HEMTs, it is expected that the top-cooled design will possess a lower overall thermal resistance. Therefore, this work focuses on layouts which incorporate top-cooled switches.

Figure 4.5: Cross sections of top-cooled and bottom-cooled GaN converter

In order to examine the trade-off in between parasitics on the board and thermal resistance of the heat sink, three reference designs were considered for the half-bridge of a 48V to 12 V buck converter as depicted in Figure 4.6. The output power of this theoretical converter is assumed to be 250W and operating frequency is assumed to be 600 kHz. The converter is hard-switched. Under such conditions, switching losses are expected to make up most of the losses in the semiconductor.

Figure 4.6: Schematic and waveforms of bidirectional buck converter

The buck converter is designed to have a peak-to-peak current ripple that is twenty percent of the load current as seen in Figure 4.6 (b). At time $t = 0$, the top switch of the buck converter turns on and the body diode of the half-bridge turns off. The total switching energy of the half-bridge at this instant of time hence consists of the turn-on energy of the top switch, E_{on-T} , and the turn-off energy of the lower body diode, E_{off-bd} . At time $t = t_1$ the top switch of the buck converter turns off and the body diode of the half-bridge turns on. The total switching energy of the half-bridge at this instant of time hence consists of the turn-off energy of the top switch, E_{off-T} , and the turn-on energy of the bottom diode, E_{on-bd} . Since switching frequency is high, it is assumed that conduction loss is relatively small. Total power loss dissipated across the semiconductors, P_{sw} , can therefore be expressed as shown in (4.5) where f_{sw} is the switching frequency.

$$P_{sw} = (E_{on-T} + E_{off-bd} + E_{off-T} + E_{on-bd})f_{sw} \quad (4.5)$$

As mentioned in section 4.2, the presence of parasitic inductances can affect the values of E_{on-T} , E_{off-bd} , E_{off-T} and E_{on-bd} . A simulation was done in LTSPICE using the model from Chapter 3 to extract these values under varying values of commutation and gate loop inductance. The circuit of Figure 3.13 was modified for modelling the parasitic inductances in the half-bridge. In Figure 4.7, this circuit is presented to highlight the critical inductances involved in the simulation. The energy values for E_{on-T} , E_{off-bd} and E_{off-T} are found by integrating power with respect to time from when the time starts rising above ten percent peak power to the time it falls below ten percent peak power. For the case of E_{on-bd} , the value is negative as the device's capacitance is being discharged during that instant. Hence integration starts when power falls below ten percent of the minimum point and stops when power rises above ten percent of the minimum point.

Figure 4.7: Simulated half-bridge with parasitic inductances

As MLCC capacitors typically possess lower impedance at higher frequencies compared with electrolytic capacitors, it is assumed that the majority of the commutation current is supplied by the MLCC capacitor bank. The number of MLCC capacitors in this bank is adjusted based on the design of the half-bridge. In this work, six MLCC capacitors were used. Hence, ESL_1 , the equivalent series inductance of the MLCC capacitor is involved in the commutation loop. L_{d_u} , L_{s_u} , L_{d_l} and L_{s_l} are package inductances associated with the switches. L_{trace} and R_{trace} are the lumped parasitic inductance and resistance of the copper trace respectively.

In order to obtain the parasitic inductances, the gate driver loops and commutation loops were approximated as microstrip structures and simulated in ANSYS Q3D. The structure used for the simulation is described in Figure 4.8. The parameters for

copper thickness, t_c , width of the forward conduction path, w_1 , width of the return conduction path, w_2 , thickness of the enclosed dielectric, t_d and length of the enclosed dielectric, l_d . In practical circuits, the return path consists of a large ground plane. Hence w_2 is made large relative to w_1 . Copper thickness is typically fixed at $70\ \mu\text{m}$ for high power boards. Hence t_c is fixed at $70\ \mu\text{m}$. w_1 represents the trace-width of the forward path of the commutation or gate driver currents and is hence allowed to vary. PCBs also come with many thicknesses and in multi-layer boards, the thickness of the dielectric layer in between copper layers is variable. Hence, t_d is also allowed to vary. l_d is also allowed to vary as distances in between components are typically adjusted in PCBs to accomodate components of varying sizes.

Figure 4.8: Simulated microstrip structure in ANSYS

A parametric sweep of w_1 , t_d and l_d was done to examine the effect of these three parameters on the loop inductance under dc conditions, L_{loop_DC} . The graph for each sweep was consolidated in Figure 4.9. It is seen that loop inductance decreases with respect to increasing w_1 in an inversely proportional manner. It is also seen that the loop inductance increases linearly with increasing t_d and l_d . This behaviour is consistent with (4.1).

Figure 4.9: Effect of w_l , l_d and t_d on loop inductance

The layout of a typical PCB showing the position of the gate driver, gate resistor, power transistor and bus capacitors is depicted in Figure 4.10. In order to examine the trade-off in between the parasitic inductances of the circuit and thermal resistance of the thermal paths, three layouts are designed and considered. The cross sections of their gate driver loops and commutation loops are presented in Figure 4.11 and Figure 4.12.

Figure 4.10: Layout of a typical PCB involving GaN transistors

The design rationale of the three designs are touched upon next. Design 1 was created with the intent of minimising both the gate loop and commutation loop inductances without any regard for thermal design. The layout of this board is based on the optimal power loop proposed in [24]. As seen by Figure 4.11(a), the area enclosed by the commutation current loop is very small compared with the other three designs. Hence this design is expected to possess the least parasitic inductance in both the gate driver and commutation loops. This design has been recommended to reduce voltage overshoots and improve efficiency. However, it can be seen that due to the relatively high profile of the bus capacitors, the heatsink cannot be centred over the switches. In fact, the switches are positioned close to the edge of the heatsink where the thermal resistance leading to ambient air is higher.

Using design 1 as the reference, design 2 was created with the intent of shifting the switches closer to the centre of the heatsink to improve thermal dissipation capability. However, the expected trade-off of this design relative to design 1 is that the voltage overshoot of the design will be higher and that more turn-off losses will be incurred in the power transistors as a result of increased parasitic inductance. In this study, the capacitors of design 2 have been placed about 7.6 mm further away from the switches compared with design 1.

The third design is a two-layer variant of design 1. This design is expected to be less costly and easier to manufacture compared with design 1 due to the reduced number of layers. However, the size of both current loops has been increased significantly. In addition, the switches in this design are also positioned very close to the edge of the heatsink. Hence, in terms of electrical and thermal performance, design 3 is expected to exhibit the highest power loss and the highest temperature rise.

Figure 4.11: Commutation loops of four designs

Figure 4.12: Cross section of gate driver loops

It can be seen in Figure 4.11 and Figure 4.12 that the current loops formed are highly rectangular. Hence, the microstrip structure of Figure 4.8 (a) can be used to approximate these structures and extract the parasitic inductances. In Table 4.1, the values of t_c , t_d , l_d , w_1 and w_2 used to model and extract the parasitic inductances are shown along with the corresponding values of high frequency inductance for each loop. The range of frequencies used for the AC inductance was 50 MHz to 1GHz. It was observed that for this range, the AC inductance was roughly constant.

Table 4.1: Consolidated geometrical parameters and inductances

Loop	Geometrical parameters					AC Inductance/nH
	t_c /mils	t_d /mils	l_d /mils	w_l /mils	w_2 /mils	
Design 1 commutation loop	2.8	4	400	130	400	0.43
Design 2 commutation loop	2.8	4	700	130	400	0.67
Design 3 commutation loop	2.8	62	400	130	400	3.40
Gate driver loop for designs 1 and 2	2.8	4	122	26	400	0.43
Gate driver loop of design 3	2.8	62	122	26	400	2.74

The values of parasitic inductances were then used in conjunction with the simulation of the circuit of Figure 4.7 to obtain the power losses of the semiconductors. The gate driver loop inductances were used for the inductance value of $L_{g,l}$. For the commutation loop, it was assumed that the loop inductance was evenly distributed over $L_{d,u}$, $L_{s,u}$, $L_{d,l}$, $L_{s,l}$ and the equivalent series inductances of the six MLCC capacitors. Hence, the commutation loop inductance was simulated by distributing the value over $L_{d,u}$, $L_{s,u}$, $L_{d,l}$, $L_{s,l}$ and ESL_l according to (4.6).

$$L_{d,u} = L_{s,u} = L_{d,l} = L_{s,l} = \frac{ESL_l}{6} = \frac{L_{com}}{5} \quad (4.6)$$

For the heatsink, a junction temperature of 60°C was chosen as the target temperature for thermal design. The heatsink and fan of Figure 4.3 was used for the thermal design. The height of the fins was allowed to vary until the target temperature was met. The fixed parameters of the thermal simulation are listed in Table 4.2. The final box volume of the heatsink was then recorded along with the power losses in the next section.

Table 4.2: Fixed parameters for thermal simulation

Parameter	Value	Units
Heatsink length	59	mm
Heatsink width	37	mm
Base plate thickness	2	mm
Fan radius	20	mm
Fan hub radius	10	mm
Fan flow rate	5	cfm

4.5: Simulation Results

The simulation software used to extract the parasitic inductances was ANSYS Q3D extractor. The circuit simulator used was LTSPICE version IV. The simulation software used for thermal simulation is ANSYS ICE-Pak version 15. The parasitic inductances of the gate driver and commutation loops of each design are first extracted using ANSYS. The commutation loop inductance value is then distributed over the respective inductances in Figure 4.7 using (4.6). The switching energies are obtained by simulating the circuit of Figure 4.7 in LTSPICE. It should be noted that the values of E_{on-bd} are negative because the capacitance of the switch is discharging as the switch transits into a reverse conducting state.

The semiconductor losses are then calculated using (4.5) and then used as the heat sources in the ANSYS ICE-Pak simulation. As mentioned in section 4.4, a maximum allowable junction temperature of 60°C was used for the switches. The height of the fins of the heatsink was adjusted until the temperature of the switches were close to this value before the results were recorded in Table 4.3.

The simulated switching energies, power loss, heatsink volume, heatsink fin height, parasitic inductances and gate resistance for each design were consolidated in Table 4.3. The results are analysed using design 1 as a benchmark.

Designs 1 and 2 are compared. Design 2 possesses a higher commutation inductance. Hence, a lower value is expected for E_{on-T} for design 2 and this expectation is corroborated by Table 4.3. A higher commutation inductance also increases turn-off losses of switches. This is corroborated by the E_{off-T} and E_{off-bd} values in Table 4.3. Overall, switching losses for design 2 are expected to be slightly higher than those

of design 1. As the switches are more centred on the heat sink compared with design 1, it is expected that the junction-to-baseplate thermal resistance is lower compared with that of design 1. This potentially allows the designer to incorporate a higher baseplate-to-ambient thermal resistance and hence a smaller heatsink if the power loss is small enough. For the case depicted in Table 4.3, the potential reduction in heatsink volume was offset by the increase in losses.

Design 3 is considered next. This two layer design has a higher commutation inductance relative to designs 2 and 1 and also a higher gate loop inductance relative to the other two designs. Hence, it is expected that this design exhibits the highest losses of the three. This is again supported by Table 4.3. As the switches are positioned at the same location on the heat sink as design 1, it is expected that a larger heat-sink will be required to maintain the same temperature rise.

Table 4.3: Consolidated results and parameters for designs

Quantity	Design 1	Design 2	Design 3
$E_{on-T} / \mu\text{J}$	6.20	5.88	4.46
$E_{off-T} / \mu\text{J}$	2.27	2.33	2.85
$E_{on-bd} / \mu\text{J}$	-0.48	-0.44	-0.35
$E_{off-bd} / \mu\text{J}$	5.94	7.42	8.92
Power loss/W	8.36	9.11	9.53
L_{com}/nH	0.43	0.69	3.4
L_{gate}/nH	0.43	0.43	2.74
R_{gate}/Ω	5.1	5.1	5.1
Heatsink fin height/mm	14	14.5	16
Heatsink box volume/ml	34.9	36.0	39.3

Based on the listed results in Table 4.3, it is seen that in terms of power loss and heatsink volume, design 1 is the best of all the designs. Design 3 still has the cheapest PCB but exhibits the most losses and requires the largest heatsink to cool. It is seen from design 2 that increasing the distance in between the capacitors and the switches caused the overall losses to increase but as the switches were centred on the heatsink and their losses were not as high as those of design 3, the increase in heatsink volume was not as drastic compared with design 3.

It can be seen that the required heatsink volume increases with a PCB layout that incorporates a higher amount of PCB inductance. Hence, the results suggest that if a small volume is desired, it is not worthwhile to increase parasitic inductance to reduce the spreading resistance. However, it can be seen by comparing designs 1 and 3 that reducing the number of layers from four to two only results in an increase of 2 mm of heatsink fin height. This suggests that cost-wise, it is better to employ a two-layer design than a four-layer design.

4.6: Experimental verification of effect of PCB layout on power losses

In order to experimentally verify the effect of inductances in the PCB on the total power loss of the half-bridge, designs 1, 2 and 3 were realised and tested using the first part of the opposition method detailed in Chapter 5. It is expected that design 1 will exhibit the least switching losses followed by design 2 and then design 3. Two half-bridges of each design were tested using the configuration depicted in Figure 4.13. By setting the voltage of the power supply and the dc component of the inductor current, i_L , the switching conditions experienced by the switches in the half-bridge may be controlled. The ripple component of i_L is minimised through modulation so that the dependence of the inductor loss on switching frequency is minimised. A graph of power loss may then be plotted against switching frequency so that the total switching energy dissipated by the half-bridges may be read from the gradient.

Figure 4.13: Setup for testing power loss of half-bridges

Half-bridges for the three designs were tested with the voltage of the source set at 30V and the dc component of the inductor current set at 1A. The voltage and current was set low so as to prevent the half-bridges from overheating. The switching frequency of the half-bridges was varied from 350 kHz to 600 kHz in order to plot a graph of power loss against switching frequency. The hardware for the three different designs is depicted in Figure 4.14. The plot of power loss against frequency is depicted in Figure 4.15. The trend lines for the 3 designs are also depicted. As

expected, design 1 exhibits the lowest gradient, indicating that it has the least switching losses. This is followed by design 2 and then design 3.

Figure 4.14: Half-bridge hardware

Figure 4.15: Plot of power loss vs switching frequency for 3 designs

4.7: Possible 2-sided PCB designs

Up to now, singled-sided PCB designs were discussed due to the fact that these PCBs were easier to assemble and hence less prone to reliability issues. However, a possible set of two-sided PCB designs that can be explored in future is depicted in Figure 4.16. Unlike one-sided designs, two-sided designs allow the designer to put all the high profile components like capacitors and inductors on one side and the low-profile components on the other. Hence the switches can be centred perfectly on the heatsink. However the commutation loop inductance of the design is increased as enclosed area of the loop is larger.

A 4 layer design allows the designer to incorporate the gate driver loop of Figure 4.12 (a) which possesses a lower inductance but at the expense of a higher cost but

a 2 layer design allows the designer to design at a lower cost but at the expense of a higher gate loop inductance caused by the gate driver loop of Figure 4.12 (b). The designer may also choose to experiment with the thickness of the PCB of Figure 4.16 (b) to reduce the inductances of the PCB while simultaneously reducing costs. These designs could be potentially explored in a future work.

Figure 4.16: 2-sided designs

4.8: Chapter summary

In this chapter, the basic theory behind parasitic inductances and thermal resistances of a half-bridge is reviewed. The impact of PCB parasitics and thermal resistance of thermal pathways on the design of a 48V/12V buck converter was examined. Three PCB designs were explored and the resulting power loss and required heatsink volume were examined. The three single-sided designs were realised and tested at low power loss levels to check whether they exhibited the power losses in the right order. It was also found that volume-wise, it is not worthwhile to increase parasitic inductance in return for lower thermal resistance. However, cost-wise, the converter design benefits from reducing the number of layers from four to two. The resulting increase in parasitic inductance and consequent increase in losses does not cause much change in the amount of material needed to construct the heatsink and hence the overall costs is expected to be lower. As mentioned before in section 2.3, the half-bridge can be seen as a building block for certain topologies. Hence the result is applicable to topologies such as dual-active bridges, two-level inverters and cascaded multi-level H-bridge inverters.

CHAPTER 5 : VERIFICATION

5.1: Chapter overview

In this chapter, the verification techniques employed for the power transistor model are discussed in detail. The extracted waveforms from the double pulse test for the case of slow switching are used to verify the accuracy of the model. As it is desirable to eventually use the model to predict switching losses in a practical converter, a suitable method must be used to extract the switching losses under more practical, fast switching conditions. In this chapter, a critical comparison between the double pulse test method and the opposition method for extracting the associated losses of a half-bridge converter realised using GaN HEMTs is also presented. Results from both methods are examined in terms of accuracy and compared with those predicted by the model. The opposition method was found to be better for extracting the switching losses predicted under practical conditions and hence it is used to verify the model under those conditions.

5.2: Critical comparison in between double pulse test method and opposition method for extraction of switching losses

In order to verify the accuracy of the model in terms of how well it predicts switching losses of GaN HEMTs under practical operating conditions, it is necessary to choose a method to properly extract the switching losses under these conditions. The double pulse test method is the typical method used for extracting switching losses. However, due to the fast switching speeds of the GaN HEMT under practical operating conditions and the limited bandwidth of present measurement equipment, inaccuracies are introduced in the switching energies which lead to an overestimate of the switching losses of GaN HEMTs under practical operating conditions. The inclusion of the current shunt in the commutation loop also increases the loop inductance of the commutation loop and hence, reduces the range of testable di/dt s. Due to the limits of the double pulse method, it is necessary to consider an alternative method for measuring the switching losses under practical operating conditions. As calorimetric methods are time-consuming and require much development effort, a suitable electrical method must be chosen instead. Amongst the electrical methods reviewed, the opposition method was chosen as an alternative to the double pulse test method for extracting switching losses. In the next few sections, the operating

principles of both methods and a comparison between them is performed for a set of predefined criterion.

5.2.1: Operating principles of the double pulse test and opposition methods

The double pulse test is an oscillographic method which typically involves the circuit in Figure 5.1. As seen in Figure 5.1, the inductor is pre-charged to a desired current level before the device under test (D.U.T.) is turned off. During the second gate pulse, the waveforms for hard turn-on and hard turn-off are observed at t_1 and t_2 respectively and from them, the switching energies of the transistor, E_{on-T} and E_{off-T} , can be calculated.

(a) Double pulse configuration for testing of switching energies of active switch

(b) Waveforms during test

Figure 5.1: Double pulse test method with waveforms

The double pulse tester can also be reconfigured to obtain the turn-on and turn-off energies, E_{on-bd} and E_{off-bd} , of the body diode of the complementary switch as shown in Figure 5.2. The forward recovery waveforms can be observed at t_1 whereas the reverse recovery waveforms can be observed at t_2 .

(a) Body diode test configuration

(b) Waveforms during test

Figure 5.2: Double pulse tester reconfigured to test body diode

The schematic for the double pulse tester used in this work is presented in Figure 5.3. As seen in Figure 5.3, the tester consists of two GaN HEMTs, T1 and T2. If the

turn and turn off energies of the GaN HEMT is desired, this can be done by connecting the inductor in between ports P1 and P2 and applying a gate signal to T1 while shorting out the gate of T2. By doing so, the schematic of Figure 5.3 effectively becomes that of Figure 5.1 (a). If the energy dissipated across the body diode of the device is desired, the inductor can be reconnected in between P2 and P3. The gate signal can then be applied to T2 while shorting out T1. In doing so, Figure 5.3 effectively becomes that of Figure 5.2 (a).

Figure 5.3: Schematic of double pulse tester used in this work

By extracting values of E_{on-T} , E_{off-T} , E_{on-bd} , E_{off-bd} corresponding to the operating points in a converter, the switching loss of the power devices can be computed. Using a typical boost converter as an example as seen in Figure 5.4, two sets of switch operating conditions are identified which occur at time t_l and t_h . The first corresponds to the low point of the inductor ripple and the second corresponds to the highest point of the inductor ripple. Therefore, in order to obtain the total switching losses, P_{sw} , the hard turn-on energy and reverse recovery energy corresponding to the lowest point of the current ripple, E_{on-Tl} and $E_{off-bdl}$, must be extracted along with E_{off-Th} and E_{on-bdh} which are the turn-off energy and the forward recovery energy of corresponding to the high point of the inductor current. Switching loss is then computed as seen in (5.1).

$$P_{sw} = (E_{on-tl} + E_{off-bdl} + E_{on-bdh} + E_{off-th}) f_{sw} \quad (5.1)$$

(a) Typical boost converter

(b) Waveforms for v_{ds} and i_L

Figure 5.4: Typical boost converter with waveforms

The opposition method involves the circuit of Figure 5.5 and is done in two parts. In the first part, the two half-bridges in the setup are operated in phase. The first half-bridge consists of T1 and T2 whilst the second half-bridge consists of T3 and T4. T1's duty ratio is fixed at fifty percent whilst T3's duty ratio is controlled through feedback. The test voltage and test current, I_{DC} , are set using the supply and the closed loop control of the inductor current.

Figure 5.5: Opposition method schematic

Figure 5.6: Waveforms for opposition method

The gate signals of the devices and the current waveform for the first part for one period, T_{sw} , are presented in Figure 5.6. During the time period from zero to t_1 , switches T1 and T4 are on and the inductor current ramps up. At time t_1 , T4 is switched off. This is followed by a dead-time before the gate signal of T3 is applied. During this dead-time, the body diode of T3 turns on and current freewheels through it. When the gate signal of T3 is applied, conduction of current shifts from the body diode of T3 to the channel of the device. During the time period from t_1 to t_2 , inductor current ramps down as the current circulates in the loop formed by T1, T3 and the inductor. Just before time t_2 , the gate signal of T3 is removed and this is followed by dead-time. During this dead-time the body diode of T3 conducts until time t_2 when the gate signal of T4 is applied. At this point, the body diode of T3 turns off and T4 experiences hard turn-on. In between time t_2 to t_3 , the inductor current ramps up again. At time t_3 , T1 is turned off and this is followed by a dead-time before the gate signal of T2 is applied. During this dead-time, the body diode of T2 turns on and current freewheels through it. Once the gate signal of T2 is applied, conduction of current shifts from the body diode of T2 to the channel of the device. From time t_2 to time t_4 , the inductor current ramps down as it circulates in the loop formed by T2, T4 and the inductor. Just before time t_4 , the gate signal of T2

is removed and this is again followed by a dead-time during which the body diode of T2 conducts. At time t_4 , T1 experiences hard turn-on and the body diode of T2 is turned off.

It can be seen that over the course of one period, switching energy is dissipated by T1 and T4 as well as the body diodes of T2 and T3. By plotting a graph of total power loss, P_t , against the switching frequency, f_{sw} , a linear relationship can be obtained if measures have been taken to sufficiently suppress frequency-dependent loss components other than those that occur in the power transistors. The gradient, m , of this graph represents the total switching energy dissipated by the semiconductor devices over one period of operation and is inclusive of E_{on-T} , E_{off-T} , E_{on-bd} and E_{off-bd} for one defined set of applied switch voltage and current. Due to the symmetry of operation, it is expected that the switching loss of each half-bridge will be the same. Hence, the total energy dissipated in one leg, E_l , over one switching period is half that of the gradient. Hence, m is related to E_l as written in (5.2).

$$m = 2E_l = 2(E_{on-T} + E_{off-bd} + E_{off-T} + E_{on-bd}) \quad (5.2)$$

For the first part of the opposition method, it is important that the inductor ripple is minimized so as to minimize the inductor losses and keep the inductor current at the point of switching events as close to the dc value, I_{DC} , as possible. This can be done by increasing the value of inductance through the use of a ferrite core with minimal copper windings to reduce resistance.

For the second part, the duty ratios of T1 and T3 are both fixed at fifty percent. A phase-shift is introduced in between the gate signals of T1 and T3 using open loop control. This phase is adjusted such that the peak value of the inductor current, I_p , matches that of I_{DC} .

From time zero to time t_1 , the inductor current ramps up through T1 and T4. At time t_1 , T4 is turned off and this is followed by a dead-time before the gate signal of T3 is applied. During the dead-time, the body diode of T3 turns on and conducts. After the dead-time has elapsed, the gate signal of T3 is applied and conduction is passed to the channel of the device. In between time t_1 and time t_2 , the inductor current circulates in the loop formed by T1, T3 and the inductor. During this period, the inductor current decays slightly. At time t_2 , T1 is turned off and this is followed by a dead-time before the gate signal of T2 is applied. During this dead-time the body diode of T2 turns on and conducts. After the dead-time has elapsed, the gate signal

of T2 is applied and conduction is passed to the channel of the device. From time t_2 to time t_3 , the inductor current ramps down as it circulates in the loop formed by the inductor, T2 and T3. At time t_3 , T3 is turned off and this is followed by a dead-time before the gate signal of T4 is applied. During this dead-time the body diode of T4 turns on and conducts. After the dead-time has elapsed, the gate signal of T4 is applied and conduction is passed to the channel of the device. In between time t_3 and time t_4 , the inductor current circulates in the loop formed by T1, T3 and the inductor. During this period, the inductor current decays slightly. At time t_4 , T2 is turned off and this is followed by a dead-time before the gate signal of T1 is applied. During this dead-time the body diode of T1 turns on and conducts. After the dead-time has elapsed, the gate signal of T1 is applied and conduction is passed to the channel of the device. Since all four switches experience turn off of the transistor and turn-on of the body diode, the energy dissipated over one switch is E_2 as shown in (5.3).

$$E_2 = E_{off-T} + E_{on-bd} \quad (5.3)$$

In order to experimentally extract E_2 , (5.4) can be used where P_t , I_n , R_n , I_{rms} and R_{dson} are the total power loss measured supplied by the DC supply, inductor harmonic currents, resistance at the n^{th} harmonic, the inductor rms current and the on-resistance of the switch respectively. It should be noted that the second and third terms in the numerator correspond to the inductor losses and conduction losses of the switch respectively. The inductor used in the extraction of E_2 is an air-core inductor wound using litz wire. (5.4) neglects the effect of capacitor losses and in practice, the capacitor losses can be negligibly small if a few MLCC capacitors are used in parallel.

In order to account for the effect of temperature on R_{dson} , the temperature of the switch can be sensed using a thermal camera and then the datasheet can be used to account for the increase in conduction losses. In this paper, R_{dson} of (5.4) is assumed to be constant with temperature. In practice, this assumption causes a slight overestimate of E_2 . However, as conduction losses typically constitute only about ten percent or less of the total power loss, the error is not significant. Since I_{rms} remains relatively constant with f_{sw} , the impact of this error reduces significantly with increased switching frequency as the conduction loss makes up a smaller portion of the total power loss.

$$E_2 = \frac{P_t - \sum I_n^2 \cdot R_n - 2I_{rms}^2 \cdot R_{dson}}{4f_{sw}} \quad (5.4)$$

By taking the difference in between E_1 and E_2 , the sum, E_3 , of the turn-on energy of a transistor and the turn-off energy of the body diode of the complementary switch can be extracted as shown in (5.5). In this way, E_3 and E_2 are extracted for one defined set of voltage and current and can be later used to find the switching loss.

$$E_3 = E_1 - E_2 = E_{on-T} + E_{off-bd} \quad (5.5)$$

Using the boost converter as an example again, the switching loss can be found by adding E_{3-l} which is the extracted value corresponding to the lowest value of inductor current ripple and E_{2-h} which is the extracted value corresponding to the highest value of inductor current ripple. The switching loss can be found using (5.6) which can be expanded to yield the same expression seen in (5.1).

$$P_{sw} = (E_{3-l} + E_{2-h})f_{sw} \quad (5.6)$$

5.2.2: Components used for realising hardware

In Table 5.1, the key components of the double pulse test module and the half-bridges involved in the opposition method are listed.

Table 5.1: Key components involved in both double pulse test module and half bridges for opposition method

Components	Double pulse tester module	GaN half-bridges
Gate driver	LM5113	LM5113
Gate resistance	5.1 ohm, 0402 package	5.1 ohm, 0402 package
Power transistors	EPC2001	EPC2001
MLCC capacitors	C3225X7S2A475K200AB, 4.7 uF, 100V, 1210 package	C3225X7S2A475K200AB, 4.7 uF, 100V, 1210 package
Electrolytic	EKMQ101ETC470MHB5D, 100V, 47 uF	EKMQ101ETC470MHB5D, 100V, 47 uF
Shunt resistor	SDN-414-10	N/A

5.3: Comparison

The two methods are compared against each other with respect to their accuracy, range of testable switching speeds and ease of measurement.

5.3.1: Range of testable switching speeds

One of the key characteristics of GaN HEMTs is their fast switching speeds. These fast switching speeds require instruments with high bandwidth to sense [22]. At

present, the typical instrument used to sense the current of GaN HEMTs is a coaxial shunt resistor [118, 97, 21]. This instrument is typically chosen over other options like current clamps or H-field probes for its high bandwidth and relative ease of use. However, the shunt resistor must be connected as part of the commutation loop as depicted in Figure 5.7 and hence increases the parasitic loop inductance. The additional inductance leads to greater voltage overshoots in the double pulse tester during turn-off compared with that of an actual half-bridge at the same di/dt . The voltage overshoot, v_{over} , is related to the device's di/dt and loop inductance, L_{loop} as defined by (5.7). (5.7) can be used to do a rudimentary assessment of the range of di/dt testable by both the opposition and double pulse test methods.

Figure 5.7: Commutation loops of double pulse tester and half-bridge

$$v_{over} = L_{loop} \frac{di}{dt} \quad (5.7)$$

The parasitic inductance of a SDN-414 current shunt is measured using a Wayne Kerr 6500B impedance analyser to be 4 nH. In this paper, the EPC2001 GaN HEMT with a voltage rating of 100V is considered. The loop inductance of an optimized half-bridge layout involving this switch can be as low as 0.4 nH [24]. Hence, an optimized double pulse tester layout involving an EPC2001 switch can possess, in theory, a loop inductance of as low as 4.4 nH. In practice, this loop inductance is expected to be higher than that value as space must be made to accommodate voltage probe points and additional clearance must be given to the shunt so that the user can attach it to the board.

Using (5.7) and assuming a maximum allowable voltage overshoot of 30V, the maximum testable di/dt for a double pulse tester is 6.8A/ns. The di/dt of GaN switches larger than the EPC2001 has been recorded to be as high as 18.7A/ns [20]. As larger devices have a higher voltage blocking rating, the voltage overshoot can

be larger, hence allowing faster speeds to be tested. Since the EPC2001 is a smaller device, it is anticipated that it should possess a higher switching speed than the larger devices. However, due to the inductance of the current shunt and the EPC2001's lower voltage rating, the testable di/dt is limited to a value below the di/dt of larger devices.

The opposition method uses half-bridges without the additional parasitic of the current shunt. Using (5.7), and assuming a maximum allowable voltage overshoot of 30V, the maximum testable di/dt for the opposition method is 75A/ns. This higher value indicates that the opposition method is more suitable for measuring the switching energy of GaN HEMTs under fast-switching conditions.

In summary, the opposition method is better suited for measuring the switching energy of GaN HEMTs under fast-switching conditions. This is especially so if the device is small and has a low maximum voltage rating.

5.3.2: Ease of data extraction

Using a typical boost converter operated in continuous current mode as an example, if the switching loss is required for a defined operating condition of output power, input voltage, output voltage and frequency, the total number of double pulse test measurements needed to find the switching loss is four – two for the active switch and two for the complementary diode. By contrast, the number of points needed if the opposition method is used is about eight. For the first part of the opposition method, a few power loss measurements must be made in order to plot the power against frequency. In this paper, the typical number of readings used is six. For the second part of the opposition method, two readings for E_2 must be made – one of the readings is used to calculate the value of E_3 that corresponds to the switching energy dissipated by the semiconductor devices when the inductor current ripple through the boost converter is at its minimum. The second reading for E_2 is the energy dissipated when the semiconductor devices in half-bridge switch at the maximum point of the inductor current. The second part of the method also requires the user to take note of the current harmonics through the inductor. Overall, the opposition method is more time-consuming.

5.3.3: Accuracy

The accuracy of each method is considered. The relative impact of each error source is examined in detail to determine which method is more accurate.

Error sources with the double pulse tester are first assessed. Three error sources associated with the double pulse test method are the additional parasitic inductance of the shunt, deskew time in between drain voltage and drain current of the switch and limited bandwidth of the measuring instruments.

First the impact of the parasitic inductance of shunt is considered. In another publication [24], it was shown through calculation that adding 3 nH of loop inductance can increase device loss by as much as thirty percent. In order to verify the impact of loop inductance on switching losses, two half-bridges with slightly different board layouts were created. Their layouts are shown in Figure 5.8. They were tested at an applied drain voltage and drain current of 30V and 1A using the first part of the opposition method. In Figure 5.8 (a), the bus capacitors are placed closer to the switches to reduce loop inductance and in Figure 5.8 (b), they are placed further away to increase loop inductance. By performing the first part of the opposition method and obtaining a plot of power loss against switching frequency as seen in Figure 5.9, it can be seen that the total power loss of the layout of Figure 5.8 (b) is greater. The steeper gradient of the orange trendline of Figure 5.9 suggests that the total switching energy has also increased by about ten percent. Since the shunt adds about 4 nH of loop inductance to the commutation loop, it is expected that the total value of switching loss determined by the double pulse test method will be about thirty percent more than that obtained in a practical circuit.

Figure 5.8: GaN half-bridge layouts

Figure 5.9: Plot of power loss vs frequency for different board layouts

The next source of error in the double pulse test method is the deskew time. In the case of GaN, the switching time has been reported by various authors to be within the range of a few nanoseconds [97, 118, 21, 20]. The delay in between the voltage and current channel is also typically a few nanoseconds. Hence, the deskew time is comparable to the total switching time of the GaN transistors and is expected to significantly impact the extracted value of switching loss. For the case of a 125W, 25V/40V boost converter switching at 263kHz without any deskewing in between the current and voltage channel, the switching losses calculated is 0.37W. However, with 3 ns of deskew time, the switching losses calculated is 0.96W.

The third source of error is the limited bandwidth of present measuring equipment. Many contemporary oscilloscopes and probes are not fast enough to accurately measure GaN HEMTs. It has been mentioned in [22] that low-power GaN HEMTs can exhibit switching times as short as 279 ps and that a 5.5 GHz oscilloscope with a 5.5 GHz voltage probe would be required to measure this time. Presently, oscilloscopes of such high bandwidth are available but are typically expensive to acquire and high voltage probes with 1 GHz bandwidth and above are not yet commercially available. In order to illustrate the impact of insufficient bandwidth on switching energy, an estimate for the turn-off energy of an EPC2001 with an applied drain voltage of 50V and drain current of 25A is made using datasheet. In Figure 5.10, the gate drive circuit and approximated turn-on waveforms are presented. It is

assumed that the LM5113 is used along with an external zero ohm resistor for turn on. The internal turn-on resistance of the gate driver can be calculated using the value of peak sink current of 5A from the datasheet. This sink current is found with drive voltage, V_{dr} , set at 0V and the output pin connected to 5V. The internal resistance, R_g , of the gate driver can be approximated as 1Ω through ohm's law. R_g forms an R-C circuit with the input gate resistance, C_{iss} , of the transistor. Using a value of 850pF for C_{iss} as stated in the datasheet, the time constant for the R-C circuit can be determined and used to approximate the rise time in current, t_{ri} . To determine t_{fi} , the time taken for the gate voltage to fall from miller voltage, V_m , to threshold voltage, V_{th} , is found using (5.8). From time $t = t_1$ to $t = t_2$, the miller plateau is exhibited. Miller charge Q_{gd} can be read from the datasheet and using (5.9) and (5.10), the rise time of voltage, t_{rv} , can be found. Turn off energy is subsequently found using (5.11).

Figure 5.10: Approximated gate driver circuit and theoretical turn-off waveforms

$$V_{gs} = V_m \exp\left(-\frac{t}{R_g C_{iss}}\right), \quad t > t_2 \quad (5.8)$$

$$I_{gate} = \frac{V_m}{R_g} \quad (5.9)$$

$$t_{rv} = \frac{Q_{gd}}{I_{gate}} \quad (5.10)$$

$$E_{off} = \frac{1}{2} I_{DC} V_{DC} (t_{fi} + t_{rv}) \quad (5.11)$$

Due to the limited speed of measurement equipment, the measured values of t_{fi} and t_{rv} are expected to be longer. In this paper, a DPO7354C oscilloscope is used in conjunction with a SDN-414 current shunt for probing current and a passive probe

for probing voltage. Using (5.12), the minimum rise time or fall time that an instrument can measure, t_{slope} can be related to its bandwidth, BW. The measured rise time or fall time of current or voltage, $t_{measured}$, is related to the rise or fall times of the oscilloscope, t_{scope} , the associated probe, t_{probe} as well as the actual value of the measured time, t_{actual} , based on (5.13). In Table 5.2, t_{scope} and t_{probe} times are consolidated for the equipment used. In Table 5.3, a comparison is made in between the datasheet values and the expected measurement values. As seen by Table 5.3, the turn-off energy is about fifteen percent larger as a result of the limited speed of the measuring equipment. For lower values of applied drain voltage and current, the error will be more substantial. As faster devices and better gate drivers are developed, it is expected that the difference between the actual and measured switching energies will increase further.

$$BW = \frac{0.35}{t_{slope}} \quad (5.12)$$

$$t_{measured} = \sqrt{t_{scope}^2 + t_{probe}^2 + t_{actual}^2} \quad (5.13)$$

Table 5.2: Equipment with bandwidth and calculated t_{slope}

Equipment	Bandwidth	t_{slope}
DPO7354C oscilloscope	3.5 GHz	0.1 ns
SDN-414 current shunt	2.6 GHz	0.13 ns
Passive probe	500 MHz	0.7 ns

Table 5.3: Comparison between datasheet calculation and expected measurement

Quantity	Datasheet calculation	Expected measurement value
t_{rv} /ns	0.96	1.19
t_{fi} /ns	0.42	0.45
E_{off} /uJ	0.86	1.03

Next, error sources associated with the opposition method are assessed. Three potential error sources associated with this method are the temperature of the switches, the inductor and the capacitor losses.

The first source of error is temperature. In general, temperature of the transistor affects the switching loss of the transistor. In the case of GaN HEMTs, the effect of temperature on switching behavior has been reported in papers [118, 21, 20]. The dependence of switching losses on temperature varies based on which GaN HEMT is used. In [21], the combined turn-on and turn-off energies were examined for junction temperatures of 25 °C and 100 °C for the EPC1010 from Efficient Power Conversation (EPC) Corporation and it was found that at elevated temperatures, the total switching energy did not increase significantly. In [118], the GS66508 from GaN systems was examined and it was found that the temperature had a significant influence on the turn-on energy but not the turn-off energy. In order to verify the effect of temperature on switching energy the first part of the opposition method was conducted for the test condition of $V_{DC} = 50V$ and $I_{DC} = 5A$ for the frequency range of 350 kHz to 600 kHz. The case temperature of the switches were observed with a thermal camera for each measurement point as shown in Figure 5.11. The half-bridges were run continuously for ten minutes in between each set of readings and were cooled using a 12V fan. It can be seen that despite the increase in temperature of the switches, the graph is highly linear as indicated by the high r-squared value. This suggests that the influence of temperature on the total switching energy of the EPC2001 switches is not significant.

Figure 5.11: Power loss vs frequency for VDC = 50V and IDC = 5A with case temperatures of switches. Verification procedure

Temperature also affects the conduction loss of the switches. The extent of this effect on the calculated total switching energies in the first part of the opposition method is relatively small as conduction losses constitute about ten percent or less of the total loss. This is again supported by Figure 5.11 which shows a highly linear graph despite changes in temperature of the switches. For the second part of the opposition method, the conduction loss typically constitutes about ten percent or less of the total loss measured when the half-bridges are operated at high frequencies so that the combined switching loss and inductor loss predominate. Hence it is not expected to heavily influence the values of E_2 calculated using (5.4).

Capacitor loss is another potential error in the opposition method. However, this source of error is easily mitigated by paralleling a sufficient number of mlcc capacitors and operating the half-bridges such that the harmonic content of the capacitor current correspond to the frequency range for which the equivalent series resistance for the capacitors are very close to its minimum. In this work, six C3225X7S2A475K200AB mlcc capacitors from TDK were used in parallel to supply high frequency harmonic currents. Based on the datasheet values for the mlcc capacitor, the switching frequencies were chosen such that the majority of the harmonic content of the capacitor current will fall within 350 kHz to 20 MHz where the equivalent series resistance of one mlcc capacitor varies from 4 mΩ to 20 mΩ.

Hence it is expected that in both parts of the opposition method, the capacitor losses are minimized and nearly negligible.

The next source of error is the inductor loss. The inductor loss consists of loss in the windings as well as loss in the core. Both of these components exhibit non-linear frequency dependence that must be mitigated in order for the first part of the opposition method to be viable. First, the core loss of the Steinmetz equation is shown in (5.14). The power loss per unit volume, P_V , is related to the amplitude of the ac components of the applied magnetic field, B_{ac} , and the frequency of the ac components, f . Constants k , a and b are material dependent. It should be noted that B_{ac} is directly proportional to the amplitude of the applied current harmonic.

$$P_V = k B_{ac}^a f^b \quad (5.14)$$

For the winding, skin effect losses occur at high frequencies of applied current. Since both the core loss and winding loss are proportional to the amplitude of the applied current harmonics, the frequency dependent loss of the inductor can be mitigated by reducing the current ripple of the inductor. For this paper, a ferrite inductor was chosen to minimize the loss per unit volume. At steady state, the inductor ripple is small and nearly imperceptible as seen in Figure 5.12. As seen by the graphs of Figure 5.9 and Figure 5.11, the power loss is highly linear with respect to frequency. Hence it is expected for the first part of the opposition method, the inductor losses are relatively small.

Figure 5.12: Waveforms for opposition method

For the second part of the opposition method, an air core inductor is used to avoid saturation. In the second part, the inductor was realized using litz wire to minimize losses. However, the loss of the inductor is not negligible compared with the total

loss, P_t , and can easily account for thirty percent or more of it. Hence, the resistances of the winding for different frequency points must be measured using an impedance analyser and the harmonic content must of the inductor be considered. The inductor power loss, P_l , can be related to the rms harmonic current I_n and measured resistance, R_n , at the frequency of the n^{th} harmonic through (5.15). It should be noted that in practice, only a finite number of harmonics up to m can be considered. m must be chosen manually by the experimenter. As only a finite number of harmonic components can be considered, it is expected that the value of E_2 as calculated in (5.4) will be overestimated.

$$P_l = \sum_{n=1}^m I_n^2 R_n \quad (5.15)$$

In summary, maximum testable di/dt , ease of characterization and amount of error associated with each method was assessed in this section. Table 5.4 summarises the comparison in between the two methods. It should be noted that the maximum di/dt was in Table 5.4 was calculated based on an overvoltage of 30V and a layout designed around an EPC2001 switch. Error for the double pulse test and the opposition method were estimated.

Table 5.4: Summary of comparison

	Double pulse test method	Opposition method
Maximum testable di/dt / A/ns	6.8	75
Number of measurements needed per half-bridge characterization	4	8
Error/%	30	5

5.3.4: Experimental comparison

In this section, the double pulse and opposition methods are compared through experiment. The switching loss of a boost converter realized using EPC2001 GaN HEMTs was characterized using both the double pulse test and opposition methods for different output power, output voltage and switching frequency. The test conditions of each operating point are summarized in Table 5.5. The measurement equipment used for each method along with their purposes are recorded in Table 5.6 and Table 5.7.

Table 5.5: Table of operating conditions

Operating condition no.	Input voltage/V	Output voltage/V	Output power/W	Switching frequency/ kHz
1	25	50	25	263
2	25	50	75	263
3	25	50	125	263
4	25	40	125	263
5	25	50	125	400
6	25	50	125	500

Table 5.6: Testing equipment for double pulse test method

Equipment	Purpose
DPO7354C oscilloscope	Display of waveforms
P6139B passive probes	Voltage measurement
SDN-414 current shunt	Current measurement

Table 5.7: Measurement equipment used for opposition method

Equipment	Purpose
U3401A benchtop multimeters	Measurement of input power.
FLIR T440 thermal camera	Measurement of casing temperature of switches.
6500B impedance analyser	Measurement of inductor resistances.
HDO6104 oscilloscope	Measure inductor harmonic current content.
CP031 current clamp	Measure inductor current.

In order to improve measurement accuracy and maximum testable di/dt of each method, it is important to design the double pulse test module and the half-bridges involved in the opposition method carefully. The hardware for each setup is depicted in Figure 5.13. The gate driver, capacitors and gate resistance involved in both the double pulse test module and the half-bridge are the same. The half-bridge utilizes the suggested optimal layout from [24]. As the current shunt introduced additional

parasitic inductance in the double pulse tester, the switching speed had to be limited through the use of a larger gate resistance of 5.1Ω . For the experiment, the gate resistance of the half-bridge to be characterized was also set to be 5.1Ω so that the tester can be used for the characterization.

Figure 5.13: Opposition method and double pulse test method hardware

The steady state inductor current waveform for a boost converter is depicted in Figure 5.14. For each operating condition, the combined switching energy of the body diode and the active switch corresponding to the high point of the inductor current, E_{2h} , and the low point of the inductor current, E_{3l} , must be extracted.

Figure 5.14: Bidirectional boost converter with inductor waveforms

In the double pulse test method, there is delay time in between the acquisition of a measurement point and the display of it on the screen as a result of the analog-to-digital conversion. This delay is different for the current and voltage channels and hence greatly affects the calculation of switching energies. V_{ds} and I_{ds} must be repositioned to the correct positions relative to each other through the procedure of deskewing in order to get accurate results. The deskewing of the double pulse tester is important as it significantly affects calculated switching losses. In Figure 5.15, a deskew time of 3 ns is introduced into the waveform of I_{ds} for the cases of turn-on and turn-off. In Table 5.8, the effect of deskew time on the calculated switching

energies is illustrated. In the following paragraphs, the procedure for deskewing is described.

Figure 5.15: Effect of deskewing on turn-on and turn-off current waveforms

Table 5.8: Effect of deskewing on switching energies

Turn-on energy/uJ		Turn-off energy/uJ	
Without deskew	With deskew	Without deskew	With deskew
1.40	0.30	0.31	0.62

After turn-on of the active switch, a period of oscillations follow. During this time period, the switch exhibits highly inductive behaviour. By considering the di/dt across it and using a scaling factor, L_{par} , for the parasitic inductance of the switch, the voltage across the switch, V_{osc} , during the oscillatory period can be plotted and aligned with the voltage oscillations of the drain-to-source voltage as depicted in Figure 5.16. V_{osc} is related to L_{par} and di/dt through (5.16). V_{osc} can then be superimposed on V_{ds} and deskew time can be adjusted such that the parasitic oscillations of V_{ds} and the V_{osc} waveform align as seen in Figure 5.16.

$$V_{osc} = L_{par} \frac{di}{dt} \quad (5.16)$$

After turn-off of the active switch, a period of oscillations follow. During this time period, the switch exhibits highly capacitive behaviour due to its output capacitance. By considering the dv/dt across it and the value of output capacitance, C_{oss} , in the datasheet, the current across the switch, I_{osc} , during the oscillatory period can be plotted and aligned with the voltage oscillations of the drain-to-source voltage as depicted in Figure 5.16. I_{osc} is related to C_{oss} and dv/dt through (5.17). I_{osc} can then be superimposed on I_{ds} and deskew time can be adjusted such that the parasitic oscillations of I_{ds} and the I_{osc} waveform align as seen in Figure 5.16.

$$I_{osc} = C_{oss} \frac{dv}{dt} \quad (5.17)$$

It was found that the deskew time for both the turn-on and turn-off cases was 3 ns. This time was consistent across a few switching conditions as depicted in Figure 5.16 and hence, it was also applied to the current waveforms of the body diode.

Figure 5.16: Examples of deskewing technique

In order to account for uncertainty of the double pulse method, the scaling errors, V_s and I_s , and the offset errors, V_o and I_o of the oscilloscope were read from the manual. The errors were added and subtracted from the measured voltage and current values, V_m and I_m , according to (5.18) to (5.21) to find the upper and lower bounds of the current, I_{lb} and I_{ub} , and voltage values, V_{lb} and V_{ub} , obtained during switching. The waveforms along with their envelopes were processed in MATLAB to compute the

upper and lower bounds of the instantaneous power and subsequently the switching energies according to .

$$V_{lb} = V_m - (V_o + V_s) \quad (5.18)$$

$$V_{ub} = V_m + (V_o + V_s) \quad (5.19)$$

$$I_{lb} = I_m - (I_o + I_s) \quad (5.20)$$

$$I_{ub} = I_m + (I_o + I_s) \quad (5.21)$$

$$P_{lb} = V_{lb} \cdot I_{lb} \quad (5.22)$$

$$P_{ub} = V_{ub} \cdot I_{ub} \quad (5.23)$$

where V_{lb} , V_{ub} , I_{lb} , I_{ub} , P_{lb} and P_{ub} represent the upper and lower bounds of the voltage current and power respectively. The resulting upper and lower bounds for the cases of measured voltage, current and power are superimposed on the measured values as shown in Figure 5.17.

Figure 5.17: Current, voltage and power waveforms with upper and lower bounds

The values for the double pulse test method were extracted and presented in Figure 5.18. It should be noted that E_{on-bdh} is negative because the output capacitance of the switch is being discharged at the same time that the active switch is being turned off. The integration limits for finding these energies were defined as seen in Figure 5.18. In Figure 5.18(a), t_1 is the time taken for the power to rise to one percent of the maximum power, P_m during the switching time and t_2 is the time taken for the power to fall back to one percent of the maximum power. In Figure 5.18(b), t_1 is the time taken for the power to fall to one percent of the minimum power, $-P_m$ during the switching time and t_2 is the time taken for the power to rise back to one percent of the minimum power.

Figure 5.18: Integration limits definitions

Table 5.9: Results for double pulse test method

Operating condition	E_{on-tl}/uJ	$E_{off-bdl}/uJ$	E_{off-th}/uJ	E_{on-bdh}/uJ
1	0.37	4.35	0.82	-0.71
2	0.42	4.21	0.76	-0.64
3	0.56	4.22	0.90	-0.59
4	0.30	3.18	0.62	-0.44
5	0.47	4.17	0.88	-0.58
6	0.48	4.25	0.89	-0.59

The opposition method was also applied for various conditions. In Figure 5.19, the graphs for the first part of the opposition method are presented. In Table 5.9, the values for E_2 are presented. In the opposition method, instruments from both parts contribute to the uncertainty of E_{3l} and E_{2h} . Hence in order to quantify the relative impact of the errors introduced by each error, the graph of Figure 5.20 was created. In the first part of the opposition method, the multimeters introduced uncertainties in the power loss values which affected the slope of the graphs in the first method. The relative error introduced into E_1 is typically about three percent. The impedance analyser used to measure the inductor resistance can measure the impedance to within 0.05% uncertainty. This was also taken into account for Figure 5.20.

Figure 5.19: Extraction of first part of opposition method

Table 5.10: E_2 values for opposition method

Operating condition no.	$E_{2-l}/\mu\text{J}$	$E_{2-h}/\mu\text{J}$
1	0.98	0.14
2	0.27	0.55
3	1.06	1.56
4	0.78	1.06
5	0.71	1.08
6	0.86	1.05

Figure 5.20: Relative impact of error sources on uncertainty of E_{2h} and E_{3l}

5.3.5: Results of comparison and analysis of uncertainty

The switching loss for both methods were consolidated in Table 5.11. It is seen that the double pulse test method exhibits a higher switching loss as expected due to the presence of the current shunt. This deviation is much more significant under operating conditions 1 and 2 where light load is applied to the converter. This also expected because at lighter loads, the switching time of the transistor is significantly less and based on (5.12) and (5.13), the overestimate of the switching time will be more significant and leads to greater overestimate of switching energies.

Table 5.11: Switching loss comparison of both methods

Operating condition no.	Opposition method		Double pulse test method	
	Switching loss/W	Uncertainty/%	Switching loss/W	Uncertainty/%
1	0.44	2.5	1.27	12
2	0.73	1.7	1.25	14
3	1.01	1.9	1.34	14
4	0.73	6.6	0.96	12
5	1.49	4.4	1.98	12
6	1.77	2.5	2.52	12

5.4: Verification

5.4.1: Slow switching conditions

When the driving capability of the gate driver is very low, the switching speed of power devices will be very slow. Under such conditions, the di/dt s and dv/dt s are low enough to be captured accurately by the scope and the deskew time in between the current and voltage channels is negligibly small compared with the switching time. Hence, the switching energies obtained using the double pulse tester will be highly accurate. In addition, the parasitics do not influence the switching behaviour significantly when switching speeds are low. Hence, the observed behaviour will be primarily caused by the semiconductor itself and can be used to verify how well the semiconductor physics have been predicted by the model. Simulation results from the proposed model in Chapter 3 were compared with experimental ones under slow-switching conditions. Switching speed was limited using a $1\text{k}\Omega$ gate resistance. The simulation for slow-switching conditions was done in LTSPICE IV using the circuit of Figure 3.12. The turn-on and turn-off waveforms for the experiments, the manufacturer's simulation model and the proposed model are presented in Figure 5.21 and Figure 5.22. In Figure 5.23, the switching energies of the model are compared against those obtained in the experiment.

Figure 5.21: Turn-on waveforms under slow switching conditions

Figure 5.22: Turn-off waveforms for slow-switching conditions

(a) Turn-on energy comparison

(b) Turn-off energy comparison

Figure 5.23: Turn-on and turn-off energy comparisons for experiment and simulation results

The higher miller gate voltage levels in Figure 5.21 and Figure 5.22 indicate that the model possesses a lower transconductance compared with the actual device. However, the transitions of I_{ds} and V_{ds} fit with experiment well. This suggests that the capacitances have been modelled sufficiently. As the transitions of I_{ds} and V_{ds} match well, the switching energies predicted by the model for the case of slow-switching also match well with experiment.

5.4.2: Fast switching conditions

The simulation of the switch under fast switching conditions was done in LTSPICE IV using the circuit of Figure 3.13. When the driving capability of the gate driver is high, the switching speed of the power devices will be very fast. Under such conditions, the di/dts and dv/dts are high. Due to the limited bandwidth of present measuring equipment and high switching speeds of GaN HEMTs, the double pulse tester's accuracy deteriorates significantly. Parasitic inductances also limit the range of testable switching speeds. Hence, in order to extract the switching energy under practical fast-switching conditions, the opposition method is used. Using the values of E_{3l} and E_{2h} and switching loss corresponding to operating conditions 2, 4 and 6 from Table 5.5, the model is assessed in terms of its accuracy.

Table 5.12: Comparison of simulation results with opposition method results

Operating condition no.	$E_{3l}/\mu J$			$E_{2h}/\mu J$			Power loss/W		
	Measured	Vendor	Proposed	Measured	Vendor	Proposed	Measured	Vendor	Proposed
2	2.23	3.46	9.20	0.55	0.15	0.19	0.73	0.95	2.47
4	1.72	2.72	6.25	1.06	0.17	0.27	0.73	0.76	1.71
6	2.49	3.80	10.51	1.05	0.15	0.32	1.77	1.98	5.42

It can be seen from Table 5.12 that the model consistently overestimates the power loss and E_{3l} values while consistently underestimating the E_{2h} values. This is due to the fact that both the proposed and vendor models constantly overestimate the miller voltage during switching as evidenced in the gate voltage waveforms of Figure 5.21 and Figure 5.22.

An increased miller voltage opposes the gate driver voltage during turn-on of the device, hence causing slower switching speed and increasing the simulated turn-on energy of the transistor. This in turn causes E_{3l} to be higher than the expected experimental value.

An increased miller voltage also helps to discharge the power transistor gate more quickly during turn-off, hence causing faster switching speed and reducing the simulated turn-off energy of the transistor. This in turn causes E_{2h} to be lower than the expected experimental value.

The proposed model also deviates further from the experimental values of E_{3l} than the vendor model. The likely cause is that the proposed model predicts a longer miller plateau period as evidenced by Figure 5.21 and Figure 5.22. This leads to a higher value of E_{on-T} and consequently, a significantly higher predicted switching loss.

In light of these observations, one of the possible ways of improving the model's accuracy is to improve upon its ability to predict the gate voltage more accurately. In particular, the model's i-v characteristic can be further adjusted such that the miller voltage and miller plateau periods are predicted with better accuracy.

5.5: Chapter summary

In this chapter, the verification techniques used for the model were touched on. A critical comparison was done in between the double pulse test method and the opposition method and it was found that the opposition method was more suitable for extracting switching energies under more practical, fast-switching conditions.

Finally, results from the model were compared against the experimental results for both slow-switching and fast-switching conditions. Under slow-switching conditions, the transitions of I_{ds} and V_{ds} of the simulation of the GaN HEMT matched the experiment very well indicating that the capacitances were modelled sufficiently. However, the higher miller plateau voltage indicates that the transconductance is underestimated. This observation is further corroborated by the higher values of E_{3l} predicted by the model in the opposition method.

CHAPTER 6 : COMPARISON BETWEEN GaN HEMT CONVERTER AND SILICON MOSFET CONVERTER

6.1: Chapter overview

In the past decade or so, there has been much interest in the field of renewable energy systems [158, 159, 160, 161, 162]. Home energy storage systems that manage power flow in between photovoltaic panels, batteries and the grid have long been commercialised by companies like SMA and Infinisolar. In such systems, battery storage is often quite expensive and hence, it is desirable to incorporate modular battery storage so that the user can save on initial investment costs but have the flexibility to upgrade later. In Figure 6.1, the block diagram of such a system is displayed. In Figure 6.1, the input battery voltage is boosted to the required 400 Vdc voltage in two stages. Doing so in this manner reduces the boost ratio of the isolated dc-dc converter and hence could potentially lead to a smaller isolation transformer and less overall system costs.

Figure 6.1: System architecture of modular home energy storage system

For the low power dc-dc converter of the first stage, either silicon power MOSFETs or GaN HEMTs can be used for its realisation. In this chapter, two 400W, 48V to 70V bidirectional dc-dc converters are designed and tested. They are benchmarked against each other in terms of volume, cost and efficiency in order to assess the design benefits of GaN HEMTs in such systems.

6.2: Design considerations

6.2.1: Design criteria

For the example system of this chapter, it was assumed that lead acid batteries would be used for the energy storage as they were inexpensive common. The voltage of such batteries is typically 48V which corresponds to the input of the bidirectional converter. For the topology of the bidirectional converter, a half-bridge boost converter was chosen as depicted in Figure 6.2. The design parameters of this converter are consolidated in Figure 6.2. A high switching frequency was chosen so as to minimise the volume of the inductor and potentially save costs on the casing required.

Figure 6.2: Boost converter with inductor current waveform

Table 6.1: Consolidated design criteria of converter

Design parameter	Value
Input voltage/V	48
Output voltage/V	70
Power rating/W	400
Switching frequency/kHz	263
Inductor ripple/A	± 0.9
Peak to peak output voltage ripple	< 5 percent of output voltage

By keeping the design parameters the same for both the silicon MOSFET converter and the GaN HEMT converter, it is expected that the converters will exhibit a difference in terms of the cooling requirements and consequently the size of heatsink.

The value of inductance and switching frequency was selected based on an input current peak-to-peak ripple that is 20 percent of the dc component of the current going through the inductor. Hence, the current rating of the switches must be above 9.2A. The inductor value was chosen to be 34 μ H.

6.2.2: Gate drive design

Both the silicon MOSFET and the GaN HEMT may be driven using bootstrap gate drivers which are relatively cheap and easy to realise. The key difference between both switches in terms of gate drive design is that the GaN HEMT exhibits a significantly higher gate leakage current. In this work, the BSC160N10NS3 silicon MOSFET and EPC2001 GaN HEMT are used. Based on datasheet values, the silicon MOSFET possesses a typical forward gate-source leakage current of 1nA compared with the GaN HEMT's forward gate-source leakage current value of 1mA. Due to the larger leakage current, it is advisable to use larger values of capacitance for the bootstrap capacitance to ensure that the voltage across it is maintained.

6.3: Switch selection

In order to select a good silicon MOSFET for comparison, the voltage rating of the switch was fixed at 100V which was the same voltage rating as the GaN HEMT. In order to minimise parasitic inductances, the package of the silicon MOSFET was fixed to be a PG-TDSON-8 surface mounted package. Out of the devices shown in Table 6.2, the best one was selected based on Huang's device figure of merit (HDFOM) [42] for comparison with the 100V EPC2001 power transistor. HDFOM is defined in (6.1). Miller charge, Q_{gd} , was measured at 50V according to the datasheets. As seen from Table 6.2, the BSC160N10NS3 G MOSFET was the best candidate amongst the pool of 100V-rated devices. The EPC2001 GaN HEMT was also selected in a similar fashion.

$$HDFOM = \sqrt{Q_{gd}R_{dson}} \quad (6.1)$$

Table 6.2: Silicon Power MOSFETs and their respective HDFOMs

Switch	I_d/A	$R_{dson}/m\Omega$	Q_{gd}/nC	$HDFOM/(m\Omega nC)^{\frac{1}{2}}$
BSC750N10ND G	13	75	2	12.2
BSC440N10NS3 G	18	44	1.3	7.6
IRFH7194	22	16.4	4.3	8.4
IRFH5210	35	14.9	11	12.8
IRFH7110	37	13.5	16	14.7
IRFH5110	40	12.4	15	13.6
BSC252N10NSF G	40	25.2	3	8.7
BSC265N10LSF G	40	26.5	3	8.9
BSC160N10NS3 G	42	16	3	6.9
BSC196N10NS G	45	19.6	6	10.8

6.4: Results

A silicon MOSFET half-bridge and a GaN HEMT half-bridge were created and compared in terms of size, efficiency and cost. A third commercially available 600W boost converter was selected as an additional reference. In Figure 6.3, these converters are presented to give the reader a sense of their relative sizes. The box volumes of each converter are recorded beside converter in parenthesis.

Figure 6.3: Bidirectional boost converters relative sizes

The converters are also benchmarked against each other in terms of efficiency as seen in Figure 6.4. It can be seen that the GaN converter is significantly more efficient than the commercial and silicon converters as expected.

Figure 6.4: Efficiency of different converters

The loss components of the silicon-based and GaN-based prototypes can be approximated using datasheet values. For this work, it is assumed that the large number of capacitors were able to suppress the voltage ripple and hence make the losses across the capacitor bank negligibly small. The approximated loss components for the silicon and GaN-based prototypes when they output 400W are presented in Table 6.3.

Table 6.3: Approximated loss breakdown at 400W

Loss component	Silicon converter	GaN converter
Inductor	1.51W	1.51W
Switching loss	10.60W	4.09W
Conduction loss	1.11W	0.49W

All three converters were all cooled with a 12Vdc fan and the temperature of the power transistors of the silicon MOSFET and GaN HEMT half-bridges were recorded using a thermal camera as shown in Figure 6.5. It is seen from spot 2 of the silicon MOSFET converter and from the hot spot of the GaN HEMT converter that the temperatures of the switches are comparable. However, it should be noted that the GaN HEMT converter did not have an additional heatsink unlike the silicon MOSFET converter. This suggests that the GaN switches exhibit significantly less losses than the silicon MOSFET switches.

(a) Temperature reading of switches of silicon MOSFET converter

(b) Temperature reading of switches of GaN HEMT converter

Figure 6.5: Temperature readings of silicon MOSFET and GaN HEMT converters

Next, the cost of the GaN HEMT converter and the silicon MOSFET converter are compared and the cost breakdown of each is given in terms of SGD as shown in Figure 6.6. In total, the cost of one silicon half-bridge is 45.20 SGD and the cost of one GaN half bridge is 44.23 SGD. It can be seen that although the GaN HEMTs are twice as expensive as the silicon MOSFETs, the absence of the heatsink compensated for the more expensive switches.

(a) Cost breakdown of silicon MOSFET prototype

(b) Cost breakdown of GaN HEMT prototype

Figure 6.6: Cost breakdown of both types of half-bridge converters

6.5: Chapter summary

In this chapter, a GaN HEMT half-bridge and a silicon MOSFET half-bridge were constructed for application in a home energy storage system. By comparing these two designs in terms of cost, volume and efficiency, it was found that the GaN HEMT half-bridge demonstrated better efficiency with smaller volume and comparable cost.

It can be seen that GaN HEMTs offer many advantages over silicon MOSFETs without significantly incurring drawbacks such as a more complex gate driver design. At present, hindrances to the adoption of GaN HEMTs include the relatively

low voltage and current ratings of the devices as well as parasitic inductances arising from packaging and circuit interconnect which limit the switching speed of the devices. For applications which require relatively low power rating of a few kilowatts and a relatively low voltage rating of 650V and below, optimally packaged devices and gate drivers already exist. Hence, it is expected that GaN HEMTs will replace silicon MOSFETs for various low-power, low-voltage applications but in high-power, high-voltage applications, where optimal packaging technology has yet to exist, the adoption of GaN will be less widespread.

CHAPTER 7 : CONCLUSION AND RECOMMENDATIONS

7.1: Conclusions

In this work, the following was done:

- 1) In Chapter 3, a new model was proposed for the GaN HEMT which utilises behaviourally modelled capacitances and an i-v characteristic that was approximated from physics –based equations.
- 2) In Chapter 4, the trade-off in between parasitic inductance and thermal dissipation of a half-bridge is considered.
- 3) In Chapter 5, the verification techniques and extraction techniques used to develop the half-bridge model are discussed. The advantages and disadvantages of the double pulse test and opposition methods in terms of extraction of switching losses were highlighted in detail. The accuracy of the half-bridge model was also tested experimentally under both fast-switching and slow-switching conditions.
- 4) In Chapter 6, a GaN HEMT half-bridge is benchmarked against a silicon half-bridge for the case of a home energy storage system.

The following conclusions from each chapter are summarised below:

- 1) In Chapter 3, the proposed model was able to fit the capacitances well. It was found that the proposed i-v characteristic also allowed for the derivation of an expression for the sensitivity of the transconductance with respect to temperature. This expression could potentially be useful for signal processing applications.
- 2) In Chapter 4, the trade-off in between a low parasitic inductance design and a good thermal dissipation capability was investigated through simulation and experiment. 3 PCB layouts were investigated and as expected, the layout with a high amount of parasitic inductance in both the gate driver and commutation loops was the most lossy followed by the layout with a high commutation loop inductance but low gate loop inductance and followed by the layout with the least parasitic inductance in both loops. The half-bridge model overestimates the losses of the half-bridges but predicts the general relationship in between the parasitic inductances and switching energies.

- 3) In Chapter 5, the double pulse test method and the opposition method were compared against each other in terms of how accurately they can extract switching losses of GaN transistors. It was found that due to the additional parasitic inductance of the current shunt, the double pulse test method overestimates the overall switching losses. The switching speeds testable by the double pulse method are also limited by the current shunt and the bandwidth of state-of-the-art oscilloscopes and probes. The half-bridge model was also tested under both slow-switching and fast switching conditions. Under slow-switching conditions, where the effects of parasitic inductances are negligible, the model exhibits good agreement with the experimental results. Under fast-switching conditions, where the effects of parasitics became more pronounced, the model overestimates the switching losses significantly. The results suggest that this deviation was caused by overestimation of miller voltage by the model. Making the gate voltage fit better could be the focus of a future work.
- 4) In Chapter 6, a GaN HEMT half-bridge was benchmarked against a silicon MOSFET half-bridge and it was found that the GaN HEMT half-bridge was three times smaller in terms of box volume, more efficient by as much as two percent and still possessed a comparable cost to the silicon MOSFET half-bridge.

7.2: Suggestions for Future Work

The following suggestions have been made for future work.

- 1) The developed model does not relate power device behaviour to temperature. Electro-thermal modelling of GaN transistors can be the subject of a future work.
- 2) In Chapter 4, PCBs with components on two sides were not explored. The possibility of changing the thickness of a two-layer PCB to reduce the parasitic inductances while preserving costs can be explored in future.
- 3) In Chapter 5, one of the main drawbacks of the opposition method is the self-heating of the switches. This can be counter-acted by operating the converter in short bursts and then measuring power at the appropriate instances in time. In doing so, the error caused by self-heating can be minimised and it will also be easier to set the device temperatures.

- 4) GaN HEMTs are the only power transistors with a body diode that can be enhanced by an applied gate bias. Future work could exploit this fact to develop a gate driver that reduces the losses that occur during dead-time.
- 5) In Chapter 6, silicon MOSFETs were compared against GaN HEMTs for the case of a hard-switched boost converter. However, for the case of soft-switched low power converters, it has been reported that the benefit of GaN HEMTs is marginal [163]. A comparison in between both technologies involving a larger range of topologies can be the subject of future work

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APPENDIX

A1: Derivation of i-v characteristic for GaN HEMT

The derivation of i-v characteristic is presented below. Starting from (3.11) and substituting charge sheet expression from (3.12), (3.13) can be derived as seen in (A1) below.

$$\begin{aligned}
 I_{ds} &= Zq\mu_n \left[n_{s0} \exp \left(\frac{q\epsilon \left(V_{gs} - V_c(x) - V_{th} - \frac{q(d_d + d_i)n_{s0}}{\epsilon} \right)}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \right) \frac{dV_c}{dx} \right. \\
 &\quad \left. + \frac{kT}{q} \left(\frac{-q\epsilon}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \right) n_{s0} \exp \left(\frac{q\epsilon \left(V_{gs} - V_c(x) - V_{th} - \frac{q(d_d + d_i)n_{s0}}{\epsilon} \right)}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \right) \frac{dV_c}{dx} \right] \\
 &= \frac{Z\mu_n q^3 (d_d + d_i) n_{s0}^2}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \cdot \left[\exp \left(\frac{q\epsilon \left(V_{gs} - V_c(x) - V_{th} - \frac{q(d_d + d_i)n_{s0}}{\epsilon} \right)}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \right) \right] \frac{dV_c}{dx} \\
 &= K_1 \exp(K_2(V_{gs} - V_c - V_{th} - K_3)) \frac{dV_c}{dx} \tag{A1}
 \end{aligned}$$

Where K_1 , K_2 and K_3 are given below.

$$K_1 = \frac{Z\mu_n q^3 (d_d + d_i) n_{s0}^2}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \tag{A2}$$

$$K_2 = \frac{q\epsilon}{q^2(d_d + d_i)n_{s0} + \epsilon kT} \tag{A3}$$

$$K_3 = \frac{q(d_d + d_i)n_{s0}}{\epsilon} \tag{A4}$$

Integrating A1 with respect to x from 0 to L as shown in (A5), (5) is eventually derived as seen in (A6).

$$\int_0^L I_{ds} dx = \int_0^{V_{ds}} K_1 \left[\exp \left(K_2(V_{gs} - V_c - V_{th} - K_3) \right) \right] dV_c \tag{A5}$$

$$\begin{aligned}
 I_{ds} &= \frac{K_1}{K_2} \left[\exp \left(K_2(V_{gs} - V_{th} - K_3) \right) - \exp \left(K_2(V_{gs} - V_{ds} - V_{th} - K_3) \right) \right] \\
 &= \frac{K_1}{K_2} \left[\exp(-K_2 K_3) \right] \left[\exp \left(K_2(V_{gs} - V_{th}) \right) \right] [1 - \exp(-K_2 V_{ds})] \\
 &= K_4 \left[\exp \left(K_2(V_{gs} - V_{th}) \right) \right] [1 - \exp(-K_2 V_{ds})] \tag{A6}
 \end{aligned}$$

Where K_4 is given in (A7).

$$K_4 = \frac{K_1}{K_2} \left(\exp(-K_2 K_3) \right) \tag{A7}$$

A2: Partial derivatives of K_4 and K_2 with respect to temperature

$$\frac{\partial K_2}{\partial T} = - \frac{q \varepsilon^2 k}{(q^2 (d_d + d_i) n_{s0} + \varepsilon k T)^2} \quad (\text{A8})$$

$$\frac{\partial K_4}{\partial T} = \frac{K_1}{K_2} \frac{1}{L} \left(\exp(-K_2 K_3) \right) \left(\frac{q \varepsilon^2 k (d_d + d_i) n_{s0}}{(q^2 (d_d + d_i) n_{s0} + \varepsilon k T)^2} \right) \quad (\text{A9})$$

VITA

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