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**Design of a One-Watt Level RF Power
Amplifier for Smartphones**

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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Table of Contents

Acknowledgments.....	i
Table of Contents.....	ii
Summary	iv
List of Figures	vi
List of Tables	ix
List of Abbreviations	x
Chapter 1 Introduction.....	1
1.1 Background and Motivations.....	1
1.2 Objectives and Scope.....	4
1.3 Contributions.....	5
1.4 Organization.....	6
Chapter 2 Literature Review.....	7
2.1 Power Amplifier Fundamentals	7
2.1.1 Gain.....	7
2.1.2 Power-Efficiency	10
2.1.3 Linearity.....	11
2.1.4 Stability	14
2.2 RF Power Amplifier Design	14
2.2.1 Output Stage.....	16

2.2.2	Output Matching Network	18
2.3	Transformer.....	27
2.3.1	Layout Parameters	27
2.3.2	Loss Mechanisms.....	30
2.3.3	Lumped-Element Model	35
2.4	Conclusions.....	38
Chapter 3	Substrate Thickness Effect on the Transformer.....	39
3.1	Introduction.....	39
3.2	Transformer with Different Substrate Thicknesses	40
3.3	Simulation Results	42
3.4	Conclusions.....	50
Chapter 4	Design of a One-Watt RF Power Amplifier	51
4.1	Introduction.....	51
4.2	Output Transformer Analysis	52
4.3	Fully Integrated 4G/LTE CMOS RF Power Amplifier	66
4.4	Measurements and Results.....	74
4.5	Conclusions.....	81
Chapter 5	Conclusions and Recommendations	82
5.1	Conclusions.....	82
5.2	Recommendations and Future Work	83
	Author's Publications & Awards	86
	Bibliography	87

Summary

Smartphones, embodying wireless data and voice communications means, are increasingly the wireless communications transceiver (phone) of choice. Nevertheless, the primary complaint of smartphone users is the short battery lifespan between charges, and this complaint is exacerbated with the increasing speed and the amount of data communications, particularly with the existing 4G Long Term Evolution (LTE) data and impending 5G data communication protocols.

The radio frequency (RF) power amplifier is one of the most critical blocks in the smartphone, in part because it is often the most power-consumptive and power-dissipative block therein. To address the said short battery lifespan, it is imperative that the power dissipation of the RF power amplifier be low and its power-efficiency high.

In this MEng program, we identify that the ultra-thin substrate thickness in CMOS processes can drastically degrade the parameters of the transformer, including the parasitic resistances, quality factor, coupling factor, and power-efficiency. The most appropriate substrate thickness option of the GF 65nm CMOS process is selected to improve the thermal dissipation without compromising the performance of the transformer.

Our designed CMOS RF power amplifier uses the series-combining transformer to combine the power cells in order to achieve approximately 30dBm maximum output power. To improve the power-efficiency of the series-combining transformer, we

analyze and investigate the influence of the non-ideal center tap at the primary winding of the series-combining transformer. We derive an analytical expression and show that how the parasitic resistance between the non-ideal center tap and the real ground, and the process variation degrade the power efficiency of the transformer due to the non-ideal center tap of the transformer.

Further, we model the bonding wires of the 32pin QFN (5mm x 5mm) package, including the co-simulations of the CMOS RF power amplifier circuit and 32pin QFN (5mm x 5mm) package. The bonding wire structure is subsequently designed to reduce the power loss at the supply and ground nodes, thereby somewhat improving the power-efficiency.

We design and monolithically realize a CMOS RF power amplifier prototype that embodies a custom-designed output transformer with ideal center taps at primary windings. The designed RF power amplifier was monolithically realized, achieving 29.3dBm maximum output power and 17.29% PAE; the PAE is somewhat lower than reported designs. We attribute the low PAE to the insufficiently rigorous extraction and modeling of the wide and long metal lines. Improvements to rectify the low PAE are suggested in our future work. For the intended 4G LTE applications, the spectrum emission masks of the 20MHz QPSK and 16QAM LTE signals are fulfilled at the 23dBm output power.

List of Figures

Fig. 1.1 Wireless communication standards development.....	1
Fig. 2.1 Power flow diagram of an RF power amplifier [9]	8
Fig. 2.2 P_{OUT} versus P_{IN} for RF power amplifier indicating P_{1dB} and IP_3 [12]	13
Fig. 2.3 Intermodulation products in the two-tone measurement [12]	13
Fig. 2.4 Block diagram of a typical two-stage RF power amplifier	15
Fig. 2.5 Power combining technique with LC baluns [28]	20
Fig. 2.6 Simple model of an ideal transformer	21
Fig. 2.7 Power combining technique with transformers	23
Fig. 2.8 (a) Series-combining transformer (SCT), and (b) Parallel-combining transformer (PCT) [24]	24
Fig. 2.9 Layout parameters of a 2-to-3 transformer	28
Fig. 2.10 Magnetic field and electric field distribution in the substrate [47].....	34
Fig. 2.11 The π -network of an inductor [38]	36
Fig. 2.12 The lumped-element model of a transformer [35, 52, 54].....	37
Fig. 3.1 The 3D view of a 3-to-3 interleaved transformer	41
Fig. 3.2 Cross-section substrate structure of the commercial 65nm CMOS technology	41
Fig. 3.3 Simulation results at different substrate thicknesses for (a) the primary winding inductance L_p , and (b) the secondary winding inductance L_s	43
Fig. 3.4 Simulation results at different substrate thicknesses for (a) the primary winding resistance R_p , and (b) the secondary winding resistance R_s	45

Fig. 3.5 Simulation results at different substrate thicknesses for (a) the primary winding quality factor Q_p , and (b) the secondary winding quality factor Q_s	46
Fig. 3.6 Simulation results of the coupling factor K for different substrate thicknesses	48
Fig. 3.7 Maximum power-efficiency η_{max} of transformer for different substrate thicknesses	49
Fig. 4.1 Block diagram of our designed CMOS RF power amplifier	52
Fig. 4.2 A 1-to-1 transformer with the center-tapped primary winding	53
Fig. 4.3 The transformer lumped–element model (a) with an ideal center tap, and (b) with a non-ideal center tap	54
Fig. 4.4 The transformer power-efficiency versus RA for different a_1	59
Fig. 4.5 The transformer power-efficiency versus a_1 for different RA	60
Fig. 4.6 Process variation effects on the transformer power-efficiency for different a_1	62
Fig. 4.7 The transformer lumped–element model for M power cells (a) with ideal center taps, and (b) with non-ideal center taps	63
Fig. 4.8 (a) Schematic of our designed CMOS RF power amplifier, and (b) Die micrograph of our designed CMOS RF power amplifier	67
Fig. 4.9 Output transformer layout with ‘ideal’ center taps at the primary windings..	69
Fig. 4.10 Simulation structure for the bonding wires	70
Fig. 4.11 Multilevel design of the watt-level CMOS RF power amplifier	72
Fig. 4.12 Bonding wire diagram of the 32pin QFN (5mm x 5mm) package	73
Fig. 4.13 PCB photo of our designed RF power amplifier	75
Fig. 4.14 Output Power versus input power and PAE	76

Fig. 4.15 Gain versus input power	76
Fig. 4.16 The measured output spectrum of our designed CMOS RF power amplifier with 20MHz LTE QPSK signal	77
Fig. 4.17 The measured output spectrum of our designed CMOS RF power amplifier with 20MHz LTE 16QAM signal.....	78
Fig. 5.1 Comparison of power losses of the conventional linear power amplifier and the envelope tracking power amplifier	85

List of Tables

Table 2.1 Typical PAPR for wireless communication standards	16
Table 2.2 Summary of the input impedance and power-efficiency of SCT and PCT [24].....	26
Table 4.1 Two transformers (A and B) with the designed a_1 and real a_1 (including process variations)	61
Table 4.2 Benchmark of RF power amplifiers for the LTE application	79
Table 5.1 Comparison of III-V and CMOS process	84

List of Abbreviations

AC	Alternating Current
ADS	Advanced Design System
AMPS	Advanced Mobile Phone System
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
EER	Envelope Elimination And Restoration
EM	Electromagnetic
ESD	Electrostatic Discharge
ET	Envelope Tracking
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	Global System for Mobile Communication
HFSS	High Frequency Structure Simulator
IC	Integrated Circuit
InGaP	Indium Gallium Phosphide
InP	Indium Phosphide
LEES	Low Energy Electronic Systems
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMCAP	Metal-Insulator-Metal Capacitor
MOMCAP	Metal-Oxide-Metal Capacitor
NMT	Nordic Mobile Telephone
OD	Outer Diameter
OFDM	Orthogonal Frequency Division Multiplexing
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PCT	Parallel-Combining Transformer
PGS	Patterned Ground Shield
QAM	Quadrature Amplitude Modulation
QFN	Quad-Flat No-Leads

QPSK	Quadrature Phase-Shift Keying
RF	Radio Frequency
SCT	Series-Combining Transformer
SMART	Singapore-MIT Alliance for Research and Technology
SoC	System-on-Chip
TACS	Total Access Communication System
TDMA	Time-Division Multiple Access
VNA	Vector Network Analyzer
VSG	Vector Signal Generator
WCDMA	Wideband Code Division Multiplexing Access

Chapter 1 Introduction

1.1 Background and Motivations

Congruous with the rapid development of advanced wireless communication systems from low-speed 1G (AMPS/NMT/TACS) to the prevailing high-speed 4G [1] as depicted in Fig. 1.1, the demand for full integration of electronics continues to increase. To achieve high integration and low cost for a System-on-Chip (SoC), a full CMOS integration (vis-à-vis III-V semiconductors (e.g. GaN/GaAs/InP/InGaP) and CMOS in separate packages) is, at this juncture, the most effective solution.

Fig. 1.1 Wireless communication standards development

In a transceiver for wireless communications, the RF power amplifier is arguably one of the most challenging and important blocks because of the nuances in design

and its contribution to the overall power efficiency of the transceiver. The merits and shortcomings between CMOS and III-V technologies for the realization of RF power amplifiers are well established and discussed in the literature [2]. As mentioned earlier, since CMOS technology is advantageous in terms of lower cost and full integration, the RF power amplifier realization with CMOS processes remains very worthy in many applications. Nevertheless, when compared to their III-V counterparts, the CMOS RF power amplifier is disadvantageous in terms of reduced power-efficiency and linearity due to the low breakdown voltage and lossy substrate [3, 4] of CMOS processes.

To design a CMOS RF power amplifier, there are challenges pertaining to the power-efficiency and linearity, especially at high maximum output power. It is difficult to simultaneously improve the efficiency, linearity and maximum output power.

The maximum output power of a CMOS RF power amplifier is approximately 30dBm for advanced wireless communication standards like LTE. This power level is difficult in CMOS realization due to the low breakdown voltage of CMOS. Assuming that a sinusoidal signal with the peak-to-peak amplitude of V_{pp} is delivered to a load R from a CMOS RF power amplifier, the output power is expressed as Eqn. (1.1) [5].

$$P = \frac{(V_{pp}/2)^2}{2R} \quad (1.1)$$

In order to deliver one watt (~30dBm) output power to a 50Ω antenna, the peak amplitude of the output voltage of a CMOS RF power amplifier should be 10V and

this typically exceeds the maximum voltage limit of CMOS technology. To reduce the peak voltage experienced by CMOS output transistors, the power combining technique implemented by using on-chip transformers is widely applied [6-8]. However, the transformer is not an efficient device, especially in CMOS processes.

One of the most challenging aspects of the CMOS RF power amplifier design with respect to the high maximum output power is high power-efficiency. Because of the high maximum output power ($\sim 30\text{dBm}$), high currents are generated and flow through the CMOS RF power amplifier. These are some of the serious issues in the design of power amplifiers and the package. Specifically, the high currents increase the power losses in the transistor blocks, interconnect lines, transformers and bonding wires, which in turn affect the power-efficiency of the CMOS RF power amplifier. Moreover, the high current induces the thermal problem for the CMOS RF power amplifier design. The high temperature degrades the properties of CMOS devices, including mobility.

Due to the high peak-to-average power ratio (PAPR) of orthogonal frequency-division multiplexing (OFDM) modulation schemes for LTE applications, a large power back-off from the maximum output power is required. This is to avoid signal clipping and spectral spreading, which lowers the power-efficiency of the CMOS RF power amplifier. This results in a linearity-efficiency trade-off in the design of the CMOS RF power amplifier for LTE applications. In addition, the power combining transformer used for the high maximum output power may affect the linearity of the CMOS RF power amplifier.

In short, due to the need for low cost and full integration, the RF power amplifier realization in CMOS processes is a viable and effective solution for high-speed data transmissions, e.g., 4G LTE. Nevertheless, in order to achieve the high maximum output power for LTE applications, the design for high power-efficiency for the CMOS power amplifier with the high linearity and high maximum output power remains a major challenge. As their power-efficiency is relatively low, hence a serious impact on the reduced battery lifetime, there are strong incentives to investigate and design a watt level CMOS RF power amplifier with high power-efficiency. Such investigations are somewhat broad, including the design of on-chip layout, package, and PCB, in addition to the core power amplifier design.

1.2 Objectives and Scope

The overall objective of this MEng program is to design a power-efficient one-watt RF power amplifier based on the GF 65nm CMOS process for 4G LTE applications. The specific objectives are:

- (i) An investigation into loss mechanism of and design considerations for the transformer;
- (ii) An investigation into the influence of the non-ideal center tap on the transformer efficiency; and
- (iii) The investigation into the linearity and efficiency issues relating to watt-level CMOS RF power amplifiers, including chip layout, and package.

1.3 Contributions

The contributions of this MEng program pertain to the aforesaid objectives:

- (i) An analytical investigation into the substrate thickness effect on the transformer quality. The investigation reveals how the ultra-thin substrate affects the parasitic resistances, quality factor, coupling factor and power-efficiency of the transformer. This investigation is useful as it offers insights into optimization for the substrate thickness, including the trade-off between the performance of the related circuit devices and the thermal release;
- (ii) A derived analytical expression to depict the influence of the non-ideal center tap of the transformer, including the parasitic resistances between the non-ideal center tap and the real ground, and the process variations. Further, an output transformer is designed to eliminate the non-ideal center tap influence, thereby improves the power-efficiency of the CMOS RF power amplifier;
- (iii) Modeling of the bonding wires of the 32pin QFN (5mm x 5mm) package for the co-simulations of the CMOS RF power amplifier and the package. The bonding wire structure is designed and optimized to reduce the influence of the bonding wire, especially at the supply and ground nodes with high currents; and
- (iv) The design and monolithic realization of a one watt-level RF power amplifier for 4G LTE application using a commercial 65nm CMOS process.

On the basis of physical measurements, our designed CMOS RF power amplifier achieved 29.3dBm maximum output power and 17.29% PAE. The spectrum emission masks of 20MHz QPSK and 16QAM LTE signals are fulfilled at the 23dBm output power. When compared to the state-of-the-art, the power-efficiency is somewhat low. We attribute the low PAE to the insufficiently rigorous extraction and modeling of the wide and long metal lines. The further investigations and analysis are ongoing.

1.4 Organization

This thesis is organized in the following manner.

Chapter 1 presented the introduction and overview of this MEng program, including the motivations, objectives, and contributions.

Chapter 2 provides a comprehensive and critical literature review of RF power amplifiers, including the power amplifier fundamentals, power combining technique, and the transformer.

Chapter 3 investigates the substrate thickness influence on the transformer of the RF power amplifier.

In Chapter 4, a one watt RF power amplifier for 4G LTE applications is delineated, including the design, monolithic realization, and measurement results.

In Chapter 5, conclusions are drawn, and recommendations for future work are presented.

Chapter 2 Literature Review

This chapter provides a comprehensive literature review of the RF power amplifier and the transformer. Section 2.1 discusses the fundamentals of the RF power amplifier that includes gain, efficiency, linearity, and stability. A review of the RF power amplifier design is presented in Section 2.2, including the output stage and output matching network. Finally, since the transformer used for power combining is one of the most important blocks in the RF power amplifier design, its fundamentals, loss mechanisms, and lumped-element model are discussed in Section 2.3. Section 2.4 draws the conclusions.

2.1 Power Amplifier Fundamentals

In this section, the most important fundamental parameters such as gain, power efficiency, linearity, and stability that define largely the performance of an RF power amplifier are reviewed.

2.1.1 Gain

Gain is a definition of the ability to amplify the power or amplitude of an AC signal from the input port to the output port of a two-port network. This is typically the ratio of the output to input current (current gain), voltage (voltage gain), and power (power gain). In the field of audio and general amplifiers (e.g., the operational

amplifier), gain generally refers to the voltage gain. However, in the RF power amplifier, it refers to the power gain.

Unlike the current gain and voltage gain, the definition of power gain is somewhat ambiguous. There are three important definitions of the power gain of the RF power amplifier: the transducer power gain, operating power gain, and available power gain [9, 10].

To define power gain, we consider how the power flows at the input and output sides of an RF power amplifier. The power flow diagram of an RF power amplifier is illustrated in Fig. 2.1, which indicates the power transmission and reflection at the input and output interfaces. The input and output power are indicated by P_{IN} and P_L , respectively. P_{AVS} represents the available power generated from the input source, while P_{AVN} is the available power generated from the power amplifier. If the input or output impedance of the power amplifier is not conjugately matched to the source or load impedance, the reflected powers (P_{r1} and P_{r2}) are undesirably produced at the input and output interfaces.

Fig. 2.1 Power flow diagram of an RF power amplifier [9]

The three important power gains mentioned earlier can be defined by the incident, transmitted and reflected powers at the input and output interfaces, as expressed in Eqns. (2.1) - (2.3) [11].

Transducer Power Gain

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_S \Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22} \Gamma_L|^2} \quad (2.1)$$

Operating Power Gain

$$G_P = \frac{P_L}{P_{IN}} = \frac{1}{1 - |\Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22} \Gamma_L|^2} \quad (2.2)$$

Available Power Gain

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11} \Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_L|^2} \quad (2.3)$$

where Γ_S is voltage reflection coefficient at source,

Γ_L is voltage reflection coefficient at load,

Γ_{IN} is voltage reflection coefficient at the input of the two-port network,

S_{11} is the ratio of reflected and incident waves at the input interface

when the reflected wave from the load is zero, and

S_{22} is the ratio of reflected and incident waves at the output interface

when the reflected wave from the source resistance is zero.

The transducer power gain takes into account the mismatches at the input and output interfaces, where the gain measured of an RF power amplifier usually refers to the transducer power gain. The operating power gain, on the other hand, takes into account the mismatch at the output interface. It is applicable to high power amplifiers that need to optimize the output impedance to achieve a high output power. Finally, the available power gain takes into account the mismatch at the input interface and is used for low-noise amplifiers that need to optimize the input matching network for low-noise performance.

2.1.2 Power-Efficiency

Power-efficiency is a measure of the effectiveness of an RF power amplifier to convert the DC supply power and RF input power to the output power. This is often defined as the drain efficiency or power-added efficiency (PAE).

The drain efficiency of an RF power amplifier is defined as the ratio of the output power P_{OUT} to the DC power P_{DC} , as expressed in Eqn. (2.4) [5].

$$\eta = \frac{P_{OUT}}{P_{DC}} \quad (2.4)$$

Aside from the drain efficiency, a more common power-efficiency index is usually employed. This power-efficiency index, PAE [5], is expressed as:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (2.5)$$

where P_{IN} is the average input power.

For an RF power amplifier with infinite power gain, the PAE equals to the drain efficiency. In practice, the PAE is however always less than the drain efficiency.

RF power amplifiers are classified either as a switching power amplifier or a linear power amplifier based on their output characteristics. The switching power amplifier has higher power-efficiency, but with poor linearity. Conversely, the power-efficiency of the linear power amplifier is relatively low, but its linearity is high.

2.1.3 Linearity

Linearity is a specification on the signal fidelity that can be maintained by an RF power amplifier. The linearity of the RF power amplifier can be defined in terms of the 1-dB compression point (P_{1dB}), the third-order intercept point (IP_3), and the third-order intermodulation distortion (IMD_3).

P_{1dB} is measured by means of the single-tone testing at the fundamental frequency. In the single-tone measurement, an RF signal with a fundamental frequency generated by a vector signal generator (VSG) is applied to the input of an RF power amplifier. The output power versus the input power obtained at the fundamental frequency is depicted in Fig. 2.2 [12]. At low output power level, the

curve of the output power versus the input power is linear. However, due to the nonlinear effects at the high output power level, this curve is compressed. P_{1dB} is defined as the point where the output power deviates by 1dB from the straight line. The higher the magnitude of P_{1dB} , the more linear is the RF power amplifier.

When two RF signals with frequencies ω_1 and ω_2 are applied to the input of an RF power amplifier, i.e., two-tone measurements, these RF two signals are mixed. Due to the non-linearity of the RF power amplifier, intermodulation products (IM_n) comprising power products at different frequencies are produced. This is depicted in Fig. 2.3 [12]. The third-order intermodulation products (IM_3) are located at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, and as they are very close to the fundamental frequencies and cannot be filtered out. If the magnitudes of IM_3 are too large, the signal fidelity may be compromised. IMD_3 is defined as the difference between the power of the fundamental and IM_3 products as depicted in Fig. 2.3. Note that, IMD_3 is not a fixed value but varies with the output power at the fundamental frequency. Consequently, IP_3 is a fixed point for an RF power amplifier. In Fig. 2.2, IP_3 is the intercept point of the fundamental and IM_3 lines.

Fig. 2.2 P_{OUT} versus P_{IN} for RF power amplifier indicating P_{1dB} and IP_3 [12]

Fig. 2.3 Intermodulation products in the two-tone measurement [12]

2.1.4 Stability

The RF power amplifier may become an oscillator if it is not stable, particularly when the power amplifier embodies a very high gain. The oscillation may occur at the frequency related to or unrelated to the fundamental frequency. A commonly used specification for stability characteristics based on S -parameters is the stability factor (K) [13-15] defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (2.6)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (2.7)$$

If K is greater than one and Δ is less than one, the RF power amplifier is unconditionally stable with any combination of the input and output impedances. For the watt-level RF power amplifier design, care must be taken to ensure that it is unconditionally stable. It requires S_{12} to be small for high gain (high S_{21}).

2.2 RF Power Amplifier Design

The majority of RF power amplifiers employs two stages with three matching networks. These matching networks are placed at the RF input, between the two stages, and at the RF output as depicted in Fig. 2.4.

Fig. 2.4 Block diagram of a typical two-stage RF power amplifier

The driver interposed between the input matching network and inter-stage matching network can be treated as a buffer, which provides a sufficient gain for the RF power amplifier with the high output power. For example, for the output power 30dBm, the RF power amplifier needs sufficient gain of 25~30dB because the RF power amplifier input power (or the output power of the upconverter) is usually around 0~5dBm. Moreover, due to the number of transistors in the output stage, a high parasitic capacitance exists at the input of the output stage, which requires a buffer placed before the output stage.

The input matching network is used to allow the standard input impedance 50Ω and serves as a balun in order to convert the single-ended input signal to the differential output signals. The output matching network amplifies the voltage swing to the load and converts the differential input signals to the single-ended output signal. The inter-stage matching network is used to match the input impedance that is required for the output stage in order to maximize the power efficiency.

There are several wireless communication standards. For LTE applications, an RF power amplifier with watt-level output power is required due to several reasons. First, the maximum output power specified for LTE applications is 23dBm. The designed

RF power amplifier should fulfill the spectrum emission mask at 23dBm output power (measured as the average band power). Secondly, the LTE systems provide high data rates, requiring a high maximum output power in order to prevent compression. This results in a high PAPR, 6~7dB as shown in Table 2.1[16].

Table 2.1 Typical PAPR for wireless communication standards

Wireless Communication Standards	GSM	TDMA	WCDMA	LTE
Typical PAPR	1.5dB	3.5dB	8-9dB	6~7dB

In short, due to the high PAPR (6~7dB), the maximum output power of an RF power amplifier is required to be 6~7dB higher than the average output power (23dBm) for LTE applications, which is 29~30dBm. Put simply, an RF power amplifier with one-watt output power is required for LTE applications.

We will now review the output stage and the output transformer network, the most critical blocks for the high power RF power amplifier.

2.2.1 Output Stage

The output stage of watt-level power RF power amplifiers consists of several power cells. This is because one power cell is unable to provide watt-level output power due to the low impedance at the output port and the CMOS low breakdown voltage. The differential structure is usually used for the power cells. In the design of

the output stage for high power applications, the critical issues include high current, noise, and bias voltage.

Because of the high maximum output power required, the currents in the power cells are high and this leads the thermal problem. To accommodate the thermal problem, it is necessary to maintain sufficient space between the multiple cells [17] in the layout. Other efforts [17] include the design of the gate width and the unit finger size of the power cells. The large gate resistance causes non-uniform current distribution because of the large width of output transistors required for the high maximum output power.

A reported investigation [18] has shown that the substrate noise coupling between the power cells and transformers may affect the stability of RF power amplifiers, especially when the maximum output power of the RF power amplifier is high. To reduce the substrate noise coupling in the RF circuits, the substrate isolation techniques are reportedly employed. These common isolation techniques include the guard ring [19], deep N-well [20], deep trench isolation [21] and high resistive substrate [22]. However, the deep trench isolation and high resistive substrate are difficult to be implemented or unrealizable in CMOS processes. The deep N-well and guard ring, on the other hand, are applicable for CMOS, where the deep N-well is placed under the circuits and the guard ring surrounds the devices and is connected to the AC ground. By providing a short current path for the noise, the noise blocked by a blocking region is generally highly effective.

To achieve the high maximum output power, the output transistors are designed with a large width. This, however, affects the linearity of RF power amplifiers

because of the induced large transconductance, output conductance, gate-source capacitance, and drain junction capacitance. A reported investigation [17] depicted the relationship between the bias voltage and these nonlinear parameters, providing a means of optimum high linearity.

2.2.2 Output Matching Network

The output matching network serves to transform a low impedance R_A , seen by the power amplifiers, to a high output impedance R_L (normally 50Ω). The impedance transformation ratio r is defined in Eqn. (2.8) [8] below.

$$r = \frac{R_L}{R_A} \quad (2.8)$$

One of the most common transformation networks is the LC -matching network using L -match, T -match or π -match. However, for the high impedance transformation ratio, this type of network wastes a lot of power [8], especially at watt-level output power.

To solve this problem, the reported [23-27] power combining technique is widely applied in the output matching network. This is often achieved by LC baluns or transformers.

Power Combining Technique with LC Baluns

The LC balun is implemented with two LC -matching networks. This structure reduces the power loss by combining several power amplifier cells in parallel with the on-chip LC balun, such as that depicted in Fig. 2.5 [28]. In this structure, the differential power amplifier structure is used and combined with LC baluns.

The impedance transformation ratio of this structure [28] is

$$r = \frac{R_L}{R_A} = 2 \cdot N \cdot \left(\frac{R_L}{B} \right)^2 \quad (2.9)$$

$$B = \omega L = \frac{1}{\omega C} \quad (2.10)$$

where N denotes the number of differential power cells.

Fig. 2.5 Power combining technique with LC baluns [28]

From Eqn. (2.9), we observe that the impedance transformation ratio depends on the ratio of the output impedance (50Ω) to the inductor/capacitor impedance. However, the inductor/capacitor impedance may change due to process variations, resulting in a change of the impedance transformation ratio for a fixed output impedance. In general, the impedance transformation ratio should not depend on any absolute device value to eliminate the influence of process variations.

Power Combining Technique with Transformers

For the power combining technique realization [23-27], the transformer generally provides a solution [24]. Compared to the LC -matching network, the transformer stores less energy for a given quality factor, which in turn results in low power loss. Moreover, the impedance transformation ratio of a transformer does not depend on any absolute value of the devices but, instead, depends on the turn ratio which is unaffected by process variations. Fig. 2.6 depicts a simple model of an ideal transformer, where N_1 and N_2 are the numbers of turns of the primary and secondary windings, respectively. This transformer transforms the input impedance R_A to the load R_L .

Fig. 2.6 Simple model of an ideal transformer

The turn ratio (a) of a transformer is defined in Eqn. (2.11). From Eqn. (2.8) and Eqn. (2.11), it can be seen that the impedance transformation ratio of a transformer is equal to the square of the turn ratio - a ratio instead of an absolute value of devices. Practically, this means that in the layout, the number of turns of each transformer

winding can be matched akin to transistor layout matching in analog design, resulting in an accurate impedance transformation ratio.

$$a = \frac{N_2}{N_1} = \sqrt{\frac{R_L}{R_A}} \quad (2.11)$$

The well-established power combining structure by means of the on-chip transformer is depicted in Fig. 2.7. In this structure, the transformer is used to combine several power cells at the primary winding to generate a watt-level output power at the secondary winding.

The first watt-level CMOS RF power amplifier implementation [29] with an integrated transformer was probably the 2.4-GHz, 2.2-W CMOS power amplifier based on a 0.35 μm CMOS process. This power amplifier achieved 31% PAE for the 2V supply voltage. More recently, CMOS RF power amplifiers featuring a saturated output power of >30dBm with a PAE of more than 30% [6, 7, 30] were reported.

Fig. 2.7 Power combining technique with transformers

The transformer combination structure has significant influence on the performance of the transformer, which in turn affects the overall linearity and efficiency of the RF power amplifier. There are two types of transformers [24] with different combination structures: series-combining transformer (SCT) and parallel-combining transformer (PCT).

The structures of these two combinations [24] are shown in Fig. 2.8, where the number of the power cells is indicated by M . In our following comments, we assume that the power cells are identical, i.e., the input voltages to the transformers are same, represented as V_1 . The output voltage at the secondary winding is indicated as V_2 . The R_1 and R_2 are the parasitic resistances of the primary and secondary windings, respectively.

Fig. 2.8 (a) Series-combining transformer (SCT), and (b) Parallel-combining transformer (PCT) [24]

- Series-Combining Transformer (SCT)

Fig. 2.8 (a) depicts the transformer equivalent circuit of the series combination structure [31]. The secondary winding is connected in series. The AC voltages at the secondary winding are added up to achieve a high output power for a fixed load

resistance. By controlling the transformer turn ratio, a very low voltage can be applied to the primary winding. The advantage of this structure is that each of the power stages can operate separately and be turned off in the low power mode for improving the power efficiency [32]. However, this transformer requires a relatively large area when four (or more) power cells are combined [23]. Further, the secondary winding with a high number of power cells has high parasitic resistance, which results in a high loss. During design, attention is necessary to ensure that the layout is symmetrical. Any mismatch in the layout can affect the power amplifier efficiency and linearity.

- Parallel-Combining Transformer (PCT)

Fig. 2.8 (b) depicts the parallel combination structure of a transformer where all the primary windings are magnetically coupled to the same secondary winding. The currents are added at the secondary winding to achieve high output power. The parallel combination structure yields lower loss at the secondary winding and provides better signal symmetry [33]. However, the parallel combination structure needs a high turn ratio for the same output impedance when compared with the series combination transformer [30].

Table 2.2 Summary of the input impedance and power-efficiency of SCT and PCT [24]

Transformer Type	SCT	PCT
R_{in}	$R_1 + \frac{1}{M} \left(\frac{N_1}{N_2} \right)^2 (R_2 + R_L)$	$R_1 + M \left(\frac{N_1}{N_2} \right)^2 (R_2 + R_L)$
η	$\frac{1}{1 + \left[M \left(\frac{N_2}{N_1} \right)^2 R_1 + R_2 \right] / R_L}$	$\frac{1}{1 + \left[\frac{1}{M} \left(\frac{N_2}{N_1} \right)^2 R_1 + R_2 \right] / R_L}$

Table 2.2 [24] tabulates a summary of the input impedance and power-efficiency of SCT and PCT. For the same parasitic resistances, load impedance and turn ratio, SCT is more advantageous because the input impedance to the transformer is reduced by increasing the number of combined power cells. On the other hand, for the same input impedance R_{in} , parasitic resistances and load impedance, SCT needs a low turn ratio compared to PCT.

In terms of transformer power-efficiency, PCT is conversely advantageous if the number of the power cells combined increases. However, the large number of power cells increases the parasitic resistances, which in turn is disadvantageous as the power loss increases.

In this project, the series combination structure of the transformer is investigated and applied to achieve the watt-level output power; See Chapter 4 later.

2.3 Transformer

The on-chip transformer is widely applied in low noise amplifiers (LNAs), oscillators and RF power amplifiers. This is because, for the high impedance transformation ratio, the on-chip transformer is well suited for impedance matching networks due to its low insertion loss compared to *LC*-ladder based circuits. Moreover, the impedance transformer ratio of the transformer is independent of process variations as mentioned in Section 2.2 earlier.

We will now review the on-chip transformer. This section initiates with a general review of the layout parameters which affect the performance of a transformer and this provides a guideline for the design of the transformer. Thereafter, the loss mechanisms of a transformer are reviewed, including the metal and the substrate losses. Finally, the lumped-element model of a transformer is reviewed.

2.3.1 Layout Parameters

The layout parameters [34] which affect the performance of the transformer includes the transformer structure, turn ratio (a), metal spacing (S), metal width (W), metal thickness (d) and the outer diameter (OD). These are depicted in Fig. 2.9.

Fig. 2.9 Layout parameters of a 2-to-3 transformer

There are two common types of the transformer structure: stacked and interleaved structure. The stacked transformer embodies two identical metal windings. These two windings (primary and secondary windings) use different metal layers with one on the top of the other. Due to the small space between the two adjacent metal layers, the coupling factor of the stacked transformer is high while the parasitic capacitance increases.

The interleaved transformer, on the other hand, uses the same metal layer. The primary and secondary windings are laterally interleaved. The space between these

two windings is larger than two adjacent metal layers' space, resulting in poorer coupling compared with the stacked transformer. However, the interleaved structure achieves high symmetry, which minimizes the phase difference between differential signals.

The effects of layout parameters to the transformer are well established [35-38]. The outer diameter of a transformer is a very important parameter, which determines the transformer size and the overall performance. If the outer diameter is reduced with a fixed transformer winding length, the inner diameter is changed and affects the performance of the transformer windings. For a small inner diameter, the inner turns of the transformer winding are affected by the induced electromagnetic field, which generates an eddy current inside the inner turns. This results in a non-uniform current flow and increases the parasitic resistance, which in turn decreases the quality factor [39, 40]. Consequently, the inner diameter should be carefully designed to get an 'optimum' outer diameter for a fixed metal width of each transformer winding [41]. When the inner diameter increases from a small value to the 'optimum' value, the parasitic resistance of the transformer winding decreases, resulting in improving quality factor.

It has been reported [41] that the metal width affects the transformer winding inductance of per unit value, parasitic resistance, and the frequency of the peak quality factor. The metal width would need to be carefully designed to ensure that the operating frequency is equal to the frequency of the peak quality factor.

The coupling factor [41] is significantly affected by the metal spacing between the primary and secondary windings. The metal spacing is usually designed to the closest

value allowed by the process design rule. Although a smaller metal spacing means higher coupling capacitance, it may be negligible compared to the parasitic capacitance between the transformer and the substrate.

The impedance transformation ratio of the transformer depends on the turn ratio as discussed in Section 2.2. The turn ratio of an on-chip transformer cannot be too large, because a large turn ratio causes other problems, including low self-resonant frequency [42] and reduced power-efficiency of the transformer (Table 2.1). The metal thickness of transformer windings can be increased by stacking multiple layers together in order to enhance the coupling factor of the on-chip transformer and the transformer winding quality factor.

2.3.2 Loss Mechanisms

For integrated and inductive devices such as the on-chip transformer fabricated in CMOS process, the primary challenge is how the power loss can be minimized. This includes maximizing the quality factor (Q) for a given inductance (L). The power loss of an on-chip transformer is largely due to the effective resistances (R) of the primary and secondary windings and the substrate.

There are two types of metal loss mechanisms related to the effective resistances of the primary and secondary windings - the skin effect and the proximity effect.

The skin effect [38] takes place when a time-varying current flows through a metal line. A magnetic field is induced in and out of this metal line. The change of the induced magnetic field creates an electric field, which is strong at the center of the

metal line. This electric field pushes the electrons to the outside boundary from the center of the metal line. This phenomenon nonuniformly distributes the electrons in the metal line and decreases the effective conducting area, which in turn increases the effective resistance. The skin effect is qualified by the skin depth - the thickness where the current density is reduced to 37% and where most (63%) of the electrons flow between the metal boundary and the skin depth. The skin depth is frequency-dependent as expressed in Eqn. (2.12) [5].

$$\delta = \sqrt{\frac{1}{\mu \cdot \sigma \cdot \pi f}} \quad (2.12)$$

where μ is the permeability,

σ is the conductivity, and

f is the frequency.

With increased operating frequency, the effective resistances of the primary and secondary windings will increase due to the skin effect, i.e., the effective resistance is frequency-dependent and higher than the DC resistance. The effective resistances at DC and AC conditions (R_{DC} and R_{AC}) are expressed in Eqns. (2.13) and (2.14) [34], respectively.

$$R_{DC} = \frac{\rho l}{wd} \quad (2.13)$$

$$R_{AC} = \frac{\rho l}{w\delta \left(1 - \exp\left(\frac{-d}{\delta}\right)\right)} \quad (2.14)$$

where ρ is the resistivity,

l is the length of the wire,

w is the width of the wire, and

d is the thickness of the wire.

Because of the skin effect, edge mesh [43] is widely adopted in electromagnetic (EM) simulation tools, e.g., ADS [44] and HFSS [45] tools. The edge mesh provides relatively accurate simulation results because it increases the mesh density between the skin depth and the boundary of metal lines. As most of the electrons are flowing between the skin depth and the boundary of metal lines at high frequencies, the edge mesh applied to the metal lines is efficient and accurate.

To reduce the effective resistances of the primary and secondary windings, the top thick metal layers of the CMOS process are typically used in the design of the signal lines and transformers. This is because the top metal layers are thicker than the low metal layers, hence less resistance.

Another type of metal loss mechanisms is the proximity effect, which occurs when the two conducting metal lines A and B are too close to each other. With time-varying current flowing through an adjacent conducting metal line B , a magnetic field

is induced. The induced time-varying magnetic field generates an eddy current in the conducting metal line A . This eddy current, in turn, reduces the current in this conducting metal line A and increases its effective resistance.

To mitigate the skin effect and the proximity effect, the layout design of the transformer needs careful attention, particularly if a transformer with high efficiency is to be designed.

Besides metal losses in metal windings, the substrate also affects the power loss of the transformer. This is due to the electromagnetic coupling between the transformer metal windings and the substrate. In CMOS processes, the transformer suffers from silicon substrate loss due to the high substrate conductivity [46]. The silicon substrate has a pronounced effect on the quality factor and the mutual resistive coupling factor of the primary and secondary windings, which degrades the maximum available gain of a transformer. At low frequencies, the magnetic and electric field magnitudes are low in the substrate, thereby contributing little to the overall losses. At high frequencies, on the other hand, the substrate losses are large, and comparable with the metal losses of the metal windings. The influence of the substrate loss due to electric and magnetic fields on the characteristics of a transformer is well established and are depicted in Fig. 2.10 [47].

The mechanism of these losses are well established when a time-varying current passes through a metal line, it generates a time-varying magnetic field and an electric field. This time-varying magnetic field penetrates the substrate and induces an eddy current. The eddy current flows through the substrate and results in power losses.

Fig. 2.10 Magnetic field and electric field distribution in the substrate [47]

In order to reduce the substrate loss, different types of Patterned Ground Shield (PGS) layout structures have been reported [47-50]. In CMOS processes, the distance between the metal lines of a transformer and the substrate is small compared with the wavelength of high-frequency signals. Consequently, the transformer can be considered as a near-field source. However, the magnetic field of the near-field source cannot be effectively shielded by PGS at frequencies below 10GHz. In this situation, the dominant shield mechanism is the absorption loss which takes effect only when the metal thickness is much thicker than the skin depth [51].

The electric field of the near-field source can be effectively shielded by PGS. The electric field is mainly reflected in this situation due to the impedance mismatch between the boundary of silicon and PGS.

If the conductivity of a silicon substrate is not too high, the ensuing losses are mainly caused by the electric field, which can be shielded by PGS. Due to the loss reduction with the PGS shield, the quality factor of the transformer windings is improved.

2.3.3 Lumped-Element Model

There is substantial reported literature to characterize a transformer, including extraction and curve fitting from S -parameters or from EM simulations. However, as accurate calibrations and simulations take an extended long time, scalable lumped element models are often employed to facilitate fast simulations and circuit optimizations [35, 52, 53]. For accuracy, the skin effect and substrate loss mechanisms are reportedly included in this model.

A transformer is formed by the coupling of two inductors. Each inductor can be modeled by a simple π -network as depicted in Fig. 2.11, including the parasitic resistance (R), inductance (L) and substrate network. The substrate network is composed of oxide dielectric capacitors (C_{ox1} and C_{ox2}) modeled as the parasitic capacitances between the metal windings and the substrate, and the substrate parasitic capacitors (C_{sub}) and resistors (R_{sub}).

Fig. 2.11 The π -network of an inductor [38]

The inductance (L) and the resistance (R) of metal windings that can be extracted by Y -parameters are expressed in the Eqns. (2.15) and (2.16) [41], respectively. To minimize the power loss, the quality factor (Q), as expressed in Eqn. (2.17) [41], should be maximized.

$$L = \frac{\text{Imag}(1/Y_{11})}{2\pi f} \quad (2.15)$$

$$R = \text{Real}(-1/Y_{11}) \quad (2.16)$$

$$Q = \frac{\text{Imag}(1/Y_{11})}{\text{Real}(1/Y_{11})} \quad (2.17)$$

Using the π -network model and taking into consideration the coupling between two windings, the lumped-element model of a transformer is depicted in Fig. 2.12 [35, 52, 54]. This model includes the parasitic elements of metal windings, the coupling model between the primary and secondary windings, and the substrate network. The parasitic elements of the transformer's primary and secondary windings are represented as resistors (R_p and R_s) and inductors (L_p and L_s). The coupling between the primary and secondary windings is modeled by the coupling capacitors (C_{p1} and C_{p2}) and the coupling factor (K) between two transformer windings. The substrate network is modeled by the oxide dielectric capacitors (C_{ox1} and C_{ox2}), the substrate capacitors (C_{sub}) and the substrate resistors (R_{sub}). The substrate loss is directly related to the substrate network, which affects the power-efficiency of the transformer.

Fig. 2.12 The lumped-element model of a transformer [35, 52, 54]

The energy of a transformer is transformed through the magnetic coupling between the primary and secondary windings. The coupling factor (K) indicates how much energy is transformed from the primary winding to the secondary winding, and can be extracted from Z -parameters as expressed in Eqn. (2.18) [55]. In an ideal transformer, the energy is fully transformed from the primary winding to the secondary winding, which means the coupling factor is equal to one.

$$K = \sqrt{\frac{\text{imag}(Z_{12}) * \text{imag}(Z_{21})}{\text{imag}(Z_{11}) * \text{imag}(Z_{22})}} \quad (2.18)$$

2.4 Conclusions

In this chapter, an RF power amplifier fundamentals have been reviewed, including its gain, power-efficiency, linearity, and stability. For the watt-level RF power amplifier design, the output stage and output matching network have been reviewed with emphasis on the power-combining technique implemented with LC baluns and transformers (SCT and PCT) in the output matching network. In this project, the SCT is used as the output transformer. As the transformer is a critical component for the power combining technique realization, its fundamentals, loss mechanisms, and lumped-element model to achieve a high performance such as low parasitic elements and high power-efficiency have been reviewed.

Chapter 3 Substrate Thickness Effect on the Transformer

3.1 Introduction

One of the most important design issues of the one-watt level RF power amplifier is the inevitable temperature increase due to its high power loss. The temperature affects the electrical properties of both the devices and signal paths, and particularly the transistor properties, such as the carrier mobility and the threshold voltage [56].

The simplest way to mitigate the thermal effect on the performance of the RF power amplifier is to employ a thin substrate [57] for its improved thermal conductivity. Nevertheless, a potential drawback of the ultra-thin substrate is that the performance of the circuit components may degrade if the electromagnetic field distribution in the substrate is changed. For instance, the RF transformer may suffer from reduced quality factor (Q) and reduced coupling coefficient (K). This results in reduced power-efficiency of the transformer and consequently the overall power-efficiency of the system embodying the transformer is reduced, i.e., the overall power dissipation is increased [8, 26, 58-60]. Put simply, the substrate thickness should be reduced without affecting the performance of the transformer.

In this chapter, the effects of the substrate thickness on the performance of a transformer for an RF power amplifier are analyzed.

3.2 Transformer with Different Substrate Thicknesses

As reviewed in Chapter 2, there are two common types of transformer structures [42] - interleaved and stacked transformer. With a smaller space between the primary and secondary windings, the stacked transformer has a higher mutual coupling factor than the interleaved transformer. However, as the stacked transformer has a smaller primary-to-secondary space, the parasitic capacitance is higher, which in turn decreases the self-resonant frequency. Further, for watt-level power amplifier applications, wide metals are required to withstand high currents. This further increases the coupling area between the primary and secondary windings, resulting in higher parasitic capacitance. Consequently, despite the lower mutual coupling of the interleaved structure [6], it is the preferred choice over the stacked transformer.

We design a symmetric and interleaved transformer depicted in Fig. 3.1 to investigate the substrate thickness effects on the performance of the transformer. This design is based on a commercial 65nm CMOS technology with a default substrate thickness of $737\mu\text{m}$ and resistivity of $1.499\Omega\cdot\text{cm}$. Three top metal layers EA, OI, and LB are stacked together to reduce the metal resistances. The metal width of both primary and secondary windings is $6\mu\text{m}$, the space between them is $2\mu\text{m}$, and the outer dimension is $275\mu\text{m} \times 275\mu\text{m}$ with a turn ratio 3:3. Fig. 3.2 shows the cross-section substrate structure of the commercial 65nm CMOS technology employed, including metal layers (M1-M6, EA, OI, and LB) and vias (V1-V5, NT, JQ, and VV). The substrate thickness is denoted as T_{sub} whose default value is $737\mu\text{m}$.

Fig. 3.1 The 3D view of a 3-to-3 interleaved transformer

Fig. 3.2 Cross-section substrate structure of the commercial 65nm CMOS technology

3.3 Simulation Results

This interleaved transformer with different substrate thicknesses T_{sub} (10 μm , 50 μm , 100 μm , 200 μm , 500 μm , and 737 μm) is simulated using Agilent's Advanced Design System (ADS) 2012 [61]. The results are obtained by the One-Port simulation and Two-Port simulation.

One-Port Simulation

The one-port simulation was employed to acquire the Y_{11} parameters of the primary and secondary windings. The simulations were completed from 10MHz to 10GHz. The inductance, parasitic resistance and quality factor of the primary and secondary windings, as depicted in Fig. 3.3 - Fig. 3.5 respectively, were subsequently extracted from the Y_{11} parameters based on Eqns. (2.15) - (2.17) after the one-port simulation.

On the basis of Fig. 3.3(a) and Fig. 3.3(b), we make the following comments. The self-resonant frequency, as expected, is influenced by the overall inductance including the mutual inductance between the primary winding and the substrate, and the self-inductance. At the default substrate thickness of 737 μm , Fig. 3.3(a) depicts the inductance of the primary winding (L_p) is 3.5nH with a self-resonant frequency 5.6GHz. For the substrate thicknesses of 100 μm , 200 μm , 500 μm , and 737 μm , the self-resonant frequency is largely the same, which means the substrate thickness reduction shows little effect in the same range of 100 μm to 737 μm . However, for 10 μm and 50 μm substrate thickness, the self-resonant frequency shifts to a high frequency, which indicates that the overall inductance decreases when the substrate

thickness is reduced. At a 10 μm substrate thickness, the influence is very significant which affects not only the self-frequency but also the primary winding inductance.

(a)

(b)

Fig. 3.3 Simulation results at different substrate thicknesses for (a) the primary winding inductance L_p , and (b) the secondary winding inductance L_s

On the basis of Fig. 3.4(a) and Fig. 3.4(b), we make the following comments. The primary winding resistance (R_p) is 4.5Ω at low frequencies for the default substrate thickness of $737\mu\text{m}$; see Fig. 3.4(a). With increasing frequency, the resistance increases due to the skin effect as described in Section 2.3. When the substrate thickness changes from $100\mu\text{m}$ to $737\mu\text{m}$, the resistance versus frequency curves of these substrate thicknesses is almost the same. This means the thickness effect for this range of substrate thicknesses can be ignored. However, the curve changes noticeably when the substrate thickness is reduced to $50\mu\text{m}$ or less.

(a)

(b)

Fig. 3.4 Simulation results at different substrate thicknesses for (a) the primary winding resistance R_p , and (b) the secondary winding resistance R_s

As discussed in Chapter 2, the quality factor (Q_p) is an important figure of merit for the inductor (primary and secondary windings) of the transformer, where the higher the quality factor, the lesser the loss. On the basis of Fig. 3.5(a) and Fig. 3.5(b), we make the following comments. The maximum quality factor of the primary winding is 6 at 2.3GHz for the substrate thickness of 100 μm , 200 μm , 500 μm , and 737 μm , see Fig. 3.5(a). The maximum quality factor degrades when the substrate thickness is 50 μm or less. At 10 μm substrate thickness, the maximum quality factor is reduced to 4 and the frequency at the maximum quality factor shifts to 4GHz. Although the metal loss is reduced because of low resistance for 10 μm substrate, the magnetic energy dissipation in the substrate is increased which decreases the quality factor.

(a)

(b)

Fig. 3.5 Simulation results at different substrate thicknesses for (a) the primary winding quality factor Q_p , and (b) the secondary winding quality factor Q_s

Fig. 3.3(b) - Fig. 3.5(b) depict the simulation results at various substrate thicknesses of the secondary winding for the inductance (L_s), resistance (R_s) and quality factor (Q_s). The substrate thickness effect on the inductance, resistance and quality factor of the secondary winding is largely the same as the effect on the primary winding. This is inferred by comparing the simulation results of Fig. 3.3(b) - Fig. 3.5(b) to Fig. 3.3(a) - Fig. 3.5(a).

Two-Port Simulation

The two-port simulation was employed to acquire Z-parameters of the transformer. The simulations were completed from 10MHz to 10GHz. The coupling factor (K) between the primary and secondary windings, as depicted in Fig. 3.6, was subsequently extracted from Z-parameters based on Eqn. (2.18) after the two-port simulation.

On the basis of Fig. 3.6, we make the following comments. The coupling factor is ~ 0.9 for this transformer at low frequencies, depicting good coupling between the primary and secondary windings. A high coupling factor indicates a good power transformation from the primary winding to the secondary winding. The coupling factor is largely the same for the substrate thickness of 50 μm , 100 μm , 200 μm , 500 μm , and 737 μm . However, the coupling factor reduces to 0.8 when the substrate thickness reduces to 10 μm . This is not unexpected because when the substrate thickness reduces, the magnetic loss in the substrate increases. This in turn decreases the magnetic energy transformed from the primary winding to the secondary winding.

Fig. 3.6 Simulation results of the coupling factor K for different substrate thicknesses

With the quality factors of primary and secondary windings extracted by the one-port simulation (Fig. 3.5) and the coupling factor extracted by the two-port simulation (Fig. 3.6), the maximum power-efficiency of the transformer, as depicted in Fig. 3.7, is obtained based on Eqn. (3.1) [4]. On the basis of Fig. 3.7, we make the following comments. For the default substrate thickness ($737\mu\text{m}$), the maximum power-efficiency is 70% at 2GHz. This maximum power-efficiency is largely the same for the substrate thickness of $100\mu\text{m}$, $200\mu\text{m}$, and $500\mu\text{m}$. However, for the $50\mu\text{m}$ and $10\mu\text{m}$ substrate thicknesses, the maximum power-efficiency of the transformer at 2GHz frequency degrade to 68.6% and 50%, respectively. This is expected because of the degradation of the quality factor and the coupling factor (Fig. 3.5 and Fig. 3.6), which in turn significantly reduces the maximum power-efficiency of the transformer (Eqn. (3.1)) for a thin substrate thickness such as $10\mu\text{m}$ or $50\mu\text{m}$.

$$\eta_{max} = \frac{1}{1 + \frac{2}{Q_p Q_s K^2} + 2 \sqrt{\frac{1}{Q_p Q_s K^2} \left(1 + \frac{1}{Q_p Q_s K^2}\right)}} \quad (3.1)$$

Fig. 3.7 Maximum power-efficiency η_{max} of transformer for different substrate thicknesses

In the view of our investigations above, the inductance, the resistance, the quality factor, the coupling factor and the maximum power-efficiency are not affected when the substrate thickness is in the range of 100 μm to 737 μm for the 65nm CMOS process. For thermal dissipation considerations, a suitable substrate thickness should be chosen without affecting the transformer performance.

Commercial foundries typically provide substrate thickness options, including that for the 65 μm CMOS process. In our design based on the 65nm CMOS fabrication, the 11mil (279.4 μm) thickness is selected – this is within the range described above where the performance of the transformer should be unaffected.

3.4 Conclusions

To investigate the substrate thickness effects on the transformer performance, we have designed a symmetric and interleaved transformer with the metal width of 6 μm , the space of 2 μm , and the *OD* of 275 μm . This transformer was simulated for different substrate thicknesses within a frequency range of 10MHz to 10GHz. We have shown that the inductance, the resistance, the quality factor, the coupling factor and the maximum power-efficiency are not affected when the substrate thickness is in the range of 100 μm to 737 μm . This provides a guideline for us to optimize the substrate thickness for the thermal release without affecting the transformer performance.

Chapter 4 Design of a One-Watt RF Power Amplifier

4.1 Introduction

Following our investigations into the transformer in Chapter 3, this chapter presents a fully integrated CMOS RF power amplifier with a series-combining transformer. Section 4.2 provides an analysis of the output transformer, revealing how the non-ideal center tap at the primary winding of the transformer affects the power-efficiency of the transformer. Section 4.3 describes the circuit design of the watt-level CMOS RF power amplifier, including the on-chip design issues and the package/bonding diagram. Finally, the measurement and testing results are described in Section 4.4, and conclusions are drawn in Section 4.5.

The block diagram of our designed CMOS RF power amplifier is depicted in Fig. 4.1, including two power stages and three matching networks. In our design, we adopt the differential structure to transistor blocks in order to eliminate even-order harmonics. The input matching network serves as a balun to convert the single-ended signal to the differential signal. The inter-stage matching network converts one pair of differential inputs to two pairs of differential outputs. Two output stages are combined by the output matching network to provide high output power. The detailed circuit design is shown in Section 4.3

Fig. 4.1 Block diagram of our designed CMOS RF power amplifier

4.2 Output Transformer Analysis

As discussed in Section 2.2, to achieve watt-level output power, the power-combining technique using *LC* baluns or transformers should be implemented in the output matching network. Compared to *LC* baluns, the transformer has low power loss for a given quality factor and its impedance transformation ratio is independent of process variations. For these reasons, the transformer is adopted and implemented in our designed CMOS RF power amplifier as the power combiner. Further, due to low input impedance, less than four power cells combination (two power cells in our design) and the mutually independent primary windings, we adopt the SCT rather than PCT as the output transformer in our project.

There is no power loss in an ideal on-chip transformer. However, in practice, the on-chip transformer is not an efficient device, especially on a lossy CMOS substrate. Section 2.3 had reviewed and discussed the parameters (transformer structure, a , S , W , d , OD , and substrate) and the loss mechanisms that affect the power-efficiency of the

on-chip transformer. For completeness, other parameters including the center tap of the transformer primary winding, to which the supply voltage is connected, should be considered. Perhaps somewhat interestingly, this has not been widely discussed in the literature. In view of this, we will discuss and analyze how the non-ideal center tap of the transformer primary winding affects the power-efficiency of the on-chip SCT, which serves as a power combiner.

Fig. 4.2 A 1-to-1 transformer with the center-tapped primary winding

Fig. 4.2 depicts a 1-to-1 transformer with the center-tapped primary winding. The positive and negative ports ($P1$ and $P2$) of the transformer's primary winding are connected to the differential transistor blocks. The center tap (A) of the primary winding is connected to the supply voltage. If the center tap is ideal, exactly the middle point of the primary winding, it should be the virtual ground for AC signals. However, in practice, the transformer may be asymmetric with respect to the center

tap. As the center tap becomes non-ideal and is no longer the perfect virtual AC ground, the transformer performance such as the transformer power-efficiency is likely to be affected.

Fig. 4.3 The transformer lumped-element model (a) with an ideal center tap, and (b) with a non-ideal center tap

Consider first the analysis of a simple transformer for one power cell. Fig. 4.3(a) shows the lumped-element model of the transformer with an ideal center tap at the primary winding. In this model, the parasitic resistances of the primary and secondary windings are taken into account with R_1 and R_2 being their parasitic resistances. The turn ratio of the transformer is $N_1:N_2$. The point A is the center tap of the primary transformer winding, which is connected to the supply voltage. In this situation (Fig. 4.3(a)), the center tap is a virtual AC ground.

If the center tap is non-ideal, the point A is not the virtual ground. There is an AC signal flowing through the point A to the real AC ground. To model the effects of the non-ideal center tap of the primary winding, a lumped-element model with the parasitic resistance (R_A) is augmented in Fig. 4.3(b). R_A is the parasitic resistance of the metal line between the non-ideal center tap and the real AC ground.

To analyze the non-ideal center tap influences, the primary winding is split to two primary windings (P_1 and P_2) from the center tap A (Fig. 4.3(b)), and the secondary winding is split to two secondary windings (S_1 and S_2). These two primary windings (P_1 and P_2) are magnetically coupled to the secondary windings (S_1 and S_2), respectively. The inductances of these primary and secondary windings are indicated as a_1L_1 , a_2L_1 , a_3L_2 , and a_4L_2 , respectively, with $a_1 + a_2 = 1$ and $a_3 + a_4 = 1$. If the transformer is symmetrical with respect to the center tap, then $a_1 = a_2 = 0.5$. The parasitic resistances of these two primary windings are expressed as a_1R_1 and a_2R_1 , respectively. The voltages of these two primary windings are indicated as V_{1p} and V_{2p} , respectively. The currents flowing through these two primary windings are represented by I_{1p} and I_{2p} , respectively. Due to the non-ideal center tap at the primary

winding, the point A is no longer the virtual ground, and a current ' I_A ' flows from the point A to the AC ground.

The current I_A can be expressed as:

$$I_A = |I_{1p} - I_{2p}| \quad (4.1)$$

The primary winding is split to two primary windings at the center tap A . These two primary windings are coupled to the secondary windings (S_1 and S_2). The turn ratios of them can be expressed as Eqns. (4.2) and (4.3), respectively.

$$\frac{N_{1s}}{N_{1p}} = \frac{I_{1p}}{I_2} = \sqrt{\frac{a_3 L_2}{a_1 L_1}} \quad (4.2)$$

$$\frac{N_{2s}}{N_{2p}} = \frac{I_{2p}}{I_2} = \sqrt{\frac{a_4 L_2}{a_2 L_1}} \quad (4.3)$$

The equivalent input resistances of these primary winding (P_1 and P_2) include the parasitic resistance of the primary winding and the transformed resistance of the secondary winding are expressed in Eqns. (4.4) and (4.5), respectively.

$$R_{1in} = a_1 R_1 + \left(\frac{N_{1s}}{N_{1p}} \right)^2 (a_3 R_2 + a_3 R_l) = a_1 R_1 + \frac{a_1 L_1}{L_2} (R_2 + R_l) \quad (4.4)$$

$$R_{2in} = a_2 R_1 + \left(\frac{N_{2s}}{N_{2p}} \right)^2 (a_4 R_2 + a_4 R_l) = a_2 R_1 + \frac{a_2 L_1}{L_2} (R_2 + R_l) \quad (4.5)$$

From Eqns. (4.1) - (4.3), the current I_A can be expressed as:

$$I_A = |I_{1p} - I_{2p}| = \left| \sqrt{\frac{a_3 L_2}{a_1 L_1}} - \sqrt{\frac{a_4 L_2}{a_2 L_1}} \right| I_2 \quad (4.6)$$

The total input power can be expressed by the sum of the powers (P_{1in} and P_{2in}) consumed by the equivalent input resistances of two primary windings and the power (P_A) consumed by the parasitic resistance between the center tap A and the ground. This is expressed in Eqn. (4.9).

$$P_{in} = P_{1in} + P_{2in} + P_A \quad (4.7)$$

$$= R_{1in} (I_{1p})^2 + R_{2in} (I_{2p})^2 + R_A (I_A)^2 \quad (4.8)$$

$$= \left[\frac{L_2}{L_1} R_1 + (R_2 + R_l) \right] (I_2)^2 + R_A \frac{L_2}{L_1} \left(\sqrt{\frac{a_3}{a_1}} - \sqrt{\frac{a_4}{a_2}} \right)^2 (I_2)^2 \quad (4.9)$$

The power (P_L) consumed by the load impedance is:

$$P_L = R_l(I_2)^2 \quad (4.10)$$

The power-efficiency of this transformer can be expressed as:

$$\eta = \frac{P_L}{P_{in}} = \frac{R_l}{\left[\frac{L_2}{L_1} R_1 + (R_2 + R_l) \right] + R_A \frac{L_2}{L_1} \left(\sqrt{\frac{a_3}{a_1}} - \sqrt{\frac{a_4}{a_2}} \right)^2} \quad (4.11)$$

If the center tap is ideal, which means $a_3 = a_1 = 0.5$ and $a_4 = a_2 = 0.5$, the power-efficiency of the transformer is:

$$\eta = \frac{P_L}{P_{in}} = \frac{R_l}{\left[\frac{L_2}{L_1} R_1 + (R_2 + R_l) \right]} \quad (4.12)$$

Consider now the case where the center tap of the primary winding is non-ideal. The parasitic resistance R_A now exists. To investigate the influences of the non-ideal center tap, we assume that $R_1=0.8\Omega$, $R_2=1.4\Omega$, $L_2/L_1=1$, $R_l=50$ and $a_3=a_4=0.5$. By means of Eqn. (4.11), we plot the transformer power-efficiency versus R_A for different a_1 as depicted in Fig. 4.4.

Fig. 4.4 The transformer power-efficiency versus R_A for different a_1

On the basis of Fig. 4.4, we make the following comments. As expected, the larger the difference is between the value of a_1 and 0.5, the less symmetric the transformer is. When a_1 is equal to 0.5, the center tap is ideal and the parasitic resistance R_A has no effects on the transformer power-efficiency. When the value difference between a_1 and 0.5 becomes larger, the effects of the parasitic resistance R_A on the transformer power-efficiency becomes increasingly significant as expected. The relationship between the parasitic resistance R_A and the transformer power-efficiency is linear.

Fig. 4.5 depicts the transformer power-efficiency versus a_1 for different R_A . We make the following comments on the basis of this figure. As expected, when the

parasitic resistance R_A is small, the effects of a non-ideal center tap on the transformer power-efficiency is insignificant. The relationship between the a_1 and the transformer power-efficiency is not linear. In practice where there are process variations, the effect of the process variations on the transformer power-efficiency at the different a_1 are not same. This is due to the nonlinear relationship between the a_1 and the transformer power-efficiency. To appreciate this, we design two transformers with $a_1 = 0.49$ and 0.46 and assume that the process variation for a_1 is ± 0.01 . They are tabulated in Table 4.1.

Fig. 4.5 The transformer power-efficiency versus a_1 for different R_A

Table 4.1 Two transformers (*A* and *B*) with the designed a_1 and real a_1 (including process variations)

Transformer	<i>A</i>	<i>B</i>
Designed a_1	0.49	0.46
Real a_1 with process variations ± 0.01	0.48-0.5	0.45-0.47

The transformer power-efficiency variation can be obtained from Eqn. (4.13), which is the difference between the maximum power-efficiency ($\eta(a_1 + 0.01)$) and minimum power-efficiency ($\eta(a_1 - 0.01)$) caused by process variations (± 0.01). Consequently, the transformer power-efficiency variation range is from 0 to η_d where

$$\eta_d = \eta(a_1 + 0.01) - \eta(a_1 - 0.01) \quad (4.13)$$

By means of Eqn. (4.13), we plot in Fig. 4.6 the process variation effects on the transformer power-efficiency for different a_1 , and we make the following comments of the two transformers. The process variation influence on the power-efficiency of the transformer with $a_1 = 0.46$ is as expected larger. Also, it is imperative that the symmetry of the transformer be designed as much as possible, i.e, an ideal center tap at the primary winding of the transformer.

Fig. 4.6 Process variation effects on the transformer power-efficiency for different a_1

Our discussion thus far is for one power cell. To achieve the high output power, several power cells are combined. An example is depicted in Fig. 4.7 where the number of power cells combined is M and each transformer is identical.

Fig. 4.7 The transformer lumped-element model for M power cells (a) with ideal center taps, and (b) with non-ideal center taps

The secondary winding of the transformer is connected to the load with the impedance R_l . Because there are M power cells, the load impedance seen by each power cell is $\frac{1}{M}R_l$. The equivalent input impedance of primary windings (P_1 and P_2) can be expressed as:

$$R_{1in} = a_1 R_1 + \left(\frac{N_{1p}}{N_{1s}} \right)^2 \left(a_3 R_2 + \frac{1}{M} a_3 R_l \right) = a_1 R_1 + \frac{a_1 L_1}{L_2} \left(R_2 + \frac{1}{M} R_l \right) \quad (4.14)$$

$$R_{2in} = a_2 R_1 + \left(\frac{N_{2p}}{N_{2s}} \right)^2 \left(a_4 R_2 + \frac{1}{M} a_4 R_l \right) = a_2 R_1 + \frac{a_2 L_1}{L_2} \left(R_2 + \frac{1}{M} R_l \right) \quad (4.15)$$

The input power for the transformer considering M power cells can be derived as expected in Eqn. (4.18).

$$P_{in} = M(P_{in}^1 + P_{in}^2 + P_A) \quad (4.16)$$

$$= M \left[R_{in}^1 (I_p^1)^2 + R_{in}^2 (I_p^2)^2 + R_A (I_A)^2 \right] \quad (4.17)$$

$$= M \left[\frac{L_2}{L_1} R_1 + \left(R_2 + \frac{1}{M} R_l \right) \right] (I_2)^2 + M R_A \frac{L_2}{L_1} \left(\sqrt{\frac{a_3}{a_1}} - \sqrt{\frac{a_4}{a_2}} \right)^2 (I_2)^2 \quad (4.18)$$

The power-efficiency of the transformer with M power cells is hence:

$$\eta = \frac{P_L}{P_{in}} = \frac{R_l}{M \left[\frac{L_2}{L_1} R_1 + R_2 \right] + R_l + MR_A \frac{L_2}{L_1} \left(\sqrt{\frac{a_3}{a_1}} - \sqrt{\frac{a_4}{a_2}} \right)^2} \quad (4.19)$$

From Eqn. (4.19), it is apparent that the power efficiency decreases with the increasing number of power cells. Hence, for the SCT, the number of the power cells should not be excessively large.

In conclusion, due to the non-ideal center tap of the primary winding, the center tap which the supply voltage is connected to is no longer a virtual AC ground, resulting in power losses. The parasitic resistance between the non-ideal center tap to the real AC ground has a linear relationship with the power-efficiency of the transformer. Reducing this parasitic resistance can improve the transformer power-efficiency for a non-ideal center tap at the primary winding of the transformer. The more asymmetric the transformer is, the higher is the influence process variations on the transformer power-efficiency. In short, in the design of an output transformer, it is imperative to attempt to design the center tap of the primary winding to be as close to the middle point of the primary winding as possible - as an AC virtual ground.

4.3 Fully Integrated 4G/LTE CMOS RF Power Amplifier

In this project, a fully integrated CMOS RF power amplifier is designed for 4G LTE applications. This CMOS RF power amplifier operates at the center frequency of 1.732GHz with 20MHz bandwidth and achieves the watt-level output power with the power-combining technique discussed in the previous section. The schematic of our designed CMOS RF power amplifier is depicted in Fig. 4.8(a). This design is classical/well-established design [17, 62]. The micrograph of our designed CMOS RF power amplifier is depicted in Fig. 4.8(b). The block diagram of our designed CMOS RF power amplifier was already depicted in Fig. 4.1. The chip size is 2.4mm x 1.5mm.

At the outset, we will first describe some aspects of the CMOS process and our approach. Due to the low breakdown voltage of CMOS processes, the established cascode topology is adopted where necessary to withstand ‘high’ supply voltage, typically 3.3V - 4.2V for a phone battery. The thick oxide device `dgnfet_rf` with the higher breakdown voltage 2.5V is used with the device `nfet_rf`. The thick oxide device with the higher breakdown voltage can also increase the voltage swing at the drain of the `nfet_rf` device, which improves the power-efficiency of the CMOS RF power amplifier.

In the view of the schematic of the CMOS RF power amplifier, the inter-stage matching between the driver and the output stage is achieved by transformer and capacitor. At the output of the power amplifier, the SCT is used to combine two power cells for the high power. As discussed somewhat extensively earlier, the performance of a transformer has a significant impact on the overall power-efficiency of the RF power amplifier.

(a)

(b)

Fig. 4.8 (a) Schematic of our designed CMOS RF power amplifier, and (b) Die micrograph of our designed CMOS RF power amplifier

Output Transformer Design

The output transformer used in the output matching network of our designed CMOS RF power provides several functions. First, it serves as a power combiner to combine several power cells to achieve approximately one-watt output power. Second, it provides impedance matching by controlling the turn ratio. Third, it acts as a balun which transforms the differential signal to the single-ended signal. Finally, it provides good DC isolation and electrostatic discharge (ESD) protection as there is no physical connection between the primary and secondary windings of the transformer.

Based on the analysis and the derived analytical expression (Eqn. (4.19)) in Section 4.2, we design and optimize the series-combining output transformer with the center-tapped primary windings with due consideration to ensure that the center tap is virtual ground.

Our designed output transformer is depicted in Fig. 4.9. In this design, a commercial 65nm CMOS process with six metal layers (M1-M6) and three top layers (EA, OI, and LB) are used (Fig. 3.2). This process provides an OI layer with the thickness of $3.3\mu\text{m}$, which is utilized for the transformer layout design. Compared with the other layers, the OI layer is considerably thicker and offers reduced parasitic resistances. Because the CMOS RF power amplifier needs to generate watt-level output power and the voltage driving the primary winding of the transformer is low, very high current flows through the primary winding. Consequently, a small parasitic resistance can cause significant voltage drop in the primary winding, which in turn lowers down the overall power-efficiency and the maximum output power. To resolve this problem, two turns of metal lines are combined to reduce the primary winding

parasitic resistances as depicted in Fig. 4.9. The length of the primary winding is adjusted to ensure that the transformer is symmetrical to reduce the mismatch. To reduce the substrate loss and increase the power-efficiency, an M1 patterned shield structure is designed and placed under the transformer. The outer dimension and the width of the metal lines are ‘optimized’ for the best performance of the transformer. The width and the spacing of the metal lines are $24\text{ }\mu\text{m}$ and $2.53\text{ }\mu\text{m}$, respectively, and the outer dimension is $400\text{ }\mu\text{m}$.

Fig. 4.9 Output transformer layout with ‘ideal’ center taps at the primary windings

Decoupling Capacitor

To reduce the noise influence between the supply and the power amplifier, a decoupling capacitor is added near the supply pads on the chip. To determine the value of the decoupling capacitor, we perform simulations to extract the parasitic

value of the supply bonding wires as depicted in Fig. 4.10. The bonding diagram will be discussed later.

Fig. 4.10 Simulation structure for the bonding wires

From simulations, the resistance and reactance of the supply bonding wires are ascertained to be 0.1Ω and 10Ω . The impedance of the supply bonding wires at the operating frequency 1.732GHz is given by:

$$|Z| = \text{real}(Z) + \text{imag}(Z) = 0.1 + 10 = 10.1\Omega \quad (4.20)$$

The decoupling capacitor provides a short pass for RF signals where most of the high-frequency signals would flow through it to the ground without largely affecting the supply voltage. The impedance of the decoupling capacitor should be lower than the impedance of the bonding wire as expressed below.

$$\frac{1}{\omega C} < 10.1 \quad (4.21)$$

From the above equation, we can derive that the capacitance should be larger than 9.098 pF for the frequency of 1.732GHz. In the 65nm CMOS process, we combine the metal-insulator-metal capacitor (MIMCAP) and metal-oxide-metal capacitor (MOMCAP). This is because MOMCAP only uses the metal layers from M1-M6, while the MIMCAP uses the additional HT and QT layers which are above the M1-M6 layers. Thus, the MIMCAP can overlap and be used in conjunction with the MOMCAP to achieve high capacitance without occupying excessive chip area. This layout structure is suitable for decoupling capacitor applications because the decoupling capacitor does not need to be a precise value.

Package/Bonding Diagram

To achieve the watt-level output power, the linear CMOS RF power amplifier typically dissipates much more power than the RF output due to its relatively low power-efficiency (see later) - around 3~5W DC power from the supply [4]. The high DC power consumption generates relatively high current (1~2A) at the supply node for the normal 3.3V phone battery voltage. Not unexpectedly, the bonding wires of

the package at the supply and ground node greatly influence the circuit performance where there are significant DC power loss and voltage drop across the bonding wires. As shown in Fig. 4.11, the considerations of the watt-level CMOS RF power amplifier relate to two levels: chip level and package level, i.e, optimization would involve co-design and the co-simulations of the CMOS RF power amplifier chip and the package.

Fig. 4.11 Multilevel design of the watt-level CMOS RF power amplifier

Fig. 4.12 Bonding wire diagram of the 32pin QFN (5mm x 5mm) package

Our designed CMOS RF power amplifier IC was packaged in a QFN package for its small parasitics. As the parasitic elements associated with the package will significant influence on the RF power amplifier performance, the bonding diagram should be determined and the model of the bonding diagram is co-simulated with the CMOS RF power amplifier circuit in ADS2012 as Fig. 4.11.

In this design, the estimated length of the bond wires of the supply and ground node is 1.5mm. Each of these bond wires introduces 1.5nH inductance and 0.075 Ω resistance. When high current passes through the supply (VDD) or ground (GND)

node, a significant voltage drop appears because of the bond wires parasitic impedance. To mitigate the parasitic effects by reducing the total impedance of the bond wire, multiple bond wires are connected to the VDD or GND as shown in Fig. 4.12. However, due to the mutual coupling, the signals can be coupled between the bond wires nearby. To avoid the noise coupling to the input/output node, the Ground-Signal-Ground (GSG) structure is adopted as depicted in Fig. 4.12. This provides noise a short pass to the ground.

4.4 Measurements and Results

The die micrograph of our designed CMOS RF power amplifier was depicted in Fig. 4.8(b) earlier and packaged in a 32pin QFN (5mm x 5mm) package. Fig. 4.13 depicts an FR-4 printed circuit board (PCB) with our designed CMOS RF power amplifier. This PCB comprises four layers: two signal layers and two power layers. The impedance of the input/output transmission line is designed to 50Ω . Decoupling capacitors are placed between the supply/bias and ground.

Fig. 4.13 PCB photo of our designed RF power amplifier

Single-tone testing is used for measurements involving a vector network analyzer (VNA), signal generator and DC power supply. The measured output power versus input power is depicted in Fig. 4.14, where the RF power amplifier achieves a maximum output power 29.3dBm with a PAE of 17.29%. Compared with the simulation results in Fig. 4.14, the measured low PAE is not as expected; this issue will be discussed at the end of this section. The measured gain of the RF power amplifier is depicted in Fig. 4.15, where the gain achieved is 31.3dB. Comparing the simulation and measurement results in Fig. 4.15, the degradation of gain is not very large and is largely acceptable.

Fig. 4.14 Output Power versus input power and PAE

Fig. 4.15 Gain versus input power

This RF power amplifier is designed for 4G LTE applications, and the output signal is required to pass the spectrum emission mask at 23dBm. The baseband signal is at a center frequency of 1.732GHz with a bandwidth of 20MHz. As depicted in Fig. 4.16 and Fig. 4.17, the output spectrum of our designed CMOS RF power amplifier fulfills the spectrum emission masks of 20MHz QPSK and 16QAM LTE signals at 23dBm.

Fig. 4.16 The measured output spectrum of our designed CMOS RF power amplifier with 20MHz LTE QPSK signal

Fig. 4.17 The measured output spectrum of our designed CMOS RF power amplifier with 20MHz LTE 16QAM signal

To benchmark the design of our RF power amplifier, we tabulate in Table 4.2 a benchmark of reported RF power amplifiers for the LTE application. On the basis of this table and the preceding figures, we make the following comments. Compared with the other RF power amplifiers in this benchmark table, the maximum output power of our designed power amplifier is sufficient. In our design, the driver stage is integrated into the same chip to achieve sufficient gain, which ensures that the LTE signal can directly connect to the input of our designed RF power amplifier. The reported 130nm CMOS RF power amplifier [63] has a low gain because the driver stage is not included in the design. The P_{1dB} of our designed RF power amplifier is 27.5 dBm and is comparable to that reported works.

Table 4.2 Benchmark of RF power amplifiers for the LTE application

	Ref. [58] MTT 2012	Ref. [63] ISSCC 2015	Ref. [64] JSSC 2015	Ref. [65] JSSC 2014	Ref. [66] Skyworks 2011	This work
Freq. (GHz)	0.93	2.4	1.9	1.95	2.35	1.732
Max (P_{out}) (dBm)	29.4	31.6	28	28	-	29.3
Gain (dB)	23*	9.6	30*	30.5	-	31.3
P_{1dB} (dBm)	27.7	29.7	24*	-	-	27.5
Peak PAE	25.8%	39.6%	34%	39%	36%	17.29%
Supply (V)	3.3	3.3	1.5	3.3	3.4	3.3
Modulation	10MHz 16QAM LTE	20MHz 16QAM/QPSK LTE	20MHz 16QAM LTE	10MHz/20MHz 16QAM LTE	1.4-20MHz QPSK/16QAM LTE	20MHz QPSK/16QAM LTE
Technique	Linear	-	Doherty/Mode Switching	Envelope Elimination and Restoration (EER)	-	Linear
Transformer	On-chip	Off-chip	On-chip	On-chip	-	On-chip
Technology	90nm CMOS	130nm CMOS	40nm CMOS	90nm CMOS	InGap BiFET	65nm CMOS

*estimated from the graph

The output spectrums of our designed CMOS RF power amplifier fulfill the spectrum emission masks of 20MHz QPSK and 16QAM LTE signals at 23dBm. However, the peak PAE of our designed CMOS RF power amplifier is somehow low when compared with the other RF power amplifiers in the benchmark table. Our investigations indicate that this low peak PAE is probably due to the inaccurate extraction of the parasitic elements of the metal lines at the output stage, leading to a somewhat poorly optimized metal tracks. Specifically, due to the high current, the width of metal lines would need to be very wide where large output stage requires long metal lines to connect each power cell and the transformer. Put simply, the parasitic self-inductances and mutual-inductances would need to be rigorously characterized and thereafter appropriately optimized for the impedance matching. However, in our design, the parasitic elements of the metal lines extracted by Cadence included only the parasitic resistance and capacitance, and not the parasitic self-inductances and mutual-inductances. This extraction is hence insufficient for wide and long metal lines at high frequencies, leading to unoptimized impedance matching to the load, and the ensuing low power-efficiency. In view of this, we intend to employ the EM simulator, HFSS [45], to extract the accurate parasitic elements of the output stage, including all the parasitic elements (inductance, resistance and capacitance). The further investigations and analysis are ongoing.

As this RF power amplifier is a linear power amplifier without using any power efficiency enhancement technique, its power efficiency is not expected to be high; somewhat similar to that in reference [58]. The designs [64, 65] in the benchmark table adopt techniques (Doherty/Mode Switching and EER) to enhance the power efficiency and, as expected, feature higher power efficiency. Design methods to

improve the power efficiency are being investigated, including the envelope tracking technique; see Chapter 5 in the future work.

4.5 Conclusions

In this chapter, the influence of the non-ideal center tap of the transformer has been investigated with an analytical equation derived. The design of a watt-level CMOS RF power amplifier has been presented, including our design of the CMOS RF power amplifier structure, and the power combining structure to achieve the watt-level output power. The SCT was adopted for the output power combination and the output impedance matching. The issue pertaining to the decoupling capacitor has been discussed, and the MIMCAP and MOMCAP were combined for the high capacitance density. The 32pin QFN (5mm x 5mm) was selected as the package of our designed RF power amplifier. In the bonding diagram, multiple wires were placed at the supply and ground pads to reduce the impedance, and the GSG structure was chosen at the pads of the input and the output for noise isolation. Finally, the measurements and results of our designed CMOS RF power amplifier have been presented. It achieved a 29.3dBm maximum output power with a 17.29% PAE - this power efficiency is somewhat low and we attributed this to the insufficiently rigorous extraction and modeling of the parasitic elements of output stage metal lines by Cadence; see Chapter 5 for future work. The spectrum emission masks requirement has been fulfilled for the 20MHz QPSK and 16QAM LTE signals at 23dBm.

Chapter 5 Conclusions and Recommendations

5.1 Conclusions

We have presented the introduction, motivations, and overview of our research pertaining to a watt level RF power amplifier in Chapter 1 of this dissertation. In Chapter 2, a comprehensive review of the power amplifier, power combining technique, and transformer has been presented. In Chapter 3, we investigated the effect of the substrate thickness on the transformer to improve the thermal dissipation without affecting the transformer performance. In Chapter 4, we have presented several design issues relating to our monolithic watt-level RF power amplifier realization. First, the output transformer as an essential block in this design has been investigated. We have investigated the influence of the non-ideal center tap on the transformer power-efficiency, including deriving an analytical expression. Second, the structure of the one watt RF power amplifier has also been discussed, where two power cells were combined with the SCT to achieve approximately one-watt output power. The output transformer was designed considering the center tap influences. Third, the design consideration of the bonding wire has been discussed, including the following. The bonding diagram accommodated input/output, supply, and ground placement. A GSG structure was used to eliminate the noise influence at the input and the output side. Multiple wires were used to reduce the parasitic effect, thereby increasing the overall power-efficiency of the power amplifier. Finally, the measurement and the results of this design have been presented. This CMOS RF power amplifier achieved a 29.3dBm maximum output power with a 17.29% PAE.

The spectrum emission mask requirements were for the 20MHz QPSK and 16QAM LTE signals at 23dBm. When compared to the state-of-the-art, the power-efficiency is somewhat low. We attribute the low PAE to the insufficiently rigorous extraction and modeling of the wide and long metal lines. This low power efficiency is an on-going investigation and is one of our major efforts in our future work.

5.2 Recommendations and Future Work

In view of the progress of this MEng program at this juncture, we recommend the following as future work.

- (a) First, as discussed above, one of our primary future activity is to investigate the reason for the low power-efficiency of this design.
- (b) Second, to investigate the realization of the CMOS RF power amplifier based on the LEES (Low Energy Electronic Systems) SMART (Singapore-MIT Alliance for Research and Technology) III-V-on-CMOS process.

LEES SMART is developing a proprietary III-V-on-CMOS process that offers the considered advantages of the III-V and CMOS processes as shown in Table 5.1. Because III-V semiconductor offers significantly improved electron mobility and other advantages over MOS, leading to higher power-efficiency, this process is more appropriate than CMOS for the output stage, they are nevertheless appropriate for digital logic, etc [67]. We plan to investigate the realization of the CMOS RF power amplifier with its output

stage based on the III-V process and with the other parts based on CMOS process.

Table 5.1 Comparison of III-V and CMOS process

	III-V Process	CMOS Process
Power-efficiency	High	Lower
Cost	High	Low
Integration	Challenging	Routine

- (c) Third, further to said second, we will investigate efficiency enhancement techniques, like envelope tracking system, etc.

This third future work pertains to the design and implementation of an LTE RF power amplifier with emphasis on high power-efficiency. The envelope tracking (ET) system to be investigated aims to achieve higher power-efficiency than the linear power amplifier. As depicted in the top left-hand corner of Fig. 5.1, the ET power amplifier comprises of two parts, the linear amplifier which transmits the desired RF signal via an antenna, and the supply modulator which provides a variable supply voltage to the linear amplifier. In this design, the supply of the linear amplifier varies according to the output RF signal. Specifically, when the output signal is high, the output of the supply modulator is high and vice versa. As a result, the power-efficiency of the linear amplifier can be significantly improved.

Fig. 5.1 Comparison of power losses of the conventional linear power amplifier and the envelope tracking power amplifier

Fig. 5.1 illustrates the advantages of the ET power amplifier over a commonly used two-mode linear amplifier – it is apparent that the power loss of the ET power amplifier is potentially significantly lower than that of a conventional two-mode power amplifier. The power loss of the ET power amplifier, the green shaded area, is substantially lower than the conventional power amplifier, the red shaded area.

In our future design, we intend to realize the output stage of the supply modulator and the linear amplifier based on III-V transistors and realize the other parts based on CMOS.

Author's Publications & Awards

- [1] **J. Yu**, T. Ge, H. He, and J. Chang, "Substrate thickness effect on transformer," in *2016 International Symposium on Integrated Circuits (ISIC)*, 2016, pp. 1-4.
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