Printed electronics : modeling, variations and bending

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Printed Electronics:

Modeling, Variations and Bending

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Summary

The sanguine projection of the gargantuan growth of Printed Electronics to a large extent assumes that intelligent (embodying analog, mixed-signal and digital signal processing functionalities) Printed Electronics circuits/systems can be realized. This also largely assumes that the printing can be realized on flexible low-cost substrates by green, low-cost, on-demand and scalable printing and that all chains in the entire supply chain is manageable/established. However, at this juncture, Printed Electronics-only circuits/systems remain nascent, i.e., Printed Electronics-only circuits are often rudimentary – lacking sophisticated signal processing functionalities. This is particularly the case for Fully-Additive Printed Electronics.

The overall objective of this research project is to augment intelligence in Printed Electronics. Specifically, this research focuses on the second chain (printing) and the third chain (circuits) of the supply chain of the emerging Printed Electronics technology from following imperative perspectives: manufacturability (e.g., low process variations), functionality (e.g., full-fledged electronics, and bendability of the substrates), designability (e.g., availability of the Process Development Kit), and low cost (e.g., Fully-Additive, All-Air, Low-Temperature process). A number of contributions are made herein with respect to these imperatives.

First, for the manufacturability of Printed Electronics, a novel screen printing Low-Cost Fully-Additive all-air-processed low-temperature Printed Electronics printing process featuring very-low process variations is proposed. Specifically, the process variations are $\pm 4.9\% \mu$ (carrier mobility) and $\pm 0.43\text{V } V_{th}$ (threshold voltage). To the best of our knowledge, this is the smallest μ variations amongst all reported Fully-Additive printing processes, and comparable to the best of Subtractive processes. These very low variations are achieved by blade coating the semiconductor layer comprising a polymer-small molecular blend in a dual-solvent system, yielding precise control of the semiconductor film formation. Further by means of careful layout, the matching between our two printed transistors is markedly improved from 7.2% (arising from $\pm 4.9\% \mu$ and $\pm 0.43\text{V } V_{th}$ variations) to 2.1% – to date, the best reported matching.

Second, for the functionality of Printed Electronics, a comprehensive investigation into the effects of concave/convex bending to printed circuit-elements and basic-circuits is presented, and a novel localized self-compensation means is proposed. The variations of said circuit-elements range from mild-to-severe, depicting that for accurate transfer-functions, capacitor-based circuits are preferred; and the variation direction of capacitors and resistors is the same, but the converse of transistors. For the inverter and ring oscillator, the variations range from moderate to very-severe and severe to extremely-severe respectively for diode-connected and zero- V_{GS} connected topologies. This depicts that diode-connected circuits are preferred; and for speed, concave-bending is preferred. For the op-amp, the gain and gain-bandwidth variations range from mild-to-severe; and concave- and convex-bending is respectively preferred for gain-bandwidth and gain. By leveraging on the process-simplicity of our Fully-Additive all-air-processed low-temperature printing-processes, we propose a novel localized self-compensation means involving the partition of a given circuit-element/circuit into two-halves, each placed on the top/bottom of the flexible substrate surface. The proposed means is highly efficacious – the reduction of variations ranges from $\sim 2x$ to $>100x$, yet without power, hardware or substrate-area overheads but with additional printing steps.

Third, for the designability of Printed Electronics, an ‘Open-Platform’ PDK for our Fully-Additive all-air-processed low-temperature printing process with very low process variations is developed. Our PDK embodies a novel simple yet accurate transistor model that can not only accurately model the printed transistors depending on their layout and when they are flat (unbent substrate) but also accurately model the process variations when they are bent (bent substrate). This PDK accommodating bending is important for Printed Electronics circuits/systems whose substrate is adhered to uneven surfaces or bent to fit odd spaces, thereby expanding the applicability of Printed Electronics circuits/systems. The efficacy of the proposed Open-Platform and the proposed Printed Electronics transistor model is verified by means of comparisons between simulations of and measurements on basic individual printed electronic elements and for several fundamental printed digital and analog circuits. These comparisons include when the substrate is flat and bent, depicting that bending is not necessarily detrimental, but may be advantageously exploited. The proposed PDK is compatible with commercial computer aided design simulation tools.

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List of Abbreviations

$\mu\text{c-Si}$	Microcrystalline Silicon
1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional
ADC	Analog to Digital Converter
AFM	Atomic Force Microscopy
Ag	Silver
Al	Aluminum
Al_2O_3	Aluminum Oxide
AlGaAs	Aluminium Gallium Arsenide
Ar	Argon
a-Si	Amorphous Silicon
Au	Gold
BT	Benzothiadiazole
BTBT	Benzothieno(3,2-b)(1)benzothiophene
BW	Bandwidth
BZT	Barium Zirconate Titanate
C12-4CldiPBI	Tetrachlorinated Diperylene Bisimide
CdS	Cadmium Sulfide
CDT-BTZ	Cyclopentadithiophene and Benzothiadiazole
CdTe	Cadmium Telluride
CIGSe	Cu(In,Ga)Se_2
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
Cr	Chromium
CVD	Chemical Vapor Deposition
DAC	Digital to Analog Converter
DNA	Deoxyribonucleic Acid
DNL	Differential Nonlinearity
DPP	Diketopyrrolopyrrole
DRC	Design Rule Checker
DT-TTF	Dithiophene-tetrathiafulvalene
ENOB	Effective Number of Bits
FOM	Figure-of-Merit
GaAs	Gallium Arsenide

GBW	Gain Bandwidth
HfO ₂	Hafnium Oxide
HM-TTF	Hexamethylene-tetrathiafulvalene
HOMO	Highest Occupied Molecular Orbital
IC	Integrated Circuit
IDT	Indacenodithiophene
InAs	Indium Arsenide
INL	Integral Nonlinearity
IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide
La ₂ O ₃	Lanthanum Oxide
LED	Light-Emitting Diode
LUMO	Lowest Unoccupied Molecular Orbital
Mg	Magnesium
MIM	Metal-Insulator-Metal
MoS ₂	Molybdenum Disulfide
MW	Molecular Weight
N ₂	Nitrogen
NDI	Naphthalene Diimide
Ni	Nickel
NM	Noise Margin
O ₂	Oxygen
OE-A	Organic Electronics Association
OLED	Organic Light-Emitting Diode
OPVD	Organic Vapor-Phase Deposition
P3HT	Poly(3-hexylthiophene)
P4VP	Poly(4-vinylphenol)
PANI-CSA	Polyaniline Doped with Camphor-Sulphonic Acid
PBTTT	Poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene
PC	Polycarbonate
Pd	Palladium
PDI	Perylene Diimide
PDI	Polydispersity Index
PDK	Process Development Kit
PDMS	Polydimethylsiloxane
PECVD	Plasma-enhanced Chemical Vapor Deposition
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene):Poly(styrenesulfonate)
PEEK	Polyetheretherketone

PEN	Polyethylene naphthalate
PES	Polyethersulfone
PET	Polyethylene terephthalate
PFBT	Pentafluorobenzenethiol
PI	Polyimide
PMMA	Polymethyl methacrylate
PnP	Pick-and-Place
poly-Si	Polycrystalline Silicon
PQT-12	Poly(3,3'-dialkyl-quaterthiophene)
PS	Polystyrene
PSRR	Power Supply Rejection Ratio
PSS	Poly(styrene sulfonate)
Pt	Platinum
PTCDI-C13	N,N'-ditridecyl-3,4,9,10-perylenetetracarboxylic Diimide
PVA	Poly(vinyl alcohol)
PVDF	Poly(vinylidene fluoride)
PVP	Poly(vinylpyrrolidone)
P α MS	Poly(α -methylstyrene)
R2R	Roll-to-Roll
RF	Radio Frequency
RFID	Radio-Frequency Identification
RH	Relative Humidity
RMS	Root Mean Square
SFDR	Spurious Free Dynamic Range
Si	Silicon
Si ₃ N ₄	Silicon Nitride
SiO ₂	Silicon Dioxide
SNDR or SINAD	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
TESADT	Triethylsilylethynyl Anthradithiophene
THD	Total Harmonic Distortion
TiO ₂	Titanium Dioxide
TiOPc	Titanylphthalocyanine
UV	Ultra Violet
VLS	Vapor-Liquid-Solid
ZnO	Zinc Oxide
ZrO ₂	Zirconium Dioxide

Chapter 1 Introduction

1.1 MOTIVATIONS

Printed Electronics (or Flexible Printed Electronics) is often touted as ‘Electronics Everywhere, Big Opportunities’. To facilitate Printed Electronics to be one of the key technological enablers for the Internet of Things (IoTs) and other ubiquitous applications, the desirable attributes include Low-Cost (cost in terms of cents, hence disposable), On-demand (print quickly (where production time goes from months/weeks to minutes), print anywhere and print anytime), Green (non-corrosive chemicals), Scalable (large-format printing, e.g., wallpaper), ‘Intelligent’ (embodying analog, digital and mixed-signal processing), and Mechanical Flexibility (printable on flexible substrates such as plastic films, etc.) such that they can be molded or bent to fit in odd and uneven spaces, etc. [1-4]. Ideally, it is akin to a low-cost, on-demand, green, and scalable ‘printing press’. There are a number of synonyms for Printed Electronics.

Printed Electronics is sometimes termed ‘Organic Electronics’, perhaps a slight misnomer because, although the early materials were organic, many recent materials are inorganic. Printed Electronics is also known as ‘Large Area Thin Film Transistor’, and this is also perhaps a slight misnomer because other circuit-elements such as capacitors, resistors, etc., are also printable; see later. It is also sometimes called ‘Plastic Electronics’, and this is similarly a misnomer because non-plastic materials can also be used, e.g., paper as the substrate. In some instances, ‘Flexible Electronics’

is sometimes used where 'Flexible' refers to the mechanical flexibility described earlier. Flexible Electronics embodies both Printed Electronics and Hybrid Electronics (or Flexible Hybrid Electronics) where the latter is heterogeneous integration of the former and conventional silicon-based electronics; see later.

The market potential for Printed Electronics is gargantuan – the Organic Electronics Association (OE-A) [4] projects that the Printed Electronics market will grow from US\$15B today to US\$190B within a decade. IDTechEx [5], on the other hand, projects that the market for Printed Electronics will grow from US\$27B in 2016 to US\$69B in 2026. Although, at this juncture, the market for conventional silicon-based electronics is substantially larger, it is possible that the Printed Electronics market may, at a future juncture, be a significant portion of the overall electronics market. Nevertheless, as the semiconductor carrier mobility of Printed Electronics is likely to remain very low ($>1000\times$ slower) compared to conventional silicon-based semiconductors, the application space of Printed Electronics is expected to remain to very low-speed applications [6-10]. Hence, its market is likely to be smaller than conventional silicon. In this sense, Printed Electronics is not a competitor to silicon-based electronics but complementary thereto. Not unexpectedly, there is considerable international effort [11-27] to realize printed transistors with higher carrier mobility.

In view of the limitations arising from the limited carrier mobility and other challenges in Printed Electronics, many applications involving Printed Electronics are in fact Flexible Hybrid Electronics. Particularly, the specific technology, either Printed Electronics or conventional silicon, is chosen which most makes sense. For example, a sensing instrument realized by Flexible Hybrid Electronics embodies a printed sensor and a silicon microchip, both mounted on a flexible plastic film. There

are numerous examples in the published literature [28-49], technology shows [50-54], etc., including the recent Proceedings of the IEEE special issue [28-42] and impending special issue in the IEEE Journal of Emerging and Selected Topics [55].

In the perspective of ubiquitous applications of Printed Electronics, including as IoTs, cost is a major consideration. In this perspective, a fully-printed (i.e., Printed Electronics-only) realization would be advantageous over its printed-cum-silicon (i.e., Flexible Hybrid Electronics) counterpart in terms of considerably lower; notwithstanding the significantly higher functionality of the latter. For example, in typical Flexible Hybrid Electronics, the thinning of the silicon die (to enable mechanical flexibility) and its attachment (and handling) to the flexible substrate are complex and expensive processing steps [56]. For this reason, there is a considerable international effort to realize Printed Electronics-only devices (despite their limited functionality) – this is the emphasis of the impending special issue in the IEEE Journal of Emerging and Selected Topics [55]; in chapter 2, we will review some of the challenges of Printed Electronics-only realizations.

To this end, our emphasis and effort in this PhD program and reported in this thesis are towards **Printed Electronics-only** realizations.

State-of-the-art Printed Electronics (and Flexible Hybrid Electronics) printing methods can, as depicted in Fig. 1-1, be generally classified into Subtractive [57-66] or Fully-Additive processes [1-3, 6, 63, 67-74]. The former process is considerably more complex and expensive than the simpler and cheaper latter process. At this juncture, of the two classes of Printed Electronics processes, the subtractive-based Printed Electronics processes are dominant, including Laser Ablation [57] and Photolithography [58]. They largely resemble and leverage on present-day

conventional silicon-based processing, involving a series of additive and subtractive steps. The primary shortcoming of this process is the complexity of the steps thereof – they involve highly specialized processing (and associated expensive/sophisticated equipment and infrastructure), including the use of corrosive chemicals for the subtractive steps. Not unexpectedly, the ensuing Subtractive-based Printed Electronics is high-cost (including high wastage of chemicals, in part due to etching/lift-off, etc.), not-on-demand, ‘not-green’ (use of corrosive chemicals), and not-scalable (printing sizes are limited to wafer-size due to the specialized equipment, e.g., 200mm and 300mm). In this sense, Subtractive-based Printed Electronics somewhat contravenes the often-touted attributes of Printed Electronics: low-cost, on-demand, green and scalable.

Fig. 1-1 Printed Electronics: patterning processes; adapted from [4]

At this juncture, several Fully-Additive Printed Electronics processes have been reported [67-69, 71-76], where the steps strictly involve depositions only (without etching or lift-off). In principle, these processes are similar to the mechanical 3D-printing, which involves only additive steps. In Fully-Additive Printed Electronics processes, each printed layer is deposited on layer-upon-layer to realize transistors, passive components (resistors, capacitors and inductors) and interconnections. In this thesis, the denotation ‘Fully-Additive’ explicitly stipulates that all processing steps in the process are strictly depositions, i.e., strictly no subtractive steps. This is important because ‘Additive’ is sometimes inappropriately used in literature where several reported processes were inadvertently deemed ‘Additive’ when some of the printing steps therein are subtractive, e.g., [57].

Although the performance of printed transistors and circuits realized by Subtractive Printed Electronics is typically superior to that realized by Fully-Additive Printed Electronics, Fully-Additive Printed Electronics can be very competitive [1, 2, 4, 6]; the performance herein is qualified in terms of minimum feature size, carrier mobility, process variations, etc. Particularly, as low cost, including simple (no subtractive steps) processing steps, on-demand printing, and scalability are typically imperative for practical applications, Fully-Additive Printed Electronics is in general preferred. Furthermore, for reasons of even lower costs, it is desirable that the Fully-Additive process is all-air and low-temperature. All-air processing involves printing in air without special gases such as nitrogen in specialized chambers. Low-temperature, on the other hand, typically specified as $<120^{\circ}\text{C}$, is desirable as many inexpensive substrates such as the ubiquitous polyethylene terephthalate (PET) plastic films deform beyond $\sim 120^{\circ}\text{C}$.

To this end, our emphasis and effort in this thesis are towards **Fully-Additive All-Air-Processed Low-Temperature Printed Electronics** realizations.

It is generally accepted that for the Printed Electronics market to grow aggressively in addition to low-cost and other attributes described earlier, it would be necessary for Printed Electronics devices to embody ‘intelligence’, i.e., sophisticated analog, mixed-signal or digital signal processing, albeit not at the speed of conventional silicon. Not unexpectedly, because of the formidable (and largely unresolved) challenges associated with the entire supply chain of Printed Electronics (see Fig. 1-2 later), this augmentation of intelligence remains largely elusive. Specifically, at this juncture, there are only very few Printed Electronics-only circuits [77, 78] that embody intelligence. Furthermore, they are based on the Subtractive Process that, as delineated earlier, largely contravenes the advantageous attributes of the ‘printed press’ Printed Electronics. To the best of our knowledge, hitherto, there is no reported ‘intelligence’ in Printed Electronics realized by the Fully-Additive printing process, save our reported work [1, 6].

Put simply, at this juncture, despite the immense interest within the academic and industry communities, Printed Electronics technology remains largely nascent. This nascency can be explained by the formidable challenges of each chain of the Printed Electronics supply chain depicted in Fig. 1-2 that we will now delineate.

Fig. 1-2 Printed Electronics supply chain

The first chain of Printed Electronics is ‘Materials’, and is largely related to chemistry, materials, and chemical engineering. It is not surprising that there is substantial international research effort in the first chain at this juncture [13, 19, 21, 23, 27, 79-99]. The primary challenges include the low carrier mobility of ink-printable semiconductors, process stability, etc. For instance, for the former, the carrier mobility is typically three to four orders of magnitude lower than silicon-based processes; and for the latter, the performance of printed devices (e.g., the carrier mobility) degrades when exposed to air and over time.

The second chain is ‘Processing/Equipment Platform’ and pertains to the patterning/printing processes. Fig. 1-1 earlier depicted the various patterning/printing processes [4]. As depicted in the figure and delineated earlier, the printing technologies can in general be classified as ‘Subtractive’ and ‘Additive’ processes. The Subtractive processes, including Laser Ablation [57] and Photolithography [100], are akin to the established IC fabrication processes. Compared to Additive processes, they are advantageous in terms of smaller resolution, and their printed devices are faster (higher carrier mobility). They are, nevertheless, disadvantageous in a number of aspects. These include more expensive, not-on-demand (printing), ‘not-green’ and not-scalable, hence largely contravening the aforesaid often touted attractive attributes of the ‘printing press’ Printed Electronics.

The Additive processes, including inkjet, flexographic, gravure, offset and screen printing, are akin to printing processes used for graphic arts – they are hence largely ‘printing press’ Printed Electronics with the aforesaid attractive attributes. However, compared to Subtractive processes, Additive process suffers from larger resolution (20~100 μ m), hence lower circuit density and reduced speed (lower carrier mobility). Nevertheless, these shortcomings are largely mitigated by the lower cost offered by Fully-Additive Printed Electronics.

Pertaining to the first and second chains, the ensuing high process variations are one of the formidable challenges. From a manufacturability perspective, it is imperative that the printing processes feature low process variations where the primary parameter is carrier mobility μ ; and in some cases, threshold voltage, V_{th} .

The typical mobility μ and V_{th} variations of reported Fully-Additive processes [3, 6, 70, 101, 102] on flexible substrates are $\pm 30\%$ and $\pm 1\text{V}$ respectively, while those of reported Subtractive processes [64, 103] are typically lower, at $\pm 20\%$ and $\pm 0.7\text{V}$ respectively. The lowest mobility μ and V_{th} variations of Fully-Additive processes on flexible substrates are reportedly [101] $\pm 9.5\%$ and $\pm 0.02\text{V}$ respectively. Nevertheless this process is somewhat impractical and high-cost due to the use of a silicon stencil, largely unscalable as wafer sizes are limited to 300mm, and the processing requires high temperature (300°C; thereby prohibiting the use of low-cost ubiquitous PET substrates) and in nitrogen. On the other hand, the lowest mobility μ and V_{th} variations of Subtractive processes on flexible substrate involve a photolithography process [64] are reportedly $\pm 4.7\%$ and $\pm 0.3\text{V}$ respectively.

In the case of the basic ring oscillator circuit (with diode-connected active loads, see Fig. 3-1(a) in Chapter 3) with $\pm 30\%$ μ variations, typical of many reported Printed

Electronics processes on flexible substrates, we can show [1] that its characteristics become highly unpredictable to the point of failure, i.e., no oscillation. Specifically, the variation of the frequency of oscillation is a large $\pm 13.2\%$ and the failure rate is an unacceptable 13%. In the case of the basic gate-source connected inverter (see Fig. 3-1(b) in Chapter 3 later) with a $\pm 1\text{V}$ V_{th} variations (with rail voltage $V_{DD} = 60\text{V}$), we can show [1] that the variation of the delay is a large $\pm 185\%$. For a combined $\pm 30\%$ μ variations and $\pm 1\text{V}$ V_{th} variations, the severity exacerbates – the variations of the ring oscillator oscillating frequency deteriorate to $\pm 13.5\%$ and with an increased failure rate of 17%; and the delay variations of the inverter deteriorate to $\pm 195\%$. In the case of the basic analog differential amplifier (see Fig. 3-1(c) in Chapter 3 later) with a $\pm 30\%$ μ variations, we can show [1] that the variation of the gain is $\pm 23.2\%$ and input offset is a large $\pm 2.7\text{V}$, and they deteriorate respectively to $\pm 23.6\%$ and $\pm 2.8\text{V}$ for a combined $\pm 30\%$ μ and $\pm 1\text{V}$ V_{th} variations. The large variations are particularly intolerable because negative feedback is generally inapplicable due to small open-loop gain [6].

Put simply, the effects of variations can be very severe because when Printed Electronics circuits are printed/manufactured, the worst-case variations usually define their minimum operating parameters. In part because of this challenge, it is unsurprising that the Organic Electronics Association (OE-A) [4] recently postponed their projection that ‘intelligent’ Printed Electronics circuits/systems will only be realized in 2019 from an earlier 2017 projection.

In short, the formidable challenges of the combined first and second supply-chain include large process variations, low resolution, poor stability of printed circuit-elements (when exposed to air), etc. From the manufacturability perspective, all these

challenges are pertinent, and the large process variations are as challenging as the low carrier mobility.

The third chain in Fig. 1-2 is related to the designs and applications – the display/lighting/power source/communications/sensors/circuits. Pertaining to this chain there are several challenges. First, following the challenges pertaining to first and second supply chains, the circuit designs need to accommodate the low carrier mobility, hence circuits with limited speed. Of particular interest, negative feedback that is ubiquitously applied in analog circuits, is largely inapplicable as the limited speed of printed transistors severely limits the gain-bandwidth.

Second, following the challenges also pertaining to the first and second chains, the large variations are particularly difficult. This is because the definition of the performance of circuits needs to accommodate the worst-case conditions, i.e., the worst-case variations. In the view of the already limited carrier mobility, the high variations lead to even lower ‘usable’ carrier mobility, and hence the even slower ensuing applications. As delineated earlier, it is not unexpected that hitherto, Printed Electronics-only circuits are largely lacking.

Third, further to said second, mechanically flexibility of Printed Electronics (and Flexible Hybrid Electronics) exacerbates the variations problem. Mechanically flexibility is a major Printed Electronics attribute as it significantly broadens the Printed Electronics application space, including as a key technological enabler for the IoTs, e.g., use-and-dispose stick-on wearable IoTs on the human skin. Specifically, when the substrate (e.g., PET plastic film) is bent, it is not unexpected that the characteristics of the printed circuit-elements and circuits on the flexible substrate would change significantly [104-106] – this is a critical yet-unresolved drawback.

As a case in point, when a regular (e.g., 100 μ m-thick PET) flexible substrate is bent, the variations of the Printed Electronics devices/sensors thereon and the ensuing variations of the performance of the printed circuits/systems are effectively intractable. In some cases, the variations are so severe that the circuits/systems fail [1]. It is very difficult, if not impossible, to ascertain if the change in a given bent device/sensor and circuit/system is due to the bending or otherwise, hence largely rendering its functionality nugatory. For completeness, although bending is not a problem if the substrate is very thin ($\sim 2\mu$ m [107]), this is impractical because such substrates are not only highly frangible but also difficult to handle, hence of very limited applications.

In the perspective of the aforesaid third challenge pertaining to said third supply chain, one of our specific applications of interest is the e-skin, depicted in Fig. 1-3, to mimic the pressure sensitivity of the human skin. The e-skin comprises tactile sensors for sensing pressure/bending and flexible Printed Electronics circuits/systems for signal conditioning/processing, e.g., to convert the sensed analog parameters to digital signals that mimic physiological stimulation signals. The overall intention is the realization of a neuroprosthetics device [108] where we envision that both the sensors and signal conditioning circuits are printed in close proximity (ideally, the sensor is realized above the conditioning circuit), unlike that reported elsewhere [109]. In this e-skin, when its substrate is bent as part of pressure sensing, the substrate at the point of the contact bends inwards (concave) while the adjacent areas bend outwards (convex) as depicted in the middle diagram of Fig. 1-3. To depict the severity of the intractable changes, consider the ring oscillator conditioning circuit which represents the mechanical-electronic transduction circuit of the e-skin. We can show (see Section 4.3.2 later) [110] that its output frequency varies by a large 46% and 125%

respectively due to 1cm bending (with the tactile sensor disabled) for a diode-connected and a zero- V_{GS} connected ring oscillator.

Fig. 1-3 An artificial tactile e-skin sensing system, comprising a flexible sensor layer and our Fully-Additive printed circuit layer

Despite the imperativeness of resolving/mitigating the effects of bending, a comprehensive investigation thereto remains largely incomplete, in part due to the nascency of Printed Electronics. Perhaps somewhat surprising for printed passive elements, including capacitors and resistors, the effects of bending remain largely unreported; reported work [104-106] hitherto is on transistors. For circuits, the reported [111-113] effects of bending are limited to basic inverters (diode-connected) and ring oscillators.

Not surprisingly, an electronic/layout means to mitigate the effects due to bending remains unreported/unresolved. At this juncture, the one reported non-electronic/layout method [112] involves depositing another substrate layer on top of the device. This, however, undesirably doubles the overall substrate thickness. Another [113] involves placing devices on an area where the bending is minimum

which requires a priori information that may not be available, and the application is hence highly restrictive.

Fourth, another formidable challenge in the third supply-chain (and related to said first and second supply chains) is the unavailability of Process Development Kits (PDKs) [4]. The PDK is a critical constituent of Computer-Aided-Design/Electronic-Design-Automation tools for a given fabrication technology. It largely embodies the models of the device characteristics, and a set of layout design rules that defines the minimum dimensions for printed devices and minimum distance between them. Not unexpectedly, the PDK is imperative in modern circuits/systems design – for both conventional silicon and Printed Electronics where it facilitates circuits/systems design including the prediction of the performance of the designs under various conditions. In the perspective of the Printed Electronics-only and Flexible Hybrid Electronics design flow, the unavailability of PDK is a major disconnect between the Printed Electronics processing community and the circuits-and-systems community. Put simply, unless the Printed Electronics PDKs become available, Printed Electronics-only circuits/systems will likely remain nascent in the perspective of manufacturing and the sophistication of Printed Electronics-only circuits/systems will likely remain modest.

The fourth and fifth supply chains, the system integration and test/verification pertain more closely to the industry and lesser to academia. They serve to ensure product quality and a reasonable product lifetime.

In summary, Printed Electronics technology embodies multidisciplinary technologies and many formidable challenges that, whilst well recognized, remain unresolved. It is not unexpected that at this juncture, Printed Electronics technology

remains nascent, and the complexity of reported Printed Electronics work are largely of very limited signal processing or ‘intelligence’ (save the more complex Subtractive processes which contravene the spirit of Printed Electronics). In short, there are many unresolved issues pertaining to Printed Electronics, and of particular interest, that pertaining to Fully-Additive all-air-processed low-temperature Printed Electronics-only processing.

1.2 OBJECTIVES

The grand objective of this research project is to augment intelligence into Printed Electronics. Specifically, this research focuses on the second chain (printing) and the third chain (circuits) of the supply chain of the emerging Printed Electronics technology from following imperative perspectives: manufacturability (e.g., low process variations), functionality (e.g., full-fledged electronics, and bendability), designability (e.g., availability of the Process Development Kit), and low cost (e.g., Fully-Additive, All-Air, Low-Temperature process). The specific objectives of this PhD program are now delineated.

- I. For the manufacturability of Printed Electronics, the specific objectives pertaining to the process variations are to significantly reduce the process variations in the first, second and third chains of our Fully-Additive Low-Temperature process:

(i) First Supply Chain

To develop a low-cost Fully-Additive all-air-processed low-temperature (e.g., $<120^{\circ}\text{C}$) printing process (on flexible substrate) that features very low process variations by utilizing a novel semiconductor solution;

(ii) Second Supply Chain

Following (i), to minimize the process variations of the Fully-Additive printing process by investigating/optimizing the process parameters; and

(iii) Third Supply Chain

Following (ii), to investigate the associated mismatch between two transistors printed by our optimized Fully-Additive printing process, and how layout affects the mismatch.

II. For the functionality of Printed Electronics, the specific objectives pertaining to variations arising from the effects of bending are:

(i) To investigate the effects of concave/convex bending for passive and active printed circuit-elements with different bending radii;

(ii) Similar to (i), but for printed circuits, including several fundamental analog (op-amp) and digital (inverter and ring oscillator) circuits;

(iii) Leveraging on the process-simplicity of our Fully-Additive All-Air-Processed Low-Temperature printing process, to develop a novel localized self-compensation means to mitigate the effects of bending for printed circuit-elements and circuits on flexible substrates; and

- (iv) On the basis of (iii), to design, print and verify several analog (op-amp) and digital (inverter and ring oscillator) circuits to ascertain the efficacy of our said proposed localized self-compensation means.

III. For the designability of Printed Electronics, in view of the unavailability of PDKs in literature, the specific objectives pertaining to the development of a PDK for our Fully-Additive All-Air-Processed Low-Temperature process are:

- (i) To develop a transistor model (part of the PDK), particularly, for our low-cost Fully-Additive All-Air-Processed Low-Temperature printing process on flexible substrates. It is a further objective that our developed model is able to accurately model the entire transistor operation region (from cut-off to supra-threshold) when the printed transistor is flat (unbent substrate);
- (ii) On the basis of (i), to develop a comprehensive transistor model to not only accurately model the printed transistors when they are flat but also accurately model the process variations thereto when they are bent (bent substrate);
- (iii) On the basis of (ii), extend our developed transistor model to circuits (including when they are flat and bent) embodying several transistors vis-à-vis a single transistor;
- (iv) Further to (ii), to develop Layout Design Rules (part of the PDK) for our Fully-Additive All-Air-Processed Low-Temperature printing process; and
- (v) On the basis of (i) to (iv), to design and print several fundamental analog (op-amp) and digital (inverter and ring oscillator) circuits (third chain) to ascertain the efficacy of our PDK and our derived model.

1.3 CONTRIBUTIONS

Congruous to the aforesaid objectives, a number of contributions are made in this Ph.D. program. These contributions are largely reported in four journal articles [1, 6, 110, 114] (3 published and 1 accepted) and five conference papers [2, 115-118].

For the manufacturability of Printed Electronics, the contributions pertaining to the process variations in the first, second and third supply chains include:

- (i) Development of a novel low-cost Fully-Additive all-air-processed low-temperature Printed Electronics printing process featuring very low process variations by utilizing our proposed semiconductor blend. Specifically, the process variations are $\pm 4.9\% \mu$ and $\pm 0.43V V_{th}$. To the best of our knowledge, this is the smallest μ variations amongst all reported Fully-Additive printing processes, and comparable to the best of Subtractive processes;
- (ii) Investigation and optimization of the process parameters, e.g., semiconductor solution and coating conditions. Our proposed polymer-small molecular blend semiconductor is compared against the non-blend approach. This investigation is carried out not only for the process performance at the point of printing but also for performance degradation 3 months after printing. Our proposed dual solvent system used for our blend is thereafter investigated with respect to the volume percentage of anisole used in the semiconductor solution. Following this, the blade coating conditions for the semiconductor layer, including coating temperature and coating speed, are investigated. The optimized parameters ascertained for our Fully-Additive all-air-processed low-temperature process are 20 vol% anisole in TIPS-

Pentacene/PS based blend (vis-à-vis TIPS-Pentacene), 60°C coating temperature and 0.2mm/s coating speed; and

- (iii) Further to (ii), the associated mismatch between two transistors printed by our optimized Fully-Additive printing process and how layout affects mismatch are investigated. The I-V characteristics of the two transistors are better matched as the layout progresses from simple → interdigitation → centroid → 2D centroid layouts: respectively 7.2%, 5.3%, 2.8% and 2.1%. For the same layouts, the matching between two transistors based on our optimized process is respectively 6.7x, 4.1x, 6.1x and 4.2x better than that of based on typical Fully-Additive processes.

For the functionality of Printed Electronics, the contributions pertaining to the effects of bending include:

- (i) A comprehensive investigation into the effects of concave/convex bending to printed circuit-elements with different bending radii, including passive and active printed circuit-elements. The variations of said circuit-elements range from mild-to-severe, depicting that for accurate transfer-functions, capacitor-based circuits are preferred; and the variation directions of capacitors and resistors are the same, but the converse of transistors;
- (ii) A comprehensive investigation into the effects of concave/convex bending to printed circuits with different bending radii. For the inverter and ring oscillator, the variations range from moderate to very-severe and severe to extremely-severe respectively for diode-connected and zero- V_{GS} connected

topologies. This depicts that diode-connected circuits are preferred; and for speed, concave-bending is preferred. For the op-amp, the gain and gain-bandwidth variations range from mild-to-severe; and concave- and convex-bending is respectively preferred for gain-bandwidth and gain;

- (iii) Proposal of a localized self-compensation means to mitigate the effects of bending for printed circuit-elements and circuits on flexible substrate. The proposed means involves the partition of a given circuit-element/circuit into two-halves, each placed on the top/bottom of the flexible substrate surface; and
- (iv) On the basis of (iii), several digital (inverter and ring oscillator) and analog (op-amp) circuits are designed and printed. Our proposed self-compensation means is shown to be highly efficacious – the reduction of variations ranges from $\sim 2\times$ to $>100\times$, yet without power, hardware or substrate-area overheads but with additional printing steps;

For the designability of Printed Electronics, the contributions pertaining to the unavailability of PDKs include:

- (i) Development of a transistor model, particularly for our low-cost Fully-Additive printing process on flexible substrate that features very low process variations. This transistor model can accurately model the characteristics in the entire transistor operation region (from cut-off to supra-threshold) when the printed transistor is flat;

- (ii) On the basis of (i), a comprehensive transistor model that accommodates bending (including both concave and convex bending) is developed to not only accurately model the printed transistors when they are flat but also accurately model the process variations when they are bent (bent substrate);
- (iii) On the basis of (ii), several fundamental circuits are simulated to extend our developed transistor model to circuits (including when they are flat and bent);
- (iv) Further to (ii), Layout Design Rules are developed for our Fully-Additive printing process; and
- (v) On the basis of (i) to (iv), several fundamental analog (op-amp) and digital (ring oscillator) circuits are designed, printed and measured. The efficacy of the PDK and the model are verified by comparing simulations against measurements of these circuits.

From an overall perspective, the contributions made in this Ph.D. program are significant – they provide Printed Electronics researchers useful insight from the first supply chain to the second and third supply chains of Printed Electronics to facilitate the realization of ‘intelligent’ Printed Electronics flexible circuits/systems based on low-cost, on-demand, green and scalable Fully-Additive process.

1.4 ORGANIZATION OF THE THESIS

This thesis is organized as follows. Chapter 1 describes the motivations, objectives, contributions and organization of this thesis. The subsequent chapters of this thesis are organized in the following manner.

In Chapter 2, a comprehensive and critical literature review is provided. Flexible Electronics, Hybrid Electronics and Printed Electronics, are reviewed in turn, including their technological challenges and application space. As the emphasis of our PhD program is Printed Electronics, our review focuses on Printed Electronics, including the complete supply chain and the challenges and solutions thereto. Finally, we review our NTU Printed Electronics process.

In Chapter 3, for the manufacturability of Printed Electronics, we present our novel Fully-Additive Low-Cost all-air-processed low-temperature screen printing process for realizing transistors with very low variations, include very low mobility μ and V_{th} variations; to date the lowest variations of reported Fully-Additive processes. Said very low variations are achieved by means of blade coating of our polymer-small molecule blend (TIPS-Pentacene/PS) in our dual solvent system (toluene and anisole). The optimized parameters are delineated. We also present an investigation on the matching of two transistors by means of layout – as a means to reduce the variations – and show that matching can be markedly improved by means of appropriate layout but with some printed area compromises.

In Chapter 4, for the functionality of Printed Electronics, we first present a comprehensive investigation into the effects of concave/convex bending on individual printed passive and active elements and on basic-circuits. We show that in terms of variations, capacitor-based circuits and diode-connected circuits are preferred; and for inverters and ring oscillators, concave bending is preferred. We propose a novel localized self-compensation means to mitigate the variations of printed circuit-elements and circuits due to bending. The proposed means is shown to be highly efficacious.

In Chapter 5, for the designability of Printed Electronics, we describe an Open-Platform PDK to facilitate the design and simulations of Printed Electronics circuits and systems. Our PDK embodies an accurate yet simple model that can not only model the Printed Electronics transistors when they are flat but can also model the Printed Electronics transistors when they are bent. Our PDK further includes the layout design rules. The efficacy of the PDK and the model are verified by comparing simulations against measurements on individual components and translated to several fundamental analog and digital circuits embodying said components.

In Chapter 6, conclusions of this research program are drawn and recommendations for further work are presented.

Chapter 2 Literature Review: Flexible Hybrid and Printed Electronics

The scope of the Flexible Hybrid and Printed Electronics is very wide as it encompasses many disciplinary fields. In this review chapter, we will comprehensively and critically review Flexible, Hybrid, Printed Electronics (including our interpretation of the definitions thereto), but for sake of brevity, the review is skewed towards a circuits and systems perspective; i.e., the review of some parts of the supply chain in Fig. 1-2 may be somewhat succinct. Also congruous to the emphasis on Printed Electronics in this PhD thesis, this review will also focus on Printed Electronics.

As delineated in Chapter 1, we interpret ‘Flexible’ as mechanically flexible where the substrate of the electronics can, at the very least, be bent concavely or convexly. In some cases, flexibility includes stretching. It is interesting to note that in the perspective of the circuits and systems and solid-state communities, flexibility is sometimes interpreted as reconfigurable electronics, e.g., FPGA (Field Programmable Gate Array) in conventional silicon electronics - this is not our interpretation herein.

We interpret ‘Hybrid’ as heterogeneous electronics, embodying conventional silicon and printed electronics (see below for our more complete interpretation). In the perspective of the circuits and systems and solid-state communities, hybrid electronics ‘traditionally’ refer to thick film circuits which is an alternative to the more conventional printed circuit board (PCB). In our interpretation herein, ‘Hybrid’ is

more often termed ‘Flexible Hybrid’ electronics where the conventional silicon die is thinned down (typically to $<50\mu\text{m}$) so that it can be bent (mechanically flexible). This thinned down die is placed on a mechanically flexible (or stretchable) substrate with printed electronic elements, where the choice of the specific technology is that which most makes sense. For example, for a Flexible Hybrid Electronics sensing system, the sensor is printed on a flexible substrate and connected to a thinned down silicon IC die placed on said flexible substrate. In some sense, ‘Flexible Hybrid’ electronics is a subset of Flexible Electronics, and ‘Flexible Hybrid’ and ‘Flexible’ are sometimes used interchangeably in literature.

As in Chapter 1, we interpret ‘Printed’ electronics as electronics that are printed directly on a substrate (both rigid and flexible). The printing typically resembles that used in graphics art where electrically functional electronic or optical inks are deposited on the said substrate, creating passive or/and active circuit elements. At present, the interest of the Printed Electronics community is Printed Electronics on flexible substrates as printed devices on rigid substrates do not generally offer competitive advantages over rigid silicon ICs or devices placed on a rigid PCB.

In this chapter, our literature review is as follows. Flexible Electronics, Hybrid Electronics and Printed Electronics, including combinations thereof, are reviewed in turn, including their technological challenges and application space. As the emphasis of our PhD program is Printed Electronics, our review thereafter focuses on Printed Electronics, including the complete supply chain and the challenges and solutions thereto.

2.1 FLEXIBLE ELECTRONICS

A substrate that is mechanically flexible is highly advantageous over a rigid substrate because many surfaces, natural and man-made, are curvilinear. The ‘need’ to realize Flexible Electronics whose substrate can be bent to accommodate curvilinear surfaces and enclosures was recognized approximately five decades ago. One of the earliest for consumer electronics is a telephone [39] in the 1960s embodying flexible circuitry where said flexibility allowed 25% additional room to contain more functionality within the same enclosure. In that same era, some were used in specialized applications, including thin solar cell (cell thickness $\approx$ 178 μ m) arrays for aerospace and satellites [119, 120]. The mechanical flexibility of the solar cell arrays offered a convenient yet reliable means for compact stowage (rolled up in a 20.3-cm diameter cylinder) and thereafter opened for deployment.

As briefly delineated earlier, ‘Flexible Electronics’ is, at this juncture, realized either as Flexible Hybrid Electronics embodying a ‘bendable’ (thinned down) silicon IC and Printed Electronics on a flexible substrate, or Printed Electronics-only on a flexible substrate. There are now a myriad of applications and some [35, 121-127] are tabulated in Table 2-1; this tabulation is by no means exhaustive. In the perspective of our research, our primary interest is for the Internet-of-Things where designability (e.g., availability of the Process Development Kit), low cost (e.g., Fully-Additive, All-Air, Low Temperature process), manufacturability (e.g., low process variations) and functionality (e.g., full-fledged electronics, and bendability) are some of the imperatives.

Table 2-1 Application space of Flexible Electronics

Lighting Flexible lighting	e-skin Multifunctional sensing (e.g., pressure, temperature, etc.)
Display Flexible TV	Packing/Shipping/Logistics Cold chain management Tampering detection Food freshness/quality
Energy Organic photovoltaics	Consumer Electronics Interactive toys/games Virtual reality
Medical and Pharmaceutical Smart bandage Patient monitoring X-ray imaging Fitness feedback/assist	Structural/Building and Architecture Airframe
Sports Performance monitoring Injury rehabilitation	Textiles and Fashion Smart textiles
Vehicles/Automotive Passenger comfort Safety	Environment Smart buildings (e.g., temperature, air flow monitoring)
White Goods	Soft Robotics
Printing and Graphic Arts	

Table 2-2 Functional modules in Flexible Electronics

Sensors <i>Sensor categories:</i> Electromechanical sensors Photonic sensors Chemical and biological sensors <i>Applications:</i> Accelerometer/strain/pressure Environmental (temperature, gas and air quality, humidity, etc.) Physical activity (heart rate, blood oxygen, etc.) Biometric sensing (electrolytes, blood gases, DNA markers, protein markers, photoplethysmograph, etc.)	Displays/Lighting Flexible displays/lighting (e.g., OLED)
	Energy Battery, Super capacitors Energy harvesters e.g., Solar cell, RF pickup
	Processing/Computation/Memories Amplifiers, Data converters Microcontrollers, Memories
	Communications RF readout, Connectors

Further to Table 2-1, the circuits/systems therein typically comprise one or several functional modules, including sensors, processing/computation/memory, energy, communications, etc. Table 2-2 tabulates some of these functional modules – they may be realized by Flexible Hybrid Electronics or Printed Electronics on a flexible

substrate. In general, Flexible Hybrid Electronics offers high-performance but the process is complex and the cost high. Printed Electronics, on the other hand, suffers from substantially lower performance but the process is usually substantially less complex and lower cost. In following sections, we will review these two approaches in turn.

2.2 HYBRID ELECTRONICS (FLEXIBLE HYBRID ELECTRONICS)

The specific Hybrid Electronics of interest is Flexible Hybrid Electronics, i.e., Hybrid Electronics realized on a flexible substrate. An example of an Flexible Hybrid Electronics is ‘smart label’ [128], an RFID tag. As an HFE device, it embodies both conventional silicon ICs (power management and signal computation) and printed devices (antenna, interconnects, and sensor) on a flexible plastic film. As delineated earlier, the specific technology is chosen which makes most sense.

Table 2-3 tabulates the functional modules in the various state-of-the-art applications realized by Flexible Hybrid Electronics. It can be seen that the Printed Electronics and conventional silicon play somewhat complementary roles in Flexible Hybrid Electronics such that the specific technology is chosen which most makes sense. For instance, the various sensors and large area energy harvesters are realized by Printed Electronics, while the ‘intelligent’ functions (e.g., the precision readout, power management, high performance computation circuits, and low-energy transceivers) are realized by conventional silicon ICs.

Table 2-3 Functional modules in Hybrid Electronics

	Printed Electronics	Silicon
Sensing	Diverse sensors on flexible and large area substrate	Precision readout circuits
Energy	Large area energy harvester	Power management circuits (e.g., power rectification, over/under voltage protection, and DC-DC conversion)
Processing/ Computation/ Memory	Modest performance (complementary and non-complementary) transistors, low-speed inverters and low-speed ring oscillators, amplifiers, etc.	High-performance transistors, amplifiers, data converters, microcontrollers, and memories
Communication	Large-dimension antennas and inductors	Low-energy transceivers

It can be appreciated that in state-of-the-art Hybrid Electronics, conventional silicon ICs provide the high performance circuits, such as high-precision amplifiers, complex signal processing circuits, memory, communications, as well as relative precise in-situ passive components, such as resistors, capacitors, inductors and antennas. Printed Electronics, on the other hand, are typically ‘unsophisticated’ elements such as sensors, interconnects, antennas, etc., and occasionally low performance circuits. The high performance (speed and density) of conventional silicon ICs is largely an exploitation of the high carrier mobility of the single crystalline silicon which is unavailable in Printed Electronics at this juncture. For instance, a typical low-cost 8-bit microcontroller comprises more than 100,000 transistors. This is considered relatively simple in conventional IC industry, but far beyond the capability of present-day Printed Electronics technology – both the transistor number and transistor performance of conventional silicon are orders of magnitude higher than those of state-of-the-art Printed Electronics technology.

In this perspective and in the context of this PhD thesis, our intention is to increase the functionality of Printed Electronics beyond sensors and interconnects, i.e., the intelligence of Printed Electronics – to perform some, if not all, of the functionalities

of the conventional silicon IC; see Section 2.3 later. The ultimate intention is to design and realize intelligent Printed Electronics-only (i.e., without the silicon IC) circuit/system which is potentially substantially lower cost, green, on-demand printed, etc.

To realize and integrate some of the various functional modules in Table 2-3, the supply chain of Flexible Hybrid Electronics encompasses the supply chain of conventional ICs and Printed Electronics (Fig. 1-2) and that associated with their combination, involving the thinning/dicing of the silicon ICs, and placement/interconnection of silicon ICs on a flexible substrate. Fig. 2-1 depicts a typical complete supply chain of Flexible Hybrid Electronics. Due to the diversity of applications and specificities of various technologies, the supply chain may vary for different applications and technologies used. For instance, some devices (e.g., antenna) may be printed before or after the die attachment/interconnection.

Fig. 2-1 Flexible Hybrid Electronics supply chain

The chains pertaining to the silicon ICs comprise five major chains: Silicon Foundry, IC Design, IC Fabrication, Die Thinning/Dicing and Test/Verification. The first chain pertaining to the Silicon Foundry is extremely sophisticated (and expensive) and well-established. Their associated major challenges are well documented in

numerous reports [129-134], including the International Technology Roadmap for Semiconductors [134]. Of particular interest, as the feature size continues to shrink, the variations (process, voltage and temperature) of the transistors increase and the gain of these nano-scaled transistors diminishes. In some sense, these challenges are similar to Printed Electronics transistors; see later. The Flexible Hybrid Electronics chain beyond that of the conventional IC includes Die Thinning to obtain mechanical flexibility of the IC die.

The details of the supply chain for Printed Electronics will be delineated in Section 2.3 later.

The final supply chains of Flexible Hybrid Electronics involve a combination of the conventional IC supply chain (with thinned IC dies) and Printed Electronics. These involve IC Die placement and interconnection on the flexible substrate, and final test and verification.

Table 2-4 compares the attributes of ICs realized on conventional rigid substrates and those required in the Flexible Hybrid Electronics. Due to the flexible form factor of the latter, the die thickness needs to be ultra-thin, typically $<50\mu\text{m}$, to accommodate bending. Fig. 2-2 depicts a photograph [56] to illustrate the imperativeness of thin dies, specifically of $25\mu\text{m}$ and $250\mu\text{m}$ thick dies attached onto a flexible substrate bent to a radius of approximately 1.2cm. It can be seen that the thicker $250\mu\text{m}$ die delaminates from the substrate while the thinner $25\mu\text{m}$ die complies with the bending.

Table 2-4 IC attributes in rigid applications and Flexible Hybrid Electronics

Attributes	Rigid Applications	Flexible Hybrid Electronics
Flexibility	No	Required
Bending-induced effects	Limited, if any	Must be considered
Effects of substrate thickness	Limited, if any	Significant
Thin	Some applications*	Required
Chip preparation	Dicing, packaging	Thinning, dicing
Packaging platforms	Packaged IC	Bare dies
Assembly techniques	Conventional Pick-and-Place	Unique
Bridging the interconnection gap	IC packages, interposers	Flexible interposers, etc.

*3-D and 2.5-D IC packaging

Fig. 2-2 Photograph of a 25µm thick silicon die (left) and a 250 µm thick die (right) on a flexible substrate [56]

The typical die assembly process in Flexible Hybrid Electronics (the top fourth left supply chain and the second right-most chain in Fig. 2-1) is depicted in Fig. 2-3. There are several formidable challenges in Die Thinning/Dicing and Die Placement/Interconnection due to the flexible form factor. First, the thinning of the wafer may cause some undesired effects, such as residual stresses, stress concentrators, changes in microstructures, and substrate microcracks. These undesired effects lead to possible chip fracture and failure when the thinned die is bent. Second, the wafer dicing, typically by saw dicing and laser ablation, may damage and leave residuals on the dies on the wafer.

Fig. 2-3 A typical die assembly process in Flexible Hybrid Electronics [56]

Third, the conventional Pick-and-Place (PnP) technology for die placement and interconnection in general have difficulty handling ultra-thin dies. The workings of the PnP machine typically involve picking up bare silicon dies with a vacuum nozzle, orienting and placing the die in the desired location on the flexible substrate, and applying a combination of pressure and heat for a specific time to cure the adhesive under the die. Due to the thinness of the IC die, the die may bend into the vacuum channel of the pick-up tool, potentially leading to undesired contact stress on the die. The handling capability limit for die thickness of conventional PnP technology is typically $\sim 50\mu\text{m}$. Additionally, conventional PnP technology is largely incompatible with the desired low-cost printing-type manufacturing, such as roll-to-roll processes. Fourth, reliability issues may arise for the die interconnections on the flexible substrate. For instance, there are risks of interconnects cracking due to incompatible mechanical properties between the silicon die and the substrate, particularly upon bending, and ensuing die delamination when the thinned silicon die with limited flexibility is attached to a more flexible substrate. To prevent potential cracking of the

interconnects at the interface, compliant flexible interposers (such as low-temperature conductive adhesives/inks) are sometimes employed. At this juncture, this challenge remains largely unresolved, in part because the flexible adhesives/inks will undesirably increase the interconnection (electrical) resistance.

In summary, due to the embodiment of high performance silicon IC die and some printed devices (e.g., sensors), Flexible Hybrid Electronics (in a flexible form factor) feature similar performance to traditional silicon IC realizations but with the advantage of mechanical flexibility. For the same reasons, Flexible Hybrid Electronics feature substantially higher performance than Printed Electronics-only realizations. Nevertheless, the die assembly process in Flexible Hybrid Electronics is complex and challenging, thereby leading to undesired high assembly cost.

2.3 PRINTED ELECTRONICS

As delineated at the outset of this chapter, we interpret ‘Printed Electronics’ as electronics that are printed directly on a substrate (both rigid and flexible). The printing typically resembles that used in graphics art where electrically functional electronic or optical inks are deposited on the said substrate, creating passive or/and active circuit elements. At present, the interest of the Printed Electronics community is Printed Electronics on flexible substrates as printed devices on rigid substrates do not offer competitive advantages over silicon ICs or devices placed on rigid substrates such as conventional PCBs. Compared to Flexible Hybrid Electronics, the major advantage of Printed Electronics-only realizations is low cost, which is a key consideration for commercialization, including low-cost IoTs.

Note that various thin-film transistor (TFT) technologies, such as amorphous silicon (a-Si) TFT, polycrystalline silicon (poly-Si) TFT, microcrystalline silicon (μ c-Si) TFT, are sometimes called ‘Printed Electronics’. This is probably a misnomer as the above TFT technologies are largely not printable. This review is skewed towards the technologies (e.g., organic TFT) that are printable or at least potentially printable. Hence, a-Si, poly-Si and μ c-Si TFT technologies are largely not included in this review.

2.3.1 State-of-the-Art Printed Electronics

With the exception of high performance signal processing modules, various modules realized by Printed Electronics have been reported, including a diversity of sensors [135-137], energy harvesters (by large-area solar [138-141], thermal devices [142] and piezoelectric [143]), flexible thin-film battery [144], large displays (OLEDs and their backplanes) [145, 146], physically large antenna [147], etc. By integrating various Printed Electronics realized modules, several Printed Electronics-only systems have been reported and some of them will now be reviewed.

M. Jung *et al.* reported a fully-printed Radio Frequency tag realized from a combination of inkjet printing and gravure printing. This tag consists of a printed antenna, diode, capacitor, humidity sensor and a signage unit. The Palo Alto Research Center and Thin Film Electronics reported a Printed Electronics-only realized temperature threshold sensor tag [40] consisting of sensor, logic circuits, and memory. The sensor tag is used to detect if the temperature exceeds a set threshold and to record data digitally for later retrieval. The sensor thereon is a printed thermistor bridge; the logic circuits are based on complementary transistors realized by inkjet printing, spin

coating and laser ablation; and the nonvolatile memories are realized by gravure-printed ferroelectric capacitors. Nevertheless, the carrier mobility achieved in the circuit is a low $0.04\text{--}0.1\text{cm}^2/\text{Vs}$, and an undesired subtractive step of laser ablation is involved in the printing of the logic circuits. Myny *et al.* [148, 149] reported a microprocessor (on rigid substrate, with the potential of being realized on a flexible substrate) based on the combination of photolithography realized logic circuits and memory is ‘programmed’ by inkjet-printed top layers. It operates at 6.5 V with clock frequencies up to 2.1 kHz, a frequency that is considered ‘very high’ in the context of Printed Electronics.

In summary, at this juncture, very few Printed Electronics-only realized systems have been reported. Particularly, the printed Processing/Computation/Memory module is largely lacking due to the low/moderate performance of printed transistors. We will now review the supply chain of Printed Electronics and discuss the challenges thereto.

2.3.2 Supply Chain and Challenges

For sake of readability, the Printed Electronics supply chain earlier depicted in Fig. 1-2 is redrawn in Fig. 2-4 below. The Printed Electronics supply chains chronologically include Materials, Process/Equipment/Platforms, Display/Lighting/Power Source/Communications/Sensors/Circuits, System Integration, and Test/Verification. Perhaps somewhat surprising, despite the somewhat ‘long’ history, arguably from the 1970s arising from the pioneering work of Nobel Laureates Alan J. Heeger, Alan MacDiarmid, and Hideki Shirakawa, the technologies in the supply chain of Printed Electronics are still considered emerging or nascent as the key

challenges thereto remain largely unresolved. Each chain of the supply chain (and its challenges) will now be delineated.

Fig. 2-4 Printed Electronics supply chain

2.3.2.1 Chain 1: Materials

The Printed Electronics community has over a decade has invested concerted effort to improve the carrier mobility, environmental stability, processability and ensuing cost of the semiconductor materials. In general, semiconductors in Printed Electronics can be classified as organic and inorganic semiconductor materials, and often the classification of organic and inorganic transistors is based on the semiconductor employed.

In general, organic semiconductors feature better solution-processability overt their inorganic counterparts and this is desirable in terms of low-cost. Nevertheless, inorganic semiconductors typically have much higher carrier mobility and better environmental stability. In view of our emphasis on low cost Printed Electronics, our review herein will mainly focus on organic semiconductors. Nevertheless, inorganic semiconductors will be first succinctly reviewed for completeness.

Inorganic semiconductors in Printed Electronics can be largely classified as either 1D or 2D materials. The former includes as nanowires and nanoribbons, and the latter includes graphene and exfoliated mono- and polycrystalline semiconductors derived

from bulk substrates or high quality deposited films; the classification of graphene-based materials as inorganic is somewhat contentious because graphene is essentially carbon-based. Table 2-5 tabulates a summary of some reported inorganic semiconductors. Research into inorganic (and carbon nanotube- and graphene-based) semiconductors by the printed electronics community is intensive and new and novel materials that circumvent the limitations of present materials are expected.

Table 2-5 Summary of inorganic semiconductors

Reference	Year	Semiconductor	Mobility (cm ² /Vs)	Supply Voltage (V)
Geim <i>et al.</i> [150]	2007	Graphene	5000	-
Radisavljevic <i>et al.</i> [151]	2011	MoS ₂	200	10
Rogers <i>et al.</i> [152]	2006	Silicon	500	6
Hussain <i>et al.</i> [153]	2014	Silicon	142	1.5
Dayeh <i>et al.</i> [154]	2007	GaAs	6.6k	2

Since the first organic transistor (based on polythiophene) [155] was introduced approximately three decades ago, the development of high-performance organic semiconductors has been intensive. The carrier mobility of the early reported organic materials was a dismal $\sim 10^{-5}$ cm²/Vs [155] and has improved substantially to a present-day high of ~ 40 cm²/Vs for *p*-type semiconductor (pentacene crystalline thin film) [156] and ~ 11 cm²/Vs for *n*-type semiconductor (Fullerene (C₆₀)) [157].

In terms of chemical structure, organic materials can be generally classified as small molecule semiconductors and polymer semiconductors. The former typically features higher carrier mobility than the latter; while the latter usually offers better print-ability (e.g., better solubility, and more uniform layer surface). For the organic

semiconductor, there are largely two main deposition/patterning methods: vapor-phase deposition and solution-based processing.

Small molecular semiconductors are usually deposited/patterned by vapor-phase deposition method (e.g., thermal evaporation) [158, 159] because they typically have relatively poor solubility. The vapor-phase deposition process is mainly based on the evaporation of the organic semiconductor materials by heating in a vacuum chamber. Due to the lack of a solvent, there is no chemical reaction between different layers, leading to the ease of building multiple-layer structure for the transistor. Additionally, the electrical performance realized by vapor-phase deposition is typically better than that realized by solution-based processes. However, the vapor-phase deposition is relatively expensive due to the material wastage and the associated high-cost equipment. To mitigate the material wastage, the organic vapor-phase deposition (OVPD) [160] method was reported in mid 1990's. In this method, the only places where the deposition can happen on the substrate are that located at the cooled reactor end.

There are many types of small molecule semiconductors in terms of molecular structure. The first type is the acenes-based semiconductors. Pentacene, a small molecule acene-based semiconductor, is widely used as the *p*-type semiconductor due to its relatively high mobility. For instance, a high $\sim 40 \text{ cm}^2/\text{Vs}$ was reported based on pentacene crystalline thin film [156]. When deposited as thin film, pentacene also features highly orientated morphology, high stability in ambient environment, and good compatibility with most electrode metals, such as aluminum and gold [161]. Pentacene is generally not readily solution-processable, and requires complex processing, such as vacuum vapor-phase deposition, thereby limiting their applicability for low-cost Printed Electronics applications.

Not unexpectedly, acenes-based derivatives of pentacene with better solution-processability and high carrier mobility continue to be intensely investigated by the Printed Electronics community [162, 163]. For example, TIPS-Pentacene, product of modifications to the herringbone-structured pentacene, has two bulky side groups which lead to regular π - π stacking arrangements and good solubility in organic solvents. Giri *et al.* [164] recently reported carrier mobilities up to $\sim 11 \text{ cm}^2/\text{Vs}$ by controlling TIPS-Pentacene shear strain applied in blade coating under optimum growth conditions.

The second type of small molecule semiconductors are those based on fused heteroacene materials. For instance, triethylsilylethynyl anthradithiophene (TESADT) [165] and difluorinated (di-F) TESADT [166] offer similar performance to TIPS-Pentacene. Benzothieno(3,2-b)(1)benzothiophene (BTBT), another heteroacene semiconductor, reportedly achieved a high mobility of $\sim 10 \text{ cm}^2/\text{Vs}$ [167]. Minemawari *et al.* [168] reported some of the highest mobilities (maximum = $31.3 \text{ cm}^2/\text{Vs}$, average = $16.5 \text{ cm}^2/\text{Vs}$) for solution-based organic transistors by using 2,7-dioctyl(1)benzothieno(3,2-b)(1)benzothiophene (C_8 -BTBT) as the semiconductor.

There are some other small molecular semiconductors with reportedly high performance. Titanylphthalocyanine (TiOPc, a tetrathiafulvalene derivative) [169] has been reported with a high mobility of $\sim 10 \text{ cm}^2/\text{Vs}$. Dithiophene-tetrathiafulvalene (DT-TTF) realized transistors [170] was reported with mobilities up to $\sim 3.6 \text{ cm}^2/\text{Vs}$. Hexamethylene-tetrathiafulvalene (HM-TTF) crystal [171] that is solution grown has achieved high mobility of $\sim 10 \text{ cm}^2/\text{Vs}$.

Table 2-6 summarizes the basic performance of the above reported small molecule semiconductors.

Table 2-6 Summary of small molecular semiconductors

Reference	Year	Semiconductor	Mobility (cm ² /Vs)	Supply Voltage (V)
Palstra <i>et al.</i> [156]	2007	Pentacene	40	10
Giri <i>et al.</i> [164]	2013	TIPS-Pentacene	11	100
Lee <i>et al.</i> [165]	2009	TESADT	0.36	50
Gundlach <i>et al.</i> [166]	2008	DiF-TESADT	0.1	60
Minemawari <i>et al.</i> [168]	2011	C ₈ -BTBT	31.3	50
Li <i>et al.</i> [169]	2007	TiOPc	10	60
Leufgen <i>et al.</i> [170]	2008	DT-TTF	3.6	16
Zhang <i>et al.</i> [171]	2009	HM-TTF	10	150

In this PhD program, TIPS-pentacene is selected as the organic semiconductor material due to its relatively high carrier mobility and easy morphology control during the solution deposition.

Compared to small molecule semiconductors, polymer semiconductors have better solubility but degraded carrier mobility. Although fully amorphous polymers have low motilities ranging from 10⁻³cm²/Vs to 10⁻²cm²/Vs [172-174], the most widely reported conjugated polymers have been those with semicrystalline lamellar microstructures and edge-on polymer orientation which is similar to those found in poly(3,3'-dialkyl-quaterthiophene) (PQT-12) [175] and regioregular poly(3-hexylthiophene) (P3HT) [176]. PQT-12 in a hot dichlorobenzene solution spin coated under ambient conditions achieved a low mobility of ~0.1cm²/Vs, and but high I_{on}/I_{off} of ~10⁷ [175]. Regioregular P3HT in an inert atmosphere was reported to have a carrier mobility of ~0.1cm²/Vs and a relatively high I_{on}/I_{off} of ~10⁶ [176]; while poorer mobility and significantly lower I_{on}/I_{off} were resulted when fabricated in ambient environment [177]. An excellent realization of highly-semicrystalline structure is in

Poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene (PBTTT), with which a mid-high mobility of $\sim 1.1 \text{ cm}^2/\text{Vs}$ [178] has been reported.

At present, there is intensive research effort on donor-acceptor copolymers which have significant larger conjugated and more complex backbone than BTTT and P3HT. As the donor-acceptor copolymers typically have alternating electron rich and electron deficient units along the backbone, the ensuing band gap is relatively low, thereby facilitating intramolecular charge transfer transition between the electron deficient and electron rich units. An early example for the high-mobility donor-acceptor copolymers is cyclopentadithiophene and benzothiadiazole (CDT-BTZ) [179]. CDT-BTZ has high mobility up to $\sim 3.5 \text{ cm}^2/\text{Vs}$ [180] when dip coated on the SiO_2 gate dielectric layer and up to $\sim 5.5 \text{ cm}^2/\text{Vs}$ [181] when grown by drop casting. Diketopyrrolopyrrole (DPP) is a donor-acceptor copolymer which is presently actively researched at present. By using DPP copolymer with thienothiophene-based acceptor units (DPP-DTT-based polymer), Ong *et al.* [182] reported a high mobility of $\sim 10 \text{ cm}^2/\text{Vs}$. Two other promising classes of donor-acceptor copolymers are indacenodithiophene (IDT)- and isoindigo (IID)-based polymers. An IDT-based copolymer with benzothiadiazole (IDT-BT) was recently reported [183] with a high mobility of $\sim 3.6 \text{ cm}^2/\text{Vs}$. An recently reported IID-based copolymer [184] also achieved a high mobility of $\sim 1.9 \text{ cm}^2/\text{Vs}$.

The basic performance of above reported *p*-type polymer semiconductor materials is summarized in Table 2-7.

Table 2-7 Summary of *p*-type polymer semiconductors

Reference	Year	Semiconductor	Mobility (cm ² /Vs)	Supply Voltage (V)
Sirringhaus <i>et al.</i> [176]	1998	P3HT	0.10	80
Ong <i>et al.</i> [175]	2004	PQT-12	0.14	60
Sirringhaus <i>et al.</i> [185]	2000	F8T2	0.015	60
Hamadani <i>et al.</i> [178]	2007	PBTTT	0.70	60
Müllen <i>et al.</i> [181]	2012	CDT-BTZ	5.5	60
Ong <i>et al.</i> [182]	2012	DPP-DTT-based polymer	10.0	60
McCulloch <i>et al.</i> [183]	2013	IDT-BT	3.6	60
Lei <i>et al.</i> [184]	2012	IID	1.9	100

At present, the *n*-type organic semiconductor lags its *p*-type counterparts. To realize an *n*-type organic semiconductor, the injections of electrons into the HOMO level are needed. However, the high work functions of the commonly used metals for electrodes are better suited for holes injections into the HOMO level (*p*-type). Some low work function metals, such as Mg and Al, can be used to improve the electron injections but suffer from poor stability (e.g., easy oxidation) in ambient environment.

A crucial consideration when designing an *n*-type organic semiconductor is its ambient stability. The instability of *n*-type materials is typically due to the vulnerability of electron charge carriers to O₂ and H₂O. There are basically two strategies to improve the ambient stability of *n*-type materials. The first one is to use large size substituents, such as fluorocarbon substitutions, instead of typical N,N'-alkyl substituents at the N,N'-positions. This strategy helps prevent the diffusion of O₂ and H₂O by creating a hydrophobic layer and solid-state atmospheric barriers which are close-packed. The second strategy is to introduce highly electron affinity groups, such as cyanogroup and chloration to lower the LUMO levels. According to these two strategies, there are many *n*-type semiconductors designed, such as the

naphthalene diimide (NDI) and perylene diimide (PDI) derivatives, N,N'-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13), and tetrachlorinated diperylene bisimide (C12-4ClDiPBI).

C₆₀ can be used as *n*-type semiconductor with a reported high mobility of ~11cm²/Vs [157]. This high mobility is obtained on the basis of single crystals which are formed by droplet-pinned crystallization process. Nevertheless, the synthesis of C₆₀ is difficult and its ambient stability is poor, limiting its use in practical applications.

The basic performance of above reported *n*-type semiconductor materials is summarized in Table 2-8.

Table 2-8 Summary of *n*-type semiconductors

Reference	Year	Semiconductor	Mobility (cm ² /Vs)	Supply Voltage (V)
Joon <i>et al.</i> [186]	2010	NDI	1.43	100
Yue <i>et al.</i> [187]	2012	Hybrid NDI and PDI	0.25	100
Tatemichi <i>et al.</i> [188]	2006	PTCDI-C13	2.1	100
Wang <i>et al.</i> [189]	2012	C12-4ClDiPBI	0.14	50
Bao <i>et al.</i> [157]	2012	C ₆₀	11.0	120

In this PhD program, there is little emphasis on *n*-type organic semiconductors. It is nevertheless is a future research field delineated in Chapter 6.

2.3.2.2 Chain 2: Patterning/Printing Processes

Fig. 1-1 earlier in Chapter 1 depicts the various patterning/printing processes [4]. For sake of readability, it is redrawn in Fig. 2-5 below.

Fig. 2-5 Printed Electronics: patterning processes; adapted from [4]

As depicted in the figure and delineated earlier, the patterning/printing technologies can in general be classified as ‘Subtractive’ and ‘Additive’ processes. The Subtractive processes, including Photolithography [100] and Laser Ablation [57], are akin to the established IC fabrication processes. Compared to Additive processes, they are advantageous in terms of higher resolution, and their printed devices are typically substantially faster, i.e., higher carrier mobility. They are, nevertheless, disadvantageous in a number of aspects. These include being a substantially more expensive, not-on-demand printing (i.e., slow to print), ‘not-green’ (i.e., typically requiring toxic chemicals for lift-off and etching) and not-scalable (i.e., incompatible with large area printing). These disadvantages largely contravene the often touted attractive attributes of the ‘printing press’ Printed Electronics.

The Additive processes, including inkjet, flexographic, gravure, offset and screen printing, are akin to printing processes used for graphic arts – they are hence largely

‘printing press’ Printed Electronics with the aforesaid attractive attributes. When compared to Subtractive process, Additive process suffers from lower resolution (20~100 μ m), hence lower circuit density and reduced speed (lower carrier mobility). Nevertheless, these shortcomings are largely mitigated by the lower cost offered by Fully-Additive Printed Electronics.

Other than the classification of Subtractive and Additive, the various printing processes may be classified with respect to different features, such as pattern type, contact mode, analog or digital, and scalability. These features of various printing methods are tabulated in Table 2-9.

In terms of contact mode, the printing processes may be classified as contact printing and non-contact printing. In most printing processes (such as flexography and gravure printing), physical contact is needed between the underlying material or substrate and the materials to be printed. This contact can cause several undesired effects, such as contamination, and perturbation of the physical structure of the underlying layer. A few printing processes (mainly jet printing methods, such as inkjet printing, and aerosol jet printing) are able to print materials with no physical contact with underlying material or substrate.

The printing processes may also be classified as analog and digital printing processes. Analog processes (such as screen, flexography, and gravure printing) typically use physical masters for the layer patterning while digital processes (such as inkjet and aerosol jet printing) usually do not involve physical masters. In this sense, analog and digital printing processes are also sometimes respectively classified as printing processes that use physical masters and processes that do not use physical masters.

Table 2-9 Feature comparison of patterning processes⁺

Printing Process*	Subtractive/ Additive	Pattern type	Contact	Analog/ digital	Scalable
Photolithography	Subtractive	Indirect	Photolithography	Analog	No
Photolithography R2R	Subtractive	Indirect	Photolithography	Analog	Yes
Laser ablation	Subtractive	Indirect	Non-contact	Digital	Partially
Laser ablation R2R	Subtractive	Indirect	Non-contact	Digital	Yes
Imprinting	Subtractive	Indirect	Contact	Analog	Yes
Nanoimprint lithography (Nanoimprint)	Subtractive	Indirect	Contact	Analog	Yes
Inkjet	Additive	Direct	Non-contact	Digital	Partially
Aerosol jet	Additive	Direct	Non-contact	Digital	Partially
e-jet (electro- hydrodynamic printing)	Additive	Direct	Non-contact	Digital	No
Flatbed screen	Additive	Direct	Usually contact	Analog	Yes
Rotary screen	Additive	Direct	Contact	Analog	Yes
Flexography	Additive	Direct	Contact	Analog	Yes
Gravure	Additive	Direct	Contact	Analog	Yes
Gravure offset (Pad)	Additive	Direct	Contact	Analog	Yes
Offset lithography	Additive	Direct	Contact	Analog	Yes
Soft lithography (e.g., micro contact printing)	Additive	Direct	Contact	Analog	Partially

⁺ Note that these are general features of the various processes, and because of the large diversity of the various printing methods, there are exceptions to the specific processes. These exceptions may hence make the specific classifications contentious.

Scalability is another attribute that can be used for classifying the printing processes. There is various reported work [94, 190, 191] that are largely in research settings (such as deposition/patterning on wafer) which are difficult to scale up. Arguably, the most scalable process are the roll-to-roll processes which feature high printing throughput and printing in large formats.

In general, there are tradeoffs between high throughput and high resolution for the various printing processes. For instance, Additive processes have high throughput but suffer from relatively poor resolution, while Subtractive processes have much better resolution but suffer from low throughput. Furthermore, cost is closely related to process throughput. Slow laborious processes usually lead to undesired high cost.

In this thesis, we generally classify the printing processes into Subtractive processes and Additive processes. The main reason for this classification vis-à-vis other classifications is because this classification provides a simple unambiguous indication of some most desired attributes of Printed Electronics, such as low cost, on-demand, green, and scalability – these attributes are imperative for mass production. In this thesis, several commonly employed processes will be reviewed herein and their advantages and limitations will also be discussed.

2.3.2.3 Chain 3: Display/Lighting/Power Source/Communications/Sensors/Circuits

The challenges in Printed Electronics circuit design will be briefly discussed herein. The first challenge in Printed Electronics circuit design is the significantly lower (typically three to four orders of magnitude lower) carrier mobility and poorer resolution (typically ranging from $\sim 10\mu\text{m}$ to $>100\mu\text{m}$, and the ensuing long channel length) of printed transistors compared to established silicon transistors in typical CMOS foundry processes, e.g., 180nm CMOS. This low carrier mobility and poor resolution lead to very limited speed digital and analog circuits – in a ‘general’ sense, severely limiting the application space of Printed Electronics. Although this ‘general’ view does not account for the unique attributes offered by Printed Electronics (including low cost, greenness, on-demand and large format printing, and substrate flexibility), the low carrier mobility and poor resolution challenges would render Printed Electronics as complementary to conventional silicon and not a ‘competing’ technology.

For analog circuit design, the low carrier mobility severely limits the speed of printed transistors. In the context of the basic analog operational amplifier (op-amp) building block embodying these low-speed transistors, its ensuing open-loop (feed-forward) gain and gain-bandwidth (GBW) are severely limited. When viewed in the perspective of contemporary analog circuit designs where the op-amp is a basic building block, a predictable consistent and repeatable closed transfer function due to the application of negative feedback is not attainable. This is because negative feedback requires a high open-loop gain in the operating frequency range of interest [192]. In view of these limitations, our view is that contemporary analog signal processing design modalities embodying high open-loop gain op-amps would need to be replaced with ‘classical antiquated’ analog circuit designs.

These classical analog designs are designs where every transistor counts (e.g. in the 1970s), feedback is limited and localized (usually within one or several transistors), designs are open-loop (such as that adopted in radio frequency low noise amplifiers and output power amplifiers), etc. In the contemporary analog circuit design context, these designs are akin to open-loop analog signal processing voltage-mode (and voltage-charge mode) and current-mode transistor circuits [192]. In our view, the appropriate analog designs are low-count transistor designs where transistors are not only expensive (hence used very sparingly) and whose performance is modest.

In digital circuit design, the low carrier mobility implies very limited digital signal processing functionality in terms of the speed of digital processing or ‘intelligence’.

For both digital and analog circuit designs, the challenge of low carrier mobility is further compounded by the carrier mobility degradation when exposed to air and over time. Although this may be somewhat mitigated with encapsulation where the rate of degradation is reduced, in most cases, however, degradation remains an issue [4].

The second challenge in Printed Electronics circuit design is that complementary (n -type and p -type) transistors are generally unavailable [193, 194], i.e., most processes are able to print only uni-polar transistors, usually p -type. In the analog circuit design context, there are a number of issues with uni-polar designs [192, 195], including the difficulty with dc bias, dc level shifting, difficulty with active loads to obtain high impedance for high voltage gain, reduced signal swings, increased power dissipation and lower power-efficiency, etc.

For the digital circuit design, there are also a number of issues [192, 195]. First, the logic level may be significantly degraded. For example, the uni-polar inverter and uni-polar logic gate with typical diode-connected load are equivalently voltage dividers, leading to significant degradation in the output logic level (in terms of reduced output voltage swing) and ensuing reduced noise margin. While with complementary circuits comprising both p -type and n -type transistors, the output can swing close to the supply rails. The second issue in the digital circuit is the relatively low power efficiency of the uni-polar design. The reason is that the typical diode-connected load continuously drains current during operation, resulting in low power efficiency while in a complementary circuit, energy is largely dissipated at switching only. The power issue is a considerable issue because digital circuits typically embody a large number of transistors. For example, the simple 4-bit Intel 4004 microprocessor (also a uni-polar realization in 1971 [196]) embodies 2,300 transistors – this transistor count is far beyond most state-of-the-art printing processes.

The third challenge in Printed Electronics circuit design is the considerably lower I_{on}/I_{off} ($10^2 \sim 10^5$) of the printed transistors compared to that ($>10^7$) of the silicon transistors. For the analog circuit design, the I_{on}/I_{off} ratio is not usually a parameter of concern except where the transistor is used as a switch (i.e., digital modality), for

example in switching circuits such as pulse width modulation circuits in DC-DC converters (power management) [197] and Class D amplifiers [198]. In this modality, the I_{on}/I_{off} ratio is important as these transistors are essentially on-off switches, and a high ratio is needed to adequately define the ‘on’ and ‘off’ states of the transistor. Put simply, I_{on}/I_{off} is a critical parameter for digital designs.

The challenges arising from the low I_{on}/I_{off} in Printed Electronics transistors is further compounded by the depletion-mode operation of most printed transistors – most processes are only able to print depletion-mode transistors [199, 200]. To switch off a depletion-mode transistor, which is otherwise ‘normally-on’ when the gate voltage is between 0 to V_{DD} , a negative driving voltage is required. This complicates the system design as a negative supply voltage which is not generated by the digital circuit itself is required.

The low I_{on}/I_{off} further results in the degradation of the output voltage level and ensuing reduced noise margin. This means that at some point in a cascade of digital circuits the voltage output is insufficient for a digital input that defines a logic ‘1’. This can be observed in the voltage swings of several reported ring oscillators where the output voltage of the inverters decreases as signal propagates through the inverters.

The low I_{on}/I_{off} also pertains to ‘fan-in’ and ‘fan-out’ of digital circuits. With low I_{on}/I_{off} , the ‘fan-out’ issue needs to be considered due to the limited I_{on} current. Additionally, the ‘fan-in’ to a logic gate also needs to be carefully considered as a higher ‘fan-in’ may lead to even smaller I_{on} (due to longer transistor paths) and higher I_{off} (due to more parallel transistor paths).

The fourth challenge in Printed Electronics circuit design is the high process variations in Printed Electronics. Process variations come in many different forms,

and arguably the most important is that of the matching between various printed elements. This challenge is further exacerbated by the different rates of degradation of the various parameters of the printed elements, particularly when they are exposed the environment and aging.

For analog circuit design, as discussed earlier, without the self-correction mechanism from negative feedback, high process variations may lead not only to detrimental effects in circuit functionality but also ambiguities with manufacturability. In the case of a simple Printed Electronics single-stage amplifier, high process variations lead to (open-loop) high gain variations. In the case of a current mirror where the current gain is determined by the transistor aspect ratios, high process variations lead to imprecise output current and ensuing poorly defined current bias (to other branches of the analog circuit).

A more imperative issue pertains to differential-input circuits whose functionality requires precise matching between transistors. Differential-input circuits are prevalent both in analog and digital circuits, in part because well-designed differential-input circuits feature high CMRR. A high CMRR, i.e., a high ratio between the amplification of differential signals over common-mode signals, rejects common-mode signals which are largely noise while amplifying the desired differential signals. This differential modality is the basis of analog differential amplifiers and digital communications (including high reliability Ethernet wired communications, Controller Area Networks in automotive and satellite applications, etc.) for maintaining high signal integrity, etc.

In the case of analog circuits, there are other implications to their performance. These include input voltage offset, distortions such as Total Harmonic Distortion (THD), etc., and for fully-differential circuits, the PSRR.

The effects of process variations on the digital circuits are arguably relatively less severe compared to that on analog circuits. Other than the variations leading to matching issues discussed above, one of the largest variations is the V_{th} variations. An increased V_{th} change for the n -type transistor in a complementary inverter will reduce the noise margin low (and increase the noise margin high) of the inverter as the input voltage needs to be higher to switch on the n -type MOS transistor. If the severity of the variations is not excessive, including the V_{th} variations, the usual outcomes are typically operational variations, such as speed variations for ring oscillators. If V_{th} increases, the speed of digital circuits will slow down; this phenomenon is well established [192].

For both digital and analog circuit designs, excessive process variations may lead to catastrophic failure of circuit functionality and reduced yield/increased rejects in manufactured printed circuits.

2.3.3 Considerations for Designability, Manufacturability and Functionality

Following our review of Printed Electronics processes and circuits and systems, we would now review the reasons for the exiguity from three perspectives: designability, manufacturability and functionality.

2.3.3.1 Designability

For the designability of Printed Electronics circuits/systems, particularly if there is some sophistication thereto, one of the major challenges is the lack of established Process Development Kits (PDKs) [4]. The PDK is a critical constituent of computer-aided-design/Electronic-Design-Automation tools for a given fabrication technology.

It largely embodies the models of the device characteristics, and a set of layout design rules that defines the minimum dimensions for printed devices and minimum distance between them. Not unexpectedly, the PDK is imperative in modern circuits and systems design – for both conventional silicon and Printed Electronics where it facilitates circuits and systems design including the prediction of the performance of the designs under various conditions including statistics of the performance of the manufactured parts.

Our review shows that, at this juncture, comprehensive PDKs for Printed Electronics are unavailable – some transistor models [201-206] have nevertheless been reported. Consequently, the performance of the Printed Electronics circuits and can only largely be estimated but not accurately predicted. The inavailability of PDK is a major disconnect between the Printed Electronics processing community and the circuits-and-systems community, and unless the Printed Electronics PDKs become available, Printed Electronics-only circuits and systems will likely remain nascent in the perspective of manufacturing and the sophistication of Printed Electronics-only circuits and systems will likely remain modest.

To the best of our knowledge, the layout design rules for Printed Electronics PDKs have not been reported probably because they constitute part of important intellectual property of the various research groups. The state-of-the-art transistor models [201-216] will now be reviewed.

To accurately model the transistor characteristics, there are several factors that need to be considered and modeled. First, it is desired to model the printed transistor for all operating regions: from cut-off to linear to the supra-threshold regions. Second, as the carrier mobility of a printed transistor may be affected by the channel length, this effect should be modeled. For example, if the printed semiconductors are based

on small molecular organic materials, the effect of channel length on the carrier mobility is particularly significant. This is because the transistor channel is filled with small semiconductor crystals instead of a film. The crystal boundaries slow the charge carrier speed, leading to reduced carrier mobility compared to the single crystal carrier mobility. Consequently, a shorter channel length may lead to reduced number of boundaries, and the carrier mobility may be significantly improved.

Third, to verify the efficacy of the transistor model, various circuits should be designed, simulated, printed and measured to verify the correlations between simulations and measurements. Fourth, if the substrate of the Printed Electronics circuits and system is expected to be bent, it is then critical that the models of active (transistor) and passive elements (resistor, capacitor, inductor, antennas and interconnects) embody the effects of bending to accommodate the accompanying variations of their parameters; see Chapter 1 earlier.

Table 2-10 tabulates the various reported state-of-the-art printed transistor models. The transistor model described in [201, 202] provided cut-off-to-linear-to-supra-threshold region modeling by a small number of parameters. This model assumes the exponential dependence of the subthreshold current on the gate biasing voltage. The model reported in [207, 208] emphasizes the power-law relationship between the carrier mobility and the gate biasing voltage. In this model, the cut-off region and above-threshold region are independently defined and merged by a transition function. The model reported in [203, 204] considers the potential barrier between different grains in a polycrystalline film. The carrier mobility is derived on the basis of the gate voltage, free carrier density and trapped carrier density.

In Table 2-10, there are several other models reported for printed transistors. We note that several reported models are capable of simulating both the cut-off and the

supra-threshold regions. Most of the reported models feature relatively good fitting capability for the electrical characterization of a single printed transistor.

In the perspective of reported PDKs, we view that there remain several limitations. First, of the reported models, only one reported model [215] embodies the effects of the channel length on the carrier mobility. Second, the efficacy of most of the reported models is somewhat ambiguous as the authors of these papers [201-204, 206-208, 211, 214-216] did not include circuit simulations and circuits measurements in their reported work. Third, it is somewhat surprising that although the bending issue in Printed Electronics transistors and circuits is well known [106], reported models thus far only embody modules when the Printed Electronics transistors are flat but not when they are bent. In other words, at this juncture, an accurate transistor model that can model Printed Electronics transistors when they are bent is lacking. In short, a comprehensive PDK remains lacking in literature.

Table 2-10 Reported models for printed transistors

Reference	Year	All operating regions	Effects of L on μ	Circuits simulation	Circuits measurements verification	Bending
Marinov <i>et al.</i> [201, 202]	2009	Yes	No	No	No	No
Benjamin <i>et al.</i> [207, 208]	2013	Yes	No	No	No	No
Li <i>et al.</i> [203, 204]	2010	Yes	No	No	No	No
Abdinia <i>et al.</i> [205]	2014	Yes	No	Yes	Yes	No
Meixner <i>et al.</i> [206]	2008	No	No	No	No	No
Fadlallah <i>et al.</i> [209, 210]	2007	Yes	No	Yes	Yes	No
Torricelli <i>et al.</i> [211]	2012	Yes	No	No	No	No
Yaghmazadeh <i>et al.</i> [212]	2008	No	No	Yes	No	No
Kaveh <i>et al.</i> [213]	2016	Yes	No	Yes	No	No
Calveti <i>et al.</i> [214]	2005	Yes	No	No	No	No
Maiti <i>et al.</i> [215]	2016	No	Yes	No	No	No
He <i>et al.</i> [216]	2016	Yes	No	No	No	No

For the designability of Printed Electronics, this formidable challenge of the lack of a comprehensive PDK will be addressed in Chapter 5. Particularly, in view of the mechanical flexibility of the substrates, and as delineated above, the comprehensive PDK should include parameters of the circuits elements when they are flat and when bent.

2.3.3.2 Manufacturability

For the manufacturability of complex Printed Electronics circuits/systems, the high process variations are one of the most formidable challenges for the realization of complex Printed Electronics circuits and systems. For sake of predictability, it is imperative that the printing process not only feature low process variations at the juncture of printing but also the degradation be small (hence low ensuing variations) during the lifetime of the Printed Electronics circuits and systems.

As discussed in Section 2.3.2.3, high process variations lead to detrimental effects for both analog and digital circuits. For analog circuit design, as discussed earlier, without the self-correction mechanism from negative feedback, high process variations may lead not only to detrimental effects in circuit functionality but also ambiguities with manufacturability. An imperative issue pertains to differential-input circuits whose functionality requires precise matching between transistors. The effects of process variations on the digital circuit design are arguably relatively less severe compared to that on analog circuit design. Nevertheless, high process variations, particularly V_{th} variations, can cause undesired performance variations. To adequately predict circuit performance, statistical analysis (Monte-Carlo simulations) on the basis of process variations needs to be performed, e.g., by means of PDK and measured variations of individual circuit elements.

It is interesting that despite the large number of reported work on printing, only a few report their variations. From our review, we tabulate in Table 2-11 the reported process variations for Fully-Additive printing processes and Subtractive processes. In the reported Fully-Additive processes [3, 6, 70, 101, 102] on flexible substrates, the typical mobility μ and V_{th} variations are large: approximately $\pm 30\%$ and $\pm 1V$ respectively. As expected, the variations are typically lower in reported Subtractive processes [64, 103]: approximately $\pm 20\%$ and $\pm 0.7V$ respectively.

The processes of note are as follows. Our all-air low-temperature Fully-Additive printing process [1, 6] on flexible substrates features the lowest μ variation of $\pm 4.9\%$. Another Fully-Additive process achieves low mobility μ and V_{th} variations of $\pm 9.5\%$ and $\pm 0.02V$ respectively [101]. Nevertheless this process is somewhat impractical and high-cost due to the use of a silicon stencil, largely unscalable as wafer sizes are limited to 300mm, and the processing requires high temperature ($300^\circ C$; thereby prohibiting the use of low-cost ubiquitous PET substrates) and in nitrogen. The lowest mobility μ and V_{th} variations of Subtractive processes on flexible substrate involves a photolithography process [64] are reportedly $\pm 4.7\%$ and $\pm 0.3V$ respectively. In the perspective of Printed Electronics circuits, these variations are largely insufficient for well-matched transistors pairs for high-precision differential amplifiers.

The reasons for large variations include poor uniformity of each layer's deposition (particularly the semiconductor layer), poor registration in printing processes, and difficulty to print consistent fine pitches/lines/patterns for each layer of the devices due to the rheology of the pastes and the printing processes used.

Table 2-11 Summary of reported Printed Electronics process variations

Reference	Printing Technology	Mean μ (cm^2/Vs)	μ Variations	Mean V_{th} (V)	V_{th} Variations (V)	Printed Circuits
Ours [1, 6]	Screen printing, slot die coating	0.31	4.9%	1.76	± 0.43	Op-amps, and DAC
Kang <i>et al.</i> [24]	Gravure printing, inkjet printing, spin coating	0.5	>60%*	-	-	-
Abbas <i>et al.</i> [217]	Evaporation, spin coating	0.97	17.5%	-14*	-	-
Hwang <i>et al.</i> [218]	Evaporation, spin coating	0.24	33.3%	-1.3	± 0.1	-
Kempa <i>et al.</i> [70]	Flexography printing, gravure printing	p : 0.0039 n : 0.0029	p : 48.7% n : 41.3%	p : -1.5 n : -1	p : ± 6.6 n : ± 7.1	Ring oscillator
Lin <i>et al.</i> [74]	Inkjet printing	0.025	32.3%	-7.8	± 1.2	-
Pierre <i>et al.</i> [102]	Evaporation, blade coating, inkjet printing	0.31	20%	-0.07	± 0.21	-
Hyun <i>et al.</i> [101]	Aerosol jet printing	0.21	9.5%	0.42	± 0.02	-
Kjellander <i>et al.</i> [219]	Inkjet printing, and photolithography	0.5	40%	3.4	± 0.7	-
Baeg <i>et al.</i> [64]	Inkjet printing, photolithography	0.43	4.7%	-3.1	± 0.3	-
Lau <i>et al.</i> [103]	Gravure printing, etching	4.27	37.9%	2.29	± 1.15	-

*Estimated based on reported measurement results

For the manufacturability of Printed Electronics, this formidable challenge of large process variations will be addressed in Chapter 3.

2.3.3.3 Functionality

One of the major attractive attribute of Printed Electronics is the mechanical flexibility of its substrate. This would require the Printed Electronics circuits and systems to retain its functionality when its substrate is bent – i.e., the variations of the printed elements and ensuing circuits and systems to be predictable and within acceptable limits – often a major challenge.

The performance variation for single printed device upon bending is relatively intuitive and largely caused by the changes in the device’s physical dimensions. The

dimension change upon bending is relatively intuitive and it is based on basic physics. Consider the cross section of a device (e.g., capacitor, resistor or transistor) depicted in Fig. 2-6 when it is flat, convexly bent and concavely bent. It can be seen that when a device is convexly bent, it is stretched, i.e., its length increases from nominal a to $a+\theta t/2$. Conversely, when it is concavely bent, it is compressed, i.e., its length decreases from nominal a to $a-\theta t/2$.

Fig. 2-6 Cross section of a device when it is flat, convexly bent and concavely bent

For a capacitor comprising a dielectric layer sandwiched between top and bottom electrodes, the dielectric thickness (d) and the electrode area (A) of the dielectric will similarly be respectively stretched and compressed when the substrate is bent convexly and concavely. As the capacitance of a capacitor is $C = \epsilon A/d$ (ϵ is dielectric permittivity, A is capacitor area, d is dielectric thickness), the ensuing capacitance will change respectively when the substrate is bent. In the case of a resistor where the resistance $R = \rho L/dW$ (ρ is resistivity, L is resistor length, d is resistor thickness, W is resistor width), it can be easily shown that its resistance also varies upon bending.

In the case of a transistor, the effects of bending may not be necessarily intuitive. The reason is that the carrier mobility, other than the physical dimension changes (e.g., the channel length, and the layer thickness), can be affected by the transistor bending. Additionally, both the threshold voltage and the leakage current may also vary upon

bending. Put simply, the variations in the transistor performance upon bending may not only depend on the physical dimension changes, but also depend on the material properties and the printing processes.

Compared to single printed device, the performance variations for printed complex circuits/systems upon bending may be difficult to predict. This difficulty is partially due to the lack of PDKs that accommodate the effects of bending. As a case in point, when a regular (e.g., 100 μm -thick PET) flexible substrate is bent, the variations of the Printed Electronics devices/sensors thereon and the ensuing variations of the performance of the printed circuits/systems may be intractable. In some cases, the variations are so severe that the circuits/systems fail [1].

For completeness, although bending is not a problem if the substrate is very thin ($\sim 2\mu\text{m}$ [107]), this is impractical because such substrates are not only highly frangible but also difficult to handle, hence of very limited applications.

From our review, we note that despite the imperativeness of resolving/mitigating the effects of bending, a comprehensive investigation thereto remains largely incomplete, in part due to the nascency of Printed Electronics. Perhaps somewhat surprising for printed passive elements, including capacitors and resistors, the effects of bending remain largely unreported; reported work [104, 105] hitherto is for transistors. In [104], the transistor bending characterization is based on pentacene-based organic semiconductor realized by an evaporation process. The transistor drain current is increased when compressed and is decreased when stretched. In [105], however, the drain current is reported to be conversely increased when the flexible transistor is stretched. Although the reason for the difference in the effects of bending

is largely unknown, both work show significant transistor drain current variations upon bending.

For printed circuits, the reported effects of bending [111-113] are largely limited to basic inverters (diode-connected) and ring oscillators. In [111, 113], inverters on flexible substrates have significant changes in gain and threshold voltage when they are bent. In [112], both inverter and ring oscillator are characterized for the effects of bending and have moderate performance variations upon bending.

Not surprisingly, an electronic/layout means to mitigate the effects due to bending remains unreported/unresolved. At this juncture, the sole reported non-electronic/layout method [112] involves depositing another substrate layer on top of the device. The encapsulation layer is designed to have the same thickness as the substrate so that the devices can sit near the neutral strain position. As delineated, the inverter and the ring oscillator using this method only experience moderate performance change upon bending. The encapsulation layer used, however, undesirably doubles the overall substrate thickness. Another non-electric/layout method [220] involves placing devices on an area where the bending is minimum which requires a priori information that may not be available, and the application is hence highly restrictive.

For the functionality of Printed Electronics, this formidable challenge of the significant effects due to bending will be addressed in Chapter 4.

2.4 CONCLUSIONS

In this chapter, Flexible Electronics, Hybrid Electronics and Printed Electronics, have been reviewed in turn, including their technological challenges and application space. As the emphasis of our PhD program is Printed Electronics, our review focused on Printed Electronics, including the complete supply chain and the challenges and solutions thereto.

As a general concluding remark, Flexible Electronics, Hybrid Electronics and Printed Electronics remain largely nascent and the challenges are formidable in virtually all aspects, including from a circuits and systems design perspective.

Chapter 3 Fully-Additive Low-Cost Printed Electronics with Very-Low Process Variations

3.1 INTRODUCTION

A large portion of this chapter is extracted from our publication [1] recently published in the IEEE Transactions on Electron Devices.

In this chapter, we address the challenges in Printed Electronics largely from the manufacturability perspective. Particularly, as earlier delineated in Chapters 1 and 2, the major challenge in manufacturability is high (process) variations of the printed elements which ultimately lead to the exiguity of manufactured Printed Electronics-only circuits and systems. In this chapter, we will describe our proposed Fully-Additive Low-Cost All-Air-Processed Low-Temperature ($<120^{\circ}\text{C}$) screen printing process which features very-low (in the perspective of Printed Electronics) μ variations ($\leq \pm 5\%$) and very-low V_{th} variations ($\leq \pm 0.43\text{V}$) – the first and second chains of the entire Printed Electronics Supply Chain in Fig. 1-2. The low temperature allows realization on low-temperature low-cost flexible substrates such as PET and PC substrates, and the screen printing process allows scalability (large format printing).

Of specific interest, to the best of our knowledge, the μ variations of our proposed process are the lowest of all Fully-Additive processes to date – substantially lower than that of typical Fully-Additive printing processes ($\pm 30\%$ μ variations and $\pm 1\text{V}$ V_{th}

variations) [3, 6, 70, 101, 102] and is comparable to the lowest of Subtractive processes ($\pm 4.7\% \mu$ variations and $\pm 0.3\text{V } V_{th}$ variations) [64].

From a circuits/systems perspective, the very-low variations are very worthwhile, as it is crucial for printed circuits functionality and the ensuing manufacturability. To depict the imperativeness of the need for low variations, consider the following for the aforesaid combined $\pm 30\% \mu$ and $\pm 1\text{V } V_{th}$ variations of typical Fully-Additive processes against our very low $\pm 4.9\% \mu$ and $\pm 0.43\text{V } V_{th}$ variations. For the basic ring oscillator (Fig. 3-1(a)), the variations of its oscillating frequency and failure rate drop significantly from $\pm 13.5\%$ and 17% to $\pm 1.9\%$ and 0% respectively. For the basic digital gate (Fig. 3-1(b)), the delay variations similarly improve significantly from $\pm 195\%$ to $\pm 74\%$. For the basic analog differential amplifier (Fig. 3-1(c)), the gain and input offset variations improve markedly from $\pm 23.6\%$ and $\pm 2.8\text{V}$ to $\pm 2.63\%$ and $\pm 0.5\text{V}$ respectively.

In this chapter, further to said variations, we investigate the effect of layout to the matching of two printed transistors as an indication of the variations between two transistors – this pertains to the third chain of the Printed Electronics supply chain in Fig. 1-2. Interestingly, to the best of our knowledge, there is no reported work on the matching of printed transistors by means of specific layout methodologies. This work is significant because good matching between two printed transistors is imperative in many analog circuits, e.g., differential op-amps, and in some digital circuits; see Chapter 2 earlier.

We show herein that by means of 2D common centroid layout vis-à-vis simple layout, we dramatically improve the matching between two transistors for our proposed very-low variations process by 3.4x – from 7.2% to 2.1% . This is marked

improvement over that of Fully-Additive processes (e.g., our earlier process [6]) with $\pm 30\% \mu$ and $\pm 1V V_{th}$ variations, where the matching between two printed transistors improves from 48.4% to 8.7% for the same layout. It is interesting to note that because of the very-low variations of our proposed process, the matching between two simple-layout transistors printed using our process is better than that of the two 2D common centroid layout transistors of processes with typical $\pm 30\% \mu$ and $\pm 1V V_{th}$ variations. Practically, this is worthy because the area required of the simple layout is $\sim 40\%$ smaller – particularly pertinent for low-cost Fully-Additive processes because the minimum feature size is typically large ($>20\mu m$).

Fig. 3-1 Schematic of (a) A basic ring oscillator with diode-connected active loads, (b) A basic gate source connected digital inverter, and (c) A basic analog differential amplifier

This chapter is organized as follows. Section 3.2 describes our proposed Fully-Additive printing process. Section 3.3 presents the results and discussion. Finally, conclusions are drawn in Section 3.4.

3.2 FULLY-ADDITIVE PRINTING PROCESS

Fig. 3-2(a) and (b) illustrate the fabrication steps of transistors using our proposed Fully-Additive screen printing process on a PET flexible substrate. These fabrication steps are similar to our process steps stipulated in Chapter 2 save the semiconductor deposition and composition. Both active and passive components are screen printed on the PET substrate, using a DEK Horizon screen printer. All layers are printed in air and the maximum temperature involved is a low 120°C. The bottom-gate transistor structure realized is depicted in Fig. 3-2(c).

(a)

Fig. 3-2 Our Fully-Additive printing on flexible substrates: (a) Screen printing process, (b) Blade coating of semiconductor layer, and (c) Transistor structure

It is well-established [221] that the process variations of transistors are affected by the choice of deposition methods and composition of the semiconductor layer. Typical approaches for the deposition include spin casting [222], spin coating [24] and blade coating [102]. While these methods achieve relatively good electrical performance and somewhat uniform devices, their respective reported process variations are high. Specifically, for spin-cast, inkjet and blade coating, their μ variations are respectively $\pm 31\%$ [222], $\pm 60\%$ [24] and $\pm 20\%$ [102]. In general, as the simple and large area compatible blade coating method yield lesser transistor performance variations compared with other semiconductor deposition methods, we adopt the blade coating method. For this reason, our Fully-Additive printing process embodies the blade coating method.

Blending two or more material components [223] such as the integration of small molecules with polymeric matrices provides a means for greater morphological control of the semiconductor active layer during film formation. For example, the blending of TIPS-Pentacene and various polymers (e.g., polycarbonate [224], poly(α -methylstyrene) (P α MS) [225] and polystyrene (PS) [223]) reportedly enhances the carrier mobility and semiconductor film uniformity, thereby resulting in reduced variations. However, most reported work on polymer-small molecule blend has to date been carried out on rigid substrates such as silicon wafer and glass [225] or in controlled environment such as nitrogen [102, 223] – incompatible to flexible and low-cost Printed Electronics. Conversely, we propose to blade coat a blend of TIPS-Pentacene with PS onto a flexible PET substrate, and all the printing steps are in an air environment and involve only low-temperature processing (e.g., <120°C).

The film crystallinity in solution-based processes is strongly influenced by the choice of the solvent. Notably, a dual-solvent approach [25] reported that the addition of a more polar solvent to the main solvent is potentially beneficial as it enhances both the crystallization of small molecules and the solubility of the polymer. This effectively improves the control of the deposition process by tuning the rheological properties of the solution vis-à-vis the need for post-deposition or environment optimization. In our proposed Fully-Additive printing process, a dual-solvent system, comprising the main solvent toluene added with a more polar solvent anisole, to enhance device-to-device uniformity is applied in conjunction with a semiconducting blend.

3.2.1 Fully-Additive Printing Process for Transistors

The PET substrate is first cleaned. With the first stainless steel mask (400 mesh count), the gate layer is screen printed using silver paste (DuPont 5028 [226]) and is then cured at 120°C for 10 minutes. With the second stainless steel mask (325 mesh count), the dielectric layer is screen printed over the gate layer using dielectric paste (DuPont 5018 [226]) and is then UV cured (Fusion UV Curing System) on a conveyor belt with speed of 20ft/min at UV power of 350W/inch. With the third stainless steel mask (400 mesh count), the drain and source layer is screen printed on top of the dielectric layer and is then cured at 120°C for 10 minutes. Before the deposition of the semiconductor layer, the drain/source layer is treated with a 10mM solution of Pentafluorobenzenethiol (PFBT, Sigma Aldrich) in ethanol to improve the metal/organic contact [6]. The semiconductor layer is realized by blade coating the semiconductor solution comprising of a blend of TIPS-Pentacene (Sigma Aldrich) and polystyrene (MW 400,000, PDI 1.06, Regent Chemicals) dissolved in a dual solvent system containing toluene and anisole. As in typical blade coating, the substrate is placed on a temperature-controlled vacuum suction plate and preheated to the desired coating temperature. The process fluid is dispensed and the blade is precisely moved relative to the substrate. The semiconductor blend is blade coated with our optimized process parameters (20 vol% anisole in dual solvent system, 60°C coating temperature and 0.2mm/s coating speed), followed by curing for 30 minutes at 90°C.

3.2.2 Fully-Additive Printing Process for Passive Elements

After the PET substrate is cleaned, the first layer (bottom electrode of a capacitor (DuPont 5018 [226]), a resistor (DuPont 5036 and DuPont 7082 [226]) or an inductor

(DuPont 5018 [226]) is screen printed with a stainless steel mask (200 mesh count) and is then cured at 120°C for 10 minutes. In the case of the capacitor where a dielectric layer is required, the dielectric layer of the capacitor is subsequently screen printed using the second stainless steel mask (325 mesh count) and is then UV cured on a conveyor belt with speed of 20ft/min at UV power of 350W/inch. With the third stainless steel mask (400 mesh count), the top electrode layer of the capacitor is finally screen printed (DuPont 5018 [226]) and it is cured at 120°C for 10 minutes. The capacitance of printed capacitors ranges from 223.8pF/cm² for the single dielectric layer to 1.1nF/cm² for the quintuple dielectric layer capacitor. The resistance of printed resistors can be adjusted by means of the ink composition/blending and ranges from <10Ω/□ to 800kΩ/□. Depending on the size of printed inductors and the operating frequency, the inductance of the printed inductor ranges from 1μH to 8μH with quality factor $Q > 10$ at 10MHz. This Q is sufficient for many applications, including the 13.56MHz RFID.

3.3 RESULTS AND DISCUSSION

In this section, investigations leading to optimized process parameters used for our Fully-Additive printing process, e.g., semiconductor materials and coating conditions, are delineated. The primary optimization considerations are to minimize mobility μ and V_{th} variations. Our proposed polymer-small molecular blend compared to non-blend approach is first investigated. The investigation is carried out not only for the process performance (at the point of printing) but also for performance degradation after 3 months. Our proposed dual solvent system used for our blend is thereafter investigated with respect to the volume percentage of anisole used in the semiconductor solution. Following this, the blade coating conditions for the

semiconductor layer, including coating temperature and coating speed, are investigated. Finally, we investigate the associated mismatch between two transistors printed by our optimized Fully-Additive printing process, and how layout affects mismatch. The ensuing implications of the mismatch with respect to the printed area and to circuits/systems are also succinctly discussed.

3.3.1 Process Investigations

3.3.1.1 TIPS-Pentacene/PS Blend vs TIPS-Pentacene

We employ our TIPS-Pentacene/PS blend in our semiconductor layer deposition because of its relatively high mobility and good film formation uniformity. Fig. 3-3 and Fig. 3-3 depict the optical differences between the TIPS-Pentacene non-blend (Fig. 3-3(a) and Fig. 3-3(b) respectively) and our TIPS-Pentacene/PS (1:1 wt%) blend and from atomic force microscopy (AFM) 3D images (Fig. 3-4(a) and Fig. 3-4(b) respectively). It can be observed that the formation of the crystals by blade coating our blend is substantially more benign than of the non-blend, particularly that the formation of the crystals are significantly larger and more homogenous with smaller morphological anisotropy. The ensuing surface roughness of the channel area from our blend, as expected, is substantially lesser – $0.146\mu\text{m}$ vis-à-vis $0.370\mu\text{m}$ of the non-blend.

Fig. 3-3 Optical micrograph: (a) Non-Blend (TIPS-Pentacene), and (b) Our Blend (TIPS-Pentacene/PS)

Fig. 3-4 AFM 3D image of the channel: (a) Non-blend (TIPS-Pentacene), and (b) Our blend (TIPS-Pentacene/PS)

These ensuing attributes of transistors based on our blend over the non-blend are very worthy. First, because of the formation of large crystals – sufficiently large to cross the channel, thereby connecting the source and drain – the ensuing μ is greatly enhanced. Specifically, the μ of our blend is $0.308 \text{ cm}^2/\text{Vs}$ against $0.025 \text{ cm}^2/\text{Vs}$ of the non-blend, i.e., 12.4 times improvement. This improvement is evident from the I-V transfer characteristics of the printed transistor depicted in Fig. 3-5 where for the same gate-source voltage, V_{GS} , the drain current, I_{DS} , of the transistor based on our blend is over an order of magnitude higher than that of the non-blend.

Fig. 3-5 I-V transfer characteristics of transistors based on our blend and non-blend at the point of printing and at the 3-month juncture

Second, as expected from the improved morphology of the channel area by using our polymer-small molecule blend, the device-to-device uniformity of the transistors is enhanced considerably. Specifically, transistors based on our blend exhibit mobility μ

and V_{th} variations of $\pm 4.9\%$ and $\pm 0.43\text{V}$ respectively compared to the significantly larger $\pm 16.5\%$ and $\pm 1.8\text{V}$ respectively of the non-blend.

Third, perhaps somewhat unexpected, the transistors based on our TIPS-Pentacene/PS blend exhibit substantially lesser aging effects compared to the non-blend counterparts. Specifically, as depicted in Fig. 3-5, the μ degradation (after 3 months) of transistors based on our blend is only slight, at 35% compared to that at the juncture of printing. Conversely, the μ degradation of the non-blend counterparts is substantially larger, at 82%. Put simply, at the 3-month juncture, the μ of transistors based on our blend is 45 times higher than that of the non-blend against 12.4 times at the point of printing. The reduced degradation of the former can be attributed to the innate in-situ encapsulation of the channel semiconductor by the insulating polymer (PS) in our blend.

Fourth, further to said third for degradation after a 3-month juncture, the V_{th} and the I_{on}/I_{off} changes of transistors based on our blend are also substantially smaller than that of the non-blend counterparts. Specifically, the V_{th} and I_{on}/I_{off} of the former and latter change from 1.76V and 3.9×10^5 to 2.34V and 3.2×10^5 respectively, and from 3.06V and 1.8×10^5 to 10.66V and 2.9×10^2 respectively. The mitigated degradation is likewise attributed to said innate in-situ encapsulation.

The aforesaid four attributes are imperative from a circuits/systems perspective. The greatly enhanced carrier mobility results in improved operational speed of printed circuits, such as increased oscillating frequency of the digital ring oscillator, smaller delay of the inverter and higher gain and wider gain-bandwidth of an analog amplifier. As discussed in the introduction, the smaller transistor mobility μ and V_{th} variations based on our blend lead to reduced performance variations of printed circuits, such as

smaller variation of the oscillation frequency for the digital ring oscillator, reduced variation of the delay for the inverter and smaller variations of the gain and offset for the analog amplifier. The aforesaid reduced performance variations based on our blend lead to ensuing worthy improved manufacturability of Printed Electronics circuits/systems. The reduced aging effect of the transistors based on our blend is essential for more consistent printed circuit performance over time, thereby prolonging the lifetime of the Printed Electronics circuits/systems.

3.3.1.2 Dual Solvent System

The volume percentage of anisole in our dual solvent system (anisole and toluene) is investigated as a means to optimize the channel crystallization during the blade coating of our TIPS-Pentacene/PS blend. The micrographs of the channel area of the printed transistors are shown in Fig. 3-6(a), (b) and (c) respectively for 0 vol%, 20 vol% and 40 vol% volume percentage of anisole in our dual solvent system. Table 3-1 summarizes several parameters of transistors based on our blend for varying volume percentages of anisole.

Fig. 3-6 Micrographs of printed transistors based on our blend with varying volume percentages of anisole: (a) 0 vol%, (b) 20 vol% (as in Fig. 3(a)), and (c) 40 vol% in dual solvent system

Table 3-1 Transistors performance with varying volume percentages of anisole in our dual solvent system. The mean is obtained from 40 samples.

Vol% Anisole	μ Mean $\pm$ Variations (cm ² /Vs)	V_{th} Mean $\pm$ Variations (V)	I_{on}/I_{off} Mean $\pm$ Variations
0 vol%	0.119 $\pm$ 9.2%	2.71 $\pm$ 2.40	1.0 $\pm$ 0.5 $\times 10^5$
10 vol%	0.276 $\pm$ 6.7%	2.46 $\pm$ 1.89	2.2 $\pm$ 1.0 $\times 10^5$
20 vol%	0.308 $\pm$ 4.9%	1.76 $\pm$ 0.43	2.4 $\pm$ 1.1 $\times 10^5$
30 vol%	0.267 $\pm$ 6.6%	1.86 $\pm$ 0.55	1.2 $\pm$ 0.5 $\times 10^5$
40 vol%	0.282 $\pm$ 5.5%	1.80 $\pm$ 0.75	1.4 $\pm$ 0.8 $\times 10^5$
50 vol%	0.232 $\pm$ 6.1%	2.08 $\pm$ 0.62	0.8 $\pm$ 0.5 $\times 10^5$

From these micrographs, we observe an increase in crystal formation size and improved morphology in the channel area as the vol% of anisole increases. These may be attributed to the plasticization effect of anisole on the PS molecule. From Table 3-1, the optimum parameters are obtained for 20 vol% anisole where the maximum mean μ (0.308 cm²/Vs), highest I_{on}/I_{off} (2.4 $\times 10^5$) and lowest mean V_{th} (1.76V) are obtained. In this composition, the μ ($\pm 4.9\%$) and V_{th} ($\pm 0.43V$) variations are also minimum. Of particular interest, these parameters are substantially better than that for the single solvent (0 vol% anisole).

In general, where there is insufficient vol% anisole, the crystal formation size is smaller and somewhat oriented (Fig. 3-6(a)) due to the high solvent evaporation rate. This leads to low μ , high V_{th} , and high mobility μ and V_{th} variations. Conversely, when there is excessive vol% anisole, the crystal formation is somewhat larger and tends to be increasingly distorted (Fig. 3-6 (c)) due to high crystallization rate of the small molecule in our blend. The ensuing μ remains relatively high, V_{th} relatively low, variations of mobility μ and V_{th} relative low, but I_{on}/I_{off} decreases.

3.3.1.3 Coating Temperature

In this and the next sections, the processing parameters of blade coating are investigated, including the coating temperature and speed. These two parameters have significant influence on the formation of channel crystals, and can potentially afford transistors of differing electrical characteristics. Fig. 3-7(a), (b) and (c) respectively depict the micrographs of the channel area (top view) blade coated at temperature 30°C, 60°C and 90°C; the coating speed is 0.2mm/s. It can be seen that at the optimum coating temperature of 60°C, highly oriented crystals with good thin-film uniformity are achieved. At the lower coating temperature of 30°C, larger crystal domains are observed albeit with less orientation while coating at 90°C results in smaller crystal formation. The smaller crystal formation at 90°C is largely attributed to the higher evaporation rate of our dual solvent system, which does not allow the channel area sufficient time to self-organize and for the occurrence of phase segregation/crystallization.

(a)

(b)

(c)

Fig. 3-7 Micrographs of printed transistors based on our blend with varying blade coating temperature: (a) 30°C, (b) 60°C (as in Fig. 3(a)), and (c) 90°C

Several measured transistor parameters for varying coating temperatures are summarized in Table 3-2. In general, when the temperature is low ($\leq 70^\circ\text{C}$) the processing temperature has relatively small effect, save the V_{th} variations at 30°C. The optimum is 60°C.

Table 3-2 Transistors performance at different coating temperatures

Coating temperature, T (°C)	μ Mean $\pm$ Variations (cm ² /Vs)	V_{th} Mean $\pm$ Variations (V)	I_{on}/I_{off} Mean $\pm$ Variations
30	$0.270 \pm 6.5\%$	2.52 ± 2.80	$1.6 \pm 1.0 \times 10^5$
40	$0.279 \pm 5.9\%$	1.91 ± 1.23	$1.7 \pm 1.0 \times 10^5$
50	$0.284 \pm 5.8\%$	2.32 ± 1.62	$1.7 \pm 0.8 \times 10^5$
60	$0.308 \pm 4.9\%$	1.76 ± 0.43	$2.4 \pm 1.1 \times 10^5$
70	$0.289 \pm 5.3\%$	1.34 ± 0.85	$5.1 \pm 2.3 \times 10^4$
80	$0.225 \pm 8.0\%$	1.25 ± 1.75	$2.9 \pm 1.9 \times 10^3$
90	$0.110 \pm 10.2\%$	1.28 ± 1.52	$2.1 \pm 1.6 \times 10^3$

3.3.1.4 Coating Speed

Fig. 3-8(a), (b) and (c) respectively depict the micrographs of the printed transistors blade coated at 0.2mm/s, 0.4mm/s and 0.6mm/s; coating temperature is the optimum 60°C ascertained in the preceding section. At lower coating speed of 0.2mm/s, highly aligned crystal formation parallel to the coating direction is observed. Increased coating speed $\geq 0.4\text{mm/s}$, on the other hand, affords smaller and disconnected crystal formations with no preferential orientation. Carefully tuning the blade coating speed is thus imperative for controlling the crystal formation behavior and formation direction in the channel area.

(a)

(b)

(c)

Fig. 3-8 Micrographs of printed transistors based on our blend with varying blade speeds: (a) 0.2mm/s (as in Fig. 3-6(a)), (b) 0.4mm/s, and (c) 0.6mm/s

Several measured transistor parameters for varying coating speeds are summarized in Table 3-3. It is observed that relatively low speed is desired and the optimum speed is 0.2mm/s which leads to highest μ (and mean μ), low V_{th} , highest I_{on}/I_{off} and lowest μ and V_{th} variations. Speeds lower or higher than the optimized condition yield deteriorated performance. Particularly, for coating speed ≥ 0.5 mm/s, the μ , V_{th} and I_{on}/I_{off} deteriorate markedly. Both low and high coating speeds, respectively 0.1mm/s and higher than 0.4mm/s, lead to substantially increased μ and V_{th} variations.

Table 3-3 Transistors performance at different coating speeds

Coating speed (mm/s)	μ Mean $\pm$ Variations (cm ² /Vs)	V_{th} Mean $\pm$ Variations (V)	I_{on}/I_{off} Mean $\pm$ Variations
0.1	0.255 $\pm$ 9.6%	1.43 $\pm$ 1.32	2.8 $\pm$ 2.4 $\times 10^3$
0.2	0.308 $\pm$ 4.9%	1.76 $\pm$ 0.43	2.4 $\pm$ 1.1 $\times 10^5$
0.3	0.293 $\pm$ 4.9%	1.78 $\pm$ 0.85	1.9 $\pm$ 1.3 $\times 10^5$
0.4	0.217 $\pm$ 6.7%	2.25 $\pm$ 1.63	1.8 $\pm$ 1.4 $\times 10^5$
0.5	0.103 $\pm$ 11.8%	1.98 $\pm$ 1.62	2.1 $\pm$ 1.4 $\times 10^4$
0.6	0.081 $\pm$ 8.0%	3.05 $\pm$ 2.79	1.1 $\pm$ 1.7 $\times 10^4$

3.3.1.5 Process Variations

Using the optimized parameters already ascertained for our Fully-Additive all-air-processed low-temperature process, i.e., TIPS-Pentacene/PS based blend (vis-à-vis TIPS-Pentacene), 20 vol% anisole, 60°C coating temperature and 0.2mm/s coating speed, 40 transistors are printed to determine their variations. The process variations are characterized based on 40 printed transistors with same ink batch and same printing equipment. The measurements are carried out under ambient conditions and room temperature. Although the process variations presented in this chapter are based on the same ink batch, similar results are obtained using another ink batch. Relatively larger process variations are expected if the characterization is based on different ink batches and/or ink over time. The effects on the process variations due to ink largely depend on the ink properties, such as the air stability and the uniformity across batches. As commercial inks (e.g., from DuPont and Sigma-Aldrich) are used, the process variations due to ink are not included in this thesis. The distribution of the μ and V_{th} of these transistors are plotted in Fig. 3-9(a) and (b). The mean mobility μ and V_{th} are respectively 0.308 cm²/Vs and 1.76 V with very low mobility μ and V_{th}

variations of $\pm 4.9\%$ and $\pm 0.43\text{V}$ respectively. These variations are substantially smaller than reported Fully-Additive printing processes [3, 6, 70, 102].

Fig. 3-9 Distribution of the μ and V_{th} of transistors printed at optimized process parameters

3.3.2 Mismatch vs Layout

In conventional silicon layouts, it is well established that the matching between transistors is influenced by the layout. In this section, we will investigate the same for transistors. As delineated in Chapter 2, the matching between transistors is imperative in many analog circuits, e.g., the differential amplifier.

Fig. 3-10(a), (b), (c) and (d) respectively depict the layout of a pair of transistors based on the simple layout, interdigitation, common centroid and the 2D common centroid layout. The mismatch characterization is based on 40 device pairs. For the sake of clarity, Fig. 3-11 depicts only one pair of typical transfer characteristics out of

the 40 transistor pairs for each layout technique. Fig. 3-11 depicts the measured transfer characteristics of the two transistors based on the different layout techniques. . It can be seen here, and as expected, the I-V characteristics of the two transistors are better matched as the layout progresses from simple → interdigitation → centroid → 2D centroid layouts. . Specifically, the respective matching is 7.2%, 5.3%, 2.8% and 2.1%. Of particular interest, the matching herein for all these layouts is substantially better than that of based on typical Fully-Additive processes, whose respective matching is 48.4%, 21.6%, 17.1% and 8.71%. Put simply, for the same layouts, the matching between two transistors based on our optimized process is 6.7x, 4.1x, 6.1x and 4.2x better respectively.

Fig. 3-10 Micrographs of the printed transistors: (a) Simple layout, (b) Interdigitation, (c) Common centroid, and (d) 2D common centroid layout

The drawback of the more complex layout is the larger area penalty, as in the case of conventional silicon. Particularly, the area overhead for the interdigitation, common centroid and 2D common centroid over the simple layout is respectively 53%, 36% and 65% larger area. In view of this overhead, a Printed Electronics circuits/systems designer would need to weigh the need for better matching against printed area. In general, good matching is needed when differential signals are involved.

Fig. 3-11 I-V characteristics of the printed transistors: (a) Simple layout, (b) Interdigitation layout, (c) Common centroid layout, and (d) 2D common centroid layout

3.4 CONCLUSIONS

To facilitate the manufacturability of Printed Electronics, we have presented our novel Fully-Additive Low-Cost all-air-processed low-temperature screen printing process for realizing transistors with very low variations, including very low mobility μ and V_{th} variations; to date the lowest variations of reported Fully-Additive processes. Said very low variations were achieved by means of blade coating of our polymer-small molecule blend (TIPS-Pentacene/PS) in our dual solvent system (toluene and anisole). The optimized parameters have been delineated. We have also presented an investigation on the matching of two transistors by means of layout – as a means to reduce the variations – and have shown that matching can be markedly improved by means of appropriate layout but with some printed area compromises.

Chapter 4 Effects of Bending and a Self-Compensation Means

4.1 INTRODUCTION

A large portion of this chapter is extracted from our publication [110] recently published in the IEEE Transactions on Circuits and Systems-I.

In this chapter, we address the challenges in Printed Electronics from the functionality perspective – this constitutes to the second and third chains of the Printed Electronics supply chain in Fig. 1-2, more particularly to a co-optimization between printing and circuit layout. As delineated in Chapters 1 and 2, a major attribute of Printed Electronics is the mechanical flexibility of its substrate, thereby allowing the bending of its substrate. However, a major challenge in the functionality of Printed Electronics is the undesired effects of bending, particularly the variations of parameters of the printed elements. In some sense, other than the variations of printing discussed in Chapter 3, the already large variations are exacerbated when the substrate is bent.

In this chapter, we propose a localized self-compensation means that innately and very effectively self-compensates for the variations of the Printed Electronics circuits/systems due to bending. The advantages of the proposed means over reported means include: (i) Localized self-compensation; (ii) No/little hardware overhead; (iii) No power dissipation overhead; (iv) Little, if any, area overhead; (v) Non-mechanical means – the thickness of the original substrate remains unchanged; and (vi) No a priori

information for the placement of devices is needed; the drawback is increased printing steps which are easily accommodated in our aforesaid Fully-Additive all-air-processed low-temperature Printed Electronics process. To the best of our knowledge, this is not only the first electronic/layout means but also the first self-compensated means for mitigating the variations of the Printed Electronics elements and circuits due to bending. This proposed means is highly efficacious – the variations due to bending are reduced by between $\sim 2\times$ and $>100\times$, depending on the circuit-element and circuit.

This chapter is organized as follows. Section 4.2 describes the bending of printed elements and our proposed localized self-compensation means. Section 4.3 presents the bending of printed circuits. Finally, conclusions are drawn in Section 4.4.

4.2 BENDING AND PROPOSED LOCALIZED SELF-COMPENSATION MEANS

In this section, we will investigate the effect of bending on passive and active printed elements, and delineate our proposed compensation means. Fig. 4-1(a) and (b) are respectively the perspective view of transistors on a flat (unbent) and bent substrate; for sake of illustration, the thickness of the printed transistors is exaggerated. To define the bending, Fig. 4-1(c) depicts the cross-sectional view of Fig. 4-1(b) where the bending is qualified in terms of radius, r (or equivalent angle, θ). These transistors are printed in the conventional fashion, i.e., the printing is only on one side (top side) of the substrate. In this instance of bending, transistor A and B are placed where the substrate is convex and concave respectively. The bending of the substrate results in the change of the physical dimensions and stresses to the printed circuit-elements. As the substrate is significantly thicker and stiffer than the transistors, the

center of the bent substrate can be assumed to be the neutral plane where there is no physical deformation; see Fig. 4-1 (c).

Fig. 4-1 Perspective view of printed transistors (not to scale) on the flexible substrate:
(a) Unbent conventional design, and (b) Bent conventional design. Cross-sectional
view: (c) Bent conventional design

As a preamble to our proposed Self-Compensation means, we remark the following. First, the changes in the characteristics of a printed circuit-element when bent concavely and convexly are the converse. In the case of our transistors, their drain current increases when it is bent concavely, and conversely decreases when bent convexly. Second, the degree of change of the current is largely determined by the radius r . Consequently, if r of two equal-sized transistors is the same, but one is bent concavely and the other convexly, their current change is approximately the same but with opposite signs; and the average of their currents is approximately equal to that when both transistors are unbent. For example, in Fig. 4-1(c), if convex-bent transistor A and concave-bent transistor B are of equal r , their average current is approximately equal to that of when unbent in Fig. 4-1(a).

On the basis of these two observations, our proposed method is as follows. We propose to partition a given printed device into two identical half-parts – first-half on the top and second-half on the bottom side of the substrate, and electrically connected through vias. The perspective and cross-sectional view of transistors embodying the proposed method are depicted in Fig. 4-2(a) and (b). In this fashion, when the substrate is bent, first-half transistor on the top side (top-half) and second-half transistor on the bottom side (bottom-half) will experience largely equal but opposite stresses. For example, when the substrate is bent convexly, the top-half transistor A1 will be stretched and the bottom-half transistor A2 will be compressed. Consequently, because of the opposing effects, the total current of the bent collective transistor A1-cum-A2 will be approximately the same as unbent transistor A (Fig. 4-1(a)).

The efficacy of the proposed means for circuit-elements, transistors, capacitors and resistors, will now be delineated in turn.

Fig. 4-2 Bent proposed Localized Self-Compensated design: (a) Perspective view of printed transistors (not to scale), and (b) Cross-sectional view

4.2.1 Transistor Bending

For bending characterizations, Fig. 4-3 depicts the measurement setup under ambient conditions for bending radius of 2cm. Some of the equipment used are ‘home-made’ implements – cut plastic tubes of various radii and ‘home-made’ probes. The printed circuit-elements and/or printed circuits under test are placed on the

curvature surface (concavely or convexly) of plastic tubes with various bending radii (see Fig. 4-3(b)). The circuit-element/circuit are connected to the measurement equipment by our 'home-made' probes, e.g., see some manually made probes in Fig. 4-3(a) and (c). For repeatability, the measurements are performed two times under the same ambient conditions for the same sample for each circuit-element and digital/analog circuit. As the two measurements are almost identical, for sake of brevity, we include only one of measurement for each element/circuit.

Fig. 4-3 Bending setup for the measurement ($r=2\text{cm}$), (b) Curvature surfaces with various bending radii, and (c) Manually made probe

Fig. 4-4, Fig. 4-5 and Fig. 4-6 depict the characteristics of conventional (single-sided) transistors and transistors based on our proposed (double-sided, each side with one half of the device) method. For $r=1\text{cm}$, Fig. 4-4(a) and 4(b) respectively depicts the output characteristics of a conventional transistor bent concavely and convexly, where the bold and dashed plots respectively correspond to unbent and bent transistors. Fig. 4-4(c) depicts the output characteristics of our proposed transistor where the characteristics for concave and convex, henceforth denoted concave/convex, are largely the same. Fig. 4-5(a) and (b) respectively depicts the input-output characteristics of the conventional and our proposed transistors. Fig. 4-6 compares the current variations of the conventional and our proposed transistors (with respect to an unbent transistor) versus r .

(a)

Fig. 4-4 Output characteristics of bent transistor with $r = 1\text{cm}$: (a, b) Conventional transistor, and (c) Proposed transistor

(a)

(b)

Fig. 4-5 Input-output characteristics of bent transistor with $r = 1\text{cm}$: (a) Conventional transistor, and (b) Proposed transistor

Fig. 4-6 Normalized I_{DS} variations for $r = 1$ cm to 8cm

On the basis of Fig. 4-4, Fig. 4-5 and Fig. 4-6, we remark the following:

- (i) From Fig. 4-4(a) and (b), it can be seen that when the conventional transistor is bent concavely and convexly, its drain current increases and reduces respectively. The current variations due to bending are indeed severe. As a case in point, with $r=1$ cm and at the bias condition of $V_{GS}=60$ V, the current varies respectively by 37% and -26% when the transistor is bent concavely and convexly.

In the perspective of our intended neuroprosthesis application in Fig. 1-3, the overall variation is a very large 63% ($37\% + 26\%$) when bent concavely to convexly or vice-versa. This large variation problem is in fact, exacerbated because the magnitude of the variation changes not only for different bending radii (Fig. 4-6)) but also for different bias conditions (Fig. 4-4(a) and (b)).

- (ii) Comparing the variations of the conventional transistor bent concavely (Fig. 4-4(a)) and convexly (Fig. 4-4(b)) against the proposed transistor (Fig. 4-4(c)), it is apparent that the proposed means is highly efficacious as a means to innately self-compensate for bending. Specifically, for $r=1\text{cm}$ and $V_{GS}=60\text{V}$, the variation from concave-to-convex (or vice-versa) bending reduces from 63% in the conventional transistor to 5% in the proposed transistor – over an order of magnitude (12x) reduction.

Arguably, more significantly, the now reduced 5% variation from bending is approximately equal to the variations of a low-variation Printed Electronics process, e.g., our process [1]. In the context of circuit design, the 5% variation is easily accommodated.

- (iii) Further to (i) and (ii), the efficacy of our proposed means can be ascertained by comparing the input-output characteristics of the conventional and our proposed transistors, depicted in Fig. 4-5(a) and (b) respectively. Specifically, our proposed transistor significantly reduces the variations due to bending by over one order of magnitude (12x) for $V_{GS} = 60\text{V}$ and $r = 1\text{cm}$.
- (iv) The characteristics in Fig. 4-4 and Fig. 4-5 are for bending with $r=1\text{cm}$. For completeness, Fig. 4-6 depicts the variations of the current of conventional and proposed transistors for $V_{GS}=60\text{V}$ bent at different bending radii, ranging from $r=1\text{cm}$ to 8cm . The following are noted. First, as expected, the variations of the proposed transistor are substantially reduced compared to the conventional transistor – specifically, the reduction is very substantial, from about one order to two orders of magnitude (12x, 26x,

34x, 99x, 19x, 14x, 10x and 8x for bending radius of 1, 2..., 8cm respectively). Second, as expected, the variations increase for smaller r , when bent either concavely or convexly. Third, as delineated earlier, in general, the variations of a conventional transistor bent concavely and convexly are largely the same but of opposite directions. The worst case variations occur for the smallest bending radius, $r=1\text{cm}$ – 63% for the conventional vs 5% for our proposed transistor.

4.2.2 Capacitors Bending

The top of Fig. 4-7 depicts the micrograph of a printed capacitor using our Fully-Additive process. The capacitor embodying our proposed means, as in the case of our proposed transistor, involves a top-half capacitor and a bottom-half capacitor, and are electrically connected by means of vias. Each half has an area of 64mm^2 with a nominal (unbent) capacitance of 142.8pF .

The bottom of Fig. 4-7 depicts the % capacitance variation for various r . We remark the following. First, converse of the transistors, the variations increase negatively and positively respectively for concave and convex bending; for transistors the variations phenomenon is the converse (for convex and concave). This is probably because when the capacitors bent concavely, the area of printed capacitor decreases, and vice versa. Second, as expected, the capacitance variations increase as bending radius reduces. Third, compared to the conventional means, the proposed printed capacitors feature lower variations. Specifically, for $r=1\text{cm}$, the 2.9% variation (1.7% convex + 1.2% concave) of the conventional capacitor is significantly reduced by over an order of magnitude ($\sim 11\times$) to 0.27%. Fourth, for bending radius of

1cm to 8cm, the proposed means provides variations reduction of 11x, 5x, 6x, 8x, 6x, 3x, 4x and 3x respectively.

Fig. 4-7 Micrograph and characteristics for bent capacitor

4.2.3 Resistors Bending

The top of Fig. 4-8 depicts the micrograph of a printed resistor whose dimension and resistance are 8mm×1mm and 26.4kΩ respectively. The resistor embodying our proposed self-compensation means, as in the case of our proposed transistor and capacitor, involves two equal-half resistor on each side of the substrate and electrically connected by means of vias. The % resistance variation of the printed resistor for various r is depicted at the bottom of Fig. 4-8.

Fig. 4-8 Micrograph and characteristics for bent resistor

We remark the following. First, as in the case of capacitors (converse of the transistors), the variations increase negatively and positively respectively for concave and convex bending. Second, as expected, the resistance variations increase as r reduces. Third, compared to the conventional resistors, the proposed printed resistors feature substantially lower variations. Specifically, for $r=1\text{cm}$, the overall 14.1% variation (8.9% convex + 5.2% concave) of the conventional resistor is significantly reduced by nearly an order of magnitude ($\sim 8\times$) to a small 1.8%. Fourth, for bending radius of 1cm to 8cm, the proposed means provides variations reduction of 8x, 15x, 6x, 6x, 4x, 5x, 4x and 3x respectively. Fifth, the variations of the printed resistors are

substantially more severe than the printed capacitors (e.g., for $r=1\text{cm}$, 14% vs 3%). This is probably because of the intrinsic property differences for the different materials used for the resistors and capacitors, such as elasticity and Young's modulus. Sixth, in the context of the transfer function of Printed Electronics circuits, a capacitor-based circuit (e.g., a ratio of capacitors) [227] is preferred over a resistor-based circuit.

In summary, we have delineated the effects of bending on passive and active elements and shown that our proposed self-compensation means is highly efficacious (up to $\sim 100\times$ reduced variations). We will now extend our investigations to several fundamental digital and analog circuits, including inverters, ring oscillators and an op-amp.

4.3 BENDING OF PRINTED CIRCUITS

4.3.1 Inverters

The two common printed inverters [6] are the diode-connected load inverter and zero- V_{GS} connected load inverter, respectively depicted in Fig. 4-9(a) and Fig. 4-12. The former and latter respectively features relatively higher operation speed and higher noise margin [3].

Fig. 4-9(a) and (b) respectively depicts the schematic of the conventional and our proposed diode-connected inverters. In the latter, each transistor comprises two-halves, each placed on opposite sides of the substrate. For example, in Fig. 4-9(b), the first-half transistors (unshaded $1/2 M_{1-top}$ and $1/2 M_{2-top}$) and the other-half transistors (shaded $1/2 M_{1-bottom}$ and $1/2 M_{2-bottom}$) are respectively placed on the top and bottom side of the substrate. One such printed half-inverter is depicted in Fig. 4-9(c). Note that the effective substrate area of the proposed inverter is smaller than the conventional inverter due to its printing on both sides of the substrate. For $r=1\text{cm}$ and 2cm , Fig. 4-10(a) and Fig. 4-11(a) respectively depicts the voltage transfer

characteristics and voltage gain of the conventional inverter, where the bold and dashed plots are respectively the unbent and bent inverters. For comparison, also for $r=1\text{cm}$ and 2cm , Fig. 4-10(b) and Fig. 4-11(b) respectively depicts the same for our proposed inverter.

Fig. 4-9 Schematics of the diode-connected inverter: (a) Conventional design, and (b) Proposed design. (c) Micrograph of the half inverter

(a)

(b)

Fig. 4-10 Output characteristics: (a) Conventional diode-connected inverter, and (b) Proposed diode-connected inverter

(a)

(b)

Fig. 4-11 Gain: (a) Conventional diode-connected inverter, and (b) Proposed diode-connected inverter

On the basis of Fig. 4-10 and Fig. 4-11 and with variations qualified in terms of V_{th} and gain, we remark the following. First, from Fig. 4-10(a), V_{th} of the conventional inverter increases positively and negatively for concave and convex bending respectively. For $r=1\text{cm}$ and 2cm , the V_{th} of the conventional inverter varies respectively by 0.99V (0.38V concave + 0.61V convex) and 0.52V (0.31V + 0.21V) when the inverter is bent concavely to convexly or vice-versa. For the same conditions, from Fig. 4-10(b), the V_{th} variations of our proposed inverter reduce to 0.09V and 0.04V respectively – a very significant reduction by over one order of magnitude, i.e., 11x and 13x respectively. Second, from Fig. 4-11(a), the maximum gain of the conventional inverter increases negatively and positively for concave and convex bending respectively. For $r=1\text{cm}$ and 2cm , its maximum gain varies respectively by 6.7% (2.4% + 4.3%) and 3.3% (1.9% + 1.4%). For the same conditions, the gain variations of the proposed inverter reduce to 1.4% and 0.9% respectively – a substantial variation reduction by 4.8x and 3.7x respectively. The possible reason for the V_{th} and gain variations is the different effects of bending (e.g., disproportional on-resistance variations) to the drive and load transistors in the inverter.

The schematic of the conventional and our proposed zero- V_{GS} connected inverter is respectively depicted in Fig. 4-12(a) and (b). One printed half-inverter is depicted in Fig. 4-12(c). Fig. 4-13(a) and Fig. 4-14(a) respectively depicts the transfer characteristics and the gain of the conventional inverter for $r=1\text{cm}$ and 2cm . Fig. 4-13(b) and Fig. 4-14(b) respectively depicts the same for our proposed inverter.

Fig. 4-12 Schematics of the zero- V_{GS} connected inverter: (a) Conventional design, and (b) Proposed design. (c) Micrograph of the half inverter

(a)

(b)

Fig. 4-13 Output characteristics: (a) Conventional zero- V_{GS} connected inverter, and (b) Proposed zero- V_{GS} connected inverter

Fig. 4-14 Gain: (a) Conventional zero- V_{GS} connected inverter, and (b) Proposed zero- V_{GS} connected inverter

On the basis of Fig. 4-13 and Fig. 4-14, we remark the following. First, from Fig. 4-13(a), the V_{th} of the conventional zero- V_{GS} connected inverter increases negatively and positively for concave and convex bending respectively. For $r=1\text{cm}$ and 2cm , the conventional inverter V_{th} varies respectively by 2.17V ($1.19\text{V} + 0.98\text{V}$) and 1.15V ($0.59\text{V} + 0.56\text{V}$) when the inverter is bent concavely to convexly or vice-versa. For the same conditions, from Fig. 4-13(b), the V_{th} variations of our proposed inverter reduce to 0.57V and 0.27V respectively – a significant reduction of 3.8x and 4.3x respectively. Second, from Fig. 4-14(a), the maximum gain of the conventional inverter increases negatively and positively for concave and convex bending respectively, congruous to the diode-connected inverter. For $r=1\text{cm}$ and 2cm , the maximum gain of the conventional inverter varies respectively by 28.6% ($14.3\% + 14.3\%$) and 21.9% ($10.1\% + 11.8\%$). For the same conditions, the gain variations of the proposed inverter reduce to 10.1% and 6.7% respectively – a substantial variation reduction by 2.8x and 3.3x respectively.

We note two differences between the bending of the diode-connected and that of zero- V_{GS} connected inverters. First, their direction of V_{th} variations is opposite, i.e., for the diode-connected inverter, V_{th} increases positively and negatively for concave and convex bending respectively, while that for the zero- V_{GS} connected inverter, the variation of V_{th} is the converse. The difference may be attributed to the different connections of the load transistors. Second, the gain variations of zero- V_{GS} connected inverter have the same direction but are substantially more severe than the diode-connected inverter (e.g., for $r=1\text{cm}$ and 2cm , respectively 28.6% and 21.9% vs 6.7% and 3.3%). This may be attributed to the relatively more severe effects from bending for the on-resistance of the zero- V_{GS} connected load transistor which operates closer to subthreshold region. For Printed Electronics circuit design in the perspective of the

variations due to bending, circuits embodying the diode-connected inverter is preferred over the zero- V_{GS} connected inverter. Interestingly, concave bending results in higher speed (see Section 4.3.2) for both inverters, and is hence preferred over convex bending.

4.3.2 Ring Oscillators

Consider now ring oscillators embodying diode-connected load and zero-VGS connected load topologies, respectively depicted in Fig. 4-15 and Fig. 4-20. The former and the latter respectively features relatively higher oscillating frequency and higher reliability with respect to process variations [1, 3]. Fig. 4-15(a) and (b) respectively depicts the conventional and our proposed diode-connected ring oscillator. In the latter, each transistor comprises two-halves, each placed on opposite sides of the substrate. One printed half-ring oscillator is depicted in Fig. 4-16(a), and Fig. 4-16(b) depicts a photo of the ring oscillator printed on both sides of the flexible substrate.

Fig. 4-15 Schematics of the diode-connected ring oscillator with level shifter: (a) Conventional design, and (b) Proposed design

Fig. 4-16 (a) Micrograph of diode-connected ring oscillator. (b) Photo of ring oscillators on both sides of the substrate

Fig. 4-17(a) and (b) respectively depicts the measured output voltage for the conventional diode-connected ring oscillator for $r=1\text{cm}$ and 2cm . Fig. 4-18 depicts the same for our proposed ring oscillator. Fig. 4-19 compares the output frequency variations of conventional and proposed ring oscillators (with respect to an unbent ring oscillator) versus r . On the basis of these figures, we remark the following. First, from Fig. 4-17(a) and (b), the output frequency of the conventional ring oscillator increases and decreases respectively for concave and convex bending – this is congruous to the drain current variations of the transistors in Fig. 4-6. For $r=1\text{cm}$ and 2cm , the output frequency varies respectively by 46.2% (29.4% + 16.8%) and 30.3% (19.4% + 10.9%) when the ring oscillator is bent concavely to convexly or vice-versa. For the same conditions, Fig. 4-18 depicts that the output frequency variations of our proposed ring oscillator reduce respectively to 5.8% and 4.0% – a very significant reduction by 8.0x and 7.6x respectively. Second, as expected, from Fig. 4-19, the variations increase when r reduces. Third, with $r=1\text{cm}$ to 8cm , the variations reduction of our proposed ring oscillator is very substantial – about one order of magnitude (8x, 8x, 9x, 8x, 9x, 20x, 23x and 11x respectively) smaller.

Fig. 4-17 Output voltage of the diode-connected ring oscillators for conventional design: (a) $r=1\text{cm}$, and (b) $r=2\text{cm}$

Fig. 4-18 Output voltage of the diode-connected ring oscillators for proposed design

Fig. 4-19 Output frequency of the diode-connected ring oscillator for $r = 1\text{ cm}$ to 8 cm

Fig. 4-20(a) and (b) respectively depicts the schematic of the conventional and our proposed zero- V_{GS} connected ring oscillator. The micrograph of one half-ring oscillator is depicted in Fig. 4-20(c). Fig. 4-21(a) and (b) depict the output voltage for the conventional zero- V_{GS} connected ring oscillator for $r=1\text{cm}$ and 2cm respectively. Fig. 4-22 depicts the same for the proposed ring oscillator. Fig. 4-23 compares the output frequency variations of conventional and proposed ring oscillators (with respect to an unbent ring oscillator) versus r .

Fig. 4-20 Schematics of the zero- V_{GS} connected ring oscillators: (a) Conventional design, and (b) Proposed design. (c) Micrograph of half ring oscillator

Fig. 4-21 Output voltage of the zero- V_{GS} connected ring oscillators for conventional design

Fig. 4-22 Output voltage of the zero- V_{GS} connected ring oscillators for proposed design.

Fig. 4-23 Output frequency of the zero- V_{GS} connected ring oscillator for $r = 1\text{cm}$ to 8cm

On the basis of Fig. 4-21, Fig. 4-22 and Fig. 4-23, we remark the following. First, from Fig. 4-21(a) and (b), like the conventional diode-connected ring oscillator, the output frequency of the conventional zero- V_{GS} ring oscillator increases and decreases respectively for concave and convex bending – this is congruous to the drain current variations of the transistors. Specifically, with $r = 1\text{cm}$ and 2cm , the output frequency varies respectively by 124.9% ($76.3\% + 48.6\%$) and 86.5% ($43.6\% + 42.9\%$) when the ring oscillator is bent concavely to convexly or vice-versa. For the same conditions, from Fig. 4-22, the output frequency variations of our proposed ring oscillator reduce to 10.6% and 0.8% respectively – a very significant reduction by over an order of magnitude (12x and 108x respectively). Second, as expected, from Fig. 4-23, the variations increase when r reduces. Third, with $r=1\text{cm}$ to 8cm , the variations reduction of the proposed ring oscillator is very substantial – from about one

order to two orders of magnitude (12x, 108x, 80x, 13x, 12x, 8x, 7x and 14x respectively) smaller.

Of the two ring oscillators, the variations of the conventional zero- V_{GS} connected ring oscillator are substantially more severe. This may be attributed to the relatively larger drain current variations and ensuing larger on-resistance variations of the zero- V_{GS} connected load transistor which operates near subthreshold region; see Fig. 4-4. In the perspective of variations due to bending, similar to the inverters, the diode-connected topology is preferred over the zero- V_{GS} connected topology for ring oscillators. From a circuits perspective, placing both the diode-connected and zero- V_{GS} connected ring oscillators such that they are bent concavely is preferred over convexly, as this leads to increased speed.

4.3.3 Op-amp

Fig. 4-24(a) and (b) respectively depicts the conventional and our proposed op-amp. The micrograph of one half-op amp is depicted in Fig. 4-24(c). Fig. 4-25(a) and (b) respectively depicts the frequency response of the conventional and the proposed op-amp, where the bold and dashed plots respectively correspond to unbent and bent amplifiers.

Fig. 4-24 Schematics of the op-amp: (a) Conventional design, and (b) Proposed design. (c) Micrograph of half op-amp

(a)

(b)

Fig. 4-25 Frequency response: (a) Conventional op-amp, and (b) Proposed op-amp

We remark the following. First, from Fig. 4-25(a), the gain of the conventional op-amp at low frequency decreases and increases respectively for concave and convex bending. For $r=1\text{cm}$ and 2cm , the gain at low frequency varies by 0.56dB ($0.49\text{dB} + 0.07\text{dB}$) and 0.43dB ($0.38\text{dB} + 0.05\text{dB}$) respectively. For the same conditions, from Fig. 4-25(b), the gain variations of the proposed op-amp reduce to 0.32dB and 0.12dB respectively – somewhat significant reduction by $1.7\times$ and $3.6\times$ respectively. From a circuits perspective, note that because Printed Electronics op-amps are expected to operate in open-loop (vis-à-vis closed-loop), the variations of gain (and unity-gain bandwidth variations) need to be low. Second, from Fig. 4-25(a), the unity-gain bandwidth conversely, perhaps somewhat unexpectedly, increases positively and negatively for concave and convex bending respectively; a placement such that the bending is concave is thus preferred over convex. For $r=1\text{cm}$ and 2cm , the unity-gain bandwidth varies by 63.6% ($33.6\% + 30.0\%$) and 37.0% ($21.9\% + 15.1\%$) respectively. For the same conditions, from Fig. 4-25(b), the unity-gain bandwidth variations of the proposed op-amp reduce to 10.7% and 6.5% respectively – a significant reduction by $\sim 6\times$.

The high efficacy of our proposed means can likewise be appreciated from the time waveforms of the conventional and proposed op-amps. Fig. 4-26 depicts the input (1V) and output ($\sim 1.3\text{V}$) waveforms of unbent and bent op-amps. Congruous to the variations of the frequency response depicted in Fig. 4-25(a), the output of the conventional op-amp increases and decreases respectively for concave and convex bending. For $r=1\text{cm}$ and 2cm , the output varies by 0.26V ($0.10\text{V} + 0.16\text{V}$) and 0.18V ($0.08\text{V} + 0.10\text{V}$) respectively. For the same conditions, from Fig. 4-26(b), the output variations of the proposed op-amp reduce to 0.030V and 0.011V respectively – a

substantial variations reduction by about one order of magnitude (8.7x and 16.4x respectively).

(a)

Fig. 4-26 Time-domain input-output waveforms: (a) Conventional op-amp, and
(b) Proposed op-amp

In summary, we have shown that our proposed self-compensation means provides very significant variations reduction (up to over two orders of magnitude) due to bending for both printed digital and analog circuits. A summary of the variations of conventional and proposed circuit-elements/circuits, and the ensuing variations reduction is tabulated in

Table 4-1; there is no benchmarking against competing methods as our proposal, to date, is the only electronic/layout means to mitigate the variations due to bending.

Table 4-1 Summary of measurements of unbent and bent circuit-elements/circuits and reduction of variations arising from the proposed self-compensation means

Circuit-Elements and Circuits	Parameters	Variations (Conventional)		Variations (Proposed)		Variations Reduction	
		$r = 1\text{cm}$	$r = 2\text{cm}$	$r = 1\text{cm}$	$r = 2\text{cm}$	$r = 1\text{cm}$	$r = 2\text{cm}$
Transistor	I_{DS}	63%	30%	5.0%	1.2%	12x	26x
Capacitor	C	2.9%	1.5%	0.27%	0.30%	11x	5x
Resistor	R	14%	8.0%	1.8%	0.54%	8x	15x
Diode-Connected Inverter	V_{th}	0.99V	0.52V	0.09V	0.04V	11x	13x
	Gain	6.7%	3.3%	1.4%	0.90%	5x	4x
	V_{th}	2.17V	1.15V	0.57V	0.27V	4x	4x
Zero- V_{GS} Connected Inverter	Gain	28.6%	21.9%	10.1%	6.7%	3x	3x
Diode-Connected Ring Oscillator	Output Frequency	46.2%	30.3%	5.8%	4.0%	8x	8x
Zero- V_{GS} Connected Ring Oscillator	Output Frequency	124.9%	86.5%	10.6%	0.8%	12x	108x
Op-amp	Gain at Low Frequency	0.56dB	0.43dB	0.32dB	0.12dB	2x	4x
	Unity-Gain Bandwidth	63.6%	37.0%	10.7%	6.5%	6x	6x

4.4 CONCLUSIONS

For the functionality of Printed Electronics when its substrate is bent, we have presented a comprehensive investigation into the effects of concave/convex bending on individual printed passive and active elements and on basic-circuits. We have shown that in terms of variations, capacitor-based circuits and diode-connected circuits are preferred; and for inverters and ring oscillators, concave bending is preferred. We have proposed a novel localized self-compensation means to mitigate the variations of printed circuit-elements and circuits due to bending. The proposed means has been shown to be highly efficacious – the reduction of variations ranges from $\sim 2x$ to $>100x$ – without power dissipation, substrate-area or hardware overheads but with additional printing steps.

Chapter 5 An Open Platform for Fully-Additive Printed Electronics

5.1 INTRODUCTION

A large portion of this chapter is extracted from our publication [114] accepted as an invited paper for publication in the IEEE Journal of Emerging and Selected Topics.

In this chapter, we address the challenges in Printed Electronics from the designability perspective. As delineated in Chapters 1 and 2, a major issue in designability is the lack of reported Process Development Kits (PDKs) which, to some degree, leads to the exiguity of Printed Electronics-only circuits and systems. This lack of the PDK pertains to the third chain of the entire Printed Electronics supply chain in Fig. 1-2.

We present an Open-Platform PDK for Printed Electronics based on our Fully-Additive Low-Temperature All-Air printing process with Very-Low process variations [1]; see Chapter 3 earlier. Our Open-Platform embodies a novel transistor model that can not only accurately model the Printed Electronics transistors when they are flat (unbent flexible substrate) but can also model the variations of Printed Electronics transistors when they are bent (bent flexible substrate). To the best of our knowledge, this is the first-ever transistor model that can model the Printed Electronics transistors when they are bent; the model also takes into account the layout of the transistors [2, 3]. The possibility to model the performance of Printed Electronics when the substrate is bent is useful as Printed Electronics circuits and systems can then be

applied to uneven surfaces, including e-skin, curved walls and enclosures, etc. – thereby expanding the scope of applications.

The proposed model is simple and it is compatible with industry-standard Computer-Aided-Design and Electronic-Design-Automation tools. This Open-Platform and the proposed transistor model are verified by comparing the simulations and measurements on individual printed circuit elements and on several fundamental printed digital and analog circuits including inverters, ring oscillators and amplifiers.

This chapter is organized as follows. Section 5.2 describes the PDK, including the proposed transistor model and layout design rules. Section 5.3 presents the verification of the proposed model, including the statistical simulations based on the proposed model. Finally, conclusions are drawn in Section 5.4.

5.2 PDK: A NOVEL TRANSISTOR MODEL AND DESIGN RULES

In this section, we will present our PDK based on our recent Fully-Additive Low Temperature All-Air printing process with low process variations. This PDK includes a novel transistor model that can model not only when the transistor is flat but also when it is bent – see Fig. 5-1 later. This transistor model is based on the amorphous silicon model, but with three augmentations: 1) the cutoff coefficient, 2) the effect of channel length on carrier mobility, and 3) effect of bending. The former two augmentations have been reported in our previous publication [3] and the third augmentation will now be presented. The design rules for the transistor layout are also presented. This PDK can be extended to other printing process if the process parameters and design rules are available.

5.2.1 A Novel Transistor Model

We had previously proposed a transistor model (eqn. (5-1)) [3] that can accurately model the transistor characteristics in the entire operation regions (from cut-off to above-threshold regions) when the printed transistor is flat. The drain-source current of the p -type printed transistor is:

$$I_{DS} = \frac{C_{cutoff} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^{1+Y} V_{DS} (1 + \lambda V_{DS})}{\left[(V_{AA})^Y + \mu C_{ox} \frac{W}{L} R (V_{GS} - V_{th})^{1+Y} \right] [1 + (V_{DS}/V_{sat})^M]^{1/M}} \quad (5-1)$$

where W is the channel width,

L is the channel length,

C_{ox} is the gate dielectric capacitance,

R is the drain and source resistance,

V_{AA} is characteristic voltage for field effect mobility,

Y is the power law mobility parameter,

λ is the output conductance parameter,

$V_{sat} = \alpha_{sat} (V_{GS} - V_{th})$ is the saturation voltage,

α_{sat} is the saturation modulation parameter,

M is the knee shape parameter,

μ is expressed in eqn. (5-2), and

C_{cutoff} is the cutoff coefficient and expressed in eqn. (5-3).

$$\mu = \frac{\theta + 5^{\frac{L_{norm}}{L}}}{\theta + 5^{\frac{L}{L_{norm}}}} \mu_{norm} \quad (5-2)$$

$$C_{cutoff} = \frac{1 + \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{th}} \right)^\omega}{1 + [1 + V_m - \phi(V_{GS} + V_m + V_{th})] \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{th}} \right)^\omega} \quad (5-3)$$

where V_{DS} is the voltage across the drain and source,

V_{GS} is the voltage across the gate and source,

V_m is the modulation voltage,

ϕ is the voltage modulation parameter,

ω is the power law modulation parameter,

L_{norm} is the nominal channel length which is 100 μm , and

μ_{norm} is the carrier mobility at nominal channel length.

Fig. 5-1 Printed transistors bent on a flexible substrate

One of the unique advantages of Printed Electronics realized on flexible substrates (e.g., PET) is that the substrate may be bent, hence the possibility of adhering the Printed Electronics on uneven surfaces and fitted into odd spaces. Fig. 5-1 depicts two bent transistors, Transistor A convexly and Transistor B concavely.

It is well-established that the transistor characteristics vary significantly when the transistor (the substrate) is bent and when the bending directional is along the channel (as depicted in Fig. 5-1). This is partially because the effective channel length is increased when the transistor is bent convexly and vice versa. On the other hand, when the bending direction is perpendicular to the channel, the characteristics of the transistors remain largely unchanged – this is because the channel length largely remains unchanged in this case. At this juncture, all reported transistor models [3, 201, 212-214] can only model the transistors when they are flat but not when they are bent. This is also true for our earlier proposed transistor model given in eqn. (5-1), rendering our model similarly somewhat incomplete. To accommodate this shortcoming, we propose to augment the effect of bending into our transistor model.

In Fig. 5-1, we define the bending of the transistor according to the bending radius, r ; a corresponding parameter, θ , may also be used.

On the basis of measurements on 150 printed transistors, we amend our earlier derived eqn. (5-1) to augment the effect of bending. By empirical means, we derive the expressions for mobility with bending, μ_b , and threshold voltage with bending, V_{thb} , in eqns. (5-4) and (5-5) accordingly.

$$\mu_b = (k \frac{d}{r} + 1) \mu \quad (5-4)$$

$$V_{thb} = \left[a \left(\frac{d}{r} \right)^3 + b \left(\frac{d}{r} \right)^2 + c \left(\frac{d}{r} \right) + e \right] + V_{th} \tag{5-5}$$

where d is the thickness of the flexible substrate in μm ,

k, a, b, c, e are the bending coefficients, and

r is the bending radius in μm .

Based on this model, the new process parameters for our Fully-Additive printed transistor with low process variations are derived and summarized in Table 5-1.

Table 5-1 Process parameters of our Low-Variation Fully-Additive printed transistor with bending

Parameter		Value	Parameter		Value
μ_{flat}		0.31cm ² /Vs	ω		60
L_{norm}		100 μm	λ		0.0001V
ϕ		0.08	M		2.0021
α_{sat}		0.6775	V_{AA}		10 ⁹ V
Y		0.1	$V_{th(flat)}$		-2V
V_m		3V	C_{ox}		223pF/cm ²
a	Concave	-8.018 $\times 10^5$	b	Concave	1.6113 $\times 10^4$
	Convex	-2.7468 $\times 10^6$		Convex	3.6186 $\times 10^4$
c	Concave	-1.8483 $\times 10^2$	e	Concave	0.1376
	Convex	31.94		Convex	-9.42 $\times 10^{-2}$

The proposed model and the associated parameters will be verified by means of comparing simulations against measurements on printed transistors and circuits, both unbent and bent, in Section 5.3 later.

5.2.2 Layout Design Rules

The layout design rules in a PDK serve to define the (minimum) physical dimensions for printed devices and these dimensions are ascertained for a given printing process for manufacturability. Table 5-2 tabulates the primary design rules in our PDK (further design rules are expected for later versions of the PDK) for our Fully-Additive printing process, and their associated definitions are given in Fig. 5-2. Our developed layout design rules are coded into the Design Rule Checker (DRC) in a commercial Electronic Design Automation tool that serves to check that a given layout abides by the design rules. The single printed transistor and printed digital and analog circuits in Section IV abide by these design rules.

The DRC is designed with an intuitive user interface. After the DRC check and if there is a DRC error in the layout, a window delineating the DRC error will be popped up. By double clicking on the DRC error in the popup window, the DRC error in the layout will be highlighted. After the DRC has ascertained that there is no DRC error, the layout versus schematic check is performed to ascertain if there is any discrepancy between the schematic and the layout, and the results will be displayed in the Comparison Results window.

Using our PDK, a number of Printed Electronics circuits are designed, and simulated, see Fig. 5-4 to Fig. 5-7 later. After several design and simulation iterations, the design of these Printed Electronics circuits are finalized. These circuits are thereafter printed and measured. Some of these circuits will now be presented and these in part verify the efficacy of our PDK, including both the proposed transistor model and the layout design rules.

Table 5-2 Design rules of our Low-Variation Fully-Additive printed devices

Design Rules	Comments	Dimension (μm)
a1	Dielectric enclosure	≥200
a2	Gate enclosure	≥100
a3	Drain/Source width	≥300
a4	Drain/Source spacing (Channel Length)	$80 \leq a4 \leq 300$
a5	Dielectric width	≥700
b1	Dielectric length	≥700
b2	Drain/Source length	≥800
b3	Gate length	≥500
b4	Drain/Source spacing	≥200
b5	Channel width (single finger)	≥300
c1	Dielectric enclosure	≥200
c2	Bottom electrode enclosure	≥100
c3	Top electrode width	≥1000
c4	Bottom electrode width	≥1200
c5	Capacitor dielectric width	≥1600
r1	Resistor width	≥300
r2	Resistor length	≥1000

Fig. 5-2 Layout rules for: (a) Printed transistor, (b) Capacitor, and (c) Resistor

5.3 VERIFICATION OF OUR PDK

In this section, we will verify our PDK including our proposed model (and the associated parameters) and the layout design rules. The proposed model is coded in Verilog-A and written into a commercial Electronic Design Automation tool.

Fig. 5-3(a) and (b) respectively depicts the input and output characteristics for our Printed Electronics transistors when they are flat, and these figures delineate the differences/agreement between the modelling (simulations) and the measured characteristics. It can be seen that the simulated characteristics agree well with the measurement results, thereby depicting that the accuracy of derived process parameters (i.e., PDK) when the substrate is flat (unbent).

Fig. 5-3 Comparison of transistor characteristics obtained from measurements and from simulation: (a) I_D vs V_{GS} , and (b) I_D vs V_{DS}

To delineate the changes to the transistor characteristics, when the transistor is bent concavely or convexly, we will plot the changes to mobility μ and V_{th} with respect to bending radius, r . Also, for sake of illustration, these changes will be plotted with respect to the flat substrate. Fig. 5-4(a) and (b) respectively depicts the comparison between the modelling (simulations) and the measured carrier mobility and the threshold voltage due to bending. We note, as expected, that the mobility of the printed transistor increases when bent concavely; positive variation indicates a higher mobility. This mobility increase is largely due to the reduced channel length when the transistor is bent concavely. It can also be seen that the simulated characteristics agree well with the measurement, thereby verifying our proposed transistor bending model and the associated process parameters, i.e., PDK.

(a)

(b)

Fig. 5-4 Comparison of transistor characteristics obtained from measurements and from simulation: (a) Normalized carrier mobility, and (b) Variation of threshold voltage

To further verify and extend our proposed transistor model to circuits (particularly when the circuits are on a bent substrate) vis-à-vis a single transistor, several digital and analog fundamental circuits are designed, simulated, printed and measured. These fundamental circuits are a digital diode-connected ring-oscillator, zero- V_{GS} ring-oscillator and an analog amplifier.

As before, for sake of illustration, the changes of the key parameters of the different circuits when bent convexly and concavely will be plotted against the same when flat, and expressed as a percentage.

Fig. 5-5(a), (b) and (c) respectively depicts the schematic, the layout and microphotograph of the diode-connected ring oscillator. The oscillation frequency obtained from simulations and measurements are depicted in Fig. 5-5(d). It can be seen that the simulation results and measurement results agree well, thereby verifying the accuracy of our proposed transistor model encompassing bending applied to the diode-connected ring oscillator.

It is interesting, as expected, that the oscillation frequency increases when the printed ring-oscillator is bent concavely, and vice versa. This is largely because, as depicted in Fig. 5-4(a), the carrier mobility of the printed transistor increases when they are bent concavely and vice versa.

Fig. 5-5 Diode-connected ring-oscillator: (a) Schematic, (b) Layout, (c) Microphotograph, and (d) Comparison of oscillation frequency of the ring-oscillator obtained from simulation and from measurements when it is bent

Fig. 5-6(a), (b) and (c) respectively depicts the schematic, layout and microphotograph of the zero- V_{GS} ring oscillator. The oscillation frequency obtained from simulations and measurements are depicted in Fig. 5-6(d). As before, the measurement results and simulation results agree well, thereby further verifying the accuracy of our proposed transistor model applied to the zero- V_{GS} ring oscillator.

Similarly, due to the increased carrier mobility when bent concavely, the oscillation frequency increases, and the converses when bent convexly.

From an application perspective, the direction of bending (i.e., either concave or convex) provides the user/designer a degree of freedom to increase or reduce the oscillation frequency. Specifically, if the user has the option of deciding if the substrate is to be bent concavely or convexly, the concave bending provides a means for increasing the oscillation frequency. Note that for a given curve surface, the concave or convex bending can be obtained by placing the substrate either face-up or face-down (or vice-versa). For example, if the Printed Electronics circuit is placed face-up (i.e., the printing of the Printed Electronics circuit is on the top surface of the substrate) on a concave surface, its operation would be higher than if the Printed Electronics circuit is placed face-down (i.e., the printing of the Printed Electronics circuits on the bottom surface).

(a)

(b)

(c)

(d)

Fig. 5-6 Zero- V_{GS} ring-oscillator: (a) Schematic, (b) Layout, (c) Microphotograph, and (d) Comparison of oscillation frequency of the ring-oscillator obtained from simulation and from measurements when it is bent

Consider now a printed analog circuit and the accuracy of the proposed model to analog circuits. Fig. 5-7 (a), (b) and (c) respectively depicts the single-stage amplifier schematic, layout and microphotograph. Fig. 5-7(d) and (e) respectively depicts the frequency response of the printed amplifier obtained from simulations and measurements. For the amplifier, its performance is qualified by its gain and gain-bandwidth.

As expected, the simulations results and measurements also agree well, hence verifying the proposed transistor model applied to an amplifier. It can also be seen from Fig. 5-7(d) and Fig. 5-7(e) that the gain-bandwidth product increases (slightly) when the circuits bent concavely due to the increased carrier mobility.

(e)

Fig. 5-7 Amplifier: (a) Schematic, (b) Layout, (c) Microphotograph, and (d) Measured frequency response, and (e) Simulated frequency response

By means of our PDK and measured variations of individual circuit elements, we are also able to perform statistical analysis, (Monte-Carlo simulations) to predict circuit performance. Due to the innately high process variations of Printed Electronics, Monte-Carlo simulations are important as they provide the Printed Electronics circuit designer invaluable insight into the Printed Electronics circuit functionality, circuit performance variations, and hence manufacturability.

To depict the effect of process variations on the performance variations and manufacturability of analog and digital designs, and also to depict the efficacy of our model, the simulations are based on two processes, our previous [6] Fully-Additive printing process with process variations of $\pm 30\% \mu$ and $\pm 1V V_{th}$ and our recent Fully-

Additive printing process with low process variations of $\pm 4.9\% \mu$ and $\pm 0.43\text{V } V_{th}$ [1] respectively.

Fig. 5-8 depicts the variations of the oscillation frequency of the diode-connected ring-oscillator whose schematic was shown in Fig. 5-5(a) earlier.

Fig. 5-8 Oscillation frequency of the zero- V_{GS} ring oscillator based on two processes variations: (a) $\pm 30\% \mu$ and $\pm 1\text{V } V_{th}$, and (b) $\pm 4.9\% \mu$ and $\pm 0.43\text{V } V_{th}$

It can be seen from Fig. 5-8 that by reducing the process variations, the failure rate is significantly reduced. Specifically, 17% of diode-connected ring oscillators realized from our previous screen printing process whose variations is $\pm 30\% \mu$ and $\pm 1\text{V } V_{th}$ fail. For the diode-connected ring-oscillator design but realized from our current printing process whose variations are $\pm 4.9\% \mu$ and $\pm 0.43\text{V } V_{th}$, there is no failed ring-oscillators, i.e., all oscillators are functional. Further, amongst all the functional ring oscillators, the variations of the oscillation frequency are $\pm 13.5\%$ and

$\pm 1.9\%$ respectively for that printed from our previous high-variation and present lower variation process.

Fig. 5-9 depicts the performance variations of the amplifier (whose schematic is in Fig. 5-7(a)), based on our said previous high variation and based on recent low process variations printing processes. The variations of its offset and gain are respectively $\pm 2.8\text{V}$ (Fig. 5-9(a)) and $\pm 23.6\%$ (Fig. 5-9(c)) for our previous Fully-Additive printing process and reduced to $\pm 0.5\text{V}$ (Fig. 5-9(b)) and $\pm 2.63\%$ (Fig. 5-9(d)) for our recent Fully-Additive printing process with low process variations. Following Fig. 5-8 and Fig. 5-9, it is apparent that printing based on low variations process is desired.

Fig. 5-9 Amplifier Offset voltage (a) Based on our previous $\pm 30\% \mu$ and $\pm 1V V_{th}$ process, and (b) Based on our present $\pm 4.9\% \mu$ and $\pm 0.43V V_{th}$ process; Amplifier Gain variation (c) Based on Our previous $\pm 30\% \mu$ and $\pm 1V V_{th}$ process, and (d) Based on our present $\pm 4.9\% \mu$ and $\pm 0.43V V_{th}$

5.4 CONCLUSIONS

For the designability of Printed Electronics, we have described an Open-Platform PDK to facilitate the design and simulations of Printed Electronics circuits and systems. Our PDK embodied an accurate yet simple model that can not only model the Printed Electronics transistors when they are flat (and based on layout) but can also model the Printed Electronics transistors when they are bent. Our PDK also included the layout design rules. The efficacy of the PDK and the model have been verified by comparing simulations against measurements on individual components and translated to several fundamental analog and digital circuits embodying said components. The simulations agreed well with the measurements, depicting the efficacy of our proposed PDK and proposed model.

Chapter 6 Conclusions and Recommendations

In this chapter, conclusions will be drawn for the work reported in this Ph.D. program, and recommendations for future work delineated.

6.1 CONCLUSIONS

The broad objective of this Ph.D. research program is to address the issues pertaining to the second and third supply chains of Printed Electronics-only circuits/systems, particularly that realized by a Fully-Additive All-Air-Processed Low-Temperature process. This would thereby facilitate the possibility of commercial (and low-cost) Printed Electronics-only circuits/systems. The conclusions of our research work will now be delineated.

Chapter 1 delineated the motivations of this Ph.D. research program and the specific objectives of the aforesaid broad objective.

In Chapter 2, Flexible Electronics, Hybrid Electronics and Printed Electronics, have been comprehensively reviewed in turn, including their technological challenges and application space. As the emphasis of our PhD program is Printed Electronics, our review thereafter focused on Printed Electronics, including the complete supply chain and the challenges and solutions thereto. Finally, we have reviewed our NTU Printed Electronics process that served as the preamble to Chapters 3-5.

In Chapter 3, we have investigated the most important issue of manufacturability – the variations of the printed elements. We have presented our novel Fully-Additive

Low-Cost all-air-processed low-temperature screen printing process for realizing transistors with very low variations, include very low mobility μ and V_{th} variations; to date the lowest variations of reported Fully-Additive processes. Said very low variations were achieved by two means: (i) Our polymer-small molecule blend (TIPS-Pentacene/PS) in our dual solvent system (toluene and anisole), and (ii) Blade coating of our said polymer-small molecule blend (TIPS-Pentacene/PS) in our dual solvent system. The various parameters were investigated and were optimized accordingly. The matching of two transistors have been shown to be markedly improved by means of layout.

In Chapter 4, we have investigated one of primary issues with functionality, specifically the investigation into the effects of concave/convex bending of the flexible substrate where individual printed passive and active elements and on basic-circuits are printed on. We have shown that in terms of variations, capacitor-based circuits and diode-connected circuits are preferred; and for inverters and ring oscillators, concave bending is preferred. We have proposed a novel localized self-compensation means to mitigate the variations of printed circuit-elements and circuits due to bending. The proposed means has been shown to be highly efficacious – the reduction of variations ranges from $\sim 2x$ to $>100x$ – without power dissipation, substrate-area or hardware overheads but with additional printing steps.

In Chapter 5, we have investigated the primary issue on designability. Specifically, we have described an Open-Platform PDK to facilitate the design and simulations of Printed Electronics circuits and systems. Our PDK embodied a proposed accurate yet simple model that can not only model the Printed Electronics transistors when they are flat (and based on layout) but can also model the Printed Electronics transistors when they are bent. Our PDK also included the layout design rules. The efficacy of the

PDK and the model have been verified by comparing simulations against measurements on individual components and translated to several fundamental analog and digital circuits embodying said components.

From an overall perspective, the contributions made in this Ph.D. program are significant – they provide Printed Electronics researchers useful insight from the first supply chain to the second and third supply chains of Printed Electronics to facilitate the realization of ‘intelligent’ Printed Electronics flexible circuits/systems based on low-cost, on-demand, green and scalable Fully-Additive process.

6.2 RECOMMENDATIONS FOR FUTURE WORK

On the basis of the investigations in this thesis, we recommend the following as future work:

- (i) Investigations into printing of the n -type transistors.

It was delineated in Chapter 2 that complementary circuits provide major various advantages over uni-polar circuits, such as higher noise margin and higher power efficiency. Although relatively complex circuits, such as DAC, have been realized by uni-polar (p -type) transistors in our process, the availability of both p -type and n -type transistors will provide more design flexibility with significantly improved circuit performance. The n -type semiconductors can be synthesized or obtained from commercial available materials.

In short, we propose investigations into printing n -type semiconductor and its integration with other printed layers to realize an n -type transistor – with the Fully-Additive All-Air Low-Temperature process with low variations (and complementary transistors). Meanwhile, the device stability in air and over time should be also be considered.

- (ii) Investigations to reduce the operation voltage of our printed transistors (and ensuing printed circuits).

Although the ‘high voltage’ of 60 V used in our printed transistors (and ensuing printed circuits) is largely of the same order with the literature of Fully-Additive Printed Electronics, it is incompatible with the widely commercially available power suppliers that provide low-voltage of 3-6V or lower. The threshold voltage (and the associated operation voltage) is affected by both the intrinsic material properties (e.g., dielectric constant) and the physical dimensions (e.g., dielectric thickness) of each layer in the printed transistors. For instance, screen printing thin and high- κ polymer dielectrics (e.g., P(VDF-TrFE)/PMMA/BaTiO₃/Silica nanocomposite) can be a promising method to reduce the operation voltage.

In short, we propose an investigation for the realization of a Low-Voltage Fully-Additive All-Air Low-Temperature Printed Electronics process with complementary transistors.

(iii) Investigations into the completeness of our open-platform.

As delineated in Chapter 5, our proposed model can not only model printed transistors when they are flat but can also model the printed transistors when they are bent. Additionally, our PDK also includes the layout design rules. The high efficacy of the model and the PDK have been verified.

Nevertheless, our PDK remains relatively rudimentary compared to mature PDKs in silicon design. For completeness, we propose an investigation into the dimension limitations and the upper frequency of the printed transistors and circuits. Furthermore, the investigation should include layout vs schematic check and post layout simulation – this would be helpful to reduce the circuit design cycle.

(iv) Investigations into Display/Lighting/Power Supply/Communications/Sensors

As reviewed in Chapter 1, display/lighting, power supply, communications, sensors are several key modules in a Printed Electronics system. We propose an investigation to expand the application space of our Fully-Additive All-Air Low-Temperature process.

(v) Design/printing of ‘Intelligent’ Printed Electronics circuit.

As reviewed in Chapter 1, the printed circuits in Printed Electronics remain relatively simple and the performance is typically low. To be used in real-life applications, design/printing relatively more complex (‘intelligent’) circuits would be useful, including full-fledged microprocessor. However, due to the formidable challenges delineated in Chapter 1, new design methods may be needed for ‘intelligent’ Printed Electronics circuit design, such as using asynchronous design to accommodate large process variations, and employing ‘analog computing’ to reduce the transistor count.

In short, we propose an investigation into novel circuit design methods, probably different from that applied in conventional silicon-based designs, to accommodate the limitations of Printed Electronics. This would likely expand the application space of Printed Electronics.

Author's Publications

Journal Publications

- [1] **J. Zhou**, T. Ge, E. Ng, and J. S. Chang,
"Fully Additive Low-Cost Printed Electronics with Very Low Process Variations,"
IEEE Transactions on Electron Devices, vol. 63, pp. 793-799, 2016.
- [2] **J. Zhou**, T. Ge, and J. S. Chang,
"Printed Electronics: Effects of Bending and a Self-Compensation Means,"
IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64 , pp. 505-515, 2017.
- [3] **(Invited)** T. Ge and **J. Zhou**,
"An Open Platform for Fully-Additive Printed Electronics,"
IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 7, pp. 123-132, 2017
- [4] J. Chang, X. Zhang, T. Ge, and **J. Zhou**,
"Fully Printed Electronics on Flexible Substrates: High Gain Amplifiers and DAC,"
Organic Electronics, vol. 15, pp. 701-710, 2014

Conference Publications

- [1] **J. Zhou**, T. Ge, and J. S. Chang,
"A highly-efficacious Self-compensation Means to Reduce Variations due to the Bending of the Substrate,"
IEEE International Symposium on Circuits and Systems (ISCAS), USA, 2017
- [2] T. Ge, **J. Zhou**, Y. Kang, and J. S. Chang,
"An Open Platform for Fully-Additive Printed Electronics"
IEEE International Symposium on Circuits and Systems (ISCAS), USA, 2017
- [3] J. Chang, T. Ge, and **J. Zhou**
"Printed Electronics: Effects of Bending and a Self-Compensation Means,"
2017 Flex, USA, 2017

- [4] **(Invited) J. Zhou**, T. Ge, and J. Chang,
"Fully-Additive Printed Electronics: Process Development Kit,"
IEEE International Symposium on Circuits and Systems (ISCAS), Canada,
2016.
- [5] T. Ge, H. He, **J. Zhou**, Y. Kang, and J. S. Chang,
"An investigation of THD of a BTL Class D amplifier,"
IEEE International Symposium on Circuits and Systems (ISCAS), Canada,
2016.
- [6] **J. Zhou**, T. Ge, L. Guo, N. P. J. Eileen, H. He, and J. Chang,
"A High Power Driver IC for Electroluminescent Panel: Design Challenges and
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- [7] **(Invited) J. Chang**, T. Ge, and **J. Zhou**,
"Development Kit for a Fully-Printed All-Air Low-Temperature Printed
Electronics Process,"
CMOS Emerging Technologies Research Conference (ETCMOS), Canada,
2016.
- [8] T. Ge, L. Guo, Y. Kang, **J. Zhou**, *et al.*,
"A Driver Circuit Based on the Emerging GaN-on-CMOS Process for the
Emerging Electroluminescent Panels,"
*IEEE 58th International Midwest Symposium on Circuits and Systems
(MWSCAS)*, USA, 2015.

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- [2] J. Zhou, T. Ge, and J. Chang, "Fully-Additive Printed Electronics: Process Development Kit," in *IEEE International Symposium on Circuits and Systems*, Montreal, 2016.
- [3] X. Zhang, T. Ge, and J. Chang, "Fully-Additive Printed Electronics: Transistor model, process variation and fundamental circuit designs," *Organic Electronics*, vol. 26, pp. 371-379, 2015.
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