Germanium-on-insulator for group IV laser and III-V integration on silicon

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2018

Bao, S. (2018). Germanium-on-insulator for group IV laser and III-V integration on silicon.
Doctoral thesis, Nanyang Technological University, Singapore.

<http://hdl.handle.net/10356/73379>

<https://doi.org/10.32657/10356/73379>

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

SINGAPORE

**GERMANIUM-ON-INSULATOR FOR GROUP
IV LASER AND III-V INTEGRATION ON
SILICON**

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School of Electrical and Electronic Engineering

2018

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A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2018

Acknowledgements

I would like to thank my supervisors, Assoc. Prof. Tan Chuan Seng and Prof. Eugene Fitzgerald, for their continuous support and patient guidance throughout my Ph.D. study. I would also like to thank Dr. Lee Kwang Hong for his mentoring on epitaxy, bonding and characterisations. Additionally, I would like to express my appreciation to A/P Donguk Nam for his helpful guidance and valuable suggestions on strain engineering for Ge nanowire laser.

I would also like to thank Dr. Chong Gang Yih, Dr. Tan Yew Heng, Dr Wang Bing, Dr. David Kohen, Dr. Wang Cong, Dr. Zhang Li, Dr. Qiu Haodong and Dr. Riko I Made for their guidance and assistance in my experiments. I extend my gratitude to the group members: Mr. Chua Shen Lin, Dr. Anantha P, Mr. Lin Yiding, Mr. Li Wei, Dr. Wang Yue, Mr. Daeik Kim, Mr. Chibuzo Onwukaeme, Mr Yongduck Jung and Mr. Yeji Kim. In addition, sincerely thanks to the lab staffs Mr. Chung Kwok Fai and Ms. Ng Ling Ling for their helps.

My deep appreciation goes to the National Research Foundation Singapore and Singapore-MIT Alliance for Research and Technology's (SMART) Low Energy Electronic Systems (LEES) for the funding support in my research.

Finally, I'm deeply grateful to my family, for their support, care, and encouragement.

Abstract

Germanium (Ge) laser on Ge-on-insulator (GOI) shows great promises as the light source in photonic integrated circuits (PICs) for future data communication and sensing applications. In addition, small lattice mismatch between GaAs and Ge also enables hybrid integration of III-V photonics on silicon (Si) platform via a GOI substrate. This thesis is focused on the development of a high quality GOI substrate for photonics integration. A low-threshold Ge nanowire laser structure was fabricated on the GOI substrate, and the GOI substrate was also used for the epitaxial integration of III-V photonics on Si.

Firstly, in order to fabricate a GOI substrate, a Ge layer needs to be grown on a Si wafer and then transferred to an insulator/substrate via wafer bonding. The Ge layer was directly grown on an 8 inch Si (001) substrate (Ge/Si) using a two-step growth method by metal-organic vapour deposition (MOCVD). Due to the large lattice mismatch ($\sim 4\%$) between Ge and Si, the threading dislocation density (TDD) of the Ge buffer on Si was high (TDD $\sim 1 \times 10^8 \text{ cm}^{-2}$). By introducing a highly arsenic (As)-doped Ge seed layer to the growth steps, the dislocation velocity in Ge was increased, resulting in a low TDD of $5 \times 10^6 \text{ cm}^{-2}$. Then the Ge/Si wafer was bonded to an 8 inch Si (001) wafer with a bonding dielectric layer to form a GOI structure. The investigations on wafer bonding processes, in terms of TDD reduction and thermal bubbles suppression were conducted to obtain a high-quality mechanically-stable GOI substrate for photonics integration.

Secondly, although Ge is a very promising gain material that enables a monolithically integrated light source on Si, it is still very challenging to achieve a low-threshold Ge laser due to its indirect bandgap. In this thesis, a highly strained Ge nanowire laser structure was fabricated on the previously developed GOI substrate. By employing a high uniaxial tensile strain of 1.6 % in the Ge nanowire, direct band transitions were promoted, resulting the reduction in lasing threshold density to $\sim 3.0 \text{ kW cm}^{-2}$ at 83 K under optical pumping. An unambiguous multimode lasing action was evidenced by nonlinear threshold behavior in output power and linewidth narrowing as a

function of pump power. These achievements markedly narrow the gap between conventional III–V lasers and group IV lasers, thus opening up new avenues for PICs.

Thirdly, the epitaxial integration of III-V on GOI shows another promising approach for large-scale electronic-photonic integration. Since the GOI substrate resolves the issue of the lattice mismatch between III-V and Si, III-V initiation conditions on Ge surface are essential to the materials quality of III-V epi-layers. A high-quality GaAs buffer grown on Ge was achieved using a high AsH₃ partial pressure of 5 mbar to suppress the formation of anti-phase boundaries (APBs), and the root-mean-square (RMS) roughness was reduced below 1 nm. Then, the GaAs/GOI structure was used as a substrate template for the growth of an AlGaInP LED structure on Si. The LED performance on GOI was investigated to explore the possibilities of using GOI for III-V photonics integration.

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Chapter 1: Introduction

1.1 Background

1.1.1 Overview of Photonic Integrated Circuits

According to Moore's Law, supercomputer performance doubles every 18 months. Thus, large volume data transmission technologies are highly demanded. However, it is very challenging to extend the bandwidth beyond 100 Gbs⁻¹ using copper interconnects [1]. Huge power consumption and heat dissipation in electrical wires become more influential to the computing performance.

Large scale photonic integrated circuits (PICs) for on-chip and off-chip data communication using optical interconnects have shown great promise to overcome the performance bottleneck of traditional copper interconnects in high-performance computing centres [2], [3]. The optical interconnects use light for data transmission, which eliminates the problems of electromagnetic interference, interconnect parasitic and signal loss and delay in long distance transmission [4]. In a fully integrated photonic system, as shown in Fig. 1.1, individual photonic components (lasers, modulators, multiplexers, demultiplexers and photodetectors) are built on the same platform and connected with processors for optical and electrical signal conversion and data transmission [5]. The recent reports on the optical interconnects have demonstrated encouraging progress in terms of modulator and photodetector performance [6], monolithic integration processes [7], and multiple-wavelength accessibility [8]. Additionally, Intel Cooperation has built a 4-channel integrated optical link with an aggregate bandwidth of 40 Gbs⁻¹ and a low error-bit-rate of 10⁻¹² [9].

However, having a low-cost, efficient light source compatible with complementary metal-oxide-semiconductor (CMOS) electronic circuitry remains one of the biggest challenges in the PICs. Group IV and III-V materials are considered promising candidates for the light source in the PICs. Group IV materials are compatible with CMOS processes, but they are indirect band materials and inefficient for light emission. Direct band-gap III-V can be used

for high performance lasers, but the fabrication is complex and costly, and it is difficult to avoid cross-contamination with CMOS circuitry [10], [11].

Fig. 1.1 A schematic of an photonic integrated circuits (PICs) for large-volume data transmission [5].

1.1.2 Group IV Light Sources

Group IV materials (Si, Ge, $\text{Si}_{1-x}\text{Ge}_x$ and Sn) are chemically compatible with CMOS circuitry, and group IV laser on Si is promising for monolithic, large-scale electronic-photonic integration [12]. However, most group IV materials are indirect band-gap materials, which are not efficient for light emission. For indirect band materials, free electrons tend to reside in the indirect valleys of the conduction band rather than in the direct Γ valley. Therefore, phonon-assisted transitions are involved to conserve the momentum of the carrier recombination process, which reduces the optical transition rate. In addition, radiative recombination also needs to compete with other non-radiative recombination processes, such as Auger recombination, indirect recombination and free-carrier absorption. These processes further reduce the luminescent efficiency of indirect band materials. The poor luminescent efficiency caused by indirect band properties becomes the main drawback of group IV light sources in PICs. Therefore, recent research efforts on integrated Si photonics are focused on the development of an efficient light source for the PICs. Since lasers are a preferred light source in data transmission, the recent progress on group IV lasers is introduced in the following sections.

Raman Si Laser

An all-silicon Raman laser with an optical pump power density of 2.5 kW/cm² has been demonstrated [13]. In order to achieve a net gain, a rib waveguide containing a p-i-n diode structure in Fig. 1.2 was designed to reduce the cavity loss caused by two-photon generated free carrier absorption (FCA) [14], [15]. By applying a reverse biased voltage of 25 V to the p-i-n diode structure, the carrier lifetime is shortened. As a result, the nonlinear loss due to the two-photon absorption induced FCA is reduced [13]. A continuous wave (c.w.) Raman lasing can be achieved in the near future by improving the materials and cavity design. However, indirect band properties of Si are still the major limiting factors on the Si Raman laser performance.

Fig. 1.2 A cross-sectional schematic of a p-i-n Si ridge waveguide Raman laser on a silicon-on-insulator (SOI) substrate. A reverse biased voltage is applied to the device to reduce the free carrier absorption loss.

Ge-Based Lasers

Ge has a direct band minimum located ~140 meV above its indirect L valley (in Fig. 1.3a). This small energy difference can be compensated by band engineering techniques. Three main band-gap engineering techniques are used for a more direct band-gap Ge material: (1) n-type doping [16], (2) Sn incorporation [17] and (3) strain engineering [18]. These techniques have

demonstrated promising proof of principle in the recent development of a Ge-based laser on Si.

Fig. 1.3 Band structures of (a) bulk Ge and (b) heavily n-type doped Ge. The energy difference between Γ valley and L valley is ~ 140 meV. Heavy n-type doping causes a band filling effect and intra-valley scattering, which increase the carrier injection into the Γ valley [12].

In heavily doped bulk Ge, since the Fermi level increases with increasing doping concentration, the n-type doping causes the band filling effect in indirect L conduction band. When the Fermi level reaches the Γ band minimum at $n = \sim 1 \times 10^{19} \text{ cm}^{-3}$, Ge becomes a pseudo-direct band material and more electron carriers are injected into the Γ band valley, resulting in the enhancement of direct band transitions, as shown in Fig. 1.3b [19]. Based on these mechanisms, a heavily n-type doped ($\sim 1 \times 10^{19} \text{ cm}^{-3}$) 0.2% biaxial tensile-strained Ge with laser action at room-temperature was reported [19], and its optical pumping threshold was 36 kW/cm^2 . Later, an electrically pumped Ge laser doped to $\sim 4 \times 10^{19} \text{ cm}^{-3}$ was demonstrated [20]. However, the above results of lasing actions have not substantiated yet with similarly doped and strained materials [21]. One possible explanation was that heavy n-type doping in Ge generated not only direct band gain, but also pump-induced absorption (PIA) [22]. As a result, the optical gain from the strain and doping were not sufficient to

compensate for the loss, and the optical amplification in heavily doped Ge was prohibited.

Another concept is to incorporate Sn atoms into Ge to reduce the band-gap of Ge at the Γ point to form a direct band GeSn material. The indirect-to-direct band transition of $\text{Ge}_{1-x}\text{Sn}_x$ alloy occurs when x is between 6% and 10%, and the temperature-dependent photoluminescence (PL) measurement showed direct band material behaviours [23]. A partially strain-relaxed GeSn with 12.6% Sn grown on Ge-on-Si demonstrated lasing under optical pumping [17]. However, it showed a high threshold of 325 kW/cm^2 at 20 K, and the lasing was observed up to 90 K under an excitation density of 1000 kW/cm^2 . Although further increasing the Sn fraction makes GeSn a more direct band alloy for a lower lasing threshold, the major challenges for the realization of such an alloy come from the low equilibrium solubility of Sn in Ge and the large lattice mismatch between Ge and Sn [24].

Other investigated approaches concern the strain engineering techniques to tune the band profile of Ge. The simulation and experimental results show that a biaxial tensile strain of 1.7%-1.9% [22] or a uniaxial strain of 4.6% [18] is required for direct band-gap Ge material. The simulations of biaxial and uniaxial strain effects on the Ge band structure agree well with the literature, as shown in Fig. 1.4. As the heavy-hole valence band (VB2) of Ge has a much larger density of states than the light-hole valence band (VB1), the band transitions of conduction bands to VB2 dominate. A Ge microdisk with a 1.5% biaxial tensile strain using a strained silicon nitride layer was reported [22]. The peak emission wavelength was shifted towards 2100 nm due to the strain effect. For the uniaxial-strained Ge micro-bridge structure, a large tensile strain of 5.7% has been reported [18]. Although the strain transforms Ge into a direct band-gap material, most electrons remain in the indirect conduction valleys. This is due to the larger effective electron mass of indirect conduction band ($0.56 m_0$) than that of direct conduction band ($0.22 m_0$) in Ge [25]. Therefore, the indirect conduction band has a larger density of states, and the majority electrons stay in the indirect valley. By further increasing the tensile strain to 8%, it is expected that the majority carrier transitions can occur in the direct conduction band. Nam et al. [26] proposed a gradually strained Ge micro-

bridge to enable strong carrier confinement. This structure significantly increased the carrier concentration in the active region, which resulted in enhanced emission. Although Ge-based gain materials have demonstrated great progress in laser performance [17], [19], [20], it remains very challenging to achieve a low threshold to allow their practical use in an integrated system.

Fig. 1.4 Bandgap energies vs. strain of (a) biaxial strained Ge and (b) uniaxial strained Ge. The band transitions between the conduction bands (Γ and L) to the valence bands (VB1 and VB2) are presented. The solid lines and dashed lines represent the band transitions of Γ -VB and L-VB, respectively. Indirect-to-direct band gap transition is expected at $\sim 1.7\%$ biaxial strain or 4.6% uniaxial strain along the $[100]$ direction.

1.1.3 Integration of III-V photonics on Si

Direct band-gap III-V compounds have been known for their robustness and high performance in electronic and optical devices. The realization of III-V components integrated on Si platform can be used not only for the light source in the PICs to enable on-chip optical communications [27], [28], but also for many other attractive benefits. Si substrate can be used directly as a silicon waveguide in InGaAs and InP photonics for mid-infrared emission. Since Si wafers are available in 8 inch size and above, integration of III-V on Si increases the manufacturing scalability and reduces the production cost. Furthermore, possibilities of utilizing existing CMOS infrastructures for the processing of III-V devices exist [10]. In addition, compared to conventional III-V substrates, such as GaAs, Si substrate has higher mechanical strength and thermal conductivity. However, for a III-V based integrated photonic system, each III-V component introduces many variations in topologies and process parameters, which significantly increases the complexity in fabrication and the difficulties in developing standard processes [9].

One major technique of III-V integration on Si is to use die bonding or wafer bonding to transfer III-V components or a whole III-V epi-layer to a Si substrate. The lattice mismatch between III-V and Si is no longer important as III-V components are attached to the Si substrate via covalent bond. In the past, laser dies were transferred and aligned manually with the waveguides, which is a time-consuming, expensive, low compact layout that requires highly skilled labour. Although the use of etched silicon grooves for die attachment requires minimum alignment with the waveguide after bonding [29], the manufacturing cost is still high and extra care is required to maintain good coupling efficiency.

The vertical integration of laser on the silicon waveguide by using evanescent coupling significantly reduces the complexity and cost in integration processes. This design enables wafer-scale bonding, and the III-V epi-layer is transferred with simple alignment to the top of fabricated silicon waveguides on a Si wafer. III-V components are then fabricated after wafer bonding. The optical mode of the fabricated laser overlaps both the III-V active region and the silicon waveguide, as shown in Fig. 1.5. The optical mode obtains gain from the III-V materials and is guided through the waveguide [30], and a high

theoretical coupling efficiency of ~90% could be achieved, as verified by the experimental results in [31]. However, the manufacturing scalability remains limited by the size of the III-V wafer, as 2-inch GaAs substrates are commonly used for non-nitride III-V photonics. In addition, III-V substrates, such as GaAs and InP wafers, are very fragile and expensive compared to Si wafers.

Fig. 1.5 Cross-sectional view of a vertically integrated laser on a SOI substrate. Its optical mode overlaps the III-V gain region and the Si waveguide [30].

Another technique to integrate III-V photonics on a Si substrate is to use epitaxial integration, which can increase the scalability to 8-inch or 12-inch by growing III-V materials on a Si substrate. However, due to the large lattice mismatch, the direct growth of III-V on Si generates a large amount of threading dislocations. With the development of high-quality SiGe graded buffer on Si, Ge-on-Si and Ge-on-insulator substrates [32]–[34], Ge becomes a promising candidate for III-V integration on Si since Ge has a small lattice mismatch with GaAs ($< 0.1\%$). A CMOS-compatible lateral III-V photonic-electronic integration has been demonstrated on a SiGe/Si platform, as shown in Fig. 1.6 [10]. A Si layer for CMOS fabrication was bonded to the oxide on Ge, and III-V materials were regrown on opened trenches. A III-V light emitting diode (LED) was fabricated, and an amorphous Si layer was added to protect its top surface to avoid cross-contamination during CMOS fabrication on the same platform. However, the concerns regarding III-V contamination on a CMOS

device and production lines remain. One possible solution to avoid the cross-contamination issues fully is to separate the fabrications of the III-V wafer and the CMOS wafer and then use wafer-scale bonding to obtain III-V/CMOS photonic-electronic integration. Therefore, wafer-scale bonding is only possible if the high-quality epitaxy of III-V on 8 inch Si can be achieved, as only 8 inch or larger CMOS wafers are available.

Fig. 1.6 The schematic of a CMOS-compatible substrate for III-V/Si integration. CMOS transistors and III-V LEDs are fabricated on the same platform, and the III-V device is covered with a Si layer to avoid cross-contamination during CMOS fabrication [10].

1.1.4 Germanium-on-Insulator

As mentioned in the previous sections, Ge shows great potential as both the gain material for group IV lasers and the intermediate buffer for III-V/Si integration. SiGe graded buffer on Si, Ge-on-Si (Ge/Si) and Ge-on-insulator (GOI) are promising substrate templates to enable large-scale electronic-photonic integration by using 8 inch or 12 inch Si wafers. SiGe graded buffer can achieve a low threading dislocation density (TDD) of $\sim 1 \times 10^6 \text{ cm}^{-2}$. In order to achieve such a high quality buffer, a slow grading rate of $10\% \mu\text{m}^{-1}$ is required: resulting in a rather thick graded buffer ($\sim 10 \mu\text{m}$). Cross-hatched patterns are formed during the buffer grading: leading to surface roughening. Thus, a chemical mechanical polishing (CMP) step is needed at the grading composition of $\text{Ge}_{0.5}\text{Si}_{0.5}$, which interrupts the continuous buffer growth [10].

The direct epitaxy of a thin Ge layer ($1\sim 2 \mu\text{m}$) on Si can resolve the issues caused by surface roughening, a thick graded buffer and the interruption of

epitaxy. In addition, for waveguide integrated devices, such as photodetectors, a thin layer is preferred for fast transit time. The TDD can also be possibly reduced due to the dimension of the integrated devices. Thus, the Ge/Si is a highly desired substrate if the TDD of the Ge layer can be well-controlled (TDD $\sim 1 \times 10^6 \text{ cm}^{-2}$). However, Ge/Si substrates have three main drawbacks in integrated photonics applications: (1) the Si substrate as a waveguide is transparent to the wavelength longer than 1130 nm, (2) the refractive index difference between Ge and Si is too small to provide good optical confinement and (3) the defective region at the Ge/Si interface would increase the non-radiative recombination and cause additional optical loss [35]. Therefore, a GOI structure is developed to overcome these drawbacks.

Similar to a silicon-on-insulator (SOI) structure, the buried oxide layer (SiO_2) or other types of bonding dielectrics provides a wide range of optical transparency (from ultraviolet to infrared) and a large index contrast with Ge ($> \sim 1.5$) [36]. For an 8-inch GOI substrate, the Ge layer is transferred from a Ge/Si wafer, and the defective region of the Ge layer is removed by a CMP step after the layer transfer [37]. Therefore, a GOI substrate combines the merits of both Ge/Si and silicon-on-insulator (SOI).

For III-V/Si integration, the recent achievements have demonstrated an InGaAs/GaAs HBT, InP-based HEMT and InGaP/GaAs solar cell on GOI substrates [38]–[40]. The reported TDD values of these GOI substrates are comparably high for reliable photonic devices, whose carrier lifetime is reduced along with strong non-radiative recombination due to the high TDD [41]. Therefore, the performance of III-V light emitting devices on GOI is not fully investigated yet.

1.2 Motivation and Objectives

Large-scale, compact electronic-photonic integration requires a low-cost, high-efficiency light source on the Si platform. Ge-based lasers show great promise as a monolithically integrated light source compatible with CMOS processes. Strain engineered Ge can achieve a net gain. However, the high lasing threshold needs to be further reduced for practical use in the PICs. Direct band III-V

compounds can be used for highly efficient light sources, and the manufacturing scalability of III-V photonics is significantly increased by the epitaxial integration on an 8-inch Si substrate via a Ge buffer. A GOI substrate provides the material gains and optical confinement for the Ge laser and the lattice matching conditions for III-V epitaxy on Si. The materials quality of the GOI substrate is essential to the performance of both Ge laser and III-V photonics. Therefore, the motivations of this thesis include three major topics: (1) the development of a low TDD, high bonding strength GOI substrate, (2) the design and analysis of a low threshold Ge laser and (3) investigation on III-V photonics integration on GOI.

To understand the state of art achievements on the topics mentioned above, several related papers are considered:

2013: K. H. Lee et al. reported a high-quality Ge buffer directly grown on an 8-inch Si (001) substrate [33]. A two-step growth mode was used. It started with a low temperature (LT) growth at 400 °C for a Ge seed layer, followed by a high temperature (HT) growth at 600 °C for a bulk Ge buffer. An intermediate temperature ramp (LT-HT) of ~10 °C/min was used. A post-growth annealing in hydrogen at a temperature ranging from 650 to 825 °C further reduced the TDD of the Ge buffer layer. The final Ge layer thickness was ~1 µm with a TDD of $\sim 5 \times 10^7 \text{ cm}^{-2}$ and a root-mean-square (RMS) roughness of ~0.75 nm. Most importantly, this growth recipe was developed in the Singapore-MIT Alliance for Research and Technologies (SMART) lab. Based on this progress, the TDD of the Ge/Si substrate was further reduced in order to fabricate a better quality GOI substrate.

2016: J. Petykiewicz et al. employed a high tensile strain of 2.37% in a Ge nanowire laser cavity. Direct band emission was observed from the nanowire under optical pumping [42]. The strain variation over the laser cavity created a pseudo-heterostructure leading to strong carrier confinement. It showed optical resonances with a high quality factor (Q-factor) and a wide range of tuneable emission. This work inspires the design of the Ge laser in this thesis for a low threshold laser utilizing a highly strained active region with a high Q-factor cavity.

2016: C. Wang et al. recently investigated the performance of an InGaP red LED on Ge and Ge/Si substrates with different TDDs [43]. The research showed that the Ge/Si substrate with a high TDD caused high electrical leakage and degraded the light output significantly. In order to have reliable III-V LED performance on Si, the TDD of the Ge buffer needs to be reduced below $\sim 5 \times 10^6 \text{ cm}^{-2}$, and a much lower TDD is highly desired for III-V lasers.

At this point, several research gaps in the Ge lasers and the III-V photonics integrated on GOI for the PICs are clearly identified. First, the Ge/Si wafers developed in the SMART lab by using a two-step growth method with post-growth annealing can only achieve a relatively high TDD ($\sim 5 \times 10^7 \text{ cm}^{-2}$) of the Ge/Si substrate. Either Ge laser or III-V photonics performance are significantly affected by the Ge buffer quality. A new technology needs to be investigated to reduce the TDD to the order of magnitude of $\sim 10^6 \text{ cm}^{-2}$. Furthermore, in order to fabricate a high-quality GOI substrate, optimization of the wafer bonding processes is required to avoid materials degradation and bonding defects.

Second, the state of art Ge-based lasers have a very high lasing threshold. Heavily n-type doped Ge induces high cavity loss and reduces the net gain, while it is also difficult to grow a high quality GeSn alloy with a large Sn fraction to further reduce the threshold. Then highly strained Ge becomes a promising candidate as the gain materials for low-threshold Ge lasers. Although direct band emission was observed from a highly tensile strained Ge nanowire laser cavity, the room-temperature PL measurement did not show any lasing action [42]. Therefore, modifying the design of laser cavity in terms of the strain profile and DBR mirrors is required. Additionally, the improvement of the GOI substrate quality also contributes to a longer non-radiative lifetime [44].

Third, the epitaxial integration of III-V electronics has been demonstrated on GOI substrates, but studies on III-V light emitters on GOI have not been fully investigated. With the improvement of GOI substrate quality and the growth conditions of III-V compounds on GOI, the possibilities of using GOI substrates for III-V LEDs or even lasers can be explored for future PICs.

The key to filling these research gaps is to develop a high-quality GOI substrate for the Ge laser and III-V/Si integrations. The ultimate goals are to develop a low-threshold Ge laser on GOI and explore the epitaxial integration technology of III-V photonics on GOI. In this thesis, the four main objectives are to:

1. Improve the epitaxy quality of the Ge buffer on an 8-inch Si substrate.
2. Optimize the bonding processes to achieve a high-quality GOI substrate.
3. Design and fabricate a low-threshold Ge nanowire laser on GOI.
4. Investigate the epitaxial integration of III-V LEDs on GOI.

1.3 Major Contributions

The scope of the research work on integrated photonics on GOI substrates in this thesis is:

- Studies on the n-type doping effect on the reduction in TDD of the Ge buffer directly grown on the Si substrate.
- Development of the 8-inch wafer-scale bonding process to suppress defect formations and obtain a high bonding strength for a GOI structure.
- Design and fabrication of a Ge nanowire laser benefiting from strain-induced net gain and high Q-factor cavity design for a low-threshold laser.
- Investigations on the growth conditions to initiate III-V growth on the Ge surface and the characterizations of III-V LED performance on GOI.

The studies on the n-type doping effect on the reduction in TDD were based on the previous work of using a two-step growth mode for the epitaxy of a Ge/Si substrate. In the step of a low-temperature Ge seed layer, a heavy n-type doping was employed in order to increase the dislocation velocity. The doping effect on TDD reduction was characterized by electron-beam and optical inspection techniques.

Then the Ge layer of the Ge/Si substrate was transferred to an 8-inch Si wafer via bonding. The materials quality of the Ge layer could be degraded during the bonding and layer transfer processes and new defects would form at the bonding interface. Therefore, two aspects of developing the wafer bonding processes are: (1) removal of the defective region of the transferred Ge layer and (2) studies on bonding dielectrics to eliminate thermal bubbles at the bonding interface.

A Ge nanowire laser structure was fabricated on the developed GOI substrate. The design of the nanowire and the DBR mirrors determined the strain profiles and the Q-factor, respectively. Simulations and experimental measurement of the laser geometry and properties were conducted in terms of (1) strain distribution, (2) optical confinement, (3) temperature-dependent lasing action and (4) parameters fit from lasing emission.

The epitaxy and characterizations of AlGaInP red LEDs on GOI substrates were investigated. The growth conditions of the initiation of GaAs on Ge surface were optimized to suppress the APBs and surface roughening by using a high arsine (AsH_3) pressure. Then the III-V epitaxy continued to grow a multi-quantum wells (MQWs) AlGaInP red LED structure. The electrical and optical performance were analysed and compared with the LEDs on a bulk Ge substrate.

1.4 Thesis Organization

This thesis is organized into seven chapters. Chapter 1 is the introduction of the thesis and provides the background, motivation and objectives, contributions, and organization of the thesis.

Chapter 2 describes the research methods and equipment used in this thesis. It contains the epitaxy of Ge/Si and III-V, the wafer bonding techniques and the materials and device characterizations.

Chapter 3 studies the n-type doping effect on threading dislocation velocity in order to reduce the TDD of the Ge buffer directly grown on Si (Ge/Si). The aims of this chapter are to (1) introduce n-type doping to the LT

Ge seed layer and (2) study the effects of dopants and doping concentrations on the TDD of the Ge buffer.

Chapter 3 also describes the wafer bonding processes by using the Ge/Si wafer to fabricate a GOI structure. The aims of this chapter are to (1) develop the wafer-scale bonding processes for 8-inch wafers, (2) reduce the defect density and surface roughness of the transferred Ge layer, and (3) develop the bonding dielectrics to suppress thermal bubbles.

Based on the achievements of a high-quality GOI substrate, Chapter 4 reports the design, simulation, fabrication and measurement of a Ge nanowire laser structure on GOI. The aims of this chapter are to (1) obtain a high tensile strain in the nanowire, (2) design a high Q-factor cavity and (3) measure and analyse the lasing action under different pump powers, temperatures and strains.

Chapter 5 shows the epitaxial integration of an III-V LED on GOI. The aims of this chapter are to (1) initiate a high-quality GaAs buffer on Ge surface, (2) demonstrate an AlGaInP red LED structure on GaAs/GOI and (3) analyse the LED performance and compare it with the LEDs on bulk Ge.

Chapter 6 provides the conclusions of the thesis and some recommendations for future research. In particular, it presents recommendations for possible methods to (1) reduce the lasing threshold of a Ge laser further, (2) achieve lasing performance at a high temperature and (3) improve the GOI substrate quality for more reliable performance of III-V photonics.

Chapter 2: A Review on GOI Fabrication and Materials Characterization

2.1 Past Development and Techniques for Ge-on-Insulator Fabrication

Si has long been the dominant semiconductor material, and the well-established processing technology enables the production of almost defect-free wafers at low cost. With continued scaling, the performance constraints imposed become more obvious [45], [46]. GOI has emerged as an attractive alternative substrate, which exhibits the advantages of Ge as well as “on-insulator” [47]. It provides excellent carrier transport properties and hence higher saturation current and a low band-gap, which allows lower supply voltage and lower power dissipation. It is ideal for optical communication and near-IR imaging with a limited quantity of Ge [7], [48]–[50]. Besides superior electrical and optical properties, germanium layer is lattice-matched with GaAs epitaxy, making GOI suitable as a viable substrate option for III-V integration. In addition, the on-insulator advantages allow it to have mechanical stability close to the Si substrate, better electrostatic control of MOSFET application (i.e. attenuated short-channel effects [51]), lowered parasitic capacitance and the absence of latch-up [52]. Moreover, unlike the Ge substrate, GOI is compatible with the semiconductor industrial processing technique and shows better heat dissipation to the surroundings via the bulk Si substrate. Nevertheless, practical problems emerge such as a high threading dislocation density (TDD) and roughness because of the 4.2% lattice mismatch.

For the past three decades, numerous synthesis methods have been developed for the GOI structure. Methods such as germanium condensation technique [53]–[56], liquid phase epitaxy [57], [58], germanium on crystalline dielectric [59]–[61], layer transfer with Smart CutTM [62]–[67], wafer bonding and etch-back technique have their respective advantages and limitations in terms of the fabrication of wafer-scale GOI [37], [47], [68]–[70].

Germanium Condensation Technique

The germanium condensation technique is based on high temperature dry oxidation of the SiGe epitaxial layer, which is grown on a Si-on-insulator (SOI) substrate. The condensation method includes two steps: (1) the epitaxy of pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ followed by (2) thermal oxidation in a dry O_2 atmosphere, as shown in Fig 2.1. First, an initial SiGe layer with a low Ge fraction is deposited onto a SOI substrate via ultrahigh vacuum CVD or reduced pressure CVD systems at 650 °C. Then thermal oxidation is carried out in a 100% oxygen atmosphere at temperatures lower than the melting point of $\text{Si}_{1-x}\text{Ge}_x$ (< 1400 °C). Since the melting temperature of $\text{Si}_{1-x}\text{Ge}_x$ decreases with increasing Ge fraction, the oxidation temperature is continuously reduced during the condensation process. Finally, at an oxidation temperature of 900 °C, a homogeneous Ge layer is obtained.

The germanium condensation method is a simple and conventional process that leads to high quality ultrathin GOI with a low surface roughness (RMS roughness = 0.4 nm) [54]. GOI fabricated via this method has been proven a good candidate material for p-MOSFET. The hole mobility has over four times enhancement as compared to Si [55]. However, the high thermal budget (>1200 °C) and the large amount of dislocations pose limits to this method in GOI fabrication.

Fig. 2.1 The GOI fabrication process using germanium condensation by oxidation. (a) Epitaxy of SiGe on SOI, (b) the oxidation of SiGe forming Ge and SiO_2 , and (c) a homogeneous Ge is obtained after condensation [56].

Liquid Phase Epitaxy

Germanium-on-insulator without dislocation or stacking fault can be realised through liquid phase epitaxy using defect necking techniques [57]. In liquid phase epitaxy, Ge is first sputtered onto a Si substrate patterned with silicon nitrides. Then the Ge film is encapsulated by a low-temperature oxide layer. This step is followed by rapid thermal annealing (RTA). During the cooling processes, liquid phase epitaxy occurs at the Si/Ge interface inside the trenches following the Si substrate orientation, and the epitaxy propagates over the trenches laterally forming a high quality GOI strip with low-defect density [58]. However, this method still faces several limitations such as complicated fabrication processing, limited lateral extent, and a large portion of surface area is still very defective.

Germanium on Crystalline Dielectric

Germanium grown on crystalline dielectric is a fully epitaxial approach to fabricate a GOI substrate. Although GOI structures have been demonstrated on Si (100) substrates using highly crystalline oxides such as SrHfO_3 (SHO) and $\text{SrHf}_x\text{Ti}_{x-1}\text{O}_3$ (SHTO) oxide systems [61], the large lattice mismatch between Ge and oxides causes a highly defective Ge layer (TDD of $10^8\sim 10^9 \text{ cm}^{-2}$).

Layer Transfer with Smart Cut™

Layer transfer by the Smart Cut™ technique was first introduced in 1995 for SOI fabrication [62]. Its application has been further extended for a variety of heterostructures, such as Si on quartz wafer, SiGe on insulator [63], [67], strained Si on insulator, silicon carbide on insulator and Ge on insulator [64], [65].

Four steps are involved in the fabrication of GOI via the Smart Cut™ technique, as shown in Fig 2.2. First, a Ge bulk donor wafer coated with PECVD deposited oxide layer is implanted with H^+ . The implanted hydrogen ions are trapped in the inherent voids in the Ge atoms. Second, after necessary cleaning processes, the Ge donor wafer is bonded to a Si handle wafer coated with a thermal oxide layer at room temperature. Third, the thermal activation under $400\sim 600^\circ\text{C}$ annealing condition accelerates the hydrogen molecules

agglomeration at the highly implanted region and breaks the Ge-Ge bonding. The annealing results in the split of the Ge donor wafer from the bonded pairs and forms a GOI substrate [66]. Finally, fine polishing and thermal treatment are applied to prepare the GOI substrate for device fabrication. Although the Smart Cut™ technique provides a versatile and robust way to obtain a high-quality GOI substrate, the Ge donor wafer constrains the GOI wafer-size to 200 mm and below, and the Ge layer thickness in GOI is below 300 nm. These limitations restrict the use of GOI wafers for large-scale fabrication.

Fig. 2.2 Schematic of the Smart-Cut process [66].

Wafer Bonding and the Etch-back Technique

Wafer bonding and the etch-back method shares some similar fabrication processes with Smart Cut™ techniques including wafer bonding, layer transfer, fine polishing and thermal treatment. The donor wafer is a Ge-on-Si (Ge/Si) substrate, which overcomes the obstacle of the small Ge donor wafer-size [68]. Additionally, the etch-back method enables a thick Ge layer to be transferred to the handle wafer.

In this method, the material quality of the Ge layer on insulator is highly dependent on the epitaxy quality of Ge on Si [69], [70]. Benefiting from recent progress in developing the Ge/Si epitaxial and processing methods, the defect density of the GOI substrate can be reduced to 10^6 - 10^7 cm^{-2} with low surface

roughness [37]. Table 2.1 compares the advantages and disadvantages of each method. This work is focused on the development of the wafer bonding and etch-back method, since it shows great promise to achieve a high-quality and large wafer-size GOI substrate.

Table 2. 1 Comparison of different GOI on Si substrate fabrication methods.

Method	Advantages	Disadvantages
Germanium Condensation Technique	<ul style="list-style-type: none"> • Simple and conventional processes • Orientation identical to SOI layer • Low surface roughness • A very thin GOI layer with high purity • Hole mobility enhanced 	<ul style="list-style-type: none"> • High thermal budget • Large amount of dislocations, including microtwins and threading dislocations
Liquid Phase Epitaxy	<ul style="list-style-type: none"> • Compatible with Si-based fabrication • High quality film • Orientation controlled by the Si substrate • Allow integration at desired location 	<ul style="list-style-type: none"> • Additional lithography steps • Limited lateral extent of GOI • Surface loss due to defective seed region
Growth on Crystalline Dielectric	<ul style="list-style-type: none"> • Fully epitaxial approach • Relatively flat surface 	<ul style="list-style-type: none"> • Highly defective of $\sim 10^8$-10^9 cm⁻² • Not applicable in device application
Layer Transfer with Smart Cut™	<ul style="list-style-type: none"> • Commercialized process and versatile method • Donor wafer reusable • High quality GOI • Low defect density <10⁵ cm⁻² • Thickness homogeneity (deviation~5%) • RMS of 0.2 nm 	<ul style="list-style-type: none"> • Size constraint caused by the fragile nature and productivity of Ge bulk wafers • Thermal mismatch of heterostructure, especially in the case of large diameter integration
Wafer Bonding and Etch-back	<ul style="list-style-type: none"> • No size constraints • Smooth and thin surface with CMP • TDD: 10⁶-10⁷ cm⁻² 	<ul style="list-style-type: none"> • Complex synthesis process • Requires high quality Ge/Si, which cannot be reused

2.2 Epitaxy and Processing of Ge/Si Substrate

Wafer bonding and the etch-back method show great promise in achieving a high-quality and large dimension GOI substrate. Its quality is highly dependent on the epitaxy of Ge on Si, as mentioned in Section 2.1. Therefore, the epitaxy and processing methods to create a high-quality Ge/Si substrate are discussed in this section.

2.2.1 Materials Growth

A production-style metal-organic chemical vapour deposition (MOCVD) system is used exclusively in this work for the epitaxy of group IV and group III-V materials. The Aixtron Crius MOCVD reactor was installed at the SMART-LEES laboratory in Singapore. In Fig. 2.3, the MOCVD reactor is equipped with a close-coupled showerhead. Small holes are uniformly distributed over the showerhead and chemical gases can be injected through these holes to sample surface. Samples are placed inside sample holders on a graphite coated susceptor. The susceptor is changeable and able to load multiple wafers with different dimensions: 2"×6, 6"×1 and 8"×1. An 11 mm gap between the susceptor and the showerhead is kept constant to prevent parasitic reactions in the vapour phase.

Fig. 2.3 Image of the MOCVD reactor showerhead and 2"×6 susceptor.

Group IV hydride gases, germane (GeH_4) and silane (SiH_4), are needed for Ge and Si epitaxy, respectively. Arsine (AsH_3) and phosphine (PH_3) are the group V hydride gases used for n-type doping in group IV materials. For III-V epitaxy, AsH_3 and PH_3 hydride dopant sources become hydride precursors to provide the reagents of As and P in III-V compounds. The group III precursors include trimethyl-gallium (TMGa), trimethyl-indium (TMIn) and trimethyl-aluminum (TMAI). Diethyl-tellurium (DETe) is used for n-type doping and dimethylzinc (DMZn) is used for p-type doping. An informative illustration of the MOCVD epitaxy for Si, Ge, and GaAs is shown in Eqs. (2.1)–(2.3) [71], [72]:

Hydride precursors are injected directly from gas cylinders, while solid or liquid precursors (TMGa, TMIn and TMAI) and dopant sources (DETe and DMZn) are stored in bubbler cylinders, as shown in Fig. 2.4. Ultra-high purified hydrogen (H_2) is supplied by a hydrogen generator and serves as carrier gas to pass through the gas cylinders. The chemical vaporizes in the bubbler and mixes with the carrier gas. Then the gas mixture leaves the bubbler and flows to the reactor. H_2 carries out the evaporated chemical gases from the bubbler, and a mass flow controller (MFC) is used to control the gas flow rate. As the temperature and pressure inside the cylinder are important to the chemical evaporation, both parameters are kept constant for each cylinder to calculate the effective flow rate [73].

Fig. 2.4 Schematics of the precursor bubbler. The flow rates of the carrier gas and the gas mixture are controlled by a MFC and many valves.

For MOCVD, the deposition of a solid from the vapour phase can be modelled by the processes of restoring a non-equilibrium to an equilibrium condition in terms of Gibbs free energy [74]. The difference of the Gibbs free energy between the deposited chemicals in the vapour and solid phases is the driving force for the deposition. These deposition reactions are governed by thermodynamics, kinetics and hydrodynamics of the growth processes [71]. As shown in Fig. 2.5, the growth processes have three main steps: (1) gas phase reactions, (2) transportation to surface and (3) surface reactions. The pyrolysis of the injected precursors starts from the first step. Then the pyrolyzed precursors transport to a so-called boundary layer between the main flow region and the interface region. The gas velocity decreases to zero at the deposition surface and surface reactions occur, such as thermal adsorption of reagents, diffusion of ad-atoms, chemical reactions on wafer surface forming epi-films and generating other by-products [71].

Fig. 2.5 Growth process steps: gas phase reaction, mass-transport to surface and surface reactions.

As shown in Fig. 2.6, at low temperature the surface reaction is slow and the growth rate is kinetically limited by the rate of surface reaction. At high temperature, the rate of surface reaction is high, where the growth rate is relatively insensitive to the temperature and mainly limited by the mass-transport rate through the boundary layer. At higher temperature, the parasitic reaction rate becomes significant, which reduces the growth rate. The mass-transport limited region is normally desired for MOCVD epitaxy since the growth rate is controlled by the partial pressure of the input gas [71]. Additionally, the reactor pressure is also an important parameter related to the hydrodynamic effects on the mass-transport process by influencing the partial pressure.

Fig. 2.6 Plot of the normalized growth rate, R_g as a function of growth temperature, $1/T$. The three growth regions are labelled [71].

2.2.1 Methods to Reduce Defects in Ge/Si

Due to the large lattice mismatch ($\sim 4\%$) between Ge and Si, the direct growth of Ge on Si results in a large TDD (around 10^8 - 10^9 cm^{-2}) [50]. These generated dislocations are electrically active recombination centres and cause dramatic performance degradation in electronic and photonic devices. Thus, engineered methods are needed to control the dislocation density with a low-roughness surface for device fabrication and III-V integration.

The $\text{Si}_{1-x}\text{Ge}_x$ graded buffer has been well studied for III-V integration on Si, and it has achieved a low TDD of $\sim 1 \times 10^6$ cm^{-2} grading from a Si substrate to 100% Ge [75]–[79]. The strain relaxation via grading buffers cause a cross-hatch patterned surface that requires two times CMP processes to ensure a smooth surface.

Although the direct epitaxy of Ge on Si generates a large number of dislocations, methods such as two-step growth techniques [49], [80], [81], thin buffer layer techniques [82], [83] and the H_2 annealing process [84]–[87] have demonstrated great promise in achieving a high-quality Ge/Si substrate via the direct epitaxy method.

Two-Step Growth Technique

As the name implies, the two-step growth technique involves two growth steps. First, a 30 nm Ge layer is grown at a low temperature of $330\sim 350$ °C. At the low temperature growth, island formation is suppressed due to the low surface diffusivity of Ge atoms and strain is released via misfit dislocations [49]. Then the temperature is increased to 600 °C to homo-epitaxially grow a thick Ge buffer until the desired thickness with a high growth rate is achieved.

Colace's group used a thin buffer layer of Ge to obtain a high quality Ge layer through the low pressure chemical vapor deposition (LPCVD) using pure germane source material without carrier gas [49]. They first grew a 50 nm buffer layer with a H_2 surfactant. The presence of the H_2 surfactant inhibited the nucleation of 3D islands. Then a growth at 500°C was carried out. A Ge layer with less dislocated material and a RMS around 0.5 nm resulted. Cyclic

annealing was added to reduce TDD and obtain a planar surface [80]. As a result, a TDD around $2.3 \times 10^7 \text{ cm}^{-2}$ and a RMS around 0.5 nm was achieved. The TDD can be further reduced by 1 magnitude by selective area growth combined with cyclic annealing.

Relatively low TDD together with low surface roughness can be achieved via a two-step growth technique. However, a large thermal budget is required in high temperature annealing, which causes the interdiffusion of Si and Ge. As in device application, a sharp interface is more favourable. To minimize the interdiffusion, Dehlinger et al. carried out experiments following Luan's method in which a SOI substrate was employed to minimize the available Si source for interdiffusion [81]. The TDD in their experiment was 10^8 cm^{-2} .

Thin Buffer Layer Technique

The thin buffer layer technique can eliminate the disadvantage of the graded layer growth method while obtaining a high quality epilayer. With the growth of a thin buffer layer in Ge on a Si structure, dislocation can be trapped at the heterojunction, which will lead to a reduced dislocation density in the Ge layer [82]. Huang et al. used two thin buffer layers with a total thickness of $1 \mu\text{m}$ to develop Ge on Si material, which is applicable in photodetector fabrication [82]. Nakatsuru's group modified this technique with a further reduced buffer layer thickness down to 10s of nm [83]. In their experiments, a thin buffer layer combined with two-step growth method was used and a high quality Ge layer with a RMS of 0.44 nm was generated.

H₂ Annealing Process

Post-growth annealing carried out in a H₂ environment can reduce surface roughness and threading dislocations. Formation of H-Ge clusters during annealing enhances the surface mobility and diffusivity by reducing the diffusion barrier [84]. As a result, the gliding of threading dislocations is promoted and dislocation annihilations occur. The cyclic annealing in the H₂ ramping temperature fluctuating between 680 °C and 825 °C achieved a low TDD of $2 \times 10^7 \text{ cm}^{-2}$ [86]. Choi et al. applied H₂ annealing during the growth

with a cyclic growth mode [85], and they also observed the reduction of both roughness and TDD to 0.4~0.6 nm and $0.8\sim 1\times 10^7 \text{ cm}^{-2}$, respectively.

2.3 Wafer Bonding Techniques

This section is focused on the bonding techniques to transfer a high-quality Ge buffer on a Si substrate with an insulating layer. Successful wafer bonding can only be achieved under stringent requirements in bonding energy, surface cleanness, roughness and flatness.

2.3.1 Bonding Energy

Room temperature bonding is formed through van der Waals interactions or hydrogen bridge bonds. It is usually accompanied by applying a force at one point that allows the bond front to propagate. The propagation of the bond front leading to interface adhesion is dependent on the balance between the surface energy and the interface energy, as shown Fig 2.7 [88]. In that figure, W is the work of adhesion of a bonded area, γ_1 and γ_2 are the surface energies bonding materials, and γ_{12} is the interface energy.

Fig. 2.7 Plot of the bonding force vs. the separation at bonding interface. The shaded region shows the work of function, summed by surface and interface energies [88].

In order to evaluate the bonding strength of a bonding interface, a crack opening model is used by inserting a razor blade into the bonded wafer edges, as shown in Fig 2.8. The bonding strength, γ , can be expressed as shown in Eq. (2.4) [89]:

$$\gamma = \frac{3Ed^3 y^2}{8L^4}, \quad (2.4)$$

where E is the elastic modulus, y is the thickness of the razor blade, d is the thickness of a single wafer, and L is the measured crack length along the bonding interface.

Fig. 2.8 Schematic of the crack-opening method that determines the surface energy [90].

2.3.2 Bonding Surface Requirements

Bonding surface requirements contain three stages: (1) surface cleaning processes, (2) surface roughness and (3) wafer bow (surface flatness). Surface cleaning processes are essential to wafer bonding as they affect the chemical and electrical properties of the bonding interface [91]. The surface needs to be free of organic and metallic contamination and particles. Therefore, proper surface treatment must be applied to ensure a clean wafer surface while not degrading the roughness of the wafer surface.

The Radio Corporation of America (RCA) cleaning method, developed by Werner Kern while working for RCA in 1965, is commonly used in the semiconductor industry. This method is also used for surface treatment in wafer bonding. The RCA cleaning process involves two hydrogen peroxide-based chemicals: RCA1 ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1: 1: 5$) and RCA2 ($\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O} = 1:$

1: 6). RCA1 is designed to remove organic contaminants, especially hydrocarbon, via the oxidizing action of H_2O_2 and the solvating action of NH_4OH . Since NH_4OH can attack the Ge surface and increase the surface roughness, it is recommended to reduce the ratio of NH_4OH in RCA1 for wafer cleaning. A strong oxidizer periodic acid, H_5IO_6 , is often used after RCA1 cleaning to remove hydrocarbon residue. Then RCA2 is applied to remove metallic (ionic) contaminants.

Besides organic and metallic contaminations, the presence of particles also causes serious issues during bonding processes. The particles function as spacers and prevent intimate contact between two mating wafers, leading to unbonded areas or intrinsic voids. The size of the void depends on the dimensions of the particles and the bonding strength. Although the particle size can be as small as few micrometres, it can lead to voids of several millimetres large. The use of megasonic cleaning, dust-free wafer transport and a higher class (preferably Class 1) cleanroom environment can effectively reduce the number of particles during wafer bonding.

Surface roughness is a microscopic parameter of wafer surface quality that is crucial to wafer bonding. A low RMS roughness below 0.5 nm is suggested for bonding at room temperature via hydrogen bonds [91]. The CMP process is a powerful technique that produces a low RMS surface roughness less than 0.1 nm.

Wafer bow is also an important factor in achieving a void-free bonding interface. Wafer bow is defined as the macroscopic deviation of the front wafer surface from a reference plane with the assumption that the back-side of the wafer is flat [91]. When bonding two well-polished wafers together, the gap between the wafers caused by flatness deviation needs to be overcome and deformed into a common shape [88]. Otherwise, the gap prevents the wafers from bonding together or it causes unbonded areas. External or internal strain can help to reduce wafer bow to achieve a high-quality bonding interface.

2.3.3 Thermal Bubbles Generation, Causes and Prevention

Thermal bubbles originate from the by-products reaction at the bonding interface, and they become a detrimental factor to the bonding quality. In hydrophilic bonding, the bonding is initiated between two mating surfaces via van der Waals interactions or hydrogen bridge bonds [92]. Then the bonding is strengthened by thermal annealing with the release of bonding by-products such as H_2O and H_2 . Only a small portion of the bonding by-products can be removed from the bonding interface via lateral diffusion. The rest of them are trapped at the bonding interface [90], [93]. However, these trapped by-products can diffuse through oxide or nitride insulating layers at a high temperature of 900 °C [94], [95]. Meanwhile, the high temperature may cause undesired dopant diffusion or deteriorate the bonding structure. Therefore, it is crucial to find other methods to eliminate the thermal bubbles. Since the main species in the thermal bubbles is H_2 , and it dissolves in the oxide, a thick oxide layer in the bonding structure may help reduce the formation of thermal bubbles.

2.4 Materials Characterisations

X-Ray Diffraction (XRD) and Micro-Raman Spectroscopy

The X-ray diffraction (XRD) tool is used to measure in-plane and out-of-plane lattice parameters of semiconductor materials, and the materials strain state can be calculated from these parameters. Reciprocal space mapping (RSM) is a powerful function in XRD, which provides more information on the composition and strain state of a multi-layer structure [96]. In this work, XRD was used to study the strain status of the Ge layer on Si and insulator, and RSM was used to calibrate compound compositions and characterise the lattice matching conditions of III-V layers on GOI [96].

Raman spectroscopy can be used to measure the vibrational modes from a semiconductor. The laser source of the Raman spectroscopy interacts with molecular vibrations and phonons and results in the energy shift of laser beams [97]. Therefore, information on the vibrational modes can be provided by analyzing the energy shifts. In a micro-Raman spectroscopy system, the laser beam is focused on a sample surface by the objective lens of a microscope. An

optical fibre couples the scattered light from the sample to a grating spectrometer. By moving the sample stage, the energy shift at multiple positions of the sample can be collected for a Raman mapping. In this work, a semiconductor sapphire laser at 532 nm is used as the optical pumping light source in the Raman system. The laser beam is focused on the sample by an optical microscope with a magnification of up to 100×. The depth of spatial resolution in the direction perpendicular to the sample surface is strongly dependent on the laser wavelength, optical absorption of the sample being tested, microscope objective and sample structure [98].

Under optical pumping, the coupled spectroscopy measures the phonon energy from the sample due to the lattice vibrations of a crystal [99]. This phonon energy is a parameter related to the crystal lattice constant and the strain. When the strain changes, the phonon energy changes correspondingly, causing the Raman peak shift. The measured Raman peak position can be expressed as a function of strain [100]:

$$\omega_1 = \omega_0 + b\varepsilon \quad (2.5)$$

where ω_1 is the Raman peak position under strain, ω_0 is the Raman peak position of a fully relaxed crystal, b is the strain coefficient and ε is the in-plane strain. By fitting the Raman emission spectrum using a Lorentz fit, the Raman peak positions with and without strain can be identified. Then the strain can be calculated with a known strain coefficient for that crystal.

Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a useful tool for surface morphology characterisations. A silicon cantilever with a sharp tip is mounted on a piezoelectric transducer. The photodiode in AFM measures the reflected laser beam from the cantilever, and the position information is captured when the cantilever sweeps across the sample surface under the AFM tapping mode [101]. As mentioned, the surface roughness is crucial to ensure successful wafer bonding. Therefore, the RMS roughness measured by AFM is an important criterion to evaluate the epitaxy and bonding qualities.

Transmission Electron Microscopy (TEM) and Defect Selective Etching (DSE)

Transmission electron microscopy (TEM) and defect selective etching (DSE) are the inspection techniques used to visualise defects and estimate materials defect density. TEM utilises high-energy electron beams focused on an electron-transparent thin sample. Two-beam diffraction conditions in the orientation of $\langle 220 \rangle$ are often employed for the imaging of dislocations [102]. Plan-view and cross-section TEM images can provide useful information on the defect density counting and the interface quality, respectively. However, due to the localised inspection area, TEM is usually used to inspect the materials sample with a TDD above $1 \times 10^7 \text{ cm}^{-2}$ [103]. Otherwise, it is difficult to find any defects in the image. The direct epitaxy of Ge on Si generates a high TDD of $10^8 \sim 10^9 \text{ cm}^{-2}$, and the defects can be easily found by TEM. However, after applying the engineering techniques to reduce the TDD of the Ge buffer below $1 \times 10^7 \text{ cm}^{-2}$, TEM is no longer a suitable technique to estimate the TDD.

Defect selective etching (DSE) uses chemical etching to reveal etch pits on a sample surface by repeated etching and nucleation events at the surface terminating point of a dislocation [104]. The association between TDD and etch pit density (EPD) was found [105]. This makes DSE a valid technique to estimate TDD at a low level since the etched defects can be visualised and counted under a microscope or scanning electron microscope (SEM). For the optimised Ge/Si and GOI substrates, the TDD of the Ge buffer is expected to be less than $1 \times 10^7 \text{ cm}^{-2}$. For III-V photonics and Si integration, a lower TDD (low $1 \times 10^6 \text{ cm}^{-2}$) is required for reliable LED performance. Therefore, DSE was used to calculate the TDD for these evaluations.

Secondary Ion Mass Spectroscopy (SIMS) and the Hall Effect Measurement

The highly n-type doped Ge layer is expected to reduce the TDD during Ge epitaxy on Si. The active doping carriers can also modify the Ge band structure for a more direct band-gap. Secondary ion mass spectroscopy (SIMS) and the Hall Effect measurement are commonly used to analyse doping

concentration and active carrier concentration, respectively. SIMS provides the information of elementary concentration as a function of depth in materials, and it can be used to analyse multilayer structures. In the growth of Ge on Si, in-situ doping was introduced at the Ge initiation and two-step (LT and HT) growth followed by cyclic thermal annealing. Thus, SIMS was used to analyse the doping distribution profiles throughout the Ge growth and Ge and Si inter-diffusion at the growth interface.

The Hall Effect measurement is used to analyse an electrically active doping concentration. Dopants may not be fully electrically activated at a high doping concentration due to auto-compensation, out-diffusion and competition between the absorption and desorption of the dopants [106]–[108]. Then SIMS may not be valid to correlate elementary incorporation with active doping concentration. The Hall Effect measures the Hall voltage of electrons travelling along an electrical field perpendicular to an applied magnetic field, and the carrier concentration can be determined by the measured Hall voltage and the known parameters of the applied current and magnetic field [109]. In this study, in order to ensure the in-situ dopants were fully activated, the Hall Effect measurement was compared with the SIMS measurement.

Photoluminescence

Photoluminescence (PL) is used to measure the optical properties of bulk Ge material and Ge nanowire, and the laser beam is focused via optical lenses. In direct band transitions, an electron and a hole recombines radiatively, emitting a photon. Its photon energy is equivalent to the direct band transition energy. Since Ge is an indirect band-gap material, its PL signal is very weak at room temperature due to strong indirect band transitions. Applying band engineering techniques such as strain and doping, Ge can become a more direct band material. Its direct band transition can be observed at room temperature under a high excitation power density. The PL measurement is extensively used in this work to study the impacts of doping, strain and device structure on Ge-based laser and sensor performance. It is a straightforward technique to estimate if direct band transitions are promoted by band engineering techniques by

measuring the PL peak intensity, shape and position. More information on the Ge band structure can be derived from the temperature-dependent PL measurement and PL spectrum fit.

Electro-luminescence (EL)

Electroluminescence (EL) is used to measure the optical response of the device to an electric current or an electric field. By injecting current, electron-hole pairs are created, thus making it different from the PL measurement. The excited electrons then release their energy in the form of photons. The EL measurement setup consists of a programmed signal source, probe station, a lens and spectrometer. Based on the measurement results, the light output efficiency of a LED sample is estimated by comparing the EL performance of LED grown on GOI and bulk Ge substrates.

Current-voltage Measurement (I-V)

Current-voltage (I-V) or current density-voltage (J-V) measurement is to obtain the current vs. voltage by applying a current or voltage and thus measuring the voltage or current. It is a fundamental technique to analyse LED electrical performance. In the I-V measurement of LED devices, it is focused on extracting the saturation current densities, the series resistance, the shunt resistance and the ideality factor.

Infrared Imaging

Bonding defects caused by either the presence of particles or by thermal bubbles are highly undesirable, as they result in degradation in device performance and yield. The detection of bonding defects is of great importance in direct wafer bonding. One of the most commonly used methods is infrared (IR) imaging. It utilizes the transmission of infrared radiation as silicon is transparent to radiation with a wavelength $> 1.1 \mu\text{m}$. The bonding defects are observed as dark spots, voids or interferential lines under IR imaging. Although

IR imaging is a fast and cheap method to detect bonding defect, it is limited by its resolution.

Chapter 3: Epitaxy and Bonding for Ge-on-Insulator

3.1 Introduction

As mentioned in Chapter 1, Ge is gaining attention for both electronic and photonic applications. Compared with bulk Ge wafer, a germanium-on-insulator (GOI) substrate has superior properties such as enhanced optical confinement, reduced parasitic capacitance, reduced short channel effect, improved mechanical strength and reduced self-heating effect [67], [110]–[112]. Moreover, GOI fabricated through epitaxial growth followed by wafer bonding is compatible with the current CMOS industrial processing technique. These advantages make GOI extremely favourable in volume fabrication for next generation light emitters, photodetectors, III–V integration and transistors.

As discussed in Chapter 2, most GOI fabrication techniques have their drawbacks, while wafer bonding combined with the etch-back technique is one of the most promising methods. The epitaxy quality of Ge on Si (Ge/Si) and the wafer bonding techniques have crucial impacts on the GOI quality and device performance on GOI. The main challenge for the growth of Ge on Si is still the $\sim 4\%$ lattice mismatch between Si and Ge. This can result in a high defect density with a rough surface. The well-known method to address this problem is through a SiGe graded buffer for a low TDD. Nevertheless, this method requires a rather thick buffer, the interruption of epitaxy, surface roughening and extra polishing and cleaning steps. Therefore, it will be desirable to use a simpler two-step growth method for the epitaxy of Ge on Si while having a low enough TDD for photonic applications.

In the 1960s and 1970s, several groups investigated the velocities of dislocations in undoped and doped Ge bulk crystals (grown by the Czochralski technique). They discovered that the velocity of dislocation is enhanced when the Ge crystal is doped with arsenic (As) [113], [114]. This finding motivated this research work to investigate the possibility of using n-type doped Ge to reduce the TDD in Ge/Si epitaxy.

In this chapter, a high-quality 8-inch Ge/Si substrate is developed based on a three-step growth method to reduce the TDD to $< \sim 1 \times 10^7 \text{ cm}^{-2}$. A thin highly As-doped Ge seed layer is added in order to increase the dislocation

velocity. The investigation of doping effects on the TDD is conducted to develop a doping profile for a low TDD in the Ge/Si substrate. Then, based on the characterization results, the As-doped Ge buffer on Si will be used to fabricate a high-quality GOI substrate.

To obtain a GOI structure, a Ge/Si substrate is treated as a donor wafer. Its Ge epitaxial layer is bonded and transferred to an insulator-on-Si handle wafer. In order to improve the GOI quality, studies on wafer bonding will be conducted in terms of bonding dielectrics materials, annealing conditions and the suppression of thermal bubbles formation.

3.2 Epitaxy of Ge on Si (Ge/Si)

3.2.1 Growth and Characterization of Ge/Si

Eight-inch silicon (001) wafer (p-type, resistivity = 1~100 Ω -cm) with 6° off-cut toward the [110] direction was cleaned using standard RCA solutions. Then it was dipped into a diluted HF solution (HF: H₂O = 1: 10 by volume). The 6° off-cut Si substrate was chosen because it can eliminate the formation of an anti-phase boundary for the subsequent III-V compound semiconductor materials growth. The cleaned wafer was loaded into the N₂-purged load-lock of the MOCVD reactor in preparation for Ge growth.

Prior to the epitaxy, the wafer was baked in hydrogen (H₂) at 1050 °C for 10 min to desorb the thin surface oxide. After that, a Si layer (~500 nm) was grown to condition the Si surface and bury any surface contamination in order to provide a high quality surface for Ge growth. As mentioned, a two-step Ge growth was developed for Ge/Si epitaxy in previous studies, and the growth temperature varied from 330–600 °C at low-temperature (LT) and high-temperature (HT) growth modes [49], [80], [115]. In this experiment, a three-step Ge growth on Si was introduced by combining the two-step growth with a thermal cyclic annealing in H₂, and the LT and HT growth temperatures were slightly different from the literature due to different reactor designs and conditions. The three-step growth sequence were: (1) low-temperature growth of a thin Ge seed layer at 400 °C with highly As-doped (concentration of the As dopants $\sim 10^{19}$ cm⁻³); (2) high temperature Ge growth at 650 °C by gradually

reducing the concentration of As dopants to pure Ge and (3) high temperature pure Ge growth at 650 °C to achieve the intended thickness with a reasonable growth rate. Immediately after the Ge growth, thermal cyclic annealing was introduced. The thermal annealing step can obtain a low surface roughness and reduce the TDD by enhancing the surface mobility of the Ge atoms. The thermal cycling was performed in H₂ between 650–850 °C with a repetition of five times and a 10 min hold time at 850 °C. For comparison, a control sample was grown (i.e. a Ge/Si substrate was grown under the same conditions but without As doping).

The cross-sectional bright field TEM image in Fig 3.1 shows the regrowth of a Si layer and the epitaxy of an undoped Ge layer on Si. The thickness of the Ge epitaxial film is 950 nm, which is closely matched with the targeted value of 1 μm. The 475 nm thick Si re-growth film is shown to be defect-free in the figure, and its quality is expected to be extremely good due to the homo-epitaxy. Not only can this Si re-growth layer bury some defects or small particles on the Si substrate surface, but it also replaces the 1000 °C hydrogen baking step. The hydrogen baking step was conventionally used to desorb the surface oxide film on the sample surface, which is detrimental to the sub-sequential epitaxy. As shown in the inset to Fig. 3.1, a large number of misfit dislocations are observed at the Ge/Si growth interface. These dislocations are mostly confined near the interface, and dislocation propagation throughout the Ge layer was not observed in this image. This indicates that a relatively good epitaxy of the Ge buffer was achieved. However, the cross-section TEM was not an adequate method to quantitatively estimate the TDD and to easily inspect the dislocations with a TDD lower than $\sim 1 \times 10^8 \text{ cm}^{-2}$. Thus, a plan-view TEM inspection was also performed.

Fig. 3.1 A cross-sectional TEM image of undoped Ge epitaxy on Si. A ~500 nm Si layer was re-grown on a Si substrate followed by the epitaxy of a ~1000 nm Ge layer using a two-step growth mode (without n-type doping). Inset: Magnified TEM image of the Ge/Si interface [116].

The plan-view TEM image in Fig 3.2 shows the threading dislocations at the sample surface. The TDD value was estimated based on an average number of 40 plan-view TEM images for better accuracy, and the estimated TDD is $4.8 \times 10^7 \text{ cm}^{-2}$. This TDD value agrees with the reported results of Ge/Si epitaxy using optimized two-step growth and thermal annealing techniques [49], [80], which indicate that other defect-reduction techniques need to be developed to improve the Ge/Si epitaxy quality further.

Fig. 3.2 A plan-view TEM image of the undoped Ge epitaxy on Si. The TDD of the Ge layer is $4.8 \times 10^7 \text{ cm}^{-2}$ [116].

3.2.2 Doping Effect on Dislocation Density

The early discoveries of As-doping impacts on dislocation velocity in Ge show a promising method to reduce the TDD of Ge further [113], [114]. In order to prove this concept, a high As-doping concentration of $\sim 10^{19} \text{ cm}^{-3}$ was introduced to the Ge seed layer at the low-temperature growth step, while the other growth steps remained the same. The cross-sectional TEM image in Fig 3.3 shows an As-doped Ge epitaxial layer grown on Si. Similar to Fig. 3.1, misfit dislocations were mainly confined near the Ge/Si growth interface, and there was no threading dislocations observed in the Ge layer at 700 nm away from the interface. Although the As-doped Ge buffer was thicker, the TDD of the portion above the 1 μm Ge layer is expected to be unchanged, as threading dislocations neither generate nor terminate with the increase of epitaxial layer thickness.

Fig. 3.3 A cross-sectional TEM image of the As-doped Ge epitaxy on Si. The As-doping concentration is $\sim 10^{19} \text{ cm}^{-3}$ [116].

The TDD of the highly As-doped Ge/Si was counted from the plan-view TEM images, as shown in Fig 3.4 (a) and (b), by combining the number of dislocations at different locations across the entire samples. Only one threading dislocation is found in Fig 3.4 (a), while no threading dislocation is found in most of the images such as Fig 3.4 (b). Based on the plan-view TEM images, the estimated average value of TDD is $1.06 \pm 0.639 \times 10^7 \text{ cm}^{-2}$, which has reached the plan-view TEM inspection range to count TDD.

Fig. 3.4 Plan-view TEM images of the As-doped ($\sim 10^{19} \text{ cm}^{-3}$) Ge epitaxy on Si at two locations. One dislocation is found in (a), while no dislocation is observed in (b) [116].

To quantify the TDD with lower magnification images, scanning electron microscope (SEM) was used with the so-called defect selective etching (DSE) technique. The highly As-doped Ge/Si sample and the normally undoped Ge/Si sample were etched in iodine solution (a mixture of $\text{HF}/\text{HNO}_3/\text{CH}_3\text{COOH} = 5:10:11$ with iodine) for 1 s to reveal the threading dislocations on the Ge surface. The etch pit density (EPD) was counted under SEM to estimate the TDD. Since the dislocations are etched much faster in the etchant, the etch pit can be delineated and observed. Additionally, the previous literature has shown very good correlation between the TDD and the EPD with a 5%~10% deviation [105]. Therefore, it is a complementary method to TEM for a count of TDD lower than $1 \times 10^7 \text{ cm}^{-2}$.

The EPD value is estimated based on the average number of twenty $10 \times 10 \text{ }\mu\text{m}^2$ plan-view SEM images for each sample. The estimated EPD of the highly As-doped Ge/Si sample is $4.57 \pm 0.39 \times 10^6 \text{ cm}^{-2}$, as shown in Fig 3.5(a). The estimated EPD of the normally undoped Ge/Si sample is $5.63 \pm 0.63 \times 10^7 \text{ cm}^{-2}$. The EPD of the normally undoped Ge/Si sample agrees well with the plan-view TEM results in Fig 3.2, which indicates the consistency between these two TDD counting methods. The EPD result showed that the TDD was reduced by one order of magnitude by introducing high As-doping to the Ge seed layer.

Fig. 3.5 SEM images ($10 \times 10 \mu\text{m}^2$) of the defect selectively etched (a) As-doped Ge/Si sample and (b) the normally undoped Ge/Si sample for the count of etch-pit density (EPD) [116].

Although no completely satisfactory mechanism quantitatively explains the defect reduction in Ge/Si epitaxy using high As-doping, some possible ways can help to answer the question regarding the dislocation motion influenced by n-type doping. Previous studies on charged impurity effects on dislocation velocity in Ge show the enhancement of dislocation velocity by As-doping [113], [114]. The dislocation velocity started to increase when the doping concentration was higher than $1 \times 10^{18} \text{ cm}^{-3}$ at 500°C , where the activation energy for the diffusion of the dislocation core is reached [117]–[119]. Based on this explanation, the early introduction of As-doping in the Ge seed layer, where most of dislocations were generated, increased the dislocation velocity. Therefore, the threading dislocations moved faster to the wafer edge or annihilated each other more during gliding. The thermal cyclic annealing can also increase the probability that dislocations with opposite signs of the Burgers vector would meet more readily and annihilate each other. As a result, the TDD was reduced to a greater degree than the normally undoped Ge seed layer with a lower dislocation velocity.

Another possible hypothesis to explain the defect reduction in Ge/Si concerns the As-doping enhanced Si-Ge inter-diffusion at the growth interface. Recently, it was reported that Si-Ge inter-diffusivity was enhanced 10-20 times

when the Ge was highly doped with another n-type dopant: phosphorus (P). This is because phosphorus dopants transport much faster than Ge towards the Si side, resulting in an increase in the negatively charged vacancy concentration in the Ge seed layer. It is known that the charged defect concentration can be characterized as a function of the Fermi level [120], [121]. When the doping concentration is higher than the intrinsic carrier concentration, the Fermi level can change the defect concentration and thus the diffusivity [122]. Therefore, a strong Si-Ge inter-diffusion suggests a significant Fermi effect on defect concentration. As the Si-Ge inter-diffusion would result in an intermixing $\text{Si}_{1-x}\text{Ge}_x$ layer, the Fermi effect can be indirectly predicted from the XRD measurement in order to examine the validity of this hypothesis.

The high-resolution XRD asymmetric 2theta-omega scans of the highly As-doped Ge/Si sample and the normally undoped Ge/Si control sample are plotted in Fig 3.6. The figure shows a clear shoulder from 66.2 to 68.0 degrees between the Ge signal peak and the Si signal peak for both Ge/Si samples. To gain a better understanding of the shoulder signal peaks, the strain state of the Ge/Si samples was calculated. The XRD measurement showed that the Ge epilayer with and without the As-doped seed layer experienced a tensile strain of 0.21% and 0.16%, respectively. The 0.16% tensile strain originated from the difference in thermal expansion coefficients (CTEs) of Ge and Si, as Ge has a CTE of $5.8 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$ compared to the CTE of Si of $2.6 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$ [123]. The shift of the As-doped Ge signal peak to the right of the undoped Ge signal peak increased the tensile strain by 0.05%. In addition, the shoulder peak of the As-doped Ge/Si sample also shifted to the right, and it was a broader shoulder compared to the control sample. Combining the observations of the strain state and shoulder-shape, an enhanced intermixing As-doped $\text{Si}_{1-x}\text{Ge}_x$ layer is indicated rather than an abrupt change at the Ge/Si growth interface. The right-shift of the peak suggests the tensile strain in the Ge layer is larger than the tensile strain in the undoped control sample. The broader shoulder indicates a gradual composition change of $\text{Si}_{1-x}\text{Ge}_x$, and this also contributes to the TDD reduction in the highly As-doped Ge/Si sample.

Fig. 3.6 The high resolution XRD 2theta-omega scan the shows strain states of the Ge epitaxial films. The spectral width indicates the crystallinity of the Ge films [116].

As suggested in Chapter 2, the Ge surface roughness is also an important parameter to ensure the wafer bonding quality, and a RMS roughness lower than 0.5 nm is recommended [91]. The AFM images of the Ge/Si samples without and with the As-doped Ge seed layer are shown in Fig 3.7 (a) and (b), respectively, using the same scanning range of $5 \times 5 \mu\text{m}^2$. The undoped Ge epitaxial layer shows a relatively high RMS roughness of 0.8 nm, and clear cross-hatched patterns are seen on the Ge surface. A smooth surface is obtained in the As-doped Ge/Si sample, and the RMS roughness is reduced to 0.4 nm. The smooth surface is another indication of enhanced dislocation movement and the migration of Ge atoms caused by As-doping and post-growth annealing.

Fig. 3.7 AFM images ($5 \times 5 \mu\text{m}^2$) of (a) undoped Ge/Si and (b) As-doped Ge/Si. The RMS roughness of (a) and (b) are 0.8 nm and 0.4 nm, respectively [116].

3.3 Fabrication of Ge-on-Insulator (GOI)

3.3.1 Wafer Bonding and Layer Transfer Processes

The experiment details of Ge/Si epitaxy were described in the last section. The 8-inch Ge/Si wafers were used as the donor wafers for wafer-scale bonding. The flow of the wafer bonding procedures, as shown in Fig. 3.8, illustrates the standard processes to fabricate a GOI substrate structure. Based on this standard wafer-scale bonding procedure, four aspects to further improve the GOI quality are proposed: (1) a polishing process to remove the transferred defective region, (2) a thermal oxide thickness study to suppress thermal bubble generation, (3) a

new bonding dielectric for more efficient heat dissipation and (4) annealing conditions to reduce defects. These aspects will be discussed in the next sections.

As shown in Fig. 3.8 (a), a Ge/Si donor wafer was provided for the wafer bonding. In Fig. 3.8 (b), an 8-inch Si wafer (p-type, resistivity = 1-1000 Ω -cm) with a thermal oxide (THOX) layer on top was used as a handle wafer. Prior to bonding, both donor and handle wafers were exposed to O₂ plasma for 15 s, which could increase the surface hydrophilicity of the dielectric. After O₂ plasma exposure, both wafers were rinsed in deionized water and then spin-dried. The rinsing step cleaned the wafer surface, and populate it with a high density of hydroxyl (OH) group to initiate wafer bonding. Then the wafers were sent to the EVG-850LT bonder tool for wafer bonding at room temperature. After bonding (Fig. 3.8 (c)), the bonded wafers were annealed in N₂ at 300 °C for 3 hours to further enhance the bond strength. Then, in Fig. 3.8 (d), the Si donor wafer was removed in the tetramethylammonium hydroxide (TMAH) solution. The backside of the Si handle wafer was spin-coated by ProTEK®B3-25 to avoid the etching. The etching was carried out at 80 °C until the Si was completely removed. Due to the high etching selectivity of Ge over Si in the TMAH solution, Ge acted as an etch-stop layer. Thus, the Ge epitaxial layer was successfully transferred to a Si handle wafer forming a GOI substrate. The ProTEK®B3-25 protective coating was then removed with acetone. However, the exposed Ge layer surface of the GOI wafer was originally the interface between Ge and Si of the Ge/Si wafer, which was highly defective (TDD of $\sim 5.1 \pm 0.8 \times 10^8 \text{ cm}^{-2}$). Thus, a chemical mechanical polishing (CMP) step is needed to remove the highly defective region, as shown in Fig. 3.8 (e).

Fig. 3.8 Process flow chart for obtaining dislocation engineered GOI via (a) epitaxy, (b) plasma treatment, (c) wafer bonding and annealing, (d) grinding and etching for layer transfer and (e) surface polishing to reduce the defective region.

3.3.2 Removal of Defective Transferred Layer

As mentioned in the last section, a CMP step needs to be performed to remove the defective top region of the transferred Ge layer and smooth its surface. To compare the TDD before and after the CMP process, defective selective etching (DSE) combined with SEM inspection was used to observe the changes of TDD in Ge. In this experiment, the transferred Ge layer was undoped for simplicity, and its TDD measured from the Ge/Si wafer before bonding was $\sim 5 \times 10^7 \text{ cm}^{-2}$.

The Ge samples of as-grown-on-Si, after-layer-transfer, and after-CMP were etched in iodine solution for 1 s to reveal the etch pits. The etch pit density (EPD) was counted under SEM. The SEM images in Fig 3.9 show that the EPD increased from $3.5 \pm 0.2 \times 10^7 \text{ cm}^{-2}$ to $5.1 \pm 0.8 \times 10^8 \text{ cm}^{-2}$ after layer transfer, and the EPD almost returned to its value of as-grown on Si of $4.3 \pm 0.4 \times 10^7 \text{ cm}^{-2}$ after CMP processing. This occurred because the exposed Ge surface after layer transfer was the highly defective interface between Ge and Si of the Ge/Si wafer [86]. After employing the CMP process, the top 400 nm Ge layer with a

high TDD was removed and the EPD was reduced to a comparable value to the EPD of Ge as-grown on Si. III-V integration and Ge laser fabrication only requires a thin Ge layer (200 nm~500 nm). Therefore, the Ge layer can be further thinned down and the defective layer will not influence the GOI quality.

Fig. 3.9 SEM images of (a) as-grown on Si (b) after layer transfer and (c) after CMP. The EPD of these samples can be estimated [124].

In addition to the TDD characterization, it is also important to have a smooth surface for III-V epitaxy and Ge laser fabrication. The $5 \times 5 \mu\text{m}^2$ AFM images in Fig 3.10 (a), (b) and (c) show the RMS roughness of the Ge layer as-grown, after layer transfer and after CMP processing, respectively. Ge as-grown on Si has a low RMS roughness of 0.4 ± 0.1 nm, and some cross-hatched patterns were observed due to the non-uniform elastic strain field [125]. After chemical etching for the Si donor substrate removal, the Ge surface was roughened. The roughening resulted in the increase in RMS roughness to 1.5 ± 0.3 nm. With the assistance of the CMP process, the surface roughness was

reduced to 0.2 ± 0.1 nm. Therefore, the Ge surface roughness after the CMP process is sufficient for reliable bonding processes.

Fig. 3.10 AFM ($5 \times 5 \mu\text{m}^2$) images show the RMS surface roughness of the Ge layer (a) as-grown on Si (b) after layer transfer and (c) after CMP [124].

The strain status of the Ge layer during the bonding processes were characterized by XRD and Raman spectroscopy. A XRD reciprocal space mapping (RSM) of the CMPed GOI substrate is taken at (004) and ($\bar{2}\bar{2}\bar{4}$) diffraction planes, as shown in Fig 3.11. A tensile strain of 0.16% was estimated in the Ge layer, which was same as the tensile strain of the Ge layer (0.20%) on Si before wafer bonding. This indicated the conservation of a strain state in the Ge layer before and after low-temperature bonding processes.

Fig. 3.11 RSM of the GOI substrate taken at (004) (left) and $(\bar{2}\bar{2}4)$ (right) diffraction plane. The tensile strain of the Ge layer in GOI is 0.16% [124].

A 532 nm laser was used for the Raman spectroscopy measurement. As the penetration depth of the 532 nm laser in Ge was about 20 nm, the Raman peaks were measured from the sample surface. In Fig 3.12, a bulk Ge was used as a reference sample in the Raman spectroscopy measurement. The Ge-Ge peak in Ge/Si (299.6 cm^{-1}) and CMPed GOI (299.9 cm^{-1}) samples shifted towards a lower wavenumber compared to the Ge-Ge peak (300.8 cm^{-1}) in bulk Ge, which indicated the presence of tensile strain [18]. According to the Ge-Ge peak shift, the calculation showed that the tensile strains in Ge/Si and CMPed GOI were 0.28% and 0.21%, respectively, which agreed with the XRD measurement. In addition, the Ge-Ge peak of GOI after the layer transfer appears to be asymmetric in shape. As mentioned, the exposed Ge layer surface after the layer transfer was the interface of Ge/Si. A Ge-Si inter-diffusion layer was expected to form at the interface due to the high thermal budget [116]. Therefore, the asymmetric shape tailing towards the lower wavenumber was induced by the alloy disorder [126]. Furthermore, the appearance of Si-Ge peaks at $380\sim 400\text{ cm}^{-1}$ confirmed the existence of a Si-Ge inter-diffusion layer.

Fig. 3.12 Raman spectra of the Ge/Si, GOI after layer transfer and after CMP and Ge (001) bulk substrates. The Ge-Ge peaks of Ge/Si and the GOI substrate shift toward lower wavenumbers compared to the Ge bulk substrate. Using the Raman shift results, the tensile strain of the Ge layer in Ge/Si and GOI after CMP is calculated to be 0.28% and 0.21%, respectively [124].

3.3.3 Thermal Bubble Suppression

After surface polishing, the defective region of the Ge layer was removed and the rough surface was smoothed for the subsequent processes of III-V epitaxy or Ge laser fabrication on a GOI substrate. During III-V epitaxy and CMOS integration, the growth and processing temperature can vary from 600 –725 °C. Therefore, it is essential to ensure that the GOI substrate is compatible with these high-temperature processes. It was previously reported that thermal bubbles were formed at the bonding interface when the bonded wafer was treated in a wide temperature range between 200 °C–800 °C [94], [95]. These thermal bubbles are commonly induced by the generated by-products (mainly H₂) at high temperatures. Only a small portion of the bonding by-products can be removed from the bonding interface via lateral diffusion towards the wafer edges. The rest are trapped at the bonding interface [90], [93]. Since the main

species in the thermal bubbles is H_2 , the thermal bubbles can dissolve in oxide, which makes the thermal oxide (THOX) layer in the GOI structure a promising candidate to resolve the thermal bubbles issue.

In order to suppress the formation of thermal bubbles, the H_2 gas needs to be fully absorbed by the THOX layer [127]. As H_2 solubility in oxide decreases with increasing temperature, a thicker THOX layer is required for higher temperature treatment. In the study of the absorption of H_2 in oxide, the THOX layer thickness varied from 40–1000 nm. A Nomarski optical microscope was used to inspect the formation of new thermal bubbles with different THOX thicknesses. The bonding strength was examined after post-bonding annealing by the crack opening method.

Fig. 3.13 shows the plan-view Nomarski images of the 8-inch GOI wafers with a 40 nm, 200 nm and 1000 nm THOX layer after four hours of annealing at 750 °C in N_2 ambient. Fig. 3.13 (a) shows that the GOI wafer with a 40 nm THOX has a large density of thermal bubbles and blistering ($1.5 \times 10^6 \text{ cm}^{-2}$). The GOI wafer with a 200 nm oxide layer effectively reduces the density of thermal bubbles to a moderate level ($2.0 \times 10^3 \text{ cm}^{-2}$), as shown in Fig 3.13(b). In Fig 3.13(c), the GOI surface becomes bubble-free when the THOX increases to 1000 nm thick. Based on these observations, there is an exponential decrease in the number of thermal bubbles with an increasing THOX thickness. From the perspective of device performance, the THOX layer should be as thin as possible due to its poor thermal conductivity. Therefore, a 200 nm THOX layer has been proved to suppress thermal bubble formation effectively, which can be used in the GOI structure.

Fig. 3.13 Nomarski images of 8-inch GOI wafers with a thermal oxide (THOX) layer thickness of (a) 40 nm, (b) 200 nm, and (c) 1000 nm. All of these GOI wafers have been annealed for 4 hours at 750 °C in N₂ ambient [124].

Bonding strength analysis was also conducted on the 8-inch GOI wafer with a 200 nm THOX layer after thermal treatment. The bonding strength is another important parameter to GOI, as the bonded wafer needs to withstand grinding and film thinning during the layer transfer process. Thus, a large bonding strength is a necessity to prevent film delamination [128]. As mentioned in the bonding process flow in Fig 3.8, the bonding strength can be enhanced by a post-bonding annealing. The bonding strength enhancement was due to the formation of covalent bonds during post bonding annealing. At a relatively high annealing temperature, polymerization between –OH groups occurs across the bonding interface, which can be expressed as:

Here, M denotes the semiconductors. The water molecules are released and M-O-M bonds are formed, which leads to a high bonding strength.

As mentioned in Chapter 2, a crack opening model can be used to calculate the bonding strength. The bonding strength, γ , can be calculated through substituting the value of crack length L into Eq. (3.2) [89]:

$$\gamma = \frac{3Ed^3t^2}{8L^4} , \quad (3.2)$$

where E is the elastic modulus, y is the thickness of the razor blade, t is the thickness of a single wafer, and L is the measured crack length along the bonding interface.. The measured crack length is 23.6 mm. Thus, the bonding strength is estimated to be 1720.6 mJ/m², which is expected to be sufficient for GOI to sustain mechanical processes [129].

The bonding quality of GOI with a 200 nm THOX after 300 °C post-bonding annealing was examined by IR imaging for the inspection of bonding defects. Compared to the IR image in Fig 3.14 (a) of before post-bonding annealing, Fig 3.14 (b) shows that there is no new void formation or void enlargement after the annealing. However, some dark spots, voids, or interferential lines are observed on the surface. They were caused by particle contaminations on the two mating surfaces during wafer bonding, which can be resolved with a better cleaning process and better control of wafer handling processes.

Fig. 3.14 IR images of Ge/Si bonding to 200 nm thermal oxide on Si before (a) and after (b) post bonding annealing. Some de-bonded areas were caused by particle contaminations [124].

3.3.4 Thermal Conductivity Improvement

Efficient heat dissipation is important to most photonic devices. For III-V photonics, overheating causes optical output saturation at high electrical pumping [43]. In Ge gain materials, high temperature increases the intervalence band absorption (IVBA), which reduces the net gain [17]. Ge lasers especially require a high pumping power due to indirect band properties generating a large amount of heat. Therefore, thermal conductivity is essential to ensure lasing behaviour in Ge lasers.

In order to increase the heat dissipation of the GOI wafer, a thin aluminium oxide (Al_2O_3) bonding oxide layer was developed to replace the SiO_2 thermal oxide (THOX). The thermal conductivity of Al_2O_3 is about ~20 times higher than that of SiO_2 ($30 \text{ Wm}^{-1}\text{k}^{-1}$ vs. $1.4 \text{ Wm}^{-1}\text{k}^{-1}$). Thus, it is expected to provide better thermal management in the GOI structure. Fig. 3.15 shows the simulations of the thermal conductivity in the wafer structures of Ge/THOX/Si and Ge/ Al_2O_3 /Si. The simulated stack consists of $1 \mu\text{m}$ Ge, 200 nm insulator layer and $10 \mu\text{m}$ Si. Here, the thickness of insulator layer was set to the optimized value at 200 nm. When a heat flux of $1 \times 10^8 \text{ W/m}^2$ is applied, the surface temperature of Ge/THOX/Si increases by 20.5 K to 318.5K, while the temperature increment of Ge/ Al_2O_3 /Si is 8.1K. This finding shows a

significant improvement in the heat dissipation capability by replacing thermal oxide with Al_2O_3 .

Fig. 3.15 COMSOL simulation on the temperature distribution of (a) Ge/THOX/Si and (c) Ge/ Al_2O_3 /Si stack structures. Their cross-sectional temperature profiles are shown in (b) and (d), respectively.

Based on the simulation results, Al_2O_3 is more efficient for heat dissipation than SiO_2 . The integration of the Al_2O_3 bonding oxide into the wafer bonding processes is shown in Fig. 3.16. Once the Ge/Si donor wafer was ready for bonding, a 10 nm thin Al_2O_3 layer was deposited using atomic layer deposition (ALD) on both the donor wafer and another Si (100) handle wafer. After room temperature bonding, the Si donor wafer was removed to form a Ge/ Al_2O_3 /Si structure. The rest of the bonding processes were similar to the standard wafer bonding processes in Fig. 3.8.

Fig. 3.16 Schematic flow of the fabrication of the GOI substrate with Al₂O₃ bonding dielectric [34].

The cross-sectional TEM images in Fig 3.17 (a) shows the bonding interface of the two Al₂O₃ layers between the donor wafer and the handle wafer. The Ge epitaxial layer thickness and the Al₂O₃ bonding dielectric thickness were 1.3 μm and 20 nm, respectively. As shown in Fig 3.17 (b), the two Al₂O₃ layers from each wafer are bonded uniformly with no sign of defects, such as micro-voids or delamination. The difference in contrast within the Al₂O₃ layer is likely attributed to the O₂ plasma activation, which modifies the stoichiometry of the Al₂O₃. These observations confirm that a seamless bond at the micro-scale has been achieved successfully using Al₂O₃ as a highly thermal-conductive bonding oxide.

Fig. 3.17 Cross-sectional TEM images of (a) the GOI substrate with multiple Al_2O_3 layers, and (b) the magnified bonding interface of the Al_2O_3 layers [34].

3.3.5 Defect Reduction by Annealing

The TEM image in Fig. 3.17 shows a very defective Ge layer after bonding and layer transfer processes. As mentioned in Section 3.3.2, the removal of the defective region by CMP can reduce the TDD in the Ge layer. However, for specific applications, such as a Ge photodetector, a thick Ge layer ($\sim 2 \mu\text{m}$) is required for higher quantum efficiency [130]. Thus, an alternative approach to reduce the TDD while maintaining a relatively thick Ge layer is desired.

In this study, oxygen (O_2) annealing was introduced to reduce the TDD without significantly reducing the Ge layer thickness. O_2 annealing is chosen because it serves two purposes: (1) oxidation of the Ge seed layer at the Si-Ge interface to remove the misfit dislocations and (2) removal of the threading dislocations once the misfit dislocations are eliminated. This annealing step was employed after the wafer bonding. The bonded GOI substrate was subjected to annealing at 850°C in an O_2 environment for four (4) hours. After that, the sample was etched in a HF solution (49% HF: $\text{H}_2\text{O} = 1:20$, by volume) for 30 seconds to remove the oxidised Ge layer. In order to examine the O_2 annealing impacts on the material quality of GOI, cross-sectional TEM inspections were performed on the GOI wafer before and after O_2 annealing. The GOI sample with thin Al_2O_3 layers was used in this experiment as the defects are clearly observed in the TEM image in Fig. 3.17 (a).

As shown in Fig 3.18 (a), the top portion of the Ge epitaxial layer is full of misfit and threading dislocations after wafer bonding. After the O₂ annealing, most of the misfit dislocations were oxidized, and the oxidized Ge seed layer on the surface was removed by chemical etching. As shown in Fig 3.18 (b), there is no sign of misfit dislocations, and the thickness of Ge film is also reduced by ~250 nm after O₂ annealing. Since the misfit dislocations are consumed during oxidation, the threading dislocations are not necessarily to form a loop. Thus, the remaining threading dislocations are able to move under thermal treatment, and the annihilation of the threading dislocations can occur. This hypothesis is likely to explain the obvious reduction in threading dislocations, as shown in Fig. 3.18 (b). Another possibility is that oxygen is more preferably oxidized the Si in Si-Ge inter-diffusion layer causing the piling-up of Ge, and further oxidized Ge is more volatile at annealing temperature, which may also contribute to the reduction in TDD after O₂ annealing.

Fig. 3.18 Cross-sectional TEM images showing the GOI substrate (a) before and (b) after O₂ annealing. [37]

The TDD values of the GOI wafer before and after O₂ annealing were quantitatively estimated by plan-view TEM and SEM inspections. The TEM images in Fig 3.19 (a) and (b) show the TDD of the GOI wafer before and after O₂ annealing is $7.7 \pm 0.6 \times 10^8 \text{ cm}^{-2}$ and $6.4 \pm 0.5 \times 10^7 \text{ cm}^{-2}$, respectively. The defect selective etching (DSE) SEM images in Fig 3.19 (c) and (d) show that the EPD of the GOI wafer before and after O₂ annealing is $5.2 \pm 0.5 \times 10^8 \text{ cm}^{-2}$ and $2.5 \pm 0.4 \times 10^7 \text{ cm}^{-2}$, which is consistent with the TEM results. This confirms the materials quality improvement of the GOI wafer after O₂ annealing. Additionally, the etch pits have a square shape because the circular pits are located on the cross-hatched lines, which are often oriented along the two orthogonal $\langle 110 \rangle$ directions [131].

Fig. 3.19 Plan-view TEM images showing the threading dislocations on the GOI surface (a) before and (b) after O₂ annealing. The EPD determination for (c) before annealing and (d) after O₂ annealing [37].

The oxidation reaction at the Si/Ge interface (Ge seed layer and Si-Ge intermixing layer) also contributes to the defect reduction. The Raman spectroscopy measurement in Fig. 3.20 shows that the Si-Ge vibration mode disappears after O₂ annealing compared to the Raman spectrum of the GOI without O₂ annealing. In addition, the Ge peak shifts to a higher wavenumber overlapping with the bulk Ge peak after annealing (inset image), which indicates a fully relaxed Ge layer. All these observations indicate that an oxide layer at the Si/Ge interface, which may have contributed to the reduction of misfit dislocations, and therefore, resulted in a decrease in TDD after O₂ annealing.

Fig. 3.20 Raman spectroscopy spectra of the Ge epilayers on GOI before and after annealing with reference to bulk Ge, and the inset of the Ge-Ge vibration peak [37].

3.4 Summary

In summary, the highly As-doped Ge seed layer reduced the TDD and RMS roughness of the Ge/Si substrate to $\sim 5 \times 10^6 \text{ cm}^{-2}$ and 0.37 nm, respectively. The low TDD value of the highly As-doped Ge/Si substrate would enable the III-V photonics integration and Ge-based photonics, and the RMS roughness has met the criteria for reliable wafer bonding processes. The As-doping in the Ge seed layer was expected to enhance the diffusion of dislocations, which is possibly due to the increased dislocation velocity or the Fermi level effect. The Fermi level effect was indirectly predicted through the XRD measurement of the enhanced $\text{Si}_{1-x}\text{Ge}_x$ inter-diffusion. As a result, the n-type As-doping contributes to the defect reduction and surface morphology improvement. The improvement of the Ge/Si epitaxy quality can contribute to the future development of a high-quality GOI substrate.

Following the epitaxy, a wafer-scale bonding process for an 8-inch GOI substrate was successfully demonstrated. During the bonding and layer transfer processes, the TDD and RMS of the transferred Ge layer on insulator increased.

By employing a CMP step, the TDD was reduced from 5×10^8 to $\sim 4 \times 10^7 \text{ cm}^{-2}$ and a low RMS roughness ($0.2 \pm 0.1 \text{ nm}$) was achieved. These results are comparable to the Ge layer quality as-grown on Si. In order to further improve the GOI quality in terms of thermal bubble formation, heat dissipation and defect reduction, several wafer bonding techniques were developed. First, the THOX thickness was optimised. A 200 nm THOX obtained a moderate thermal bubble density of $2.0 \times 10^3 \text{ cm}^{-2}$. The quality was sufficient to ensure a reliable subsequent material growth. Second, a thin Al_2O_3 layer was developed to replace the THOX to increase the thermal conductivity for practical device applications. The COMSOL model showed that the temperature of the Ge layer using 200 nm Al_2O_3 bonding oxide was 8.1 K lower than that using 200 nm THOX under the same flux power density of $1 \times 10^8 \text{ W/cm}^2$. The integration of this newly proposed Al_2O_3 bonding oxide into the existing wafer bonding processes was achieved. At last, the GOI was annealed at 850°C in an O_2 environment to reduce the TDD without reducing the transferred Ge layer significantly ($\sim 250 \text{ nm}$). After O_2 annealing, the TDD was reduced by one order of magnitude due to the removal of misfit dislocations by oxidizing the Ge surface (Ge seed layer) and the annihilation of the threading dislocations by removing the dislocation loop. By combining these developed techniques in epitaxy and wafer bonding, a high-quality GOI substrate can be obtained with a low TDD, low surface roughness, high bonding strength and thermal-bubble-free surface. These improvements in GOI quality make it a promising candidate for III-V integration and Ge photonics. The applications based on the high-quality GOI substrate will be investigated in Chapters 4 and 5.

Chapter 4: Ge-on-Insulator for Lasing

4.1 Introduction

The integration of efficient, miniaturized group IV lasers into CMOS architecture holds the key to the realization of fully functional photonic-integrated circuits [132], [133]. Unlike silicon (Si), the energy difference between the direct Γ and indirect L conduction valleys of Ge is only ~ 140 meV. Therefore, it is possible to force some electrons to populate the direct Γ conduction valley and to create a population inversion in Ge [134]. As mentioned in Chapter 1, three main bandgap engineering techniques are used to increase the net gain in indirect band Ge material: (1) n-type doping [16], (2) Sn incorporation [17] and (3) strain engineering [18]. Despite several years of progress, however, all the Ge-based group IV lasers reported to date exhibit impractically high thresholds owing to their unfavourable band structures [20], [135]–[137].

Among these mentioned bandgap techniques, the highly strained germanium with its fundamentally altered band structure has emerged as a potential low-threshold gain medium [26], [48], [138]–[142]. The small energy difference between the Γ and L conduction valleys can be reduced even further with tensile strain: resulting in increased material gain [141], [142]. This hypothesis has been supported by numerous theoretical simulations that predict a significant reduction in the lasing threshold through tensile strain [143], [144]. Regarding practical realization, several innovative platforms for inducing large mechanical strain have been demonstrated experimentally [26], [48], [138], [140], thus suggesting the possibility of low-threshold group IV lasers. However, there has not been any successful demonstration of lasing from this seemingly promising material system mainly due to the material quality, inadequate strain value, non-uniform strain distribution and intrinsic losses from carrier absorption [134], [144]–[146].

In this chapter, a highly strained Ge nanowire laser is demonstrated using a previously developed Ge-on-insulator (GOI) substrate. Based on the finite-element method (FEM) and finite difference time domain (FDTD) simulations, the laser cavity is designed to have a highly uniform uniaxial tensile strain

(>1%) with high-quality (high-Q) factor. Particularly, the laser structure is lying on the bonding dioxide (SiO_2), which provides an extra path for thermal conduction while confining optical fields within the Ge layer. Based on the simulation, the laser cavity is designed and a uniformly distributed high strain up 4.6% can be achieved. In a 1.6% uniaxial tensile strained Ge nanowire laser, an unambiguous multimode lasing action is observed, which is evidenced by nonlinear threshold behaviour in output power and linewidth narrowing as a function of pump power as the optical losses are compensated by the amplified material gain with an optical pumping threshold density of $\sim 3.0 \text{ kW cm}^{-2}$.

4.2 Simulation

4.2.1 Strain on Band Structure

As briefly discussed in Chapter 1, the strain effect on the band structure of Ge. The indirect and direct conduction band valleys shrink with increasing tensile strain, while valence band degeneracy occurs (heavy-hole and light-hole valence bands). As the direct Γ valley shrinks faster than the indirect X and L valleys, the indirect Ge will transit to direct bandgap materials under a large mechanical tensile strain. The simulation and experimental results show that direct band-gap Ge material requires applying a biaxial tensile strain of 1.7%~1.9% [22] or a uniaxial strain of 4.6% [18]. Since this chapter is focused on the uniaxial tensile strained Ge nanowire structure, the modelling of the uniaxial strain effect on the Ge band structure is reviewed.

In the simulation, the in-plane strains in the x (ϵ_{xx}) and y (ϵ_{yy}) directions and the out-of-plane strain in the z direction (ϵ_{zz}) perpendicular to the nanowire surface are the main variables, which can be expressed by the following matrix:

$$\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{S_{44}}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{S_{44}}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{S_{44}}{2} \end{bmatrix} \begin{bmatrix} \sigma \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

and

$$\varepsilon_{xx} = S_{11}\sigma, \varepsilon_{yy} = S_{12}\sigma, \varepsilon_{zz} = S_{12}\sigma \quad (4.1)$$

The uniaxial strains, ε_{100} , are the main variables in the model and $\varepsilon_{100} = \varepsilon_{xx}$. Then, ε_{yy} and ε_{zz} can be expressed by Eq. (4.2) [147]:

$$\varepsilon_{yy} = \varepsilon_{zz} = \frac{S_{12}}{S_{11}} \varepsilon_{100}, \quad (4.2)$$

where S_{11} and S_{12} are the coefficients of the mechanical compliance matrix for germanium. Then the strain effect on the bandgap energies of Γ and L can be modelled by Eqs. (4.3)–(4.7) [147]:

$$E_g^\Gamma(LH) = E_g^\Gamma(0) + aTr(\varepsilon) + \frac{\Delta_0}{2} - \frac{1}{4}\delta E_{001} - \frac{1}{2}\sqrt{\Delta_0^2 + \Delta_0\delta E_{001} + \frac{9}{4}(\delta E_{001})^2}, \quad (4.3)$$

$$E_g^\Gamma(HH) = E_g^\Gamma(0) + aTr(\varepsilon) + \frac{1}{2}\delta E_{001}, \quad (4.4)$$

$$E_g^L(LH) = E_g^L(0) + (\Xi_d + \frac{1}{3}\Xi_u - a_v)Tr(\varepsilon) + \frac{\Delta_0}{2} - \frac{1}{4}\delta E_{001} - \frac{1}{2}\sqrt{\Delta_0^2 + \Delta_0\delta E_{001} + \frac{9}{4}(\delta E_{001})^2}, \quad (4.5)$$

$$E_g^L(HH) = E_g^L(0) + (\Xi_d + \frac{1}{3}\Xi_u - a_v)Tr(\varepsilon) + \frac{1}{2}\delta E_{001}, \quad (4.6)$$

$$Tr(\varepsilon) = (1 + 2\frac{S_{12}}{S_{11}})\varepsilon_{100}, \delta E_{001} = 2b(\varepsilon_{100} - \varepsilon_{010}) = 2b(1 - \frac{S_{12}}{S_{11}})\varepsilon_{100}, \quad (4.7)$$

where a , a_v , Ξ_d, Ξ_u and b are the deformation potentials and Δ_0 is the spin-orbit splitting energy. In the above equations, $a = a_{c,dir} - a_v$ for direct band transitions, where $a_{c,dir}$ is the conduction band deformation potential of the Γ valley and

$\Xi_d + 1/3\Xi_u - a_v$ for indirect band transitions. Table 4.1 provides the deformation potential constants for elastic compliance contents and spin-orbit splitting energy to simulate the strain effects [148]. The changes of direct and indirect band transition energies with uniaxial strain are modelled in Fig. 4.1.

Table 4. 1 Deformation potential constants, elastic compliance constants and spin-orbit splitting energy for Ge.

	S_{11} (Pa)	S_{12} (Pa)	$a_{c,dir}$ (eV)	a_v (eV)	$\Xi_d + 1/3\Xi_u -$ a_v (eV)	Δ_0 (eV)	b (eV)
Ge	9.69×10^{-12}	-2.65×10^{-12}	- 8.24	1.24	-2.78	0.3	-1.88

Fig. 4. 1 Bandgap energy vs. uniaxial tensile strain in Ge.

4.2.2 Doping Effect

A simple expression of BGN in n-type doped semiconductors has been developed by S. C. Jain et al. [149] without taking account of the thermal effects on the intervalley scattering transitions [150]. Therefore, this model is generally valid for BGN effects at low temperature. The model of BGN energy, ΔE_g , includes the exchange energies, correlation energies and the impurity interaction energies. The sum of these terms can be expressed in a simplified equation:

$$\frac{\Delta E_g}{R} = \frac{1.83}{r_s N_b^{1/3}} + \frac{0.95}{r_s^{3/4}} + \frac{\pi}{2} \frac{1}{r_s^{3/4} N_b} \left(1 + \frac{m_{\min}^*}{m_{\max}^*}\right), \quad (4.8)$$

where R is the effective Rydberg energy, r_s is the many-body parameter and N_b is the number of equivalent valleys in the conduction band. For an n-type doped semiconductor, $m_{\min}^*$ is for hole mass and $m_{\max}^*$ is for electron mass. In the equation, both R and r_s are dependent on the density of states (DOS) mass of electrons, and r_s is also a function of doping concentration.

The Fermi-Dirac distribution function, $f(E_c)$, describes the probability of electron population in the transition between two energy states. The quasi-Fermi level, E_{fc} , is used to represent the electron population in thermal equilibrium. The doping-related quasi-Fermi energy is derived from the expression shown in Eq. (4.9):

$$n = N_c \exp\left(\frac{E_c - E_{fc}}{kT}\right), \quad (4.9)$$

where N_c is the effective conduction band DOS, E_c is the conduction band edge and kT is the thermal energy. The changes of E_{fc} as a function of doping concentration at room temperature are shown in Fig. 4.2.

Fig. 4. 2 Bandgap narrowing (Fermi level) with doping.

4.2.3 Temperature Dependent Bandgap

Besides the strain and doping impact on the bandgap, the bandgap also depends on the temperature. The bandgap energy increases with a decrease in temperature. The temperature-dependence relation can be described by Varshni's empirical expression as shown in Eq. (4.10) [151]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad (4.10)$$

where $E_g(0)$ is the bandgap energy at 0 K and α and β are material constants. The parameter values used to estimate the temperature dependent bandgap are provided in Table 4.2.

Table 4. 2 Material constants for temperature dependent bandgap of Ge.

	$E_g(0)$ (eV)	α (eV/K)	β (K)
Ge,indir	0.7412	4.561×10^{-4}	210
Ge,dir	0.8893	6.842×10^{-4}	398

4.2.4 Structure Dependent Strain

In the design of a Ge nanowire laser cavity, the strain in the nanowire is amplified through the relaxation of the Ge stressing pads in the cavity [152]. Distributed Bragg reflector (DBR) mirrors are integrated on the stressing pads to provide optical feedback to the gain medium. For simplicity reasons, the nanowire with only stressing pads was used in the structure dependent strain distribution simulation. Fig. 4.3 (a) shows a schematic structure of the nanowire with stressing pads. By using a 2D finite element method (FEM) on COMSOL software, the strain distribution can be simulated, as shown in Fig. 4.3 (b). The FEM simulation shows a highly uniform strain within the entire gain medium for a homogeneous gain medium. The stressing pad length, L_2 , is highlighted in white colour, and it is used to adjust the level of strain. By having multiple structures with different L on a single chip, one can achieve a number of lasers operating at different spectral ranges without complicated material growth such as for compound semiconductor lasers. The strain level of the nanowire determines the operating wavelengths of the lasers.

Fig. 4. 3 (a) A schematic structure of a highly strain Ge nanowire with the stressing pads, and (b) the FEM simulation showing a uniform strain distribution in the Ge nanowire.

4.2.5 Design of Mirror, Reflectivity

As shown in Fig. 4.4 (a), for the laser cavity design, an 8 μm long, 700 nm wide Ge nanowire was surrounded by two pads containing DBR mirrors. The mirrors were 10-period DBR mirrors with a period width of 379 nm. The first air trench is 65 nm, and the rest of air trenches are 189 nm wide. The trenches follow circular arcs with an optimized curvature radius for a high quality factor based on Eqs. (4.11)-(4.12). The optimization of the mirror design was carried out by Yongduck Jung at Inha University. The reflectivity in Fig. 4.4 (b) is the ideal reflectivity assuming no absorption and no scattering losses.

$$h_H = (\lambda_0 / 4) / (n_H \cos \theta_H) , \quad (4.11)$$

$$h_L = (\lambda_0 / 4) / (n_L \cos \theta_L) , \quad (4.12)$$

where h_H and h_L are the thickness of the high-index (Ge) and low-index (air) materials, respectively. λ is the light emission wavelength, n is the reflective index, and θ is the incident angle of light, which is 0 degree in this cavity design. The various cavity parameters including the active region length L_a , the passive section length L_p , the mirror length L_g and the cavity length L_{DBR} are schematically illustrated in Fig. 4.4 (c).

Fig. 4. 4 (a)Schematic of DBR mirror design, (b) simulation of reflectivity and (c) laser schematic (cross-section) illustrating various lengths.

4.2.6 Thermal Conductivity

COMSOL multi-physic simulation is also performed to compare the heat conduction in the stuck (lying on SiO_2) and suspended structures, as shown in Fig. 4.5. The stacking layer structure is 220 nm Ge/ $1\ \mu\text{m}$ SiO_2 (air)/ $50\ \mu\text{m}$ Si in the simulation. The structure centre is subjected to a $7\ \text{kW cm}^{-2}$, $7.5\ \mu\text{m}$ radium circular heat flux at 83 K, which are similar to the experimental conditions. The simulation results show that the temperature at the centre of the suspended structure increases to 160 K when subjected to the heat flux, while the

temperature only increases to 100 K owing in the stuck structure. The better heat conduction in the stuck structure is due to the SiO₂ layer as a more efficient heat conducting path compared to the air.

Fig. 4. 5 COMSOL multi-physics simulations of temperature distribution of (a) stuck (lying on SiO₂) structure and (b) suspended [100].

4.3 Experimental Procedures

The details of the epitaxy of the Ge/Si wafer and the wafer bonding processes for a GOI structure were provided in Chapter 3. The Ge nanowire laser structure was fabricated on a GOI substrate. The GOI substrate was made via epitaxy and wafer bonding, where the details of the Ge/Si epitaxy and GOI bonding processes were provided in Chapter 3. The Ge/Si wafer was grown using a three-step growth mode with a highly arsenic (As)-doped Ge seed layer to reduce the TDD. The Ge layer thickness was $\sim 2.2 \mu\text{m}$, and the top 900 nm Ge layer was uniformly phosphorus or (P)-doped to $\sim 6 \times 10^{18} \text{ cm}^{-3}$. After removing the 100 nm Ge layer by chemical mechanical polishing (CMP) for a smooth bonding surface, a 50 nm Al₂O₃ sacrificial layer was deposited on top by atomic layer deposition (ALD). This Al₂O₃ sacrificial layer was selectively

etched away during the Ge laser fabrication, rather than keeping it as a high thermal conductivity layer (see Chapter 3). Then, the Ge/Si with a thin Al_2O_3 was bonded to an 8-inch Si (100) handle wafer with a 1 μm thick thermal oxide (SiO_2) layer followed by post-bonding annealing and the removal of the Si donor substrate. Lastly, the Ge layer was transferred to the handle wafer and thinned down to the desired thickness of 220 nm, forming a GOI substrate structure for subsequent Ge laser device fabrication.

$1 \times 1 \text{ cm}^2$ pieces were diced from the 8-inch GOI wafer for device fabrication. A small biaxial tensile strain existed in the GOI sample due to the thermal mismatch between Ge and Si, as indicated with red arrows in Fig. 4.6 (a). The nanowire laser structure was defined by the e-beam lithography (EBL), and its pattern was transferred to the Ge layer by reactive etching (RIE) using Cl_2 gas. The dry etch stopped at the Al_2O_3 layer, and the sample was wet etched in 30% KOH solvent to selectively remove the sacrificial Al_2O_3 layer, forming an undercut structure. The releasing process would cause the strain redistribution and amplify the tensile strain in the nanowire [26], [138], [152]. As shown in Fig. 4.6 (b), the patterned Ge nanowire laser cavity consists of a gradually strained micro-bridge nanowire active region and two diffractive Bragg reflector (DBR) mirrors on each side. The high tensile strain along the [100] direction of the nanowire was employed via the relaxation of the stress pads, as indicated by the red arrows. Then the sample was dimmed in 100% IPA. By drying the sample on a hotplate, the whole nanowire structure was allowed to be in contact with the thermal oxide layer due to capillary force and van der Waals forces. The underlying thermal oxide layer provides the optical confinement and additional heat conduction path for the Ge nanowires, as shown in Fig. 4.6 (c).

Fig. 4. 6 (a) Bulk Ge on insulator with a small biaxial tensile strain due to thermal mismatch, (b) nanowire pattern transferred to Ge layer and (c) undercut nanowire with a high tensile strain along the [100] direction.

The dopant concentration and distribution were determined by SIMS. A concentration profiling with a scanning depth of 600 nm was performed; thus providing the elementary information of the Ge layer as well as the insulator layers (Al₂O₃ and SiO₂). Fig 4.7 shows the elemental concentration as a function of depth. Clear interfaces are observed between Ge, Al₂O₃ and SiO₂. The Ge layer has a phosphorous (P) doping concentration of $6 \times 10^{18} \text{ cm}^{-3}$ in a box-like distribution.

Fig. 4. 7 The doping profile of n-type doped GOI measured by SIMS.

The strain level in the nanowire and the strain distribution pattern within the laser cavity is determined using Raman spectroscopy mapping. The Raman measurement was performed using a 532 nm excitation source, a 100× objective lens featuring a numerical aperture (NA) of 0.9 (corresponding to a spot diameter of 721 nm) and a fibre coupled grating spectrometer (1600 lines/mm). The estimated sampling depth is ~20 nm. During the measurement, the input power was optimized to minimize the thermal induced Raman shift. The piezo stage step size was set to 200 nm during the mapping. Strain estimation was based on the strain-shift coefficient $b=152 \text{ cm}^{-1}$ for [100] uniaxial strained Ge nanowire.

The PL measurements were performed by Daeik Kim, Chibuzo Onwukaeme at Inha University. The strained nanowire along the [100] direction is photo-excited by a 1064 nm pulsed laser, and the stimulated emission is collected at a DBR through a 50× objective lens, as shown in Fig. 4.8. The pulse duration and repetition period were 20 ns and 100 ns, respectively, to minimize heating. The spot size was ~15 μm with a perfect Gaussian distribution limited by $1/e^2$: thus covering the whole nanowire uniformly. The scatter emission from the mirror was collected from the DBR

through the objective lens to a spectrometer. An InGaAs 1D-array detector with the cut-off at $1.7\ \mu\text{m}$ was used to investigate the optical properties.

Fig. 4. 8 Schematics of a cavity showing light excitation and collection points.

4.4 Result and Discussion

4.4.1 Strain Measurement

The cross-sectional TEM image in Fig. 4.9 (a) shows a GOI stacking layer structure used for the Ge nanowire laser fabrication. The stacking layer structure is 220 nm Ge/50 nm Al₂O₃/1000 nm SiO₂/Si. The nanowire was a pattern in the top Ge layer, and it formed an undercut Ge nanowire by selectively etching away the thin Al₂O₃ sacrificial layer. The strain amplification method first introduced in [153]. The SEM image in Fig. 4.9 (b) shows the geometrical parameters: $L1$ (nanowire length), $W1$ (nanowire width), $L2$ (pad length), $W2$ (pad width) and defines the laser cavity structure. By varying the geometrical parameters, different strain values can be induced in the nanowire active region.

Fig. 4. 9 (a) Cross-sectional TEM of GOI and (b) plan-view SEM of fabricated nanowire cavity.

Fig 4.10 shows the SEM image of a strained Ge nanowire and its corresponding strain distribution by Raman spectroscopy mapping and optical field distribution by FDTD simulation. The contour of an SEM image is superimposed onto the strain map and optical field as a guide to the eye. As shown in Fig. 4.10 (b), a high tensile strain of 1.6% is uniformly distributed along the [100] direction over the nanowire active region measured by Raman spectroscopy mapping. The strain distribution profile agrees well with the results from the FEM simulation in Fig. 4.3 (b), which indicates a good reliability of the model. The calculated optical field in Fig. 4.10 (c) is confined to the nanowire gain medium, enabling the spatial overlap of optical field with the strain fields. The optical confinement factor is assumed to be 0.45. The FDTD optical simulation was carried out by Yongduck Jung at Inha University.

Fig. 4. 10 (a) SEM, (b) strain distribution from Raman mapping and (c) FDTD simulated optical field distribution of a strained nanowire.

Fig. 4.11 shows room-temperature PL spectra of Ge nanowire samples (without cavity integration) with different strain status under the same pumping condition. An extended InGaAs photodetector with the cut-off at $2.1\ \mu\text{m}$ is used to access the longer wavelength. A broad spontaneous peak is observed from each sample originating from the overlapped emission peaks related to the band transitions of Γ to VB1 and Γ to VB2 [138]. The dominant PL emission peak (red solid lines) shifted from $0.792\ \text{eV}$ at 0.4% strain to $0.714\ \text{eV}$ at 2.3% tensile strain, while the integrated PL intensity increases by more than 5 times at 2.3% compared to that has a low strain. This indicates the enhancement of radiative recombination in a highly tensile strained Ge.

Fig. 4. 11 Room-temperature PL emission from 0.4%, 1.9%, and 2.3% strained Ge nanowire (without cavity integration). The solid and dashed lines are the fitted PL peaks.

4.4.2 Power Dependent Emission

This section is focused on the study of the progression of lasing behaviour with increasing excitation pump power in a 1.6% strained Ge nanowire laser (nanowire length = 8 μm) at 83 K. High-temperature operation increases the carrier absorption losses in the Ge gain medium, which reduces the net gain [17]. Therefore, a net gain is easier to be achieved at low temperature due to the reduced absorption losses. Additionally, the strain in the Ge nanowire changed less than 0.01% when the temperature was reduced from room temperature to 83 K, which can be neglected in this study.

Fig. 4.12 shows the PL emission spectra from the 1.6% strained Ge nanowire laser. At the lowest pump power of 0.7 kW cm^{-2} , the strained structure shows a featureless broad spontaneous emission. The broad spontaneous emission is arisen from the two overlapped peaks of Γ -VB1 and Γ -VB2 optical transitions. On increasing the pump power to 1.4 kW cm^{-2} , periodic modulations due to longitudinal Fabry–Pérot resonances appear at

longer wavelengths (1540~1640 nm), which indicates the optical loss is gradually compensated by the material gain. Although such cavity modes near the band edge from highly strained Ge have been already observed numerous times [22], [42], [145], [146], [154]–[156], all the previous reports showed the apparent intensity saturation and linewidth broadening of cavity modes with pump powers possibly owing to insufficient gain at low strain [155], [156], poor optical cavity [22], [145] and/or unsatisfactory thermal management [42], [146]. For a larger pump power of 3.5 kW cm^{-2} , the cavity modes become much stronger with a superlinear increase in the output intensity along with linewidth narrowing. This presents the evidence of optical amplification in highly strained Ge gain medium. Additionally, the spontaneous emission well above the band edge ($<1550 \text{ nm}$) also collapses into sharp cavity modes, thus suggesting that the entire emission band is close to the transparency condition. A wide gain bandwidth (FWHM $\sim 150 \text{ nm}$) is obtained. The measured mode spacing is 8 nm , which is consistent with the simulated value. It is worth mentioning that the occurrence of amplified cavity modes over the whole emission band is in stark contrast to conventional lasing materials for which cavity modes are generally observed only within a relatively narrow gain bandwidth.

At higher pump powers of 5.1 , 8.5 , and 14.6 kW cm^{-2} , the cavity modes near 1530 nm preferably build up as they enter the lasing regime. In contrast, the modes near the band edge ($> 1600 \text{ nm}$) appear to saturate. At the highest pump power of 14.6 kW cm^{-2} , the peak emission intensity of the cavity modes near 1530 nm is >20 times stronger than the background emission intensity, and the FWHM of the gain bandwidth is reduced to $\sim 50 \text{ nm}$ from $\sim 100 \text{ nm}$. While, the bandwidth of the background emission is $\sim 150 \text{ nm}$. Although the gain bandwidth is relatively large, it is comparable to the previously reported value ($\sim 40 \text{ nm}$) for a 0.6% strained Ge photonic wire [157]. This large gain bandwidth is likely attributed to the unusually large amount of strain-induced valence band splitting ($\sim 72 \text{ meV}$ for 1.6% uniaxial strained Ge). In addition, the gain tends to saturate above the threshold carrier density, while the loss continuously increases with increasing injection density (resulting in a zero net gain eventually). Therefore, the large valence band degeneracy and the gain saturation restrict a narrow gain bandwidth for a single mode laser [158].

Fig. 4. 12 PL emission spectra of the 1.6% strained Ge nanowire laser at 83 K.

The lasing action can also be quantitatively evidenced by the evolution of the linewidth narrowing with increasing pump power, as illustrated in Fig. 4.13. The linewidth was measured by the FWHM of the cavity mode at 1530 nm. The linewidth is reduced from 2.5 nm to 1.3 nm by increasing the pump power above the threshold. The corresponding threshold Q-factor at 1530 nm is ~ 850 . Above 15 kW cm^{-2} , it shows the linewidth broadening, which is likely attributed to the local heating. As increasing the pump power, the sample temperature increase is large enough to preclude lasing action owing to rapidly

increasing material loss. This challenge can be resolved by replacing the thermal oxide layer with a more thermally conductive material, such as Al_2O_3 , and Si_3N_4 .

Fig. 4. 13 FWHM of the linewidth vs. the pump power at 83K.

Fig. 4.14 (a) shows the integrated PL intensity of the lasing modes as a function of pump power. The output intensity shows a superlinear growth (projected by a black dashed line), and the threshold pump power is determined to be $\sim 3.0 \text{ kW cm}^{-2}$. than 325 kW cm^{-2} of the recently reported GeSn laser [17]. The linear growth ends up with the output saturation at a high pump (above 14.6 kW cm^{-2}) due to the thermal effect. A double-logarithmic plot of the integrated output power in Fig. 4.14 (b) clearly shows an S-shaped curve: manifesting typical nonlinear threshold behaviour. The non-linear kink represents the transition from spontaneous emission to lasing action.

Fig. 4. 14 (a) The linear plot of integrated output intensity vs. the pump power.
(b) The double-log plot of the integrated output intensity.

4.4.3 Rate Equation Analysis

A multi-mode rate equation analysis was employed to obtain the spontaneous emission factor, β , which calculates the fraction of the spontaneous emission contributing to the lasing emission. The curve fitting was performed by assuming five cavity modes (the peak mode at 1530 nm) with the same

threshold modal gain, group velocity and spontaneous emission factor [159]. The simplified rate equations to describe the dynamic relation between carrier density and photon density can be expressed as:

$$\frac{dN}{dt} = \eta_{eff} P - \frac{N}{\tau_r} - \frac{N}{\tau_{nr}} - CN^3 - m_s v_g g(N) S, \quad (4.13)$$

$$\frac{dS}{dt} = \Gamma v_g (g(N) - g_{th}) S + \Gamma \beta \frac{N}{\tau_r}, \quad (4.14)$$

where N is the carrier density in the Ge nanowire, S is the photon density, P is the optical pumping power, η_{eff} is the fraction of the optical pumping power absorbed by the nanowire, τ_r and τ_{nr} are radiative and non-radiative recombination lifetimes, C is the Auger recombination coefficient, m_s is the number of lasing modes, v_g is the group velocity, $g(N)$ is the material gain, g_{th} is the threshold gain, Γ is the confinement factor and β is the spontaneous emission factor.

The non-radiative recombination lifetime of a Ge layer was previously measured to be ~ 3.14 ns [160], [161]. They used a multiple hydrogen-annealing heteroepitaxy (MHAH) growth technique. By MHAH method, the TDD is around $1 \times 10^7 \text{ cm}^{-2} \sim 1 \times 10^8 \text{ cm}^{-2}$ [160]. In the experiment, on the other hand, an As-doped Ge seed layer was employed to reduce the TDD in the Ge layer to $< 5 \times 10^6 \text{ cm}^{-2}$ [116]

Previously, the carrier lifetime has been empirically correlated to the threading dislocation density as in the following equation [162]:

$$\frac{1}{\tau_{TDD}} = \pi^3 D N_{TDD} / 4 \quad (4.15)$$

where τ is the minority carrier lifetime, τ_0 is the minority carrier lifetime without considering recombination, τ_{TDD} and τ_p are the minority carrier lifetime associated with the recombination at threading dislocation and dopants, respectively. D is the minority-carrier diffusion coefficient and N_{TDD} is the threading dislocation density.

The lower bound value of the TDD of $1 \times 10^7 \text{ cm}^{-2}$ was taken for Ge grown by MHAH technique, and the upper bound value of the threading

dislocation density of $5 \times 10^6 \text{ cm}^{-2}$ was taken for the Ge layer in the study. Since the lifetime is inversely proportional to the TDD as shown in Eq. (4.15), the lifetime of the Ge layer is estimated to be $\sim 6.78 \text{ ns}$.

In addition, lifetime is also highly dependent on doping concentration as extrinsic dopants act as recombination centres. For a doping concentration of $>10^{16} \text{ cm}^{-3}$, E. Gaubas, et al. showed that the carrier lifetime related to the doping concentration can be expressed as [163]:

$$\tau_p = \frac{1}{n_{dop}}, \quad (4.16)$$

where n_{dop} is the doping concentration. Since the doping concentration is of $6 \times 10^{18} \text{ cm}^{-3}$, doping concentration the lifetime in Ge layer of 11 ns is used. The radiative lifetime is estimated to be 28 ns based on the radiative coefficient of $1.3 \times 10^{-10} \text{ cm}^3 \text{ s}^{-1}$ [48]. Therefore, τ_{nr} and τ_r are assumed to be 11 ns and 28 ns , respectively. An Auger recombination coefficient of $1 \times 10^{-32} \text{ cm}^6 \text{ s}^{-1}$ is used due to the non-negligible surface recombination [164].

A linear relationship between the material gain and the carrier density is assumed, which can be expressed as $g(N) = \alpha(N - N_0)$. The differential gain $\alpha \sim 1.4 \times 10^{-17} \text{ cm}^2$ and the transparency carrier density $N_0 \sim 5.9 \times 10^{19} \text{ cm}^{-3}$ based on simulation. The modal gain at the threshold is calculated by $\Gamma g_{th} = 2\pi n_g / Q\lambda$, where n_g is the group index. The confinement factor is assumed to be $\Gamma \sim 0.45$. The group index $n_g \sim 3.2$ and the threshold Q-factor ~ 850 , as mentioned in Section 4.4.2 The fitted curve to extract β is plotted with the measured data in Fig. 4.15, and the β value is 0.08 according to this fitting. The fitting parameters are listed in Table 4.3.

Fig. 4. 15 Light-out versus light-in (L-L) curve of the strained Ge nanowire laser. Symbols and a red line represent the measured data and the calculated theoretical curve, respectively. A spontaneous emission factor of $\beta \sim 0.08$ is extracted. Calculated curves with other β values are also plotted for comparison.

Table 4. 3 Parameters list for spontaneous emission factor fitting.

Parameter	Definition	Value
τ_r	Radiative lifetime	28 ns
τ_{nr}	Non-radiative lifetime	11 ns
C	Auger recombination coefficient	$1 \times 10^{-32} \text{ cm}^6 \text{ s}^{-1}$
Q	Quality factor of the cavity	850
Γ	Optical confinement factor	0.45
m_s	Number of lasing modes	5
n_g	Group index	3.2
v_g	Group velocity ($v_g = c/n_g$)	$9.38 \times 10^9 \text{ cm/s}$
α	Differential gain	$1.4 \times 10^{-17} \text{ cm}^2$
N_0	Transparency carrier density	$5.09 \times 10^{19} \text{ cm}^{-3}$
Γg_{th}	Threshold modal gain	151.2 cm^{-1}
g_{th}	Threshold gain	336 cm^{-1}
β	Spontaneous emission factor	0.08

The threshold injection carrier density in active region N_{th} is estimated to be $5.7 \times 10^{19} \text{ cm}^{-3}$. In the pumping condition, the pulse duration is at the same order as the carrier lifetime. The excited carrier density is not only dependent on the number of photons per pulse but also on the pulse duration and carrier lifetime. The injection carrier density N is calculated based on a rate equation:

$$\frac{dN}{dt} + \frac{N}{\tau} = G_n, \quad (4.17)$$

where τ is the carrier lifetime and G_n is the electron generation rate. The electron generation rate is calculated from the below equation by assuming perfect quantum efficiency [159].

$$G_n = G_p = \frac{\eta_a A_p}{\hbar \omega V_a} \left(\frac{P_{peak}}{A_p} \right), \quad (4.18)$$

where η_a is the fraction of pump power absorbed, A_p is the pump spot size area, and $\hbar\omega$ is the injection photon energy, P_{peak} is the peak pump power and V_a is the active region volum. Based on Eqs. (4.17) - (4.18), N depends on the carrier lifetime and can be expressed as τG_n . Here, the reflection loss is neglected [165].

According to Eq. (4.19), an absorbance of 0.153 is used for a 220 nm Ge with the absorption coefficient of 16000 cm^{-1} at 1064 nm. The fraction of pump power absorbed, η_a related to absorbance, A , and transmittance, T , can be expressed by:

$$I = I_0 \exp(-\alpha d) , \quad (4.19)$$

$$\eta_a = 1 - T , \quad (4.20)$$

$$A = 2 - \log_{10} T , \quad (4.21)$$

Thus, the fraction of pump power absorbed is 30%.

At threshold peak pump power of 2.3 mW, the injection carrier injection is limited by the carrier lifetime and calculated to be $3.0 \times 10^{19} \text{ cm}^3$ using the parameters mentioned above.

The injection carrier density at the active region is enhanced due to the carrier collection effect. There is a strong strain gradient in active region (as shown in Fig. 4.10 (b)). The strain maximizes at the device/nanowire centre and reduces as moving away from this centre position. Subjected to the strain induced electric field, the injected carriers are drifted to the active region and constricted [26], [154]. To estimate the carrier enhancement, it was assumed that all the injected carriers can reach the active region. Then, the carrier enhancement factor approximately equals the total excited area over the uniformly strained active area of $8 \mu\text{m} \times 700 \text{ nm}$. The yellow circles in Fig. 4.16 gives the total excited area. Therefore, the carrier enhancement factor is ~ 1.9 , and the threshold injection carrier density in active region N_a is $5.7 \times 10^{19} \text{ cm}^{-3}$.

Fig. 4. 16 Plan-view SEM of fabricated nanowire cavity. The Ge area within the yellow circle represents the total excited area. Cavity Structure: nanowire width W1: 700 nm, nanowire length: 8 μm . DBR design: 10 periods, 189 nm air trench/ 190 nm Ge trench.

The threshold gain is estimated from the threshold modal gain equation. The equations are expressed as:

$$\Gamma g_{th} = k_0 n_g / Q, \quad (4.22)$$

$$k_0 = 2\pi / \lambda(6), \quad (4.23)$$

where Γ is the confinement factor, Γg_{th} is the threshold modal gain at threshold, n_g is the group index, k_0 is angular wavenumber and Q is the quality factor at threshold. The confinement factor and group index are estimated from the FDTD simulation: $\Gamma = 0.45$, $n_g \sim 3.2$. Near the threshold pumping density, the peak at 1529.6 nm has a FWHM of 1.80 nm, fitted to a Lorentzian function. The estimated Q -factor at threshold is 850, and the corresponding threshold modal gain Γg_{th} is calculated to be 151.2 cm^{-1} . Thus, the threshold gain g_{th} was estimated to be $151.2/0.45 = 336 \text{ cm}^{-1}$.

4.4.4 Strain Dependent Emission

This section will focus on the strain effect on PL emission. As shown in Fig. 4.17 (a), the normalized PL spectra of the 1.6% strained laser device clearly show the multi-mode lasing emission at a high pump power (14.6 kW cm^{-2}), while it shows only the spontaneous emission at low pump power (0.7 kW cm^{-2}). However, for the unstrained laser device (0% strain) in Fig. 4.17 (b), only weak cavity resonances are observed from the PL spectra at the high pump power. This comparison between strained and unstrained structures proves that the high tensile strain in the Ge nanowire increases the gain and lowers the lasing threshold.

Fig. 4. 17 Normalized PL spectra of (a) a 1.6% strained structure and (b) an unstrained (0%) structure at 83 K.

Fig. 4.18 provides the detailed studies optical property dependency on nanowire strain by comparing the emission spectra of 0%, 0.6%, 1.2% and 1.6% strained structures at the same pump power of 14.6 kW cm^{-2} . The unstrained structure only shows weak cavity resonances, in terms of the ratio of resonance peak intensity versus the spontaneous emission peak, while the resonance peaks are strong for the other three samples. The 0.6% structure starts to show resonance peaks with a high optical loss as the emission is still dominated by the background spontaneous emission. When the strain is increased to 1.2%, the resonance peaks become stronger and spread over the entire emission band. Due to the increase in net gain, the resonance peaks dominate the background spontaneous emission and lasing modes are built up near 1530 nm. All these observations clearly show the positive effect of strain in reaching lasing oscillation. The material gain of the highly strained nanowire is able to compensate the loss, and the resonances with peak gain can be amplified.

Fig. 4. 18 Normalized PL emission spectra of the 0%, 0.6% 1.2% and 1.6% strained Ge nanowire structures at 14.6 kW cm^{-2} pump power at 83 K.

4.5 Summary

In summary, the multi-mode lasing action was achieved from a highly strained (1.6%) Ge nanowire cavity at 83K with a low threshold of $\sim 3.0 \text{ kW cm}^{-2}$. This measured threshold is approximately two order of magnitudes lower than the reported GeSn laser [17]. Besides using the high-quality GOI substrate, the net gain that can be achieved was also due to the large tensile strain and the low temperature operation. The uniform high tensile strain was induced to the nanowire active region through the relaxation of the stress pads. This resulted in enhanced carrier injection into the direct Γ band. The tensile strain can be also varied by easily changing the geometric parameters of the cavity. The good thermal management of the nanowire design in contact with the thermal oxide provides an extra heat-conducting path. This design releases the heating effect caused by the high pumping power. Combined with the low temperature operation at 83 K, the gain compensated the optical losses induced by carrier absorption, resulting in the lasing action.

The demonstration of this low-threshold, highly strained Ge nanowire laser markedly narrows the gap between conventional III–V lasers and their group IV counterparts. Thus, it opens up new avenues for a fully integrated electronic-photonic system. Additionally, room-temperature lasing action can possibly be achieved by employing a larger gain and improving the thermal conduction.

Chapter 5: Viable Substrate for III-V Compounds

Integration

5.1 Introduction

Direct band-gap III-V compounds have been known for their robustness and high performance in electronic and optical devices. The realisation of III-V components integrated on a Si platform can be used for many novel applications, such as enabling high mobility transistors [39] and on-chip optical communications [27], [28]. Apart from these applications, the possibility of utilizing existing CMOS infrastructures for the processing of III-V components on Si substrates bring additional advantages in terms of production cost and manufacturing scalability [10].

Silicon-on-insulator (SOI) has been widely used for low off-state leakage transistors and a waveguide layer for III-V photonics [36]. However, due to the large lattice mismatch between Si and III-V materials, the integration of a III-V device with Si can be implemented by wafer-bonding [166], [167]. Many of these III-V devices, such as InGaAs high electron-mobility transistors (HEMT) and AlInGaP light emitting diodes (LEDs), are based on GaAs substrates. As Ge and GaAs are closely lattice matched (mismatch $< 0.1\%$), it is possible to epitaxially grow III-V devices on a bulk Ge. The recent achievements have demonstrated InGaAs/GaAs HBT, InP-based HEMT and InGaP/GaAs solar cell on Ge-on-insulator (GOI) substrates [38]–[40]. All of these results have shown great promise for using GOI for III-V integration with a Si platform while keeping the merits of SOI.

In the previous chapters, a scalable method to fabricate a GOI substrate through epitaxy, bonding and layer transfer was demonstrated. The threading dislocation density (TDD) of the GOI wafer could be reduced below 10^7 cm^{-2} by employing different growth and processing techniques, of which the TDD value is low enough for reliable electronic device performance [168]. Additionally, the smooth Ge layer surface would suppress the formation of new threading dislocations for III-V epitaxy on top [169]. In this chapter, it will focus on the III-V integration on GOI.

Besides the small lattice mismatch, there is a small difference in thermal expansion coefficient (CTE) (mismatch < 1.6%) between GaAs and Ge. Therefore, GaAs is a promising III-V material to be used for III-V initiation growth on a GOI substrate. However, the crystal polarity difference between III-V Ge causes a certain type of defect called anti-phase boundaries (APBs). The APBs result in crack-like patterns on surface and stacking faults [170][171] [172], [173]. These APB-related defects act as electrically active recombination centres, reducing the emission efficiency of the III-V compounds [174]. The APBs can be effectively suppressed by applying a certain offcut to the substrate and applying high temperature annealing prior to the growth of III-V compounds [175]. However, it still need to optimise the growth conditions to further reduce the number of APBs and achieve uniform GaAs coverage on the group IV surface. It was found that arsine (AsH_3) partial pressure has a critical influence on APBs and surface roughness during the epitaxy of GaAs on Ge [176]. Thus, to ensure the high-quality epitaxy of III-V devices, the AsH_3 partial pressure needs to be optimised to obtain a high-quality GaAs buffer.

In this chapter, it investigates the growth conditions of a high-quality GaAs buffer on GOI to initiate the III-V epitaxy. The GaAs/GOI is subsequently used as a substrate template for III-V LED epitaxy, fabrication and characterizations to explore the possibilities of using GOI for III-V photonics integration.

5.2 Experimental Procedures

In this experiment, a GOI substrate with a 200 nm thermal oxide (THOX) was used for III-V integration. The GOI had had a 6° off-cut towards the nearest (111) plane to suppress the formation of APBs. The TDD and RMS roughness of the GOI substrate calibrated previously were $4.3 \pm 0.4 \times 10^7 \text{ cm}^{-2}$ and $0.2 \pm 0.1 \text{ nm}$, respectively. Additionally, the GOI substrate was expected to be free of thermal bubble issues after III-V epitaxy at a high growth temperature due to the use of a sufficiently thick THOX layer.

First, the initiation conditions of GaAs epitaxy on a Ge surface were investigated. For simplicity, a bulk Ge substrate was used to study the impacts

of AsH₃ partial pressure on the material quality of GaAs on Ge. GaAs was grown on the GOI substrate on the MOCVD system using a group III precursor, trimethyl-gallium (TMGa), carried by purified H₂ and a hydride gas, AsH₃. The growth of GaAs on the Ge surface used a two-step growth process consisting of a thin high-temperature (HT) GaAs initiation layer and a low-temperature (LT) GaAs buffer layer, as shown in Fig. 5.1. The thin HT GaAs layer (100 nm) was initiated on Ge at 680 °C at different reactor pressures varying from 100 mbar to 400 mbar with a constant V/III ratio of 936 followed by a 500 nm GaAs buffer using normal III-V growth conditions (630 °C, 100 mbar). It was found that the optimised growth pressure was 400 mbar. This growth condition was used for III-V LED epitaxy on the GOI substrate.

Fig. 5.1 Schematic of the GaAs initiation on bulk Ge using a two-step growth process.

An AlInGaP/InGaP MQW LED for red light emission was re-grown on a 20 mm×20 mm GOI substrate sample. The LED structure is shown in Fig. 5.2. A thin GaAs layer was initiated on the Ge surface at 725 °C at a reactor pressure of 400 mbar, followed by a 200 nm GaAs buffer grown at 650 °C at 100 mbar. The growth temperatures used here were higher than those for the development of GaAs on Ge due to the temperature re-calibration of the MOCVD reactor. The GaAs buffer was n-type doped with tellurium (Te) to $\sim 1 \times 10^{19} \text{ cm}^{-3}$ as the *n*-type contact layer. The growth temperature (650 °C) and pressure (100 mbar) remained the same for the subsequent growth of a MQW LED. AsH₃ gas was switched off, while trimethyl-Indium (TMIn), trimethyl-aluminium (TMAI) and PH₃ were switched on for the (Al)InGaP materials growth. The MQW LED structure grown consisted of five periods of InGaP (10 nm)/AlInGaP (30 nm). The QWs were sandwiched between 200 nm *n*-type and

p-type AlInGaP cladding layers on each side. In order to protect the top *p*-cladding layer from oxidation and enhance the current spreading, a *p*-type GaAs cap layer doped with zinc (Zn) to $\sim 1 \times 10^{18} \text{ cm}^{-3}$ was grown. In the same growth run, a 2-inch bulk Ge substrate with a 6° offcut (*n*-type As doped, resistivity of 0.01-0.1 $\Omega \cdot \text{cm}$) was loaded along with the GOI substrate for comparison.

Fig. 5.2 The layer structure of the AlInGaP/InGaP MQW LED on GOI substrate.

At last, after the epitaxy, MQW LEDs on both GOI and bulk Ge substrates were fabricated and characterised. After defining the mesa area by the first lithography, the GaAs cap layer was removed by a mixed solution of H_2O_2 : NH_4OH : H_2O (1:1:1). The LED mesa with a geometry of 1 mm $\times$ 1 mm was wet-etched by a hydrochloride acid (HCl) solution (36%, w/w) for 30 s. Due to the etching selectivity of GaAs over (Al)InGaP in HCl, the *n*-type GaAs buffer acted as an etch-stop layer in the mesa etching process. Then another two

lithography steps were performed to define the metal contact regions. The *n*-type Ni/Ge/Au metal contact and *p*-type Ti/Au metal contact were made on the *n*-type GaAs buffer and *p*-type GaAs cap layer deposited by an electron beam (e-beam) tool. The Ni/Ge/Au contact was then annealed at 390 °C for 30 s by RTA to reduce its contact resistance. A 70 nm silicon nitride passivation layer was deposited at 300 °C in a plasma-enhanced chemical-vapour deposition (PECVD).

For materials characterisation of the GaAs epitaxy on Ge, AFM was used to measure the surface morphology. Both TEM and SEM were used to view the micro-structure of GaAs on Ge and LEDs. To analyse the crystalline quality, high-resolution reciprocal space mapping (RSM) was performed by XRD. For LED performance characterization, cross-section TEM was used to inspect the micro-defects in LED. Current density-voltage (*J-V*) measurement and electroluminescence (EL) were used to characterise LED electrical and optical performance, respectively.

5.3 Results and Discussion

5.3.1 Materials Characterisation

The normal growth reactor pressure is 100 mbar for III-V epitaxy on GaAs. High-quality III-V epitaxy can be obtained using this growth condition. However, in the growth of GaAs on a Ge surface, using 100 mbar reactor pressure leads to an extremely rough GaAs surface with a large number of voids and hillocks. The cross-section SEM image in Fig. 5.3(a) shows that many large voids originated from the GaAs/Ge growth interface, causing a large RMS roughness value of 46 nm in Fig. 5.3(b). It is highly possible that the surface roughening was caused by the formation of APBs during the GaAs initiation [170]–[173]. These results indicate that, although GaAs and Ge have a small lattice mismatch, the epitaxy of GaAs on Ge is still challenging in achieving an APB-free uniform surface.

Fig. 5.3 GaAs on Ge grown at 630 °C, 100 mbar showing (a) the cross-sectional SEM image of the voids originated from growth interface, and (b) the 10×10 μm² AFM scan of the rough GaAs surface with a RMS roughness of 46 nm.

With a constant V/III ratio, the AsH₃ partial pressure, $p(\text{AsH}_3)$, was calculated from the reactor pressure. When the reactor pressure varied from 100 to 400 mbar with a V/III ratio of 936, the AsH₃ partial pressure changed from 1.25 mbar to 5 mbar, accordingly. The Nomarski microscope images in Fig. 5.4 show the changes of surface morphology of GaAs on Ge with the increasing $p(\text{AsH}_3)$. The number of voids decreased and eventually disappeared when the $p(\text{AsH}_3)$ increased to 5 mbar.

Fig. 5.4 Nomarski microscope images of a 100 nm GaAs layer grown on Ge with the same V/III ratio of 936, but different $p(\text{AsH}_3)$ of (a) 1.25 mbar, (b) 2.5 mbar and (c) 5 mbar.

The cross-section TEM image in Fig. 5.5(a) shows a smooth GaAs surface and no sign of voids. Additionally, it shows a clean GaAs/Ge without misfit dislocations, threading dislocations and APB-related defects. The $10\ \mu\text{m} \times 10\ \mu\text{m}$ AFM image in Fig. 5.5(b) shows a significantly reduced RMS roughness of 0.5 nm. These results show that APBs were suppressed using high AsH_3 partial pressure, and the RMS roughness was reduced due to this improvement. Therefore, the III-V initiation on GOI also used a high AsH_3 partial pressure of 5 mbar.

Fig. 5.5 (a) Cross-sectional TEM image of the GaAs on Ge using an optimized $p(\text{AsH}_3)$ of 5 mbar, showing a APB-free growth interface. (b) $10 \times 10 \mu\text{m}^2$ AFM image showing a reduced RMS roughness of 27 nm.

Fig. 5.6 shows the cross-sectional TEM image of an AlInGaP/InGaP MQW LED structure on a GaAs buffer grown on a GOI substrate. The TEM image clearly shows five quantum wells in the LED, and the inset image (the right upper image) shows sharp and smooth interfaces between the AlInGaP barrier and the InGaP well. However, two threading dislocations were observed in the LED active region. The generation of threading dislocations was likely attributed to defects from the GOI. As can be seen, a clear defect cluster was found in the Ge buffer, and the TDD of the GOI was estimated to be $4.3 \pm 0.4 \times 10^7 \text{ cm}^{-2}$. Thus, it was possible to capture one or two dislocations in the cross-section TEM image. Additionally, the inset image (right bottom corner) shows good wafer bonding quality as no distinctive defects or film delamination at the bonding interface.

Fig. 5.6 Cross-sectional TEM image of an AlInGaP/InGaP MQW LED structure on GOI with 5 periods (10 nm thick per period) of InGaP MQWs cladded by AlInGaP layers. The bonding interface did not depict any distinctive defects.

The TDD level of the GOI substrate was about three orders of magnitude higher than that of the bulk Ge substrate. As shown in Fig. 5.7, the same MQW LED structure on a bulk Ge substrate shows no threading dislocations. This indicates the importance of the substrate to the materials quality of III-V epitaxy.

Fig. 5.7 Cross-sectional TEM image of AlInGaP/InGaP MQW LED structure on Ge.

The symmetric (004) and asymmetric ($\bar{2}24$) RSM were measured to calculate the strain status and compositions of MQW LED on GOI, as shown in Fig. 5.8. The fluctuated bands in Figure 10 are due to light interference at the interfaces, which indicates good crystal quality and layer homogeneity. As mentioned, the broadening in Q_x indicates the existence of strain and dislocations. The indium content of InGaP was 48%, and a thermal mismatch induced tensile strain of 0.20% existed in the MQW structure.

Fig. 5.8 The RSM of AlInGaP/InGaP MQW LED on GOI substrate taken at the (004) (left) and ($\bar{2}\bar{2}\bar{4}$) (right) diffraction plane.

5.3.2 Electrical Performance

The J - V measurement in Fig. 5.9 compares the electrical performance of the MQW LED on both GOI and bulk Ge substrates. According to the band-gap energy of InGaP for red light emission ($E_g \sim 1.91$ eV), the LED turn-on voltage was expected to be around 1.5 V. The LED on bulk Ge turns on at 1.5 V, showing a stiff linear operation region. However, the LED on GOI shows an early turn-on voltage of ~ 1.3 V and a high leakage current density < 1.5 V. The

inset image shows the semi-log plot of the J-V characteristics. In the reverse bias region (< 0 V), a high dark current density of the LED on GOI is evident compared to the LED on bulk Ge. The J-V characteristics were fitted by a two-diode model, and several parameters were abstracted from the fit.

Fig. 5.9 J-V characteristics of LEDs on a Ge substrate and GOI. The device geometry is $1 \times 1 \text{ mm}^2$.

The two-diode model is widely used for I-V characteristics analysis of III-V materials systems, and its equivalent circuitry is shown in Fig. 5.10. The equation used for the fit is expressed as shown in Eq. (5.1) [177]:

$$J = J_{01} \exp\left[\frac{q(V - JR_s)}{k_B T}\right] + J_{02} \exp\left[\frac{q(V - JR_s)}{nk_B T}\right] + \frac{V - JR_s}{R_p}, \quad (5.1)$$

where J_{01} and J_{02} are the saturation current density, q is the electron charge, R_p is the shunt resistance, R_s is the series resistance, n is the diode ideality factor, k_B is the Boltzmann's constant, and T is the junction temperature. Based on the model, the best fitting parameters showed a high reverse saturation current density, J_{02} , of LED on GOI ($J_{02} = 2.28 \times 10^{-5} \text{ A} \cdot \text{cm}^{-2}$), while the LED on bulk Ge only shows a J_{02} of $1.09 \times 10^{-11} \text{ A} \cdot \text{cm}^{-2}$. Since J_{02} is a minority lifetime-dependent parameter, the minority lifetime and diffusion length are usually limited by the high TDD [178]. Therefore, the high leakage current density in

LED on GOI was likely caused by the high TDD of the Ge layer and LED junction.

Fig. 5.10 Equivalent circuit for a two-diode model.

5.3.3 Optical Performance

Fig. 5.11(a) shows the EL spectra of LEDs on GOI and bulk Ge at the injection current density of 10 A/cm^2 . As more threading dislocations existed in LED on GOI causing non-radiative recombination and carriers scattering, the LED on GOI was about 50% as bright as the LED on bulk Ge. The LED on GOI showed a red-shift of 2.5 nm of its peak emission position, compared to the LED on bulk Ge. This was due to the different strain states in the InGaP layer: 0.20% and 0.09% tensile strain in the InGaP active layer on GOI and Ge, respectively. This led to a bandgap reduction of 12 meV for EL emission agreeing with the calculation (13 meV).

Regarding the asymmetric shape of the EL spectra, it is due to the $Ee1$ and $Ee2$ energy states of the QW structure. Two peaks are found using Gaussian distribution in Fig. 5.11(b), and the peak separation in energy is 29 meV. The calculated $Ee1$ and $Ee2$ are 32 meV and 6 meV, respectively. The energy difference between the two states (26 meV) approximately agrees with the peak separation. Therefore, the asymmetric shape of the EL spectra is caused by the different energy states of QW. Fig. 5.11(c) shows that the light output of LEDs on both substrates have approximately linear relationships with the injection current density. This shows that the LED on bulk Ge has a higher luminescence efficiency, which is about twice the LED on GOI. As TDD was

the major difference in LED devices on GOI and bulk Ge, the degraded light output of the LED on GOI is attributed to its high TDD.

Fig. 5.11 (a) Room temperature EL spectra of AlInGaP/InGaP MQW LEDs on GOI and bulk Ge. (b) The EL spectra of LED on GOI and two peaks are fitted using Gaussian distribution. (c) Linear fit of the light-current (L-I) curves for LEDs on GOI and bulk Ge.

5.3.4 Improvement of LED Quality

The electrical and optical performances show that the poorer performance in LED on GOI can be attributed to its high TDD. As mentioned in Section 5.3.1, the GOI viable substrate has a high dislocation density of $\sim 4.3 \pm 0.4 \times 10^7 \text{ cm}^{-2}$. This high dislocation level in the seeding layer leads to the generation of threading dislocations in the LED active region, which function as the recombination centres and thus degrade the LED performance. While no threading dislocations is observed in the the same MQW LED structure grown on a bulk Ge substrate. This indicates the importance of the substrate to the materials quality of III-V epitaxy. Therefore, a high quality GOI by annealing in O_2 (method mentioned in Section 3.3.5) was employed as the viable substrate. As shown in the SEM image in Fig. 5.12, the EPD counts show a TDD of $2.4 \times 10^6 \text{ cm}^{-2}$ after annealing.

Fig. 5. 12 Plan-view SEM image of etching pits in a GOI by annealing in O₂ environment

Fig. 5. 13 (a) Plane-view TEM image taken at double beam condition (220), and (b) cross-sectional TEM image of GOI after thermal treatment and CMP.

Two threading dislocations are observed under a 4 μm TEM view window (shown in Fig. 5.13 (a)). According to the plane-view TEM image, there is low in-plane dislocation in the Ge layer. The finding coincides with the EPD count obtained under SEM and optical microscope. In addition, the cross-sectional TEM image in Fig. 5.13 (b) shows no distinctive defects such as threading dislocations or dislocation arms. Both plane-view and cross-sectional

TEM images confirm that there is a high quality Ge film on top of the buried oxide layer.

The cross-sectional TEM image of an AlInGaP/InGaP MQW LED structure grown on the quality improved GOI substrate is shown in Fig. 5.14. The TEM image clearly shows ten quantum wells in the LED, and the inset image (the right upper image) shows sharp and smooth interfaces between the AlInGaP barrier and the InGaP well. No threading dislocations were observed in the LED active region as well as the GaAs buffer layer and the AlInGaP clad layer, indicating that a high quality LED structure with low defects level has been integrated on GOI. The electrical and optical properties investigation will be implemented in the future study.

Fig. 5. 14 Cross-sectional TEM image of the AlInGaP/InGaP MQW LED structure on the quality improved GOI. No distinctive defects is observed in the active region.

5.4 Summary

In summary, the epitaxy of GaAs initiation on a Ge surface was achieved

successfully using a high AsH_3 partial pressure of 5 mbar to suppress the formation of APBs. The RMS roughness was reduced below 1 nm. Using the optimised GaAs growth conditions, an AlInGaP/InGaP MQW red LED was demonstrated on a GaAs/GOI substrate. The high leakage current density and light output degradation of LED on GOI compared to LED on bulk Ge were attributed to the high TDD in the Ge layer and the LED junction. Although further improvement of GOI quality for better III-V photonics performance is still needed, this work demonstrated the possibility of using GOI for III-V integration. Furthermore, key issues during the integration were addressed.

Chapter 6 Conclusions and Recommendations

6.1 Summary of Results

The motivation of this thesis was described in detail in Chapter 1. A low-cost, high-efficiency light source on Si platform is required to enable a fully integrated photonic system with CMOS. Ge and III-V materials are promising candidates for the light source in the photonic integrated circuit, but challenges still exist for their practical use. Ge-based lasers are compatible with CMOS processes. In particular, the strain engineered Ge can achieve a net gain for lasing behaviour. However, Ge-based lasers suffer from a high lasing threshold due to their indirect band properties and high optical losses in the gain medium. Direct III-V materials are known for their high optical performance, but the integration cost with the Si platform is high.

The epitaxial integration of III-V photonics on Si can enable low-cost, large-scale integration. However, the large lattice mismatch between III-V and Si would degrade the III-V material quality and the optical performance. A high-quality GOI substrate is a promising technology, which enables the integration of the Ge laser and III-V light sources on a Si platform. The GOI substrate not only provides the material gains and optical confinement for the Ge laser, but it also creates the lattice matching conditions for III-V epitaxy on Si.

Several research gaps exist regarding the topics of the GOI fabrication, the Ge lasers on GOI and the integration of III-V photonics on GOI. First, the GOI substrate is fabricated by bonding a Ge/Si wafer to an ‘on-insulator’ wafer followed by layer transfer and other bonding processes. The GOI quality is highly dependent on the epitaxy of the Ge/Si wafer and the bonding processes. According to the literature and the Ge/Si wafers developed in the SMART lab, it is difficult to reduce the TDD of the Ge buffer grown directly on Si below $\sim 5 \times 10^7 \text{ cm}^{-2}$ using a traditional two-step growth method with post-growth annealing. This TDD value of the Ge buffer is relatively high to be used for the Ge lasers and the integration of III-V photonics. In addition, the TDD value and surface roughness of the Ge buffer increase during the bonding and layer

transfer processes. Several issues regarding bonding strength and thermal bubbles also occur in wafer bonding.

Second, Ge-based lasers have a very high lasing threshold. Strong indirect band transitions and high optical losses make it challenging to achieve a high gain and a low lasing threshold. The highly strained Ge nanowire structure is promising to obtain a net gain. The indirect band structure can be altered under tensile strain, while the optical losses, such as free carrier absorption, are not increased. Although direct band emission was observed from a highly tensile strained Ge from the literature, lasing action has not been observed yet due to the GOI material quality, the design of the laser cavity and the measurement temperature.

Third, III-V photonic devices are more sensitive to TDD than III-V electronic devices. Although working III-V electronics have been demonstrated on a GOI substrate, the III-V photonics performance on GOI is unknown. For the integration of III-V photonics on Si via a GOI substrate, more complete studies are required on the integration processes from epitaxy to device fabrication to characterizations.

This thesis has focused on these research gaps and developed the new technologies of the integrated light sources in an integrated photonic system. First, by using a highly As-doped Ge seed layer in the epitaxy of the Ge/Si wafer, the TDD and RMS roughness of the Ge buffer were reduced to $\sim 5 \times 10^6 \text{ cm}^{-2}$ and 0.37 nm, respectively. The reduction in defect density and the improvement of the surface morphology were possibly due to the increased dislocation velocity or the Fermi level effect. This TDD value would enable the integration of Ge lasers and III-V LEDs on Si with reliable optical performance. Meanwhile, the low RMS roughness of the Ge buffer ensures a good bonding surface.

Second, an 8-inch GOI structure was demonstrated via wafer-scale bonding and layer transfer from a Ge/Si wafer. However, the TDD and the roughness of the transferred Ge buffer increased during the bonding processes. By employing a chemical-mechanical polishing (CMP) step, the top defective region of the GOI was removed, and the TDD and RMS roughness of the Ge

buffer were comparable to the buffer quality of the Ge/Si wafer. In the GOI structure, the thermal oxide (THOX) thickness was optimized to suppress the formation of thermal bubbles at the bonding interface, while retaining a relatively good thermal conductivity. In order to further improve the thermal management of the GOI substrate, an Al_2O_3 insulating layer with a higher thermal conductance than the THOX was developed, which would be integrated in the GOI fabrication standard procedures. Additionally, it showed another promising method to use O_2 annealing to reduce the defective Ge buffer without significantly reducing the buffer thickness. Therefore, the GOI quality would be improved further by combining these developed techniques, and superior properties of the GOI substrate would be achieved in terms of TDD, bonding interface and thermal management.

Third, a highly strained Ge nanowire laser was fabricated on a GOI substrate, and lasing behaviour with a low lasing threshold was observed. A high tensile strain was induced and tuned by the design of the laser cavity geometry. The tensile strain reduced the energy difference between the direct Γ and indirect L valleys, which increased the carrier density in the Γ valley promoting the direct band transitions. In addition, the localized strain distribution over the nanowire created a ‘pseudo’ hetero-structure with the relaxed Ge stressing pads, which also increased the carrier density in the nanowire active region. Distributed Bragg reflectors (DBRs) were integrated on the stressing pads to form a laser cavity. Since thermal conductance has significant influences on optical losses induced by carrier absorption, the nanowire design in contact with the underlying oxide layer provided an extra path of thermal conduction. In order to reduce the optical losses further, the PL measurement was conducted at low temperature. As a result, the multi-mode lasing action was achieved from a highly strained (1.6%) Ge nanowire laser at 83K with a low threshold of $\sim 3.0 \text{ kW cm}^{-2}$. This measured threshold is approximately one order of magnitude lower than that of the reported GeSn laser [17].

Last, the studies on the III-V LED performance on a GOI substrate showed promising results of integrating III-V light sources on a Si platform for a photonic integrated circuit. A high-quality GaAs layer was initiated on the

GOI surface using a high AsH_3 partial pressure to reduce the defect density related to anti-phase domains (APBs). An AlInGaP/InGaP red LED structure was subsequently grown on the GaAs buffer on GOI. Although further improvement of the III-V epitaxy and the GOI quality were needed, this study has demonstrated the possibility of using a GOI substrate to enable the epitaxial integration of III-V photonics on a Si platform.

6.2 Suggestions for Future Studies

The development of a high-quality GOI substrate has enabled many new technologies, such as the Ge laser and the integration of III-V on a Si platform. On one hand, it has demonstrated a promising path to use GOI to realise a fully integrated photonic circuit with CMOS. On the other hand, it showed challenges to improve the GOI quality and the device performance further. The following suggestions are made regarding the unresolved issues to fill up the existing research gaps.

Epitaxy of Ge/Si

The TDD of the Ge buffer on Si was reduced by a heavy As-doping in the Ge seed layer. The increase in dislocation velocity in Ge due to n-typed doping was confirmed experimentally, which would promote the dislocation movement and self-annihilations. Although the mechanisms of the reduction in TDD due to As-doping were not fully understood, this promising technique can further improve the Ge buffer quality for use in a GOI substrate. The optimizations of the growth conditions (temperature, pressure, etc.) and the doping profiles of the Ge seed layer would suppress the generation of dislocations and promote the annihilation of dislocations, respectively.

The annealing condition can be another important method to enhance the dislocation movement and annihilation. Systematic studies on growth conditions, doping profiles and annealing conditions would be very helpful to identify the key parameters responsible for the reduction in TDD.

GOI Fabrication

Many techniques have been proposed and developed for the GOI fabrication to reduce the TDD, suppress the thermal bubbles and improve the thermal conductance. However, it is challenging to combine all these techniques at one time for an overall high-quality GOI substrate. For example, the Al_2O_3 layer has a higher thermal conductivity than the thermal oxide. By replacing the thermal oxide layer with the Al_2O_3 layer, the thermal conductance in the GOI structure can be improved. As mentioned in the Ge laser performance, a good thermal management is important to reduce the free carrier absorption losses. A nanowire in contact with Al_2O_3 layer would achieve a better thermal conductance than using a thermal oxide layer. However, film blistering issues would incur at the bonding interface [179]. Thus, more research is needed to combine these techniques to obtain a better GOI quality.

Ge Laser on GOI

By further improving the GOI quality, the Ge laser performance is expected to be improved in terms of lasing threshold, output power and lasing efficiency. The 1.6% strained Ge nanowire laser showed a low threshold at low temperature. For practical use in the photonic integrated circuit, the lasing threshold needs to be further reduced and the lasing temperature needs to be increased significantly close to the room temperature. In addition, an electrically pumped laser is more desirable than an optically pumped laser. Therefore, the laser structure needs to be modified for electrical pumping.

The indirect band properties of the Ge are still mainly responsible for the relatively large lasing threshold and the lasing behaviour only at low temperatures. In order to promote the direct band transitions in Ge, a higher tensile strain can be employed and tin (Sn) atoms can be incorporated into Ge to form a GeSn alloy. Both techniques reduce the energy difference between the direct Γ and indirect L valleys, which creates a higher carrier density in the Γ valley. The tensile strain can be increased by shortening the nanowire length or enlarging the stressing pads, and a fairly high tensile strain of 5.7% was reported using this method [180]. The incorporation of Sn atoms can be

challenging due to the low solubility and large lattice mismatch between Sn and Ge. Additionally, besides increasing the material gain using high tensile strain, the optical losses can be reduced by having good thermal management in the Ge nanowire. As mentioned previously, since the nanowire is in contact with the underlying thermal oxide layer, the replacement of the thermal oxide with an Al_2O_3 layer would also improve the thermal conductivity. By combining these technologies in the Ge laser design and fabrication, dramatic improvement in laser performance is expected.

Modification of the current cavity design is also necessary. In this work, only multi-mode lasing has been demonstrated. This was attributed to the number of possible modes in the broad gain spectrum (fsr = 8 nm, gain band width of ~50 nm). A decrease in the nanowire length and cavity length are expected to suppress the multi-mode lasing behaviour, where fewer possible modes can undergo the amplification and thus lead to a full single-mode oscillation [181].

Meanwhile, quantitative analysis of the heterogeneity Ge nanowire structure on GOI will be useful for a more realistic model to study the optical field and strain strength in the nanowire. This study will provide a better understanding of the lasing action.

Integration of III-V Photonics on GOI

The III-V photonics performance is also highly dependent on the GOI quality. Group III-V materials are especially very sensitive to TDD. Therefore, a reduction in the TDD of the GOI is key to ensure reliable LED performance, and it would show great promise to integrate III-V lasers on GOI in the near future. However, the epitaxy quality of the III-V photonics on GOI is not the only issue in the integration processes. The cross-contamination between III-V and CMOS, the CMOS-compatible contacts for III-V photonics and the light wave-guiding and coupling all need to be considered to enable a practical design for the photonic integrated circuit.

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