Analysis and design of high-speed digital-to-analog converters

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2018

Juanda. (2018). Analysis and design of high-speed digital-to-analog converters. Doctoral thesis, Nanyang Technological University, Singapore.

<http://hdl.handle.net/10356/73389>

<https://doi.org/10.32657/10356/73389>

Analysis and Design of High-Speed Digital-to-Analog Converters

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2017

Acknowledgements

First and foremost, I would like to express my sincere gratitude to Professor Joseph Chang, my Ph.D. advisor, for his guidance, support, and enthusiasm through all my years at Nanyang Technological University (NTU). He has been my advisor since my undergraduate days, and provided countless invaluable advice and extraordinary insights. I am also grateful for his thorough review and meticulous critique on the numerous drafts of this thesis and other papers that I have written. His lessons for me have gone far beyond circuits; he has taught me to be a critical, sincere, and respectable researcher. The success in this Ph.D. research program would have been impossible without him.

I would also like to express my sincere gratitude to Dr. Shu Wei, whom I have had many discussions and worked closely with on my research since my undergraduate days. I am thankful for his patient guidance and support, for his numerous suggestions and detailed comments on this thesis and other papers that I have written, and for all his mentoring efforts. It has been both enjoyable and rewarding working with him.

I would like to express my appreciation to those whom I have worked and studied with at NTU. They include Dr. Guo Linfei, Dr. Zhou Jia, Mr. Ne Kyaw Zwa Lwin, Mr. Liu Qing, Mr. Jiang Jize, Mr. Qu Yong, Mr. Sun Yin, Dr. Lin Tong, Dr. Ge Tong, Dr. Chong Kwen Siong, Mr. Kang Yang, Mr. Yu Jia, and Dr. Victor Adrian. These years would not have been enjoyable and enriching without them.

I am thankful to Prof Tony Kim Tae-Hyoung for allowing me to borrow equipment under his group, without which I may not be able to complete the measurement of my prototypes. I am also thankful to technical supports and staffs at Keysight Technologies, Cadence®, and GlobalFoundries® for their suggestions, solutions and assistance whenever I met unresolved technical/software problems.

I would also like to thank the administrative and technical staffs at NTU. Special thanks go to Mr. Sia Liang Poo, Mr. Seow Yong Hing, Ms. Lim-Tan Gek Eng, Mr. David Robert Neubronner, Ms. Eu Wan Yee, Mr. Kang Meng Fai, and Ms. Seow-Guee Geok Lian for their kind support and assistance.

Finally, special thanks go to my beloved parents and sisters. I thank them for their unconditional support, encouragement, and care throughout my life. With all my love and respect, I dedicate this thesis to my family.

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Summary

This Ph.D. thesis pertains to the investigation, design, and monolithic realization of GHz Digital-to-Analog Converters (DACs). State-of-the-art DACs rely heavily on complex digital approaches (calibrations or dynamic-element-matching (DEM)) to achieve high linearity. However, these DACs undesirably suffer from inherent drawbacks such as high switching noise, long (time) latency, and complex GHz synchronization. Consequently, GS/s DACs with innate accuracy (i.e., without calibrations or DEM) are particularly attractive. However, the design of GS/s DACs with innate accuracy is challenging as it usually involves numerous fine-tuning due to sophisticated (often intractable) design trade-offs and the degraded transistor performance at GHz. Further, the testing and verification of GS/s DACs are challenging because of the difficulty associated with the generation of high-speed digital input patterns.

To resolve some the aforesaid DAC design challenges, we investigate the relationships between several critical linearity parameters (e.g., Integral Nonlinearity (INL), Differential Nonlinearity (DNL), Spurious-Free Dynamic Range (SFDR), etc.) and the design parameters (e.g., output impedance, matching, etc.) of current-steering DAC (CS-DAC) by means of analytical analysis and comprehensive simulations. We derived an analytical relationship between the output impedance and INL, and modeled the relationship between the output impedance and SFDR. On this basis, we propose a design methodology to analytically estimate the requirements of several critical design parameters and thereafter the optimization thereto. This reduces the

number of design iterations and the ensuing design effort. Further, we propose a novel design technique to decouple the aforesaid design trade-offs, leading to the opportunity for the design of higher-optimized DACs with innate accuracy.

On the basis of the aforesaid, we present two novel GS/s DAC designs. The first is a 4-bit 10GS/s CS-DAC featuring $\text{INL}=0.16\text{LSB}$, $\text{DNL}=0.12\text{LSB}$, $\text{SFDR}>23\text{dBc}$ across the Nyquist bandwidth, and power dissipation= 30mW , for the cognitive ultra-wideband radio. These attributes are achieved primarily by the optimization of current sources based on our derivation of the relationship between the output impedance and INL, and by our proposed high-speed switch-driver circuit. Further, the CS-DAC embodies our proposed in-situ hardware efficient DPG that generates $4\times 10\text{Gb/s}$ test-data pattern to facilitate functional verification. The proposed CS-DAC achieves the highest Figure-of-Merit when benchmarked against state-of-the-art DACs.

The second DAC design is a calibration-free/DEM-free 8-bit 2.4GS/s CS-DAC featuring $\text{INL}=\pm 0.097\text{LSB}$ (equivalent to ~ 11 -bit accuracy), $\text{DNL}=-0.05/0.15\text{LSB}$, $\text{SFDR}>47.8\text{dBc}$ across the Nyquist bandwidth, and power dissipation= 26.4mW . These attributes are achieved by our proposed distributed biasing scheme which largely decouples two critical trade-offs in the CS-DAC – the trade-off between the output impedance of the current-sources and their current mismatches, and that between the current mismatches and the delay differences. To simplify the CS-DAC measurements, we propose a custom in-situ $8\times 2.4\text{Gb/s}$ DPG. The proposed CS-DAC achieves the highest Figure-of-Merit when benchmarked against state-of-the-art DACs.

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Symbols and Abbreviations

CMOS	Complementary Metal-Oxide-Semiconductor
DNL	Dynamic Nonlinearity
ENOB	Effective Number of Bits
IMD	Intermodulation Distortion
INL	Integral Nonlinearity
LSB	Least Significant Bit
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortions
f	Frequency
n	Digital-to-Analog Converter resolution
R_L	Load resistance
T	Time period
V_{TH}	Transistor threshold voltage
Z	Complex impedance
ω	Angular or radian frequency

Chapter 1

Introduction

1.1 Motivation

The digital communications system is an integral constituent of basic infrastructure in the modern information society. The global internet protocol (digital data) traffic has increased eightfold over the past five years, and is projected to increase threefold over the next five years [1]. The Cisco Visual Network Index [1] recently forecasted that the global internet protocol traffic will reach 278 exabytes/month in 2021, $\sim 2.8\times$ higher than that in 2016, and the internet protocol traffic originating from mobile devices (e.g., smartphones, tablets, Internet-of-Things, etc.) is expected to surpass the traffic originating from personal computers. As expected, the ever-increasing data is straining the spectrum resources of the digital communications system.

In view of the limited spectrum resources for wireless communications, several emerging technologies have recently been reported [2-6] in attempt to address the increasing number of users and/or data traffic. This includes the cognitive radio and millimeter-wave (mmWave). The cognitive radio potentially improves the spectrum utilization efficiency by means of exploiting underutilized spectrum segments to

accommodate more users, without violating the rights of privileged primary licensed users. The cognitive radio system does this by dynamically reconfiguring its transmitter and receiver parameters according to its current spectral environment. On the other hand, for the mmWave, as its data communication occupies the vast and underutilized spectrum region from 30GHz to 300 GHz, it facilitates multi-Gb/s throughput and high number of users [2, 6, 7].

Although virtually all signal processing in the digital communications systems is processed in the digital domain, the transmission medium across which the connections between these systems are established, is inherently analog. The digital data in the digital domain, therefore, need to be interfaced with the analog domain, by means of data conversion from the digital data to the corresponding analog signal by means of a Digital-to-Analog Converter (DAC), and vice versa by means of an Analog-to-Digital Converter (ADC). In view of high-speed digital communications, the data conversions need to be processed at commensurable (high) speed.

In high-speed digital communications systems, specifically in the transmitters therein, the DAC typically serves to interface the digital signal processing circuits with the analog radio-frequency (RF) circuits, and is required to feature wide bandwidth. The degree of the accuracy of the data conversion, i.e., the DAC linearity qualified by the Integral Non-linearity (INL), Differential Non-Linearity (DNL), Spurious-Free Dynamic Range (SFDR), Signal to Noise Ratio (SNR), Effective Number of Bits (ENOB), and Intermodulation Distortion (IMD), is dictated by the system requirements.

Present-day DACs can be generalized into two categories on the basis of their oversampling ratio (the ratio of the conversion rate to the Nyquist rate ($2\times$ signal bandwidth)): oversampling DACs (primarily delta-sigma DACs), and Nyquist-rate DACs (e.g., resistor string DACs). The conversion rate of oversampling DACs is typically substantially higher than that of the Nyquist-rate DACs, where the oversampling ratio is typically $20\times$ to $512\times$. Consequent to the high oversampling ratio, the oversampling DAC linearity is improved by means of a lower in-band quantization noise power and/or noise-shaping technique [8]. Furthermore, the oversampling is advantageous as the image frequencies are moved to higher frequencies, thereby allowing a wider filter transition band and an eased filter design [9]. Oversampling DACs are typically employed in applications where the required resolution/linearity is high (e.g., 16- to 32-bits) and where the required output bandwidth is relatively low, e.g., high-fidelity digital audio players [10]. They are, however, not preferred for synthesizing wideband signals (hundreds of MHz to a few GHz) as the required conversion rate is very high where the ensuing required speed of the transistors therein may exceed their fundamental limit (e.g., the unity current gain frequency f_T of the transistor). Furthermore, as oversampling DACs are mostly digital where their implementation is largely high-speed (RF) digital circuits, undesirable non-idealities such as jitter, clock/data skew, inter-symbol interference, crosstalk, and RF switching noise become increasingly dominant. In short, oversampling DACs are inappropriate for very high frequency applications.

On the other hand, as Nyquist-rate DACs have an oversampling ratio of 1, the speed requirement of the transistors therein for a given conversion rate is substantially alleviated. Amongst the different Nyquist-rate DAC architectures, the current-steering

DAC (CS-DAC) is reportedly [11-13] the most appropriate DAC architecture for synthesizing wideband analog outputs. Figure 1.1 depicts an ideal CS-DAC where the digital input word, $d_{n-1} \dots d_0$, selects the current-sources connections to the output load R_L . The selected currents are summed together into I_{out} that flows through R_L , and output voltage v_{out} is obtained.

Figure 1.1 An ideal binary-weighted CS-DAC

The CS-DAC is capable of very high-speed (e.g., multiple GS/s) operation largely because of its open-loop structure [14] and the inherent resistive load driving capability. For example, a reported [15] DAC based on the current-steering architecture reported conversion rate of up to 100GS/s; a review of DACs is given in Chapter 2.

At this juncture, the design art of CS-DACs is relatively mature. Nevertheless, as the specifications of the DAC are ever-increasingly high, there is as expected increasing interest within the mixed-signal design community to analyze and develop higher-speed CS-DACs with higher linearity and wider analog bandwidth. Interestingly, while the architecture and basic operating principles appear to be trivial, the practical realization of CS-DACs to achieve desired high linearity is very challenging at the operating frequencies in the multiple GS/s realm. We will now succinctly delineate some of these challenges.

The linearity of CS-DACs inevitably suffers from three primary non-ideal parameters. The first non-ideal parameter is the input code-dependent output impedance [16]. In practical CS-DACs, the current-sources are non-ideal and their output impedance is finite. As the DAC output is established by the parallel summation of the selected current-sources (see Figure 1.1), the corresponding output impedance becomes inevitably input code-dependent. Consequently, the input code-dependent output impedance compromises the DAC linearity. The degradation of the linearity is further exacerbated at high operating frequencies because the output impedance decreases substantially due to the parasitic capacitance therein.

Second, the delay differences or timing inaccuracies, for example between each of the digital control signals $d_{n-1} \dots d_0$ in Figure 1.1, introduce undesired glitches at the DAC output. Such delay differences are particularly apparent at the mid-code transition, from 011...1 to 100...0 and vice versa, because large output glitches whose peak amplitude is comparable to the output swing may occur. In GS/s CS-DACs, even a few picoseconds of delay differences could significantly deteriorate the dynamic

linearity of the DAC because the delay differences now constitute to (i.e., occupy) a significant portion of the picoseconds conversion (or clock) time period. Consequently, the layout of high-speed CS-DACs is very challenging because the delay differences depend on many factors, including the matching of the driving strength of the synchronization registers and their load impedance, the matching between the interconnection routing length and shape, the magnitude and effects of cross-talk and digital switching noises, etc. There are also other types of delay differences [17] that affect the DAC linearity.

Third, the current mismatch (due to the random process variations and the process gradient) between the current-sources is particularly undesirable. Because these current-sources are fundamental elements of the DAC analog output (see Figure 1.1), their matching, in part, determines the linearity and the accuracy of the DAC. As expected these current mismatches lead to both static and dynamic linearity errors, and affect the manufacturing yield of DACs (for a given required linearity).

Several design techniques to mitigate the said non-ideal parameters have been reported, including calibration [18-20], dynamic-element-matching (DEM) or randomization [21-23], data averaging, etc. These techniques, while effective for DACs operating at low MHz frequency, are generally ineffective in GS/s DACs. This is largely because the matching problem is no longer the only limiting factor [24]. For example, calibrations constrain the DAC operating speed as it typically involves additional parasitic capacitance at the DAC output [18]. DEM [23], on the other hand, involves relatively slow and complex digital circuits, including a thermometer decoder

and DEM shufflers, which undesirably increase the DAC latency, hardware complexity, and power dissipation.

In addition to the aforesaid three non-ideal parameters, there are inevitable trade-offs between these parameters which further exacerbate the complexity of the design and optimization of CS-DACs, particularly at GHz operation. The two major trade-offs are as follows.[†] The first trade-off is between the output impedance and the current mismatches. The general approach to mitigate the current mismatch is to enlarge the transistor size [13, 25, 26], but this undesirably reduces the output impedance at high frequencies. As this trade-off is increasingly constrained when the operating frequency increases, there is a need to precisely estimate the contradictory requirements of the output impedance and the current matching.

The second trade-off is between the current mismatches (particularly due to process gradient) and the delay differences. To compensate the process gradient errors, complex routing schemes [27] that employ a current-source (or current-cell) matrix are generally used. These schemes, however, may inadvertently increase the delay differences in view of complex routing interconnections. Put simply, the concurrent optimization of all three non-ideal parameters for CS-DACs is generally intractable, largely because the optimization is constrained by the trade-offs between these parameters, and the said constraints become increasingly exacerbated at high (GHz) frequencies.

[†] The other design trade-offs include the trade-off between the power dissipation and operating speed, the trade-off between the chip area and current matching, etc.

In view of the constrained design space due to the aforesaid non-ideal parameters and their trade-offs, there is a need for a more precise estimation of the required design parameters to reduce the number of design iterations and the ensuing design effort. In the reported [28] approximation of the required output impedance for a particular INL, it is assumed that the output impedance is much greater than the load impedance. The said condition, however, may not be satisfied for example in low- to mid-resolution GS/s DACs in part because of the output impedance degradation at high frequencies and the constraints on the transistor size imposed by the required current matching. In view of this, there is a need to investigate a precise relationship between output impedance and INL without assuming that the output impedance is very high.

Similarly, the reported [9, 29] relationship between the output impedance and SFDR is still largely incomplete; the SFDR of a DAC is defined as the ratio between the magnitude of the output signal (a single tone sinusoidal wave) and the largest spurious signal. Consider the following as a case in point. The SFDR is insufficient to determine the frequency of the largest spurious signal which could be the third order harmonic distortion (HD₃), or other harmonics distortions or non-harmonics [9]. Despite this uncertainty, the SFDR of a differential output DAC is generally assumed [9, 30, 31] to be limited by HD₃ as expressed in Equation (1.1).

$$\text{SFDR(dB)} \approx 40 \log_{10} \left[\frac{4|Z_o|}{N|Z_L|} \right] \quad (1.1)$$

where Z_L is the load impedance (Ω),

Z_o is the output impedance of a unit current-source (Ω), and

$N = 2^n - 1$, and

n is the resolution of the DAC (bit).

On the other hand, other reported analysis [32] on the SFDR of an ideal n -bit DAC where the current-sources therein are assumed to be ideal, asserted that the SFDR is approximately a function of the resolution n of the DAC as expressed in Equation (1.2) and verified by computer simulations. As Equation (1.2) expresses the SFDR of an ideal DAC, this SFDR is the upper (best-case) limit.

$$\text{SFDR(dB)} \approx 8.2n + 2.2 \quad (1.2)$$

Note, however, that Equation (1.1) may be inconsistent with Equation (1.2), in part because of the assumptions assumed in Equation (1.1). Specifically, according to Equation (1.1), the SFDR can be increased indefinitely by increasing Z_o . This is inconsistent with Equation (1.2), and also with computer simulations on ideal DACs, because the SFDR is finite and is also limited by the resolution of the DAC [32]. Therefore, Equation (1.1) may overestimate the achievable SFDR of an n -bit practical CS-DAC and consequently the corresponding Z_o therein could potentially be over-designed, i.e., with excessive margins that would not yield an improved SFDR. Such over-design is undesirable particularly in the GS/s CS-DACs because their critical design parameters are already highly and increasingly constrained by the aforesaid non-ideal parameters and their trade-offs. In view of this, and for completeness, there is need to derive or model a more precise relationship between Z_o and the SFDR of CS-DACs to ascertain the available headroom of the critical design parameters and to reduce the design iteration cycles of GS/s CS-DACs.

At this juncture, the effects of the cross-correlations between current-sources on the linearity of CS-DACs remain largely unreported. In literature [16, 33], the said cross-correlation coefficients are often assumed to be negligible (i.e., uncorrelated) for the derivations of the required transistors sizes or the manufacturing yields based on a set of specifications, e.g., INL. However, this assumption is inappropriate for some CS-DACs. For example, in CS-DACs that employ the current-splitting [20] or R - $2R$ techniques [28], the aforesaid cross-correlation coefficients are not negligible as the output currents are based on the same current-sources or references – this is also intuitive. In view of this, it is important to investigate the aforesaid cross-correlations and their effects on the performance of CS-DACs.

In addition to the challenging design issues of GS/s DACs, their measurements and verification are also challenging. Consequent to a DAC conversion rate of multiple GHz, a digital pattern generator (DPG) with an appropriate high data rate (multiple Gb/s) is needed to provide the test pattern data for the DAC input. As the high data rate external DPG is costly and largely unavailable (to us), there is a need to develop a test platform or circuit to facilitate the DAC tests and measurements. Reported techniques to generate Gb/s digital patterns without expensive DPGs typically involve a complex in-situ test circuit such a digital-signal processor [34], a random access memory (RAM) with a high-speed time-interleaving circuit [12], etc. Such circuits, however, require relatively large chip area, high pin count, additional auxiliary circuits (e.g., phase-locked loop (PLL), clock dividers, digital counter, etc.) as well as high-speed input/output (I/O) buffers. The design of such in-situ test circuits is complex, requiring significant effort and resources, and the hardware cost (e.g., integrated circuit (IC)) is considerable.

In summary, there are compelling motivations to improve the performance of GS/s DACs, particularly CS-DACs for the next generation high-speed communications systems. Of specific interest, there is a need for precise analytical investigations on the critical CS-DAC design parameters (e.g., current-source output impedance, cross-correlations between current-sources, etc.) that affect the CS-DAC linearity. Furthermore, there is a need to investigate the aforesaid seemingly intractable trade-offs between non-ideal parameters in CS-DACs, and derive an analytical approach to improve CS-DAC linearity by alleviating or partially decoupling the aforesaid trade-offs. To assist the tests and measurements of high-speed CS-DACs, there is also a need for a custom in-situ high data-rate DPG with relatively simple and small hardware overheads.

1.2 Objectives

In view of the aforesaid motivations, the overall objectives of this Ph.D. research program pertain to the analysis and practical design of high-speed (GHz) CS-DACs for the next generation high-speed digital communications systems. The specific objectives are:

- (i) To analytically investigate the critical design parameters which limit the linearity (e.g., INL, SFDR, etc.) of high-speed (GHz) CS-DACs. This includes ascertaining the mechanisms that affect the performance of CS-DACs, and providing an analytical basis for the optimization of the non-ideal parameters at GHz;

- (ii) To propose a novel technique/scheme to mitigate the aforesaid non-ideal parameters in CS-DACs and/or to largely decouple their trade-offs. This includes the design of GS/s CS-DACs embodying novel techniques/schemes to simultaneously achieve high static (low INL and low DNL) linearity and high dynamic linearity (high SFDR) at GHz frequency;
- (iii) To propose a novel high-speed in-situ DPG to generate multiple Gb/s periodic data pattern for the tests and measurements of high-speed DACs, particularly in view of the unavailability low cost Gb/s external DPG;
- (iv) Further to (ii) and (iii), to practically realize monolithic prototypes of the proposed high-speed CS-DAC designs and the proposed high-speed in-situ DPG using a standard complementary metal-oxide-semiconductor (CMOS) 65nm process. Furthermore, on the basis of physical measurements on said prototypes, to verify the efficacy of the proposed architectures and circuits, thereby demonstrating the performance of the proposed CS-DACs.

1.3 Contributions

The contributions made thus far in this Ph.D. research program and reported herein are congruous to the specific objectives outlined above. Specifically, they are:

- (a) An investigation into the relationships between the output impedance and INL, and that between the output impedance and SFDR in CS-DACs. The contributions herein include the derivation of analytical expressions of the

aforesaid first relationship, and the comprehensive simulations and the practical model of the aforesaid second relationship. These analyses are particularly useful as they offer insights into the optimization of critical design parameters in high-speed (GHz) CS-DACs;

- (b) An investigation into the cross-correlations between the current-sources in CS-DACs. The contribution herein includes the derivation of an analytical expression of the DNL for current-sources with non-negligible cross-correlation coefficients.
- (c) The proposal and design of a switch-driver circuit that provides for high-speed control signals at the current-switches with several desirable attributes to mitigate the output glitches and the nonlinearity of CS-DACs;
- (d) The proposal and design of a novel in-situ DPG to generate high speed periodic data pattern (up to 10Gb/s per channel) to facilitate tests, measurements and verification of high-speed DACs. Compared to reported data pattern generation techniques [12], the proposed in-situ DPG features smaller hardware and lesser I/O pin overheads, simpler configuration, and generally inexpensive realization;
- (e) Further to (a), (c) and (d), the design and realization of a 4-bit 10GS/s CS-DAC monolithic prototype that embodies the proposed switch-driver in (c), including the in-situ DPG in (d) using a commercial 65nm CMOS process. On the basis of physical measurements, the proposed and designed CS-DAC achieves $\leq 0.16\text{LSB}$ INL, $\leq 0.12\text{LSB}$ DNL, and $>23\text{dBc}$ SFDR across the Nyquist bandwidth up to 4.53GHz, and features the most competitive Figure-of-Merit (FoM) over similar state-of-the-art DACs reported to-date;

- (f) The proposal of a novel distributed biasing scheme that largely decouples the trade-offs between the aforesaid non-ideal parameters in the CS-DACs;
- (g) The proposal of a novel layout placement structure to reduce the systematic errors due to process gradients. The contributions herein include the analyses pertaining to the reduction of the linear and gradient errors as the result of employing the proposed structure;
- (h) The proposal of an augmented version of the in-situ DPG in (d) to generate high speed periodic data pattern (up to 2.4Gb/s per channel) to facilitate tests, measurements and verification of high-speed DACs;
- (i) Further to (f) – (h), the design and realization of a calibration-free/DEM-free CS-DAC monolithic prototype embodying the proposed distributed biasing scheme in (f), gradient cancelation technique in (g), and the in-situ DPG in (h) using a commercial 65nm CMOS process. On the basis of physical measurements, the proposed CS-DAC features an INL of $\pm 0.097\text{LSB}$, a DNL of $-0.05/0.15\text{LSB}$, and an SFDR of 47.8dBc. The FoM of the proposed CS-DAC when benchmarked against reported state-of-the-art DACs is the highest – both for calibration-free/DEM-free DACs and for DACs requiring calibration/DEM.

1.4 Organizations of the Thesis

The remainder of this thesis is organized as follows.

In Chapter 2, a comprehensive literature review on CS-DACs is provided. A brief overview of the fundamental theory of DACs including the static and dynamic metrics is first presented. Subsequently, a literature review of classical DAC architectures on their basic operations and their suitability for the GHz operations is presented. Finally, an in-depth review on the CS-DAC architectures, including the design challenges, several non-ideal parameters, and reported design are delineated.

In Chapter 3, a 10GS/s 4-bit single-core CS-DAC is proposed, designed and monolithically realized for the cognitive ultra-wideband (CUWB) radio. The design of the proposed high-speed CS-DAC prototype is optimized in part by means of our analyses and derived expressions on the relationship between the output impedance and INL. To mitigate the output glitches of the CS-DAC, a novel switch-driver circuit is proposed to generate control signals with some desired attributes. Further, a novel high data rate in-situ DPG is proposed to assist with the CS-DAC measurements and verification. The CS-DAC monolithic prototypes are verified by means of hardware measurements and are finally benchmarked against reported state-of-the-art DACs.

In Chapter 4, a calibration-free/DEM-free 8-bit 2.4GS/s CS-DAC is proposed, designed and monolithically realized for the high-speed data communications in an aerial surveillance system. This chapter commences with a discussion on the design challenges of conventional high-speed CS-DACs, particularly the non-ideal

parameters and their inevitable trade-offs. To circumvent these trade-offs, a novel distributed biasing scheme is proposed and its operating mechanism are discussed. The adopted CS-DAC architecture and the design of critical building blocks, in part based on the investigations delineated in Chapter 3, are described. Subsequently, the design of the prototype ICs embodying said innovations are presented. To assist with the CS-DAC measurements, an augmented version of the high-speed in-situ DPG is proposed to improve the robustness when switching between two clock signals. The measurements are finally benchmarked against reported state-of-the-art DACs. The benchmarking depicts the significant improvements of the proposed CS-DAC over reported state-of-the-art DACs.

In Chapter 5, conclusions of the thesis are drawn and recommendations for future works are presented.

Chapter 2

Literature Review

This chapter provides a comprehensive and critical review of DACs and serves as a preamble to the contributions delineated in Chapters 3 and 4.

This literature review is arranged in the following manner. In Section 2.1, we succinctly delineate the fundamental theory of DACs, followed by the review of DAC performance metrics, including static and dynamic metrics. Section 2.2 provides a comprehensive review of various DAC architectures including their *modus operandi*, and the review of their advantages and disadvantages, particularly for high-speed digital communications systems. In Section 2.3, an in-depth review of the CS-DACs is provided, with emphasis on the design challenges, the inherent non-ideal parameters, and the state-of-the-art design techniques. In Section 2.4, a review of the reported techniques to measure high-speed DACs is presented. Finally in Section 2.5, the conclusions are provided.

2.1 Fundamental DAC Theory

The DAC is an electronic circuit that converts or maps the digital input word (typically binary input word) to its corresponding analog output, as depicted in Figure 2.1, based on one or multiple reference signals. In the ideal single-ended output DAC, the relationship between the binary input word and the analog output can be expressed [9] in Equation (2.1).

$$A_{out} = (b_{n-1} \cdot 2^{n-1} + \dots + b_1 \cdot 2 + b_0) \cdot A_{LSB} \quad (2.1)$$

where A_{out} is the analog output of the DAC,

$b_{n-1} \dots b_0$ is the binary input word,

n is the DAC resolution,

$A_{LSB} = \frac{A_{FS}}{2^n - 1}$ is the amplitude level corresponding to 1LSB (least significant bit), and

A_{FS} is the full-scale analog output.

Figure 2.1 Black box representation of DACs where the binary input word, $b_{n-1} \dots b_0$, is converted into analog output A_{out}

Figure 2.2 depicts the transfer function of an ideal 3-bit DAC where the analog output linearly increases as the digital input word increases, and the analog output step sizes are identical. The uniformity of the analog step sizes in part determines the DAC linearity and as expected it is typically employed in DAC static metrics (see Section 2.1.1 later).

Figure 2.2 Transfer function of an ideal 3-bit DAC

Consider now the ideal DAC in time domain [9]. The reconstruction of the analog output, $a_{out}(t)$, in time domain can be considered as a sampling process with a sampling frequency of $f_s > 2f_0$, where f_0 is the output bandwidth. There are several signal formats employed to reconstruct the analog output, including the non-return-to-zero (NRZ) and return-to-zero (RZ) formats.

In the NRZ format, the analog output $a_{out}(t)$ is held for one sampling period, T_s , before it is updated based on the subsequent digital input word, i.e., the output, $A_{out}(kT_s)$, is immediately updated to $A_{out}((k+1)T_s)$ after it was held for T_s , as depicted in Figure 2.3.

In time domain, this can be expressed as [9]:

$$a_{out}(t) = \left[\sum_{n=-\infty}^{+\infty} A_{out}(nT_s) \delta(t - nT_s) \right] \otimes \text{rect}\left(\frac{t}{T_s}\right) \quad (2.2)$$

where $\delta(t)$ is the Dirac delta function,

$\otimes$ is the convolution operator, and

$\text{rect}(t)$ is the rectangular function.

Figure 2.3 Time domain waveform of an NRZ output signal where it switches from one converted level to the next at every sampling period T_s

The frequency domain of $a_{out}(t)$ can be obtained by the Fourier transform of Equation (2.2) as follows [9]:

$$a_{out}(f) = A_{out}(f) \left[\sum_{n=-\infty}^{+\infty} \delta(f - nf_s) \right] e^{-j\pi f/f_s} \text{sinc}(f/f_s) \quad (2.3)$$

where $\text{sinc}(x)$ is the normalized sinc function.

As the DAC output frequency approaches its sampling frequency, the magnitude of $a_{out}(f)$ in the frequency response approaches zero in part because of the $\text{sinc}(f/f_s)$ term in Equation (2.3). Figure 2.4 depicts the plot of the $|\text{sinc}(f/f_s)|$ against f/f_s , where $|\text{sinc}(f/f_s)|$ decreases down to -3.9dB in the first Nyquist zone ($0 \leq f/f_s \leq 0.5$). As the sinc roll-off may lead to unwanted distortion at the DAC output, it may be compensated by means of inverse-sinc filters, digital pre-emphasis, etc [34].

Figure 2.4 Sinc roll-off in the NRZ format

In the RZ format, the DAC output is held for $T_p < T_s$ and the output is reset to zero (or a constant value) during the remainder of T_s , i.e., $(T_s - T_p)$. Thereafter, the DAC output is updated based on the subsequent digital input word, and so on, as depicted in Figure 2.5. As the output is reset to zero in every cycle, the DAC output is not affected by its preceding output. This thereby significantly reduces the associated distortions [9]. The time domain of the RZ output signal is expressed in Equation (2.4) [9].

$$a_{out}(t) = \left[\sum_{n=-\infty}^{+\infty} A_{out}(nT_s) \delta(t - nT_s) \right] \otimes \text{rect}\left(\frac{t}{T_p}\right) \quad (2.4)$$

where T_p , $\forall 0 < T_p \leq T_s$, is the time duration of which the output is held, i.e., non-zero, at every sampling period.

Figure 2.5 Time domain waveform of an RZ output signal where it switches from one converted level to zero (or a constant value) before switching to the next converted level at every sampling period T_s . The output is non-zero (except if input word is zero) for a time T_p in every T_s

Its frequency domain or the Fourier transform of Equation (2.4) can be expressed as:

$$a_{out}(f) = A_{out}(f) \left[\sum_{n=-\infty}^{+\infty} \delta(f - nf_s) \right] \frac{T_p}{T_s} e^{-j\pi f T_p} \text{sinc}(f T_p) \quad (2.5)$$

The RZ format extends the “zero” locations of the sinc function to higher frequencies, thereby reducing the sinc roll-off within the first Nyquist zone and the ensuing distortion. For example, the sinc roll-off within the first Nyquist zone for $T_p = T_s/2$ is now only down to -0.91dB . For the same output bandwidth, however, the operating frequency of the RZ DACs is effectively higher than that of NRZ DACs, which is undesirable when the required bandwidth is very wide. Furthermore, the RZ CS-DACs theoretically is less power efficient than the NRZ counterparts because the analog output does not contribute to the overall signal power during the reset phase.

2.1.1 Static Metrics

In a static sense, the primary function of a DAC is simply to map a digital input word into its corresponding analog level. Ideally, the DAC transfer function is a straight line with identical step sizes as illustrated earlier in Figure 2.2. In practical DACs, the transfer function and/or the step sizes may deviate from the ideal case and the corresponding deviations or errors are generally qualified by the offset error, gain error, DNL, and INL metrics. These static metrics will now be delineated in turn.

2.1.1.1 Offset Error

The offset error, ε_{offset} , is defined as the deviation of the analog output level when the digital input word is zero (e.g., binary code 00...0) of a practical DAC from that of the ideal counterpart [35], and it can be expressed as:

$$\varepsilon_{offset} = \frac{A_{out}|_{k=0} - A_{out-ideal}|_{k=0}}{A_{LSB}} \quad (2.6)$$

where A_{out} is the analog output level,

$A_{out-ideal}$ is the ideal analog output level,

$A_{LSB} = \frac{A_{out}|_{k=N} - A_{out}|_{k=0}}{N}$ is the analog output step size,

$N = 2^n - 1$, and

k is the decimal equivalent of the digital input word.

Theoretically, the offset error causes nonlinearity because the superposition principle does not apply. Nonetheless, the offset error does not introduce harmonics, and furthermore, it can be compensated by means of circuit techniques, including trimming or calibration [9].

2.1.1.2 Gain Error

The gain error, ε_{gain} , is defined as the deviation of the analog output slope of a practical DAC from that of its ideal counterpart [35], and it can be expressed as:

$$\varepsilon_{gain} = \frac{A_{out}|_{k=N} - A_{out}|_{k=0}}{A_{LSB}} - N \quad (2.7)$$

Figure 2.6 depicts an example of the gain error of a 3-bit DAC (assuming that there are no other errors) where the step size of a practical DAC is smaller than that of the ideal counterpart. As the gain errors do not introduce nonlinearity [9], it is typically less critical than the other static metrics, except in some applications such as in some instrumentation systems [9]. As in the case of offset errors, the gain errors can also be easily accommodated – it may be compensated with circuit techniques, including trimming or calibration.

Figure 2.6 Example of the gain error of a practical 3-bit DAC

2.1.1.3 Differential Nonlinearity (DNL)

DNL is the difference between the analog output step size of a practical DAC and that of the ideal DAC (i.e., the ideal output step size = 1LSB) in the absence of the offset and gain errors. Because there are $2^n - 1$ analog output steps in an n -bit DAC, there are also $2^n - 1$ different DNLs for each step. However, the DNL specified in literature or DAC datasheets generally refers to the worst-case DNL.

There are several ways to calculate DNLs, including by means of the best-fit and the end-line line methods. In the best-fit line method, the analog output step size is calculated based on the best fitting straight line that is typically obtained by means of linear regression. On the other hand, the end-point line method [36] employs an end-point line, i.e., a straight line that connects two end points that correspond to the output levels of $k = 0$ and $k = 2^n - 1$, to calculate the analog output step size. The end-point DNL is expressed in Equation (2.8) [36].

$$\text{DNL}_k = \frac{A_{out}|_{k=k} - A_{out}|_{k=k-1}}{A_{LSB}} - 1 \quad (2.8)$$

where DNL_k is the DNL that corresponds to k ; $\forall 1 \leq k \leq 2^n - 1$.

DNL provides information about the uniformity of the analog output steps and whether a DAC is monotonic, i.e., the analog output always increases as the digital input code is increased by 1 bit. Note that the monotonicity in a DAC is guaranteed if its $\text{DNL}_{\text{worst-case}} > -1\text{LSB}$.

2.1.1.4 Integral Nonlinearity (INL)

INL is the difference between the analog output level of a practical DAC and that of the ideal DAC in the absence of offset and gain errors. Because there are 2^n analog output levels in an n -bit DAC, there are also 2^n different INLs for each level as expressed in Equation (2.9). As in the case of DNL, the INL specified in literature or DAC datasheets generally refers to the worst-case INL.

Also similar to DNL, the INLs can also be calculated on the basis of the best-fit line or end-point line methods. The end-point INL is expressed in Equation (2.9) [36].

$$\text{INL}_k = \frac{A_{out}|_{k=k} - A_{out}|_{k=0}}{A_{LSB}} - k \quad (2.9)$$

where INL_k is the INL that corresponds to k ; $\forall 0 \leq k \leq 2^n - 1$.

Additionally, from the aforesaid required DNL to guarantee the monotonicity, the corresponding required INL is $\leq 0.5\text{LSB}$.

2.1.2 Dynamic Metrics

In a dynamic sense, the function of a DAC is to synthesize an analog waveform based on the digital input waveform. The DAC dynamic linearity metrics provide a measure of the quality of the synthesized analog output based on particular input waveforms, including the single-tone (a single sine wave), two-tone (a pair of sine waves with different frequencies), multiple-tone, and/or narrowband signals with roughly constant power within the signal band. The pertinence of the specific metric depends largely on the application of the DAC. We will now review the important dynamic metrics.

2.1.2.1 Signal-to-Noise Ratio (SNR)

SNR is defined as the ratio of the signal power to the noise power at the analog output [35], and it can be expressed as:

$$\text{SNR}_{\text{dB}} = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}}} \right) \quad (2.10)$$

where SNR_{dB} is the SNR expressed in dB (decibels),

P_{signal} is the power of a single-tone signal, and

P_{noise} is the power of the noise.

2.1.2.2 Signal-to-Noise and Distortion Ratio (SNDR or SINAD)

SNDR is defined as the ratio of the signal power to the collective power of the noise and distortion at the analog output [35], and it can be expressed as:

$$\text{SNDR}_{\text{dB}} = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{distortion}}} \right) \quad (2.11)$$

where SNDR_{dB} is the SNDR expressed in dB, and

$P_{\text{distortion}}$ is the power of the spurs/distortions.

2.1.2.3 Effective Number of Bits (ENOB)

ENOB is the effective resolution of a DAC based on its SNR or SNDR, and it can be expressed as:

$$\text{ENOB} = \frac{\text{SNR} - 1.76}{6.02} \text{ or } \frac{\text{SNDR} - 1.76}{6.02} \text{ bit(s)} \quad (2.12)$$

2.1.2.4 Total Harmonic Distortion (THD)

THD is the ratio of the power of the harmonics to the signal powers, and is expressed as:

$$\text{THD} = \frac{P_h}{P_{\text{signal}}} \quad (2.13)$$

where P_h is the power of the harmonics.

2.1.2.5 Total Harmonic Distortion + Noise (THD+N)

THD+N is a variant of THD and is usually more meaningful as it includes the noise power. When the bandwidth is equal to Nyquist bandwidth, THD+N is proportional to the reciprocal of SNDR and is expressed as:

$$\text{THD+N} = \frac{1}{\text{SNDR}} \quad (2.14)$$

2.1.2.6 Dynamic Range (DR)

The dynamic range (DR) is defined as the ratio of the largest output signal over the smallest output signal. In DACs, the DR is related to the resolution of the converter and it may be expressed as:

$$\text{DR}_{\text{dB}} = 20 \log_{10} (2^n - 1) \approx 6.02n \quad (2.15)$$

where DR_{dB} is the DR expressed in dB.

2.1.2.7 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the signal (typically a single-tone signal) to the power of the largest spurious tone within the output bandwidth. The SFDR is typically expressed in dBc (decibels relative to the carrier) and it may be expressed as:

$$\text{SFDR}_{\text{dBc}} = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{spur}}} \right) \quad (2.16)$$

where SFDR_{dBc} is the SFDR expressed in dBc, and

P_{spur} is the power of the largest spurious tone within the output bandwidth.

2.1.2.8 Intermodulation Distortion (IMD)

IMD is a useful measure to characterize the linearity of the DAC within and near the output bandwidth. This is because higher order harmonics are generally filtered out by image-rejection filters. IMD occurs when the input is a two- or multi-tone signal. For a two-tone test with fundamental frequencies f_1 and f_2 , the DAC non-linearity will introduce a number of additional tones, i.e., distortion, at frequencies of $k_1 \cdot f_1 + k_2 \cdot f_2$, where k_1 and k_2 are arbitrary non-zero integer numbers, and $f_1 \neq f_2$. These tones are the intermodulation products of order $m = |k_1| + |k_2|$ and only odd order products are close to the fundamentals, while the even order products are distant [37]. IMD of order m is defined as the ratio of the fundamentals to the products and is expressed as:

$$\text{IM}_m = 10 \log_{10} \left(\frac{P_{\text{two-tone}}}{P_{IPm}} \right) \text{ dBc} \quad (2.17)$$

where IM_m is the IMD of order m expressed in dBc,

$P_{\text{two-tone}}$ is the power of one of the two fundamental tone signals, and

P_{IPm} is the power of one of the intermodulation products.

2.2 Overview of DAC Architectures

As previously mentioned in Chapter 1, DAC architectures may be classified into two groups based on their oversampling ratio: the Nyquist-rate and the oversampling DAC [10]. We will now review the various Nyquist-rate DACs, followed by a brief overview of oversampling DACs.

2.2.1 Nyquist-rate DACs

In Nyquist-rate DACs, the output signal bandwidth f_B is equal to the Nyquist frequency, $f_N = f_s/2$, where f_s is the conversion rate of the DAC. The oversampling ratio is 1 [38]. In general, the Nyquist-rate DACs can be categorized based on:

- (i) Fundamental components: resistor based, capacitor based, and current-source based DAC architectures [10];

- (ii) Segmentation: the binary, thermometer-coded, segmented DAC architectures [36, 39]; and
- (iii) Scaling method: the voltage scaling, current scaling, and charge scaling DAC architectures [40].

As Nyquist-rate DACs may overlap across multiple categories, and in view of the need for brevity in this review, we will limit our review as follows. We will first discuss the Nyquist-rate DACs based on (i), and then succinctly review some of the Nyquist-rate DACs based on (ii) and (iii).

2.2.1.1 Resistor based DACs

In resistor based DACs, resistors are the fundamental components in the digital-to-analog conversion. Resistor based DACs include the resistor string DACs, binary-weighted resistor DACs, thermometer based resistor DACs, and R - $2R$ DACs.

Resistor String DACs

In resistor string DACs, one or multiple strings of resistors (i.e., resistors connected in series) are employed to derive multiple reference levels (i.e., tap voltages) from a reference voltage, V_{REF} , for data conversion.

Figure 2.7 depicts the schematic diagram of a resistor string DAC where the resistor string consists of n unit resistors R_u connected in series to obtain N tap voltages, $V_N \dots V_0$, from V_{REF} , where $N=2^n-1$. Based on the digital input word, $b_{n-1} \dots b_0$, the switch network selects and connects one of these tap voltages to the operational amplifier (Op-Amp) which operates as an output buffer. The output buffer is typically needed in a resistor string DAC to drive the output load, and also to isolate the resistor string from the load.

Figure 2.7 Schematic diagram of a resistor string DAC

There are several variations of the resistor string DACs which employ different switch network designs such as binary tree switches [10, 35, 36], X - Y network [36], switch network with the digital decoding, etc. Further, there is also a resistor string DAC

which employs multiple stages (or multiple resistor strings) to perform data conversion [41].

While the resistor string DACs are attractive for mid- to high-resolution as its architecture is simple and generally monotonic, its conversion rate is relatively low. As the resolution increases by 1bit, the complexity of the switch network and the number of unit resistors may increase exponentially, resulting in longer propagation delay and hence slower conversion rate. Furthermore, the design of an Op-Amp is challenging when the required bandwidth is in GHz, in part because the transistors gain decreases at RF. In view of these drawbacks, the resistor string DACs are inappropriate for high-speed (GHz) applications.

Binary-weighted Resistor DACs

The binary-weighted resistor DAC features simple hardware and a small number of components. Figure 2.8 depicts the schematic diagram of a binary-weighted resistor DAC [36] where it consists of binary-weighted resistors ($R_u, 2R_u, \dots, 2^{n-1}R_u$), a feedback resistor R_F , and an Op-Amp. It employs the binary-weighted resistors to generate binary-weighted currents for data conversion. One end of these resistors is connected to the virtual ground created by the negative feedback configured Op-Amp. Based on the input word, $b_{n-1} \dots b_0$, the other end of the selected resistors is connected to V_{REF} and their currents are summed together into I_{out} that flows through R_F . The voltage developed across R_F is the output voltage.

Figure 2.8 Schematic diagram of an n -bit binary-weighted resistor DAC

The operating speed of this architecture is potentially fast, however it may be limited by the bandwidth of the Op-Amp. Furthermore, it is difficult to design an op-amp with bandwidth of several GHz.

Thermometer-code Resistor DACs

The thermometer-code resistor DAC employs control signals represented in thermometer codes, a code where the number of asserted bits represents the decimal equivalent of the corresponding binary code. Table 2.1 tabulates the truth table of a binary-to-thermometer decoder (3-to-7) that converts 3-bit binary codes into 7-bit thermometer codes. As the binary input increases by 1 bit, the number of asserted

thermometer-code bits will also increase by 1 bit, akin to the behavior of the mercury thermometer when the temperature rises.

Table 2.1 Truth table of a binary-to-thermometer (3-to-7) decoder

Binary Code			Thermometer Code						
b_2	b_1	b_0	t_6	t_5	t_4	t_3	t_2	t_1	t_0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Figure 2.9 depicts the schematic diagram of an n -bit thermometer-code resistor DAC [36] where it consists of $N=2^n-1$ unit resistors R_u , a feedback resistor R_F , a binary-to-thermometer decoder, and an Op-Amp. It employs a binary-to-thermometer decoder to convert the binary input word, $b_{n-1}\dots b_0$, into the thermometer-code word, $t_{N-1}\dots t_0$. Based on $t_{N-1}\dots t_0$, the other end of the selected unit resistors is connected to V_{REF} and their currents are summed together into I_{out} that flows through R_F . The voltage developed across R_F is the output voltage.

Compared to the binary-weighted resistor DAC, the thermometer-code resistor DAC features improved linearity, reduced glitch energy, and guaranteed monotonicity. However, as the resolution increases by 1 bit, the complexity of the binary-to-

thermometer decoder exponentially increases and this may increase the propagation delays of the digital circuits which in turn may limit the DAC speed. Furthermore, similar to the binary-weighted resistor DACs, the operating speed of this architecture may also be limited by the bandwidth of the Op-Amp therein.

Figure 2.9 Schematic diagram of an n -bit thermometer-code resistor DAC where

$$N=2^n-1$$

R-2R DACs

The R -2 R DACs employ an R -2 R ladder, a resistor configuration where there are only two resistance values with a ratio of 1:2, to derive binary-weighted voltages or currents from a reference source. Figure 2.10 depicts the schematic diagram of a voltage-mode R -2 R DAC. In the voltage-mode version, the R -2 R ladder operates a voltage divider that divides V_{REF} on the basis of the binary input word. The ensuing divided voltage at the V_+ node is subsequently buffered by the output buffer to drive the output load.

Figure 2.10 Schematic diagram of a voltage-mode R - $2R$ DAC

Figure 2.11 depicts the schematic diagram of a current-mode R - $2R$ DAC. In the current-mode version, the R - $2R$ ladder derives binary-weighted currents from I_{REF} . Based on the digital input word, the switches combine the current of the selected resistors into I_{OUT} that flows through R_2 to form V_{OUT} [10], while the current of the remaining resistors is simply terminated to ground.

Figure 2.11 Schematic diagram of a current-mode R - $2R$ DAC

Summary of Resistor based DACs

While the resistor based DACs can potentially achieve high linearity for mid- to high-resolution conversions, their operating speed is relatively slow. In resistor based DACs, there is a need for an Op-Amp to buffer the weak analog signal, or create a virtual ground, or perform a summation function, etc. Consequently, the overall DAC conversion rate is largely limited by the Op-Amp bandwidth. Further, the conversion rate of resistor based DACs is also limited by other factors, including the RC time constants of the circuit nodes, the complexity of the switch network, and the decoder speed.

Put simply, the resistor based DACs are largely inappropriate for applications that require wide bandwidth, such as multiple GHz bandwidth.

2.2.1.2 Capacitor based DACs

In capacitor based DACs, capacitors are the fundamental components for digital-to-analog conversion. The operating principle is generally based on the switched-capacitor (SC) approach [36]. Some of the capacitor based DACs include the binary charge-redistribution DACs, and the thermometer-code charge-redistribution DACs.

Binary charge-redistribution DACs

The binary charge-redistribution DACs are basically the switched-capacitor (SC) version of the aforementioned binary resistor DACs. Because of the SC operation, the binary charge-redistribution DACs may adopt well-established SC techniques such as offset cancellation or calibrations [10] to obtain higher accuracy and linearity.

Figure 2.12 depicts the schematic diagram of a simple binary charge-redistribution DAC where it consists of n binary-weighted capacitors ($C_u, 2C_u, \dots, 2^{n-1}C_u$), a feedback capacitor C_F , and an Op-Amp. During the reset phase, Φ_{RST} , C_F is discharged to ground and the Op-Amp is set into the unity-gain configuration. During the conversion phase, Φ_{DAC} , the binary-weighted capacitors operate as a capacitive divider that divides V_{REF} into the desired analog signal at the virtual ground (V_- node) according to the binary input word. The analog signal at V_- node is then amplified by the Op-Amp with C_F as the feedback element. Analytically, the DAC output can be expressed in Equation (2.18).

$$V_{out} = -\sum_{i=0}^{n-1} \frac{b_i 2^i C_u}{C_F} \quad (2.18)$$

where C_u is the capacitance of the unit capacitor, and

C_F is the capacitance of the feedback capacitor.

Figure 2.12 Schematic diagram of a binary charge-redistribution DAC

Thermometer-code charge-redistribution DACs

Thermometer-code charge-redistribution DACs are basically the SC version of the thermometer-code resistor DACs. Similar to other charge-redistribution DACs, the thermometer-code charge-redistribution DACs may also adopt SC techniques such as the offset cancelation or calibrations [10] for a higher accuracy and linearity.

Figure 2.13 depicts the schematic diagram of a thermometer-code charge-redistribution DAC where it consists of $N=2^n-1$ unit capacitors C_u , a feedback capacitor C_F , an Op-Amp, and a binary-to-thermometer decoder. In this DAC, the binary input word $b_{n-1}\dots b_0$ is converted by the binary-to-thermometer decoder into the

thermometer-code word $t_{N-1} \dots t_0$. During the reset phase, Φ_{RST} , C_F is discharged to ground and the Op-Amp is set into the unity-gain configuration. During the conversion phase, Φ_{DAC} , the unit capacitors operate as a capacitive divider that divides V_{REF} into the desired analog signal at the virtual ground (V_- node) according to $t_{N-1} \dots t_0$. The analog signal at V_- node is then amplified by the Op-Amp with C_F as the feedback element. Analytically, the DAC output is expressed as:

$$V_{out} = - \sum_{i=0}^{N-1} \frac{t_i C_u}{C_F} \quad (2.19)$$

Figure 2.13 Thermometer-code charge-redistribution DAC where $N=2^n-1$

Summary of Capacitor based DACs

As the on-chip capacitors generally have good matching attributes, similar to resistor based DACs, capacitor based DACs are appropriate for mid- to high-resolution application. Also similar to resistor based DACs, their speed is relatively slow as it is constrained by the Op-Amp bandwidth, slew rate, and the RC time constants.

2.2.1.3 Current-source based DACs

This category includes the CS-DAC architectures where current-sources are the fundamental components in the digital-to-analog conversion. As CS-DACs are the primary interest in this Ph.D. thesis for their speed advantages, they will be reviewed in depth in Section 2.3 later.

2.2.1.4 Other DAC Categories/Classifications

As mentioned earlier, there are several ways to categorize Nyquist-rate DACs. Apart from the categories reviewed in Section 2.2.1.1 to 2.2.1.3, several Nyquist-rate DACs feature attributes that overlap across different categories. In this section, we will briefly review these other reported DAC categories.

Binary DACs

In binary DACs [21], the fundamental components therein (resistors, capacitors, or current-sources) are employed to obtain binary-weighted electrical quantities (e.g., voltages and/or currents, etc.). Based on the binary input word, these binary-weighted electrical quantities are thereafter selected or combined to establish the analog output signal. Examples of the binary-scaled DAC include the aforesaid binary-weighted resistor DAC, the binary charged-redistribution DAC, etc.

Thermometer-code DACs

In thermometer-code DACs, the fundamental components (resistors, capacitors, or current-sources) are employed to obtain equally weighted electrical quantities (e.g., voltages, currents, etc.). A thermometer-code word is employed, instead of the binary-code word, to select or combine these equally weighted electrical quantities to form the analog output signal. Examples of the thermometer-code DACs include the thermometer-code resistor DACs, the thermometer-code charge-redistribution DACs, etc.

Hybrid DACs

The different types of DAC architectures have common and unique features including their advantages and disadvantages. In reported attempts to design DACs that do not suffer from the disadvantages/shortcomings of the individual DAC architectures, the

different architectures may be combined. As there are many possible combinations, there are potentially many different hybrid DACs, and with different attributes.

Examples of hybrid DACs include the resistive-capacitive DACs [10, 36], the segmented CS-DACs, etc. The hybrid resistive-capacitive DAC [10] is a DAC that combines the resistor based and the capacitor based DAC architectures, typically for higher resolution and linearity. The segmented CS-DAC is a hybrid DAC that combines two different current based (or current-steering) architectures. Because of its relevance in this Ph.D. thesis, the segmented CS-DAC will be discussed in greater detail in Section 2.3 later.

2.2.2 Oversampling DACs

As mentioned earlier, the conversion rate of oversampling DACs is substantially higher than the Nyquist rate where the oversampling ratio is typically $20\times$ to $512\times$ [36]. Unlike the Nyquist-rate DACs, the oversampling DAC, including the $\Sigma\Delta$ (or $\Delta\Sigma$) DAC architectures, could employ the noise shaping technique to increase the linearity of its output signal.

Unlike most of the Nyquist-rate DAC architectures, oversampling DACs are largely digital. Figure 2.14 depicts the block diagram of an oversampling ($\Sigma\Delta$) DAC. In this DAC, the n -bit input digital word is first fed to a digital interpolation filter where the sampling rate is increased from f_N to $k \times f_N$, and k is the oversampling ratio. The $\Sigma\Delta$ modulator performs the noise-shaping on its digital input data stream and reduces the

sample width to one bit that is converted into an analog signal V_{out} by the 1-bit DAC. Finally, the unwanted shaped quantization or out-of-band noise of the V_{out} are filtered by the output [10] and the in-band output linearity is improved.

Figure 2.14 Block diagram of an oversampling DAC

The oversampling DACs are typically employed in applications that require high linearity such as high-fidelity digital audio systems. However, because of its conversion rate is much higher than the Nyquist rate, it is extremely challenging to realize the oversampling DACs with multiple GHz bandwidth for high-speed communications systems.

2.3 A Review of CS-DACs

CS-DACs are the primary interest in this Ph.D. thesis and a basic CS-DAC schematic was earlier depicted in Figure 1.1. In the current-steering architecture, the digital input word switches or steers currents toward one of the output nodes to synthesize an analog output [9]. As its analog output is effectively in the form of current, the current-steering architecture can directly drive resistive load without the need for additional buffers [13, 42]. This feature is particularly attractive for high-speed operation because the DAC conversion speed is not constrained by the bandwidth of output buffers. In addition to the resistive load driving capability, the high-speed operation can in part be attributed to the absence of high impedance nodes and its open-loop structure.

Based on how the current-sources are sized and switched, the CS-DAC can be categorized into three general groups: binary, unary, and segmented CS-DACs. We will now delineate the basic operating principle of these CS-DACs, including a summary of their performances. Thereafter, the non-ideal parameters in the CS-DACs are reviewed, followed by a review of reported design techniques in CS-DACs. Finally, a survey of state-of-the-art high-speed CS-DACs is presented and discussed.

2.3.1 Binary CS-DACs

The binary CS-DAC, as its name implies, employs binary-weighted current-sources where the magnitude of the current-source of a particular bit is $2\times$ its preceding bit. These binary-weighted current-sources can be implemented by:

- (i) Scaling the aspect ratio of the current-source transistors [9, 43],
- (ii) Arranging multiple unit current-sources in a parallel combination [14],
- (iii) Employing a current splitter topology [20, 44] where the current of a current-source is split into multiple binary-weighted currents,
- (iv) Employing an R - $2R$ ladder [28, 34, 45], and
- (v) Combination of the aforesaid methods (i) – (iv) [9, 46, 47].

Method (i) features less interconnect parasitics and smaller area than the other methods, but it suffers from poor matching as there are many different channel widths. Method (ii) improves the current-source matching by sacrificing a relatively small increase in interconnect parasitics and area. Method (iii) can potentially reduce current errors as it ensures that the total current is relatively constant. Method (iv) is often adopted by CS-DACs that employ bipolar junction transistors (BJTs) to minimize the number of BJTs, in part because the layout of high density BJTs is relatively more difficult to implement than its CMOS counterparts [9]. Method (v) involves a combination of the aforesaid methods which potentially exploits their individual advantages and possibly mitigates the disadvantages.

Figure 2.15 depicts an n -bit binary CS-DAC where each bit of the binary input word, $b_{n-1} \dots b_0$, directly controls its corresponding current-source thereby resulting in fast operation, small hardware size, and low power dissipation. Analytically, the differential output voltage, V_{out} , of the binary CS-DACs can be expressed as:

$$V_{out} = R_L \sum_{i=0}^{n-1} b_i I_i - R_L \sum_{i=0}^{n-1} \overline{b_i} I_i \quad (2.20)$$

where b_i are the binary word bits,

$\overline{b_i}$ are the bit-wise complement of b_i ,

n is the DAC resolution,

$I_i = 2^i I_u$ are the binary-weighted currents, and

$I_u = I_{LSB}$ is the unit (LSB) current.

Figure 2.15 Schematic diagram of an n -bit binary CS-DAC

Nevertheless, despite the said attractive features, this architecture suffers from relatively poor linearity, in part due to significant glitch errors and poor matching of the current-sources [35].

2.3.2 Unary CS-DAC

In unary CS-DACs, identical unit current-sources are employed instead of binary-weighted current-sources. Consequently, the binary input word needs to be converted into the thermometer-code word to control these unit current-sources.

Figure 2.16 depicts the schematic diagram of a unary CS-DAC where the binary-to-thermometer decoder converts the binary input word, $b_{n-1} \dots b_0$ into the corresponding thermometer-code word, $t_0 \dots t_{N-1}$, which determines the connections of the $N=2^n-1$ unit current-sources to the output nodes. Analytically, the differential output voltage, V_{out} , of the unary CS-DACs can be expressed in Equation (2.21):

$$V_{out} = R_L \sum_{i=0}^{N-2} t_i I_u - R_L \sum_{i=0}^{N-2} \bar{t}_i I_u \quad (2.21)$$

where t_i are the thermometer-code word bits, and

$\bar{t}_i$ are the bit-wise complement of t_i .

Figure 2.16 Schematic diagram of an n -bit unary CS-DAC where $N=2^n-1$

There are several reported ways to implement the binary-to-thermometer decoder and they can be generalized into two methods. The first method involves the design of combinational logic for each thermometer-code bit [48]. This method is, however, inappropriate for mid- to mid-high-resolution DACs due to the digital complexity as the number of different combination logic doubles for each 1-bit increase in resolution [49].

The second method [16, 50] involves employing a matrix decoder comprising row, column, and local decoder, to reduce the digital complexity. This method can potentially improve the matching performance of the current-sources as their placement (in a matrix) is closer to each other.

The unary CS-DAC features a guaranteed monotonicity, relaxed current-source matching, and reduced glitches [16]. Nevertheless, the main disadvantages of this

architecture include relatively slow and complex digital circuits, in part due to the highly complex thermometer decoder for mid- to mid-high-resolution [13]. Further, the layout implementation of the complex digital decoding circuit operating at high-speed is challenging as the utilization of an automatic place and route software is largely inappropriate for circuits operating at several GHz. Not unexpectedly, this architecture is typically employed for low-resolution coarse sub-DACs in segmented CS-DACs [51, 52].

2.3.3 Segmented CS-DAC

The segmented current-steering architectures [51, 52] combine the binary and unary versions to exploit their individual advantages for a better trade-off DAC performance. In this approach, the total input digital bits are divided into several groups and a certain current-steering architecture is applied to each group. The unary architecture which has higher accuracy and linearity than the binary counterpart is usually applied to the coarse sub-DAC(s) associated with the more significant bits. The binary architecture which has relatively lower complexity and higher conversion rate, on the other hand, is usually applied to the fine sub-DAC(s) associated with the lesser significant bits as they have less impact on the accuracy and linearity of DAC. By appropriately selecting the number of bits in this architecture between unary and binary parts, the performance of the DAC can potentially be better designed to meet the desired specifications [52].

2.3.4 Non-ideal Parameters in CS-DACs

In this section, we will succinctly review the primary design problems in the implementation of CS-DACs.

2.3.4.1 Input Code-dependent Output Impedance

In practical CS-DACs, the DAC output impedance is finite and is equal to the parallel combination of the output impedance of the selected (or non-selected) current-sources. Hence, the DAC output impedance depends on the digital input word that controls the current-sources connections to the DAC output nodes [25]. The input code-dependent output impedance is a shortcoming of CS-DAC as it may distort the DAC output. Its impact is typically mitigated by increasing the output impedance of the current-sources for example by employing the cascode topology [14]. Nevertheless, as the DAC operating speed increases to several GHz, it becomes more difficult to obtain high output impedance. As frequency increases, the parasitic capacitance effect becomes more dominant and degrades the overall output impedance.

In single-ended output CS-DACs, the relationship between the INL and the output resistance of the unit current-source can be estimated from [28]:

$$\text{INL}_{\text{SE},pk} \approx \frac{N^2 R_L}{4r_o} \quad (2.22)$$

where $\text{INL}_{\text{SE},pk}$ is the peak INL of a single-ended output DAC,

$$N = 2^n - 1,$$

n is the DAC resolution,

r_o is the output resistance of a unit current-source, and

R_L is the load resistance.

In differential output CS-DACs, the relationship between the INL and the output resistance of the unit current-source can be estimated from [30]:

$$\text{INL}_{\text{DE},pk} = \frac{-g_l g_o^2 k(2k - N)(N - k)}{2(g_l^2 + g_l g_o N + g_o^2 kN - g_o^2 k)(g_l + N g_o)} \bigg|_{k=\frac{N}{4}, \frac{3N}{4}} \quad (2.23)$$

where $\text{INL}_{\text{DE},pk}$ is the peak INL of a differential output DAC,

$$g_o = 1/r_o, \text{ and}$$

$$g_l = 1/R_L.$$

Note that both Equations (2.22) and (2.23) assume that $r_o \gg NR_L$. Furthermore, these equations also assume the k values that correspond to the INL peak values, i.e., $k = N/2$ and $k = N/4, 3N/4$ for the single-ended output and differential output CS-DACs respectively. When these assumptions become invalid, the accuracy of these reported relationships may become unacceptable.

2.3.4.2 Current Matching

The mismatch between current-sources is one of the error sources in CS-DACs. The current mismatch is primarily due to the random process variations and the gradient effects [33]. In this section, we will briefly review these two error sources.

Random Process Variation

Variations of the parameters, e.g., oxide thickness, doping concentrations, of a fabricated device (transistors, resistors, etc.) may cause the value of the given fabricated device to deviate from its nominal value [33]. Two devices of the same design could hence have different values although they are designed to be identical.

In MOS transistors, the current mismatches are largely due to the mismatches in the threshold voltage, V_{TH} , and the current factor, β [33, 53]. The mismatch in V_{TH} of a pair of equally sized transistors can be expressed [33, 53] as:

$$\sigma_{\Delta V_{TH}}^2 = \frac{A_{V_{TH}}^2}{W \cdot L} \quad (2.24)$$

where $\sigma_{\Delta V_{TH}}^2$ variance of the ΔV_{TH} of a pair of equally sized transistors,

$A_{V_{TH}}$ is the threshold voltage matching constant,

W is the transistor gate width, and

L is the transistor gate length.

The mismatch in β of a pair of equally sized transistors can then be expressed [33, 53] as:

$$\frac{\sigma_{\Delta\beta}^2}{\beta^2} \approx \frac{A_\beta^2}{W \times L} \quad (2.25)$$

where $\sigma_{\Delta\beta}^2$ is the variance of $\Delta\beta$ of a pair of equally sized transistors, and

A_β is the current factor matching constant.

Considering only the V_{TH} and β mismatches, the mismatch in the drain current, I , of a pair of equally sized MOS transistors (in the strong inversion region) can be expressed [33, 53] as:

$$\frac{\sigma_{\Delta I}^2}{I^2} = \frac{4\sigma_{\Delta V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_{\Delta\beta}^2}{\beta^2} \approx \frac{1}{W \times L} \left[\frac{4A_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} + A_\beta^2 \right] \quad (2.26)$$

where $\sigma_{\Delta I}^2$ is the variance of ΔI of a pair of equally sized transistors, and

V_{GS} is the gate-source voltage.

We can infer from Equation (2.26) that the current mismatches can be reduced by three different approaches. The first approach is by increasing the transistor gate area ($W \times L$). This approach, however, leads to a higher parasitic capacitance that is particularly undesirable in the current-sources because, as mentioned in Section 2.3.4.1, it degrades the output impedance at high frequencies. The second approach is by increasing V_{GS} to increase the gate overdrive voltage ($V_{GS} - V_{TH}$), but it is limited by the supply voltage and/or the available voltage headroom. The third approach is by

employing devices that have better matching coefficients (A_{VTH} or A_β) that may involve higher cost process or it may not be available.

In addition to the aforesaid approaches to mitigate the current mismatches, there are other techniques to improve the current matching such as calibrations. Furthermore, the impact of the current mismatches can also be mitigated, without improving the current matching, with digital techniques such as DEM, averaging, etc. The calibration and DEM techniques in CS-DACs will be delineated later in Sections 2.3.5.1 and 2.3.5.2, respectively.

Gradient Effect

Gradients can occur due to the manufacturing (systematic) deviations (e.g., doping gradient, oxide thickness gradient, etc.), the voltage (IR) drop across the interconnect metals that connect the power supplies and core circuits, temperature gradients, etc [33].

The gradient effects are typically mitigated by means of layout and placement (e.g., common centroid [33, 54]), switch sequencing techniques (e.g., Q^2 random walks [55, 56]), etc. The gradient cancelation techniques will be delineated later in Section 2.3.5.3.

2.3.4.3 Delay Differences

Delay differences may be [17, 57] classified as either the cell-dependent delay differences or the output-dependent delay differences.

Cell-Dependent Delay Differences

Cell-dependent delays [57] are delays that are independent of the output values, including the delays from the clock pad to the back-end latches/current-switches, and the delays from the back-end latches/current-switches to the output node.

These delays largely depend on the layout implementation, particularly the placement of the DAC building blocks and their routing interconnections. For example, at the transmission end of the output lines, each current will propagate through some distance from the current-switches to the output load. Depending on the physical layout placements and routings, the delay differences for each current at the load are increasingly dominant at high frequencies and would affect the DAC linearity. The reported [57] contribution of this error source to the DAC SFDR is expressed in Equation (2.27).

$$\text{SFDR} = \frac{4(1 + 4\omega_o^2\tau^2)}{\tau_{\max}\omega_o \cos(\pi\omega_o/\omega_s)\sqrt{1 + \omega_o^2\tau^2}} \quad (2.27)$$

where τ is the output time constant (i.e., the cell-dependent delay difference model [57]),

$\tau_{\max}$ is the maximum time constant variation,

$$\omega_o = 2\pi f_o,$$

$$\omega_s = 2\pi f_s,$$

f_o is the output frequency, and

f_s is the conversion rate.

Similarly, if the clock signal (which determines the time instant when the cells change their state) does not reach all cells at the same time, the SFDR becomes [57]:

$$\text{SFDR} = \frac{4\sqrt{(1+4\omega_o^2\tau^2)/(1+\omega_o^2\tau^2)}}{d_{\max}\omega_o\cos(\pi\omega_o/\omega_s)} \quad (2.28)$$

where $d_{\max}$ is the maximum delay difference between the cells.

The SFDR is poorest at $f_o/f_s \cong 1/4$, and for low output frequencies ($\omega_o\tau \ll 1$), Equations (2.27) and (2.28) can be simplified into Equations (2.29) and (2.30), respectively. Note that the SFDR degrades at -20 dB/decade rate as the output frequency increases when the output frequencies are low ($\omega_o\tau \ll 1$), [57].

$$\text{SFDR} \cong \frac{4}{\tau_{\max}\omega_o} \quad (2.29)$$

$$\text{SFDR} \cong \frac{4}{d_{\max}\omega_o} \quad (2.30)$$

As the DAC resolution increases, the interconnection routing becomes increasingly complex because the number of current-sources and other blocks increases. This may

lead to substantial cell-dependent delay variations. Furthermore, the cell-dependent delay differences between cells may reach several dozens of picoseconds which are undesirable and may consequently degrade the DAC linearity [57].

Output-Dependent Delay Differences

Output-dependent delays are delays that are dependent on the variation of the output voltage [17]. The variations of the DAC output voltage causes voltage fluctuations at the current-sources output node which in turn results in the variations of the threshold levels of the current-switches. Because the state of current-switches depends on the difference between the input voltage and the threshold level, the variation of the latter causes variations in the switching delay. This switching delay variations/differences are undesirable because they may result in harmonic distortion at the DAC output, thereby deteriorating the SFDR [17].

2.3.4.4 Load Resistor Nonlinearity

The load resistor nonlinearity may distort CS-DAC output voltage [28] as it is the product of both the output current and the load resistor. The load resistor nonlinearity largely depends on the type of the resistors and the DAC operating frequency. For example, some polysilicon resistors exhibit a hyperbolic sine I - V characteristic that become more linear as the length of the resistor increases [58]. In high-speed CS-DACs, the load resistance is typically 50Ω for RF termination and matching purposes.

However, the physical resistor loads are non-ideal and not purely resistive because of the inherently parasitic elements. This may also affect the magnitude of the DAC output at different frequencies.

2.3.4.5 Differential Capacitive Charge Transfer

In CS-DACs, the input word controls the connection of the current-sources to the output nodes. Consequently, the voltage and the parasitic capacitance at the current-source output (drain) may vary according to the input word. These variations lead to charge variations ΔQ as expressed in Equation (2.31) [48, 51].

$$\frac{\Delta Q}{\Delta t} = V_{cs} \frac{\Delta C_{cs}}{\Delta t} + C_{cs} \frac{\Delta V_{cs}}{\Delta t} \quad (2.31)$$

where V_{cs} is the voltage at the current-source output node,

C_{cs} is the parasitic capacitance at the current-source output node, and

Q is the electrical charge stored at the C_{cs} .

It has been reported [29] that this phenomenon can generate a third harmonic and hence degrades the SFDR at high frequencies [24]. The relationship [29, 51] between SFDR and the switching capacitor can be expressed as:

$$\text{SFDR} \approx 20 \log_{10} \left(\frac{5}{\pi f_s N R_L (C_{on} - C_{off})} \right) \quad (2.32)$$

where C_{on} is the C_{cs} when the current-switch is on, and

C_{off} is the C_{cs} when the current-switch is off.

2.3.4.6 Simultaneously-off Current-Switches

Depending on the input signals (i.e., the digital control signals) of the current-switches, the current-switches could be simultaneously in the off-state for a short duration [31]. As the current-switches transistors are simultaneously in the off-state, their drain-source resistance is high and their drain-source voltage increases. Consequently, the output voltage of the current-sources decreases and their output capacitance is discharged when the current-switches are simultaneously off. This may result in undesirable glitches at the DAC output which may degrade the DAC linearity.

This issue is typically mitigated by means of a switch-driver circuit with appropriate voltage crossing levels at its differential output to ensure that the current-switches are never simultaneously off [59, 60]. It is also important to synchronize the input signals of the current-switches by means of digital registers and careful layout.

2.3.4.7 Digital Signal Feed-through via the C_{GD} of the Current-Switches

Depending on the topology of the current-switches, the digital control signals could cause output glitches through the parasitic capacitors of transistors. In a simple differential pair topology, the digital signal could feed-through via the gate-drain

parasitic capacitor, C_{GD} , of the current switches transistors thereby causes glitch errors at the output.

The DAC output glitch errors caused by the digital signal feed-through are typically mitigated by employing reduced voltage-swing control signals or by adopting the cascode current-switches topology [61, 62].

2.3.4.8 Jitter

Consider a sine wave, $V_{in} = A \sin 2\pi f_{in} t$, sampled at $t = kT_s + \tau$, where τ is the aperture jitter. In the presence of timing jitters, each sampling instant may deviate from its defined timing which may distort the sampled output. Consequently, the timing jitters may degrade the SNR of DACs as expressed in Equation (2.33) [9].

$$\text{SNR}_{\text{dB}} = 20 \log_{10} \left(\frac{1}{\sqrt{2} A \pi f_{in} \sigma_j} \right) \quad (2.33)$$

where σ_j is the root-mean-square (rms) jitter,

f_{in} is the sine wave frequency, and

A is the sine wave amplitude.

2.3.5 Reported CS-DAC Design Techniques

In this section, the reported CS-DAC design techniques, including calibration, DEM, gradient cancelation, delay differences compensation, and biased cascode scheme, are briefly discussed.

2.3.5.1 Calibration

In CS-DACs, a calibration can be employed to adjust the magnitude of the current-sources toward the designed magnitude to improve their matching and uniformity. In general, the calibration process involves measurements of the errors between the magnitude of the current-sources and that of a reference [20, 63-66], and a mechanism to adjust the magnitude of the current-sources based on these errors.

In a reported calibration [20], the sensing/measurement part is realized using a successive-approximation register (SAR) controller that translates the errors into a digital code. The code is then converted into analog calibration signals by calibration DACs. The adjustment part is performed by utilizing the analog calibrations signals to adjust the V_{TH} of the current-sources through the body bias node.

Calibrations are generally not appropriate in high-speed (GHz) CS-DACs as the calibrations circuit could affect the overall CS-DAC speed. Figure 2.17 depicts an example of a current calibration technique [63] where the current-sources are sequentially connected to a calibration circuit to calibrate their magnitude toward the

reference current I_{REF} . While this calibration may improve the current matching between the current-sources, it may significantly degrade the output impedance of the current-sources, and/or cause additional glitches at the CS-DAC output (e.g., during switching between current-sources for calibrations). Furthermore, other CS-DACs with other calibration techniques are also generally slow, largely because the calibration itself is slow and/or the parasitic capacitance is increased at the output. In view of its impact on the overall CS-DAC speed, calibrations are often omitted in CS-DACs that operate at multiple GHz.

Figure 2.17 A current calibration technique [63]

2.3.5.2 Dynamic-Element-Matching (DEM)

The DEM [67, 68] is a technique that mitigates the current mismatches, generally by randomizing the DAC components (currents or voltages), to average down their errors in the time domain. Figure 2.18 illustrates the basic principle of the DEM where the output currents I_A and I_B randomly switch between I_1 and I_2 based on a pseudorandom digital signal PR . Assuming that $I_1 = I + \Delta I$, $I_2 = I - \Delta I$, the output currents I_A and I_B approximately equal to $I = 0.5(I_1 + I_2)$, i.e., the average of the I_1 and I_2 where the current error ΔI is effectively averaged down.

Figure 2.18 Basic principle of DEM

The current errors randomization in DEM can be realized in several methods. In a reported method [69] (as illustrated in Figure 2.18), shufflers are placed in cascade or series with the current-sources to realize the DEM. The inclusion of the shufflers, however, reduces the available voltage headroom for the current-sources and current-

switches. Hence, this method is inappropriate for DACs that employ a low supply voltage.

In other reported [70] method, the DEM is obtained by scrambling the control signals that drive the current-switches. This effectively randomizes the current-sources currents. The randomness of this scrambling largely depends on the pseudorandom signals that controls the scrambling or swapper circuits. As this method does not reduce the available headroom for the current-sources or current-switches, it is suitable for CS-DACs with low supply voltages.

Interestingly, the efforts to mitigate the impact of current mismatches by the DEM may be counterintuitive. For example, the DEM is a completely digital technique that assumes no knowledge of the component (i.e., the current) mismatches, and yet it controls the error introduced by the component mismatches. By scrambling the current-sources to be employed to form the analog output in every conversion period, the respective current errors are effectively averaged down in the time domain. In the frequency domain, the randomized current errors result in reduced distortion (i.e., higher SFDR) with a marginal increase in the noise floor. Nonetheless, the effect of the increased noise floor is generally insignificant when compared to the reduction of the spurious/harmonic tones. Consequently, the overall DAC linearity is improved with DEM techniques.

There are a number of reported different DEM algorithms in literature, including the generalized cube networks [71], barrel-shift networks [72], TRI-DEMRZ [70], digital random return-to-zero [73], etc. The DEM implementations, however, involve

complex and relatively slow digital circuitry which in turn becomes the main speed bottleneck in high-speed CS-DACs. Consequently, reported DEM CS-DACs are typically slower than their non-DEM counterparts, and may not be suitable for the next generation high-speed DACs that need to operate at multiple GS/s.

2.3.5.3 Gradient Error Cancellation

Figure 2.19 depicts a common-centroid and chessboard-like distribution in the current-sources layout placement to mitigate the first order gradient error [54]. In a geometric sense, the centroid of the composite current-sources is located at the center of the matrix and the current-sources are arranged symmetrically around the center to cancel any linear gradient to the first order.

Figure 2.19 Chessboard-like layout placement to mitigate the first order gradient error

[54]

In the switching scheme techniques such the Q^2 random walk [55], the current-sources are subdivided and the switching sequence of the subdivided currents is largely random. By “randomly walked” through the current-sources, the current error is not accumulated but rather “randomized” which results in an improved overall linearity.

Note, however, that both the aforesaid techniques are increasingly difficult to implement at multiple GHz frequencies, largely because of the constrained imposed by the intrinsic speed of the transistors, and/or other non-ideal parameters, including the delay differences and jitters.

2.3.5.4 Delay Differences Compensation

The delay differences due to the interconnections mismatches can be mitigated by means of proper layout placements and routing. Figure 2.20 depicts a routing style that compensates the clock delays with the output delays [9, 57]. Alternatively, the delay differences can be mitigated with a binary tree structure for both the clock and output connections as depicted in Figure 2.21 [9, 57, 74]. Similarly, the clock H-tree structure may also be applied to mitigate the systematic timing skews and delay differences [9].

Figure 2.20 Compensation of the clock delays with the output delays [9, 57]

Figure 2.21 Compensation of the delay differences in the clock and output lines with a binary tree structure [9, 57, 74]

2.3.5.5 Biased Cascode Scheme [25]

The CS-DAC design in [25] reported a good harmonic performance at high frequencies (up to 1.6GHz), in part by means of biased cascode transistors. Figure 2.22 depicts the employed current cell in [25] where the cascode transistors M_5 and M_6 are constantly biased by the small current sources I_{bias} . As M_4 and M_5 are always "on", their parasitic elements become less signal-dependent, and their intrinsic gain also attenuates the effect of switching noises of M_2 and M_3 . Overall, this method improves the linearity at high frequency by almost an order of magnitude.

Figure 2.22 A CS-DAC current-cell with biased cascode transistors

2.3.6 A Survey of High-Speed CS-DACs

At this juncture, a number of high-speed DACs based on the CS-DAC architecture have been reported in literatures. We tabulate in Table 2.2 these state-of-the-art high-speed CS-DACs from year 2001 to 2017, including some of the critical DAC parameters. To analyze the trend between the linearity and the speed of high-speed DACs, the worst-case SFDRs in Table 2.2 are plotted against their corresponding output signal frequency f_{out} in Figure 2.23, and also against the conversion rate f_s of the DACs in Figure 2.24.

On the basis of Figure 2.23, we remark the following. When f_{out} is $<5\text{GHz}$, the reported SFDRs remain relatively high, $\sim 70\text{dBc}$. Beyond 5GHz , the SFDR decreases relatively quickly, particularly $>20\text{GHz}$ where the reported SFDRs are $\sim 30\text{dBc}$.

On the basis of Figure 2.24, we remark the following. The SFDR remains high, $\sim 70\text{dBc}$ until $\sim 9\text{GS/s}$ conversion rate, and drops rather rapidly thereafter. At conversion rate from $\sim 18\text{GS/s}$ to 100GS/s , the reported SFDRs range from $<40\text{dBc}$ to $\leq 30\text{dBc}$.

Collectively, on the basis of our review in Figures 2.23 and 2.24, the general observation, as expected, is that SFDR drops substantially at higher output signal frequencies or higher conversion rates – in the GHz or GS/s realms.

Table 2.2 Survey of the reported state-of-the-art high-speed CS-DACs from 2001 to 2017

No	Publication	Process	Feature size (nm)	n (bit)	f_s (GS/s)	SFDR (dBc)	f_{out} (GHz)	INL (LSB)	DNL (LSB)	P_d (mW)	V_{DD} (V)
1	TMTT '15 [75]	CMOS	28	8	100	27	24.9	0.2	0.04	2500	1.1/1.5/2.0
2	CSICS '11 [45]	InP HBT	500	6	60	–	–	-0.19/0.31	-0.13/0.43	1800	-4.0
3	ISSCC '11 [12]	CMOS	65	6	56	30	26.9	–	–	750	1.1/2.5
4	TMTT '16 [76]	BiCMOS	130	6	56	–	–	–	–	5200	2.5/3.3/5.7
5	MWSYM '12 [77]	BiCMOS	130	6	50	–	–	–	–	4480	5.1
6	OFC '10 [78]	BiCMOS	180	6	43	–	–	–	–	18000	–
7	JSSC '06 [79]	DHBT	InP	8	32	26.95	11.88	–	–	9450	-3.6/-4.5
8	CSICS '10 [80]	InP HBT	1000	6	28	36	6.66	-0.68/0.17	-0.16/0.68	950	-4.0
9	ISSCC '05 [81]	BiCMOS	130	6	22	–	–	0.9	0.5	1200	–
10	EuMIC '08 [47]	BiCMOS	250	8	20	–	–	–	–	2500	2.5/4.5
11	ISSCC '15 [82]	CMOS	28	8	18	38	9	–	–	84	–
12	JSSC '12 [34]	BiCMOS	130	12	12	55	6	± 0.3	–	8300	–

No	Publication	Process	Feature size (nm)	n (bit)	f_s (GS/s)	SFDR (dBc)	f_{out} (GHz)	INL (LSB)	DNL (LSB)	P_d (mW)	V_{DD} (V)
13	VLSIC '08 [83] & JSSC '08 [27]	CMOS	90	8	12	35	1.5	0.31	0.28	190	1.0/1.8
14	VLSIC '14 [84] & JSSC '15 [85]	FDSOI	28	9	11	52	4.6	–	–	110	1.0
15	TVLSI '14 [86]	CMOS	90	4	14	29.1	1.11	± 0.22	-0.21/0.16	85	1.0
16	TCSII '17 [87]	CMOS	65	4	10	23.3	4.53	0.16	0.12	30	1.2
17	VLSIC '13 [88]	CMOS	28	13	9	71	1	3	–	360	1.8
18	JSSC '12 [34]	BiCMOS	130	14	7.2	67	3.6	± 1.2	–	8300	–
19	TVLSI '15 [11]	CMOS	28	6	7	50	1	–	–	145	1.4/2.5
20	ISSCC '17 [89]	FinFET	16	14	6.8	65	5.2	–	–	330	–
21	VLSIDAT '09 [90]	CMOS	130	6	6	12.5	2.7	-0.16/0.15	-0.12/0.09	115	1.2
22	JSSC '13 [5]	CMOS	40	9	5	60	–	–	–	375	2.5
23	EuMIC '11 [91]	BiCMOS	130	8	5	42	1.25	0.29	0.58	26	3.0
24	TVLSI '15 [26]	CMOS	28	6	3.5	–	–	–	–	53	1
25	ISSCC '17 [92]	BiCMOS	130	10	3.35	48	20	–	–	1910	–

No	Publication	Process	Feature size (nm)	n (bit)	f_s (GS/s)	SFDR (dBc)	f_{out} (GHz)	INL (LSB)	DNL (LSB)	P_d (mW)	V_{DD} (V)
26	TVLSI '15 [93]	CMOS	90	6	3.1	37.2	1.43	–	–	17.7	–
27	ISSCC '12 [94]	CMOS	180	14	3	52	1.5	–	–	600	–
28	VLSIC '11 [95]	CMOS	65	9	3	50	1.5	–	–	–	–
29	ISSCC '14 [96]	CMOS	180	14	4.6	69	0.5	–	–	2300	1.8/3.3
30	ASSCC '07 [14] & JSSC '08 [13]	CMOS	130	6	3	36.2	1.43	0.02	–	29	1.2
31	TCSII '12 [97]	CMOS	90	6	3	36.24	1.5	0.07	0.05	8.32	1.2
32	MIKON '10 [98]	HBT	SiGeC	12	3	50	4.5	–	–	1300	3.3/5.0
33	ISSCC '09 [25] & JSSC '09 [24]	CMOS	65	12	2.9	50	0.65	0.5	0.3	188	1.0/2.5
34	APCCAS '06 [42]	CMOS	130	6	2.704	37	0.52	0.1	0.1	28	1.2
35	TCSII '13 [43]	CMOS	65	10	2	50.5	0.061	–	–	37	–
36	ASSCC '13 [99]	CMOS	65	12	1.7	58	0.85	-2.0/7.5	–	–	1.2
37	JSSC '14 [23]	CMOS	40	12	1.6	70.3	0.784	–	–	40	1.2
38	JSSC '05 [100]	HBT	–	12	1.6	41	2.4	-2.5/3.5	-2.0/5	2700	-5.0/3.0

No	Publication	Process	Feature size (nm)	n (bit)	f_s (GS/s)	SFDR (dBc)	f_{out} (GHz)	INL (LSB)	DNL (LSB)	P_d (mW)	V_{DD} (V)
39	TCSI '10 [48]	CMOS	130	10	1.6	54	0.55	0.34	0.29	27	1.2/1.8
40	TCSII '11 [73]	CMOS	90	8	1.6	57	0.7	-0.2/0.0	-0.03/0.04	90	1.2/2.5
41	ISSCC '13 [101]	CMOS	40	12	1.6	70.3	0.8	–	–	40	1.2
42	ISOCC '10 [102]	CMOS	65	6	1.4	40.8	0.005	-0.11/0.10	-0.18/0.12	11.9	1.0
43	ISSCC '11 [103]	CMOS	90	12	1.25	70	0.5	-1.2/1.0	-0.5/0.45	128	1.2/2.5
44	TVLSI '16 [104]	HTFET	20	14	1	67	0.46	0.7	-0.49/0.56	4.6	0.4/0.3
45	JSSC '01 [16]	CMOS	350	10	1	61.2	0.49	-0.2/0.2	-0.10/0.15	110	3.0/1.9

Figure 2.23 Plot of the worst-case SFDRs (of the reported state-of-the-art high-speed DACs from 2001 to 2017) against output frequency

Figure 2.24 Plot of the worst-case SFDRs (of the reported state-of-the-art high-speed DACs from 2001 to 2017) against conversion rate

2.4 Review of Measurement Techniques for High-Speed DACs

As mentioned earlier, test and verification of GS/s DACs are challenging. These include the difficulties in providing data patterns at the DAC input at high data rate. The data pattern for the DAC input can be either generated by external or internal DPGs. A reported DAC [23] employs an external DPG, Keysight's parallel bit-error-rate-test (parBERT) 81250, to generate the required high-speed data patterns. Because data patterns are externally generated, they can be controlled with ease and the DAC measurement process is greatly simplified. However, this method may involve a complex printed circuit board layout for precise synchronization, and additional wideband I/O buffers for equalization. Furthermore, this parBERT 81250 or other high data-rate external DPGs are rather expensive and largely unavailable.

A measurement technique that employs an internal DPG is attractive, particularly when the available external DPGs are slower than the conversion rate of the DAC to be measured. In addition to a data storage block such as a RAM [12] or shift-registers [26], this measurement technique also requires complex high-speed or RF blocks such as a frequency divider, delay or phase locked-loop, multiplexer (MUX), and Counter (for address signals). In a reported RAM based internal DPG [12], the digital data are first stored in the RAM. These data are thereafter read sequentially and cyclically based on the address signals that are generated by an auxiliary control circuit. Because of relatively slow RAM read cycle, the time interleaving technique is typically required and is implemented using multiple stages of high-speed MUXes to obtain higher data rate. In another reported DAC [26], the internal DPG employs shift-

registers instead of a RAM to store the digital data patterns, and similarly the time-interleaved technique is employed to obtain high data rate.

Besides employing DPGs, high-speed DACs measurement may also include a built-in high-speed digital signal processor (DSP) [34]. While the inclusion of a high-speed DSP enables measurements of more complex wideband analog signals, the implementation is difficult and it requires a DSP intellectual property (IP). Depending on the process technology, the specific high-speed DSP IP can be difficult to realize, and to obtain because of its lack of availability.

In summary, the test and verification of GS/s DACs are challenging. Further, and not unexpectedly, reported measurement techniques to provide high-speed data patterns generation are costly and/or difficult to implement.

2.5 Conclusions

In this chapter, we have reviewed the basic DAC architectures that are suitable for high-speed applications, including their *modus operandi* and their fundamental building blocks. Of specific interest, the in-depth review was largely focused on CS-DACs, including an overview of the current design challenges particularly when the operating frequency is in the GHz and the conversion rate is in the GS/s realms. In short, on the basis of this review, we remark that despite the mature design art of CS-DACs and their analytical investigations, there remain a number of a number of ambiguities and unresolved design limitations.

Chapter 3

A 4-bit 10GS/s Single-Core DAC for Cognitive Ultra-Widebands

3.1 Introduction

A large portion of this chapter has been published in IEEE Transaction on Circuit and System II [87].

The CUWB radio, a hybrid of ultra-wideband (UWB) and cognitive radio, is an emerging approach that enables highly efficient spectrum utilization (unlike its non-cognitive counterparts that requires spectrum band pre-allocation) and yet low interference [105]. Typically, the CUWB system searches for available spectrum bands in the vicinity, negotiates with nearby radio systems, employs the spectrum ranges resulting from the negotiations, and thereafter reiterates the said process in real time. In view of this, it is highly desirable that the CUWB transmitter can generate adaptive UWB waveforms that conform to the available spectrum bands.

In an impulse-radio version of non-cognitive UWB (UWB-IR), the UWB waveform is conventionally generated by a pulse generator by means of delay recombination,

oscillator circuit and step recovery diode approaches [106, 107]. Unfortunately, these approaches are inappropriate for a Cognitive UWB-IR (CUWB-IR) largely because the said pulse generators are typically limited to a single UWB pulse shape. While a few pulse generators can be multiplexed to obtain different pulse shapes, its realization has shortcomings of excessive hardware, complex pulse generation, and/or poor CMOS System-on-Chip (SoC) compatibility.

The alternative approach, a DAC-based pulse generator [105], can mitigate the said shortcomings by synthesizing adaptive UWB waveforms with pertinent digital inputs. Specifically, the DAC-based pulse generator offers three advantages. First, it adaptively generates the UWB signal with reconfigurable pulse shapes by leveraging on the preceding DSP. Second, it features reduced ringing tail of the pulse waveform [107], hence the ensuing improved power efficiency and noise immunity in digital communications. Third, it is CMOS SoC compatible. In view of these attributes, the high-speed Nyquist-rate DAC is arguably the optimal embodiment for the pulse generator of CUWB-IR transmitters.

In view of the advantages of low impedance nodes, high-speed open-loop structure, and resistive load driving capability without the need for additional buffers [13], the current-steering architecture [11, 12, 45, 108] is typically adopted for the design of high-speed (GS/s) Nyquist-rate DACs. Despite these advantages, state-of-the-art CS-DACs are largely inappropriate for low-power compact CUWB-IR systems. Some reported high-speed DACs [45, 108] are realized using exotic fabrication processes (e.g. SiGe, BiCMOS, III-V, etc.) with high cutoff frequency transistors. Although the high conversion rate can be achieved by means of said exotic processes, those

processes are typically costly, and are inappropriate for SoC implementation. On the other hand, reported CMOS high-speed DACs leverage on the time-interleaving technique to achieve high conversion rate, but at the cost of excessive complexity, hardware (including PLL, frequency divider, etc.) and hence excessive power dissipation [12, 109]. Put simply, there is a need for a high-speed single-core CMOS DAC with low hardware overheads to enable a lower-power compact CUWB-IR system.

In this chapter, we present a 4-bit 10GS/s single-core CS-DAC for the CUWB-IR system. The 4-bit resolution provides a small design margin over the minimum resolution requirement (3 bits [105]) to generate adaptive pulse waveforms. Furthermore, it allows for a realization featuring low hardware complexity and low power dissipation for the ensuing CUWB-IR system. The 10GS/s Nyquist rate, on the other hand, enables wide bandwidth with redundancy to cater for unavailable/occupied spectrum bands and to ensure sufficient transmission energy. To reduce the non-linearity associated with the finite output impedance, we design the output stage current-sources based on our derived relationships between current-sources output impedance and linearity parameters. We propose a novel switch-driver circuit with a high-speed buffer to minimize the output glitches without compromising high-speed operation. The high-speed buffer enables the control signals with shorter transition time and a smaller voltage swing. We also present a novel in-situ shift-register-based DPG to generate input digital data patterns up to $4 \times 10\text{Gb/s}$ with small hardware and I/O overheads (as opposed to techniques that involves digital memory, such as RAM [12]).

The designed CS-DAC and the in-situ DPG are realized using a commercial 65nm CMOS technology. The measured INL and DNL are within $\pm 0.16\text{LSB}$ and $\pm 0.12\text{LSB}$ respectively. The SFDR across the Nyquist bandwidth is greater than 23dBc with 30mW power dissipation. When benchmarked with state-of-the-art DACs, the designed CS-DAC features the best FoM.

This chapter is organized as follows. Section 3.2 presents the 4-bit 10GS/s CS-DAC design for the CUWB-IR system. Section 3.3 presents the novel in-situ DPG. Section 3.4 presents the measurement results of prototype chip and benchmarking thereof. Finally, conclusions are drawn in Section 3.5.

3.2 Design of a 4-bit 10GS/s CS-DAC

Figure 3.1 depicts the block diagram of the designed 4-bit 10GS/s binary CS-DAC. The digital binary input is first buffered at the input buffer stage and the ensuing switch-driver conditions the digital signals. Subsequently, the conditioned digital signals are fed into the current-switches at the output stage. Based on the digital binary inputs, each current of the current-sources is then switched toward one of the differential loads to form the analog output signal.

The critical building blocks – the current-sources, current-switches, and switch-drivers – will now be delineated in turn.

Figure 3.1 Block diagram of the 4-bit 10GS/s CS-DAC prototype IC

3.2.1 Current-Sources

In high-speed CS-DACs, the current-source design involves a tradeoff between high output impedance at high frequency and good transistor matching, and both affect the DAC linearity [13]. A high output impedance current-source (over wide bandwidth) is crucial for low output distortion and this can be realized by a small-sized transistor for its low parasitic capacitance. Conversely, the small-sized transistor may degrade the transistor matching amongst the array of current-sources, resulting in high nonlinearities and poor yield [13]. In short, it is imperative to design the current-sources with optimized transistor sizes to enable a good compromise between sufficiently high output impedance and good transistor matching.

Figure 3.2 Schematic diagram of one of the current cells at the CS-DAC output stage where it consists of a cascode current-source and a pair of current-switches

Figure 3.2 depicts the schematic of the well-established cascode current-source (M_1 – M_2) with current-switches (M_3 – M_4). In view of the aforesaid tradeoff, we first ascertain the output impedance that is sufficiently high to satisfy the 4-bit requirement, and thereafter the transistor matching. The desired output impedance of a differential output CS-DAC can be obtained from the specifications of INL and SFDR.

We will now derive the relationship between the output impedance and INL for the unary current-steering topology depicted in Figure 3.3. The binary current-steering topology is effectively a parallel of multiple unit current-sources. Based on end-point

INL calculation [30], the INL for each input code k can be expressed as⁺:

$$\text{INL}_k = \frac{v_{out,k} - v_{out \min}}{v_{out,LSB}} - k = \frac{k[N-k][N-2k]}{2[k+s][N-k+s]} \quad (3.1)$$

where INL_k is the INL for each input code k ,

$$s = r_o / R_L,$$

$$v_{out,LSB} = (v_{out,M} - v_{out,0}) / N,$$

$$N = 2^n - 1,$$

$v_{out,k}$ is the DAC output voltage for input code k ,

n is the DAC resolution,

R_L is the load resistance, and

r_o is the output resistance of the unit current-sources.

Figure 3.3 Schematic diagram of the equivalent circuit of a unary CS-DAC

⁺ See Appendix A for the complete derivation.

By solving $\frac{\partial \text{INL}}{\partial k} = 0$, the INL peak value, INL_{pk} , can be expressed as:

$$|\text{INL}_{pk}| = \frac{1.5s[s+N]-0.5p}{s[s+N]-p} \sqrt{N^2 + 6s[s+N] - 2p} \quad (3.2)$$

where $p = \sqrt{2N^3s + 11N^2s^2 + 18Ns^3 + 9s^4}$.

By solving Equation (3.2) for n and $N \geq 1$, and r_o , R_L , and $|\text{INL}_{pk}| \geq 0$, r_o can be expressed as:

$$r_o = R_L \left[-\frac{N}{2} + \frac{\sqrt{3}}{18} \sqrt{9N^2 + 8\text{INL}_{pk}^2 + \frac{[3N^2 + 4\text{INL}_{pk}^2]^{1.5}}{|\text{INL}_{pk}|}} \right] \quad (3.3)$$

Next, by assuming that the third order harmonic is the largest spur, the relationship between the output impedance and SFDR (dBc) can be derived, in part from the analysis in [31], as:

$$r_o \cong \frac{NR_L}{4} 10^{|\text{SFDR}|/40} \quad (3.4)$$

Based on Equations (3.3) and (3.4), and R_L of 50Ω , r_o is required to be $>1.0\text{k}\Omega$ to satisfy $\text{INL} < 0.25\text{LSB}$ and $>24\text{dBc}$ SFDR. As the effect/contribution of the current-switch on the overall output impedance is negligible at high frequency, for design simplicity (yet without compromising accuracy), the determined r_o sets the required output impedance (over wide bandwidth) of the current-sources. Note that the

aforesaid requirement for the output impedance assumes that all current-sources are perfectly matched. However in practice, the mismatch is inevitable due to process variations and gradients, unmatched parasitic capacitances, etc. In view of this, we adopt the following.

First, the mismatches due to process variations are mitigated by optimizing the transistors size of the unit current-source on the basis of statistical simulations (with nominal conditions of 1000 samples) – in an attempt to ascertain the 3σ yield of $<0.25\text{LSB}$ INL and DNL.

Second, the parasitic capacitance of the unit current-source is minimized. Both transistors of the current-source in Figure 3.2 are designed with equal channel width, hence enabling an abutted layout topology. As a result, the parasitic capacitance (and the pertinent unmatched issue) contributed by the transistor area and interconnections are substantially reduced.

Finally, the mismatch due to process gradients is mitigated by partitioning the 4-bit current-sources into multiple unit current-sources and applying inter-digitation and common-centroid techniques.

3.2.2 Current-Switches

Figure 3.2 depicts the schematic of the current-switches where the simple differential pair topology is adopted to meet the requirement of the 10GS/s conversion rate. The

current-switch design herein involves the enhancement of the DAC dynamic linearity by reducing the output glitches due to capacitive feed-through. The capacitive feed-through effect is reduced by minimizing the current-switches' parasitic capacitance and employing low voltage swing control (drive) signals on the current-switches.

In view of this, the current-switch transistors are sized with minimum channel length for small parasitic capacitance and high cut-off frequency f_T . On the other hand, the channel width is designed on the basis of the available voltage headroom ($\sim 0.5V$), the maximum control voltage, and the current magnitude, while accommodating for process, voltage, and temperature variations.

3.2.3 Switch-Drivers

The switch-driver serves to improve the dynamic linearity by reducing the output glitches at the CS-DAC output stage. It is well established [16] that there are three primary glitch mechanisms:

- (i) Improper crossover point of the differential control signals which may undesirably cause both current-switches to turn “off” simultaneously,
- (ii) Capacitive feed-through – coupling of the switching noise from the switch-driver to the CS-DAC outputs via the parasitic capacitors of the current-switches, and

(iii) Timing mismatch or jitters of the control signals into the current-switches.

The David-Goliath inverter [13] can mitigate the glitch mechanism (i) by setting the crossover point of their output so that the current-switches are never “off” simultaneously.

To further mitigate the glitch mechanism (ii), the novel switch-driver (based on David-Goliath inverters (M_1 - M_6)) with the augmentation of the high-speed source-followers (M_7 - M_8) is proposed and depicted in Figure 3.4. The augmented source-followers mitigate the glitch mechanism (ii) by ascertaining low voltage swing ($\sim 0.5V_{DD}$) and short transition time ($\sim 10\%T_{clock}$) control signals. Note that the short transition time ($3\times$ faster than the David-Goliath inverter's) during switching is important for short glitch duration.

Figure 3.4 Schematic diagram of the proposed switch-driver circuit

For glitch mechanism (iii), the delay difference amongst different current-switches is minimized by appropriate layout placements and by matching the routing metals of the differential control signals. Further, intersymbol interference is mitigated in two ways. First, resistive loads, instead of transistors in the triode mode, are adopted herein for fast switching and hence less parasitic capacitance and intersymbol interference. Second, the output impedance is designed to be sufficiently low to mitigate the intersymbol interference due to undesired excess charges [63].

3.3 Novel In-Situ Digital Pattern Generator (DPG)

It is difficult to test the proposed CS-DAC, particularly because of the required 4×10 Gb/s input digital patterns. For Gb/s baud rate, a time-interleaving technique [12, 45] is typically employed to ease the I/O requirements. However, this approach raises several other challenges including substantially more I/Os and chip area, and complex auxiliary circuits (e.g., PLL, frequency divider, etc.). In view of these challenges, we propose a simple and efficient approach to enable high-speed DAC tests.

Our proposed in-situ DPG offers three advantages. First, it offers dual-mode operation of fast (10Gb/s) READ mode and slow (25Mb/s) WRITE mode. The former serves the high-speed testing purpose, and the latter is attractive for its simplicity and low speed programmability. Second, the implementation of the proposed in-situ DPG is relatively easy because of its design modularity and reusability. Third, the hardware overhead is largely minimized because no address signals are required.

Figure 3.5 depicts the proposed novel in-situ DPG that serves to generate $1 \times 10\text{Gb/s}$ periodic high-speed digital patterns. The required $4 \times 10\text{Gb/s}$ rate is achieved by employing four unit in-situ DPGs with data pattern length of up to 64 bits. Figure 3.5 also depicts the data flows of the said operating modes: WRITE (dashed line) and READ (dotted lines) modes which will be delineated as follows.

The in-situ DPG is initially switched to WRITE mode. The clock CK is set to CK_{SLOW} (25MHz) and four 16-bit serial-in-serial-out shift-registers are connected in series (SR_1 - SR_2 - SR_3 - SR_4). Subsequently, the header/flag and input data (with certain format) B_n are serially stored in each of the flip-flops of the SR_1 - SR_2 - SR_3 - SR_4 at 25Mb/s baud rate for each DAC input bit. The WRITE mode is completed when the header/flag signal reaches the control block; i.e., all data are stored in the in-situ DPG.

Figure 3.5 Proposed novel in-situ DPG for generating a $1 \times 10\text{Gb/s}$ high-speed data patterns. The switches position reflects the READ mode operation

Thereafter, the in-situ DPG is switched to READ mode, wherein the clock CK is switched to CK_{FAST} (5GHz). In the READ mode, the shift-registers are effectively configured into two loops so that the data will remain stored in the shift-registers (they are shifted in every clock cycle). As each loop generates data at 5Gb/s baud rate, the two loops are thereafter time-interleaved to achieve the required 10Gb/s by the MUX stage.

3.4 Measurements and Benchmarking

Figure 3.6 depicts the photomicrograph of the prototype IC realized using a commercial 65nm CMOS process and embodies the proposed CS-DAC design ($340\mu\text{m}\times 100\mu\text{m}$) and the novel in-situ DPG ($150\mu\text{m}\times 100\mu\text{m}$). The analog parts are isolated from digital parts by incorporating guard rings to reduce the digital switching noise. The clock grid distribution network is adopted to ensure low timing skew while the clock buffer is based on the multi-stage clock tree structure.

Figure 3.6 Photomicrograph of the core 4-bit 10GS/s CS-DAC with the in-situ DPG

The test and measurement of our CS-DAC prototype IC is performed on high frequency (Rogers RO4003®) PCBs. Before measurements, the in-situ DPG is programmed by using an Altera® DE2 board to store test patterns. Based on these patterns, the CS-DAC is then measured with a DSAX93204A Infiniium (from Keysight Technologies) oscilloscope.

Figures 3.7 and 3.8 depict the plots of the measured INL and DNL respectively, where both INL and DNL are small, i.e., within $\pm 0.16\text{LSB}$. The small static nonlinearities are desired to reduce the unwanted spurs/harmonics for high dynamic linearity. Figure 3.9 depicts the measured SFDR against the output signal frequency. The measured SFDRs are $>23\text{dBc}$ over the entire Nyquist bandwidth up to 4.53GHz, and is sufficient for the desired CUWB-IR applications.

Figure 3.7 Measured INL of the 4-bit 10GS/s CS-DAC

Figure 3.8 Measured DNL of the 4-bit 10GS/s CS-DAC

Figure 3.9 Measured SFDR against output frequency

To benchmark our CS-DAC against state-of-the-art DACs based on CMOS and non-CMOS, we tabulate the various designs in Table 3.1. In this benchmarking, our single-core DAC features a higher conversion rate than state-of-the-art CMOS DACs [11, 26], except [12]. The CMOS DAC in [12] features a higher conversion rate than our design, largely because it employs a 16:1 time-interleaving. However on the basis of a single-core DAC (3.5GS/s), it is slower. The multi-stage interleaving approach is not considered for the intended CUWB-IR application because of the complex hardware overhead for synchronization, hence the unacceptable power penalty. When compared on the basis of dynamic linearity, our CMOS DAC achieves a relatively good SFDR close to that of 6-bit CMOS DACs [11, 12, 26] despite our 4-bit resolution.

Table 3.1 Benchmarking the proposed CS-DAC against state-of-the-art high-speed DACs

Parameters	This Work	TVLSI '15 [26]	TVLSI '15 [11]	ISSCC '11 [12]	BCTM '07 [108]	CSICS '11 [45]
Technology	CMOS	CMOS	CMOS	CMOS	BiCMOS	InP HBT
Feature size (nm)	65	28	28	65	250	500
Resolution (bit)	4	6	6	6	4	6
V_{DD} (V)	1.2	1	1.4/2.5	1.1/2.5	3.5	−4.0
$f_{conv-single-core}$ (GS/s)	10	3.5	7	3.5 ^c	30	60 ^e
$V_{out-swing}$ ($V_{pp-diff}$)	0.12	0.225	0.5	0.6	0.05	1
P_d (mW)	30	53	145	46.87 ^d	455	1800
SFDR (dBc)	23.3 ^a	30.6	26 ^b	30	—	—
INL (LSB)	0.16	0.03	—	—	0.49	0.31
DNL (LSB)	0.12	0.03	—	—	0.57	0.43
FoM (pJ)	0.19	0.24	0.32	0.21	0.95	0.47

^a f_{out} =4.53GHz;

^b f_{out} =3.45GHz;

^c 16:1 time-interleaved/multiplexed to 56GS/s;

^d estimated for single-core DAC;

^e only measured up to 13.5GS/s.

Not unexpectedly, when compared against non-CMOS DACs [45, 108], our proposed CS-DAC is slower because the transistors based on advanced process (InP HBT) or BiCMOS typically have higher cut-off frequency f_T than that of 65nm low power CMOS process. Nonetheless, the designed CMOS CS-DAC has the advantage of substantially lower power and it is appropriate for realization in CMOS SoCs. A highly worthy feature of our CS-DAC is the substantially lower power dissipation compared to the other benchmarked DACs. We achieve this desirable substantially lower power dissipation by employing a low supply voltage (1.2V) and fewer digital circuits.

As benchmarking among different architectures or process technologies is difficult, we compare the various high-speed DACs by utilizing the well-adopted FoM [13] in Equation (3.5).

$$\text{FoM} = \frac{P_d}{2^n f_{\text{conv}}} \quad (3.5)$$

where P_d is the power dissipation (mW), and

f_{conv} is the conversion rate (GS/s or GHz).

This FoM provides a composite measure of DACs performance across three critical parameters, namely, power dissipation, resolution, and conversion rate (effective bandwidth). On the basis of this FoM, our high-speed CS-DAC prototype IC features the best FoM (lowest being the best).

3.5 Conclusions

We have presented our proposed 4-bit 10GS/s single-core CS-DAC for CUWB-IR applications. To achieve the high-speed operation and required linearity, every critical block including current-sources, current-switches, and switch-drivers have been optimized, and a novel switch-driver circuit has been proposed to improve the linearity. Further, a novel in-situ DPG has been proposed to enable low-speed programmability (WRITE mode) and high-speed digital pattern generation (READ Mode). The designed CS-DAC and in-situ DPG have been realized using a commercial 65nm CMOS process. The CS-DAC features $\leq 0.16\text{LSB}$ INL/DNL and $>23\text{dBc}$ SFDR

across the Nyquist bandwidth (up to 4.53GHz) at very low 30mW power dissipation. The proposed CS-DAC achieves the best FoM when benchmarked against state-of-the-art DACs.

Appendix A

Analysis on the Relationship between Output Impedance and INL

The reported relationships [28, 30] between the finite output impedance and the INL, previously mentioned in Section 2.3.4.1, assume that the output impedance is much larger than the load impedance, and the INL is small. When the assumptions are invalid, however, these reported relationships may become inaccurate and inappropriate for estimating the required output impedance during the design process.

Figure A.1 Small-signal model of a unary CS-DAC

In this Ph.D. thesis, the relationship between the finite output impedance and INL is derived without the aforementioned assumptions for higher precision. The derivations are based on the CS-DAC model depicted in Figure A.1 where the unary topology is employed for the sake of simplicity. Note that the derived expressions later are also applicable for the other CS-DAC architectures as the INL is largely independent on the current-sources segmentation [52]. Further to this, the following derivations are intended for differential output CS-DACs as they are often employed in high-speed applications.

A.1 Derivation of INL

The differential analog output voltage, v_{out} , is defined as:

$$v_{out} = v_{out+} - v_{out-} \quad (A.1)$$

where v_{out+} is the positive output voltage (V), and

v_{out-} is the negative output voltage (V).

On the basis of the Kirchhoff's Current Law I:

$$\frac{v_{out+}}{R_L} + \frac{v_{out+}}{r_o/k} - kI = 0 \quad (A.2)$$

where k is the input code in decimal, i.e., the number of unit current-sources connected to the v_{out+} node,

I is the current of the unit current-sources (A),

R_L is the load resistance (Ω), and

r_o is the output resistance of the unit current-sources (Ω).

On the basis of Equation (A.2), v_{out+} can be derived as:

$$v_{out+} = k \left[\frac{Ir_o}{k+s} \right] \quad (\text{A.3})$$

where $s = r_o/R_L$

Similarly, v_{out-} can be derived as:

$$v_{out-} = v_{out+} \big|_{k=N-k} = [N-k] \left[\frac{Ir_o}{N-k+s} \right] \quad (\text{A.4})$$

where $N = 2^n - 1$ is the total number of unit current-sources, and

n is the DAC resolution (bit).

By substituting Equations (A.3) and (A.4) into Equation (A.1), v_{out} can be derived as:

$$v_{out} = Ir_o \left[\frac{k}{k+s} - \frac{N-k}{N-k+s} \right] = \frac{Ir_o [2k-N]s}{[k+s][N-k+s]} \quad (\text{A.5})$$

On the basis of Equation (A.5), the minimum output voltage, v_{outmin} , can be derived as:

$$v_{outmin} = v_{out} \big|_{k=0} = -\frac{NIr_o}{N+s} \quad (\text{A.6})$$

Similarly, the maximum output voltage, $v_{out\max}$, can be derived as:

$$v_{out\max} = v_{out} \Big|_{k=N} = \frac{Nr_o}{N+s} \quad (\text{A.7})$$

On the basis of Equations (A.6) and (A.7), the output step voltage (1LSB), $v_{out,LSB}$, can be derived as:

$$v_{out,LSB} = \frac{v_{out\max} - v_{out\min}}{N} = \frac{2Ir_o}{N+s} \quad (\text{A.8})$$

Based on Equations (A.5), (A.6), and (A.8), the INL for each code k can be expressed as:

$$\text{INL} = \frac{v_{out,k} - v_{out\min}}{v_{out,LSB}} - k = \frac{k[N-k][N-2k]}{2[k+s][N-k+s]} \quad (\text{A.9})$$

where $s = r_o/R_L$, and

$$N = 2^n - 1.$$

A.2 Derivation of the Worst-Case INL

To obtain the worst-case INL, we derive the input codes, k_{pk} , that correspond to the

peak value of the INLs, $|\text{INL}_{pk}|$, by solving $\frac{\partial \text{INL}}{\partial k} = 0$ as follows:

$$\begin{aligned} \frac{\partial \text{INL}}{\partial k} &= \frac{[N^2 - 6Nk + 6k^2][Nk - k^2 + Ns + s^2] - [N^2k - 3Nk^2 + 2k^3][N - 2k]}{4[Nk - k^2 + Ns + s^2]^2} \\ 0 &= [N^2 - 6Nk + 6k^2][Nk - k^2 + Ns + s^2] - [N^2k - 3Nk^2 + 2k^3][N - 2k] \\ 0 &= -2N^2k^2 + 4Nk^3 - 2k^4 + N^3s - 6N^2ks + 6Nk^2s + N^2s^2 - 6Nks^2 + 6k^2s^2 \\ 0 &= k^4 - 2Nk^3 + [N^2 - 3Ns - 3s^2]k^2 + [3N^2s + 3Ns^2]k - 0.5[N^2s^2 + N^3s] \end{aligned} \quad (\text{A.10})$$

Let $k = x + N/2$. Equation (A.10) can be converted into a depressed quartic equation and is expressed as:

$$\begin{aligned} 0 &= \left[x + \frac{N}{2}\right]^4 - 2N\left[x + \frac{N}{2}\right]^3 + [N^2 - 3Ns - 3s^2]\left[x + \frac{N}{2}\right]^2 \\ &\quad + [3N^2s + 3Ns^2]\left[x + \frac{N}{2}\right] - 0.5[N^2s^2 + N^3s] \end{aligned} \quad (\text{A.11})$$

$$0 = x^4 - \left[\frac{N^2}{2} + 3Ns + 3s^2\right]x^2 + \left[\frac{N^4}{16} + \frac{N^3s}{4} + \frac{N^2s^2}{4}\right] \quad (\text{A.12})$$

Let $y = x^2$. Equation (A.12) can be further simplified into a quadratic equation and is expressed as:

$$0 = y^2 - \left[\frac{N^2}{2} + 3Ns + 3s^2 \right] y + \left[\frac{N^4}{16} + \frac{N^3s}{4} + \frac{N^2s^2}{4} \right]$$

$$y = \frac{N^2 + 6Ns + 6s^2 \pm 2p}{4} \quad (\text{A.13})$$

where $p = \sqrt{2N^3s + 11N^2s^2 + 18Ns^3 + 9s^4}$.

On the basis of Equation (A.13) and $y = x^2$, x can be expressed as:

$$x = \pm \frac{1}{2} \sqrt{N^2 + 6Ns + 6s^2 \pm 2p} \quad (\text{A.14})$$

On the basis of Equation (A.14) and $k = x + N/2$, k can be expressed as:

$$k_{1,2,3,4} = \frac{N}{2} \pm \frac{1}{2} \sqrt{N^2 + 6Ns + 6s^2 \pm 2p} \quad (\text{A.15})$$

There are four solutions, $k_{1,2,3,4}$, to $\frac{\partial \text{INL}}{\partial k} = 0$ as expressed in Equation (A.15). For the case of $0 \leq k \leq N$, there are two valid solutions, k_{pk} as expressed in Equation (A.16).

$$k_{pk} = \frac{N \pm \sqrt{q}}{2} \quad (\text{A.16})$$

where $q = N^2 + 6Ns + 6s^2 - 2p$.

On the basis of Equations (A.9) and (A.16), the INL_{pk} can be derived as:

$$\begin{aligned}
\text{INL}_{pk} = \text{INL}|_{k=k_{pk}} &= \frac{\left[\frac{N \pm \sqrt{q}}{2} \right] \left[N - \frac{N \pm \sqrt{q}}{2} \right] \left[N - 2 \frac{N \pm \sqrt{q}}{2} \right]}{2 \left[\frac{N \pm \sqrt{q}}{2} + s \right] \left[N - \frac{N \pm \sqrt{q}}{2} + s \right]} \\
&= \frac{\left[N \pm \sqrt{q} \right] \left[N \mp \sqrt{q} \right] \left[\mp \sqrt{q} \right]}{2 \left[N + 2s \pm \sqrt{q} \right] \left[N + 2s \mp \sqrt{q} \right]} = \frac{\left[\mp \sqrt{q} \right] \left[N^2 - q \right]}{2 \left[N^2 + 4Ns + 4s^2 - q \right]} \quad (\text{A.17})
\end{aligned}$$

On the basis of Equation (A.17) and $q = N^2 + 6Ns + 6s^2 - 2p$, INL_{pk} can be expressed as:

$$\text{INL}_{pk} = \pm \frac{\left[3s^2 + 3Ns - p \right]}{2 \left[s^2 + Ns - p \right]} \sqrt{N^2 + 6Ns + 6s^2 - 2p} \quad (\text{A.18})$$

On the basis of Equation (A.18), the worst-case INL, $|\text{INL}_{pk}|$ can be expressed as:

$$|\text{INL}_{pk}| = \frac{1.5s[s + N] - 0.5p}{s[s + N] - p} \sqrt{N^2 + 6s[s + N] - 2p} \quad (\text{A.19})$$

where $s = r_o/R_L$,

$N = 2^n - 1$, and

$$p = \sqrt{2N^3s + 11N^2s^2 + 18Ns^3 + 9s^4}.$$

A.3 Derivation of r_o as a Function of the Worst-Case INL

In Section A.2, the worst-case INL as a function of the output impedance has been derived as expressed in Equation (A.19). However, because of the format of Equation (A.19), it is difficult for circuit designers to obtain the r_o . Therefore, the derived Equation (A.19) needs to be re-expressed in the form r_o as a function of $|\text{INL}_{pk}|$.

First, let $s = t - N/2$ to simplify p and the following derivations.

$$\begin{aligned} p &= \sqrt{s[s+N][3s+N][3s+2N]} = \sqrt{\left[t^2 - \frac{N^2}{4}\right]\left[9t^2 - \frac{N^2}{4}\right]} \\ &= \frac{1}{4}\sqrt{144t^4 - 40N^2t^2 + N^4} \end{aligned} \quad (\text{A.20})$$

Furthermore, let $z = |\text{INL}_{pk}|$ to shorten the following derivations. On the basis of Equation (A.20) and $s = t - N/2$, z can be expressed as:

$$\begin{aligned} z = |\text{INL}_{pk}| &= \frac{\frac{3}{2}\left[t^2 - \frac{N^2}{4}\right] - \frac{p}{2}}{t^2 - \frac{N^2}{4} - p} \sqrt{N^2 + 6\left[t^2 - \frac{N^2}{4}\right] - 2p} \\ &= \frac{12t^2 - 3N^2 - 4p}{\left[4t^2 - N^2 - 4p\right]2\sqrt{2}} \sqrt{12t^2 - N^2 - 4p} \\ &= \frac{\left[12t^2 - 3N^2 - 4p\right]\left[4t^2 - N^2 + 4p\right]}{\left[\left[4t^2 - N^2\right]^2 - 16p^2\right]2\sqrt{2}} \sqrt{12t^2 - N^2 - 4p} \\ &= \frac{N^4 + 8N^2t^2 - 48t^4 + 16t^2p - 4N^2p}{t^2\left[N^2 - 4t^2\right]32\sqrt{2}} \sqrt{12t^2 - N^2 - 4p} \end{aligned}$$

$$z = \frac{[12t^2 + N^2 - 4p][N^2 - 4t^2]}{t^2[N^2 - 4t^2]32\sqrt{2}} \sqrt{12t^2 - N^2 - 4p}$$

$$z = \frac{12t^2 + N^2 - 4p}{t^2 32\sqrt{2}} \sqrt{12t^2 - N^2 - 4p} \quad (\text{A.21})$$

By squaring both sides of Equation (A.21), z^2 is derived as:

$$z^2 = \frac{[12t^2 - 4p + N^2]^2 [12t^2 - 4p - N^2]}{2048t^4}$$

$$= \frac{[12t^2 - 4p + N^2][144t^4 + 16p^2 - 96t^2p - N^4]}{2048t^4}$$

$$z^2 = \frac{[12t^2 - 4p + N^2][36t^2 - 12p - 5N^2]}{256t^2} \quad (\text{A.22})$$

By multiplying both sides of Equation (A.22) by $256t^2$, we obtain:

$$256t^2 z^2 = 432t^4 - 24N^2t^2 - 288t^2p + 48p^2 + 8N^2p - 5N^4$$

$$[36t^2 - N^2]4p = 432t^4 - [72N^2 + 128z^2]t^2 - N^4 \quad (\text{A.23})$$

Let the left-hand-side (LHS) of Equation (A.23) be z_1 . z_1^2 can be derived as:

$$z_1 = [36t^2 - N^2]4p$$

$$z_1^2 = [1296t^4 + N^4 - 72N^2t^2]16p^2$$

$$= [1296t^4 + N^4 - 72N^2t^2][144t^4 - 40N^2t^2 + N^4]$$

$$z_1^2 = 186624t^8 - 62208N^2t^6 + 4320N^4t^4 - 112N^6t^2 + N^8 \quad (\text{A.24})$$

Let the right-hand-side (RHS) of Equation (A.23) be z_2 . z_2^2 can be derived as:

$$\begin{aligned}
z_2 &= 432t^4 - [72N^2 + 128z^2]t^2 - N^4 \\
z_2^2 &= 186624t^8 + [72N^2 + 128z^2]^2 t^4 + N^8 - 864[72N^2 + 128z^2]t^6 \\
&\quad - 864N^4t^4 + 2[72N^2 + 128z^2]N^4t^2 \\
&= 186624t^8 + [5184N^4 + 16384z^4 + 18432N^2z^2]t^4 + N^8 \\
&\quad - [62208N^2 + 110592z^2]t^6 - 864N^4t^4 + [144N^2 + 256z^2]N^4t^2 \\
z_2^2 &= 186624t^8 + [4320N^4 + 16384z^4 + 18432N^2z^2]t^4 + N^8 \\
&\quad - [62208N^2 + 110592z^2]t^6 + [144N^2 + 256z^2]N^4t^2
\end{aligned} \tag{A.25}$$

On the basis of Equation (A.23), $z_1 = z_2$, and therefore:

$$z_1^2 - z_2^2 = 0 \tag{A.26}$$

Substitute Equations (A.24) and (A.25) into Equation (A.26):

$$\begin{aligned}
&[16384z^4 + 18432N^2z^2]t^4 - [110592z^2]t^6 + [256N^2 + 256z^2]N^4t^2 = 0 \\
&64t^2z^4 + 72N^2t^2z^2 - 432t^4z^2 + N^6 + N^4z^2 = 0 \\
&[432z^2]t^4 - [8z^2][8z^2 + 9N^2]t^2 - N^4[N^2 + z^2] = 0
\end{aligned} \tag{A.27}$$

Let $u = t^2$. Equation (A.27) can be further simplified as a quadratic equation and is expressed as:

$$[432z^2]u^2 - [8z^2][8z^2 + 9N^2]u - N^4[N^2 + z^2] = 0 \tag{A.28}$$

On the basis of Equation (A.28), u is derived as:

$$u = \frac{9N^2 + 8z^2}{108} \pm \frac{[3N^2 + 4z^2]^{1.5}}{108z} \quad (\text{A.29})$$

On the basis of Equation (A.29) and $u = t^2$, t can be derived as:

$$t = \pm \sqrt{\frac{9N^2 + 8z^2}{108} \pm \frac{[3N^2 + 4z^2]^{1.5}}{108z}} = \pm \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 \pm (3N^2 + 4z^2)^{3/2}}{z}} \quad (\text{A.30})$$

On the basis of Equation (A.30) and $s = t - N/2$, s can be derived as:

$$s = -\frac{N}{2} \pm \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 \pm [3N^2 + 4z^2]^{1.5}}{z}} \quad (\text{A.31})$$

There are five solutions to Equation (A.26) where four solutions are expressed in Equation (A.31) and the last solution is $s = -N/2$, i.e., $t = 0$. As $s = r_o/R_L$, only positive real number solutions are applicable. The said five solutions are verified in the following.

The First and Second Solutions

The first and second solutions, $s_{1,2}$, are expressed in Equation (A.32)

$$s_{1,2} = -\frac{N}{2} \pm \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 - [3N^2 + 4z^2]^{1.5}}{z}} \quad (\text{A.32})$$

To verify that $s_{1,2}$ are not complex number, $9N^2z + 8z^3 - (3N^2 + 4z^2)^{1.5} \geq 0$ is verified as follow:

$$9N^2z + 8z^3 - [3N^2 + 4z^2]^{1.5} \stackrel{?}{=} 0$$

$$[9N^2z + 8z^3]^2 \stackrel{?}{=} [3N^2 + 4z^2]^3$$

$$81N^4z^2 + 64z^6 + 144N^2z^4 \stackrel{?}{=} [3N^2 + 4z^2][9N^4 + 16z^4 + 24N^2z^2]$$

$$81N^4z^2 + 64z^6 + 144N^2z^4 \stackrel{?}{=} 27N^6 + 144N^2z^4 + 108N^4z^2 + 64z^6$$

$$0 < 27N^6 + 27N^4z^2$$

$$0 < N^2 + z^2$$

As the LHS is less than the RHS, $9N^2z + 8z^3 - [3N^2 + 4z^2]^{1.5} < 0$. Therefore, the solutions $s_{1,2}$ are not applicable here because they are complex numbers.

The Third Solution

The third solution, s_3 , is expressed in Equation (A.33). This solution is also not applicable as it is a negative number.

$$s_3 = -\frac{N}{2} - \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 + [3N^2 + 4z^2]^{1.5}}{z}} \quad (\text{A.33})$$

The Fourth Solution

The fourth solution, s_4 , is expressed in Equation (A.34).

$$s_4 = -\frac{N}{2} + \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 + [3N^2 + 4z^2]^{1.5}}{z}} \quad (\text{A.34})$$

s_4 can be verified as follows:

$$\begin{aligned} & -\frac{N}{2} + \frac{\sqrt{3}}{18} \sqrt{\frac{9N^2z + 8z^3 + [3N^2 + 4z^2]^{1.5}}{z}} > 0 \\ & \sqrt{9N^2z + 8z^3 + [3N^2 + 4z^2]^{1.5}} > 3N\sqrt{3z} \\ & 9N^2z + 8z^3 + [3N^2 + 4z^2]^{1.5} > 27Nz \\ & [3N^2 + 4z^2]^3 > [27Nz - 9N^2z - 8z^3]^2 \\ & 27N^6 + 144N^2z^4 + 108N^4z^2 + 64z^6 > 729N^2z^2 + 81N^4z^2 + 64z^6 - 486N^3z^2 \\ & \quad - 432Nz^4 + 144N^2z^4 \\ & 27N^6 + 27N^4z^2 > 729N^2z^2 - 486N^3z^2 - 432Nz^4 \\ & N^6 + N^4z^2 > 27N^2z^2 - 18N^3z^2 - 16Nz^4 \\ & N^5 + 16z^4 + [N^2 + 18N - 27]Nz^2 > 0 \end{aligned} \quad (\text{A.35})$$

The inequality in Equation (A.35) is valid if the term $N^2 + 18N - 27 > 0$ and this can be verified as follows:

$$N^2 + 18N - 27 > 0$$

$$N > 1.39$$

$$2^n - 1 > 1.39$$

$$2^n > 2.39$$

$$n > 1.26$$

$$n \geq 2$$

Therefore, s_4 is valid for $n \geq 2$. But for the sake of completeness, s_4 is also verified for $n = 1$ by substituting $N = 2^1 - 1 = 1$ into Equation (A.35) as expressed below.

$$1 + 16z^4 + [1 + 18 - 27]z^2 > 0$$

$$16z^4 - 8z^2 + 1 > 0$$

$$[4z^2 - 1]^2 > 0$$

As z is ≥ 0 and a real number, the solution s_4 is also valid for $n = 1$. Therefore, s_4 is valid for $n \geq 1$ bit.

The Fifth Solution

The fifth and last solution $s_5 = -0.5N$ is not applicable here because it is a negative number.

On the basis of these verifications, only s_4 is the applicable solution for Equation

(A.26). By substituting $s = r_o/R_L$ and $z = |\text{INL}_{pk}|$ into s_4 , r_o can be derived as:

$$r_o = R_L \left[-\frac{N}{2} + \frac{\sqrt{3}}{18} \sqrt{9N^2 + 8\text{INL}_{pk}^2 + \frac{[3N^2 + 4\text{INL}_{pk}^2]^{1.5}}{|\text{INL}_{pk}|}} \right] \quad (\text{A.36})$$

where n and $N \geq 1$, and

$$r_o, R_L, \text{ and } |\text{INL}_{pk}| \geq 0.$$

The derived Equation (A.36) is applicable to all possible DAC resolutions $n \geq 1$ and $|\text{INL}_{pk}|$ values.

Note that for typical CS-DACs with $n > 3$ and $|\text{INL}_{pk}| \leq 0.5\text{LSB}$, Equation (A.36) can be simplified further into Equation (A.37) without significantly reduce its precision.

$$r_o \cong \frac{NR_L}{6} \left[-3 + \sqrt{3 + \frac{N\sqrt{3}}{|\text{INL}_{pk}|}} \right] \quad (\text{A.37})$$

Both Equations (A.36) and (A.37) provide precise expressions on the relationship between r_o and INL that is critical in the design of the current-sources of CS-DACs.

A.4 Verification of the Derived Relationship between the Output Impedance and INL

In this section, the precision of the derived relationship in Equation (A.36) is verified against computer simulations. Figure A.2 depicts the said relationships based on the derived Equation (A.36) and the simulation results for $\text{INL} = 0.5\text{LSB}$ and $n = 6, 7 \dots 16$ bit, where $R_L = 50\Omega$. It can be observed that the required output impedance increases exponentially as the DAC resolution increases linearly.

Figure A.3 depicts the comparison between the required r_o on the basis of Equation (A.36) and the simulation results across different INL peak values, for $n = 12, 13 \dots 16$ bit, where $R_L = 50\Omega$. Note that our derived Equation (A.36) matches the simulation results and this verifies the precision and correctness of our derived equation.

Figure A.2 Comparison between required r_o on the basis of Equation (A.36) and the simulation results, for

$INL = 0.5LSB$ and $n = 6, 7 \dots 16$ bit, where $R_L = 50\Omega$

Figure A.3 Comparison between the required r_o on the basis of Equation (A.36) and the simulation results across different INL peak values, for $n = 12, 13 \dots 16$ bit, where $R_L = 50\Omega$

Chapter 4

A Calibration-Free/DEM-Free 8-bit 2.4GS/s DAC with a Distributed Biasing Scheme

4.1 Introduction

A large portion of this chapter has been submitted to IEEE Journal of Solid State Circuit.

Real-time surveillance by means of unmanned aerial vehicles (UAVs), embodying high reliability electronics [110, 111], is an emerging application for remote aerial surveillance. In UAV surveillance system, the high resolution real-time uncompressed video requires a high data-rate low-latency wireless communication system to facilitate real-time time operation [3]. In the wideband transmitter therein, the DAC converts digital data from the back-end digital signal processor to wideband analog signals [34, 87]. As the system latency needs to be short, the preferred realization of the wideband DAC is a single-core high-speed Nyquist DAC without requiring calibration/DEM. Further, the DAC should not require auxiliary circuits (e.g., time-interleaving circuit [12, 85], DEM shufflers, etc.) to feature small IC area and simplified hardware for low cost and low power dissipation.

The CS-DAC is an appropriate DAC architecture to generate wideband signals for wideband transmitters because of their high speed and appropriate resistive loads driving-capability without needing wideband buffers. Amongst the reported CS-DACs [26, 27, 82, 93], the pseudo-segmented (binary) CS-DAC architecture is particularly attractive in view of its low latency, fast operation, small chip size, low hardware complexity, and low power dissipation [13].

Nevertheless, the pseudo-segmented architecture [13, 93] inherently suffers from unwanted spurs, leading to relatively poor linearity. Specifically, the linearity of the pseudo-segmented CS-DAC is severely affected by the following three primary non-ideal parameters [17, 22, 23, 57]. First, because of its finite DAC output impedance which varies with different input data, the ensuing DAC linearity is compromised [24]. The compromised linearity is exacerbated at high (GHz) frequencies because the output impedance decreases substantially due to the parasitic capacitance therein [22, 24]. Second, the delay differences between the current-switches control signals could introduce unwanted output glitches, particularly at the mid-code transition, which may in turn worsen the dynamic linearity [13, 22] of the DAC. Other types of delay differences that affect DAC linearity have also been reported in literature [17, 57]. Third, the current mismatch (due to the random process variations and the process gradient) between the current-sources is particularly undesirable because the pseudo-segmented operation is not inherently monotonic [13, 21, 27]. In view of this, the current matching for the pseudo-segmented CS-DAC is more critical than its unary/segmented counterparts [13], and output currents with a higher accuracy are needed.

Further to the imperative needs to optimize the aforesaid three non-ideal parameters, there are trade-offs between these parameters which exacerbate the complexity of the design and optimization of the CS-DAC. The first trade-off is between the output impedance and the current mismatches. The general approach to mitigate the current mismatch is to enlarge the transistor size [13, 25, 26], but this undesirably reduces the output impedance at high frequencies. The second trade-off is between the current mismatches (particularly due to process gradient) and the delay differences. To compensate for the process gradient errors, complex routing schemes [24, 27] that employ a current-source (or current-cell) matrix are generally used. These schemes, however, may inadvertently increase the delay differences in view of complex routing interconnections. Put simply, the concurrent optimization of all three non-ideal parameters for CS-DACs is generally intractable, largely because the optimization is constrained by the trade-offs between these parameters, and the said constraints become increasingly exacerbated at high (GHz) frequencies.

Reported techniques to mitigate the said non-ideal parameters, include calibrations [18-20], DEM [21-23, 73], etc. These techniques, however, generally do not improve the linearity performance when the operating frequency is in the GHz range because the matching problem is no longer the limiting factor [24]. For example, calibrations constrain the DAC operating speed as it typically involves additional parasitic capacitance at the DAC output [18]. DEM [22, 23], on the other hand, involves relatively slow and complex digital circuits, including a thermometer decoder and DEM shufflers, which increase the DAC latency, hardware complexity, and power dissipation.

In this chapter, we present an 8-bit 2.4-GS/s pseudo-segmented CS-DAC that embodies our proposed distributed biasing scheme to largely decouple the said trade-offs, yet without needing any calibration/DEM. The ensuing desired outcome is improved linearity parameters. Specifically, the INL and DNL of a CS-DAC prototype realized with 65nm low power CMOS are within $\pm 0.097\text{LSB}$ and $-0.05/0.15\text{LSB}$ respectively – a respective improvement of up to 0.48LSB and 0.89LSB over the conventional (non-distributed) biasing scheme, see Section 4.2 later.

At 2.4GS/s conversion rate, the SFDR of the CS-DAC is $>47.8\text{dBc}$ across the Nyquist bandwidth while dissipating 26.4mW from $1.2\text{V}/2\text{V}$ supplies. On particular pertinence, these improved linearity parameters are obtained without calibration/DEM. We also propose a custom in-situ DPG to simplify testing and hence the ensuing costs associated with testing during manufacturing. The DPG generates $8\times 2.4\text{Gb/s}$ periodic test pattern with small hardware overheads, no time-interleaving, and low I/O pin count. Further, as the DPG can be programmed externally at low data rate (e.g., $8\times 2.3\text{Mb/s}$), high-speed data I/O circuits are not required.

This chapter is organized as follows. Section 4.2 succinctly reviews the CS-DAC architecture as a preamble to the ensuing proposed distributed biasing scheme. Section 4.3 discusses the design and implementation of the critical building blocks. Section 4.4 describes the design of the proposed in-situ DPG. Section 4.5 presents the measurement results of the CS-DAC prototype IC and benchmarking against the state-of-the-art DACs. Finally, conclusions are drawn in Section 4.6.

4.2 CS-DAC Architecture

In this section, we will first succinctly describe the system-level design of the proposed CS-DAC. Thereafter, we will delineate the proposed technique that simultaneously improves the aforesaid three non-ideal parameters largely by decoupling their trade-offs, yet without calibration/DEM.

The CS-DAC architecture [13, 75] is well established. Figure 4.1 depicts the floorplan/block diagram of the proposed pseudo-segmented CS-DAC embodying our in-situ Gb/s DPG [87]. In the conventional design [13, 75], the DPG is absent, and the bias circuit and analog blocks are designed differently. Our CS-DAC design is effectively binary-weighted by means of a 5+3 pseudo-segmentation, i.e., a pseudo-unary 5-bit coarse sub-DAC and a binary 3-bit fine sub-DAC. The pseudo-unary architecture [13] is adopted herein for the coarse sub-DAC to exploit the high current-accuracy of the unary topology in the analog blocks, and the low hardware complexity of the binary design in the digital blocks. The coarse sub-DAC employs a pseudo-decoder [13] to buffer the 5 bits of data based on their binary weighting into 31 bits control signals which control the 31 unary current-sources. The binary architecture [22, 24, 73] is routinely employed for fine sub-DACs. The coarse and fine sub-DACs employ the same input synchronization register, switch-driver, and current-switch blocks.

Figure 4.1 Floorplan/block diagram of the proposed 8-bit 2.4-GS/s CS-DAC including the in-situ digital pattern generator

Figure 4.2 depicts the simplified schematic of the proposed current-sources, current-switches, and bias circuit. There are 31 unary ($I_{u31} \dots I_{u1}$) and 3 binary ($I_{b3} \dots I_{b1}$) currents that constitute the DAC output, and the bias circuit outputs 34 bias currents ($I_{34} \dots I_1$). Each current-source is based on the cascode current mirror topology wherein each pair of source-mirror transistors independently copies one of the 34 output bias currents.

Figure 4.2 Simplified schematic diagram of the current-sources, current-switches, and the bias circuit

By individually biasing the current-sources, the three non-ideal parameters (the output impedance, delay differences, and current mismatches) can concurrently be improved by largely decoupling the two primary trade-offs as follows.

The first trade-off between the output impedance and the current mismatches is largely decoupled as the current-matching is improved and the current-matching requirement is alleviated in the proposed distributed biasing scheme. Specifically, in the proposed distributed biasing scheme, as the source-mirror transistors (of each current-source) are placed in close proximity, higher current matching and reduced process gradient error are obtained; a reported study on matching [112] demonstrated $>1.5\times$

improvement. In addition, the linearity of the DAC is further improved by the cross-correlations between the current-sources in the proposed distributed biasing scheme.

To depict these attributes, Table 4.1 tabulates the cross-correlation coefficients between the binary-equivalent currents ($I_{MSB} \dots I_{MSB-4}$) of the unary current-sources ($I_{u31} \dots I_{u1}$) for the conventional (non-distributed) and for the proposed distributed biasing schemes based on 1000-run Monte-Carlo simulations. The cross-correlations, particularly between I_{MSB} and $I_{MSB-1} \dots I_{MSB-4}$ in the proposed distributed biasing scheme, are substantially improved. For example, the cross-correlation coefficient between I_{MSB} and I_{MSB-1} is now $4.2\times$ higher than that in the conventional counterpart. Intuitively, this would lead to an improved DNL as the variations of the current step-size $\sigma^2(\Delta I)$ would decrease. Analytically, we can show that this is the case. Assuming the current variations of $I_{b3} \dots I_{b1}$ are negligible, we derive the relationship between the mid-code current step-size $\sigma^2(\Delta I_{mid})$ and the current variations (including their cross-correlations) for our CS-DAC as:

$$\sigma^2(\Delta I_{mid}) \approx \sum_{i=MSB-4}^{MSB} \sigma_i^2 - 2\sigma_{MSB} \sum_{i=MSB-4}^{MSB-1} \sigma_i \rho_{i,MSB} + 2 \sum_{i=MSB-4}^{MSB-2} \sum_{j=i+1}^{MSB-1} \sigma_i \sigma_j \rho_{i,j} \quad (4.1)$$

where ΔI_{mid} is the current step size at the mid-code,

$I_{MSB} \dots I_{MSB-4}$ are the binary-equivalent of $I_{u31} \dots I_{u1}$,

σ is the standard-deviation, and

ρ is the cross-correlation coefficient.

Table 4.1 Cross-correlation coefficients (%) between the binary-equivalent currents of

 $I_{MSB} \dots I_{MSB-4}$ for the conventional and proposed distributed biasing schemes

Conventional		I_{MSB}	I_{MSB-1}	I_{MSB-2}	I_{MSB-3}	I_{MSB-4}
	I_{MSB}		-10	-10	-9	-7
	I_{MSB-1}	-10		-9	-7	1
	I_{MSB-2}	-10	-9		-4	-5
	I_{MSB-3}	-9	-7	-4		-3
	I_{MSB-4}	-7	1	-5	-3	

Proposed		I_{MSB}	I_{MSB-1}	I_{MSB-2}	I_{MSB-3}	I_{MSB-4}
	I_{MSB}		42	27	20	15
	I_{MSB-1}	42		22	21	8
	I_{MSB-2}	27	22		15	12
	I_{MSB-3}	20	21	15		7
	I_{MSB-4}	15	8	12	7	

Based on Equation (4.1), high (positive) cross-correlation coefficients between I_{MSB} and $I_{MSB-1} \dots I_{MSB-4}$ (see Table 4.1), reduce $\sigma^2(\Delta I_{mid})$, and improve the DNL. As the current matching and the DAC static linearity are now substantially improved, higher random process variations can be tolerated. Specifically, small-sized transistors can now be employed and are placed in close proximity to obtain higher output impedance (at GHz operation).

The second trade-off between the current mismatches due to process gradient errors and the delay differences is also largely decoupled. Assuming that the bias currents are accurate, the process gradient errors are largely negligible because the source-mirror transistors in each current-source are placed in close proximity (<2 μm spacing

distance). This consequently permits the optimized placement of the CS-DAC building blocks to match the interconnections length and shape (particularly between the different current-switches and their respective switch-drivers) to significantly reduce the delay differences. For example, the one-dimensional layout [24] placement allows straightforward interconnections between two adjacent blocks in Figure 4.1 to achieve an excellent delay matching.

In short, our proposed distributed biasing scheme effectively mitigates the aforesaid two trade-offs by partially shifting the design issues (e.g., current mismatches, delay differences, etc.) associated with the process gradient from the current-sources to the bias circuit. This means that a bias circuit with high accuracy outputs is required in the proposed distributed biasing scheme to reduce the current mismatches of the current-sources. Nevertheless, because the bias circuit does not affect the DAC conversion rate and/or its output impedance at high frequencies, the high-accuracy requirement can be easily achieved with large transistor sizes and a process gradient cancelation technique. The bias circuit design will be delineated in Section 4.3.2 later.

To depict the significance of our proposed distributed biasing scheme, its performance is compared with the conventional biasing scheme by means of 1000-run Monte-Carlo simulations based on the same transistor sizes. Figure 4.3 depicts the statistical distribution of the INL and DNL based on the conventional and proposed distributed biasing schemes from 1000-run Monte-Carlo simulations. It can be observed that the worst-case INL and DNL are significantly improved by 0.48LSB ($= 0.81\text{LSB} - 0.33\text{LSB}$) and 0.89LSB ($= 1.23\text{LSB} - 0.34\text{LSB}$) respectively.

Figure 4.3 Statistical distributions of the DNL and INL based on the conventional and proposed biasing schemes from 1000-run Monte-Carlo simulations

4.3 Building Blocks

Consider now the circuit-level design of the critical building blocks of the proposed CS-DAC: the current-sources, bias circuit, current-switches, and switch-drivers.

4.3.1 Current-Sources

As mentioned earlier, the primary design parameters for the current-source are its output impedance and current matching, and for yield of $\geq 99.7\%$, we can show that $INL < 0.5LSB$ and $SFDR > 42dBc$. We will now succinctly delineate these two design parameters in turn.

4.3.1.1 Output Impedance

To estimate the required output impedance for $INL < 0.5LSB$, we derive Equation (4.2) from our earlier derived Equation (3.3) in Section 3.2.1 for CS-DAC with $INL < 0.5LSB$. The error of Equation (4.2) is $< 0.2\%$ when $n > 3$ -bit.

$$Z_{o,cs} \cong \frac{NR_L}{6} \left[-3 + \sqrt{3 + \frac{N\sqrt{3}}{|INL_{pk}|}} \right] \quad (4.2)$$

where $Z_{o,cs}$ is the LSB current-source output impedance (Ω),

INL_{pk} is the peak INL (LSB),

R_L is the load resistance (Ω),

$$N = 2^n - 1,$$

n is the DAC resolution (bit).

From Equation (4.2), and for $\text{INL} < 0.5\text{LSB}$ and R_L of 50Ω , the estimated $Z_{o,cs}$ is $>57\text{k}\Omega$. Note that as the estimated $Z_{o,cs}$ is for static INL at DC, the $Z_{o,cs} > 57\text{k}\Omega$ requirement needs to be extended across the entire DAC bandwidth to maintain high DAC linearity at high frequencies.

To ascertain the required $Z_{o,cs}$ for $\text{SFDR} > 42\text{dBc}$, we perform extensive MATLAB simulations based on the CS-DAC model depicted in Figure 4.4.[‡] Each current-source is modeled as an ideal current-source in parallel with a parasitic element $|Z_{o,cs}|$, while R_L is 50Ω and the current-switches are assumed to be ideal. Figure 4.5 depicts the simulated minimum SFDR ($\text{SFDR}_{\min}$) for different $|Z_{o,cs}|$. The required $|Z_{o,cs}|$ for $\text{SFDR} > 42\text{dBc}$ is $>32\text{k}\Omega$. Note that the $\text{SFDR}_{\min}$ saturates as the $Z_{o,cs}$ increases beyond $100\text{k}\Omega$ and therefore it is unnecessary to design $Z_{o,cs} \gg 110\text{k}\Omega$.

Figure 4.4 CS-DAC model employed in the MATLAB's SFDR simulations

[‡] See Appendix B for our developed model for the relationship between the output impedance and SFDR.

Figure 4.5 Relationship between $SFDR_{min}$ and the output impedance of the LSB current-source for an 8-bit CSDAC

In summary, the estimated required $Z_{o,cs}$ for $INL < 0.5LSB$ and $SFDR > 42dBc$ is $> 57k\Omega$. In our CS-DAC, the designed $Z_{o,cs}$ is $> 100k\Omega$ across the Nyquist bandwidth for an additional margin.

4.3.1.2 Current Matching

As mentioned in Section 4.2, the proposed distributed biasing scheme improves the current matching by means of placing the source-mirror transistors in close proximity and by means of the increased cross-correlations between the current-sources. This subsequently permits the design of the current-source transistors in the proposed CS-DAC (for $INL < 0.5LSB$) to be smaller.

Based on extensive simulations, a current matching of $\sigma(I_{MSB})/I_{MSB}=0.18\%$ is sufficient for INL and DNL of $<0.5\text{LSB}$ in the proposed distributed biasing scheme. This estimated required current matching is $\sim 2\times$ less stringent than that ($\sigma(I_{MSB})/I_{MSB}=0.088\%$ [16]) in the conventional (non-distributed) biasing scheme counterpart with uncorrelated current-sources. This implies that the current-sources size can be designed smaller. Figure 4.3 depicts the statistical parameters of the designed current-sources featuring $\text{INL}<0.5\text{LSB}$ with the yield of $\geq 99.7\%$.

4.3.2 Bias Circuit

In the proposed distributed biasing scheme, as the mismatches of the current-sources are in part dependent on the accuracy of the bias currents, it is necessary to design the bias circuit to output accurate bias currents. Note that as the bias circuit does not affect the parasitic capacitance at the CS-DAC output (or other critical paths), it can embody large-sized transistors for higher current accuracy without degrading the CS-DAC output impedance or bandwidth.

The bias circuit is configured in a 16×16 matrix (255 unit bias currents and a dummy (black cell)) as depicted in Figure 4.6 to reduce process gradient errors, particularly that of the unary current-sources. Each bias matrix cell consists of the index of a unit bias current ($I=I_{LSB}$) where cells with identical indices are connected in parallel (except I_1 and the dummy) to form the bias currents $I_{34}\dots I_4$ and $I_3\dots I_1$ for the unary and binary current-sources respectively in Figure 4.2.

The primary objective here is to mitigate the process gradient error of $I_{34}...I_4$. Specifically, each of the bias currents $I_{34}...I_4$ is subdivided into 16 unit bias currents (i.e., 16 cells) that are evenly distributed and interdigitated in the matrix to mitigate both linear and quadratic gradient errors therein. For example, the unit bias currents of I_{34} are evenly spread along the abscissa in x ($x=x_1, x_3...x_{15}$) and ordinate in y ($y=y_2, y_4...y_{16}$) spaces in Figure 4.6. In this manner, the process gradient error is averaged down and hence mitigated.

y_{16}	19	33	34	4	5	6	7	8	17	18	3	20	21	22	23	24
y_{15}	9	10	11	12	13	14	15	16	25	26	27	28	29	30	31	32
y_{14}	17	18	2	20	21	22	23	24	34	4	5	6	7	8	19	33
y_{13}	25	26	27	28	29	30	31	32	11	12	13	14	15	16	9	10
y_{12}	34	4	5	6	7	8	19	33	2	20	21	22	23	24	17	18
y_{11}	11	12	13	14	15	16	9	10	27	28	29	30	31	32	25	26
y_{10}	3	20	21	22	23	24	17	18	5	6	7	8	19	33	34	4
y_9	27	28	29	30	31	32	25	26	13	14	15	16	9	10	11	12
y_8	5	6	7	8	19	33	34	4	21	22	23	24	17	18	1	20
y_7	13	14	15	16	9	10	11	12	29	30	31	32	25	26	27	28
y_6	21	22	23	24	17	18	3	20	7	8	19	33	34	4	5	6
y_5	29	30	31	32	25	26	27	28	15	16	9	10	11	12	13	14
y_4	7	8	19	33	34	4	5	6	23	24	17	18	3	20	21	22
y_3	15	16	9	10	11	12	13	14	31	32	25	26	27	28	29	30
y_2	23	24	17	18		20	21	22	19	33	34	4	5	6	7	8
y_1	31	32	25	26	27	28	29	30	9	10	11	12	13	14	15	16
	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}	x_{12}	x_{13}	x_{14}	x_{15}	x_{16}

Figure 4.6 Bias circuit 16×16 matrix. The bias currents, particularly of the unary current-sources (e.g., the highlighted I_{34}), are evenly distributed in the abscissa x and ordinate y spaces. The black cell is a dummy

To verify the effectiveness of the bias current matrix in reducing process gradient, the linear and quadratic gradients are modeled and simulated by using MATLAB. Consider first the linear gradient error. The linear gradient error of a unit bias current is modeled with Equation (4.3) where different linear gradient angles are considered.

$$I_{err,lin}(x, y) = a(x\cos\theta + y\sin\theta) \quad (4.3)$$

where $I_{err,lin}$ is the linear gradient error of a unit bias current,

a is the scale factor for the linear gradient error,

θ is the linear gradient angle, and

(x, y) is the unit bias current location.

Based on Equation (4.3), by means of the bias circuit configured in a 16×16 matrix, the linear gradient maximum error of $I_{34} \dots I_4$ is reduced to $|0.5a(\cos\theta \pm \sin\theta)|$. Figure 4.7 illustrates two different 2% ($\pm 1\%$) linear gradient error distributions that correspond to two different linear gradient angles, $\theta = 45^\circ$ and $\theta = 90^\circ$. Figure 4.8 depicts the MATLAB simulated current errors in $I_{34} \dots I_4$ due to 2% linear gradient errors across the complete 360° linear gradient angles at 5° steps. The maximum current error $I_{34} \dots I_4$ is very significantly reduced ($15\times$ lower) to $\pm 0.067\%$.

Figure 4.7 Linear gradient error (%) distributions for two different linear gradient angles, 45° and 90°

Figure 4.8 Simulated current error (%) in $I_{34} \dots I_4$ due to the linear gradient errors across the complete 360° linear angles at 5° steps

Consider now the quadratic gradient error. We model the quadratic gradient as a two-dimensional parabolic function in Equation (4.4).

$$I_{err,quad}(x, y) = b \left((x + x_{peak})^2 + (y + y_{peak})^2 \right) \quad (4.4)$$

where $I_{err,quad}$ is the quadratic gradient current error of a unit bias current,

b is the scale factor for the quadratic gradient error, and

(x_{peak}, y_{peak}) is the quadratic gradient peak location.

Figure 4.9 illustrates two different 2% (-1.4% to 0.6%) quadratic gradient error distributions that correspond to two different peak locations. Figure 4.10 depicts the MATLAB simulated maximum (absolute) current errors in $I_{34} \dots I_4$ due to 2% quadratic gradient errors for 256 quadratic gradient peak locations across the bias matrix. By means of the bias current configured in a 16×16 matrix, the maximum current errors are very significantly reduced. Specifically, the quadratic gradient errors when the quadratic gradient peak is at the center of the matrix is effectively nullified (reduced by $100\times$) – the maximum current errors of $I_{34} \dots I_4$ is $<0.01\%$. Conversely, when the peak locations are at the corners, the maximum current errors are also very significantly reduced $15\times$ lower to 0.067% . This is now comparable to that due to linear gradient error.

In summary, by means of the proposed bias current configured in a 16×16 matrix, both the linear and the quadratic gradient errors in $I_{34} \dots I_4$ are very significantly reduced by at least $15\times$.

Figure 4.9 Quadratic gradient error (%) distributions for two different quadratic gradient peak locations, (x_8, y_8) and (x_{16}, y_{16})

Figure 4.10 Simulated maximum (absolute) current error (%) in $I_{34} \dots I_4$ due to the quadratic gradient errors with different quadratic gradient peak locations

4.3.3 Current-Switches

Figure 4.2 depicts the schematic of current-switches that steer the output currents of the current-sources to the external load based on the digital inputs. The current-switches employ cascode transistors $M_{SW,CAS}$ to reduce the signal fluctuations (due to output signals) and unwanted parasitic capacitance variations [16] at the M_{SW} drain. The ensuing DAC non-linearity is hence mitigated.

The switching transistors M_{SW} are designed with the minimum size allowed ($(W/L)_{LSB}=410\text{nm}/60\text{nm}$). This is for low parasitic capacitance to increase the switching speed and to reduce the load, hence the power dissipation and area, of the switch-drivers and other digital blocks. Although small-sized transistors degrade the threshold matching, it is in part compensated by the fast switching speed (in part due to low parasitic capacitance) of the switch-driver [26, 74].

4.3.4 Switch-Drivers

The switch-driver outputs the control signals for the current-switches whilst mitigating the DAC output glitches. For the latter, the switch-driver needs to ascertain that the control signals feature:

- (i) Low delay differences (i.e., well synchronized control signals) [13],
- (ii) Short transition time for short DAC settling time [26], and

- (iii) Proper crossing level/point to ensure that the current-switches are never simultaneously turned off [16, 74].

Figure 4.11 depicts the switch-driver circuit that adopts topology in [42]. To satisfy (i) above, the D flip-flop re-synchronizes the single-ended output of the preceding digital blocks, and subsequently converts it into a differential signal. Transistors M_{1-4} buffers the D flip-flop outputs into differential control signals (P , N) with short transition time to satisfy (ii). The short transition time can be achieved with relatively small transistor size as the ensuing current-switches have small gate capacitance. To satisfy (iii), the positive feedback transistors $M_{5,6}$ [13] are included to optimize the crossing level of the control signals (P , N) to the desired point ($\text{half-}V_{DD,dig}$) by adjusting their rise/fall times.

Figure 4.11 Schematic diagram of the switch-driver

On the basis of 200-run Monte-Carlo simulations, the switch-driver design is shown to achieve a short (20%–80%) transition time of $12.1 \pm 4.2\text{ps}$ and $\text{half-}V_{DD,dig}$ crossing

level of $645 \pm 70 \text{ mV}$ ($> V_{TH}$ of M_{SW} , i.e., the M_{SW} pair is never simultaneously off), hence satisfying (ii) and (iii) respectively.

4.4 In-Situ Digital Pattern Generator (DPG)

Our proposed in-situ DPG facilitates the generation of high-speed $8 \times 2.4 \text{ Gb/s}$ periodic test pattern required in DAC measurements, thereby significantly reducing the hardware complexity, I/O pins, and active area. Figure 4.12 depicts the block diagram of the proposed DPG where it comprises 8 unit DPGs, $DPG_8 \dots DPG_1$, to generate the 8-bit DAC inputs, $B_8 \dots B_1$. Each unit DPG comprises of a shift-register (128 edge-triggered D flip-flops FF in series), a switch SW , and an output D flip-flop FF_Q .

Figure 4.12 Simplified block diagram of the proposed in-situ DPG

The DPG has two basic operation modes: WRITE and READ modes. During the WRITE mode, CK is set to CK_{SLOW} (2.3MHz) and the shift registers are in the open-loop state. The external periodic data, $IN_8 \dots IN_1$, are pushed into the FF s based on CK_{SLOW} and this effectively removes the need for high-speed I/O circuits and/or a high-speed external DPG. When the periodic test pattern data have been completely pushed into and stored in the shift-registers, the DPG is switched to the READ mode by toggling the $CTRL$ signal.

During the READ mode, CK is set to CK_{FAST} (2.4GHz) and each shift-register is configured into a closed-loop by switching SW . Because of the closed-loop state, the written data are remained stored in the shift-registers and sequentially shifted between FF s in every clock cycle. This modality enables high-speed periodic pattern generation without address signals, thereby reducing the I/O pin count and simplifying the hardware. Lastly, FF_Q re-synchronizes and buffers the generated periodic data at the mid-point of the shift-registers.

In summary, the inclusion of the proposed DPG on-chip significantly reduces the hardware and measurement costs as well simplifying the testing process of the high-speed CS-DAC.

4.5 Measurement and Benchmarking

Figure 4.13 depicts the photomicrograph of the IC chip realized in a commercial 65nm low power CMOS process embodying our proposed CS-DAC (core DAC: 0.22mm^2), bias circuit (0.13mm^2), and the in-situ DPG (0.24mm^2). Each building block is shielded by multiple guard rings to minimize the digital switching noise. The clock grid distribution network is adopted to ensure low timing skew. The CS-DAC (including the bias circuit) dissipates 26.4mW when the output frequency is set to 1.13GHz , and the DPG dissipates 63.5mW .

Figure 4.13 Photomicrograph of the CS-DAC prototype IC

Figure 4.14 depicts the plots of the measured $\text{INL}=\pm 0.097\text{LSB}$ and $\text{DNL}=-0.05/0.15\text{LSB}$ of the CS-DAC prototype. On the basis of the INL and DNL plots, it can be observed that our CS-DAC design is monotonic and achieves static linearity equivalent to ~ 11 -bit accuracy. We attribute these attributes to our proposed

biasing scheme that decouples two critical trade-offs, and to the appropriate design methodologies described in Sections 4.2 and 4.3.

Figure 4.14 Measured INL and DNL of the CS-DAC prototype IC

Figure 4.15 depicts the measured spectra with a single-tone close to the Nyquist bandwidth, at 1.13GHz. The measured SFDR is 47.84dBc. Figure 4.16 depicts the measured SFDR against the output signal frequency. The SFDR is $>47.8\text{dBc}$ across the Nyquist bandwidth. Figure 4.17 depicts the output spectra for the two-tone test at 2.4GS/s. The two-tone frequencies are 658MHz and 729MHz, and the ensuing third order intermodulation spurs are $\leq -52\text{dBc}$.

Figure 4.15 Measured CS-DAC output spectra with a single-tone at 1.13GHz. The SFDR is 47.84dBc

Figure 4.16 Measured SFDR of the CS-DAC prototype IC across the Nyquist bandwidth

Figure 4.17 Measured output spectra for a two-tone signal ($f_1=658\text{MHz}$, $f_2=729\text{MHz}$) at 2.4GS/s

Table 4.2 tabulates the benchmarking of our CS-DAC against the state-of-the-art DACs. The DAC in this benchmarking table is divided into two categories where the four left-most DACs are calibration-free/DEM-free while the five right-most DACs require calibration/DEM. On the basis of this table, we make the following comments.

First, the linearity parameters (SFDR, INL and DNL) of our CS-DAC are very competitive when compared to state-of-the-art DACs. Of specific interest, amongst state-of-the-art calibration-free/DEM-free DACs, our CS-DAC features the highest SFDR, and its INL and DNL are competitive – particularly given that our CS-DAC is binary-weighted and is calibration-free/DEM-free.

Table 4.2 Benchmarking of the proposed CS-DAC against state-of-the-art 6-bit to 10-bit GHz DACs

Parameters	This work	TVLSI '16 [93]	ISSCC '11 [12]	TMTT '15 [15]	JSSC '15 [85]	ISSCC '15 [82]	ISSCC '17 [92]	TCSII '11 [73]	JSSC '08 [27]
Calibration-free/ DEM-free	Yes	Yes	Yes	Yes	No	No	No	No	No
Technology	CMOS 65nm	CMOS 90nm	CMOS 65nm	CMOS 28nm	FDSOI 28nm	CMOS 28nm	BiCMOS 130nm	CMOS 65nm	CMOS 90nm
Resolution (bit)	8	6	6	8	9	8	10	8	8
Segmentation	Binary	Binary	Segmented	Segmented	Segmented	Segmented	Segmented	Segmented	Segmented
Supply (V)	1.2/2	1.2/1	1.0/2.5	1.1/1.5/2	1.0	1.0/1.5	1.2/-3.3 /-5.8	1.2/2.5	1.0/1.8
Overall f_{conv} (GS/s)	–	–	56	100	11	18	–	–	12
1-core f_{conv} (GS/s)	2.4	3.1	3.5	6.25	5.5	0.9	3.35	1.6	3
P_d (mW)	26.4	17.7	750	2500	110	84	1910	90	190
I_{FS} (mA)	5	4	12	7	8.5	16	–	20	31.9
SFDR(dBc)	47.8	37.2	30	27	52	38	54	57	35
@ f_{out} (GHz)	@1.13	@1.43	@26.9	@24.9	@4.6	@9	@20 [^]	@0.7	@1.5
INL (LSB)	±0.097	0.09	–	0.2	–	–	–	0/-0.2	0.31
DNL (LSB)	–0.05/0.15	0.06	–	0.04	–	–	–	0.04/-0.03	0.28
FoM (1/pJ)	10.9	5.42	1.0	–	8.68	6.10	3.06	2.28	2.02

[^] Multiple Nyquist Zone

Second, on the basis of a single-core DAC, our CS-DAC is relatively slow. This is largely due to the DPG whose speed is limited to 2.4GS/s due to the intended applications.

Third, as benchmarking amongst different architectures and/or process technologies is contentious, we adopt an established FoM that provides a composite measure of the DAC performance across three critical parameters, namely, power dissipation, SFDR, and bandwidth. This FoM [21], that accounts for linearity is given in Equation (4.5).

$$\text{FoM} = \frac{2^n BW_N}{P_d} \quad (4.5)$$

where BW_N is the bandwidth (Hz) where $\text{SFDR} \geq 6n$ dBc,

P_d is the DAC power dissipation (W), and

n is the DAC resolution (bit).

On the basis of this established FoM, our high-speed CS-DAC prototype IC features the highest FoM amongst all reported DACs – both for the calibration-free/DEM-free and for DACs requiring calibration or DEM.

4.6 Conclusions

An 8-bit 2.4GS/s pseudo-segmented CS-DAC design without calibrations/DEM featuring $\pm 0.097\text{LSB}$ INL, $-0.05/0.15\text{LSB}$ DNL, $>47.8\text{dBc}$ SFDR across the Nyquist bandwidth, and dissipating 26.4mW has been presented. These attributes are largely achieved by the proposed distributed biasing scheme, where the multiple inherent trade-offs in the CS-DAC are largely decoupled. When benchmarked against the state-of-the-art DACs, on the basis of an established FoM that encompasses linearity, the proposed CS-DAC features the highest FoM – both for calibration-free/DEM-free DACs and for DACs requiring calibration or DEM.

Appendix B

Analysis on the Relationship between Output Impedance, SFDR, and INL

B.1 The Relationship between Output Impedance and SFDR

In literature, the reported relationship between the output impedance and SFDR is generally based on two assumptions. First, the analog output is assumed to have continuous analog levels [30] although the analog output of practical DACs has discrete analog levels. This assumption is, hence, inappropriate for low- to mid-resolution DACs where the assumption error increases as there are fewer discrete analog levels.

Second, the SFDR of differential output DACs is assumed to be limited by the third order harmonic where the SFDR (indefinitely) increases as the output impedance increases. Conversely, the SFDR of single-ended output DACs is assumed to be limited by the second order harmonic. These assumptions however contradict with the computer simulations as the SFDR of an ideal CS-DAC is limited when the output impedance is set to infinity (i.e., no parasitic elements).

In this section, the relationship between the output impedance and SFDR is modeled based on the CS-DAC model depicted in Figure B.1. Each current-source is modeled as an ideal current-source in parallel with a parasitic element $|Z_{o,cs}|$, while the load resistance is R_L and the current-switches are assumed to be ideal. The DAC model is implemented in MATLAB to calculate the SFDR across different resolutions ($n=6, 7 \dots 16$) and output impedances, $Z_{o,cs}$ (100Ω to $200\text{G}\Omega$).

Figure B.1 CS-DAC model employed in the MATLAB's SFDR simulations

For each n and $Z_{o,cs}$, the DAC model is simulated for $>10^4$ different output signal frequencies evenly spread across the Nyquist bandwidth and subsequently the frequency spectrums are calculated with the Fast-Fourier Transform (FFT) algorithm. A high number of samples (2^{22}) are employed in the FFT to ensure that the largest spur is not masked by the quantization noise. Based on the calculated frequency spectrums,

the SFDR for each output frequency is obtained and subsequently compared to ascertain the worst-case SFDR across the Nyquist bandwidth.

Based on our MATLAB simulations, Figure B.2 depicts the relationship between the impedance ratio, r_o/R_L , and SFDR (in dBFS (decibel relative to full scale)) for differential output CS-DACs with $n = 6, 7 \dots 16$ where $R_L = 50\Omega$. It can be observed that the SFDR initially increases and then saturates as r_o/R_L increases and the inflexion points depending on the DAC resolution, n . As r_o/R_L decreases below the inflexion points, the SFDR initially decreases at around 30–40dB/decade and the SFDR slope decreases as r_o/R_L decreases.

Figure B.2 Relationship between the r_o/R_L and SFDR for differential output CS-DACs with $n = 6, 7 \dots 16$ based on MATLAB simulations, where $R_L = 50\Omega$

In high-speed DACs, a high SFDR is one of the critical requirements as it denotes good dynamic linearity. As DACs are typically designed for high SFDRs, we will limit the modeling of the said relationship for resolutions $n=6, 7 \dots 16$ bits as depicted in in Figure B.2 for $r_o \geq 0.5r_{o\min}$.

$$\begin{aligned} \text{SFDR} &= 40.2 \cdot \log\left(\frac{r_o}{R_L}\right) - 12.8n + 33.7 && ; 0.5r_{o\min} < r_o \leq r_{o\min}, \text{ and} \\ &= \text{SFDR}_{\text{sat}} = 7.69n + 4.21 && ; r_o > r_{o\min} \end{aligned} \quad (\text{B.1})$$

where $r_{o\min} = 10^{0.51n-0.73} R_L$ is the output impedance at the inflexion point, and

SFDR_{sat} is the saturation (or maximum) SFDR.

To verify the accuracy of our model, the SFDRs calculated using Equation (B.1) are compared against the simulated SFDRs. Figure B.3 depicts the errors of Equation (B.1) against our simulations in Figure B.2 – we are assuming here that the simulations are precise. These errors depicted in Figure B.3 are given as % errors, i.e., the numerical numbers (in dBFS) obtained from Equation (B.1) less that obtained by simulations, and divided by the latter. We remark that the errors of the calculated SFDRs (from Equation (B.1)) depicted in Figure B.3 are small and within $\pm 2.8\%$. This confirms the accuracy of our proposed model.

Figure B.3 Errors of Equation (B.1) against our simulations in Figure B.2

B.2 The Relationship between $r_{o\min}$, SFDR, and INL

In Section 3.2 and Appendix A, we derived the relationship between r_o and INL. By combining this derived expression Equation (3.2) and our developed model Equation (B.1), the relationship between $r_{o\min}$, INL, and SFDR can be obtained.

On the basis of these combined expressions, Figure B.4 depicts the calculated INL and SFDR_{sat} when the output impedance is equal to $r_{o\min}$. Because SFDR_{sat} is in dBFS, the $20\log(\text{INL})$ is employed for better comparison from Figure B.4, we remark the following.

The rate of increase in the SFDR – r_{omin}/R_L curve is significantly higher than the rate of decrease in the INL – r_{omin}/R_L curve. This implies that the required output impedance to obtain SFDR = SFDR_{sat} is more stringent than that for the typical INL requirement of <0.5LSB (i.e., –6dB). This therefore suggests that the generally adopted INL<0.5LSB in the CS-DACs design could be insufficient to obtain good dynamic linearity (e.g., SFDR). Put simply, it is critical to estimate the required output impedance from both the INL and SFDR requirements.

Figure B.4 Relationship between $r_{\min}$, SFDR_{sat} (Equation (B.1)), and INL (Equation (3.2)), for resolutions $n =$

6, 7...16

Chapter 5

Conclusions and Recommendations

5.1 Conclusions

The broad objective of this Ph.D. program pertained to the analysis and design of high-speed DACs, specifically CS-DACs, for high speed transmitters in next-generation digital communication systems. The conclusions of this thesis will first be delineated, followed by recommendations for research work.

Chapter 1, the introductory chapter, delineated the broad objectives and the motivations of this Ph.D. research program, and the specific objectives of the aforesaid broad objectives.

In Chapter 2, the literature review chapter, DACs have been comprehensively and critically reviewed, including the different reported DAC architectures, their basic modus operandi, and their merits and disadvantages. Subsequently, an in-depth review of the design of CS-DACs was provided. This in-depth review in part focused on the limitations of state-of-the-art designs due to the non-ideal parameters and their

inevitable trade-offs. The review also highlighted several imperative aspects of CS-DAC designs that remain incomplete or unresolved in literature.

In Chapter 3, a 4-bit 10GS/s single-core CS-DAC embodying a novel high-speed switch-driver and a novel in-situ hardware-efficient DPG have been proposed, designed, and monolithically realized. The proposed switch-driver was shown to mitigate the output glitches by simultaneously addressing three major glitch sources. The relationship between the output impedance of the current-sources and INL has been investigated and the corresponding analytical expressions were derived and subsequently adopted to optimize the current-sources. The proposed in-situ DPG circumvented the difficulties associated with the generation of 4×10 Gb/s data pattern required during hardware measurements and verification of our proposed CS-DAC. On the basis of hardware measurements, our proposed CS-DAC achieved good linearity (low INL and low DNL), and we attributed this to our proposed high-speed switch-drivers which alleviated the output glitches, and to our optimized current-sources and other critical building blocks. The proposed CS-DAC achieved the best FoM when benchmarked against state-of-the-art DACs.

In Chapter 4, a calibration-free/DEM-free 8-bit 2.4GS/s CS-DAC embodying a novel distributed biasing scheme has been proposed, designed, and monolithically realized. The proposed distributed biasing scheme permitted simultaneous optimizations of three major non-ideal parameters (finite output impedance, delay differences, and current mismatches) in CS-DACs by largely decoupling their undesirable and inevitable trade-offs. The cross-correlations among the current-sources as well as the relationship between the output impedance of the current-sources and SFDR have been

investigated and analyzed. On the basis of these analyses and our derived expressions in Chapter 3, the current-sources design was optimized to achieve high innate accuracy at high frequencies to facilitate the desired calibration-free/DEM-free operation. A simplified version of in-situ DPG proposed in Chapter 3 was implemented to generate 8×2.4 Gb/s data pattern required during hardware measurements and verification of our proposed CS-DAC. On the basis of hardware measurements, our proposed calibration-free/DEM-free CS-DAC achieved good linearity (very-low INL, low DNL, and high SFDR), and we attributed this to our proposed distributed biasing scheme, and to our optimized current-sources and other critical building blocks. The proposed CS-DAC also achieved the best FoM when benchmarked against the state-of-the-art DACs.

In conclusion, the work delineated in this thesis is significant towards the design of high-speed DACs for the next-generation high speed communications systems. Specifically, it provides profound insight to high-speed CS-DAC designers for the optimization of the current-sources by means of our derived analytical expressions and models, and the ensuing opportunities to largely decouple several trade-offs between several non-ideal parameters. Furthermore, it delineates how various design parameters may be optimized and/or traded-off to meet a given set of design specifications.

5.2 Recommendations: Future Research

On the basis of the literature review and the research work in this research program, we recommend the following future research work:

- (i) Investigation into the design of sub-TS/s ($>100\text{GS/s}$) DACs with low- to mid-resolution ($\sim 4 - 8$ bits).

As delineated in the literature review in Chapter 2, the conversion rate of high-speed CS-DACs is largely limited by the speed of the digital blocks (e.g., for DEM, calibration, time-interleaving, etc.) therein. While advanced processes (e.g., III-V, HBT, BiCMOS, etc.) with faster transistors may improve the speed of the digital blocks, it may still be insufficient for achieving sub-TS/s conversion rate as other non-ideal parameters, including the inherent parasitic components, clock and signal jitters, etc., may limit the achievable speed of CS-DACs. Furthermore, at sub-THz, the on-chip metal interconnects may behave as transmission lines and this further complicates the interconnections between transistors or building blocks in the realization of sub-TS/s DACs. In view of this, we recommend an investigation into the challenges associated with sub-TS/s CS-DACs to discover new design methodologies for the realization of sub-TS/s CS-DACs.

- (ii) Investigation into the design of sub-100GS/s ($10 - 99 \text{ GS/s}$) DACs with high dynamic linearity that is comparable to that of sub-GS/s DACs.

As delineated in literature review in Chapter 2, at this juncture, reported sub-100GS/s DACs typically have low dynamic linearity where the worst-case

SFDR of $>18\text{GS/s}$ DACs remain relatively low ($<40\text{dBc}$). One of significant shortcomings of CS-DACs is their inherent input code dependence output impedance. When the conversion rate is at sub- 100GS/s , the CS-DACs usually exhibit higher nonlinearities largely because it is increasingly difficult to address this inherent shortcoming. In view of this, we recommend an investigation into new design techniques to mitigate or possibly eliminate the dependency of the output impedance to the input code as well as to alleviate other non-ideal parameters in CS-DACs to improve the linearity of sub- 100GS/s CS-DACs.

- (iii) Investigation into the design of ultra high-speed ($>10\text{Gb/s/channel}$) in-situ DPGs as the test platform to facilitate the measurements and verification of ultra high-speed, DACs.

It was shown that in Chapter 3 that that the proposed in-situ DPG features $4\times 10\text{Gb/s}$ digital pattern generation. The achieved data rate is however insufficient for sub- 100GS/s or sub-TS/s CS-DACs. In view of this, we recommend an investigation into new design techniques to increase the data rate of in-situ DPGs toward sub-Tb/s/channel to facilitate the measurements and verification of sub- 100GS/s or sub-TS/s DACs.

Author's Publications

Journal Publications

- [1] Juanda, W. Shu, and J. S. Chang
"A 10-GS/s 4-Bit Single-Core Digital-to-Analog Converter for Cognitive Ultrawidebands"
IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, pp. 16-20, 2017

- [2] Juanda, W. Shu, and J. S. Chang
"A Calibration-Free/DEM-Free $\pm 0.097\text{LSB}$ IINL, $>47.8\text{dB}$ SFDR, 8-bit, 2.4GS/s DAC with a Distributed Biasing Scheme in 65-nm CMOS"
Submitted to the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017

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