Design and monolithic realization of high-speed high-resolution analog-to-digital converters

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**Design and Monolithic Realization
of High-speed High-resolution Analog-to-Digital
Converters**

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in partial fulfilment of the requirement for the degree of
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SUMMARY

This PhD program pertains to the design and monolithic realization of high-speed high-resolution Analog-to-Digital Converters (ADCs), particularly pipeline-based and Successive Approximation Register (SAR)-based architectures, for next-generation telecommunication systems. The primary objectives are to increase the speed and the resolution of these ADCs by means of innovative techniques/approaches, yet with minimal hardware and power overheads, and accommodating the ever-finer technology nodes. Interestingly, although the design art of pipeline and SAR ADCs are well established, several aspects of state-of-the-art designs and realizations remain inadequate. These inadequacies include the Multiplying Digital-to-Analog Converter (MDAC) in pipeline-based ADCs constraining the resolution, and the conversion algorithm of SAR-based ADCs limiting the speed.

For the pipeline-based ADC, we propose, design, and monolithically realize a novel time-interleaved ($\times 2$) 11bit 1GS/s SAR-assisted *MDAC-free* pipeline architecture. At the system level, we propose to employ a front-end sample-and-hold to mitigate the problematic timing mismatch between the two time-interleaved channel ADCs. We further propose to predetermine the MSB (Most Significant Bit) outside the channel ADCs to substantially simplify the requirement of the channel ADCs. At the block level, we propose an innovative *MDAC-free* pipeline architecture for the channel ADCs where the MDAC is absent—to the best of our knowledge, this is the first-ever reported MDAC-free pipeline ADC architecture. The significance of the MDAC-free feature is particularly valuable to the pipeline ADC design as the well-reported critical issues arising from the MDACs are largely circumvented. Particularly, this leads to higher speed and higher accuracy, yet with potentially reduced design complexity. Further, this

enables digital transmission between the pipeline stages, thereby substantially enhancing the accuracy and noise-immunity therein, and lending this architecture to ever-finer technology nodes due to its elimination of the analog residue amplification. The shortcoming, nevertheless, is the slightly increased hardware overheads. The SAR-assisted MDAC-free ADC prototype fabricated in 65nm bulk CMOS features SNDR ≥ 56 dB across 500MHz Nyquist bandwidth at 1GS/s sampling rate with 230mW power dissipation. When benchmarked against state-of-the-art ≥ 11 bits ≥ 1 GS/s pipeline ADCs, the proposed pipeline-based ADC features a highly competitive Figure-of-Merit.

For the SAR-based ADC realization, we propose a 2bit/step 10bit 400MS/s SAR ADC embodying a novel 2bit/step conversion scheme. By means of our proposed scheme, our proposed ADC offers three attractive features. First, only three capacitor arrays are required—to the best of our knowledge, the least number of capacitor arrays amongst reported CDAC-based 2bit/step SAR ADCs—leading to higher energy efficiency. Second, only two out of the said three capacitor arrays serve to sample the input signal, hence reducing the input loading. Third, the proposed ADC features an inherently symmetrical architecture with highly-matched interconnections, leading to enhanced system matching and higher accuracy. We further propose a high-speed high-accuracy dynamic comparator and a high-speed SA control logic to obtain high conversion rate. The SAR-based ADC prototype fabricated in 65nm bulk CMOS technology achieves SNDR > 52 dB and SFDR > 63.7 dB across 200MHz Nyquist bandwidth with 5.61mW power dissipation. When benchmarked against state-of-the-art CDAC-based 2bit/step SAR ADCs, the proposed SAR-based ADC features the smallest number of capacitor arrays and a highly competitive Figure-of-Merit.

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NOMENCLATURE

CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	<i>n</i> -type MOSFET
PMOS	<i>p</i> -type MOSFET
SNR	Signal to Noise Ratio
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
ENOB	Effective Number of Bits
DNL	Differential Nonlinearity
INL	Integral Nonlinearity

Chapter 1 INTRODUCTION

1.1 MOTIVATION

Driven by the increasing demand of high-speed applications (e.g., high-performance computing and core networking, multi-band radios, etc.), telecommunication systems are demanding ever-higher data rate. For instance, the data rate of Ethernet networks (IEEE 802.3) is moving from 10Gbit/s to 40Gbit/s or 100Gbit/s, and cellular network will adopt the impending 5G standard that can offer data rate up to 10Gbit/s. Congruous with this trend, sampling receivers in telecommunication systems are also evolving towards ever-higher data rate and higher accuracy, yet with the expectations of equivalent or reduced system complexity and lower cost. In particular, the conventional ubiquitous intermediate frequency (IF) sampling receiver [1] depicted in Figure 1.1(a), is increasingly replaced by its radio frequency (RF) direct sampling counterpart [2, 3] depicted in Figure 1.1(b).

Consider the merits and shortcomings of the IF sampling receiver (heterodyne receiver [1]) and the RF direct sampling counterpart. The IF sampling receiver, depicted in Figure 1.1(a), is widely adopted in communication systems where the receiver converts the received RF input signal to IF frequencies by means of appropriately adjusting the frequency of the local oscillator (LO). It is well established that the heterodyne receiver suffers from three constraints. First, there is a need to perform a down-conversion to accommodate the back-end IF analog-to-digital conversion. This analog down-conversion, being in the undesirable analog domain, renders the receiver vulnerable to environmental noise and interferences, thereby limiting the sensitivity/accuracy of the receiver [1-3]. Second, the Bandpass Filter (BPF), IF

amplifier and anti-aliasing filter designed in part to suppress the distortions from the down-conversion and to amplify the band-limited signal, undesirably increase the processing latency and the design complexity of the receiver. Third, as the signal processing of the IF sampling receiver involves a relatively long analog signal processing chain, the data rate is somewhat constrained.

Figure 1.1 Block diagrams of the (a) classical heterodyne receiver, and the (b) direct sampling receiver; LNA, BPF, and LO denote Low Noise Amplifier, Bandpass Filter, and Local Oscillator respectively

The RF direct sampling receiver, depicted in Figure 1.1(b), on the other hand, is advantageous over the heterodyne because it potentially mitigates some of the shortcomings of the classical IF sampling receiver. It features three primary advantages. First, the down-conversion in the analog domain in the IF sampling receiver is now

moved to the digital domain in the RF direct sampling receiver, i.e., the analog-to-digital converter (ADC) is now moved to the front-end of the receiver. This down-conversion modality not only improves the tolerance to noise and interferences, but also substantially reduces the aforesaid analog signal processing chain. For the latter, this is by means of the elimination of the aforesaid mixer, LO, BPF, IF amplifier and Anti-aliasing filter, thereby leading to faster data rate and reduced hardware complexity. Second, it can be observed from Figure 1.1(b) that the RF direct sampling receiver enables a higher level of digital integration, hence potentially advantageous in terms of power efficiency, hardware and ensuing IC area efficiency, and low cost. Third, in the perspective of technology scaling, the high level of digital integration inevitably enhances the data rate and reduces the power dissipation.

As depicted in Figure 1.1(b), the RF direct sampling receiver requires the front-end wideband ADC to feature high conversion rate and high resolution—this largely dictates the overall performance of the RF direct sampling receiver [1]. Specifically, the front-end wideband ADC in many telecommunication systems is required to feature $\geq$ GS/s conversion rate to directly convert the received RF input signal to its digital equivalent. Further, the dynamic range/resolution of the said ADC needs to be $\geq$ 8 Effective Number of Bits (ENOB) to meet the sensitivity/accuracy requirement of RF direct sampling receivers. In view of these attributes, it is not unexpected that the front-end wideband ADC is one of the dominant power dissipation blocks in the direct sampling receiver. Consequently, it is required to feature high energy-efficiency.

In view of these stringent requirements, it is well recognized [2-4] that the design and realization of such ADCs are challenging, particularly the high power-efficiency attribute at GS/s and multi-GS/s conversion rate. To appreciate these challenges, Figure 1.2 [5] depicts the energy-efficiency figure-of-merit (FoM) versus the Nyquist sampling

frequency (f_{snyq}) plot of ADCs published in the International Solid-State Circuits Conference (ISSCC) and the Symposium on Very Large Scale Integration (VLSI) between 1997 and 2017. In this plot, it is desirable that the FoM along the ordinate be as low as possible.

Figure 1.2 Energy efficiency (FoM) versus f_{snyq} (Nyquist sampling frequency) of ADCs published in ISSCC and VLSI from 1997 to 2017

From Figure 1.2, we observe that the FoM degrades dramatically when conversion rate exceeds approximately 300MS/s. In particular, when the conversion rate exceeds GS/s, the degradation of the FoM is approximately linear at 10 times per decade. There are several reasons for this. In the perspective of process technologies, when the circuit speed approaches the speed limit of the process technology, the power-speed trade-off becomes nonlinear, i.e., a disproportional higher power is required for speed increment [6, 7]. Consequently, amplifiers and comparators suffer from diminishing returns in their

speed as their power consumption is raised. For this reason, the FoM of the ADC based on fine technology nodes (e.g., 28nm, 16nm, etc.) likewise degrades quickly when the conversion rate increases to multi-GS/s [8-10]. In the perspective of circuit and architecture, several critical issues undesirably limit the design and realization of state-of-the-art high-speed and high-resolution ADCs. Some of these issues will now be reviewed.

High-speed (GS/s or multi-GS/s) high-resolution (≥ 10 bit) ADCs are often realized on the basis of the time-interleaved architecture [11-13]—a well-known architecture that can increase the ADC conversion rate by M times by means of M identical sub-ADCs. Nevertheless, this architecture suffers from several challenging issues. One critical issue is that the sub-ADCs therein, inevitably being not exactly identical due to systematic mismatch and process variations, introduce timing, gain and offset mismatches that undesirably distort the ADC output [7, 14]. Although various calibrations [3, 7, 11, 15-17] have been reported to mitigate the said mismatches, these calibrations, particularly for timing mismatch that is non-linear and input-dependent, often suffer from substantial hardware overheads (e.g., additional sub-ADCs) and complex off-chip computations that limit their applicability. Further, the strict matching requirement for the distribution of the critical signals (e.g., clock and input signals) to multiple sub-ADCs often entails bandwidth trimming signal paths (e.g., by means of augmented variable delay lines), leading to increased design complexity and hardware overhead.

To mitigate the aforesaid time-interleaved issues, a well-known practice is to reduce the number of the interleaved sub-ADCs by replacing these sub-ADCs with sub-ADCs with higher conversion rate [7, 14, 18]. This reduced interleaving not only reduces the interleaving distortions (caused by the aforesaid mismatches) in the ADC output spectrum [7], but also substantially reduces the design complexity and hardware

overheads [7, 14]. Nevertheless, the ensuing challenge shifts to the design and realization of higher speed sub-ADCs without compromising the conversion accuracy, with no or minimal power and hardware overheads.

Very high-speed state-of-the-art sub-ADCs unfortunately suffer from several critical design and architecture issues and limitations. We will now in turn briefly delineate some of these issues for the two most prevalent ADC realizations—the pipeline ADCs [19-21] and the successive approximation register (SAR) ADCs [3, 11, 22] respectively depicted in Figure 1.3(a) and (b); a comprehensive review will be in Chapter 2, and on this basis, two novel ADCs are proposed and delineated in Chapters 3 and 4.

Figure 1.3 Architectures of the (a) pipeline-based realization, and the (b) SAR-based realization. MDAC: multiplying Digital-to-Analog Converter, EOC: End of Conversion, S/H: Sample-and-Hold.

The pipeline ADC realization typically comprises multiple pipeline stages where each stage resolves a few bits. These stages operate concurrently with analog residue signals transmitting in between. The conversion rate is high because of these concurrent operations. However, the resolution is somewhat constrained, largely because the generation of the analog residue signals typically suffers from several limitations, particularly relating to the MDAC. In the pipeline ADC, the MDAC is the most critical building block, and the three primary issues thereto will now be discussed.

First, it is particularly challenging to realize the residue amplifier (see Figure 1.3(a), a critical building block of the MDAC) [2, 6] that achieves sufficiently high open-loop gain with the required signal swing across the high frequency range to ensure that the gain error and nonlinearity of the MDAC are sufficiently small, e.g. $< \frac{1}{2}\text{LSB}$ (least significant bit). In the perspective of CMOS fabrication technology scaling where

technology scaling enhances the ADC bandwidth, the finer feature transistors, unfortunately and undesirably, exacerbates the difficulty of the design of the residue amplifier. This is because of lower intrinsic gain of these transistors and because the supply voltage is lower.

Second, the MDAC needs sufficient time to settle to the required accuracy (speed-accuracy tradeoff). In view of the time-consuming operation [23] and timing overheads [7] of conventional pipeline stages, the settling time available for the MDAC is acutely limited.

Third, the MDAC often suffers from capacitor mismatches that undesirably distort the generation of the residue signal. This results in nonlinearities, e.g., missing code or wide code in the ADC transfer function characteristics.

Several reported foreground and background calibration techniques [6, 11, 24-26] have attempted to mitigate the aforesaid issues in the pipeline-based ADC realization. These calibration techniques, while generally useful, unfortunately suffer from various limitations. Specifically, foreground calibrations [6, 24, 27], on one hand, often require pilot signals and may interrupt the normal operation of the ADC. Background calibrations [28-32], on the other hand, often employ complex back-end digital computation that typically result in undesirable long convergence time, or need additional reference ADCs that increase the hardware and power overheads. Further, both calibration modalities undesirably significantly increase the hardware complexity [33-37]. In short, the MDAC is the primary bottleneck in the design of pipeline ADCs, and the prior-art attempts to mitigate this bottleneck inevitably result in more complex hardware, and from a hardware perspective, increasingly inefficient designs.

For the SAR-based realization, the ADC typically comprises only digital elements and does not involve challenging analog elements, e.g., the aforesaid residue amplifier in pipeline-based ADCs. In the conversion process, the SAR-based ADC performs a binary search through all possible quantization levels before converging to the final digital output. This search typically requires N iterations of binary search to achieve N -bit resolution. Consequently, although the accuracy issues in the SAR ADC are less severe than its pipeline-based counterpart, its conversion rate is, unfortunately, limited.

There are reported attempts [15, 38, 39] to mitigate the speed limitation by means of the 2bit or multi-bit/step (M -bit/step) conversion scheme where the conversion rate is improved by approximately 2 or multiple times. However, this scheme requires additional DACs (mostly capacitive DACs) and comparators, thereby often resulting in excessive hardware, i.e., from the hardware perspective, increasingly inefficient designs. In addition, as most of the augmented capacitive DACs sample the input signal at the same instance, the input capacitance of the 2bit or multi-bit/step SAR ADCs are often undesirably increased, i.e., an increased capacitive loading. This consequently imposes the requirement of additional power-hungry buffers to buffer the input signal into the ADC, thereby leading to not only hardware inefficient designs but also excessively power-dissipative designs.

In summary, at this juncture, both the pipeline-based and the SAR-based ADCs have merits and shortcomings, and there is no general consensus within the ADC design community on which specific architecture is more advantageous for high-speed high-resolution applications. Further, both architectures suffer from formidable design challenges of which several remain largely unresolved such as that delineated earlier. Yet further, most reported attempts to circumvent these limitations and issues often result in overly heavy hardware and power overheads—their efficacy is often somewhat

contentious. Some of these limitations and issues, e.g., the requirement of high-gain residue amplifier in the pipeline-based realization, are further exacerbated by CMOS technology scaling due to the reduced gain, etc.

Put simply, there is a real need for innovative techniques/approaches to mitigate the limitations and issues of the pipeline and SAR ADCs, to obtain higher-speed, higher-resolution, and yet lower-power, ADCs for next-generation high-speed applications, e.g., RF direct sampling receivers.

1.2 OBJECTIVES

The broad objective of this PhD program is to design and realize pipeline-based and SAR-based high-speed high-resolution ADCs embodying novel architectures and/or techniques to mitigate the aforesaid issues delineated in Section 1.1.

The specific objectives are:

- (i) A comprehensive literature review of various Nyquist-rate high-speed high-resolution ADC architectures, including a critical appraisal of their merits and limitations/issues;
- (ii) An investigation into the pipeline and SAR architectures—the most prevalent architectures for the realization of state-of-the-art high-speed high-resolution ADCs—with emphasis on their issues and the prior-art attempts to mitigate these issues;
- (iii) On the basis of (ii), the proposal of novel architecture and/or techniques to mitigate the issues of the pipeline-based realization for high-speed high-resolution ADCs, yet with reduced design complexity and minimal power overheads;

- (iv) On the basis of (iii), to design and monolithically realize a time-interleaved pipeline-based high-speed high-resolution ADC prototype, whose specifications are tabulated in Table 1.1;

Table 1.1 Specifications of the proposed pipeline-based ADC prototype

Parameter	Value
Process	GF 65nm
Power Supply	1.2V
Sampling Rate	1GS/s
Resolution	11bits
ENOB	≥ 8 bits
Power Dissipation	≤ 250 mW

- (v) Following (iii) and (iv), to test and measure the said ADC prototype to ascertain the merits/shortcomings of the proposed techniques/architecture to achieve the overall objective;
- (vi) On the basis of (ii), the proposal of novel techniques/approaches (i.e., 2bit/step conversion schemes) to mitigate the speed limitation of the SAR-based realization for high-speed high-resolution ADCs;
- (vii) On the basis of (vi), to design and monolithically realize an efficient 2bit/step SAR-based high-speed high-resolution non-time-interleaved ADC prototype, whose specifications are tabulated in Table 1.2;

Table 1.2 Specifications of the proposed SAR-based ADC prototype

Parameter	Value
Process	GF 65nm
Power Supply	1.1V
Sampling Rate	400MS/s
Resolution	10bits
ENOB	≥ 8 bits
Power Dissipation	≤ 10 mW

- (viii) Following (vi) and (vii), to test and measure the said ADC prototype to ascertain the merits/shortcomings of the proposed techniques/approaches to achieve the overall objective.

1.3 CONTRIBUTIONS

The contributions made in this PhD research program are congruous to the specific objectives outlined above. Specifically, they are:

- (i) A comprehensive literature review of Nyquist-rate ADCs, including a critical appraisal of the imperative performance attributes pertaining to the design and realization of high-speed high-resolution ADCs.
- (ii) On the basis of (i), an investigation into pipeline-based and SAR-based realizations of high-speed high-resolution ADCs. Specifically, for pipeline-based ADCs, we investigated the issues pertaining to the MDAC—the most critical building block in pipeline ADCs—and critically reviewed prior-art reported attempts to mitigate these issues. For SAR-based ADCs, we investigated their speed limitation, and the prior-art (reported) 2bit/step designs, including detailed analysis of their limitations and issues.

On the basis of (ii), two novel ADCs—a pipeline-based and a novel SAR-based high-speed high-resolution ADCs—are proposed and implemented. The pertinent contributions are as follows.

For pipeline-based realization, our contributions include:

- (iii) Our proposal of a novel 11bit 1GS/s MDAC-free pipeline-based architecture. The proposed architecture eliminates the need of the MDAC—i.e., an MDAC-free

pipeline ADC—to the best of our knowledge, the only MDAC-free pipeline ADC to date. Being MDAC-free, the critical issues arising from the MDAC of conventional pipeline-based high-speed high-resolution ADCs are mitigated. Consequently, the accuracy (e.g., ENOB) is enhanced and the design complexity is simplified; see Chapter 3.2 later. Nevertheless, there are compromises (e.g., slightly increased hardware overheads), albeit the merits arising from MDAC-free outweigh these compromises.

The detailed contributions include the following:

- (a) The design and realization of novel MDAC-free pipeline stages that not only reduce the design difficulty but also simplify the stage operation, thereby ultimately leading to higher speed,
 - (b) The design and realization of a high-speed high-linearity S/H where the THD remains below -75dB for input frequency $\leq 500\text{MHz}$, and the voltage gain is $\geq -2.8\text{m dB}$ for input frequency up to 3.2GHz , and
 - (c) The design and realization of a proposed novel high-speed high-accuracy comparator that features the capability of differentiating input differences $\leq \frac{1}{4}\text{LSB}$ at speeds up to 5GHz .
- (iv) The measurement of the MDAC-free pipeline ADC IC prototype realized from the GF CMOS 65nm process. The ADC prototype is benchmarked against state-of-the-art pipeline ADCs with resolution $\geq 11\text{bits}$ and sampling rate $\geq 1\text{GS/s}$ by means of a tabulation (see Table 3.2 in Chapter 3.7). The key features of the prototype ADC include SNDR $\geq 55.9\text{dB}$ across 500MHz Nyquist bandwidth at 1GS/s sampling rate with 230mW power dissipation from a dual power supply of $1.2\text{V}/2\text{V}$. Of particular interest, amongst the benchmarked ADCs, the proposed

ADC features the lowest power dissipation. Further, the proposed ADC features a highly competitive figure-of-merit (FoM), i.e., 449.2fJ/step.

For SAR-based realization, our contributions include

- (v) Our proposal of a novel 10bit 400MS/s 2bit/step SAR-based ADC architecture. By means of the proposed 2bit/step conversion scheme, the architecture mitigates the speed limitation of the conventional SAR ADC by improving the conversion rate by 2 times. Compared to the conventional 2bit/step SAR ADCs, the proposed architecture features structure simplicity with reduced input loading, and reduced hardware complexity with minimal power overhead. Further, the accuracy (e.g., ENOB) is enhanced; see Chapter 4.2 later.

The detailed contributions include the following:

- (a) The design and realization of compact Capacitive Digital-to-Analog Converters (CDACs) that feature high matching accuracy (i.e., 99.82%).
 - (b) The design and realization of a proposed novel high-speed high-accuracy dynamic comparator that largely eliminates the kickback noise and the offset.
 - (c) The design and realization of the high-speed SAR control logic that enhances the ADC conversion rate.
- (vi) The measurement of the proposed 2bit/step SAR ADC IC prototype realized in the GF CMOS 65nm process. The ADC prototype is benchmarked against state-of-the-art SAR ADCs (largely 2bit/step SAR ADCs) by means of a tabulation (see Table 4.3 later). The key features of the prototype ADC include SNDR ≥ 51.9 dB across the 200MHz Nyquist bandwidth at 400MS/s with 5.61mW power

dissipation from a 1.1V power supply. Of particular interest, amongst the benchmarked ADCs, our ADC features the highest SNDR. In terms of the FoM, which is calculated on the basis of $Power/(f_s * 2^{ENOB})$, the proposed ADC achieves a highly competitive FoM, i.e., 43fJ/step.

1.4 THESIS ORGANIZATION

This thesis is organized as follows.

Chapter 1 presented the introduction of this project, including the motivation, objectives and contributions.

Chapter 2 is the literature chapter. The review includes the review of the high-speed high-resolution Nyquist-rate ADCs, including the prevalent pipeline-based and SAR-based ADC realizations. In these reviews, the emphasis are their critical performance attributes and the critical issues, and a critical review of state-of-the-art mitigations.

Chapter 3 presents the design and realization of our proposed MDAC-free 11bit 1GS/s Pipeline ADC. Being MDAC-free, the proposed ADC largely mitigates the critical issues arising from the MDAC in conventional high-speed high-resolution pipeline ADCs (embodying MDACs). In this chapter, the system architecture is first introduced, followed by the explanation of proposed conversion algorithm, the critical building blocks of the ADC, and finally, the measurements of the ADC prototype, including its static performance and dynamic performance parameters.

Chapter 4 presents the design and realization of the proposed 2bit/step 10bit 400MS/s SAR ADC. The proposed 2bit/step ADC mitigates the critical speed limitation

of SAR ADCs. In this chapter, the system architecture is first introduced, followed by the explanation of our proposed 2bit/step conversion scheme, the circuit implementation, and finally, the measurements of the ADC prototype, including the static performance and dynamic performance parameters.

Chapter 5 draws the conclusions of this thesis and suggests recommendations for future work.

Chapter 2 LITERATURE REVIEW

This chapter critically reviews high-speed and high-resolution Nyquist-rate ADCs, including the ADC terminologies and the prevalent high-speed and high-resolution ADC architectures. This chapter serves as a preamble to the contributions described in the following chapters.

2.1 ADC OVERVIEW

An ADC, as its name implies, takes a continuous-time and continuous-amplitude analog input and converts it to an equivalent discrete-time and discrete-amplitude digital signal. Figure 2.1 depicts the block diagram of a typical Nyquist-rate ADC, which comprises a Sample-and-Hold (S/H), a quantizer, and a reference generator (Ref Generator). The S/H serves to sample and hold the analog input for time discretization. The quantizer outputs the pertinent digital outputs (D_{out}) by comparing the sampled input with analog reference voltages (V_{ref}) generated by the Ref Generator.

Figure 2.1 Block diagram of a typical Nyquist-rate ADC

The time and amplitude discretization are essentially defined by two primary attributes of the ADC, namely, the input bandwidth and the input dynamic range. The former refers to the frequency of a full-scale input signal where the resolved digital output drops by 3dB (3dB-amplitude attenuation). In the case of Nyquist-rate ADCs, the input bandwidth is typically required to be $<1/2$ the sampling rate to avoid aliasing in signal reconstruction (see Section 2.1.1 later). The input dynamic range typically refers to the amplitude range of the input signal that the ADC can resolve. This attribute is often determined by various factors such as the quantization error and the aperture jitter. We will now review the critical terminologies of Nyquist-rate ADCs.

2.1.1 Sampling Rate

The sampling rate (f_s) of the ADC is the rate at which a continuous input signal is sampled into a discrete signal. It is an imperative factor that ascertains the achievable input bandwidth for Nyquist-rate ADCs. The following analysis explains the relationship between f_s and the input bandwidth.

With a given input signal of $x(t)$, the sampling process can be mathematically represented as the product between $x(t)$ and a series of impulse functions $\delta(t)$. On this basis, the discrete signal, $x_\delta(t)$, after sampling can be expressed as

$$\begin{aligned} x_\delta(t) &= x(t) \times \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \\ &= \sum_{n=-\infty}^{\infty} x[nT_s] \times \delta(t - nT_s) \end{aligned} \quad (1)$$

where $T_s = 1/f_s$, and denotes the sampling interval (period).

As a multiplication in the time domain is equivalent to a convolution in the frequency domain, the discrete signal in the frequency domain can be obtained as

$$\begin{aligned}
 X_{\delta}(j\omega) &= X(j\omega) * \delta_{\omega_s}(j\omega) \\
 &= \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j(\omega - \tau)) \times \frac{2\pi}{T_s} \sum_{k=-\infty}^{\infty} \delta(j(\tau - k\omega_s)) d\tau \\
 &= \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(j(\omega - k\omega_s))
 \end{aligned} \tag{2}$$

where ω_s is the sampling frequency, i.e., $\omega_s = 2\pi f_s$.

On the basis of eqn. (2), $X_{\delta}(j\omega)$ is essentially a sum of input replicas that are shifted by $k\omega_s$.

Figure 2.2 depicts $X(j\omega)$ and $X_{\delta}(j\omega)$. It can be observed that the frequency (ω_{in}) of the input signal needs to be $< \frac{1}{2}\omega_s$ to avoid interference from the adjacent input replicas in the spectrum. This requirement is known as the Shannon-Nyquist Sampling Theorem. Conversely, when $\omega_{in} \geq \frac{1}{2}\omega_s$, the input signal will be contaminated by its adjacent replicas—the well-known aliasing phenomenon. It is imperative to avoid aliasing in Nyquist-rate ADCs because the original input signal otherwise cannot be reconstructed back.

Figure 2.2 Spectrums of $X(j\omega)$ and $X_{\delta}(j\omega)$

To appreciate the well-known aliasing, consider the signal in the time domain in Figure 2.3. The input signal, $V_{sig}(t)$, is a sinusoidal signal with frequency $f_{in} = 1000\text{MHz}$ and is sampled at $f_s = 1101\text{MS/s}$; $f_{in} > \frac{1}{2}f_s$. It can be observed that a signal of much lower frequency than the original input signal is sampled. This is essentially due to the insufficient number (i.e., ≤ 2) of samples obtained in one input period.

Figure 2.3 Signal with aliasing (in the time domain)

This exemplar aliasing can further be mathematically verified by the following sampling function.

$$\begin{aligned}
 V_{sig}[n] &= \sin\left(2\pi \times n \times \frac{f_{in}}{f_s}\right) \\
 &= \sin\left(2\pi \times n \times \frac{1101}{1000}\right) \\
 &= \sin\left(2\pi \times n \times \frac{101}{1000}\right).
 \end{aligned} \tag{3}$$

From eqn. (3), it can be seen that the sampled signal will be reconstructed to a signal whose frequency is 101MS/s—an aliasing error—instead of the original 1101MS/s. To avoid aliasing, the input bandwidth of the Nyquist-rate ADCs is limited

to $\leq 1/2f_s$. In practice, an anti-aliasing low-pass filter is often employed and placed in front of the Nyquist-rate ADCs to heavily attenuate the input components whose frequencies are $\geq 1/2f_s$.

2.1.2 Quantization Error

The quantization error stems from the voltage difference between the analog input and the quantized digital output. It is a truncation error introduced by the amplitude discretization during conversion. In principle, the maximum quantization error of an ideal ADC is $\pm 1/2\text{LSB}$. The quantization error is often approximated to be equally distributed within the $\pm 1/2\text{LSB}$ boundary, and the probability of the quantization error is the same at any point of the input signal.

Figure 2.4 depicts the well-known model for the quantization error of an ideal ADC. Specifically, the quantization error, $e(t)$, is represented by a periodic Sawtooth waveform with a peak-to-peak value of $q=1\text{LSB}$, a period of $-q/2$ to $q/2$, and a slope of s . Mathematically, it is expressed as

$$e(t) = st, -q/2s < t < q/2s. \quad (4)$$

Figure 2.4 Model for the quantization error

The mean-square value of $e(t)$ is

$$\begin{aligned}\overline{e^2(t)} &= \frac{s}{q} \int_{-q/2s}^{q/2s} (st)^2 dt \\ &= \frac{q^2}{12}\end{aligned}\tag{5}$$

$\overline{e^2(t)}$ typically follows the Gaussian distribution and spreads across the Nyquist bandwidth, i.e., from dc to $f_s/2$. Although the quantization also causes harmonics outside the Nyquist bandwidth, these harmonics fold back to the Nyquist bandwidth and sum up to yield the mean-square value of $\frac{q^2}{12}$. In view of this, $\overline{e^2(t)}$ is often interpreted as white noise with a bandwidth of $f_s/2$.

$\overline{e^2(t)}$ is the fundamental noise caused by the finite resolution of the ADC, and literally imposes an upper boundary for the ADC dynamic range. In the case of an N -bit ADC, the resulted upper boundary can be obtained in terms of the Signal-to-Noise Ratio (SNR):

$$\begin{aligned}
 SNR &= 10 \log \frac{P_{input}}{\overline{e^2(t)}} \\
 &= 20 \log \frac{q2^N / 2\sqrt{2}}{q / \sqrt{12}} \\
 &= 20 \log 2^N + 20 \log \sqrt{\frac{3}{2}} \\
 &= (6.02N + 1.76)
 \end{aligned} \tag{6}$$

Eqn. (6) expresses the relation between the dynamic range (i.e., SNR) and the resolution of an ideal ADC where the quantization error is the only error source. In practice, however, as the dynamic range of the ADC often deteriorates because of additional error sources (e.g., aperture jitter, thermal noise, process variations, circuit nonlinearities and distortions), the practical resolution is often lower than the ideal case. In view of this, SNDR comprising all the noise and distortions is typically employed instead of SNR in eqn. (6). The ensuing resolution is defined as *ENOB* (Effective Number of Bits). In other words, in practice, eqn. (7) below is often employed to qualify the ADC performance.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{7}$$

2.1.3 Aperture Time and Jitter

Aperture time is a time-domain quality of the sampling process, and is increasingly important for high-speed and high-resolution ADCs. It refers to the time

interval taken by the S/H (Figure 2.5) in the ADC to switch from ‘sample’ phase to ‘hold’ phase. It is essentially the time the sampling switch of the S/H needs to disconnect the sampling capacitor from the input signal, or the required time for the sampling switch to change from low impedance to high impedance.

Figure 2.5 depicts the classical block diagram of an S/H, and the pertinent waveforms wherein t_a denotes the aperture time. Ideally, the sampling switch of the S/H opens instantly (i.e., $t_a = 0$). In practice, however, $t_a \neq 0$, and the voltage ($V_{S/H}$) held on the sampling capacitor (C_S) is determined by the slew rate of the input signal and t_a . Specifically, $V_{S/H}$ is the averaged value of the input signal over t_a , and to a first order, can be interpreted as a delayed version of the input signal; delayed by t_e in Figure 2.5. It is worthwhile to note that t_e is largely independent of the slopes of the input signals as depicted in Figure 2.5. Typically, $t_e \approx t_a/2$, and is referred as effective aperture delay time.

Figure 2.5 Block diagram of the S/H and the associated waveform

Ideally, t_e is a constant, and delays the sampling process but does not necessarily degrade the ADC performance. However, in practice, t_e is inevitably contaminated by the phase jitter of the sampling clock from clock generators and in the case of the time-interleaved ADC, the systematic mismatches of the ADC. In the latter, t_e exhibits variations because of the timing mismatch between the sub-ADCs [17, 40-42]. The said variation of t_e is known as aperture jitter and often causes sampling errors to $V_{S/H}$, particularly for high frequency input signals.

The impact of the aperture jitter on the ADC performance will now be reviewed. Figure 2.6 depicts the error model for the aperture jitter. Assume that the input signal is a sinusoidal signal,

$$V_{in}(t) = A \sin(2\pi f_{in} t) \quad (8)$$

Figure 2.6 Error model for the aperture jitter

The slope, or rate of change of the input signal is then obtained as

$$\frac{dv_{in}(t)}{dt} = 2\pi f_{in} A \cos(2\pi f_{in} t) \quad (9)$$

The rms value of the slope is

$$\left. \frac{dv_{in}(t)}{dt} \right|_{rms} = \frac{2\pi f_{in} A}{\sqrt{2}} \quad (10)$$

Now let the rms value of the aperture jitter = Δt_{rms} , and the resulted rms error = $\Delta V_{S/H,rms}$. Substituting them into eqn. (10), $\Delta V_{S/H,rms}$ is obtained as

$$\Delta V_{S/H,rms} = \frac{2\pi f_{in} A}{\sqrt{2}} \Delta t_{rms} \quad (11)$$

The SNR of the ADC limited by the aperture jitter is then [43]

$$\begin{aligned} SNR &= 20 \log \frac{A/\sqrt{2}}{\Delta V_{S/H,rms}} \\ &= 20 \log \frac{1}{2\pi f_{in} \Delta t_{rms}} \end{aligned} \quad (12)$$

From (12), it can be seen that the SNR of an ADC is substantially degraded by the aperture jitter, particularly for high input frequencies. Figure 2.7 depicts the maximum SNR and ENOB that an ADC can achieve versus the input frequency for different aperture jitters. It can be observed that, the higher the input frequency, the more severe limitation imposed by the aperture jitter. In the case of GS/s or multi-GS/s ADCs, the aperture jitter is arguably the primary factor that literally limits the ADC performance. In view of the substantially increased difficulty to minimize $\Delta t_{rms} < 50\text{fs}$ [9, 44], it is not unexpected that State-of-the-Art high-speed ADCs that target GHz or multi-GHz input bandwidth [9, 11, 22] are often designed with resolution ≤ 14 bits.

Figure 2.7 Maximum SNR and ENOB versus the input frequency

2.2 OVERVIEW OF ADC ARCHITECTURES

On the basis of the way comparisons between the input signal and the reference voltages in the ADC, the analog-to-digital conversion is often categorized into either parallel conversion or series conversion. In the former, all the reference voltages are typically compared with the input signal at the same time instance. Conversely, in the latter, these comparisons take place at a series of different time instances. The prevalent Nyquist-rate ADC architectures, namely the flash, the pipeline, and the SAR architectures, feature either parallel conversion or series conversion. They will now be delineated in turn. As each architecture has its own unique attributes, and our review will emphasize their specific design and their realization for high-speed high-resolution ADCs. Our review will also delineate state-of-the-art attempts to mitigate these design issues.

2.3 FLASH ADC

Figure 2.8 depicts the block diagram of a typical flash ADC, also known as the parallel ADC. The resistor string serves to provide the reference voltages for the conversion, i.e., 2^N-1 reference voltages for N -bit resolution. The comparators serve to compare the sampled input (provided by the S/H) against the pertinent reference voltages, and generate a (2^N-1) -bit thermometer code to the Decoder. The Decoder decodes the (2^N-1) -bit thermometer code to an N -bit digital output.

Figure 2.8 Block diagram of a typical Flash ADC

Amongst the various reported ADC architectures, the flash ADC arguably achieves the highest conversion rate. This is largely because all the comparisons between the sampled input signal and the reference voltages are realized in parallel, and

the digital output is hence available in one clock cycle. State-of-the-art flash ADCs often achieve conversion rate up to a few GS/s, particularly those realized in deep submicron fabrication processes where the cutoff frequency of the transistors is very high (e.g. ~250GHz).

Despite the merit of high speed arising from the parallel conversion, the flash ADC suffers from several limitations and issues that constrain its performance. The most critical limitation is that it needs unacceptably excessive hardware to achieve high resolution. Specifically, for an N -bit flash ADC, 2^N-1 comparators and 2^N resistors are required, and with every one bit increment of the resolution, the hardware doubles. In the case of an 8-bit flash ADC, 255 comparators and 256 resistors are needed.

The excessive hardware not only results in unacceptable high power dissipation and severe silicon area penalty, hence not only in high cost, but also induces various issues that undesirably constrain the ADC's speed and accuracy. For example, the large number of comparators imposes an undesirably large load capacitance to the S/H, and requires a very long metal wire to connect to the S/H, thereby resulting in an excessive wire parasitic resistance. The collective large capacitance and resistance constitutes an RC filter, and constrains the bandwidth of the S/H, hence acutely limiting the sampling rate of the ADC. Further, the large number of resistors results in a large output resistance to the reference generation, particularly those in the middle of the resistor string. In the case where a sudden disruption to these reference nodes (e.g., noise and distortion coupling, or the sudden change of the comparators' input capacitance when a new sampled input is being updated), the settling time required for these references to settle back to offset the disrupt is large. This ultimately leads to a speed severe limitation.

In addition to the said hardware limitations, the flash ADC also suffers from severe nonlinearity caused by the resistor mismatches and comparator offsets. For example, in the case of 2% resistor mismatches, the resulting worst-case integral nonlinearity (INL) limitation is the low resolution ≤ 5 bits. In another example where the comparator offset is approximately 10~20 mV, which is possible for comparators realized in deep submicron CMOS process without any calibration, the ensuing resolution is also low, ≤ 5 or 6 bits. Put simply, although the flash ADC can achieve multi-GS/s conversion rate, its resolution is typically limited to ~ 6 bits due to the excessively high hardware overheads, i.e., a doubling of the hardware for an additional resolution bit.

It is hence not unexpected that to achieve both high conversion rate and high resolution (e.g. ≥ 10 bit), ADCs realized on the basis of the series conversion are often employed. The most prevalent ADC architectures based on series conversion are the Pipeline and the SAR ADCs, and we will critically review them in turn in the ensuing two sections.

2.4 PIPELINE ADC

The pipeline architecture is prevalent for high-speed high-resolution ADCs because it offers cogent trade-off between conversion rate and resolution [2]. This advantage is largely attributed to its well-known conversion algorithm—concurrent operations of the pipeline stages.

Figure 2.9 depicts the block diagram of the conventional pipeline ADC that embodies a multiplicity of pipeline stages in series [23, 45, 46]. These pipeline stages have similar architecture and operations, save the last stage that is typically a low-

resolution Flash ADC. These pipeline stages operate concurrently with each resolving a few digital bits. Consequently, the combination of the resolved bits from all the pipeline stages yield the final output, and the operation speed of the pipeline stages largely ascertains the overall conversion rate.

Figure 2.9 Block diagram of the conventional pipeline ADC

The operations in the pipeline stages (except the last stage which is a flash ADC) is well established [45-48] and involves three signal processing steps. First, the residue signal from the preceding pipeline stage (save stage 1 that takes the sampled input, V_s) is quantized to the pertinent digital output at the sub-ADC therein. Second, the quantized digital output is converted back to an analog signal by the DAC, and the analog signal is subsequently subtracted from the said residue signal. Third, the resultant signal from the said subtraction is amplified to constitute the updated residue signal, and this amplification serves to keep the references of all pipeline stages unaltered.

Consequent to the amplification of the residue signals along the pipeline chain, the accuracy requirement of the ensuing pipeline stages is alleviated, and the size of these stages, including the capacitors and the amplifiers therein, can be proportionally scaled down. Intuitively, a higher per-stage resolution results in less number of pipeline stages. However, a higher per-stage resolution requires higher gain, and hence smaller feedback factor in the pipeline stages, resulting in an exponentially increased per-stage power dissipation. Conversely, a lower per-stage resolution reduces the per-stage power dissipation, but more pipeline stages are needed, hence not necessarily power-efficient either. Put simply, there is an optimum stage scaling, or per-stage resolution, of the pipeline stages, and this depends on a number of factors. Some of these factors will now be reviewed.

2.4.1 Stage scaling

The determination of the optimum per-stage resolution involves maximizing SNR with a given power budget. The design leading to the optimum per-stage resolution depends on the process technology employed, conversion speed, topology of the pipeline stages, and the final layout. Due to the complexity of this problem, reported analyses [49-51] are largely qualitative analyses rather than quantitative analyses. Nevertheless, these qualitative analyses are useful as they offer a number of valuable insights to pipeline ADC designers, such as that reported in [51].

Figure 2.10 depicts the well-established circuit model [51] for the analysis to ascertain the optimum per-stage resolution. The analysis takes into account the switching noise (modelled by R1-R4), amplifier noise (g_m), conversion speed factor, amplifier small-signal closed-loop bandwidth, scaling factor (γ), parasitic capacitance at the input (C_g) and output (C_o) of the amplifier, and the sampling capacitor in the current

stage (C_S) and the ensuing stage (C_L). It is assumed that all the circuit components in the pipeline stages, including the capacitor size, g_m , and the bias current are scaled (down) along the pipeline chain by the scaling factor γ ($0 < \gamma < 1$).

Figure 2.10 Circuit model for the analysis of the optimum per-stage resolution [51]

For sake of brevity, the specific mathematical expression [51] for ascertaining the optimum per-stage resolution is not intuitive, hence not included hereinafter. Instead, more meaningful graph representations are depicted in Figure 2.11 where η is the speed factor (a large η means large C_o and C_g with respect to C_L (i.e., $C_o \approx C_g = \eta C_L$)). And the taper factor ‘ x ’ is related to γ by $\gamma = 1/2^{nx}$.

From Figure 2.11, it can be observed that at low conversion speed, the higher the per-stage resolution, the better is the energy-efficiency. This is largely due to the substantially scaled C_L . On the other hand, at high conversion speed, the optimum per-stage is 2 or 3 bits. This is largely because the increased loading effect of C_o eventually outweighs the scaled C_L .

Figure 2.11 Normalized power versus taper factor [51]

Note that the ‘low speed’ ($\eta=0$) scenario in Figure 2.11 is an extreme case assuming C_o is negligible. In practice, however, C_o cannot be ignored for the following three reasons. First, C_o may be comparable to or even larger than C_L in the case of fast stage scaling. Specifically, C_o largely includes the output parasitic capacitance of the amplifier, parasitic capacitance of the switches, input capacitance of the coarse ADC in the ensuing stage, and the wire capacitance of the inter connections. Consequently, C_o may be in the order of tens of fF in the final layout, e.g., 50fF in the design [6]. This value is larger than the noise-limited C_L equivalent to 10bit accuracy.

Second, C_o does not proportionally scale down with the stage scaling due to the relatively consistent wire and switch complexity. Instead, C_o may even increase for higher per-stage resolution. This is largely because higher per-stage resolution requires smaller feedback factor, which demands larger amplifier size and larger bias current to maintain the speed, in turn leading to larger C_o . Third, the loading effect of C_o increases with the increased conversion speed.

In view of these, the ‘low speed’ ($\eta=0$) scenario depicted in Figure 2.11 is largely academic. On the other hand, the ‘high speed’ ($\eta=1$) scenario offers substantial insights, and is often employed [2, 4, 21] for the determination of the optimum per-stage resolution.

2.4.2 Error Sources in the Pipeline ADC

Amongst the various building blocks in the pipeline ADC, the MDAC comprising the DAC and the amplifier is the most critical block. As aforementioned in Chapter 1, it is arguably the design bottleneck, and largely limits the resolution of the entire ADC, particularly at high conversion rate up to GS/s [2, 45, 51]. This is particularly true for the MDAC in the first stage because it is required to achieve full-resolution accuracy in terms of noise, distortion and nonlinearity; the requirements of subsequent stages are alleviated by the gain along the pipeline chain. In view of this, the review of the error sources in the pipeline ADC are largely pertaining to the MDAC in the first stage.

Figure 2.12 depicts the block diagram of the MDAC in the conventional pipeline ADC. There are four key error sources, namely the finite open-loop gain of the amplifier, incomplete MDAC settling, amplifier distortion, and capacitor mismatches. These errors will now be reviewed in turn.

Figure 2.12 Block diagram of the MDAC

(I) *Finite Open-loop Gain of the Amplifier (‘A’ in Figure 2.12) in the MDAC*

The finite A of the amplifier in the MDAC causes gain errors to the residue amplification. The effects of the finite A can be analytically ascertained [6] from the output of the MDAC:

$$V_{res_1} = \frac{C_{DAC}}{C_F + \frac{1}{A}(C_{DAC} + C_F + C_P)} V_S - \frac{d_1 C_1 + \Lambda + d_m C_m}{C_F + \frac{1}{A}(C_{DAC} + C_F + C_P)} V_{ref} \quad (13)$$

where $C_{DAC} = C_1 + \Lambda + C_m$ with $m = 2^{n_1}$ and where $d_1 \dots d_m$ are the thermometer code that controls the capacitor array, A is the open-loop gain of the amplifier, V_{ref} is the reference voltage of the ADC, C_{DAC} is the total capacitance of the DAC, C_P is the parasitic capacitance at the amplifier input, and C_F is the capacitance of the feedback capacitor.

Ideally, A is infinite, and V_{res} is then independent of A . However, in reality, A is finite, where from eqn. (13), finite A introduces gain error and degrades the accuracy of V_{res} [2, 6, 23, 52]. To keep the input-referred error to $< \frac{1}{2}\text{LSB}$, A is required [6, 7] to be:

$$A > (2^{n+1} - \frac{C_{DAC}}{C_F}) \times (1 + \frac{C_F}{C_{DAC}} + \frac{C_P}{C_{DAC}}) \quad (14)$$

where n is the resolution of the overall ADC, and (C_{DAC}/C_F) is the stage gain.

On the basis of eqn. (14), it can be seen that the requirement of the open-loop gain increases exponentially with the increment of the resolution. In the case of an 11bit pipeline ADC with stage gain of two, A is required to be $>70\text{dB}$. This requirement is initially not a critical issue for ADCs realized in dated (long channel devices) process technologies. However, with process technology scaling, the difficulty for design and realization of such amplifiers is increasingly challenging due to the reduced supply voltage and the decreased transistor intrinsic gain, particularly in deep submicron technologies such as CMOS 28nm, and 16nm CMOS.

Figure 2.13(a) and (b) depict the impact of the finite A on the transfer characteristics of the pipeline stage and on the overall ADC respectively; for sake of brevity, it is assumed that finite A is the only error source and the first stage is of 1bit resolution. The dashed line and the solid line are the ideal (with infinite A) and the practical (with finite A) transfer function curves respectively. It can be observed that the finite A reduces the stage gain (slope of the transfer function curves), resulting in a negative gain error. This negative gain error reduces the signal swing of V_{res} . Consequently, the signals in the vicinity of reference rails are lost, and the corresponding digital outputs are missing (i.e., missing codes).

Figure 2.13 Impact of the finite A on the transfer characteristics of the (a) pipeline stage, and (b) overall ADC

Further, by means of MATLAB simulations and FFT computations (16384 data points), we can discover the impact of the finite A on the ADC SNDR and SFDR (Spurious Free Dynamic Range). We depict in Figure 2.14 the obtained SNDR and SFDR with A ranging from 50dB to 70dB for stage gain of 2, 4 and 8. We made two observations can be made from Figure 2.14.

First, these SNDR and SFDR generally decrease with the reduced A . This is largely attributed to the increased gain error introduced by a smaller A . Second, in the perspective of the stage gain, a lower stage gain leads to smaller SFDR and worsened SNDR for the same A . This indicates that an ADC with lower stage resolution is relatively more sensitive to the finite A , and hence to achieve the desired accuracy, a higher A is often required for an ADC with lower stage resolution; stage gain = $2^{(\text{stage resolution})}$. This indication is congruous to the aforesaid eqn. (14).

Figure 2.14 SNDR and SFDR versus the amplifier open-loop gain (A)

(II) Capacitor Mismatches

The capacitor mismatches in the MDAC typically stem from two sources: the mismatch between C_F and C_{DAC} , and the mismatch between C_F and C_i , where $C_i \in (C_1$ to $C_m)$; see Figure 2.12. The former causes gain errors to the residue transfer curve, and the latter introduces nonlinearities at the transition points between the adjacent regions in the residue transfer curve. The effects of aforesaid capacitor mismatches are now analytically described [6, 7, 47, 53] on the basis of the aforesaid eqn. (13).

(a) Gain errors due to mismatch between C_F and C_{DAC}

To analyze the capacitor mismatch, it is assumed that C_{DAC} deviates Δ . On this basis, the stage gain is equal to

$$\frac{C_{DAC} + \Delta}{C_F} = \frac{C_{DAC}}{C_F} \left(1 + \frac{\Delta}{C_{DAC}}\right) \quad (15)$$

with gain error equal to $\frac{C_{DAC}}{C_F} \left(\frac{\Delta}{C_{DAC}}\right)$.

On the basis of eqns. (13) and (15), it can be seen that a larger V_S multiplying the derived gain error results in a larger deviation of the residue signal. We will now explain the said gain error on the basis of the worst-case and the best-case scenarios.

For the worst-case scenario where $(V_S = V_{ref} - V_{ref} \frac{C_F}{C_{DAC}})$, in order to have the input-referred gain error $< \frac{1}{2}\text{LSB}$ for n -bit resolution, the requirement of the capacitor mismatch is as follows.

$$\frac{\Delta}{C_{DAC}} (V_{ref} - V_{ref} \frac{C_F}{C_{DAC}}) < \frac{1}{2} \frac{V_{ref}}{2^n}, \quad (16)$$

which can be rewritten as

$$\frac{\Delta}{C_{DAC}} < \frac{1}{2^{n+1} \left(1 - \frac{C_F}{C_{DAC}}\right)} \quad (17)$$

For the best-case scenario where $(V_S = V_{ref} \frac{C_F}{C_{DAC}})$, the mismatch requirement is

$$\frac{\Delta}{C_{DAC}} (V_{ref} \frac{C_F}{C_{DAC}}) < \frac{1}{2} \frac{V_{ref}}{2^n} \quad (18)$$

which can be rewritten as

$$\frac{\Delta}{C_{DAC}} < \frac{C_{DAC}}{2^{n+1}C_F} \quad (19)$$

Eqns. (17) and (19) respectively depict the lower and upper boundaries for the mismatch between C_F and C_{DAC} imposed by the gain errors for n -bit resolution. In the case of advanced CMOS process technologies (e.g., 40nm and 65nm) where the capacitor mismatch could be $<0.1\%$, when good layout techniques are employed [3, 12, 13, 15], a pipeline ADC of stage gain $(C_{DAC}/C_F) = 2$ can achieve a resolution of 10 bits without post-fabrication trimming or calibration.

The gain errors caused by the mismatch between C_F and C_{DAC} can be either negative ($\Delta < 0$) or positive ($\Delta > 0$). Figure 2.15(a) and (b) depict the effects of the said two cases on the transfer characteristics of the pipeline stage and the overall ADC transfer respectively. It can be observed that the gain errors (for both cases) result in two types of impairments on the overall ADC transfer characteristics, namely missing codes and wide codes. The missing codes occur when the upper rail of the residue signal is smaller than V_{ref} , or when the lower rail is higher (more positive) than $(-V_{ref})$; akin to the effect of the aforesaid finite amplifier open-loop gain. Conversely, the wide codes occur when the rails of the residue signal exceed V_{ref} or $(-V_{ref})$. Specifically, as the ensuing pipeline stages are unable to quantize signals exceeding the full-scale reference, these stages output either all '0's (when $V_{res} < -V_{ref}$) or all '1's (when $V_{res} > V_{ref}$). It is worthwhile to note that wide codes imply missing decision levels [47, 54], and the original input signal cannot be correctly reconstructed.

(a)

(b)

Figure 2.15 Effects of the gain errors for (a) $\Delta < 0$, and (b) $\Delta > 0$

(b) Nonlinearity due to the mismatch between C_F and C_i

The nonlinearity due to the mismatch between C_F and C_i will now be analytically reviewed. On the basis of the thermometer code $(d_1 \cdots d_m)$ in eqn. (13), the residue

generation can be divided into $m+1$ regions (i.e., region 0 to region m) [6], i.e., the residue generation transfers from region $(i-1)$ to region i when d_i switches from 0 to 1. In view of this, the residue signal (i.e., V_{res_1} for the first stage) for region i can be rewritten to be

$$V_{res_1}(i) = \frac{C_{DAC}}{C_F + \frac{1}{A}(C_{DAC} + C_F + C_P)} V_S - \frac{C_1 + C_2 + \Lambda + C_i}{C_F + \frac{1}{A}(C_{DAC} + C_F + C_P)} V_{ref} \quad (20)$$

Assuming A is infinite, at the transition point between regions $(i-1)$ and i , V_{res_1} exhibits a vertical jump, $V_{jump} = V_{res_1}(i) - V_{res_1}(i-1) = (C_i/C_F)V_{ref}$.

Ideally, $C_i = C_F$ so that $V_{jump} = V_{ref}$. In the case of capacitor mismatch, i.e., $C'_i = C_i + \Delta_i$, the vertical jump with mismatch (V_{jump_m}) is obtained as

$$V_{jump_m} = \left(\frac{C_i + \Delta_i}{C_F}\right)V_{ref} = \left(1 + \frac{\Delta_i}{C}\right)V_{ref} \quad (21)$$

with an error equal to $\frac{\Delta_i}{C}V_{ref}$.

To ensure that the input-referred error due to $(\frac{\Delta_i}{C}V_{ref})$ is sufficiently small, e.g., $<1/2\text{LSB}$, the following criterion needs to be satisfied:

$$\left(\frac{\Delta_i}{C}V_{ref} \times \frac{C_F}{C_{DAC}}\right) < \frac{V_{ref}}{2^{n+1}} \quad (22)$$

This can be rewritten as

$$\frac{\Delta_i}{C} < \left(\frac{1}{2^{n+1}} \times \frac{C_{DAC}}{C_F} \right) \quad (23)$$

Eqn. (23) expresses the matching requirement between C_F and C_i for n -bit resolution. On this basis and given that modern process technologies (65nm, 40nm, etc.) can provide 0.1% capacitor mismatch, 10bit resolution can be achieved without post-fabrication calibrations and trimmings; the stage gain ($\frac{C_{DAC}}{C_F}$) is assumed to be 2.

Figure 2.16(a) and (b) depict the impact of Δ_i on V_{res} and the overall ADC transfer characteristic for $\Delta_i > 0$ and $\Delta_i < 0$ respectively. It can be observed that Δ_i causes over-range and under-range at the transition point between the adjacent regions for V_{res} generation. This inevitably results in wide codes and missing codes on the overall ADC transfer characteristic. It is worthwhile to note that as the mismatch between C_F and C_i varies for different i values due to the random process variation, the errors will be different at different transition points. This undesirably exacerbates the nonlinearities of the overall ADC.

(a)

(b)

Figure 2.16 Impact of Δ_i for (a) $\Delta_i > 0$, and (b) $\Delta_i < 0$

(III) Incomplete MDAC Settling

V_{res} in eqn. (13) assumes that the MDAC settling is complete. In practice, the MDAC, particularly in high-resolution GS/s pipeline ADCs, often does not have

sufficient time to settle completely, thereby resulting in errors associated with settling time. The two primary mechanisms that limit the settling time for the MDAC are as follows. First, as the operation of the conventional pipeline blocks (e.g., front-end sampling and sub-ADC conversion) [23, 55] and associated timing overheads (e.g. clock rise and fall time, buffer delays, etc.) [7] requires substantial time, the ensuing residual settling time available for the MDAC is severely limited. Second, as the conversion rate increases to GS/s, the time available for the MDAC settling is further limited. In the case of a 1GS/s ADC, the time available for the MDAC settling is $\sim 160\text{ps}$ (16% of the clock period) [6, 7, 55, 56], and this is largely insufficient for resolution of more than 10 bits with a reasonable power budget. In view of these, it is imperative to investigate the characteristics of the MDAC settling, particularly its relationship/trade-offs with the speed, resolution and power dissipation. We will now review this.

Figure 2.17 depicts the typical transient waveform of an MDAC output for an impulse or step change. The settling can be divided into two segments. First, the MDAC output slews from its initial value (before the step change at the output) to the vicinity of the final value (V_o); In Figure 2.17, this is indicated as slewing. Second, the output of the MDAC recovers from overshoots and/or undershoots, and settles to V_o with an error band (E_o), indicated as recovering and linear settling in Figure 2.17. The said overshoots and undershoots are largely due to the finite bandwidth of the MDAC, and E_o is largely ascertained by the accuracy requirement of the MDAC, i.e., in the case of a 10bit accuracy, E_o is required to $< 0.1\% V_o$.

Figure 2.17 Transient waveform of the MDAC output

The analysis for the said two segments of the MDAC settling will now be delineated in turn.

In the case of Slewing, the slew rate (dV/dt) at the output is required to be $dV/dt \leq \Delta V \times 2\pi \times f_{UGBW}$ to ensure linear slewing; where ΔV is the step size, and f_{UGBW} is the unity gain bandwidth of the MDAC. On this basis, the current required (I_{req}) to ensure fast charge/discharge of the loading capacitor (C_{load}) is [57] $I_{req} = C_{load} \times (\Delta V \times 2\pi \times f_{UGBW})$. To visualize the relationship between the power dissipation and the speed, we depict in Figure 2.18 the I_{req} versus f_{UGBW} for different C_{load} values; ΔV is assumed to be 1V.

Figure 2.18 I_{req} versus f_{UGBW} for different C_{load}

From Figure 2.18, we observe, as expected, that I_{req} increases linearly with both the increment of f_{UGBW} and C_{load} . Consequently, to minimize the power dissipation while maintaining a high conversion rate, it is highly desirable to reduce the C_{load} of the MDAC instead of reducing f_{UGBW} as the latter undesirably reduces the conversion rate. Further, a smaller C_{load} results in a smaller error band (E_o) [57], leading to higher accuracy.

In the case of recovering and linear settling, to ascertain the quantitative relationship between the recovering and linear settling time, the accuracy, and the power dissipation, the small signal response of the MDAC can, to the first order, be approximated as [57]

$$V_{res} = V_o \left(1 - e^{\frac{-t}{\tau}} \right) \quad (24)$$

where τ denotes the time constant of the MDAC.

The settling error (ΔV_{res}) at time t can be obtained from $\Delta V_{res} = V_o e^{\frac{-t}{\tau}}$.

Consequently, to achieve M -bit accuracy, ΔV_{res} needs to be [57]:

$$\frac{\Delta V_{res}}{V_o} = e^{\frac{-t}{\tau}} < \frac{1}{2^{M+1}} \quad (25)$$

This translates to the required MDAC settling time,

$$t > (M + 1)\tau \ln 2 \quad (26)$$

Eqn. (26) depicts the speed-resolution trade-off imposed by the MDAC settling. To gain insight on the associated power dissipation (by means of its transconductance, g_m), it is assumed that the settling is dominated by a single time constant, or a single pole in general; a single-pole MDAC ensures faster settling with smaller settling error—required by high-speed high-resolution ADC designs. Assuming that $\tau = \frac{C_{load}}{g_m \beta}$, where β is the feedback factor, eqn. (26) can be re-expressed as:

$$g_m > \frac{C_{load}}{\beta t} (M + 1) \ln 2 \quad (27)$$

Further, by substituting t and g_m with $\alpha \frac{1}{f_s}$ and $\sqrt{2kI_D}$ respectively, eqn. (27)

can be rewritten as

$$I_D > \frac{1}{2k} \left[\frac{C_{load} f_s}{\beta \alpha} (M + 1) \ln 2 \right]^2 \quad (28)$$

where α is a fraction of the sampling period that is available for the linear settling, I_D is the dc current needed, and $k = \mu C_{ox} \frac{W}{L}$ with charger-carrier effective mobility of μ , gate oxide capacitance (per unit area) of C_{ox} , and transistor width W and length L .

Eqn. (28) specifies the minimum I_D required to achieve M -bit accuracy at f_s sampling rate. Of particular note, I_D increases quadratically with the conversion rate and the resolution. Also, to reduce I_D without compromising the conversion rate and the resolution, it is imperative to minimize C_{load} and enlarge β .

It is insightful to appreciate that when the operating speed of the MDAC approaches the speed limit of the process technology, the required current increases substantially—a disproportionate higher power is required for speed [6, 7]. In other words, the amplifiers in the MDAC suffer from diminishing returns in their speed as their power consumption is raised, largely attributed to the increased parasitic effects, velocity saturation effect, etc. [7]. To alleviate this issue, ultra-high-speed high-resolution ADC designs tend to employ redundancies and/or calibrations to correct the error via backend digital processing. Note that the settling error results in gain errors, whose impact on the overall ADC performance is akin to the aforesaid finite amplifier open-loop gain.

2.4.3 Error Mitigations

Reported attempts to mitigate the aforesaid MDAC errors can arguably be categorized into two groups. The first group leverages on circuit innovations and/or design techniques to boost the performance of the MDAC to the required accuracy. For example, in the case of achieving sufficient amplifier open-loop gain, the pertinent circuit techniques include cascading one or two more stages [47, 48], telescopic cascade

[58, 59], folded cascade [60, 61], and gain boosting with feedback stages [51, 59]. By means of these techniques, the amplifiers in dated process technologies (i.e., long-channel technology nodes) can achieve $>100\text{dB}$ open-loop gain. However, the effectiveness of the said techniques diminishes with the process technology scaling in view of the exacerbated transistor nonlinearity, reduced transistor intrinsic gain and the low power supply voltage. For example, the gain of the amplifiers in submicron process technologies in state-of-the-art high-speed and high-resolution ADCs [6, 19, 20, 31, 62] is typically $< 70\text{dB}$ while that of dated may exceed 90dB [45-48, 63].

In the case of achieving the targeted capacitor matching, the prevalent techniques include “Sandwich” capacitors [12] customized to minimize the parasitic and routing capacitance, employment of shielding ring to isolate the external coupling [13], and large unit capacitors with common-centroid layout [3, 15]. Such techniques can facilitate the pipeline ADC achieve 10 to 12 bits without any post-fabrication calibrations or trimmings. The associated penalties, nevertheless, involve increased design effort, larger silicon area and power overheads, etc.

The second group of error mitigations involves the employment of calibrations, particularly digital calibrations that is increasingly attractive to pipeline ADCs. The general concept behind the different calibration schemes are similar—the pipeline ADCs are allowed to be realized with impairments as long as the associated errors can be mitigated at later juncture. Typically, the calibration comprises two parts, namely error detection and error correction. The former is critical, and serves to obtain the pertinent correction factors/coefficients for the error mitigation [6, 20, 64, 65]. Once the coefficients are obtained, the correction is often simply performed by means of addition, subtraction and multiplication in the digital domain. We will now review the error detection and error correction in turn.

On the basis of the methodologies of error detection, the calibrations can arguably be divided into two categories. The first category involves the detection with a known pilot input signal. This signal can be a very linear (with linearity better than the ADC under calibration) ramp signal or a sequence of pertinent dc voltages at the transition points of the residue signals [6, 20, 63, 65, 66]. By means of comparing the actual ADC digital outputs with the ideal outputs for the pilot input signal, the errors of the ADC are obtained. These errors include gain errors and capacitor nonlinearities (see Section 2.1.3 earlier). On the basis of the obtained errors, the corresponding correction factors are determined, stored, and thereafter applied to the ADC outputs for digital correction.

There are three shortcomings for this calibration category. First, they often need to be performed in the foreground, hence inevitably interrupting the ADC normal operation. Second, as the correction factors are obtained and fixed in the foreground, they are not able to track, and mask time-varying and dynamic errors, e.g., temperature and supply voltage variations. Third, the generation of the pilot input signals, e.g., high linear ramp signals, could entail substantial area and power overheads.

Figure 2.19 depicts an example [6] of the said calibration. The correction factors are denoted by β_j and $1/\alpha$, where the former and the latter respectively serve to correct the capacitor nonlinearities and the gain error. These two factors are obtained by setting the V_{in} to the transition points of V_{res} , and subsequently comparing the output, D_{res} , from the ensuing stages with the ideal output. An example of the detailed calculations for the two factors are explained in [6]. The obtained β_j is stored in a look-up table, whereas $1/\alpha$ is stored in digital registers. Finally, the digital output is corrected by applying the following function.

$$D_{corr} = \frac{1}{\alpha} (D_{res} + \beta) \quad (29)$$

where D_{corr} is the digital output after error correction.

Figure 2.19 Exemplar calibration embodying known pilot signal

The second calibration category involves adaptive algorithms for the error detection and correction, including the well-established Least-Mean-Square (LMS) algorithm [20, 25, 28] and the digital statistical estimation algorithm [25]. For error mitigation, the adaptive algorithms typically rely on a “reference” point (e.g., an ‘error-free’ ADC output) instead of a pilot input signal. In the detection, the LMS algorithm serves to align the ADC output to the “reference” point by means of recursively (in small step sizes) adjusting the ADC output. The correction factors are obtained by accumulating all the step sizes involved during the adjustment. These correction factors are often stored in memory (e.g., look-up tables) for the ensuing error correction, akin to the aforesaid first category. Note that the said “reference” point is often generated by

an additional reference ADC that features a higher resolution than the ADC under calibration [30, 67], or by pseudorandom binary sequence generator[16, 21], or by the ADC under calibration, with additional hardware modifications to obtain a few linear points [25].

Unlike the aforesaid first calibration category, this category is able to advantageously operate in the background, hence capable of tracking and mitigating time-varying and temperature-varying dynamic errors. Nevertheless, its cost is severe. First, as aforementioned, additional high-resolution reference ADCs or pseudorandom binary sequence generator are often needed, leading to increased hardware and power overheads, and increased design difficulty. Although a reported design [25] avoids the additional reference ADC, the requirements for two-mode operations and the complex digital statistical estimation severely limit the conversion rate and undesirably increase the design complexity. Second, the adaptive algorithm requires a long convergence time, e.g., >100ms, which limits its applications. Further, when the nonlinearity errors increase with technology scaling, the complexity of the error estimation rapidly increases, exacerbating convergence time [32]. Third, the complex digital calibration circuit for the adaptive algorithm undesirably increases the design difficulty of the ADC. Consequently, these calibrations are often performed off-chip by means of software (e.g., MATLAB) [10, 11, 21, 29-31, 34, 36, 58].

Figure 2.20 depicts an example [25] of the said calibrations. h_1 in Figure 2.20(a) is employed as the “reference” point because it exhibits minimized distortions. h_2 is the output that contains larger errors that need to be corrected. Figure 2.20(b) depicts the conceptual diagram for the error detection and correction with a_3 as the correction factor. In detection, the LMS algorithm recursively updates the value of a_3 with step size of u

until the mean-square value of $(h1-h2)$ equals 0. The final value of a_3 is stored in the look-up table [25], and is employed to correct the errors in the output (D_{res}).

(a)

(b)

Figure 2.20 (a) Concept of the exemplar calibration, and (b) the associated block diagrams

In summary, for the design and realization of high-speed and high-resolution pipeline ADCs, the MDAC is the bottleneck as it introduces a number of undesirable issues that literally constrain the overall ADC performance, particularly with process technology scaling and with conversion rates up to GS/s or multi-GS/s. Although a number of attempts [24-26, 28, 33-36, 48, 53, 68, 69] have been reported to mitigate these issues, these attempts often suffer from various shortcomings and limitations, and their efficiency is somewhat contentious. Consequent to our critical review of the pipeline ADC, there is a good possibility that a pipeline ADC that eliminates the need of the MDAC (i.e., MDAC-free) is potentially more advantageous for the realization of high-speed high-resolution ADCs; we will delineate our proposed MDAC-free ADC in Chapter 3.

2.5 SAR ADC

Other than the pipeline ADC, the SAR ADC is another prevalent architecture for high-speed high-resolution ADCs. Figure 2.21 depicts the block diagram of a typical SAR ADC. Its modus operandi is largely a binary search through all possible quantization levels before converging to the final digital output. Typically, N iterations of the binary search are required to achieve N -bit resolution. The first iteration serves to resolve the MSB bit, and with each iteration, one more digital bit is resolved and the DAC output V_{OUT} is one step closer to the equivalent sampled input. At the end of the conversion (EOC), the final digital output is obtained and V_{OUT} is approximately equal to the sampled input.

Figure 2.21 Block diagram of a typical SAR ADC

The DAC in the SAR ADC is either resistive (akin to the resistor string in the flash ADCs), or capacitive (i.e., a charge-redistribution CDAC that integrates the S/H function). State-of-the-art SAR ADCs [11, 15, 38, 70-72] often employ the latter because it does not dissipate static current, and the capacitor matching is often better than resistor matching for most of the process technologies. In view of this, our reviews henceforth will largely be focused on the capacitive SAR ADC.

There are four worthy merits of the SAR ADC. First, the design of the SAR ADC is typically highly scalable between fabrication processes because of its structural simplicity. Specifically, as the SAR ADC does not require challenging analog components, e.g., high-gain wide-bandwidth amplifiers in the pipeline ADC, the design difficulty is substantially lower, and designs in the dated process technologies can be easily transferred and realized in contemporary advanced processes. Second, process technology scaling is directly beneficial to the enhancement of the conversion rate of the SAR ADC. This is because of the increased transistor cut-off frequency and reduced parasitic capacitance as the minimum feature size is scaled downwards. There are

numbers of KS/s SAR ADCs based on dated processes, redesigned for tens and hundreds MS/s conversion rate [59, 73, 74]. Third, the decreased capacitance density with process technology scaling allows designers to realize smaller capacitance with larger physical size. This enhances both capacitor matching and capacitor charging/discharging speed, thereby leading to higher accuracy and higher conversion rate. Fourth, the SAR ADC typically features high energy efficiency as it often dissipates only dynamic power instead of static power.

2.5.1 Linearity

On the basis of the CDAC structure, SAR ADCs can be categorized into binary-based, unary-based and segmented-based SAR ADCs [11, 15, 38, 70-72]. The linearity attributes of these ADCs are similar. As their analyses are similar, for sake of brevity, we will review only the binary-based SAR ADC. For sake of completeness, a summary of the linearity behavior of the unary- and segmented-based will be presented at the end of this section.

Figure 2.22 depicts the block diagram of a typical binary-based SAR ADC where the capacitors ($C_0 \wedge C_{N-1}$) in the CDAC are binary weighted; C_C is the complementary capacitor employed to facilitate the binary increment. The nonlinearity, i.e., INL (Integral Nonlinearity) and DNL (Differential Nonlinearity), largely arises from the capacitor mismatches in the binary CDAC [71]. We will now review these two non-linearities.

Figure 2.22 Block diagram of a typical binary-based SAR ADC

(I) INL

To obtain the INL characteristics, the transfer function of the CDAC needs to be ascertained. From Figure 2.22, the CDAC output (V_{DAC}) can be easily derived [71]:

$$V_{DAC} = \frac{\sum_{i=0}^{N-1} D_i \times C_i}{C_C + \sum_{i=0}^{N-1} C_i} \times V_{ref} \quad (30)$$

where D_i is the digital input(s) to the CDAC, and N is the CDAC resolution.

Note that the parasitic capacitance at the input terminals of the comparator is negligible and is attributed to the following two reasons. First, the parasitic capacitance is typically much smaller than the CDAC output capacitance, e.g., a few orders of magnitude smaller, and is hence not critical [15, 71]. Second, as most CDACs utilize the well-known bottom-plate sampling technique [8, 38, 70, 73], the said parasitic

capacitance only slightly degrades the V_{DAC} gain, and does not affect the comparison result.

Consider now the modeling of the capacitor mismatch. C_i is defined as

$$C_i = 2^i C_u + \delta_i \quad (31)$$

where C_u is the unit capacitor in the CDAC, and δ_i is a random variable with a zero mean and a variance of

$$\sigma_i^2 = E[\delta_i^2] = 2^N \sigma_0^2 \quad (32)$$

with σ_0 being the standard deviation of C_u .

Substituting eqn. (31) into eqn. (30), the INL is obtained as

$$INL = V_{DAC,actual} - V_{DAC,ideal} = \frac{\sum_{i=0}^{N-1} D_i \times \delta_i}{2^N C_u + \sum_{i=0}^{N-1} \delta_i} \times V_{ref} \quad (33)$$

For the worst-case scenario, typically occurring at the mid-scaled code (i.e., $D_i = 10 \wedge 0$), the variance of the INL can be expressed as [71, 75]

$$\begin{aligned} \sigma_{INL}^2 &= E[(V_{DAC,actual}[10 \wedge 0] - V_{DAC,ideal}[10 \wedge 0])^2] \\ &\approx \frac{2^{N-1} \sigma_0^2}{2^{2N} C_u^2} \times V_{ref}^2 \\ &= 2^{N-1} \left(\frac{\sigma_0}{C_u} \right)^2 LSB^2 \end{aligned} \quad (34)$$

Eqn. (34) depicts the worst-case INL characteristic of the binary CDAC-based SAR ADC with respect to the σ_0 . As σ_0/C_u denotes the capacitor matching, to ensure $\sigma_{INL} < \frac{1}{2}LSB$, σ_0/C_u is required to be:

$$\frac{\sigma_0}{C_u} < \frac{1}{2^{(N+1)/2}} \quad (35)$$

(II) DNL

The DNL can be obtained by subtracting two consecutive DAC outputs over the full output range, and thereafter comparing the resulted residue with one LSB. Akin to the INL, the worst-case DNL also typically occurs at the mid-scale output [71, 75]:

$$\begin{aligned} DNL &= V_{DAC}[10\Lambda 0] - V_{DAC}[01\Lambda 1] - 1LSB \\ &\approx \frac{\delta_{N-1} - \sum_{i=0}^{N-2} \delta_i}{2^N C_u} \times V_{ref} \end{aligned} \quad (36)$$

The variance of the DNL:

$$\begin{aligned} \sigma_{DNL}^2 &= E[DNL^2] \\ &\approx 2^N \left(\frac{\sigma_0}{C_u} \right)^2 LSB^2 \end{aligned} \quad (37)$$

Eqn. (37) depicts the DNL characteristics of the binary CDAC-based SAR ADC.

On this basis, to ensure $\sigma_{DNL} < \frac{1}{2}LSB$, the required capacitor matching (σ_0/C_u) is:

$$\frac{\sigma_0}{C_u} < \frac{1}{2^{(N+2)/2}}. \quad (38)$$

From eqns. (35) and (38), it can be observed that the DNL imposes a higher capacitor matching requirement than INL; in the case of 10bit accuracy, the requirements for the capacitor matching are 2.2% and 1.56% imposed by INL and DNL respectively. Put simply, the linearity behavior of the binary CDAC-based SAR ADC is largely ascertained by its DNL characteristics, i.e., by ensuring the standard deviation of the DNL $< \frac{1}{2}\text{LSB}$.

By means of similar analysis, the linearity behaviors of the unary and segmented SAR ADCs can be obtained [71]. Table 2.1 summarizes the resulting INL and DNL for the binary, unary, and segmented SAR ADCs. We made three observations. First, the same INL behaviors is noted for the different types of ADCs despite their different DNL behavior. Second, the binary SAR ADC is most vulnerable to the capacitor mismatch as it suffers from the largest DNL with respect to σ_0 , followed by the segmented and unary SAR ADCs. Third, the capacitor-matching requirement for the binary SAR ADC is largely ascertained by its DNL characteristics, whereas the unary and segmented SAR ADCs are determined by the INL characteristics.

Table 2.1 Linearity behavior of binary, unary, and segmented SAR ADCs

	Standard deviation of INL (LSB)	Standard deviation of DNL (LSB)
Binary	$2^{\frac{N-1}{2}} \left(\frac{\sigma_0}{C_u} \right)$	$2^{\frac{N}{2}} \left(\frac{\sigma_0}{C_u} \right)$
Unary	$2^{\frac{N-1}{2}} \left(\frac{\sigma_0}{C_u} \right)$	$\left(\frac{\sigma_0}{C_u} \right)$
Segmented	$2^{\frac{N-1}{2}} \left(\frac{\sigma_0}{C_u} \right)$	$2^{\frac{N-k+1}{2}} \left(\frac{\sigma_0}{C_u} \right)$

2.5.2 Mitigation of Nonlinearities

The most direct means of mitigating the nonlinearities of the SAR ADC is by means of precision circuit/component designs such as customized unit capacitors to enhance capacitor matching, and enlarged unit capacitors with effective layout techniques, etc. In this sense, this is akin to the aforesaid pipeline ADC. Nevertheless, this approach often suffers from undesirable penalties of larger power and hardware overheads, and is arguably ineffective for >10bit resolutions.

An alternative and increasingly prevalent approach to mitigate the nonlinearity is to employ a redundancy technique [76, 77]. This technique typically creates multiple conversion paths from an input to its equivalent digital output. In the case of an error during conversion, an alternative conversion path is taken to obtain the correct digital output. Note that without redundancy, only one conversion path is available, and hence a conversion error inevitably leads to an incorrect digital output.

Mathematically, the digital output bits (D_{out}) of an SAR ADC with redundancy embody <2 radix modality (instead of a radix of 2 without redundancy). Specifically,

$$D_{out} = \alpha \sum_{i=0}^{N-1} D_i \beta^{-(N-i)} \quad (39)$$

where $\beta < 2$, denoting the radix of the digital bits, and $\alpha = (\beta - 1)$, denoting a scale factor required to ensure the full-scale of the D_{out} equal to 1.

Figure 2.23 depicts an example 3bit SAR conversion with redundancy, i.e., $\beta = 2^{3/4}$. It can be observed that there are at least 2 available paths for each digital output except for the first and the last outputs. When an error occurs during the conversion, the correct digital output is still obtained via the alternative path (i.e., the dash line). Note

that a smaller β will create more conversion paths from the input to the digital outputs, hence higher error tolerance.

Figure 2.23 Conversion concept of an SAR ADC with redundancy

Despite the benefit offered from the redundancy technique, it often suffers from two undesirable penalties. First, the redundancy needs additional conversion iterations, hence constraining the conversion rate. In the case of the example depicted in Figure 2.23, four iterations are needed to resolve 3 bits (instead of 3 iterations without redundancy). Second, additional hardware is required to map the non-binary outputs to binary outputs, leading to power and hardware overheads, hence increased cost.

2.5.3 Speed Limitation

The SAR ADC suffers from a primary issue—the conversion rate is severely limited by the successive approximation conversion algorithm, i.e., at least N iterations

for N bits. Even with enhanced speed arising from employing advanced deep submicron technology processes, it is still acutely difficult for the conventional single-channel SAR ADC to achieve $\text{GS/s} \geq 10\text{bit}$ attributes.

Extensive efforts have been reported [38, 39, 61, 76, 78] to attempt to alleviate the speed limitation. The M -bit/step scheme [15, 39, 79] is a prevalent technique to enhance the conversion rate of the SAR ADCs, and can theoretically improve the ADC conversion rate by approximately M times by leveraging on multiple reference voltages. Among these M -bit/step schemes, the 2bit/step scheme is arguably the most efficient due to its lower hardware and power overheads. The 2bit/step SAR scheme typically performs three parallel comparisons between input signal and three pertinent reference voltages respectively to identify the voltage range where the input signal locates. By this mean, 2 digital outputs are resolved in one clock cycle (in one SA iteration). In the perspective of hardware realization, the 2bit/step SAR scheme often requires three DACs to generate the three reference voltages, three comparators to perform the comparisons, and decoding circuit to decode the comparison outputs to the pertinent 2bit digital outputs.

Of late, various state-of-the-art 2bit/step SAR ADCs [12, 13, 39, 76, 78] were reported with enhanced conversion rate ranging from hundreds of MS/s up to GS/s. Nevertheless, these 2bit/step SAR ADCs often suffer from various undesirable issues that inevitably limit the achievable resolution or conversion rate. These issues largely arise from increased hardware overheads, large input loading, complex path routing etc.

For example, a reported 2bit/step SAR ADC [13] required three fully-differential capacitor-DACs (CDACs) realized with six capacitor arrays, and this requirement substantially increases the hardware overheads and the input loading. Consequently, the

resolution of such ADCs is severely limited. Another reported 2bit/step ADC [39] employed a resistive DAC to avoid the hardware overheads arising from the excessive CDACs. However, the employment of the resistive DAC requires large number of switches and complex routing that largely limit the reference settling time, thereby limiting the conversion rate. Further, the poor matching of the resistors in the said ADC constrains the achievable resolution.

A reported improved 2bit/step SAR ADC [76] requires only two differential CDACs (four capacitor arrays) among which only one CDAC contributes to the input loading. However, the associated top-plate sampling of these four capacitor arrays undesirably makes the ADC more vulnerable to the mismatch between the said capacitor arrays, including the mismatch between their associated parasitic capacitance, path routing and the switching non-idealities (e.g., clock feedthrough and charge injection) during the input sampling. Consequently, the resolution of this ADC is also somewhat constrained. Although decision redundancies were employed to improve the decision error tolerance and a dummy comparator was used to improve the routing matching, the penalty of associated hardware overheads and power dissipation is high.

In summary, the SAR ADC is increasingly prevalent due to its high structure simplicity, high energy efficiency, and compatibility with ever-decreasing process technology nodes. Nevertheless, the speed limitation arising from the successive approximation algorithm remain a constraint, and the prior-art attempts to mitigate this limitation often results in excessive hardware complexity and overheads, generally leading to inefficient designs. Consequent to our review of the SAR ADC, it would be interesting to explore the design of an SAR ADC embodying a more advantageous 2bit/step conversion scheme featuring low hardware complexity, low input loading, and

small power overhead; see our proposed novel 2bit/step SAR ADC design in Chapter 4 later.

2.6 SUMMARY

We have critically reviewed high-speed high-resolution Nyquist-rate ADCs, including the delineation of the imperative performance attributes. In view of high-speed and high-resolution, the emphases of our review are the prevalent pipeline-based and SAR-based realizations, including a critical review of the critical design issues and state-of-the-art attempts to mitigate these issues. Consequent to our critical review, for the pipeline-based realization, we argue that an MDAC-free pipeline ADC could potentially circumvent the yet unsolved issues for the design and realization of high-speed high-resolution pipeline ADCs—such an architecture is potentially more advantageous than the conventional pipeline ADC. For the SAR-based realization, we argue that a 2bit/step SAR ADC could potentially mitigate the speed limitation with reduced input loading, simplified hardware complexity, and minimal power overhead.

In view of the critical review of pipeline and SAR ADCs, we will now in turn describe a proposed MDAC-free pipeline ADC design and a proposed 2bit/step SAR ADC design in Chapters 3 and 4 respectively.

Chapter 3 A 1GS/s 11BIT SAR-ASSISTED

MDAC-FREE PIPELINE ADC

3.1 INTRODUCTION

This chapter delineates the design, monolithic realization, and measurements (and verification) of our proposed 1GS/s 11bit SAR-assisted MDAC-free pipeline ADC. A large portion of this chapter has been published in the IEEE Transactions on Circuits and Systems II: Express Briefs [80].

As discussed in Chapter 2, the pipeline architecture is one of the most prevalent for GS/s ADCs as it offers cogent trade-off between conversion rate and resolution [23]. However, its accuracy is largely constrained by the critical MDAC in the pipeline stage, particularly for high speed GS/s functionality. Specifically, the open-loop gain of the residue amplifier in the MDAC needs to be sufficiently high across the entire signal swing range to ensure that the gain error and nonlinearity are less than $\frac{1}{2}$ LSB. In the case of an 11bit ADC, the open-loop gain of the residue amplifier [4, 6] needs to be >72 dB across the signal swing. In the perspective of CMOS fabrication technology scaling, technology scaling that enhances the ADC bandwidth unfortunately undesirably exacerbates the said requirement of the residue amplifier due to lower intrinsic gain and lower supply voltage.

Another consideration for the MDAC is the need for sufficient time to settle to the required accuracy (settling error $<\frac{1}{2}$ LSB). In the case of an 11bit ADC, the MDAC requires $>7.6\tau$ [4, 61], where τ is the settling time constant. In view of the time-consuming operation [23] and timing overheads [7] of conventional pipeline stages, the

settling time available for the MDAC is acutely limited. Put simply, as the conversion rate increases to GS/s, the settling time available for MDAC is often limited, invariably leading to speed limitations [6, 7, 61] if no calibrations are involved.

In view of the aforesaid, there are efforts to exploit the possibility of eliminating the “problematic” MDAC. Specifically, several designs [81, 82] employed SAR ADCs as pipeline stages, and replaced the analog residue amplifiers with dynamic/digital amplifiers. However, the design effort to mitigate accuracy issues arising from the PVT variations of the dynamic amplifiers is very considerable. Another design [83] eliminated the MDAC by means of pipelined sample-and-holds (S/Hs) with cascaded SAR ADCs. However, the requirement of a large number of series-connected S/Hs (i.e., one S/H per bit) operating at the ADC full speed compromises the conversion accuracy and leads to undesirable power and hardware overheads.

In attempts to mitigate the aforesaid issues in the MDAC, various error mitigations have been reported in literature. Although these mitigations can help the ADC achieve relatively high resolution, they unfortunately have their limitations and their efficacy is somewhat contentious. For instance, foreground calibrations [6, 24, 27] often requires pilot signals and may interrupt the normal operation of the ADC. Background calibrations [28-32, 84-86] often use complex back-end digital computation that often requires long convergence time, or needs extra reference ADCs. In short, as the MDAC is one of the primary bottlenecks, our interest herein is to eliminate the MDAC from pipeline ADCs.

This chapter presents the design and realization of a proposed 11bit 1GS/s SAR-assisted pipeline ADC, wherein time-interleaved S/Hs with cascaded SAR ADCs are employed to offer combined advantages of higher accuracy and higher conversion rate

when the process technology scales to finer nodes. Specifically, the adoption of the SAR structure eliminates the need for the ‘problematic’ MDAC in conventional pipeline ADCs, thereby mitigating the accuracy limitation. Further, the operation of the pipeline stages is simplified to a single-iteration successive approximation (SA), thereby enhancing the conversion rate. In addition, 2bit/step conversion scheme is employed to reduce the number of the S/Hs, and the speed requirement of these S/Hs is substantially alleviated by the time-interleaved technique. The required hardware of the channel ADC is reduced by means of the extraction of the quantization for the MSB at the front of the channel ADCs. A prototype ADC is fabricated in 65nm CMOS technology and achieves $\text{SNDR} \geq 56\text{dB}$ and $\text{SFDR} \geq 60\text{dB}$ across 500MHz Nyquist bandwidth at 1GS/s conversion rate with 230mW power dissipation, leading to a competitive Figure of Merit of 449.2 fJ/conv-step when benchmarked with state-of-the-art high-speed high-resolution ADCs [2, 4, 9, 19, 87].

This chapter is organized as follows. Section 3.2 describes the proposed MDAC-free 11bit 1GS/s ADC. Section 3.3 explains the design and realization of the critical building blocks therein. Following this, measurement results are presented in Section 3.4 and conclusions are drawn in Section 3.5.

3.2 PROPOSED MDAC-FREE PIPELINE ADC

This section describes the SAR-assisted MDAC-free 11bit 1GS/s time-interleaved pipeline ADC. The system architecture is first introduced, followed by details of the proposed MDAC-free channel ADC, including its operation, the merits and the design challenges (and shortcoming).

Figure 3.1 System architecture of the overall ADC

Figure 3.1 depicts the system architecture of the proposed 11bit 1GS/s time-interleaved ADC. The front-end S/H (see Section 3.3.2 later) is employed to mitigate the timing mismatch between two channel ADCs. Subsequent to the front-end S/H, a high-precision front-end comparator (see Section 3.3.3 later) is employed to predetermine the MSB. In this manner, the ensuing channel ADCs only need to resolve the subsequent 10 bits instead of the full 11 bits, hence reducing the hardware and power overheads.

3.2.1 Proposed MDAC-free 10bit 500MS/s Channel ADC

Figure 3.2 (a) Conceptual diagram of the pipeline stage, and (b) block diagram of the proposed MDAC-free channel ADC

Figure 3.2 depicts the block diagram of the proposed channel ADC wherein the pipeline stages are realized on the basis of the 2bit/step SAR ADCs [13] with resolutions of 2, 4, 6, 8 and 10 bits for Stage_1 to Stage_5 respectively. Each pipeline stage resolves 2 bits, and collectively 10 bits (2nd MSB to LSB) from all pipeline stages. On the basis of the 2bit/step scheme [13], each pipeline stage comprises three comparators, whose outputs are the 3bit raw D_{out} , and the pertinent 2bit digital output is obtained by decoding the 3bit raw D_{out} using full adders; see Figure 3.2(a). In addition, the 3bit D_{out} controls the CDAC switches in the ensuing stage by means of digital logic gates and flip flops, akin to the (Successive Approximation) SA control logic in the reported design [13]. On

the basis of simulations, the power dissipations of the SAR ADCs in Stage_1 to Stage_5 are 3.79mW, 3.85mW, 4.06mW, 4.33mW, and 5.27mW respectively. The S/Hs are employed herein to sample and hold the input signal, and the sampled signals are multiplexed to the pipeline stages by the switch matrix.

Figure 3.3 Timing diagram of the front-end S/H, the front-end comparator, the 5 S/Hs, and the pipeline stages

The timing diagrams for the front-end S/H, front-end comparator, the 5 S/Hs and the pipeline stages are illustrated in Figure 3.3. The front-end S/H is level triggered while the front-end comparator is rising-edge triggered, and both are clocked at 1GHz. The clock of the front-end comparator is slightly delayed so that the comparator compares the sampled input V_S after the front-end S/H completes its sampling. The 5 S/Hs are time-interleaved and sample V_S from the front-end S/H at 100MS/s with

different phases (ϕ in Figure 3.2). The 5 associated pipeline stages operate concurrently and convert at sampling frequency, $f_s=500\text{MHz}$.

Using Figures. 3.1 to 3.3, the detailed operation of the proposed channel ADC is now described. The front-end S/H samples V_{in} , and the MSB (i.e., MSB1) is predetermined by the front-end comparator, and the remaining 10 bits are resolved by the following channel ADC. In the channel ADC, one of the 5 S/Hs, taking S/H1 as the S/H as the case in point, samples V_S and passes it to Stage_1. With the predetermined MSB, Stage_1 converts the sampled input ($V_{S_sampled}$) and resolves the 2nd and 3rd MSB by performing the aforesaid three signal-processing steps of the proposed conversion algorithm. Subsequently, Stage_1 passes its digital output D_{out1} to Stage_2; D_{out1} comprises 3bit raw output [13] of Stage_1 (see Section 3.3 later). In the meantime, S/H1 buffers $V_{S_sampled}$ to Stage_2. Similarly, with the predetermined MSB and the received D_{out1} , Stage_2 converts $V_{S_sampled}$ and resolves the 4th and 5th MSB, and passes its digital code D_{out2} to Stage_3; D_{out2} comprises the 3bit raw output of Stage_2. Similar signal processing continues until the last two bits are resolved by Stage_5. Note that digital signals (instead of analog residue signals) are transmitted between the pipeline stages.

(I) *Merits of the Channel ADC*

The proposed channel ADC offers three attractive merits. First, as aforementioned, the adoption of the SAR structure as the pipeline stages eliminates the need for the MDAC. This not only simplifies the design and realization of pipeline ADCs, but also largely mitigates the accuracy limitations arising from the MDAC, particularly when the process technology scales to smaller nodes. Second, the operation of the pipeline stages in our channel ADC is simplified to a single-iteration SA, hence leading to higher

conversion rate; conversely, in the conventional pipeline stages, a coarse analog-to-digital conversion and a time-consuming MDAC amplification and settling are required. Third, the digital transmission between the pipeline stages features high noise tolerance, potentially improving the transmission accuracy.

In the perspective of power dissipation, we will now provide some analyses for the comparison between the proposed channel ADC and the conventional pipeline ADC embodying MDAC. For sake of fair comparison, the benchmarked conventional pipeline ADC does not employ any power-saving techniques, e.g., background calibrations [20, 62] or amplifier sharing [88]. The pipeline stages in the conventional pipeline ADC embody consecutive stage resolutions of 2, 2, 2, 2, and 3 along the pipeline chains. The capacitors in the pipeline stages are scaled down proportionally (to the stage resolution), and the size of the amplifiers does not scale (i.e., k is a constant)—this is the best-case assumption in terms of lowest power dissipation for the conventional pipeline ADC.

We will assume the power dissipation of the proposed channel ADC is dominated by the S/Hs because of their large static current, and the preamplifiers in the comparators is negligible despite of the low noise requirement. Similarly, the power dissipation of the convention pipeline ADC is dominated by the MDAC.

On the basis of [57], the dc current I_D required by an amplifier to settle to N -bit resolution can be expressed as,

$$I_D > \frac{1}{2k} \left[\frac{C_{load} f_S}{\beta \alpha} (N+1) \ln 2 \right]^2 \quad (40)$$

where $k = \mu C_{ox} \frac{W}{L}$, C_{load} is the output capacitance, f_s is the sampling rate, β is the feedback factor, and α is the percentage of clock period that is available for the amplifier settling.

As C_{load} is scaled down by $(1/\beta - 1)$ with $\beta = 1/3, 1/3, 1/3$, and $1/4$ along the pipeline chains, we can approximate the ratio of the power dissipation between the proposed ADC (P_{prop}) and the conventional pipeline ADC (P_{conv}) on the basis of eqn.(40) as:

$$\begin{aligned} \frac{P_{prop}}{P_{conv}} &= \frac{5 \times \left(\frac{11}{\alpha_{prop}} \right)^2}{\left(\frac{3}{2\alpha_{conv}} \times 10 \right)^2 + \left(\frac{3}{2\alpha_{conv}} \times 8 \right)^2 + \left(\frac{3}{2\alpha_{conv}} \times 6 \right)^2 + \left(\frac{4}{3\alpha_{conv}} \times 4 \right)^2} \\ &= \left(1.12 \times \frac{\alpha_{conv}}{\alpha_{prop}} \right)^2 \end{aligned} \quad (41)$$

In the case of high-speed high-resolution (e.g., ≥ 10 GS/s and ≥ 10 bit) specifications, the time available for the MDAC in the conventional pipeline ADC is severely limited, e.g. $\alpha_{conv} < 30\%$ [6, 21, 44]. Conversely, in the proposed ADC, more time can be allocated for the S/H settling (e.g., $\alpha_{prop} \geq 50\%$), thanks to the elimination of the MDAC and the simplicity of the stage operation. In view of this, there is a good possibility that the proposed ADC offers potential advantages in terms of power dissipation, i.e., $\alpha_{prop} > 1.67\alpha_{conv}$, hence $P_{prop} < P_{conv}$ on the basis of eqn.(41).

It is worthwhile to note that P_{conv} is larger/worse when the size of the amplifiers scales along the pipeline chains [6, 20, 51, 89], and our ADC architecture potentially offers even more power advantage. Consider the following case in point, if $\alpha_{prop} =$

$1.67\alpha_{conv}$, and the amplifiers in the conventional pipeline ADC scale once (i.e., the size of the amplifiers in the second to the fourth stages is half of the first stage), then $P_{prop} = 0.65P_{conv}$, i.e., a 47% power advantage for the proposed ADC architecture.

In short, our proposed ADC architecture offers speed and accuracy advantages with potentially lower power dissipation (compared to the conventional pipeline architecture embodying MDAC). Although additional S/Hs are needed, the sampling rate of these S/Hs is much lower (e.g., 5 times lower) compared to the conversion rate of the channel ADC. In the context of the overall design, the merits of our channel ADC outweigh the shortcoming, particularly with process technology scaling; these S/Hs can be simply realized using open-loop source followers (see Section 3.2.2 later).

(II) *Design Challenges of the Channel ADC*

Despite the aforesaid merits, the shortcoming of our channel ADC is that the pipeline stages therein do not provide gain to alleviate the accuracy requirement of the ensuing pipeline stages. Consequently, the pipeline stages need to achieve full-resolution accuracy (11bit accuracy in this case). This accuracy requirement entails the need for noise optimization and nonlinearity minimization for all the associated building blocks. Specifically, the noise needs to be lower than the quantization noise of the overall ADC (-75.4dB in this case), and the nonlinearity (e.g., due to gain error or offset) need to be $< \frac{1}{2}\text{LSB}$. Our design to address these challenges is described in Section 3.3 later.

For sake of completeness, note that the S/Hs in the channel ADCs, as in conventional time-interleaved ADCs, suffer from timing and offset mismatches. In our design, the timing mismatch is mitigated by the front-end S/H, and we mitigate the offset mismatch between the S/Hs, hence the mismatch between the two channel ADCs [61],

by adopting a reported off-chip calibration [90] with a pilot dc voltage, where the associated power dissipation is approximately 9.46mW [89]. This power dissipation is largely insignificant in the context of the overall ADC power dissipation (230mW, see Section 3.4 later).

3.3 DESIGN AND REALIZATION OF THE CRITICAL BUILDING BLOCKS

On the basis of the system-level descriptions in Section 3.2, this section describes the design and realization of the pipeline stages, S/Hs and comparators.

3.3.1 Pipeline Stages

Figure 3.4 (a) Block diagram of Stage_2, (b) Circuit realization of the 4bit CDAC, (c)

Output voltage range of the CDAC, and (d) Unit capacitor

The pipeline stages are realized with 2bit/step capacitive-DAC (CDAC) SAR ADCs [13] with increased resolution from the first to the last stages. Bottom-plate sampling technique is employed for all the stages to mitigate the inter-stage gain errors caused by the parasitic capacitance at the top plates of the CDACs [15]. To mitigate the capacitor overheads, split-CDACs [15] were employed for the last three stages; the first two stages do not employ split-CDACs due to their low resolutions. The attenuation capacitors in the split-CADCs for the last three stages are slightly enlarged on the basis of the layout extraction to enhance the CDAC linearity [15]. As the operation of the 5 pipeline stages are similar, and for sake of brevity, only the pipeline Stage_2 is described herein.

Figure 3.4(a) depicts the block diagram of Stage_2 that serves to generate the 3bit raw output (D_{out2}) that serves to control the CDACs in the ensuing stage (see Section 3.1 earlier). As the generations for D_{out2_1} , D_{out2_2} and D_{out2_3} are similar, for sake of brevity, only the generation for D_{out2_3} is described herein.

Table 3.1 Logic mapping in Interface_3 for the proposed Switching Controls

	MSB=1	MSB=0
b3	V_{ref-} if $D_{out1_3} = '1'$; V_{CM} if $D_{out1_3} = '0'$	V_{CM} if $D_{out1_3} = '1'$; V_{ref+} if $D_{out1_3} = '0'$
b2	V_{ref-} if $D_{out1_2} = '1'$; V_{CM} if $D_{out1_2} = '0'$	V_{CM} if $D_{out1_2} = '1'$; V_{ref+} if $D_{out1_2} = '0'$
b1	V_{ref-} if $D_{out1_1} = '1'$; V_{CM} if $D_{out1_1} = '0'$	V_{CM} if $D_{out1_1} = '1'$; V_{ref+} if $D_{out1_1} = '0'$
a3, a2, a1	V_{CM} , V_{CM} , V_{ref+}	V_{CM} , V_{CM} , V_{ref+}

Figure 3.4(b) depicts the circuit realization of the 4-bit CDAC (fully-differential Capacitive DACs) that generates D_{out2_3} ; Table 3.1 tabulates the logic mapping in Interface_3 for the proposed Switching Controls (b3~b1 and a3~a1). The modulus operandi of the proposed conversion algorithm is as follows. First, the predetermined MSB bit is converted to an analog signal by selecting the appropriate set of switching controls (see Table I) at Interface_3. The 3bit D_{out1} (from the preceding Stage_1) is converted to an analog signal at the CDAC by connecting the bottom plates of the three ‘4C’ capacitors (controlled by b3, b2, b1) to the pertinent nodes (V_{CM} , V_{ref+} , and V_{ref-}). Similarly, the pertinent reference is obtained by connecting the bottom plates of the three ‘C’ capacitors (controlled by a3, a2, a1) to their pertinent nodes (V_{CM} , V_{CM} , and V_{ref+}). Note that the said subtraction (described in Section 3.2) for the second step of the proposed conversion algorithm is self-realized when converting D_{out1} and generating the pertinent reference, and the resultant signal (differential V_+ and V_-) are obtained. Finally, the quantization is realized by comparing V_+ and V_- .

The realization of the pipeline stage exhibits an attractive merit attributed to the proposed switching controls. Specifically, because the MSB is largely converted at the digital interface instead of the CDAC, the output swing of the CDAC is 50% of conventional CDACs [71]; our CDAC outputs (V_+ , and V_-) are of the same voltage range (V_{ref-} to V_{ref+}) centered at the common mode voltage (V_{CM}) as depicted in Figure 3.4(c). This is desirable because the reduced output swing ensures that the differential input transistors of the ensuing comparator always operates in saturation region, thereby reducing the potential dynamic offset due to the mismatch between the gate capacitance of the comparator input pairs.

(I) Capacitor Mismatch and KT/C Noise

Following the accuracy requirements of the channel ADC, the nonlinearity arising from the capacitor mismatch in our pipeline stages needs to be minimized (i.e., integral nonlinearity $< \frac{1}{2}\text{LSB}$), and the KT/C noise needs to be $< -75.4\text{dB}$. We will now describe the capacitor mismatch and the KT/C noise in turn.

In our pipeline stages, we use relatively large unit capacitors realized by the Metal-Oxide-Metal fringing structure (M3-M5), as depicted in Figure 3.4(d), and employ four layout techniques to minimize the capacitor mismatch. First, a grounded shielding ring (M1-M6) that encloses the unit capacitor is employed to create a consistent periphery condition for the unit capacitor and to prevent undesirable external noise/distortion coupling. Second, M6 (uppermost metal layer) and M2 (second lowest metal layer) that are vertically far apart from each other are employed for the top- and bottom-plate routings respectively to minimize the parasitic capacitance between the said two routings. Further, the M6 and M2 are routed orthogonally to further reduce the parasitic capacitance, and a grounded M4 layer is employed to isolate their cross-area to reduce the coupling. Third, the common-centroid layout technique is employed to address the fabrication process variation. Lastly, we isolate the capacitors from the rest of the circuitry by adopting both guard rings and BFMOAT—a physical layer to block the P-well implant and to create a resistive path. On the basis of our layout extraction, the CDACs with a 15fF unit capacitor achieve capacitor mismatch of $\sim 0.2\%$, which is sufficient to ensure the maximum variance of the nonlinearity less than $(\frac{1}{2}\text{LSB})^2$ [75].

In the case of $< -75.4\text{dB}$ KT/C noise, the total capacitance of $> 145\text{fF}$ is required for each CDAC. In view of this and of the 15fF unit capacitor required by the capacitor matching, the total capacitance for each CDAC is designed to be 480fF. Note that as the CDACs in Stage_3, Stage_4 and Stage_5 embody the well-established split DAC

structure with an enlarged bridging capacitor [15] to mitigate the capacitor overheads, the total capacitance for each CDAC is the same, i.e., 480fF.

3.3.2 High-linearity S/Hs

The front-end S/H and the five S/Hs in the channel ADC embody similar architecture and modulus operandi. The front-end S/H is required to sample input at 1GS/s whereas, the five S/Hs in the channel ADC sample at 100MS/s, as explained in Section 3.2. Hence, the front-end S/H is the most critical S/H even though its load (one S/H in the channel ADC) is slightly smaller than the load (the pipeline stage) of the S/Hs in the channel ADCs. For the sake of brevity, only the front-end S/H is described in this section. Note that the sampling capacitor of the front-end S/H and the ensuing S/Hs in the channel ADC is designed to be 450fF to obtain low KT/C noise.

Figure 3.5 Block diagram of the front-end S/H

Figure 3.5 depicts the block diagram of the front-end S/H, largely comprising bootstrapped switch and high-linearity buffers (N -type source followers). The circuit realizations of the bootstrapped switch and the high-linearity buffer are now described in turn.

(I) *Bootstrapped Switch*

The basic structure of the bootstrapped switch (bootstrap and the switches M1 and M2 in Figure 3.5) is realized by adopting a well-established bootstrap technique [91], whose linearity is largely ensured by keeping the on-resistance of M1 and M2 largely constant during sampling.

Despite the said bootstrap technique, substantial nonlinearity can also arise from signal feedthrough and clock feedthrough at the switches of M1 and M2. The signal feedthrough can be mitigated by cancelling it with a 180-degree phase-shifted replica [22]. In our design, the cross-coupled M3 and M4 serve to introduce the said replica. The clock feedthrough, on the other hand, cannot be easily cancelled. In our design, we mitigate the clock feedthrough by equalizing it at both differential signal paths ($V_{T/H+}$, $V_{T/H-}$). In this fashion, the clock feedthrough is largely a common-mode noise that is largely immune in fully-differential operation. This equalization is realized by employing cross-coupled M5 and M6 in Fig 5. Note that the gates (instead of drain or source) of M5 and M6 are connected to the signal paths to avoid the potential charge injection into the signal paths. Specifically, by appropriately sizing M5 and M6 (approximately to half of transistor M1 or M2), the gate capacitance of M5 or M6 is equalized to C_{GD} (gate-to-drain capacitance of M1 or M2). Hence, the charge (Q_p , Q_n) due to clock feedthrough at the differential signal paths is equalized, i.e., $Q_p = Q_n = C_{GD} * (V_{G+} + V_{G-})$, and becomes a common-mode noise. Consequently, the effect of clock feedthrough is, to a first order, cancelled by the fully-differential operation.

Figure 3.6 Simulated output ($V_{T/H+} - V_{T/H-}$) of the bootstrapped switch

Figure 3.6 depicts the simulated output ($V_{T/H+} - V_{T/H-}$) of the bootstrapped switch with (solid red) and without (dotted blue) the proposed mitigation of clock feedthrough technique; the dashed black curve is the input signal that serves as the reference for comparison. As expected, the sampling error due to clock feedthrough increases as the input magnitude increases since the gate of the switch experiences increased voltage drop at high-level inputs. The red curve depicts that the clock feedthrough is heavily mitigated by means of our proposed mitigation technique.

Figure 3.7 Simulated Spectra results (a) without, and (b) with the proposed clock feedthrough mitigation

Figure 3.7(a) and (b) respectively depict the simulated spectra results of the bootstrapped switch without and with the proposed mitigation of the clock feedthrough. The switching speed is 1GHz with ~500MHz input signal. It can be observed that the SFDR and THD are primarily limited by the 3rd harmonic distortion without clock

feedthrough mitigation. With the proposed mitigation, the 3rd harmonic distortion is substantially reduced, and the SFDR and THD are improved by 21.7dB and 16.4dB respectively. The resulting performance is sufficient for the stipulated ADC specifications.

(II) *High-linearity Buffer*

Figure 3.8 Unity-gain buffer

Figure 3.8 depicts the unity-gain buffer employed in the front-end S/Hs. The buffer is realized on the basis of a source follower (M1 and the PMOS Current Source) and features wide bandwidth. As the open-loop source follower typically suffers from poor linearity and relatively large gain error, three means are adopted in our unity-gain buffer. First, an additional N-type source follower (M2) is employed to keep the drain-source voltage of M1 constant [61]. Second, the triple well layout technique is adopted for M2 to eliminate the body effect therein. Third, high threshold-voltage transistors

(hvt in Figure 3.8) are adopted for M1 and M2, and low threshold-voltage transistors for the other transistors. The low threshold-voltage transistors with smaller parasitic capacitance serve to ensure wide bandwidth, and the high threshold-voltage transistors serve to ensure the required gain of the buffer. This is because high threshold-voltage transistors embody high intrinsic gain (g_m/g_{ds}). Specifically, we can show (not shown in details herein for sake of brevity) that the buffer must fulfill $(g_{m1}g_{m2})/(g_{ds1}g_{ds2}) > 2^{12}$ in order to obtain gain error of $< \frac{1}{2}\text{LSB}$. On the basis of the said three means, the proposed buffer achieves gain of $> -2.75\text{mdB}$ with bandwidth up to 3.5 GHz for full-scale input signal, which is sufficient for the requirements of 11bit and 1GS/s.

(a)

(b)

Figure 3.9 (a) Simulated THD, and (b) voltage gain of the front-end S/H

To illustrate the efficacy of the overall front-end S/H (including the bootstrapped switch and the high-linearity buffer), Figure 3.9(a) and (b) depict the simulated total harmonic distortion (THD) and the voltage gain of the front-end S/H as a function of the input frequency at a sampling rate of 1GS/s. The THD remains below -75dB for input frequency $\leq 500\text{MHz}$ and the voltage gain is $\geq -2.8\text{m dB}$ for input frequency up to 3.2GHz. Both parameters are hence sufficient for 11bit 1GS/s.

Note that the THD of the front-end S/H slightly degrades with the increment of the input frequency. This is largely because the adjacent samples at high input frequency often exhibits large voltage difference. This results in increased kickback noise [22, 61] and increased settling error due to the inter-sample interference [4]. Nonetheless, in the perspective of the system design, the front-end S/H substantially improves the ADC performance as it removes the significant error due to the timing mismatch between the channel ADCs.

In addition, on the basis of the Monte-Carlo simulations, the 3σ gain and offset variations of the S/H are -4.646m dB/-0.854m dB and -4.453mV/4.661mV respectively. For completeness, the 3σ gain and offset mismatches among the S/Hs in the channel ADC are $\pm 0.037\%$ and -7.033mV/7.265mV respectively.

3.3.3 Comparators

Figure 3.10 Block diagram of the proposed comparator

Figure 3.10 depicts the block diagram of the proposed comparator that serves to predetermine the MSB at the front-end and serve as the quantizer in each pipeline stage. The comparator comprises two Preamplifiers, one Dynamic Comparator, and circuits for offset calibration. The preamplifiers serve to amplify the input difference for the ensuing dynamic comparator to identify small input difference at high speed.

The noise of the comparator needs to be minimized so that the input-referred noise of the comparator is 78.6dB below the signal power. In the proposed comparator,

Preamplifier 1 is the dominating noise source, because the noise contributed by the rest circuitry is largely attenuated by Preamplifier 1 and/or Preamplifier 2. It is known [92] that the input-referred noise of Preamplifier 1 can be minimized by increasing the transconductance (G_m) of the input transistors, and/or by decreasing the noise conductance at the output of Preamplifier 1. We adopt the former as decreasing the conductance undesirably reduces the bandwidth of Preamplifier 1. The penalty is slightly increased power dissipation. On the basis of the Spectre noise simulation, the input-referred noise of our comparator with $G_m = 3.3\text{mS}$ is below -78.6dB .

In addition to the said noise optimization, the offset of the comparator also needs to be minimized, i.e., to $< \frac{1}{2}\text{LSB}$. The offset in our comparator is largely eliminated by the proposed calibration embodying a 7b digital Counter, a 7b Current-Steering DAC and a Current Source realized by two cascoded transistors (M1 and M2). The operation of the calibration is now described. First, the comparator inputs are shorted to V_{CM} . Second, the output of the comparator is pre-set to '1' by means of purposely introducing a positive offset at V_N (by the Current Source in Figure 3.10). Lastly, the Current-Steering DAC keeps the voltage at V_P pulled-down until the output of the comparator switches to '0'. In this manner, the comparator offset is largely eliminated.

The Current-Steering DAC is the key building block of the calibration circuits because it not only ascertains the calibration range (the maximum offset that can be calibrated), but also determines the calibration resolution (the minimum offset that can be achieved). We design the Current-Steering DAC (Figure 3.10) to be 7 bits so that our calibration is able to eliminate the offset up to $\pm 18\text{mV}$, and achieve the minimum resultant offset of 0.28mV ($< \frac{1}{2}\text{LSB}$ after calibration). The calibration range of $\pm 18\text{mV}$ is sufficient because, the 3σ offset of the comparator without calibration (from simulations) is $\pm 13\text{mV}$.

3.4 EXPERIMENTAL RESULTS

Figure 3.11 Microphotograph of the ADC prototype

Figure 3.11 depicts the microphotograph of the proposed ADC prototype realized in 65nm CMOS, and the chip size is $2.4\text{mm} \times 1.5\text{mm}$. The Pipeline Stages (mostly CDACs) occupy most of the silicon area (approximately 50%), followed by the S/Hs and the bootstrapped switches. The Clock Generator and front-end S/H are placed in the middle of the IC to facilitate the distribution of matched signals to the two channel ADCs. To minimize parasitic impedance, the prototype is directly bonded onto the test board.

The measure setup for our ADC prototype is as follows. The power supplies (including both digital power supply and analog power supply) are provided by high-performance LDOs that are surface-mounted on the PCB. The reference of the ADC was generated externally by a high-accuracy reference generator (Agilent B2902A). Further, large decoupling capacitors for power supplies and reference voltages are employed on board to decouple noise and bypass transient current therein. The input

signal of our ADC is generated by a signal generator, and subsequently converted to fully differential signals by a high-accuracy balun (i.e., BALH-0003SMG) on board. The digital outputs are collected by a logic analyzer without decimation, and subsequently analyzed by means of Matlab on PC.

The ADC operates from a dual power supply of 1.2V/2V and has full-scale input of $1.2V_{PP,diff}$. The measured total power dissipation at 1GS/s is 230mW, whose breakdown is 150mW for S/Hs, 28.8mW for comparators, 7.2mW for reference generation and the rest for digital logic. As expected, the S/Hs dominate the power dissipation because of the 2V supply voltage and the relatively large static current.

(a)

(b)

Figure 3.12 Measured (a) DNL, and (b) INL

Figure 3.12 depicts the measured differential nonlinearity (DNL) and integrated nonlinearity (INL) at 1 GS/s sampling rate. It can be observed that the DNL is within $+0.8\text{LSB}/-0.7\text{LSB}$ whereas the INL is within $\pm 2\text{LSB}$. The measured DNL and INL satisfy the requirement of the proposed ADC for the intended wideband direct sampling RF receivers.

Figure 3.13 Measured FFT spectrum (16384 points) at 1GS/s with 475.2MHz input;
HD2, ..., HD5: 2nd Harmonic, ..., 5th Harmonic respectively

Figure 3.13 depicts the measured spectrum of the ADC prototype output at the sampling frequency of 1GS/s with a $1.2V_{P-P}$ full-scale input signal at 475.2MHz. The measured SNDR and SFDR are 55.9dB and 60.05dB respectively. The HD3 (3rd harmonic) is the dominant distortion component, and largely introduced by the sampling/resampling settling error and the nonlinearity of the unity-gain buffers in the front-end S/H and the S/Hs in the channel ADCs [61]. The other nonlinearities are negligible ($\leq -70\text{dB}$) attributed to the elimination of the NADC, the simplification of the pipeline stages, the adoption of the front-end S/H, and the minimization for the noise and nonlinearity of the individual building blocks.

Figure 3.14 Measured SNDR and SFDR versus input frequency at 1GS/s sampling frequency

Figure 3.14 depicts the measured SNDR and SFDR versus input frequency at 1GS/s sampling frequency. The proposed ADC achieves $\text{SNDR} \geq 55.9\text{dB}$ (equivalent to 9 ENOB) up to 475MHz. The peak SNDR is 59.1dB, equivalent to 9.52 ENOB. The SFDR remains above 60.5dB up to 475MHz, and exhibits a peak value of 66dB at low frequency.

Figure 3.15 Measured SNDR/ENOB versus sampling frequency

Figure 3.15 depicts the measured SNDR/ENOB versus sampling frequency. The measurement is performed with normalized input frequency (Input frequency/Sampling frequency=0.475). It can be observed that the SNDR remains largely constant (< 1dB degradation) with the sampling frequency up to 1GS/s, and as expected, degrades somewhat rapidly at higher sampling frequencies (> 1GS/s). The rapid degradation is attributed largely to the increased nonlinearity (distortion) in the front-end S/H and the increased settling error in the ensuing pipeline stages. The jitter largely contributes to the noise instead of distortions.

Table 3.2 Performance Summary and Benchmark against State-of-the-Art ADCs with Similar Specifications

Reference	This work	JSSC'12 [2]	JSSC'13 [4]	ISSCC'11 [87]	VLSI'16 [10]	ISSCC'17 [8]	ISSCC'15 [93]
Technology (nm)	CMOS 65	CMOS 40	CMOS 40	BiCMOS 180	CMOS 28	FinFET 14	CMOS 28
Architecture	Pipelined/SAR	Pipeline	Pipeline	Pipeline	Pipeline	Pipelined/SAR	Pipelined/SAR
Supply voltage (V)	1/2	2.5	0.9/1.5/1.95	1.8/3.3	0.9/1.8/2.5	0.95	1
Conversion rate (GS/s)	1	3	2.1	1	5	1.5	5
Resolution (bit)	11	12	12	12	14	10	10
Area (mm ²) excluding pads	2.5	0.4	0.5	2.4	14.4	0.0016	0.35
Worst SNDR (dB)	56	51	50	59	52	50	46.1
Best SNDR (dB)	59.1	57.5	52	62	63	51	57
Power (mW)	230	500	280	575	2300	6.92	150
FoM _{Walden} (fJ/step)	449.2	574.9	516.1	789.6	1409.8	17.7	192.5
FoM _{Schreier} (dB)	149.4	145.8	145.7	148.4	142.4	160.3	148.1

Table 3.2 tabulates the key parameters of the proposed ADC prototype (realized in 65nm CMOS process), and benchmark against state-of-the-art ADCs with similar specifications. The primary features of the prototype ADC include SNDR ≥ 55.9 dB across 500MHz Nyquist bandwidth at 1 GS/s sampling rate with 230mW power dissipation from a dual power supply of 1.2V/2V. The figure-of-merit (FoM, 449.2fJ/conv-step) of our MDAC-free design, either based on Walden FoM_{Walden} or Schreier FoM_{Schreier}, is competitive amongst designs employing similar technology nodes; for sake of fair comparison, both FoMs are calculated based on the worst SNDR within the Nyquist bandwidth. As explained in Section 3.2 earlier, the proposed architecture could potentially achieve better performance with finer technology nodes. Note that for sake of fair comparison, the SNDR of the ADCs tabulated in Table 3.2 is the minimum SNDR achieved by the ADCs within their Nyquist bandwidth, and the ensuing FoM ($\frac{Power}{2^{ENOB} \times f_s}$) is calculated based on the minimum SNDR/ENOB.

3.5 CONCLUSIONS

A 1GS/s 11bit SAR-assisted pipeline ADC has been reported. The proposed ADC combined the speed advantage of the pipeline algorithm and the structural simplicity of the SAR ADC. Consequently, the MDAC was eliminated, and both the structure and the operation of the pipeline stages were simplified. Measurements on the prototype ADC depicted an SNDR ≥ 56 dB across 500MHz Nyquist input frequency at 1GS/s conversion rate. When benchmarked against state-of-the-art pipeline ADCs, the proposed MDAC-free ADC featured a competitive FoM. Attributed to the elimination of the MDAC and the simplification of the pipeline stages, the performance of the proposed ADC could be substantially enhanced when implemented using finer technology nodes.

Chapter 4 A 400MS/S 10BIT 2BIT/STEP SAR ADC

4.1 INTRODUCTION

This chapter delineates the design, monolithic realization, and measurements (and verification) of our proposed 400MS/s 10bit 2bit/step SAR ADC. A large portion of this chapter has been accepted for publication as a Regular Paper in the IEEE Transactions on Very Large Scale Integration Systems [94].

As discussed in Chapter 2, the SAR ADC is increasingly prevalent for high-speed and medium-to-high resolution applications for three reasons. First, unlike the pipeline ADC that embodies multiple critical analog elements, the SAR ADC typically and largely comprises digital elements, hence leading to simplicity in design and realization [11, 38]. Second, due to the digital-like operation, the SAR ADC dissipates mainly dynamic power, hence often exhibiting higher energy efficiency. Third, the SAR ADC is more compatible with technology scaling—particularly, the conversion rate of the SAR ADC increases with finer technology nodes, yet its accuracy is arguably unaffected by the increasingly inferior transistor linearity.

Despite the aforesaid advantages, the conversion rate of the SAR ADC is fundamentally constrained by the SA conversion algorithm. A well-known approach to enhance the conversion rate is to employ the 2bit/step scheme that in principle improves the conversion rate by approximately 2 times. However, state-of-the-art 2bit/step schemes [12, 13, 39, 76, 78, 79] often require the generation of 2 reference voltages, leading to undesirable hardware and power overheads. The reported 2bit/step SAR ADC [13] required three fully-differential CDACs that are realized by six capacitor arrays. Consequently, this realization results in undesirable excessive hardware and power

overheads, leading to a large ADC input loading. Another 2bit/step ADC [39] replaced the aforementioned three CDACs by a resistive DAC. However, the resistive DAC involves a myriad of switches and complex routing, which limits its conversion rate. Another 2bit/step ADC [76, 79] required only two differential CDACs (four capacitor arrays), hence leading to smaller input loading and less hardware and power overheads compared to [13]. However, additional efforts are needed to mitigate the accuracy issues arising from its unsymmetrical architecture and undesirable top-plate sampling, hence leading to increased design difficulty and hardware overheads.

This chapter presents the design and realization of a 2bit/step 10bit 400MS/s SAR ADC that requires only 1 reference voltage. By means of our proposed 2bit/step SAR conversion scheme, our proposed ADC offers three attractive features. First, only three capacitor arrays are required in our ADC—the least number of capacitor arrays amongst reported CDAC-based 2bit/step SAR ADCs, leading to higher energy efficiency. Second, only two out of the said three capacitor arrays serve to sample the input signal, hence a smaller input loading. Third, the proposed ADC features an inherently symmetrical architecture with highly-matched interconnections, leading to enhanced system matching and higher accuracy. Further, for our proposed ADC, we propose a high-speed high-accuracy dynamic comparator and a high-speed SA control logic to obtain high conversion rate. A prototype ADC is fabricated in 65nm bulk CMOS technology and achieves SNDR >52dB and SFDR >63.7dB across 200MHz Nyquist bandwidth, while dissipating 5.61mW power. When benchmarked with state-of-the-art 2bit/step SAR ADCs [12, 13, 76, 78], our ADC features the most competitive Figure-of-Merit of 43fJ/conv.step.

This chapter is organized as follows. Section 4.2 describes the system-level design of our proposed 2bit/step SAR ADC. Section 4.3 describes the circuit implementation,

including the design of the critical building blocks. Following this, measurement results are presented in Section 4.4 and conclusions are drawn in Section 4.5.

4.2 PROPOSED 2BIT/STEP SAR ADC

This section describes the system-level design of the proposed 400MS/s 10bit SAR ADC, including the modulus operandi of the 2bit/step conversion, and the design considerations for high speed and accuracy.

Figure 4.1 System architecture of the proposed ADC

Figure 4.1 depicts the system architecture of the ADC design. It comprises one fully-differential CDAC with two capacitor arrays (Signal_CDAC₊ and Signal_CDAC₋) and one single-ended CDAC with one capacitor array (Ref_CDAC). The former two arrays serve to sample the fully-differential input signals (V_{in-} and V_{in+}), and the latter array serves to generate the pertinent reference voltage (V_{TH}). The generated V_{sig+} , V_{sig-} and V_{TH} are compared at the three comparators, and subsequently decoded into a 2bit

digital output. In this fashion, the proposed architecture is symmetrical with balanced and matched interconnections, particularly between the CDACs and the comparators, thereby potentially leading to higher accuracy, yet with design simplicity. It is worthwhile to note that the input signal power is not reduced despite of the single-ended Ref_CDAC.

4.2.1 The Proposed 2bit/step Conversion Scheme

Figure 4.2 Proposed 2bit/step conversion scheme

Figure 4.2 depicts the modulus operandi of our proposed 2bit/step conversion scheme. Three comparisons are involved to resolve 2 bits in one conversion iteration. The first bit, akin to conventional single-bit/step SAR conversions, is obtained by directly comparing V_{sig+} and V_{sig-} . On the basis of the obtained first bit, the second bit is thereafter resolved by comparing V_{TH} with either V_{sig+} or V_{sig-} . Note that the said three comparisons are performed simultaneously (vis-à-vis sequentially) to enhance the conversion rate.

The proposed 2bit/step conversion scheme offers three attractive features. First, as aforementioned, the proposed scheme requires less hardware and power. This is primarily because our scheme needs only one reference, i.e., V_{TH} in Figure 4.2, (instead of two in state-of-the-art 2bit/step SAR ADCs [12, 13, 76, 78, 79]) in each conversion iteration, hence requiring only one single-ended CDAC for reference generation (Ref_CDAC); a saving of at least one capacitor array without reducing the input signal power. Consequently, our ADC is realized with only three capacitor arrays instead of at least four in other reported CDAC-based 2bit/step SAR ADCs [12, 13, 76, 78, 79]. Second, the proposed scheme requires only one differential CDAC (i.e., Signal_CDAC₊ and Signal_CDAC₋) to sample the input signal, leading to low input loading (as in [76, 79] that is akin to the conventional single-bit/step SAR ADC), and is approximately half of conventional 2bit/step SAR ADCs. This merit substantially alleviates the driving requirement of the power-hungry input buffer of communication systems. Third, as aforementioned, the proposed scheme enables the symmetrical and well-matched system architecture. This serves to minimize the potential mismatches between the CDAC outputs due to the unbalanced path routings [76, 79, 95], thereby enhancing the conversion accuracy.

The operation of the proposed 2bit/step conversion comprises one input sampling/reset phase (P0) and five conversion iterations (P1 to P5) with each iteration resolving 2 bits. As the operations in P1 - P5 are similar, for sake of brevity, the following explanation will only delineate P0 and P1.

Figure 4.3(a) and (b) depict the signal processing of P0 and P1 respectively. During P0, V_{in+} and V_{in-} are sampled to the bottom plates of the Signal_CDAC₊ and Signal_CDAC₋ respectively, and the top plates are reset to the common-mode voltage (V_{CM}); the complete CDAC is explained in Section 4.31 later. At the same time, the

Ref_CDAC is reset by means of connecting the bottom plates to $(-v_{ref} + V_{CM})$ and connecting the top plates to V_{CM} . Note that $(\pm v_{ref} + V_{CM})$ are the two reference rails of the ADC.

Figure 4.3 Signal processing of (a) P0, and (b) P1

During P1 (see Figure 4.3(b)), $V_{sig+_{P1}}$ and $V_{sig-_{P1}}$ are generated by transferring the sampled V_{in+} and V_{in-} (at the bottom plates in P0) to the top plates. This is achieved by means of disconnecting the top plates from V_{CM} , and switching the bottom plates to the pertinent reference nodes. In this manner, $V_{sig+_{P1}} = V_{in+}$ and $V_{sig-_{P1}} = V_{in-}$. At the same time, the pertinent reference voltage ($V_{TH_{P1}} = \frac{1}{2}V_{ref} + V_{CM}$) is generated at Ref_CDAC. Subsequently, the obtained $V_{sig+_{P1}}$, $V_{sig-_{P1}}$ and $V_{TH_{P1}}$ are compared (see Figure 4.1 and 4.2) and, on the basis of the conversion scheme in Figure 4.2, decoded into the MSB (B_9) and the 2nd MSB (B_8); Table 4.1 tabulates the logic mapping for the decoding.

Table 4.1 Logic mapping for the decoding

Input			Output	
D _{cmp_1}	D _{cmp_2}	D _{cmp_3}	B ₉	B ₈
1	0	0	1	1
1	1	0	1	0
0	1	0	0	1
0	1	1	0	0

During P2, $V_{sig+_{P2}}$ and $V_{sig-_{P2}}$ are generated at the differential CDAC on the basis of $V_{sig+_{P1}}$, $V_{sig-_{P1}}$, and the resolved B_9 , B_8 . Meanwhile, a new reference ($V_{TH_{P2}}$) is generated at the Ref_CDAC. Subsequently, B_7 and B_6 are resolved. A similar conversion process is repeated for P3 - P5.

Table 4.2 CDAC outputs for P0 to P5

	Signal_CDAC ₊ Output	Ref_CDAC Output
P0	V_{CM}	V_{CM}
P1	$V_{Sig+_{P1}} = V_{in+}$	$V_{TH_{P1}} = \frac{1}{2}v_{ref} + V_{CM}$
P2	$V_{Sig+_{P2}} = (V_{Sig+_{P1}} + v_{ref}) - B_9 * v_{ref} - B_8 * \frac{1}{2}v_{ref} - \frac{1}{4}v_{ref}$	$V_{TH_{P2}} = \frac{1}{8}v_{ref} + V_{CM}$
P3	$V_{Sig+_{P3}} = (V_{Sig+_{P2}} + \frac{1}{4}v_{ref}) - B_7 * \frac{1}{4}v_{ref} - B_6 * \frac{1}{8}v_{ref} - \frac{1}{16}v_{ref}$	$V_{TH_{P3}} = \frac{1}{32}v_{ref} + V_{CM}$
P4	$V_{Sig+_{P4}} = (V_{Sig+_{P3}} + \frac{1}{16}v_{ref}) - B_5 * \frac{1}{16}v_{ref} - B_4 * \frac{1}{32}v_{ref} - \frac{1}{64}v_{ref}$	$V_{TH_{P4}} = \frac{1}{128}v_{ref} + V_{CM}$
P5	$V_{Sig+_{P5}} = (V_{Sig+_{P4}} + \frac{1}{64}v_{ref}) - B_3 * \frac{1}{64}v_{ref} - B_2 * \frac{1}{128}v_{ref} - \frac{1}{256}v_{ref}$	$V_{TH_{P5}} = \frac{1}{512}v_{ref} + V_{CM}$

Table 4.2 tabulates the CDAC outputs for P0 to P5; note that, for sake of brevity, only the outputs of the Signal_CDAC₊ and Ref_CDAC are tabulated.

Figure 4.4 depicts an exemplar conversion encompassing phases P0 to P5 for an input weighted approximately 850LSB (Least Significant Bit). The solid (red), dashed (blue), and dotted (purple) lines represent V_{TH} , V_{sig+} and V_{sig-} respectively, and their respective values in P0 - P5 are obtained on the basis of Table 4.2. It can be seen that the resolved digital output, ‘1101010010’, is equivalent to the applied analog input (850 LSBs).

Figure 4.4 An exemplar conversion for an input weighted approximately 850LSB

4.2.2 Conversion Rate and Accuracy

On the basis of the proposed 2bit/step conversion scheme delineated in Section 4.21, this section investigates the speed and accuracy requirements, and serves as a preamble for the circuit realization in Section 4.3.

(I) Conversion Rate

The conversion rate of our ADC is ascertained by the speed of the aforesaid conversion iterations (i.e., P1 to P5). Specifically, for the targeted 400MS/s, each iteration needs to be completed at 2.4GHz, or within 416ps.

Figure 4.5 Operational diagram of the conversion iteration

Figure 4.5 depicts the operational diagram of the conversion iteration that largely comprises four signal processing segments (from t_1 to t_4), where $(t_1 + t_2 + t_3 + t_4) = 416\text{ps}$. Amongst the four segments, the CDAC settling (t_2) is the most critical. Conventionally, the time budget for (t_1+t_2) is limited to half clock period [76, 96], i.e., 208ps. To achieve 10bit accuracy, t_2 needs to be $\geq 6.9\tau$ (time constant of the CDAC), which in turn dissipates excessive power. To alleviate this, we prolong the time budget for (t_1+t_2) by means of shortening $(t_3 + t_4)$. Specifically, t_{delay} of $\sim 50\text{ps}$ is introduced for CLK_{cmp} ; see Figure 4.5. In view of this and considering the 3σ variations of 4ps for the t_{delay} (on the basis of Monte-Carlo simulations), we allocate the time budget for (t_1+t_2) and $(t_3 + t_4)$ to be 254ps and 154ps respectively. The designs to address these time budgets will be described in Section 4.3 later.

(II) Conversion Accuracy

The four primary factors that degrade the conversion accuracy are the kT/C noise of the CDACs, comparator kickback noise, comparator offset, and capacitor mismatch in the CDACs. The first two factors can be designed to be $<-65\text{dB}$ (ADC quantization noise) by means of the appropriate circuit realization (see Section 4.3 later). The last two factors will now be investigated.

Figure 4.6 Simplified block diagram for the generation of D_{cmp_2}

Figure 4.6 depicts the simplified block diagram for the generation of D_{cmp_2} ; note that the analysis herein can similarly be applied to D_{cmp_1} and D_{cmp_3} . In Figure 4.6, V_{OS} denotes the comparator offset, C_{total_ideal} denotes the ideal total capacitance for each CDAC, and C_{P1} and C_{P2} are the parasitic capacitance at the outputs of the Signal_CDAC₊ and Ref_CDAC respectively. In view of the aforesaid symmetrical system architecture (see Figure 4.1), we can ascertain that $C_{P1} = C_{P2}$, and easily derive the comparison function ($V_{TH} - V_{sig+}$) as

$$V_{TH} - V_{sig+} = \frac{C_{total_ideal}}{C_{total_ideal} + C_{P1,2}} \left[V_{in+} - V_{ref-} - \frac{C_b - C_a}{C_{total_ideal}} (V_{ref+} - V_{ref-}) - \frac{C_{total_ideal} + C_{P1,2}}{C_{total_ideal}} V_{OS} \right] \quad (42)$$

where C_a and C_b are the equivalent capacitors connected to the negative reference (V_{ref-}) in Signal_CDAC₊ and to the positive reference (V_{ref+}) in Ref_CDAC respectively.

On the basis of eqn.(42), three observations can be made. First, V_{OS} needs to be

$$< \left(\frac{C_{total_ideal}}{C_{total_ideal} + C_{P1,2}} \right) \times \frac{1}{2} LSB \text{ to ascertain the associated input-referred error to } < \frac{1}{2} LSB. \text{ In}$$

our design, $C_{total_ideal} = 480\text{fF}$ and $C_{P1,2} = 38\text{fF}$, leading to a V_{OS} requirement of $< 0.46\text{LSB}$. Second, the variation of $\left(\frac{C_b - C_a}{C_{total_ideal}} \right)$ needs to be minimized. Since C_a and C_b are constructed by identical unit capacitors, these unit capacitors need to achieve a standard deviation of 0.28% or less [71, 97]. Third, the effect of $C_{P1,2}$ on the gain of the comparison is negligible as it does not affect the polarity of the function. Our designs to address the aforesaid accuracy requirements will be described in the ensuing section.

One design consideration is the common-mode variation of the input signal. Specifically, when the common-mode voltage of the input signal varies from the ADC common mode, nonlinearities are resulted. We will now analyze the impact of the input common mode variation on the performance of our ADC, particularly on the generation of B_9 (MSB) and B_8 (2nd MSB); similar analysis can be applied for the generation of B_7 - B_0 .

Figure 4.7(a) and (b) depict the generation of B_9 and B_8 and the pertinent ADC transfer characteristic without and with input common mode variation respectively. A negative variation is taken as the case in point.

For the generation of B_9 , the input common mode variation has no impact, and the analog signal range corresponding to $B_9 = 1$ and $B_9 = 0$ are unaffected. This is because B_9 is obtained simply by means of directly comparing the fully differential input signal as depicted in Figure 4.7.

For the generation of B_8 , the impact imposed by the input common mode variation depends on the value of B_9 . Specifically, when $B_9 = 1$, the analog signal range

corresponding to $B_8 = 1$ is enlarged whereas the signal range for $B_8 = 0$ is reduced. On the other hand, when $B_9 = 0$, the analog signal range for $B_8 = 0$ is enlarged whereas the range of $B_8 = 1$ is reduced. Consequent to the overall ADC transfer characteristic, nonlinearities result as depicted in Figure 4.7(b).

Figure 4.7 Generation of B_9 and B_8 and the resulting ADC transfer characteristic (a) without, and (b) with input common mode variation

Put simply, the input common mode variation does not affect the generation of B_9 , B_7 , B_5 , B_3 , and B_1 , but will introduce errors to B_8 , B_6 , B_4 , B_2 , and B_0 , thereby resulting

in nonlinearities to overall the ADC performance. To circumvent this issue, the input signal for our design was ac coupled, and its common mode voltage was reset to the common mode of the ADC.

It is worthwhile to note that the input common-mode voltages for Cmp_2 and Cmp_3 in Figure 4.1 vary in different conversion iterations, hence leading to offset variations. However, these offset variations are largely mitigated by ascertaining the input transistors operate in the favorable strong inversion region [98]; see more details in Section 4.3.2 later.

4.3 CIRCUIT IMPLEMENTATION

On the basis of the system-level design in Section 4.2, this section will describe the design and realization of three critical circuits: the CDAC, the comparator, and the SA ctrl (Successive Approximation control) logic.

4.3.1 Signal_CDAC₊ and Ref_CDAC

Figure 4.8(a) and (b) depict the circuit realizations of Signal_CDAC₊ and Ref_CDAC respectively; for sake of illustration, Signal_CDAC₋ is not shown. They are realized by means of similar structures with binary-weighted capacitors. A bridging capacitor (C_B) is adopted to reduce the total capacitance, yet without compromising the size of the unit capacitor (C_u).

Figure 4.8 Circuit realizations of (a) Signal_CDAC+, and (b) Ref_CDAC

Analytically, $C_B = 32/31 C_u$ to ensure the binary increment across its two sides. In practice, however, the parasitic capacitance (C_{P_LSB}) at the left side of C_B slightly reduces the weight of the LSB capacitor sub-array, and possibly introduces an error to the binary increment. We mitigate this issue by slightly adjusting C_B [15] as

$$C_B \approx \frac{C_{total_LSB} + C_{P_LSB}}{C_{total_LSB} - C_u} \times C_u \quad (43)$$

where C_{total_LSB} is the total capacitance of the LSB capacitor sub-array.

C_{P_LSB} in the CDAC is estimated to be 38fF based on layout extraction, leading to the adjusted $C_B = 16.71\text{fF}$ (instead of $32/31 C_u = 15.48\text{fF}$). It has been shown [15] that the adjusted C_B can tolerate up to 5% variation of C_{P_LSB} with only 1dB SNDR degradation, which is sufficient to accommodate the process variations.

Figure 4.9 Layout designs for (a) the unit capacitor, and (b) Signal_CDAC₊, Signal_CDAC₋, and Ref_CDAC

As mentioned earlier in Section 4.2.2, the capacitor mismatch both in and between the CDACs needs to be $<0.28\%$. In our CDACs, we realize the unit capacitor (C_u) by the Metal-Oxide-Metal fringing structure (M3-M5), as depicted in Figure 4.9(a), and

employ the following four layout techniques to minimize the capacitor mismatch. First, a grounded shielding ring (M1-M6) that encloses the unit capacitor is employed to create a consistent periphery condition for the unit capacitor and to prevent undesirable external noise/distortion coupling. Second, M6 (uppermost metal layer) and M2 (second lowest metal layer) that are vertically far apart from each other are employed for the top- and bottom-plate routings respectively to minimize the parasitic capacitance between the said two routings. Further, the M6 and M2 are routed orthogonally, and a grounded M4 layer is employed to isolate their cross-areas to further minimize the parasitic capacitance.

Third, the common-centroid layout technique is employed to address the fabrication process variations both in and between the CDACs. Figure 4.9(b) depicts the common-centroid layout design for Signal_CDAC₊ (vertically hatched), Signal_CDAC₋ (horizontally hatched) and Ref_CDAC (dotted). In accordance with the associated schematic design depicted in Figure 4.8, ‘L9’ to ‘L0’ represent the locations of the unit capacitors for C_9 to C_0 respectively. ‘LB’ and ‘LC’ represent the locations of the C_B and the complementary capacitor (C_C) respectively. Forth, we isolate the capacitors from other circuitries by adopting both guard rings and BFMOAT—a physical layer to block the P-well implant and to create a resistive path. On the basis of our layout extraction, the CDACs with 15fF unit capacitor achieve a capacitor mismatch of approximately 0.18%, which is sufficient to achieve 10bit resolution [75].

The total capacitance for each CDAC is 480fF, yielding a kT/C noise <-65dB. The switches in the CDAC are bootstrapped and sized to obtain $6.9\tau \approx 150\text{ps}$.

(a)

(b)

Figure 4.10 (a) Block diagram of the input sampling, and (b) simulated Spectra of the sampled signal

Figure 4.10(a) depicts the block diagram of the bootstrapped switch for input sampling. The differential switches (M1 and M2) are bootstrapped to enhance the linearity [91]. M3 and M4 are employed to cancel the signal feedthrough [22], whereas M5 and M6 serve to cancel the clock feedthrough. Figure 4.10(b) depicts the simulated

Spectra of the sampled signal at 400MS/s. It can be observed that the obtained SFDR and THD are 87.6dB and -80dB respectively, which are sufficient for 10 bits.

4.3.2 Dynamic Comparator

Dynamic comparators (instead of static comparators) are typically adopted for high-speed ADCs, primarily due to their fast operational speed. Figure 4.11 depicts the proposed dynamic comparator that embodies three imperative features: high-speed processing (comparator core), compensation for kickback noise, and calibration for offset. These features will now be elaborated in turn.

Figure 4.11 Proposed dynamic comparator

(I) *High-speed processing of the core circuit*

The core circuit of the comparator is realized on the basis of reported designs [13, 76] whose high speed is ascertained by the regeneration speed of the outputs (V_{OUT+} and V_{OUT-}). To complete the regeneration within the stringent time budget, i.e., $(t_3 + t_4) = 158\text{ps}$, we augment a positive feedback loop formed by two cross-coupled transistors (M5 and M6). When $CLK = '0'$, the source voltages of M5 and M6 are reset to $(V_{DD} - V_{th})$. When CLK switches to '1', M5 and M6 response immediately by amplifying the voltage difference between V_{cmp+} and V_{cmp-} , and thereafter M7-M10 accelerate the regeneration process. On the basis of Monte-Carlo simulations, the comparator achieves a 3σ delay of $<90\text{ps}$ from CLK_{cmp} to D_{cmp} with a small input of 0.2mV ($<0.1\text{LSB}$), which allows a time budget of 64ps for the ensuing decoder.

(II) *Cancellation of kickback noise*

The kickback noise is the primary noise mechanism in our comparator because large input transistors (i.e., $24\mu\text{m}/60\text{nm}$) are adopted to obtain $<-65\text{dB}$ thermal noise. The kickback noise is essentially caused by the voltage coupling through the parasitic capacitance (C_{GD_1} , C_{GS_1} , C_{GD_2} and C_{GS_2}) of the input transistor pairs (M1 and M2) during CLK switching; see Figure 4.11. Specifically, when CLK switches from '0' to '1', V_{D_1} , V_{D_2} and V_{D_13} (see the core circuit in Figure 4.11) are quickly pulled down to '0'. This voltage drop is coupled to the comparator inputs through C_{GD_1} , C_{GS_1} , C_{GD_2} and C_{GS_2} , and disturbs V_{cmp+} and V_{cmp-} . As the values of the C_{GD_1} , C_{GS_1} , C_{GD_2} and C_{GS_2} vary with the amplitude of the input signal (e.g., a higher input voltage usually results in larger parasitic capacitance [99]), the said disturbance to V_{cmp+} and V_{cmp-} is imbalanced (i.e., the kickback noise contains both common-mode [100] and differential components), and need to be mitigated.

We propose to cancel the kickback noise by means of introducing a 180-degree phase-shifted replica at the input. This is realized by employing M15 to M19 (see Figure 4.11) where M15 and M16 are identical to M1 and M2. When the voltage at V_{D_1} , V_{D_2} and V_{D_13} drops, an equal opposing voltage rise is generated at V_{D_17} and V_{D_18} . This voltage rise is coupled to V_{cmp+} and V_{cmp-} through the parasitic capacitances (C_{GD_15} , C_{GS_15} , C_{GD_16} and C_{GS_16}) of M15 and M16, and, to the first order, cancels the kickback noise (both the common-mode and the differential components).

(a)

(b)

Figure 4.12 Monte Carlo simulation results of the comparator kickback noise (a)

with, and (b) without the proposed kickback noise cancellation

Figure 4.12(a) and (b) depict the 200-run Monte Carlo simulation results of the comparator kickback noise with and without the proposed kickback noise cancellation respectively; the simulations are performed at the worst-case scenario where the input signal is full scale and the comparator operates at 2.4GHz. It can be observed that the kickback noise (i.e., $\mu \pm 3\sigma$) of the comparator is efficiently mitigated from 1.3LSB/1.7LSB to 0.3LSB/0.5LSB.

(a)

(b)

Figure 4.13 Simulated SNDR and THD performance of the ADC (at 400MS/s) versus input frequency (a) with, and (b) without the proposed cancellation of kickback noise

To illustrate the efficacy of the proposed cancellation of kickback noise, Figure 4.13(a) and (b) depict the simulated SNDR and THD performance of the ADC (at 400MS/s) versus input frequency with and without the proposed kickback noise cancellation. It can be observed that the proposed cancellation significantly improves the SNDR by more than 3dB, and the THD by more than 5dB. With the proposed cancellation, the ensuing SNDR and THD are sufficient for the targeted 10bit resolution.

(III) Calibration for Offset

The comparator offset comprises both static offset and dynamic offset. The static offset is mitigated by means of the calibration (see Figure 4.11) realized on the basis of [101]. This calibration is performed in the foreground at the outset, and subsequently operates in the background to accommodate the temperature variations. The background operation is performed during the input sampling phase (P0; see Section 4.2.1) of the conversion.

During the calibration, V_{cmp+} and V_{cmp-} are connected to V_{CM} , and the comparator digital output (D_{cmp}) is initially determined by the static offset, i.e., $D_{cmp} = '1'$ for positive offset, and vice versa. Based on the D_{cmp} value, the gate voltage of M4 is adjusted by either charging or discharging C_{cal} . The adjustment continues until D_{cmp} toggles between '0' and '1', where the offset is stored in C_{cal} and cancelled through M4. Note that M20 and M25 respectively serve as the charging and discharging current source to C_{cal} . M21 and M24 are the corresponding switches, where the charge injection is cancelled by M22 and M23 respectively.

The proposed calibration is able to cancel offsets up to $\pm 18\text{mV}$, and achieves the minimum offset of $\sim 0.2\text{mV}$ ($\sim 0.1\text{LSB}$) at 400MS/s. The calibration range of $\pm 18\text{mV}$ is

sufficient because, on the basis of Monte-Carlo simulations, the 3σ offset of the comparator without calibration is $\pm 13\text{mV}$.

The dynamic offset is primarily the offset variations arising from the variations of the common-mode voltages at the comparator input as described in Section 4.2.2. These offset variations are typically relatively large when the input transistors operate in the weak inversion region, but are significantly smaller in the strong inversion region [98, 102]. In our design where the common-mode voltages vary between 550mV and 962.5mV (i.e., between V_{CM} and $V_{CM} + \frac{3}{4}V_{ref}$), the input transistors always operate in the strong inversion region, leading to small offset variations. Moreover, the size of the transistor M13 is designed to be 3 times smaller than the input transistors to limit the tail current at high input common-mode voltages, thereby further reducing the offset variations.

Figure 4.14 Simulated offset variations versus the variations of the comparator input common-mode voltage

Figure 4.14 depicts the simulated offset variations (after the aforesaid calibration performed at $V_{CM} = 550\text{mV}$). It can be observed that the resulting offset variations are largely negligibly small (i.e., $<0.1\text{LSB}$) for common-mode voltages ranging between 550mV and 962.5mV .

4.3.3 SA Ctrl Logic

Figure 4.15 Block diagram of the SA ctrl logic

Figure 4.16 Proposed high-speed FF register

Figure 4.15 depicts the block diagram of the SA ctrl logic, where the shift register and the flip-flop (FF) array serve to generate SA ctrl for the Ref_CDAC and the differential Signal_CDAC respectively. On the basis of the aforementioned speed requirements, the SA ctrl needs to complete all the generation within 94ps. As the FF array serves as the critical path herein, it is imperative that the FF is high speed. Figure 4.16 depicts the proposed high-speed FF register that is realized on the basis of the conventional C²MOS dynamic register [103] where the data is held by the parasitic capacitance between the two clocked buffers when CLK = 0. Compared to the conventional C²MOS dynamic register, the proposed FF register augments both set (SET by M1) and reset (RST by M2) functions without speed degradation. On the basis of the Monte-Carlo simulations, the proposed FF achieves 3 σ *D*-to-*Q* delay of <65ps.

4.4 MEASUREMENT RESULTS

Figure 4.17 Microphotograph of the proposed ADC prototype

Figure 4.17 depicts the microphotograph of the proposed ADC prototype realized in 65nm bulk CMOS process. To minimize parasitic impedance, the prototype is bonded

directly onto the test board, and the digital outputs are collected by a logic analyzer without decimation. The chip size is $0.3\text{mm} \times 0.25\text{mm}$, with the CDACs (Signal_CDAC₊, Signal_CDAC₋ and Ref_CDAC) occupying 61% of the silicon area. The ADC operates from a 1.1V power supply, and has 2.2V rail-to-rail full-scale differential input (V_{FS_diff}).

The measure setup for our ADC prototype is as follows. The power supplies (including both digital power supply and analog power supply) are provided by high-performance LDOs that are surface-mounted on the PCB. The reference of the ADC was generated externally by a high-accuracy reference generator (Agilent B2902A). Large bypass/reservoir capacitors (for the reference and the power supply voltages) are employed both on-board and on-chip to decouple noise and bypass the transient current therein [6]. The input signal of our ADC is generated by a signal generator, and subsequently converted to fully differential signals by a high-accuracy balun (i.e., BALH-0003SMG) on board. The digital outputs are collected by a logic analyzer without decimation, and subsequently analyzed by means of Matlab on PC.

Figure 4.18 Power dissipation breakdown of the ADC prototype

Figure 4.18 depicts the power dissipation breakdown of the ADC prototype at 400MS/s. The total power dissipation at 400MS/s is 5.61mW, where 2.6mW is dissipated for the SA control logic and CDAC switches, 1.28mW for the clock, 0.72mW for the comparators, and 1.01mW for the reference.

(a)

(b)

Figure 4.19 Measured (a) DNL, and (b) INL

Figure 4.19 depicts the measured DNL and INL at 400MS/s. It can be observed that the DNL is within $+0.72\text{LSB}/-0.81\text{LSB}$ whereas the INL is within $\pm 0.93\text{LSB}$. The

measured DNL and INL of the proposed ADC satisfy the stipulated IEEE 802.11ac specifications.

Figure 4.20 Measured FFT spectrum (16384 points) of the ADC prototype

Figure 4.20 depicts the measured FFT spectrum of the ADC prototype output at 400MS/s with -2.1dBV_{FS_diff} input signal at 197MHz. On the basis of the obtained spectrum, the measured SNDR and SFDR are 51.9dB and 63.7dB respectively. The HD3 (3rd harmonic) is the dominant distortion component, and is mainly due to the dynamic distortion in the input sampling switches, the INL arising from compactor mismatch, and the settling error arising from the inter-sample interference [4]. Other nonlinearities are largely negligible ($<-70\text{dB}$).

Figure 4.21 Measured SNDR and SFDR versus input frequency

Figure 4.21 depicts the measured SNDR and SFDR versus the input frequency at 400MS/s. The proposed ADC achieves SNDR >52dB (equivalent to 8.33 ENOB (effective number of bits)) up to 197MHz. The peak SNDR is ~55dB, equivalent to 8.78 ENOB. The SFDR remains above 64dB up to 197MHz, and features a peak value of 69dB at low input frequency.

Figure 4.22 Measured SNDR and SFDR versus conversion rate

Figure 4.22 depicts the measured SNDR and SFDR versus the conversion rate. The measurement is performed with a normalized input frequency (input frequency/conversion rate=0.493). It can be observed that the SNDR and SFDR remain largely constant as the conversion rate increases up to 400MS/s. As expected, both SNDR and SFDR degrades at higher conversion rates (>400MS/s) and this is mainly attributed to the reduced clock periods.

Figure 4.23 Measured SNDR versus input power

Figure 4.23 depicts the plot of measured SNDR versus the input power that is normalized to the full-scale input, where the input frequency and the conversion rate are 197MHz and 400MS/s respectively. It can be observed that our ADC prototype achieves the highest SNDR where the input power is between -5dBFS and -1dBFS. In the case of lower input power (e.g., <-5dBFS) where the signal strength is reduced while the noise is largely unaffected, the SNDR expectedly decreases proportionally as the input

power reduces. In the case of higher input power (e.g., $>-1\text{dBFS}$), the distortion arising from the CDAC switches increases [3], hence degrading the SNDR.

Table 4.3 tabulates the measurement performance of the proposed ADC prototype, and benchmarks it against state-of-the-art ADCs with similar specifications. The key features of the prototype ADC include $\text{SNDR} \geq 51.9\text{dB}$ across the 200MHz Nyquist bandwidth at 400MS/s , dissipating 5.61mW power from a 1.1V power supply. Of particular interest, amongst the benchmarked ADCs, the proposed ADC features not only the smallest number of capacitor arrays (amongst the reported CDAC-based 2bit/step SAR ADCs) but also the most competitive FoM of 43fJ/conv.step ; the FoM is calculated on the basis of $\text{Power}/(f_s * 2^{\text{ENOB}})$.

Table 4.3 Measurement performance summary, and benchmarking against state-of-the-art ADCs

Parameters	This work	JSSC [76]	VLSI [78]	JSSC [39]	JSSC [13]	ISSCC [104]	JSSC [11]
Architecture	2b SAR	2b SAR	2b SAR	2b SAR	2b SAR	TI-SAR	TI-SAR
Technology (nm)	65	45	28	65	130	130	65
Area (mm^2)	0.075	0.016	0.004	0.028	0.09	1.1	0.78
Supply voltage (V)	1.1	1.25	1	1.2	1.2	1.2	1
Resolution (bits)	10	7	8	8	6	8	10
Number of capacitor arrays	3	4	6	NA (Resistive)	6	NA (20 due to TI)	NA (8 due to TI)
f_s (MS/s)	400	1250	750	400	1250	600	1000
SNDR (dB) @Nyquist	51.9	40.8	43.3	40.1	31.9	44	51.4
Power (mW)	5.6	7.2	4.5	4	32	30	18.9
FoM (fJ/conv.step) @Nyquist	43	80	50	117	800	388	62.3

4.5 CONCLUSIONS

A 10bit 400MS/s SAR ADC embodying a proposed 2bit/step conversion scheme with single reference voltage has been proposed. By means of the said proposed 2bit/step scheme, the proposed ADC featured not only a simplified structure with the least number of capacitor arrays amongst the reported CDAC-based 2bit/step SAR ADCs but also high energy efficiency. The proposed ADC further featured an inherently symmetrical architecture with highly matched interconnections and small input loading, leading to enhanced system matching and higher accuracy. A proposed high-speed high-accuracy dynamic comparator and high-speed SA ctrl logic have also been proposed to enhance high conversion rate and high accuracy. The prototype ADC featured SNDR >52dB and SFDR >63.7dB across 200MHz Nyquist bandwidth at 400MS/s conversion rate while dissipating 5.61mW power. When benchmarked with state-of-the-art 2bit/step SAR ADCs, the proposed ADC 2bit/step ADC featured a highly competitive FoM of 43fJ/conv.step.

Chapter 5 CONCLUSIONS AND RECOMMENDATIONS

This chapter draws the conclusions of the work reported in this Ph.D. research program, and delineates the recommendations for further work.

5.1 CONCLUSIONS

The primary objective of this Ph.D. program pertained to the design, monolithic realization and measurements (and verification) of our proposed pipeline-based and SAR-based high-speed high-resolution ADCs for the next-generation telecommunication systems. The conclusions of the research work are as follows.

In Chapter 1, we have presented the motivation, objectives and contributions of our Ph.D. program delineated in this thesis.

In Chapter 2, we have critically and comprehensively reviewed high-speed high-resolution Nyquist-rate ADCs, including an analysis of the ADC performance attributes, a critical review of flash-based, pipeline-based and SAR-based ADC realizations, an in-depth analysis of the critical issues and the limitations of reported mitigations for these realizations. As the pipeline-based and SAR-based ADCs offer the most advantageous architectures for high speed and high resolution, the emphasis of this review was these architectures.

In Chapter 3, we have presented the design, monolithic realization, and measurements (and verification) of our proposed MDAC-free 11bit 1GS/s Pipeline ADC. The proposed ADC architecture eliminated the need for the “problematic” MDAC, thereby largely mitigating the associated critical issues. Of particular note, the proposed

architecture simplified the pipeline stage to a single-iteration SAR, and uniquely offered combined advantages of higher accuracy and higher conversion rate compared to the conventional pipeline ADC, particularly when the process technology scales to finer nodes. In addition, the required hardware of the channel ADC is reduced by means of the extraction of the quantization for the MSB at the front of the channel ADCs.

The prototype ADC was fabricated in 65nm CMOS process, and its primary attributes included $\text{SNDR} \geq 55.9\text{dB}$ across 500MHz Nyquist bandwidth at 1 GS/s conversion rate with 230mW power dissipation from a dual power supply of 1.2V/2V. The FoM of the design, either based on Walden $\text{FoM}_{\text{Walden}}$ or Schreier $\text{FoM}_{\text{Schreier}}$, was shown to be highly competitive amongst state-of-the-art designs. In addition, the proposed architecture can potentially achieve better performance with finer technology nodes.

In Chapter 4, we have presented the design, monolithic realization, and measurements (and verification) of our proposed 2bit/step 10bit 400MS/s SAR ADC. The proposed ADC embodied a novel 2bit/step conversion scheme, thereby effectively and efficiently mitigating the critical speed limitation of the SAR ADCs. The proposed ADC was shown to feature higher energy efficiency (attributed to the smallest number of capacitor arrays amongst reported CDAC-based 2bit/step SAR ADCs), smaller input loading (because of the single-CDAC sampling, and enhanced system matching) and higher accuracy (due to the inherently symmetrical architecture with highly-matched interconnections). In addition, we proposed a novel kick-back noise cancelation, a proposed offset calibration as well as a high-speed dynamic comparator and SA control logics. These were shown to effectively and efficiently enhance the performance of the proposed ADC.

The prototype ADC was fabricated in 65nm CMOS process and its primary attributes included SNDR ≥ 51.9 dB across the 200MHz Nyquist bandwidth at 400MS/s, dissipating 5.61mW power from a 1.1V power supply. Of particular interest, the proposed ADC featured not only the smallest number of capacitor arrays (amongst the reported CDAC-based 2bit/step SAR ADCs) but also the most competitive FoM amongst the benchmarked ADCs.

Overall, we have made significant contributions towards the design and realization of high-speed high-resolution ADCs for the next-generation telecommunication systems.

5.2 RECOMMENDATIONS FOR FUTURE WORK

On the basis of the literature review and the research work in this research program, we recommend the following for future work.

- (i) Investigation into the design of front-end S/Hs on the basis of InGaAs process from the SMART-LEES (III/V-on-CMOS) process for CMOS ADCs

As described in Chapter 2, the front-end S/H is one of the most critical building blocks in high-speed high-resolution ADCs as it largely determines the bandwidth and linearity of the entire ADC. The front-end S/H is typically realized by CMOS largely for sake of monolithic integration, but the penalty is severe. Specifically, as explained in the Chapter 3, the bandwidth and linearity of the S/H are severely limited by the transconductance and the intrinsic gain of the CMOS transistors, particularly in the case of a heavy output loading. To achieve the desired performance, the CMOS S/H often entails substantial power and hardware overheads.

In view of these limitations, there are unambiguous advantages to realize the front-end S/H on the basis of a III/V process (i.e., InGaAs process from SMART-LEES III/V-on-CMOS fabrication process) that intrinsically embodies higher electron mobility, hence substantially extended bandwidth and improved linearity compared to standard CMOS processes. In short, we recommend an investigation into the design of III/V-based S/H based on the SMART-LEES process.

- (ii) Following (i), in view of the attractive merits of the III/V S/H, there is a good possibility that the integration of a III/V S/H and a CMOS ADC would offer substantial advantages of wider input bandwidth, better dynamic range, yet with smaller power and hardware overheads compared to the conventional fully-CMOS counterpart. In view of these unique advantages, we recommend an investigation into the design and realization of a multi-GS/s >12bit III-V integrated S/H + CMOS ADC, with substantially enhanced energy efficiency and minimal hardware overheads.
- (iii) Finally, we suggest an investigation the calibrations for time-interleaving errors. As explained in Chapter 1, state-of-the-art calibrations for time-interleaving errors, particularly for the input-dependent timing mismatch, suffer from several undesirable issues. These include the complex digital computation with long convergence time, the need for pilot signals interrupting normal operation, etc., and the efficacy of time-interleaved ADCs is therefore largely limited. Consequently, the conversion rate of high-speed ADCs is often limited to multi-GS/s. We recommend an investigation to develop innovative calibrations to

mitigate the unsolved issues, with the intention of achieving 10GS/s and beyond ADC conversion rates, yet with minimal hardware and power overheads.

AUTHOR'S PUBLICATIONS

- [1] Q. Liu, W. Shu, and J. S. Chang,

“A 1GS/s 11bit SAR-assisted Pipeline ADC with 59dB SNDR in 65nm CMOS”

IEEE Transactions on Circuits and Systems II: Express Briefs, Accept.

- [2] Q. Liu, W. Shu, and J. S. Chang,

“A 400MS/s 10bit 2bit/step SAR ADC with 52dB SNDR and 5.61mW Power Dissipation in 65nm CMOS”

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, pp. 3444-3454, 2017.

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