Class-E RF power amplifier with a digitally-controlled output matching network for dynamic load modulation

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Class-E RF Power Amplifier with
a Digitally-Controlled Output Matching Network for
Dynamic Load Modulation

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CONTENTS

ABSTRACT

This Master of Engineering research project pertains to the analysis, design, and Integrated Circuit (IC) realization of a novel Class-E RF Power Amplifier (PA) capable of generating a variable-envelope output signal for Polar transmitters in Wireless Body Area Network (WBAN) with emphasis on high power efficiencies.

A Class-E RF PA with a novel digitally-controlled variable output matching network (OMN) is proposed. The PA is designed so that the ZVS condition can be achieved for high-efficiency operation. The OMN performs the Dynamic Load Modulation (DLM), and is controlled/varied directly by the digital Amplitude Modulation (AM) input signal without any need for a conventional supply modulator, thereby saving area and power dissipation. The OMN architecture design allows the use of on-chip inductors, as well as off-chip inductors including high Quality factor bond-wires to improve the efficiency.

The proposed Class-E PA embodying the novel digitally-controlled variable OMN is designed using the TSMC CMOS 40 nm technology and benchmarked, based on the IEEE 802.15.6 standard for WBAN, against a reference state-of-the-art PA. The benchmarking shows that the proposed PA features a higher drain efficiency, while achieving a similar/comparable performance to that of the reference PA.

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LIST OF ABBREVIATIONS

ACPR   Adjacent Channel Power Ratio

AM   Amplitude Modulation

CMOS   Complementary Metal Oxide Semiconductor

DLM   Dynamic Load Modulation

EVM   Error Vector Magnitude

IC   Integrated Circuit

OMN   Output Matching Network

PA   Power Amplifier

PLL   Phase-Locked Loop

PM   Phase Modulation

PWM   Pulse Width Modulation

RF   Radio Frequency

SMPA   Switch-Mode Power Amplifier

WBAN   Wireless Body Area Network

ZVS   Zero Voltage Switching

ZVDS   Zero Voltage Derivative Switching

Chapter 1

INTRODUCTION

1.1   Motivation

The healthcare sector is in an evolution, progressing from healing sickness towards monitoring patient data and anticipating health issues that can be identified through the data.   The enormous potential of data monitoring has been the driving force in the interest and significant growth of low-power wireless biomedical technologies, such as the Wireless Body Area Network (WBAN) [2].

The WBAN is a short-range wireless network of devices that are in the vicinity of, or implanted in the human body in order to sense vital parameters, to perform drug delivery, or to stimulate bodily functions [2, 3].   These WBAN devices have two key requirements.   First, they should have low output power to reduce the electronic and magnetic energy absorbed by human tissues for the sake of the health.   Second, they should have high power efficiencies to ensure a long battery lifespan and a small battery size [3].

The WBAN devices employ transceivers for data communications with a central node, such as a smartphone.   In the transceiver, the building block that dominates the output power and have the largest power consumption is usually the radio-frequency (RF) Power Amplifier (PA) in the transmitter part of the transceiver [4], and accordingly, it is important for the PA to have low output power and a high power efficiency.

However, for PA design, it remains a challenge to simultaneously achieve the said requirements [4].

The choice of the transmitter architecture is paramount as it dictates the PA design. The conventional quadrature architecture requires a linear PA, usually a Class-AB PA, to amplify a variable-envelope signal required by several communications standards, including the WBAN standard as described in the IEEE 802.15.6 [5]. For output linearity requirements, Class-AB PAs tend to operate in the back-off region further from their peak output power point; however, this peak is also their most efficient operating point [6]. As a result, the power efficiency of these PAs is low, typically <30%. This is undesirable, particularly in the context of the low-output-power requirements. Non-linear switched-mode PAs, such as Class-E PAs, are more power-efficient than their conventional linear counterparts. Further, with linearization techniques, such as the Polar architecture, the switched-mode PAs can also receive and amplify a variable-envelope signal [4]. The switched-mode PAs are, therefore, preferred for WBAN applications.

Fig. 1.1 depicts a transmitter embodying a Polar architecture. The input signals are digital IQ (quadrature) data generated by a preceding microcontroller in a body sensor application. The digital data represents a variable-envelope input signal. The Polar decomposition essentially splits the input signal into a Phase Modulation (PM) signal, φ, on the PA input path, and into an Amplitude Modulation (AM) signal, A, on the PA supply [4]. In conventional Polar transmitters, a supply modulator, such as a
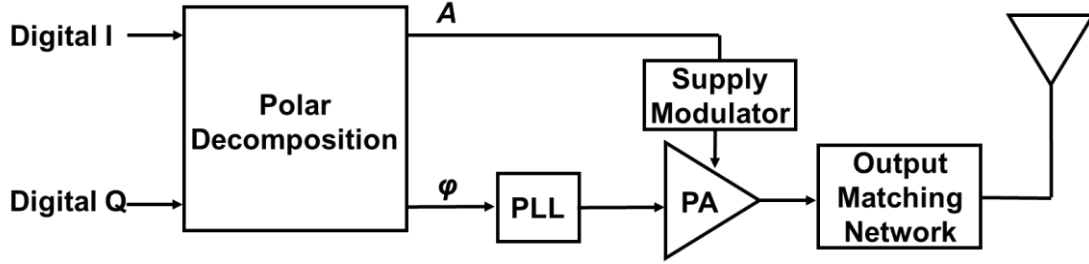
Fig. 1.1   Polar Transmitter

DC-DC converter, is typically needed to perform the AM by modulating the voltage supply to the PA.   The DC-DC converter is in the direct path of the large current flowing into the PA from the supply.   Consequently, its transistors require significant driving power that can cause considerable switching and conduction losses, and further, the passive components in the DC-DC converter also cause conduction losses.   The losses due to the DC-DC converter can translate to >20% loss to the overall power efficiency of the PA [7].   On top of that, the inductor in the output matching network (OMN) of the PA can cause another >20% loss.   Thus, it is already a loss of >40% to the power efficiency even before considering the loss from the transistors of the PA itself.   It is, therefore, desirable to mitigate the power loss due to the AM and the OMN.

A variant of the Polar transmitter architecture performs the AM by modulating the load impedance seen by the PA.   This AM technique is also known as the dynamic load modulation (DLM) [1, 8], and is done by varying the OMN according to the baseband signal (AM) as depicted in Fig. 1.2.   This DLM technique allows high-efficiency non-linear PAs to be able to generate the same variable-envelope output signal as what their linear counterparts can do.   The DLM also avoids dealing with the large power in the supply modulation method, thereby circumventing potential significant power loss [1].
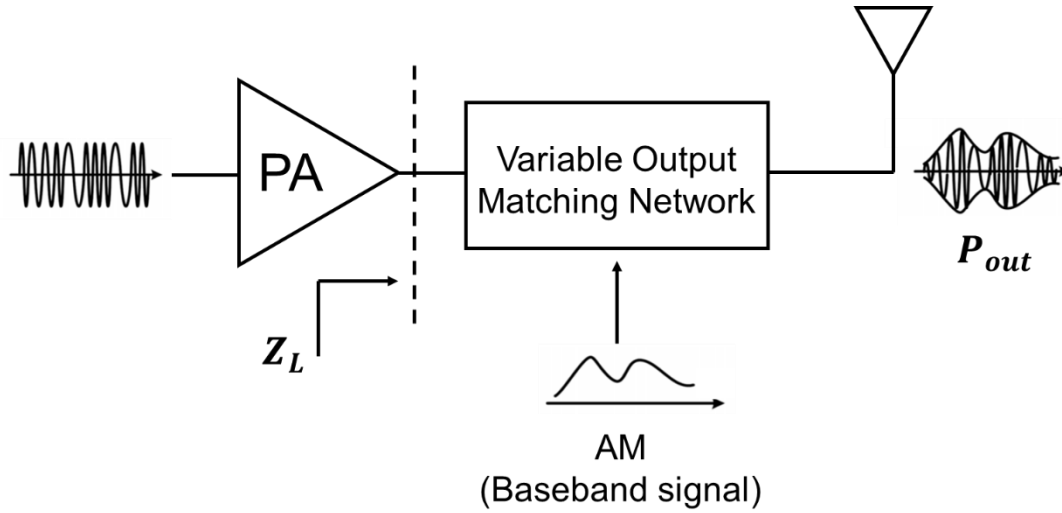
Fig. 1.2   Realizing AM by varying the output matching network

The variable OMN between the PA and the antenna load comprises one or more inductors.   When realized on-chip, the quality factor (Q) of inductors in CMOS technologies are typically only less than 10 for frequencies up to 5 GHz [4], thereby causing significant loss.   Bond-wires to the package or board or antenna can be utilized as inductors (at RF frequencies) and their Q is much higher — about 100 at 5 GHz [9]. Nonetheless, since the inductance values are fixed, they have not been used as part of variable OMNs thus far, and only capacitors are varied [1].   Further, in the Polar transmitter for the body sensor application in Fig. 1.1, the input data are digital, and it would be desirable if these digital input data could directly control the variable OMN without the need for any data converter.   In short, there is a need for a novel variable OMN that can mitigate the loss of the on-chip inductors, while at the same time, is able to vary its component values by digital means so that it can perform the AM for Class-E PAs in Polar transmitter with digital inputs applications.

In the conventional Class-E PA, as illustrated in Fig. 1.3, there are two optimum switching conditions that are required for high efficiency operation [4]. They are as follows:

(1) The Zero-Voltage-Switching (ZVS) condition: the drain voltage, $v(t)$, in Fig. 1.4 returns to zero at the moment the transistor turns on.

(2) The Zero-Voltage-Derivative-Switching (ZVDS) condition: the slope of $v(t)$, in Fig. 1.4 is zero when the transistor turns on.

Assuming the L_{rfc} is an ideal RF choke, these two conditions can be theoretically achieved by selecting properly designed values of the following three components depicted in Fig. 1.3: the shunt capacitor C_{sh}, the excess inductor L_x, and the load impedance R_L. In the conventional Class-E PA, R_L is static and the aforesaid two switching conditions can theoretically be met; however, the conventional Class-E PA cannot generate a varying-envelope output signal. We have discussed earlier that when Class-E PAs operate based on the DLM, or in other words, when they employ a variable OMN, they can generate a varying-envelope output signal that is required by many wireless communications standards. Nonetheless, the variable OMN will render the Z_L seen by the PA to vary. Accordingly, it will be difficult to ensure the switching conditions can be achieved simultaneously, and the power efficiency will be decreased [10]. In theory, satisfying the ZVS condition alone can result in 100% efficiency, whereas the ZVDS condition helps to ensure the PA achieve the ZVS condition when practical aspects are considered, such as mitigating drain current spikes of the PA. It

has been reported [11] that the ZVS condition is the more important condition among

the two conditions in terms of the power efficiency that can be achieved.   In this view,

it is imperative that the Class-E PA employing the digitally-controlled variable OMN,

discussed earlier above, is designed such that it is able to achieve the ZVS condition to

obtain a high power-efficiency.
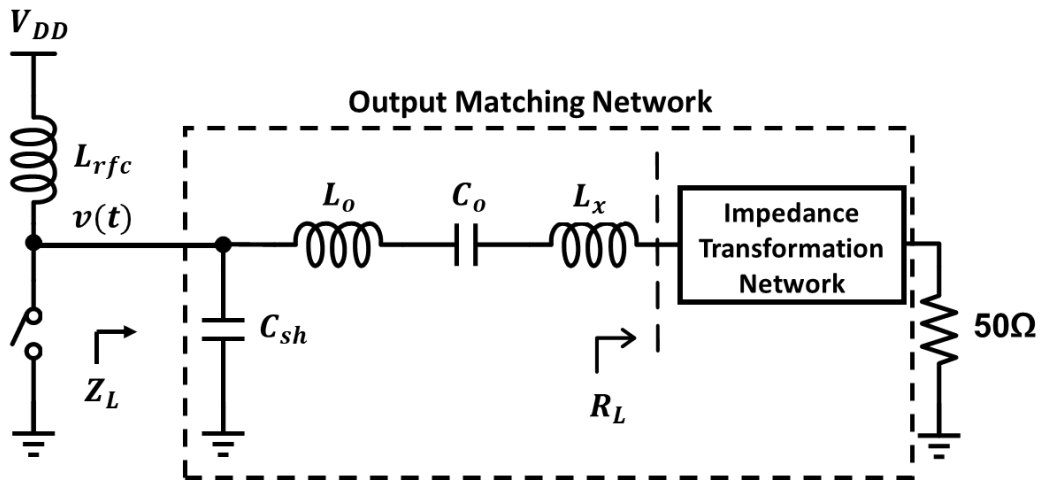
Fig. 1.3   Conventional Class-E PA
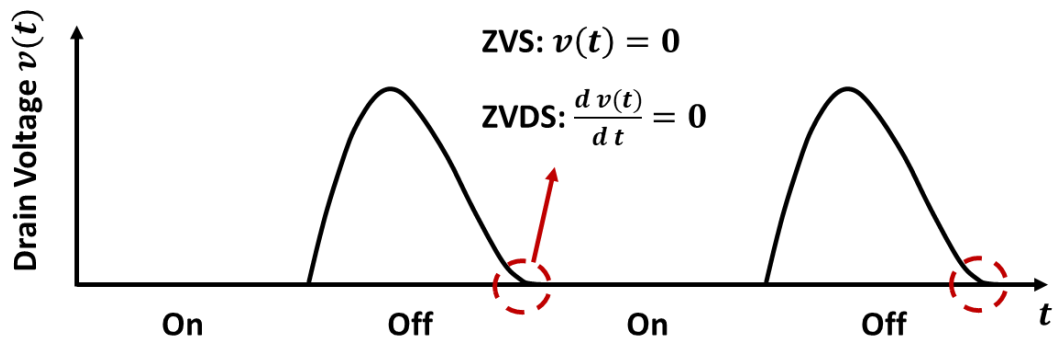
Fig. 1.4   Drain voltage of the ideal Class-E PA

1.2 Objectives

The overall objectives of the work described in this thesis are to analyze, design, and realize a variable-envelope Class-E PA in an Integrated Circuit (IC) form for Radio-Frequency (RF) Polar transmitters in short-range portable applications, such as WBAN, with emphases on low output power and high power efficiency.

The specific objectives of the work herein are:

(i) To propose a novel variable OMN that can be controlled digitally to perform the DLM for the Polar transmitter of the transceiver. The proposed OMN should be designed to operate without using on-chip inductors to mitigate the high loss therein;

(ii) To propose and design a Class-E PA that can employ and control the variable OMN in (i). The Class-PA should be designed such that it can satisfy the ZVS condition for high-efficiency operation;

(iii) To verify the proposed Class-E PA design embodying the digitally-controlled variable OMN in (ii) by means of computer simulations;

(iv) To physically realize the proposed Class-E PA design by means of a prototype IC using a CMOS technology for good integration with other CMOS digital building blocks of the transceiver; and

(v) To benchmark the proposed Class-E PA design against state-of-the-art designs.

1.3 Contributions

The contributions of the work described in this thesis are as follows:

(a)   A novel digitally-controlled variable OMN is proposed.   The OMN is controlled by the digital AM input signal, and performs the DLM.   It is realized using digital logic circuits, switched-capacitors, and bond-wires.   There are two salient features of the proposed OMN.   First, the OMN is directly controlled by the digital AM data.   It obviates the need for the conventional supply modulator, thereby saving area and power dissipation.   Unlike those in the supply modulator that have to handle a large current, the transistors employed by the OMN are small low-power digital transistors.   Second, the proposed OMN has a novel network architecture that can employ on-, or off-chip inductors, or both inductor types.   This means that high-Q bond-wires can be employed to improve the efficiency.

(b)   A Class-E PA that employs the digitally-controlled variable OMN in (a) is proposed.   Due to the variable OMN, the proposed PA can perform the DLM, and accordingly, is able to generate a variable-envelope signal (similar to linear PAs).   The PA is designed so that the ZVS condition can be achieved for high-efficiency operation.

(c)   The proposed Class-E PA in (b) is designed using the TSMC CMOS 40 nm technology.   The proposed PA is benchmarked using computer simulations at 1.1 V supply and 900 MHz carrier frequency (IEEE 802.15.6 standard for WBAN)

against a reference state-of-the-art PA with a digitally-controlled variable OMN based on the design in [1]. The proposed PA achieves a 51% drain efficiency at 14.4 dBm peak output power, a 7.8 dB dynamic range, –18.84 dB Error Vector Magnitude (EVM), and –29.7 dB Adjacent Channel Power Ratio (ACPR). On the other hand, the reference PA has a 36% drain efficiency at 12.2 dBm peak output power, a 9.9 dB dynamic range, –17.45 dB EVM, and –33.2 dB ACPR. On the basis of the simulations, the proposed PA has a 15% higher drain efficiency while having a comparable performance to that of the reference PA. Both PAs satisfy the (transmitter) requirements specified in the IEEE standard for WBAN (–15 dB EVM, –26 dB ACPR).

(d)   The proposed Class-E PA and the reference Class-E PA are realized on a prototype IC using the TSMC CMOS 40nm technology, and measured. The IC is bonded directly on a Printed Circuit Board (PCB) for the measurements, and the bond-wire inductors connect the IC pads to the PCB traces. On the basis of experimental measurements at 1.1 V supply and 900 MHz carrier frequency, the proposed PA achieves a 14.5% power drain efficiency at peak output power of 5.7 dBm, –10.5 dB EVM, and –17.6 dB ACPR, while the reference PA has a 10.8% drain efficiency at 4 dBm peak power, –9.9 dB EVM and –18.6 dB ACPR. The benchmarking shows that the proposed PA features a higher drain efficiency, while achieving a similar/comparable performance to that of the reference PA. The measured performance of both PAs, however, are somewhat inadequate to satisfy the (transmitter) requirements specified in the IEEE standard for WBAN.

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This can be attributed to the loss from the inductance and resistance arising from the closely-spaced IC pads and the consequent narrow (lossy) traces on the PCB used in the measurements. These limitations can be rectified in the subsequent IC and PCB iterations.

1.4   Organization of the Thesis

The remainder of this thesis is organized in the following manner.

Chapter 2 provides a comprehensive literature review as background for the work described herein. It commences with an overview of the WBAN standard. Thereafter, a literature review of the prevalent transmitter architectures is presented. Subsequently, linear and non-linear PAs are compared, and this is followed by a review on the Class-E PA. Finally, the bond-wire inductor is also discussed and compared with the on-chip spiral inductor.

Chapter 3 presents the proposed high-efficiency Class-E PA with a novel digitally-controlled variable OMN. It describes the theoretical analysis of the PA operation, the design procedure of the PA, and the IC layout implementation of the PA. Chapter 3 also presents the design of a reported state-of-the-art Class E-PA. This PA is used as a reference design when evaluating the performance of the proposed PA.

Chapter 4 presents the benchmarking results obtained from simulation of the proposed Class-E PA against that of the reference PA design for WBAN applications.

Chapter 5 presents the IC measurement results of the proposed PA and the reference

PA.

Chapter 6 concludes this thesis by highlighting the contributions of the work herein, and offers recommendations for future work.

Chapter 2

LITERATURE REVIEW

This chapter commences with an overview of the WBAN and the IEEE 802.15.6 standard. Thereafter, the prevalent transmitter architectures are reviewed for their suitability for WBAN applications. Subsequently, a literature review of linear PAs and non-linear PAs is presented and followed by a detailed review on Class-E PAs. Finally, the bond-wire inductor is described and compared with the on-chip spiral inductor.

2.1   Wireless Body Area Network

The trend in first-hand health monitoring and medical care [2] drives the technological advances in low-power microelectronics, sensor miniaturization, and wireless networking such as WBAN [3]. WBAN is an RF based wireless networking technology that interconnects wearable devices with sensor or actuator capabilities that are implanted inside, surface-mounted on, or carried by the human body [3].

Fig. 2.1 depicts an overview of the WBAN system. The WBAN devices or sensor nodes measure and collect physiological data, such as heart rate and blood pressure, and transmit the data to the central node, such as a smartphone, or a smartwatch, located around or on the human body. Typically, the transmission range of the WBAN devices is about 2 m. The central node is used as a data hub to collect the data from the WBAN devices and transmit the data further to another computing platform at a distant location
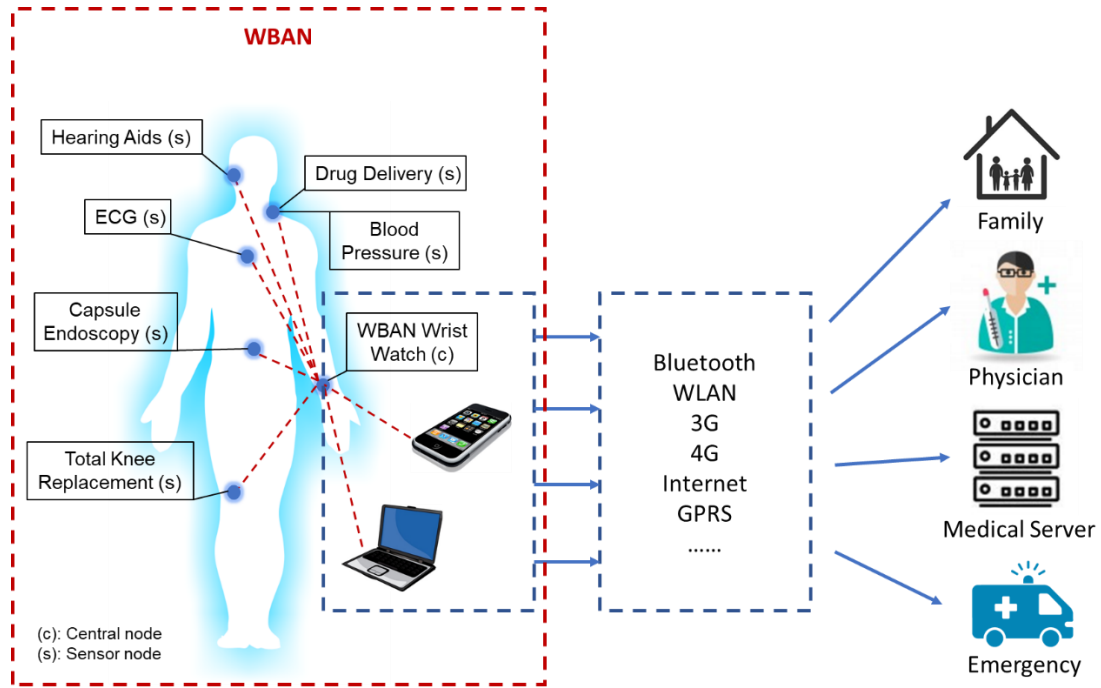
Fig. 2.1   An overview of the WBAN system

via other wireless networks with a larger transmission distance, such as the Wireless Local Area Network (WLAN), the internet, 4G, Bluetooth, etc.   This hierarchical architecture facilitates the physiological data transmission from the WBAN devices on the patient to the family members and medical professionals regardless of their locations, and enables continual monitoring on the health of the patients, local activations of emergency alarms, as well as, drug releases with a remote control [3]. In addition to healthcare, WBAN aims to apply to diverse applications, such as personnel safeguarding, secure authentication, and consumer electronics [3].

The IEEE 802.15.6 standard, ratified in 2012, sets the standards for WBAN. Table 2.1 summarizes the parameters for WBAN transmitters to follow [5].

Table 2.1   Specifications for WBAN transmitters

Modulation Scheme	Symbol Rate (ksps)	Pulse Shaping	Channel Bandwidth (kHz)	Maximum EVM (dB)	Maximum ACPR (dB)
π/4-DQPSK	600	SRRC	400	−15	−26

The π/4-DQPSK is a digital phase modulation scheme where any bit change results in a phase change in the output signal.   The sharp transitions in the time domain due to the phase change requires an unnecessarily wide bandwidth in frequency domain. Pulse shaping is required to constraint the signal bandwidth within a certain range.   Fig. 2.2 depicts the π/4-DQPSK waveform before and after the pulse shaping.   The resulting waveform after the pulse shaping shows a variable-envelope signal.   For WBAN, the pulse shaping is implemented using the Square Root Raised Cosine (SRRC) filter.

The EVM is a measure of the deviation of the actual signal points from the ideal signal points in the constellation diagram of the modulation scheme.   The EVM quantifies the signal distortion caused by the transmitter.

The ACPR is the ratio of the integrated power in the adjacent channel to the integrated power in the main channel.   It measures the spectral regrowth caused by the nonlinearity of the transmitter.
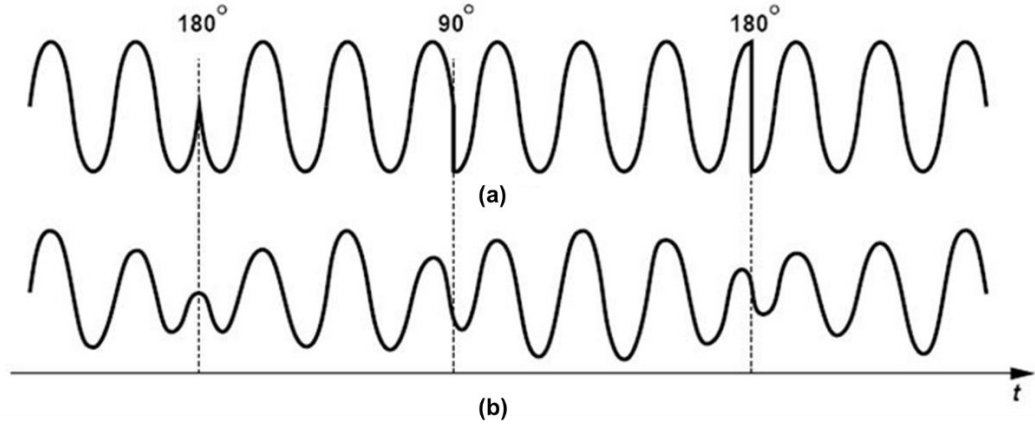
Fig. 2.2 **π/4-DQPSK waveform**

(a) before pulse-shaping and (b) after pulse-shaping

2.2 Transmitter Architectures

This section will provide a review of the conventional analog transmitter and current-art digital transmitters that are suitable for linear amplification of variable-envelope signals required by modulation schemes, such as the π/4-DQPSK used by WBAN.

Fig. 2.3 depicts a simplified version of the conventional analog transmitter architecture. The conventional analog transmitter requires a Digital-to-Analog Converter (DAC) to convert the digital baseband quadrature (IQ) signals into analog signals, and other analog building blocks, including filters and RF mixers [4]. The input to the PA is a variable-envelope input signal, and therefore, requires a linear PA, usually a Class-AB PA to amplify the input signal. Class-AB PAs, however, have to be backed-off from their peak output power point, which also happens to be its most efficient operating point [6]. Thus, the power-efficiency of these PAs is very low,

typically <30%. This is undesirable, particularly in the context of the low output power requirements.
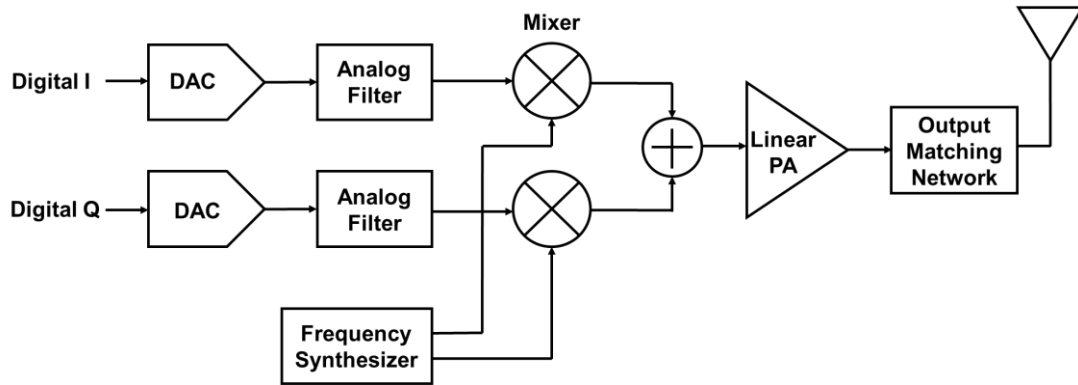
Fig. 2.3   Conventional analog transmitter

Fig. 2.4 depicts a digital transmitter based on the bandpass Delta-Sigma (ΔΣ) modulation, where the digital IQ signals are up-converted and combined into a 1-bit signal for the PA [12, 13]. Although this transmitter can employ a highly efficient switched-mode PA (SMPA), the bandpass ΔΣ modulation generates out-of-band quantization noise that degrades the power efficiency and corrupts the adjacent channels. Further, this transmitter requires an oversampling frequency of 4x the RF carrier frequency that is impractical and causes the transmitter to dissipate significant power.
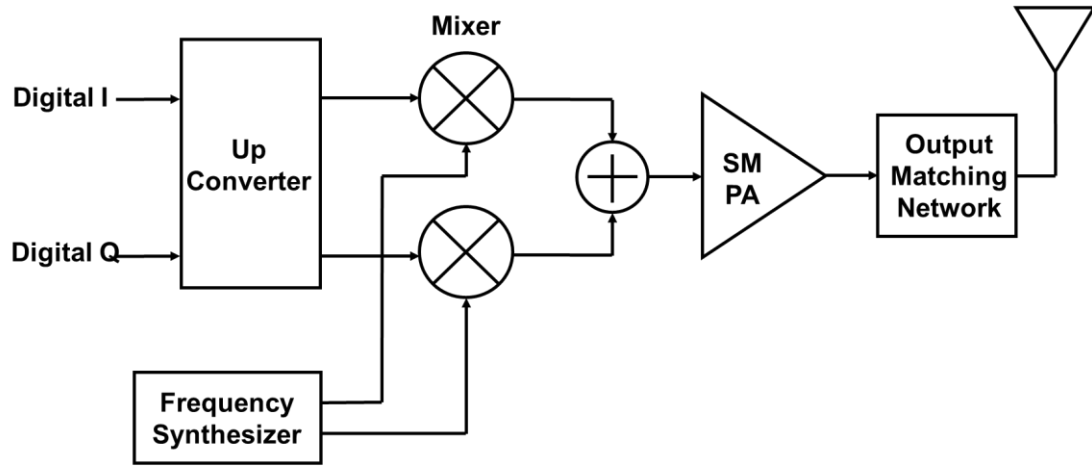
Fig. 2.4   Digital ΔΣ transmitter

Fig. 2.5 depicts a transmitter based on the RF pulse-width modulation (RF-PWM) [10, 11, 14, 15].   In this architecture, the width of the pulse represents the envelope of the signal.   The phase of the pulses represents the phase information.   The RF-PWM signal is amplified with an SMPA and the spurious products caused by the switching operation is removed by a series filter (part of the OMN) after the PA.   However, the RF-PWM architecture suffers from severe switching losses when the pulse width varies. This is because the components in the OMN is designed for a certain pulse width.   If the pulse width varies along with the envelope of the signal, the deviation of the capacitance value at the switching transistor can cause significant power loss (26-35%) [10, 16].   Further, it is also difficult to encode the information accurately using the PWM.
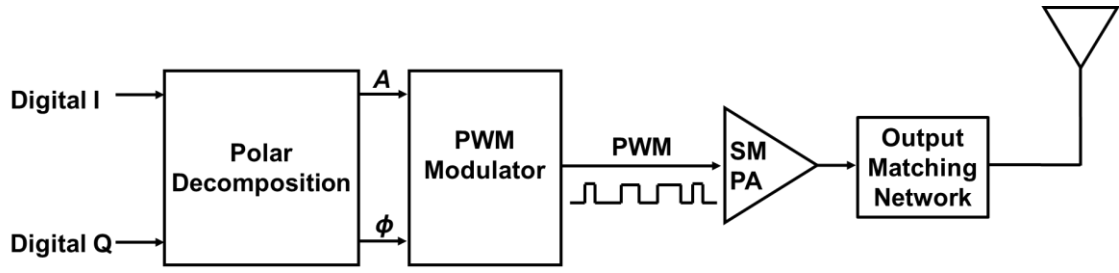
Fig. 2.5   RF-PWM transmitter

Fig. 2.6 depicts a transmitter based on the Outphasing linearization[17-19] to generate two out-of-phase RF-PWM signals for the SMPAs. This design, as in conventional Outphasing designs, must convert the differential signals into a single-ended signal for the antenna. It requires two PAs, two matching networks, and a lossy balun.   The larger area and the power loss from the extra components outweigh the advantage of mixing the phase and width data into one signal for each PA in this design.
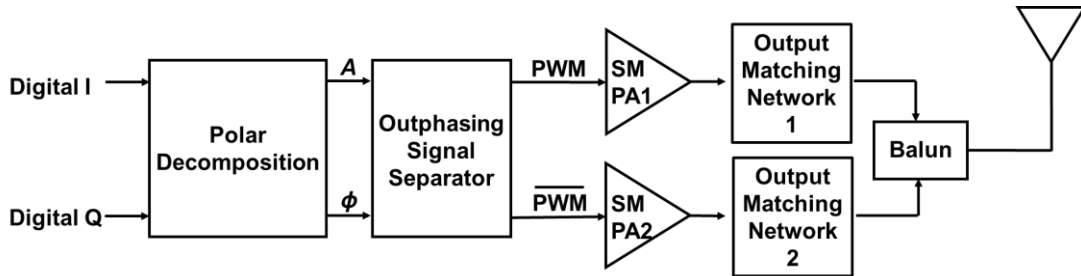
Fig. 2.6   RF-PWM Outphasing transmitter

An architecture that can alleviate the drawbacks of the transmitters above is the Polar transmitter as depicted in Fig. 2.7 [20-23]. This transmitter is based on the Polar linearization that essentially splits the otherwise variable-envelope input signal to the PA into a Phase Modulation (PM, or ϕ) signal to the PA input and an Amplitude Modulation (AM, or A) signal on the PA supply.   Thereafter, both of the signals are mixed by the PA. The ϕ signal is the RF carrier signal with its phase modulated by

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the phase information from the IQ signals, and is generated by a Phase-Locked Loop

(PLL) [4]. On the other hand, a DC-DC converter, acting as an Amplitude Modulator,

is typically needed to modulate the voltage supply to the PA, but it generally causes

>20% loss in the power-efficiency of the PA [12].
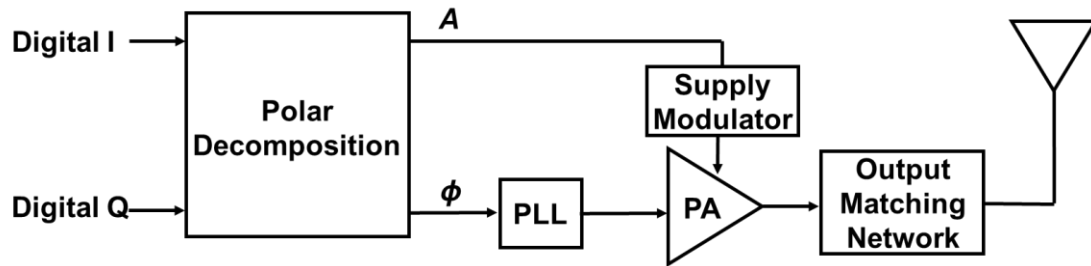
Fig. 2.7   Polar transmitter

A Polar transmitter variant with a digital AM in [24-26] circumvents the supply

modulator by employing digitally-activated switch transistors to drive the current from

the supply into multiple parallel PAs.   Similar to the supply modulator, these

transistors have to direct large power going into the PAs and can cause significant

power loss if they are not carefully designed.

Another variant in [1, 8, 27-35] performs the digital AM by directly modulating

the load impedance seen by the PA. This AM method is called dynamic load modulation

(DLM).   DLM is realized with varying the output matching network according to the

baseband signal as depicted in Fig. 2.8. The DLM PA has been successfully

demonstrated at gigahertz frequencies [33] and broadband/multi-band applications[32].

The efficiency of the DLM method is, however, limited by the losses due to the OMN

components.
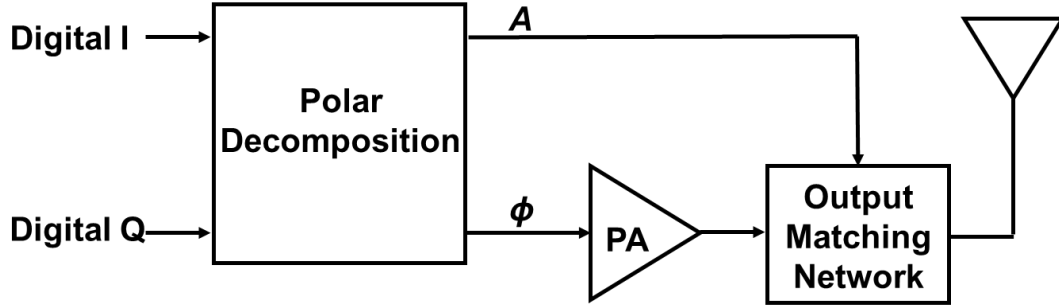
Fig. 2.8   Variant Polar transmitter with the OMN controlled by digital AM

2.3   Power Amplifier

To achieve the simultaneous low-output-power and high-power -efficiency purpose, the key point is the design of PA in the transmitter. The PA mainly determines the output power of the transmitter. Besides, it is the most power-hungry building block in the transmitter [36]. Generally, its power consumption is 50% to 70% of the whole transmitter system. Thus, the main purpose of this project is to design and realize a low-output-power and high-power-efficiency PA for WBAN device.

2.3.1   Power Amplifier Classification

PAs can be classified into two categories: linear PAs and non-linear PAs [36].

<u>Linear PAs</u>

The transistor of the linear PAs operates in the active region as a voltage-controlled current source.   The power dissipation of the transistor is proportional to the overlap time, or also denoted as the conduction angle θ, between the output voltage waveform across the transistor and the output current waveform [3, 45].   Reducing the overlap

time can greatly reduce the power dissipation. Table 2.2 compares the different

classes of linear PAs.

Table 2.2 Comparison of Class A, B, AB, and C PAs

PA Class	A	B	AB	C
θ (°)	360	180	$180 \sim 360$	$0 \sim 180$
Power Efficiency (%)	50	78.5	$50 \sim 78.5$	100
Power Capability	High	Medium	Medium	Low

The Class-A PA is biased above the threshold voltage so that the drain current is

always on during the whole period, or equivalently, θ is 360°. The drain voltage and

the drain current are both sinusoidal. The maximum drain efficiency (power

efficiency) of the Class-A PA is only 50%.

The Class-B PA is biased at the threshold voltage so that θ is 180°. Since the

PA is only active for half of a period, the drain current is a half-sinewave as illustrated

in Fig. 2.9(b). The Class-B PA is always used in a push-pull topology where two half-

sinewave drain-currents are combined into a full sinewave.

The Class-AB PA is a compromise of the Class-A PA and the Class-B PA to provide

relatively higher efficiency compared to the Class-A PA and some tolerable PA non-

linearity. θ of the Class-AB PA is from 180° to 360°. The drain efficiency (η) of the

Class-AB PA is a function of θ as follows,

$$\eta = \frac{\theta - sin\theta}{4\sin\left(\frac{\theta}{2}\right) - 2\theta\cos\left(\frac{\theta}{2}\right)} \tag{2.3}$$

The Class-C PA is biased below the threshold voltage so that θ is less than 180 °. The transistor is on only for a small fraction of the entire period as illustrated in Fig. 2.9(c). The Class-C PA obtains a higher efficiency than the aforesaid PA classes. From Eq. (2.3), η will be 100 % when θ approaches 0.
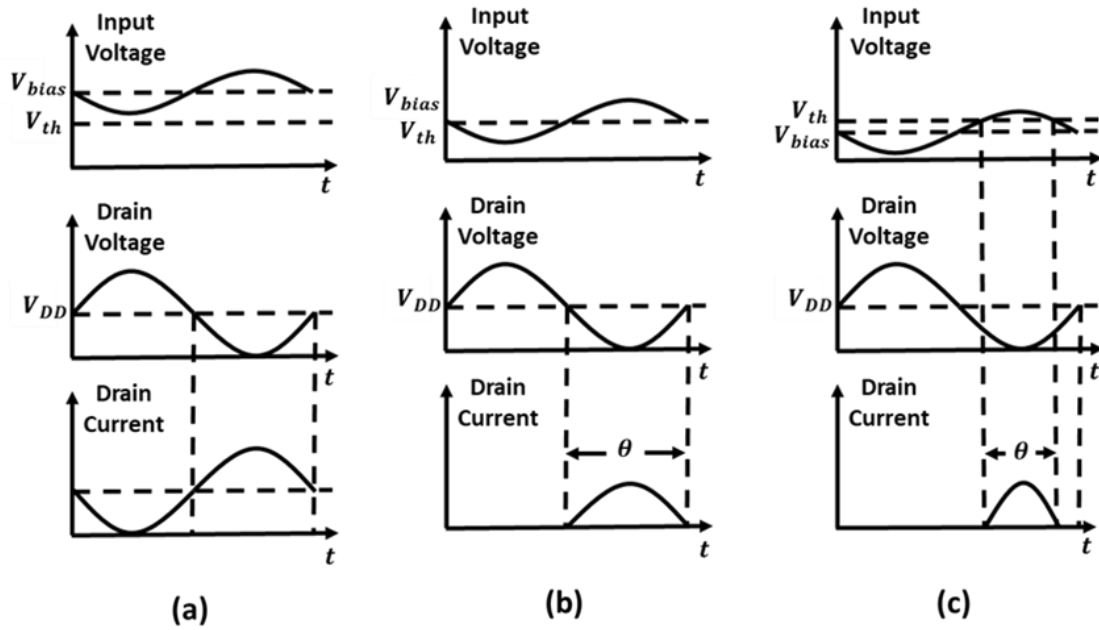
Fig. 2.9   Voltage and current waveforms for

(a) Class-A PA ($\theta= 2\pi$); (b) Class-B PA ($\theta= \pi$) and (c) Class-C PA ($0< \theta< \pi$).

Nonlinear PAs

The transistors of nonlinear PAs operate as a switch; hence, these PAs are often called as switched-mode PAs. Due to the switching operation, drain voltage and drain current, ideally, do not overlap with each other. Therefore, the power dissipation is zero, and the overall efficiency is 100% [37].

Class-D PA

The Class-D PA has two transistor switches that are driven 180 degrees out of phase, and a series resonator at the load.   Fig. 2.10 depicts the Class-D PA, and Fig. 2.11 illustrates its drain voltage and current waveforms.   Although, this PA can obtain 100% efficiency ideally; however, it is not suitable for RF operation because of the large loss caused by the output capacitance at high switching speed [36, 37].
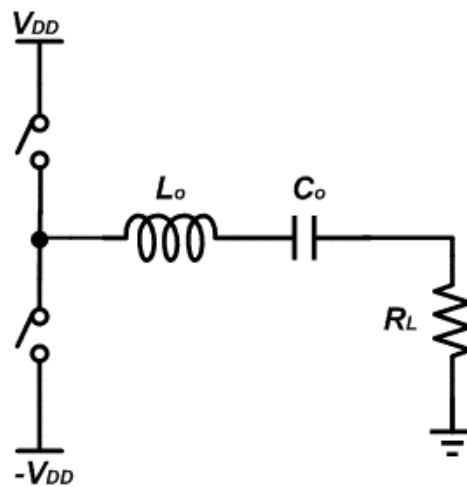
Fig. 2.10   Class-D PA
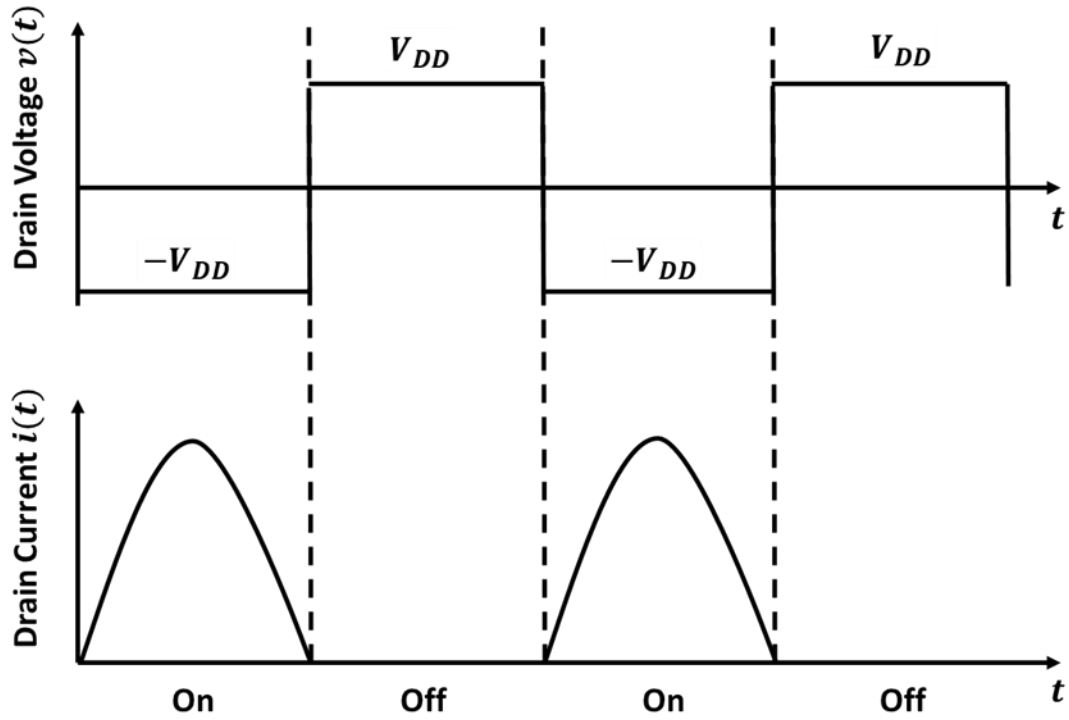
Fig. 2.11   Drain voltage and current waveforms of Class-D PA

Class E-PA

The Class-E PA consists of a switch transistor, a capacitor in parallel with the transistor, and a series resonant circuit.   Fig. 2.12 depicts the Class-E PA, and Fig. 2.13 illustrates its drain voltage and the drain current waveforms.   The drain voltage waveform is determined by the switching action and the transient response of OMN. In the Class-E PA, as illustrated in Fig. 2.13, there are two optimum switching conditions that are required for high efficiency operation [4].   They are as follows:

(1)   The Zero-Voltage-Switching (ZVS) condition: the drain voltage, $v(t)$, returns to

zero at the moment the transistor turns on.

(2)   The Zero-Voltage-Derivative-Switching (ZVDS) condition: the slope of $v(t)$, is

zero when the transistor turns on.

These two conditions ensure that there is no overlapping between the drain voltage

and the drain current, and ideally, the power efficiency is 100%.

The drawback of the Class-E PA is the peak drain voltage can be high, up to

3.56xV_{DD} and may overstress the transistor.   To mitigate this problem, transistors with

a higher breakdown voltage can be used [38], or a lower V_{DD} can be used.   Another

common method is to cascade the main transistor with an additional transistor so that

they can share the heavy the voltage stress and improve the isolation between the input

and the output [39]; however, this method may affect the linearity and the power

efficiency negatively [4, 36, 37].
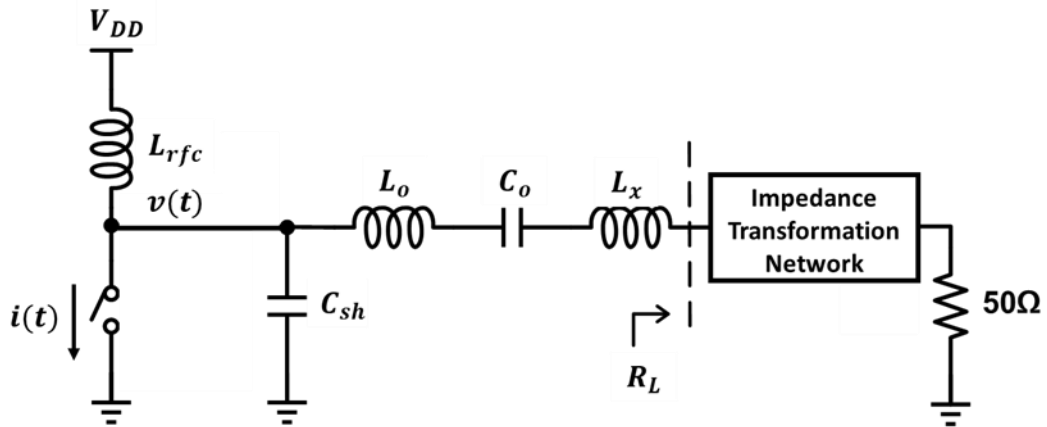
Fig. 2.12   Class-E PA
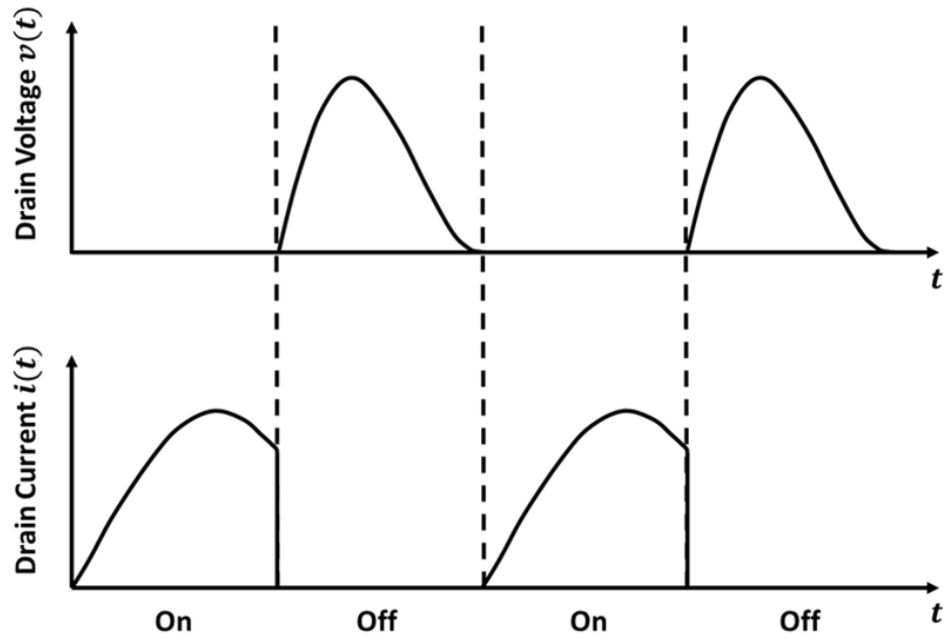
Fig. 2.13   Drain voltage and current waveforms of Class-E PA

Class-F PA

Fig. 2.14 depicts the Class-F PA.   The PA employs harmonic filters to shape the drain voltage waveform.   The odd harmonics are retained to approximate a square-wave in the drain voltage.   Fig. 2.15 illustrates the square-wave shaped drain voltage and the drain current with ideally no overlap between them.   The parallel tank, $L_o C_o$, is resonant at the fundamental frequency to filter out the harmonics and generate a sinusoidal output voltage [36, 37].
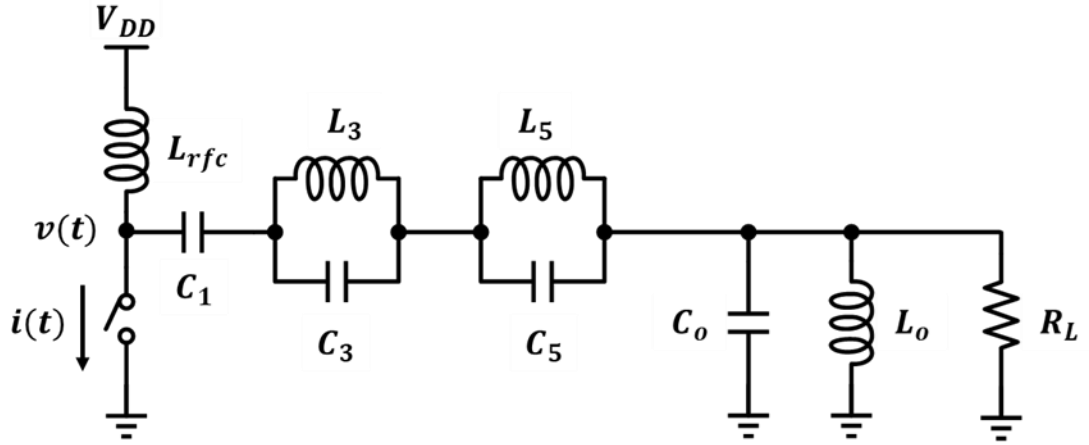
Fig. 2.14   Class-F PA
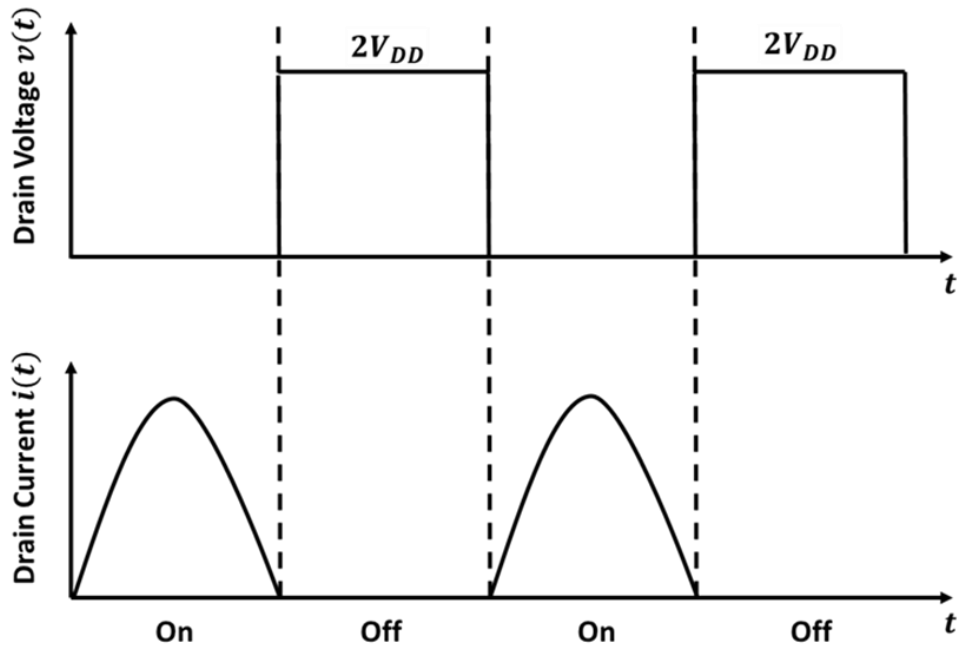
Fig. 2.15   Drain voltage and current waveforms of Class-F PA

The drawback of the Class-F PA is that the Q of the inductors in the filters are generally low, particularly in CMOS processes, and results in substantial power loss. Further, compared to the Class-E PA, the Class-F PA is more complex and involves more filters.   On the other hand, the peak drain voltage of the Class-F PA is $2 \times V_{DD}$,

and therefore, causes less stress on the transistors [37]

Based on the aforesaid discussion in this section, the Class-E PA is used for the work described later in Chapters 3. This is because the Class-E PA is more efficient than linear PAs. Compared to the Class-D PA, the parasitic capacitance of the transistor can be absorbed into the shunt capacitor of the Class-E PA so that the power dissipation related to the operating frequency can be reduced dramatically. Compared to the Class-F PA, the Class-E PA requires a less complex passive network that costs smaller area and lower power [1, 4, 36, 37].

2.3.2   Class-E PA Design Considerations

The high power efficiency of Class-E PAs has spurred many research interests on the design and analysis of Class-E PAs [11, 40, 41]. As mentioned earlier, the optimum condition of the Class-E PA has two switching conditions: ZVS and ZVDS. The ZVS condition is required to prevent losses due to discharge of the shunt capacitor C_{sh} at off-to-on switching instances, while the ZVDS condition is meant to avoid a high drain current flowing through the transistor during the off-to-on transitions [42]. Both two conditions make sure that the Class-E PA can provide 100% power efficiency theoretically [4, 36, 37].

In the case where the inductor L_{rfc} has an ideally infinite value, the waveform of the drain voltage $v(t)$ is determined by R_L, L_x and C_{sh}. To satisfy the ZVS and ZVDS conditions, the output matching network components can be calculated based on the required output power with the three following assumptions:

1. The switch is ideal with zero on-resistance and infinite off-resistance;

2. The RF choke has sufficiently large value such that the current flowing through it is approximately constant; and

3. The filter has sufficiently large Q such that the current flowing through the load resistance is pure sinusoidal.

The formulas used for calculation are listed as below [42].

$$R_L = 0.577 \frac{V_{DD}^2}{P_{out}} \tag{2.4}$$

$$L_x = 1.15 \frac{R_L}{\omega_c} \tag{2.5}$$

$$C_{sh} = \frac{0.1836}{R_L \omega_c} \tag{2.6}$$

From the derivation process of these formulas, we can understand that the components in the output matching network of the Class-E PA is not designed for the S-parameter matching, as in the design of the linear PAs, but for satisfying the two switching conditions: ZVS and ZVDS.

A variant of the Class-E PA only satisfies the ZVS condition but sacrifices the ZVDS condition. In [40, 42], authors have clearly proved that the importance of the ZVS condition over the ZVDS condition for low switching losses. The condition where the Class-E PA only satisfied ZVS condition is called sub-optimum condition. This variant of Class-E PA is still able to satisfy 100% power efficiency in the ideal case. Simultaneously, the maximum drain voltage decreases to 2.5 VDD, which relaxes the stress for the switch transistor and provides the flexibility for the design of the Class-E

PA [40].

Besides, another variant of the Class-E PA uses finite DC feed instead of RF choke [41]. The RF choke is able to maintain the DC biasing. Design equations for the Class-E PA with RF choke have been presented comprehensively in [42] and [43]. However, the RF choke in the Class-E PA will limit the maximum operating frequency and the design flexibility [41]. Using a finite DC feed in a Class-E PA can improve the power efficiency by 30% compared to the Class-E PA with RF choke [41]. The generalized design methodologies for the Class-E with finite DC feed inductance are presented in [41], [44] and [45]. It is worthwhile to note that the excess reactance, Z_x, in the Class-E PA with finite feed inductance can be either capacitive or inductive, depending on the desired output power level and the DC feed inductor [41]. In the case with finite DC feed, the waveform of the drain voltage is determined by the L_{rf}, Z_x, C_{sh} and R_L.

In [11], the design equations for sub-optimum Class-E PAs with finite feed at arbitrary duty cycle are presented. The analysis indicates the existence of infinitely many design equations. We can preserve one of the switching conditions when only two of the four components are varied, which has been proved in [11]. This provides a possibility of designing different types of digitally-controlled OMNs.

The output power of a Class-E PA can be determined as follows

$$P_{out} \propto \frac{V_{DD}^2}{R_L} \tag{2.7}$$

From Eqn. (2.7), we can observe that R_L is required to be smaller than 50 Ω for high-output-power applications [38, 46-48], and comparable to or even high than 50 Ω

for lower-output-power applications. R_L can affect the power efficiency in certain ways.

Many existing Class-E designs managed to realize a finite DC feed on-chip without sacrificing the efficiency. The reactance of the finite DC feed in those designs are much higher than R_L[49]. This requirement is easily satisfied in the designs for high output power, which have small R_L. However, for low output power designs with large R_L, a typically large inductor is required to be implemented on-chip. Furthermore, the Class-E PA, as a nonlinear PA, requires a good-performance filter. The inductance value of the series filter is proportional to R_L. For larger harmonic rejection, a large inductor is required. Besides, the authors stated that the power consumed by the impedance transformation network was 1.5 times of that consumed by the active devices in [50]. The value of the series inductor in the impedance transformation network is also proportional to R_L. This indicates that low-power applications, where the R_L is high, require a large inductor. Large inductors usually have poor Q. This leads to the low power efficiency of the PAs designed for low output power when fully integrated [50].

To solve the aforesaid three conditions, we need to make R_L as low as possible. Furthermore, we can utilize high-Q off-chip inductors to improve the power efficiency as well.   In [51-53], it has been proved that Class-E PA is feasible for low-output-power applications.

2.3.3   Review of Class-E PA Variants

Several variants of Class-E PAs exist.   In this section, the two prevalent variants — parallel-circuit Class-E PAs and even-harmonic Class-E PAs — will be reviewed. Subsequently, the effects of non-ideal components on the Class-E PA performance will be discussed.

2.3.3.1   Parallel-Circuit Class-E PAs

Fig. 2.16 depicts a typical configuration of the parallel-circuit Class-E PA [37].   This PA obviates the need for the excess inductor, typically used in other variants of Class-E PAs.   The output power and the centre frequency of the PA are determined by the parallel circuit, tuned to the centre frequency, that comprises the load impedance R_L, the shunt capacitor C_{sh}, and the finite DC feed L.   The maximum drain voltage of the transistor is at 3.65 V_{DD}, and this is higher than other Class-E variants and is undesirable as it may require a more expensive fabrication option (if it is supported by the process technology), or a more complex cascode topology to relax the drain voltage.
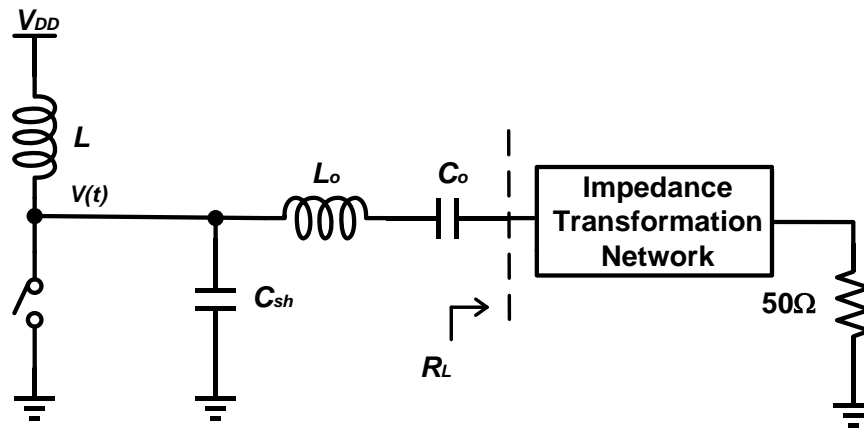
(a)
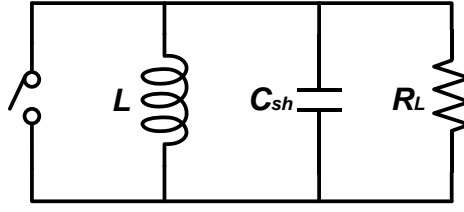
(b)

Fig. 2.16 (a) Parallel-Circuit Class-E PA

(b) Equivalent circuit of Parallel-Circuit Class-E PA

2.3.3.2 Even-Harmonic Class-E PAs

Fig. 2.17 depicts a typical configuration of the even-harmonic Class-E PA [37]. In this PA, the finite DC feed, L, and the shunt capacitor, C_{sh}, are tuned to resonate at any even-harmonic frequency. The even harmonics are retained to approximate a square-wave in the drain current. Therefore, the Even-Harmonic Class-E PA has lower power loss during the switching transition duration. Compared to other Class-E variants, an additional series capacitor C_x is required to compensate for the phase shift caused by the excess inductive reactance. Further, the drain current of the transistor reaches a peak value of four times as high as the DC current, at the end of the conduction interval. This large peak drain current may cause the breakdown of the transistor. The main problem of the Even-Harmonic Class-E PA is a substantially small value of the load impedance, R_L, which is over an order of magnitude smaller than for other variants. This will be a challenge to design the suitable impedance transformation network.
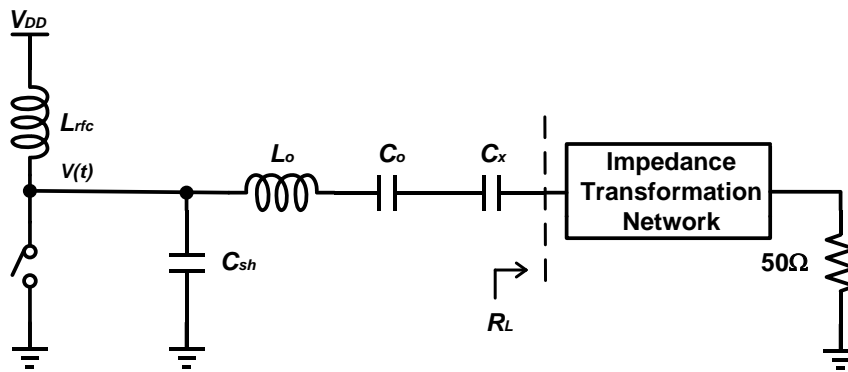
Fig. 2.17 Even-Harmonic Class-E PA

2.3.4   Effects of Non-Idealities

The discussion on the Class-E PAs so far assumes ideal components.   The significant non-idealities and their effects on the performance are now described as follows:

2.3.4.1   On-resistance of the switch

The on-resistance of the switch, R_{on}, increases the drain voltage to be above zero. The drain current will flow through the switch and cause power loss.   The power efficiency of the Class-E PA with the on-resistance considered is estimated as [37]

$$\eta \approx \frac{R}{R + 1.536\,R_{on}} \tag{2.8}$$

where R is the load resistance.

2.3.4.2   Non-zero switching transition time

During the off-to-on switching transition time, both the drain voltage and the drain current of the switch and the consequent power loss are very small.   On the other hand, the power loss during the on-to-off transition is somewhat considerable and can be estimated by integrating the product of the drain voltage and current as follows [37]

$$P_{loss} = \frac{1}{12} t_{on-off}^2 P_o \tag{2.9}$$

where P_o is the output power.

2.3.4.3 Finite Q of the passive components

The parasitic resistance of the series filter in the traditional Class-E PA, due to the finite Q of each component, can be lumped as an effective series resistance with the load that alters the total resistance value as seen by the PA, as shown in Fig. 2.18. Consequently, the optimum conditions of the traditional Class-E PA will not be satisfied. The power efficiency will be degraded.   On the other hand, the parasitic resistance, R_p, of the finite DC feed will make the effective value of V_{DD} lower than

the nominal V_{DD}, thereby degrading the output of the Class-E PA, as shown in Fig. 2.19.
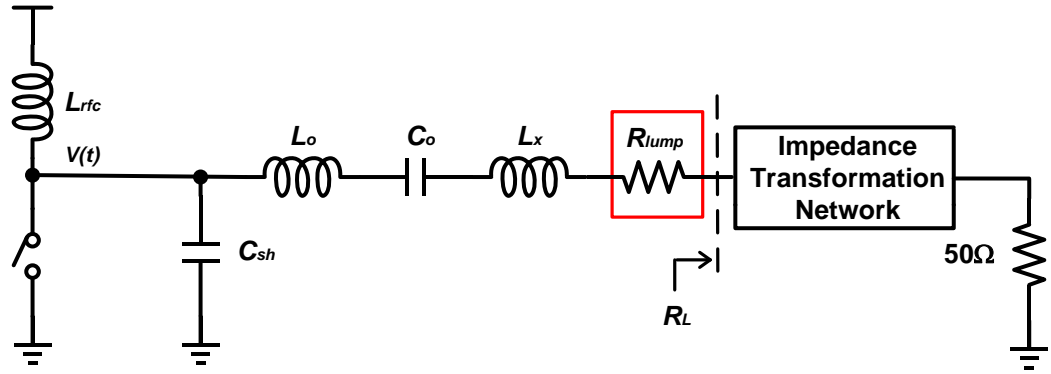
Fig. 2.18 The Class-E PA with the lumped parasitic resistance
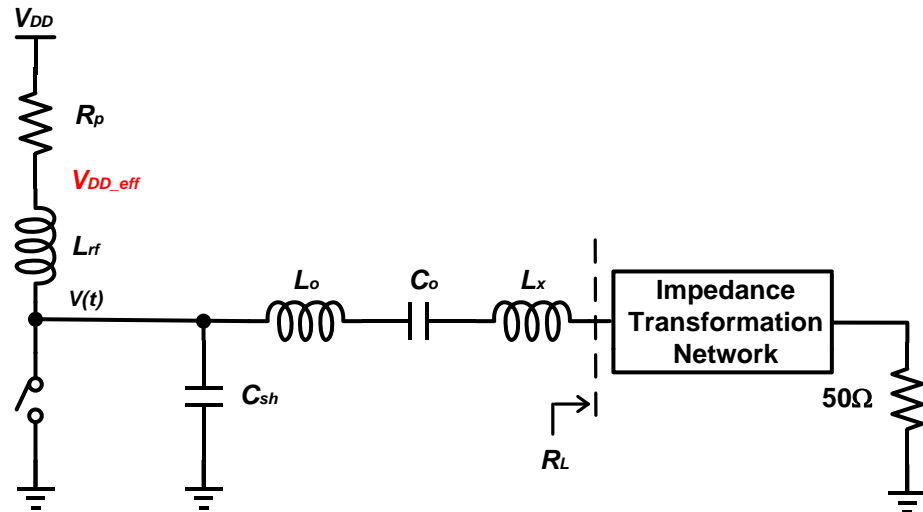
Fig. 2.19 The Class-E PA with the parasitic resistance of the finite DC feed

2.4   On-chip Inductors and Bond-wire Inductors

In CMOS process, the low-Q on-chip inductor in the input and output matching networks for the fully integrated PA design is one of the critical components which cause major power loss and limit the PA performance. The on-chip inductors suffer

from the losses of the metal trace and the substrate in standard CMOS technology [54]. The low-Q on-chip inductor reduces the power efficiency of PA and it is not desired in the context of the low-output-power and high-power-efficiency application. Therefore, high-Q inductor is the key component in the proposed design.

In 2013, KC Lin and HK Chiou have presented a CMOS PA using high-Q bond-wire inductor. The proposed 2.75 nH inductor achieves a Q of 18, which is three times as much as that of a conventional CMOS standard spiral inductor at 2.4 GHz [58]. The Q of the inductor is over 15 from 2 to 14 GHz [58]. Thus, the bond-wire inductor can be used for various applications with different frequency requirements. The power efficiency of the PA with the bond-wire inductor is enhanced by 7% as compared with those with on-chip inductor [58].

The Q of on-chip spiral inductors is lower than that of bond-wire inductors.   This can be attributed to the small track size of on-chip spiral inductors, and the penetration of the electric filed and the magnetic flux into the CMOS [58].

The bond-wire is always used for connecting the chip to the board thus we can utilize the bond-wire to provide the required inductance value in the input and output matching network. This can not only reduce the effect of extra inductance value produced by the bond-wire, provide high-Q inductor also save the silicon area. Some previously published papers have utilized the bond-wires as inductors in RF circuits, such as low-noise amplifiers [60, 61], and voltage-controlled oscillators [62, 63].

The main drawback of the bond-wire inductors is its manufacture accuracy. The

inductance is determined by its dimension, adjacent wires, and wire bending shape [58]. As in [67], the authors proposed to use the pad distance to control the wire length and reduce the manufacturing error.

2.5   Conclusions

In this chapter, we have provided an overall review on the WBAN standard. We also have presented various transmitter architectures and different types of PA. Among them, the variant Polar architecture, whose AM signal controls the OMN, can generate a variable-envelope output signal and has a high efficiency. The Class-E PA is popular with high power efficiency. Its variant type with finite DC feed value and sub-optimum condition provide the flexibility for the design of the Class-E PA. It is also suitable for low-output power applications. Bond-wire inductors have higher Q and reduced silicon area, compared to the on-chip spiral inductors. Based on the literature review, we determine to utilize the Polar architecture with Class-E PA. The AM signal in the Polar architecture is used to control the variable OMN. In short, there is a need for a novel matching network that can mitigate the loss of the on-chip inductors, while at the same time, is able to vary its component values by digital means so that it can perform the AM for PAs in digital Polar transmitter applications.

Chapter 3

THE CLASS-E PA WITH A DIGITALLY-CONTROLLED OUTPUT MATCHING NETWORK

3.1   Introduction

In Chapter 1, it was discussed that conventional Polar transmitters requires a supply modulator to perform the AM by modulating the voltage supply to the PA.   Since the supply modulator can cause considerable power loss, it is desirable to circumvent the supply modulator and perform the AM directly by modulating the load impedance seen by the PA.   This can be done using the DLM technique [7, 8], and is done by varying the OMN according to the AM signal.   Nonetheless, the on-chip inductors of the OMN can still cause significant power loss.   Further, for Polar transmitters with digital inputs, it would be desirable if these digital inputs could directly control the variable OMN.   There is an impetus for a variable OMN that can mitigate the loss of the on-chip inductors and is able to vary its component values by digital means.

In this chapter, a Class-E PA employing a novel digitally-controlled variable OMN is proposed.   The PA is designed so that the ZVS condition can be achieved for high-efficiency operation.   The OMN performs the DLM and is controlled/varied directly by the digital AM input signal without any need for the conventional supply modulator, thereby saving area and power dissipation.   Further, unlike the transistors in the supply modulator that have to handle a large current, the transistors employed by

the OMN are small low-power digital transistors. The OMN architecture design allows the use of on-chip inductors, as well as off-chip inductors including high-Q bond-wires to improve the efficiency. A state-of-the-art PA with a digitally-controlled variable OMN based on [7] is also designed, and will be used as a reference/benchmark PA for the proposed PA.

This chapter is organized as follows. First, the simplified schematics of both PAs are presented. Thereafter, the design equations for both PAs are provided, and the relationship between the performance of PAs and the design variables is discussed. Finally, the implementation procedures for both PAs are presented.

3.2   The Simplified Schematics of the Class-E PAs

3.2.1   The Simplified Schematic of the Reference PA

Fig. 3.1 shows the simplified schematic of the reference Class-E PA. As shown in Fig. 3.1(a), C_{sh} can be regarded as the shunt capacitor in the conventional Class-E PA. It dominantly determines the waveform of the drain voltage of the transistor. C_{sh} remains static during operation. L_x is a fixed inductor and it is the excess inductor which is required in the conventional Class-E PA for phase shifting. C_0 and L_0 form a series resonator and filter out the harmonics. After the series resonator, there is a L-type impedance transformation network which transforms the 50 Ω to the required load impedance. The impedance transformation network consists of L_1 and C_1. C_1 is a variable capacitor and it is the critical role to vary the load impedance seen by the PA

based on the output power level. The range of C_1 determines the tuning range of R_L, and accordingly, the dynamic range of the PA. Fig. 3.1(b) depicts the schematic of the reference PA after the inductors $L_x, L_0,$ and L_1 are merged into L_3. However, as only C_1 varies, R_L will have extra reactance which incurs power loss. Besides, as mentioned in Section 2.3.2, although the output power is varied with the load impedance, the drain voltage waveform is distorted with C_{sh} and L_x unchanged. The distorted drain voltage waveform will incur power loss during operation. L_3 is an on-chip inductor, and it will limit the power efficiency as well.
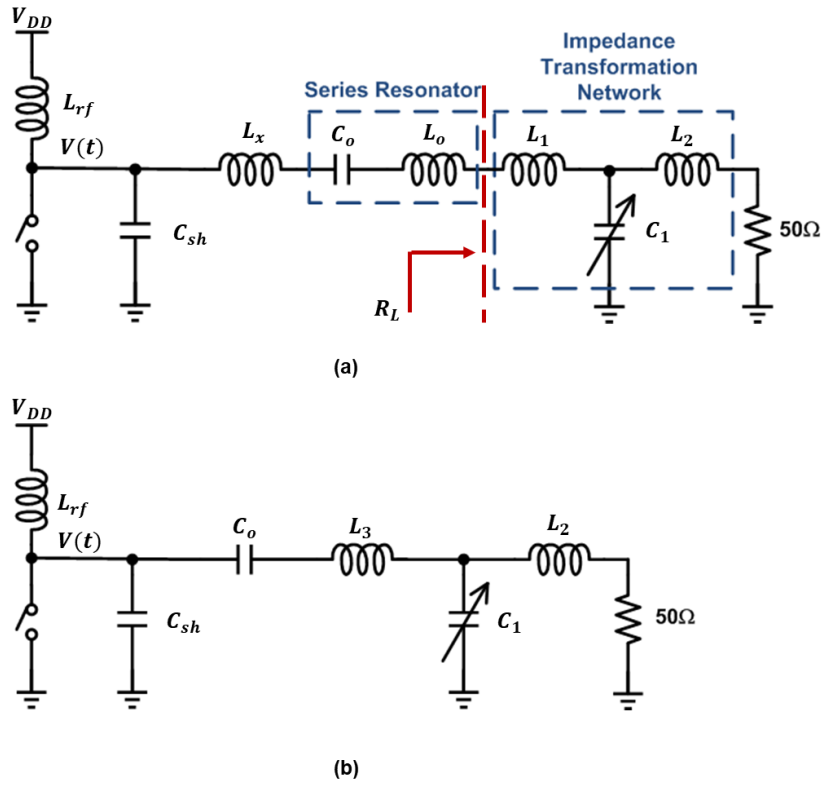
Fig. 3.1 **The simplified schematic of the reference Class-E PA (a) before merging of the inductors and (b) after merging of the inductors**

3.2.2   The Simplified Schematic of the Proposed PA

Fig. 3.2 presents the simplified schematic of the proposed Class-E PA. Compared to the reference PA, we set the R_L of the proposed PA as fixed 50 Ω such that we can avoid the use of an impedance transformation network. The avoidance of the impedance transformation network saves the silicon area and reduces power loss. Besides, without the impedance transformation network, the OMN can use the high-Q bond-wire to realize the inductors. Thus, the proposed PA can improve the power efficiency without the need for the impedance transformation network.

In the proposed OMN, we choose to vary two components, C_{sh} and L_x, in the OMN to generate the variable-envelope output signal. The variation of two components in the OMN can make sure the ZVS condition satisfied and achieve sub-optimum status. As the variable inductor is difficult to be implemented on-chip, we realize it with a variable capacitor, C_1, and a fixed inductor, L_1. The variable capacitor and the fixed inductor can be combined with the series filter as well, as shown in Fig. 3.2. Compared to the reference PA, the proposed PA has fewer components in the OMN and is able to be realized with bond-wire inductors. The value of C_{sh} and L_x will be determined in Section 3.2.
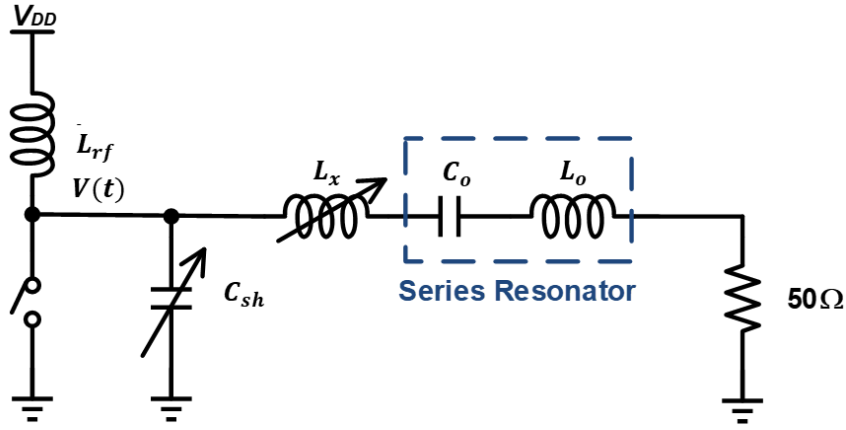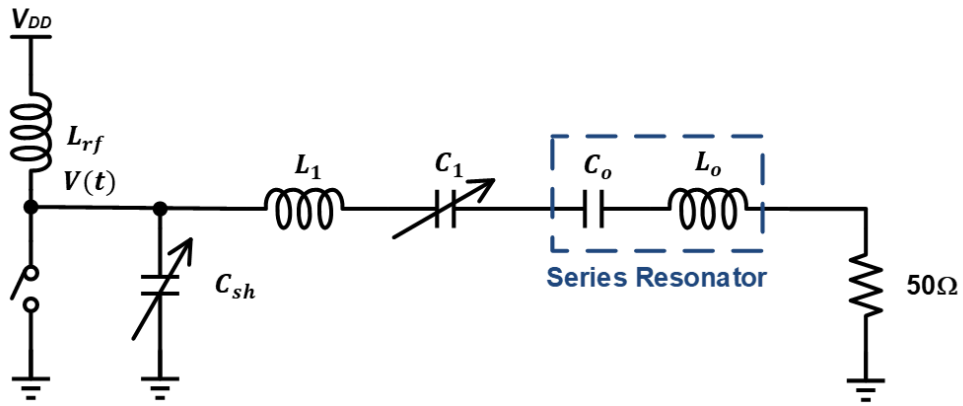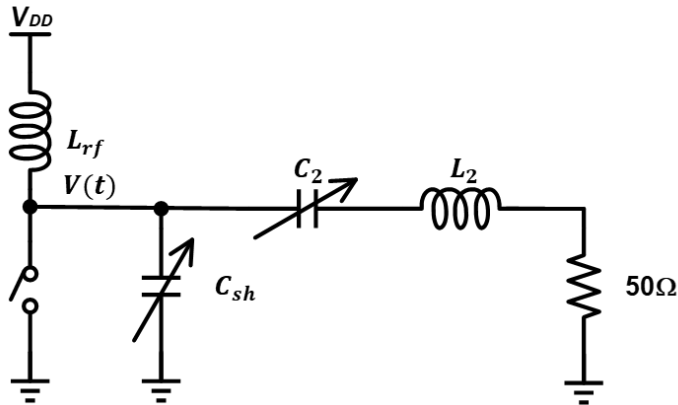
Fig. 3.2   The simplified schematic of the proposed PA: (a) with the variable inductor, (b) with the variable capacitor and the fixed inductor, and (c) after components merging

3.3   Analysis of the Class-E PA Designs

In this section, we provide the calculation equations for both designs.

In [11], Mustafa O. has presented the design equations for sub-optimum Class-E PAs with finite DC feed at arbitrary duty cycle. They defined the design set specified as follows. L is the finite DC feed, C represent the shunt capacitor, X is the excess reactance, and R is the load impedance.

$$K_L = \frac{\omega_o L}{R}, K_C = \omega_o CR, K_X = \frac{X}{R}, K_P = \frac{P_{out}R}{V_{DD}{}^2} \tag{3.1}$$

The derivation of equations is based on the following assumptions:

- The transistor is considered as an ideal switch, which has zero on-resistance and infinitely large off-resistance;

- The load resistance R (50 Ω) is the only component dissipating power in the circuit, which means the DC power is 100% transferred into RF power;

- The waveform of the current flowing through the load is pure sinusoidal due to the high-Q of the output matching network.

The authors have expressed the elements of K in terms of (d, q, k). By definition, d is the duty ratio and varies in the range (0,1), q is defined as a real positive design variable, and k represents the slope of the drain voltage at the instance of switching on and can be any real number.

The expression of each element is listed below.

$$K_L = \frac{\frac{\pi}{2}\rho^2}{\pi d\left(\pi d + \frac{k}{q^2} - \rho\sin(\varphi)\right) + \rho\sin(\pi d)\sin(\pi d + \varphi)} \tag{3.2}$$

$$K_C(d,q,k) = \frac{1}{q^2 K_L(d,q,k)} \tag{3.3}$$

$$K_X(d,q,k) = \frac{V_X}{V_R} \tag{3.4}$$

$$K_P(d,q,k) = \frac{\rho^2}{2K_L(d,q,k)^2} \tag{3.5}$$

In these expressions, the alphabets ρ, φ, V_X and V_R are also dependent only on d, q and k.

3.3.1   Analysis of the Reference PA Design

Combining Eqn. (3.2) and the expression of $K_L = \frac{\omega_o L}{R}$, we can get

$$\frac{\rho^2 V_{DD}{}^2}{2\omega_o L P_{out}} = \frac{\frac{\pi}{2}\rho^2}{\pi d\left(\pi d + \frac{k}{q^2} - \rho\sin(\varphi)\right) + \rho\sin(\pi d)\sin(\pi d + \varphi)} \tag{3.6}$$

We take $d = 0.5$. This has been proved that the power efficiency is the highest when the duty cycle is half of the period [64]. Eqn. (3.6) can be rewritten as

$$\frac{2\omega_o L}{V_{DD}{}^2} = \frac{\frac{\pi}{2} + \frac{k}{q^2} - \rho\sin(\varphi) + \rho\frac{2}{\pi}\cos\varphi}{P_{out}} \tag{3.7}$$

Let $f(k,q) = \frac{\pi}{2} + \frac{k}{q^2} - \rho\sin(\varphi) + \rho\frac{2}{\pi}\cos\varphi$

As $\omega_o, L, and\ V_{DD}$ are constant, the ratio remains constant with various values of k and q, assuming the constant is

$$\frac{2\omega L}{V_{DD}{}^2} = \frac{f(k,q)}{P_{OUT}} = \alpha \tag{3.8}$$

This is one of the two constraints to determine the values of k, q. The other is the

excessive inductor value. For the sake of less complexity, we choose the excessive

inductor as zero to reduce the on-chip inductor value thus

$$K_X(k, q) = 0 \tag{3.9}$$

Based on the two conditions above, we can find a series of constant corresponding

to a certain P_{out}. During calculation, we can observe that the range of $f(k, q)$ has a

maximum value 2.7. The range of $f(k, q)$ limits the dynamic range of the output

power which can be achieved.

The design procedure of the reference PA is summarized as below.
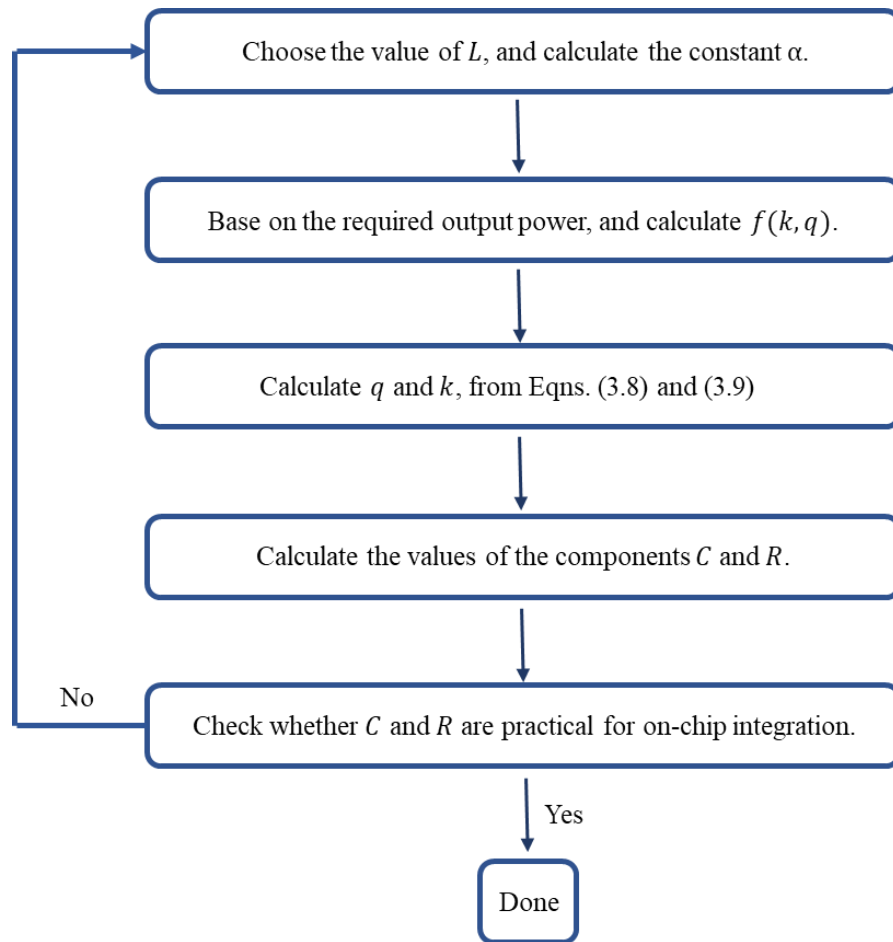
Fig. 3.3   The design procedure of the reference Class-E PA

Fig. 3.4 depicts the output power versus k with different values of L. From Fig. 3.4, we can observe that the output power increases with the increasing slope of the drain voltage at the instance of switching-on. Since the smaller inductance value of finite DC feed, L, has higher output power, we should employ the smallest practical inductance value of L. The dynamic range of the output power does not have obvious variation for different L values and it is ~10 dB.
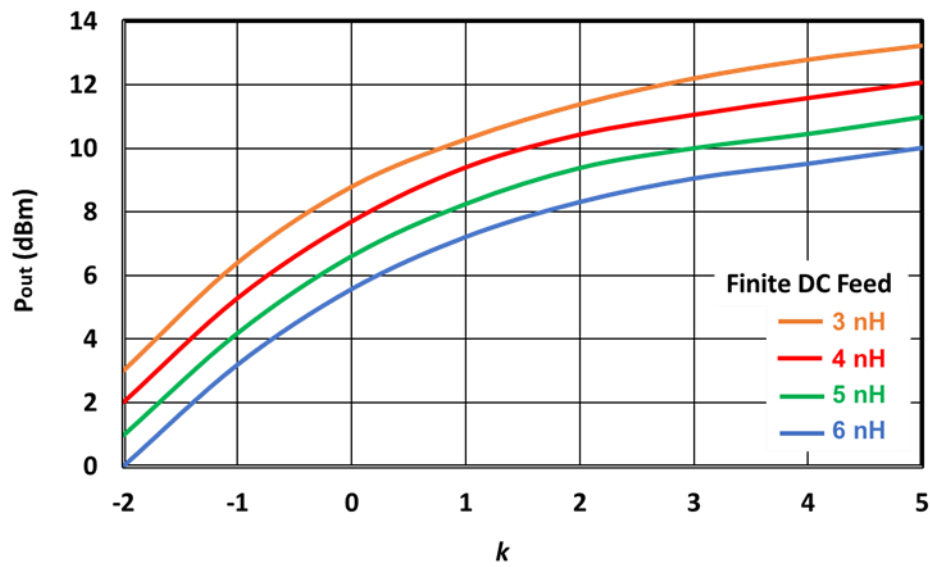
Fig. 3.4   The output power versus k for the reference PA design

Figs. 3.5 depicts the relationship between k and the OMN components of the reference PA, for different DC feed inductance values. The chosen value of the DC feed should be the smallest inductance value for practical implementation reasons. From Fig. 3.5(b), it can be observed that 4 nH is the smallest DC feed that can be utilized for the reference PA to satisfy the required load range from 55 Ω to 485 Ω. Based on the R value, we can design the impedance transformation network such that the R_L seen by the PA has least imaginary impedance and close to the required load impedance. We

determine the value of C_1 in the impedance transformation network, which is 0 pF to 5.1 pF. The C has a range from 1.86 pF to 2.63 pF. However, the reference PA does not vary it with different output power.
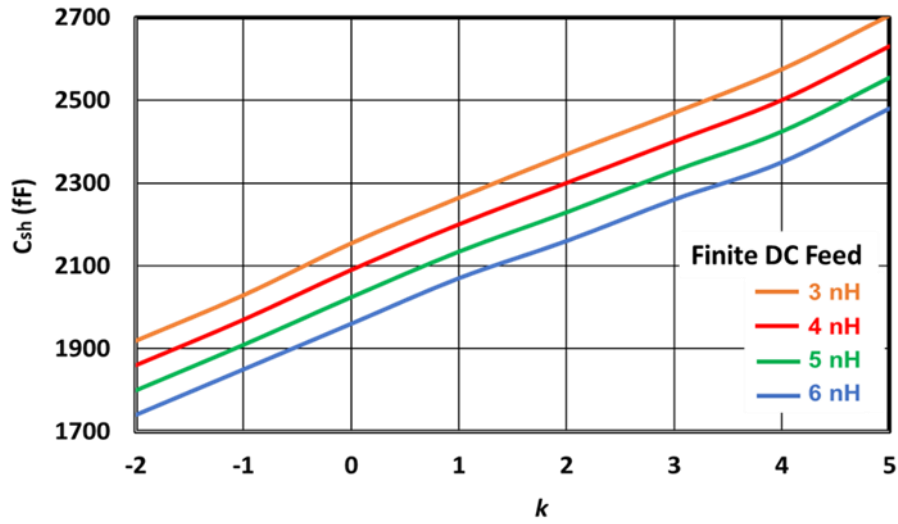
(a)
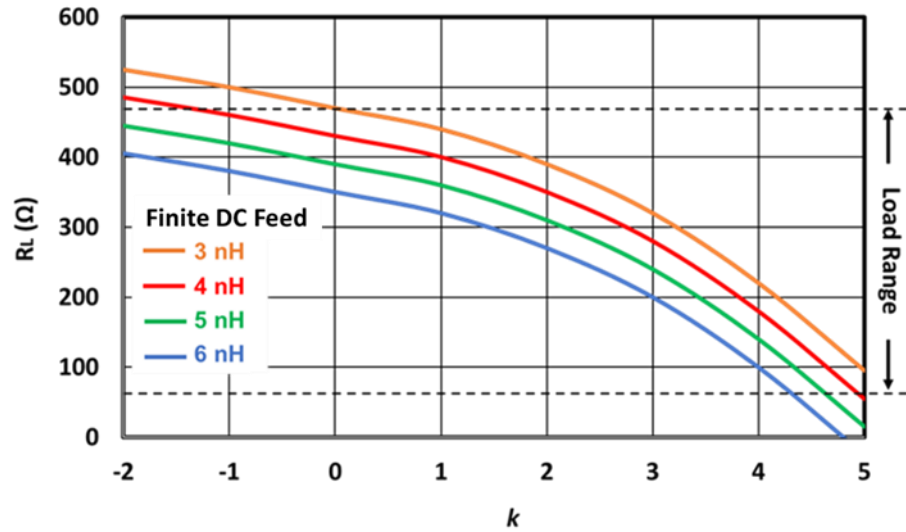
(b)

Fig. 3.5   Reference design: (a) C_{sh} capacitor versus k;
(b) R_L versus k.

Figs. 3.6 depicts the plots of the OMN components versus the P_{out} of the reference PA.

From Fig. 3.6, it can be observed that to obtain max P_{out} = 12 dBm for the reference PA, C_{sh} = 2.65 pF and R_L = 55 Ω are required.
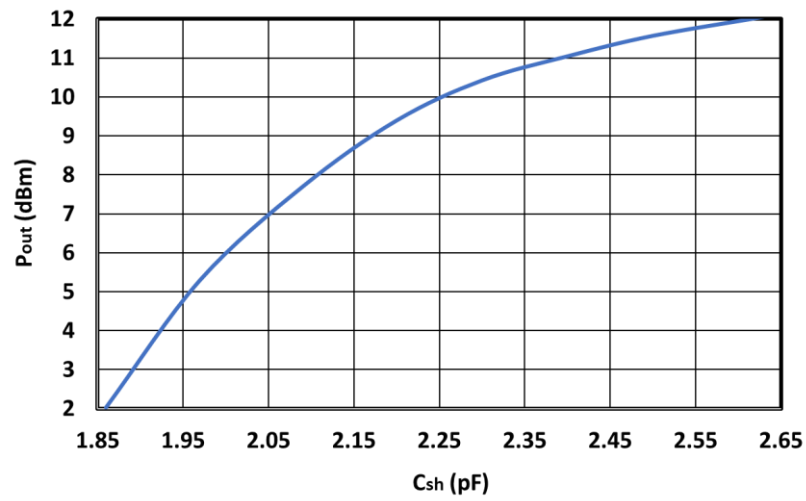
(a)
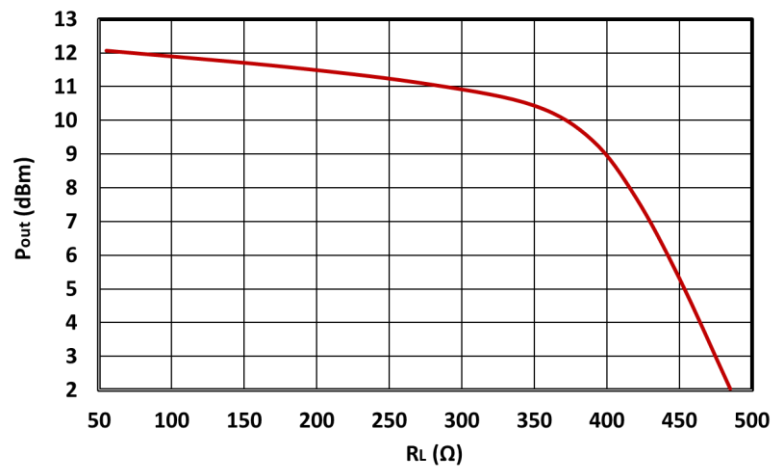
(b)

Fig. 3.6   Reference design: (a) output power versus shunt capacitor; (b) output power versus load impedance.

Fig. 3.7 depicts the optimum load impedance loci of the reference OMN that are obtained by means of analytical results (using design equations) and of simulation results. The locus obtained by simulation results somewhat agrees with that obtained by the analytical results. The small deviation represents the extra reactance and will

cause power efficiency loss.

— (a) Optimum load impedance locus obtained by analytical results
• (b) Optimum load impedance locus obtained by simulation results
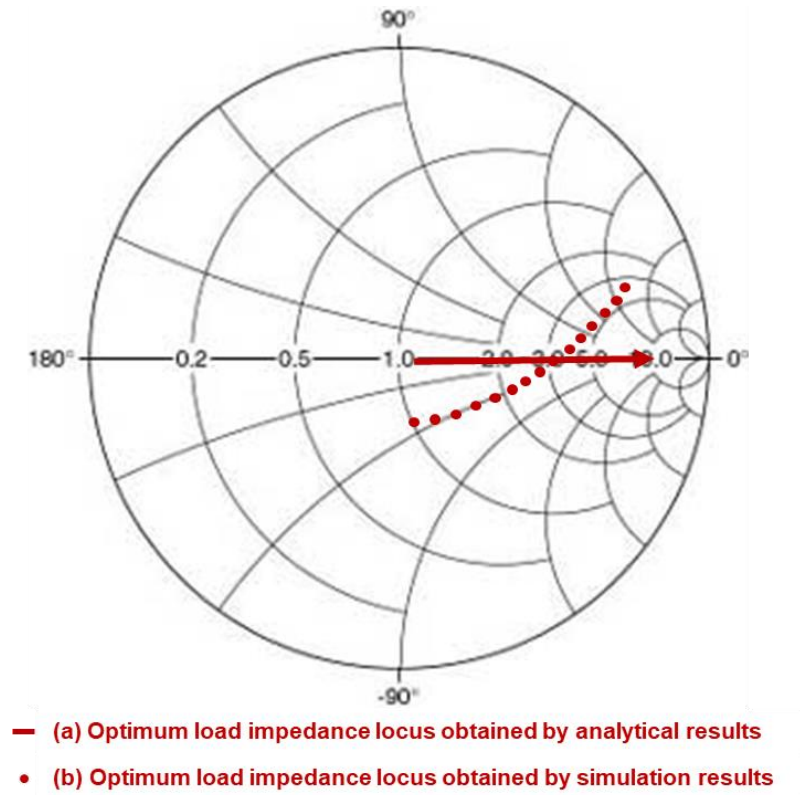
**Fig. 3.7   Optimum load impedance loci obtained by analytical results,
and by simulation results**

The drain voltage is shown in Fig.3.8 for maximum output power and minimum output power cases. The achievable minimum and maximum output power is 2 dBm and 12 dBm separately. The dynamic range is 10 dB. The current is 73 mA for maximum value. The average power efficiency is calculated as 89%. The power loss is caused by the load impedance deviation from the optimum value.
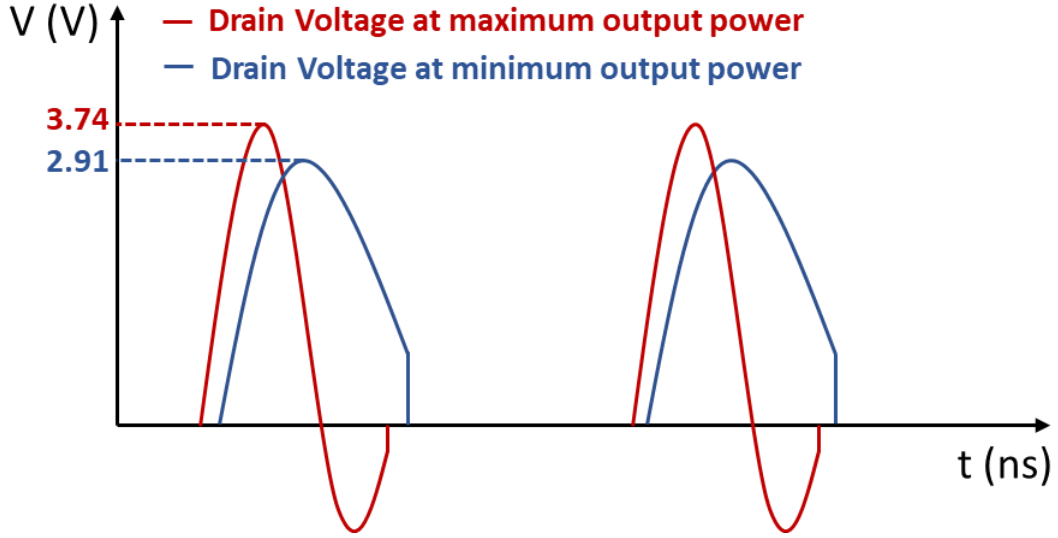
Fig. 3.8 **The drain voltage waveform of the reference PA using ideal component models**

3.3.2 Analysis of the Proposed PA Design

For our proposed PA, we define the duty cycle d as 0.5. This has been proved that the power efficiency is the highest when the duty cycle is half of the period [64]. Then we set the load impedance equal to the antenna impedance 50 Ω.

From the definition of $K_L = \frac{\omega_o L}{R}$, we can obtain that K_L become a constant, assuming it is α, under the assumption that the operating frequency and the DC feed inductor are fixed. Then we can get an equation with two variables q and k from Eqn. (3.2).

$$\frac{\frac{\pi}{2}\rho^2}{\pi d\left(\pi d + \frac{k}{q^2} - \rho\sin(\varphi)\right) + \rho\sin(\pi d)\sin(\pi d + \varphi)} = constant\ \alpha \quad (3.10)$$

From the definition of $K_P = \frac{P_{out}R}{V_{DD}^2}$, we can calculate the value of K_P with the value of the required output power. From Eqn. (3.5), we can calculate the value of ρ.

As specified in [11], ρ is a function of q and k. Therefore, we can get another equation regarding to q and k.

$$\rho = f(q, k) \tag{3.11}$$

So far, we can solve the equations and get the expression of q and k. From Eqn. (3.1), we can calculate the value of the shunt capacitor and the excess component. The design procedure of the proposed PA is summarized as below.

Choose the value of L, and calculate the constant α.

Base on the required output power, and calculate ρ.

Calculate q and k, from Eqns. (3.10) and (3.11)

Calculate the values of the components C and X.

No

Check whether C and X are practical for on-chip integration.

Yes

Done
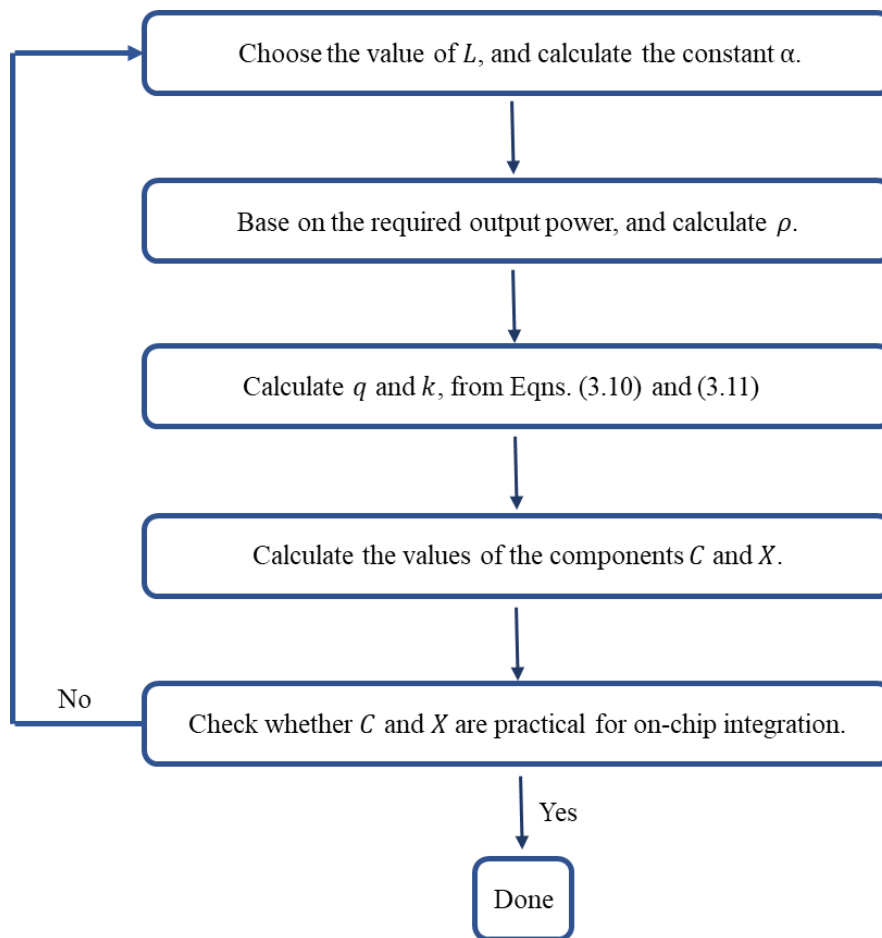
Fig. 3.9   The design procedure of the proposed Class-E PA

Fig. 3.10 depicts the output power versus k with different values of L. From Fig. 3.10, we can observe that the output power increases with the increasing slope of the

drain voltage at the instance of switching-on. Since the smaller inductance value of finite DC feed, L, has higher output power, we should employ the smallest practical inductance value of L. But the change in the dynamic range is not obvious. The dynamic range is about 7.3 dB for different values of the L.
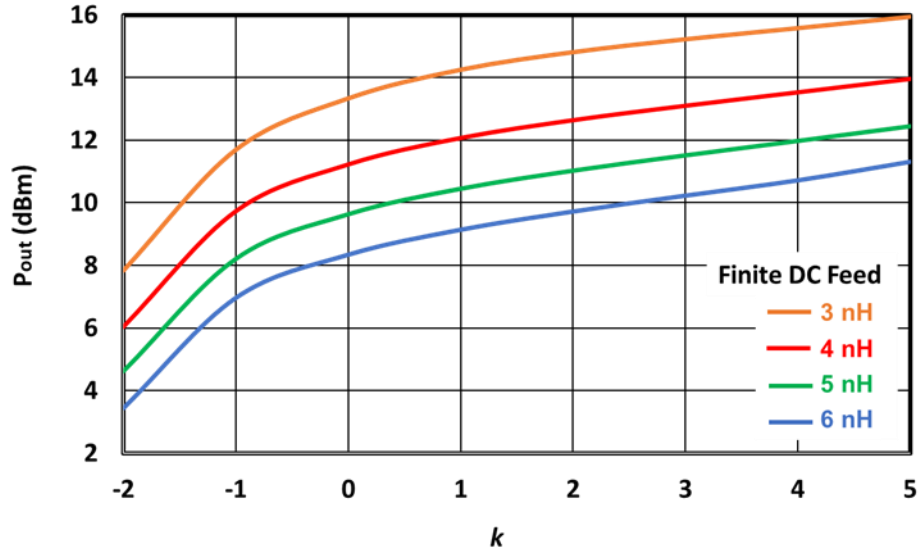
Fig. 3.10   The output power versus k for the proposed PA design

Figs. 3.11 depicts the relationship between k and the OMN components of the reference PA and the proposed PA, respectively, for different DC feed inductance values. The chosen value of the DC feed should be the smallest inductance value for practical implementation reasons.   From Fig. 3.11(b), 4 nH is also the smallest DC feed that can be utilized for the proposed PA to satisfy the required excess inductor range from 2.23 nH to 3.08 nH. C_{sh} has a range from 1.26 pF to 1.61 pF. Thus, we can calculate C_2 as from 1 pF to 10.56 pF.
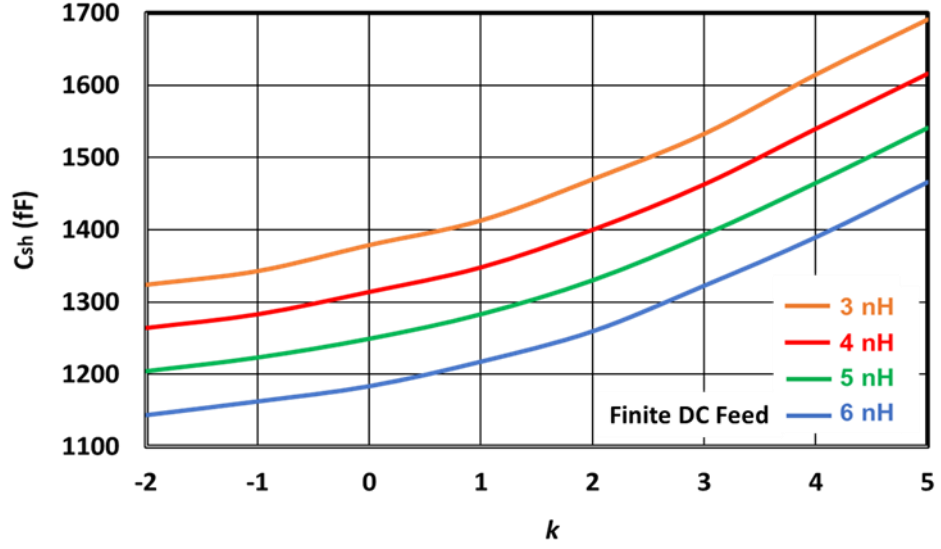
(a)
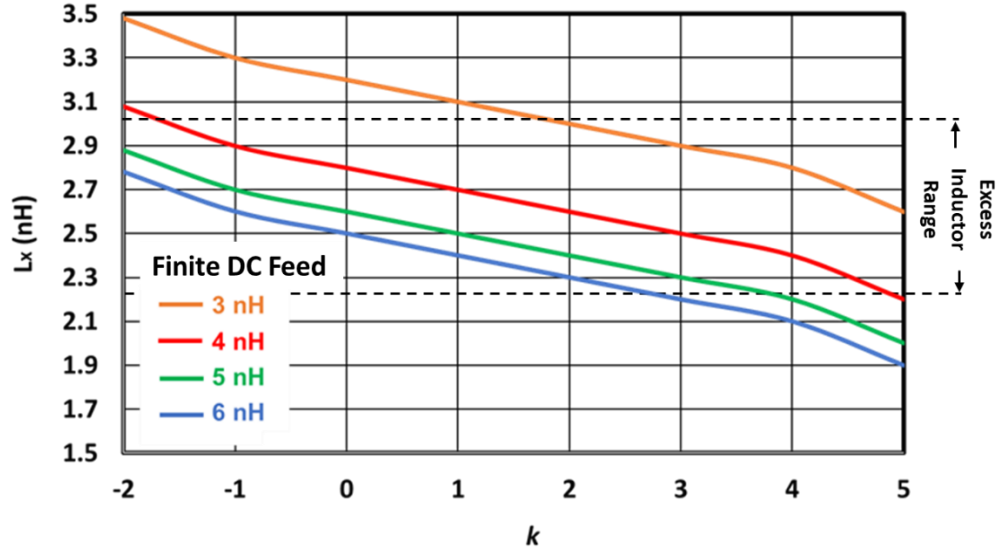
(b)

Fig. 3.11 **Proposed design: (a) C_{sh} versus k;**

(b) L_x versus k.

Figs. 3.12 depicts the plots of the OMN components versus the P_{out} of the reference PA and the proposed PA, respectively. From Fig. 3.12, to obtain max $P_{out} = 14$ dBm for the proposed PA, $C_{sh} = 1.61$ pF and $L_x = 2.2$ nH are required.
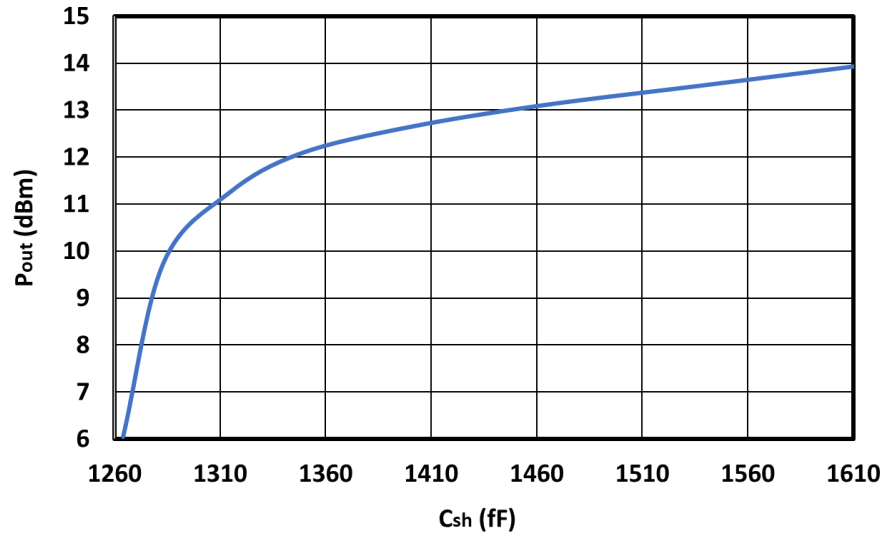
(a)
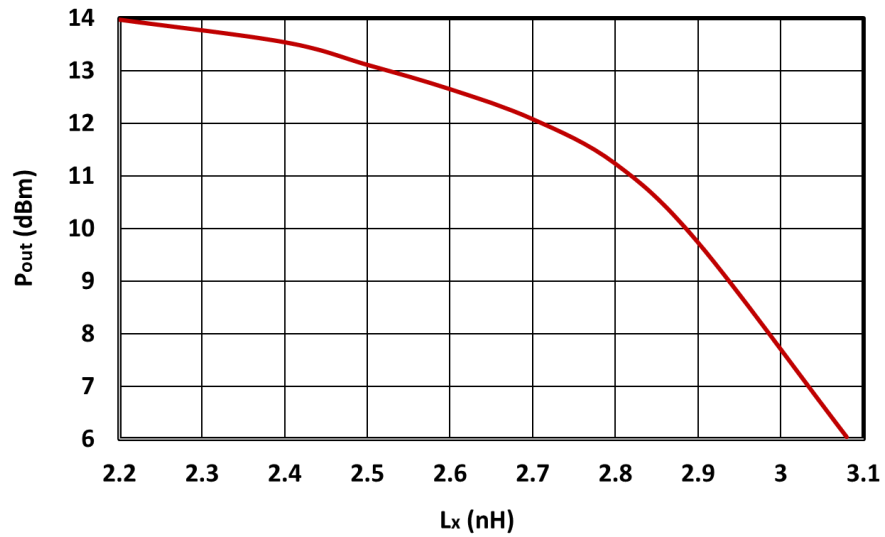
(b)

Fig. 3.12   Proposed design: (a) output power versus shunt capacitor;

(b) output power versus excess inductor.

The analytical results are verified by means of computer simulations using ideal

components. Fig. 3.13 illustrates the waveform of the drain voltage at the minimum

output power and maximum output power cases. We can see that the proposed Class-E

PA can satisfy the ZVS condition and make sure 100% power efficiency. The achievable

minimum and maximum output power is 6 dBm and 14 dBm separately. The dynamic range is 8 dB. The current is 79 mA for maximum value.
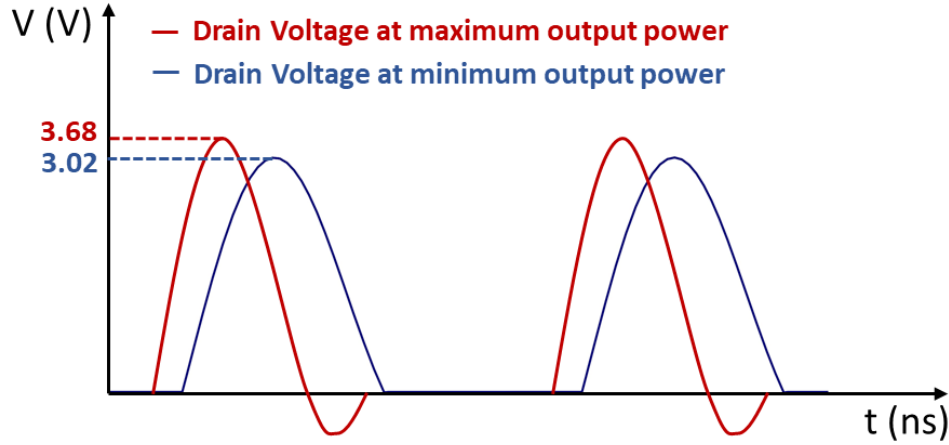
Fig. 3.13   The drain voltage waveform of the proposed PA using ideal component models

Fig. 3.14 depicts the DC currents at different output power for both the reference and the proposed PAs.   Note that the maximum output power of the proposed PA is 14 dBm, whereas it is 12 dBm for the reference PA.   At the same output power level range from 6 to 12 dBm, the proposed PA consumes lower DC currents, thereby achieving higher power efficiencies than the reference PA.   The lower DC currents can be explained analytically as follows.   The parameters that affect the DC current are indicated by the expression of the DC current $i_L(t)$ in (3.12).

$$i_L(t) = \frac{V_{DD}}{L}t + C\omega_o V_{DD}k - I_R sin\varphi \qquad (3.12)$$

For both the reference and the proposed PAs, the parameter values of V_{DD}, L, and ω_o are the same, and the impedance current I_R and the slope k are also the same when both PAs are compared at the same output power.   Therefore, the parameter

that determines the difference in the magnitude of $i_L(t)$ of the PAs is the shunt

capacitor C.   We can observe from Fig. 3.5(a) and Fig. 3.11(a) that at the same range

of k, the value of C in the proposed design is lower than that in the reference design.

Therefore, the DC current of the proposed PA is lower than that of the reference PA.
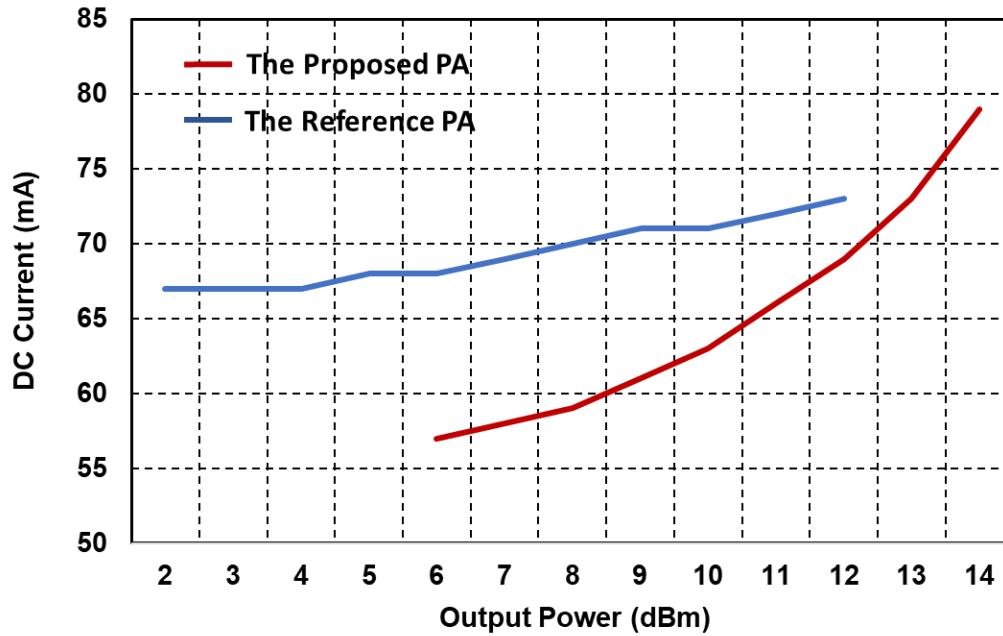
Fig. 3.14   The consumed DC currents at maximum output power for both the reference PA and the proposed PA

Based on our simulation results, we can conclude that the calculation of the

components is correct for ZVS condition. The output power can be varied with different

values of C_{sh} and L_x. The S-parameters of the proposed PA are also carefully

considered.   In conventional Class-E PA design, the OMN is designed for the purpose

of satisfying the ZVS and the ZVDS conditions, and therefore, the S-parameters are

usually not considered in the OMN design.

3.4 Implementation of the Class-E PAs

In this section, we will present the implementation procedure of the reference Class-E PA and the proposed Class-E PA with TSMC 40 nm CMOS Process. The schematic of the reference PA and the proposed PA are illustrated as below. The sizes of the components outside of the OMN are the same in the reference Class-E PA and the proposed Class-E PA.
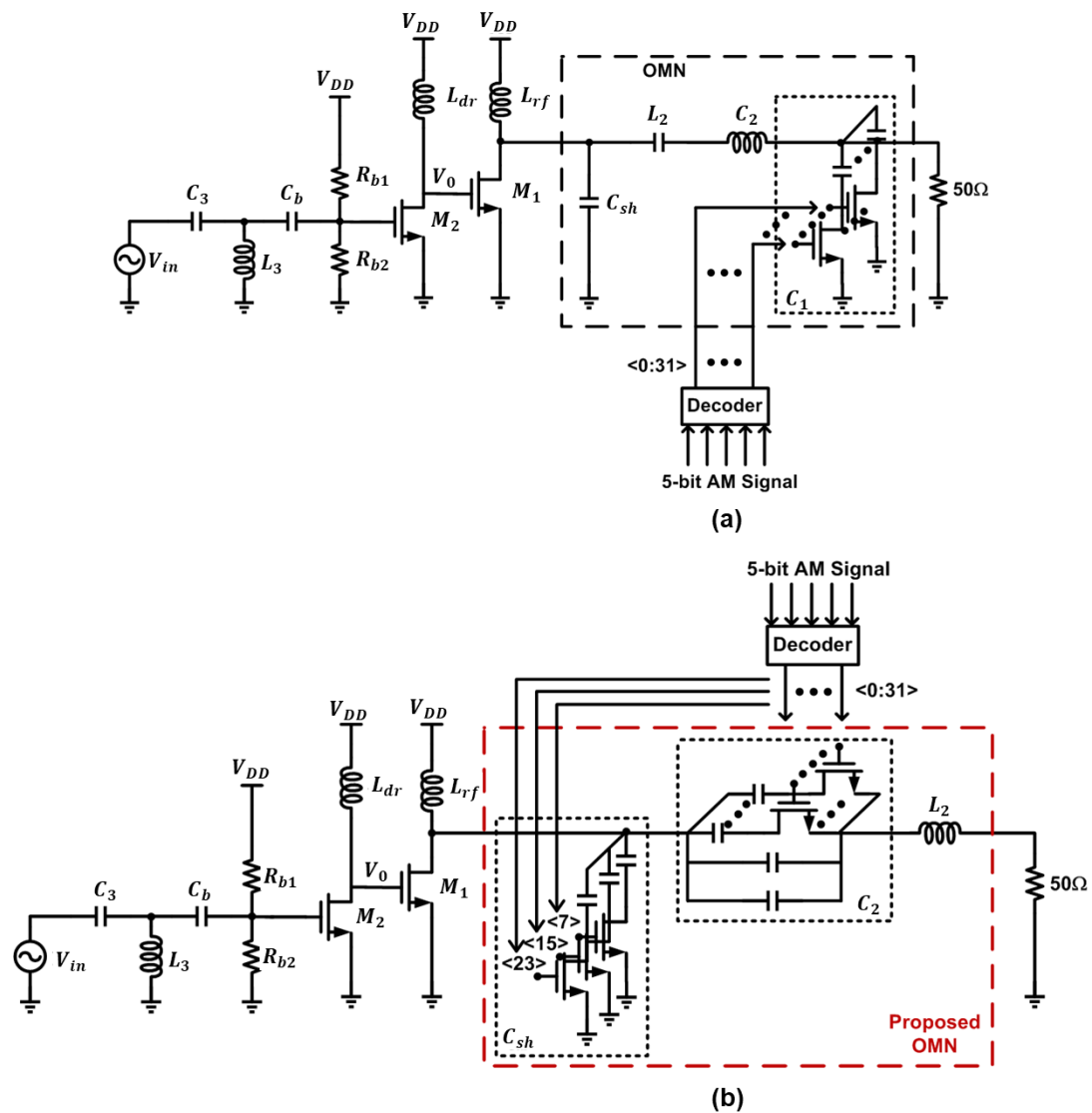
Fig. 3.15 **The schematics of (a) the reference PA and (b) the proposed PA**

3.4.1   PA transistor

In Section 3.2, we have investigated the maximum drain voltage in both designs is 3.74 V. This sufficiently high drain voltage can overstress the transistor and incur fatal oxide breakdown in current technology. To solve this problem, the common practice is to cascode a thick gate-oxide I/O transistor with the main device such that they can share the voltage stress and improve the reliability at the same time. However, this would affect the linearity and the power efficiency, which are our concern in the application. Thus, we choose not to use the cascode topology. Instead we choose to use the drain-extended transistor (DEMOS) whose drain can sustain up to 5V voltage (The maximum values of $|V_{ds}|$, $|V_{db}|$ and $|V_{dg}|$ are 5V). We utilize the nominal power supply (1.1 V), which the PA transistor can sustain during operation. The single transistor helps to reduce the complexity of the circuit and improve the power efficiency and the linearity.

There is a trade-off when we choose the size of the transistor. Large size of the switch transistor has small on-resistance such that the voltage across the switch transistor is close to zero when it is on. On the other hand, the large size of the transistor has large parasitic capacitance. The parasitic capacitance at the drain of the switch transistor can be lumped into the required shunt capacitance. If the parasitic capacitance exceeds the required shunt capacitance, it may distort the waveform of the drain voltage, thus affect the power efficiency. Fig. 3.16 shows the on-resistance and parasitic capacitance versus the size of the transistor. We can find that at the multiplier equal to

3 (each transistor size is $\frac{32\times10\ um}{540\ nm}$), the transistor has the minimum on-resistance and minimum parasitic capacitance. The parasitic capacitance of the transistor with this size is 1.143 pF, which does not exceed the required capacitance. The transistor with this size can sustain the maximum current mentioned in Section 3.2.
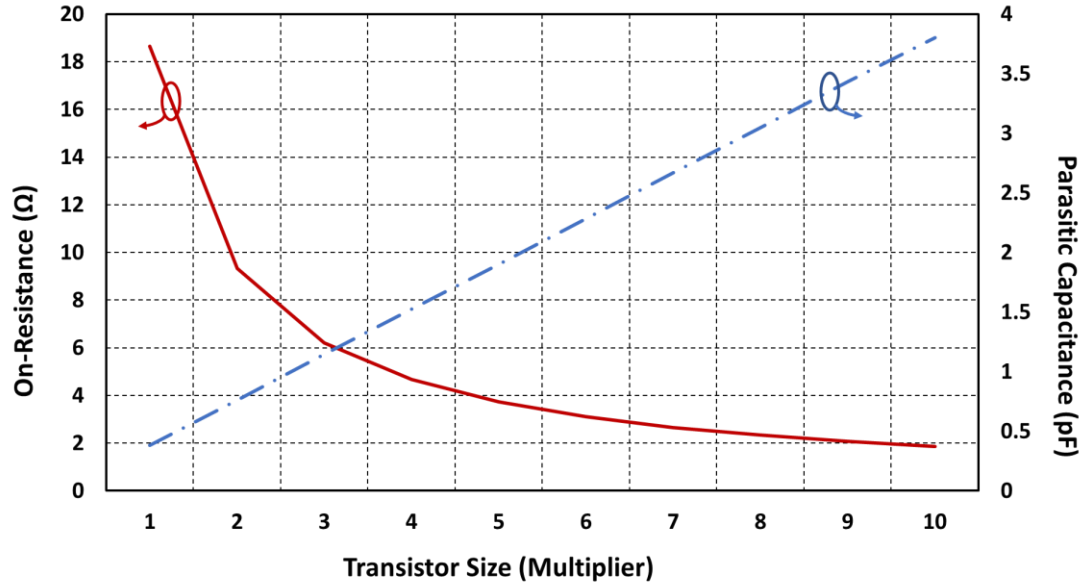
Fig. 3.16   The on-resistance and the parasitic capacitance of the transistor versus the transistor size

3.4.2   Driver

The driver comprises the transistor M_2 and the inductor L_1. The transistor M_2 has a smaller aspect ratio ($\frac{32\times10\ um}{270\ nm}$) compared with that of M_1. It reduces the capacitance load for the previous stage. The inductor L_1 is also part of the matching network between the driver and the switching PA and tunes out the drain capacitance of M_2. L_1 is set to 2 nH. When M_2 is on, the drain voltage of the driver V_0 is pulled down close to zero thus M_1 is off. When M_2 is turned off, V_0 is determined by the

transient response defined by L_1 and the total capacitances at the drain node of M_2. The driver has the same power supply 1.1 V as the PA.

3.4.3 Input Matching Network and Biasing Circuit

The biasing circuit consists of the resistor R_{b1} (5.62 kΩ) and the resistor R_{b2} (5.1 kΩ). It provides a biasing voltage at 0.523 V to the driver transistor whose threshold voltage is 0.523 V. Thus, the driver transistor can provide a 0.5-duty cycle signal to the PA transistor. Besides, there is a DC-blocking capacitor C_b.

The input matching network is designed to match the input impedance seen into the PA to the 50 Ω source impedance. The input matching network maximizes the power delivered to the next stage [65]. At 900 MHz carrier frequency, 1.1 V supply and 0.523V bias voltage, the input impedance is approximately $53.6 - j229.4$ Ω. The input matching network can thus be designed with an Smith chart to construct an L-type matching network graphically. The capacitor C_3 is 796 fF and the inductor L_3 is 21 nH.

3.4.4 Variable Capacitor Array

The variable capacitors can be realized with varactors or switchable capacitors. Varactors, however, have poor linearity performance and required advanced processes to improve the linearity. They also have a small tunable range. Thus, we choose to use the switchable capacitors in our design. The switchable capacitor consists of a capacitor and a switch (transistor) in series. The unit size of the switchable capacitor determines

linearity and quantization noise [1]. The size of the capacitor and the corresponding switch transistor is a tradeoff between tunability and efficiency [1]. As illustrated in Fig 3.17, larger size of switch transistor has smaller on-resistance and improves the Q of the tunable capacitor, but limits its tuning range as it has larger parasitic capacitance. Smaller size of switch transistor increases the tuning range, but has the smaller Q. It is worth to note that the tuning range decreases when the transistor size is smaller than certain size. It is because the parasitic capacitance of the switch transistor is close to the value of the capacitor thus it reduces the actual value of the total capacitance when the switch transistor is turned on.

In the reference PA, C_1 has a tuning range from 0 to 5.28 pF in a 5-bit resolution. As shown in Fig 3.17(a), two lines cross with each other near the transistor size of 9. As the number of finger of this type of transistor must be an even number, we set it to 8 for high Q. Each capacitor unit is 200 fF and the size of the transistor is $\frac{8 \times 1\ um}{270\ nm}$.

In the proposed PA, C_2 has a tuning range from 1 pF to 11.56 pF in a 5-bit resolution. As shown in Fig 3.17(b), two lines cross with each other at the transistor size of 10. Each capacitor unit is 380 fF and the size of the transistor is $\frac{10 \times 1\ um}{270\ nm}$. Besides, we designed to have 2 fixed capacitors which are always connected in the main branch such that they can sustain the maximum current flowing through in the main branch. Each main capacitor is 500 fF. C_{sh} use the same unit switchable capacitor as C_1 and it has a tuning range from 1.143 pF to 1.638 pF, considering the parasitic capacitance from PA transistor.
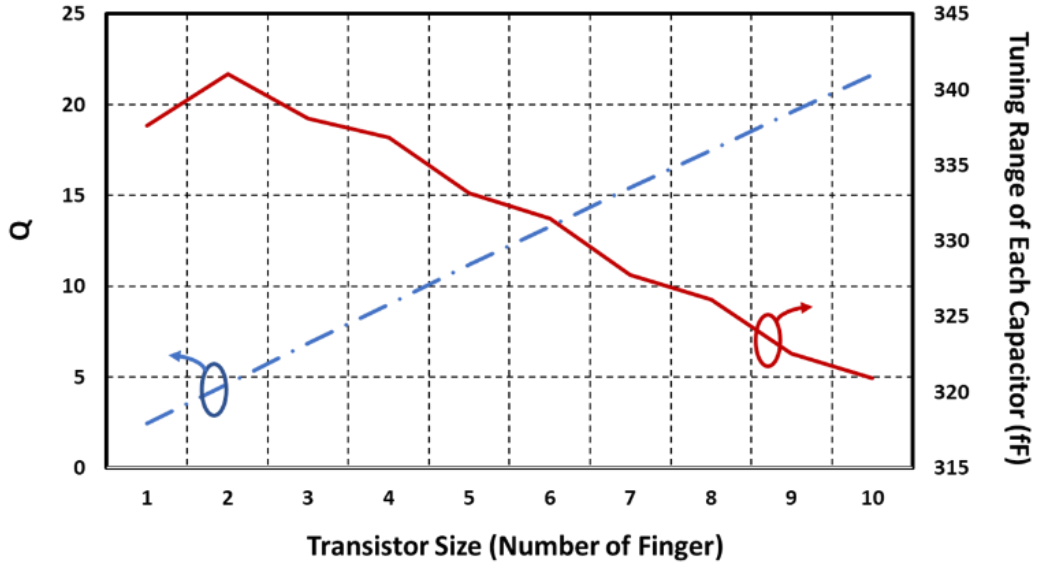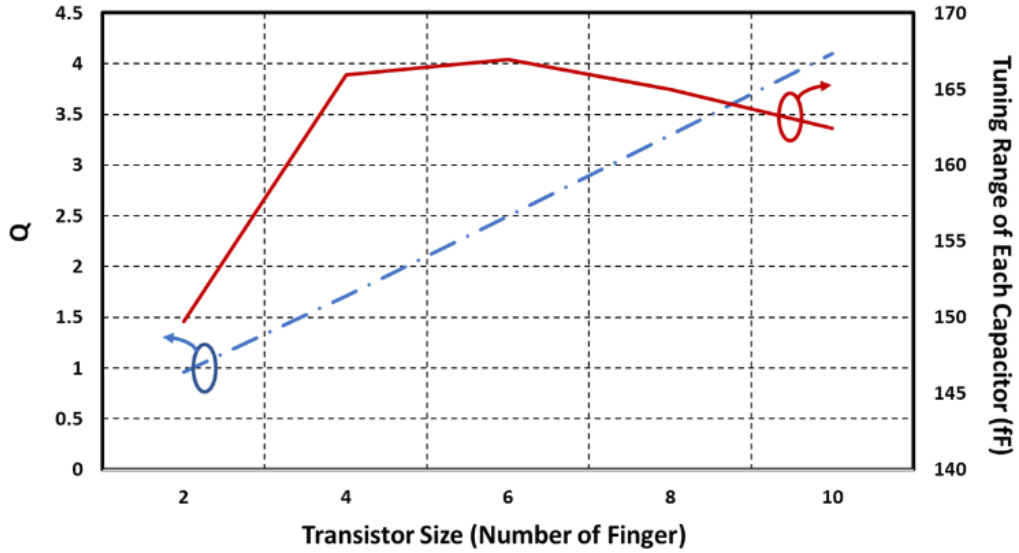
Fig. 3.17   **The Q and the tuning range of each capacitor versus the transistor size for (a) the reference PA and (b) the proposed PA**

The capacitor Q does not have a significant impact on the power dissipation of the proposed PA.   It can be explained as follows.   From (3.13) in Page 62 of the revised thesis, the relationship between the power loss due to Q, P_{LOSS}, and the output power, P_{OUT}, of Class-E PAs can be approximated as [1]

$$\frac{P_{LOSS}}{P_{OUT}} \approx \frac{1}{Q}\sqrt{\frac{50}{R_L} - 1} \; . \tag{3.13}$$

It is apparent from (3.12) that if R_L is set to 50 Ω, which is the case for the proposed PA, a finite Q will have a marginal impact to P_{LOSS}.

3.4.5   5-to-32 Decoder

The 5-to-32 Decoder is built up with simple NAND Gate and Inverter. As illustrated in Fig 3.18, first the 5-bit AM signal goes through a 5-to-32 line-decoder. The line decoder consists of one 2-to-4 line-decoder and four 3-to-8 line-decoders. The 2-to-4 line-decoder generate the enabling signal for the 3-to-8 line-decoders. The thermometer code converter converts the digital signals in the line form into the thermometer form such that the output of the 5-to-32 decoder can control the variable capacitor array directly. The D Flipflop arrays store the output signal from the converter until next the clock period. Among the output signals, <7>, <15> and <23> are used to controlled the switchable shunt capacitor in the proposed Class-E PA.
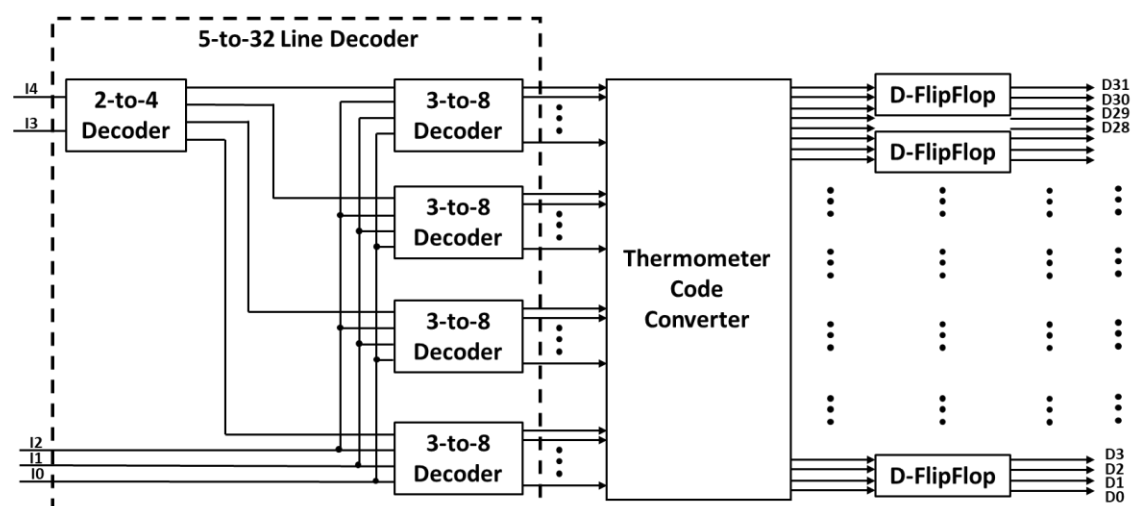
Fig. 3.18   Diagram of the proposed 5-to-32 thermometer decoder for the variable capacitor array

3.4.6   Bond-wire Inductors

Using bond-wire as an inductor can reduce the silicon area dramatically when compared to the case with on-chip spiral inductors. One on-chip spiral inductor normally occupies a quarter of the chip. Besides, bond-wire inductors have high Q. This helps to improve the power efficiency of the total system. In standard CMOS technologies, the Q of the on-chip spiral inductor is always less than 10. Furthermore, the length of the bond-wire can be adjusted such that we can control the value of bond-wire. As the bond-wire is typically far away from any conducting surface, parasitic capacitance can be seen as negligible compared to an on-chip spiral inductor [1]. Thus, we choose to use bond-wire instead of on-chip spiral inductor in the prototype.

We use the Keysight ADS tool-BONDW model to derive the required bond-wire geometry for the desired inductance values. In the ADS simulation, we assume the wire material is gold. The wire conductivity is 4.7x10^7 S and the wire size is 1 mil diameter. The minimum distance to ground layer is 100 μm.

As per the literature review, 1mm pad to pad length Wire bond provides approximately 1nH of inductances. Hence, to obtain 2nH and 4nH Inductances, different bond-wire geometries are iteratively simulated with the starting point of pad to pad length 2mm and 4mm respectively. Further, based on the simulation results, the geometric shape as well as the pad to pad lengths are modified until we reach the satisfactory inductance and feasible to achieve bond-wire profile.

The geometry parameter of the bond wire is shown in Fig. 3.19.
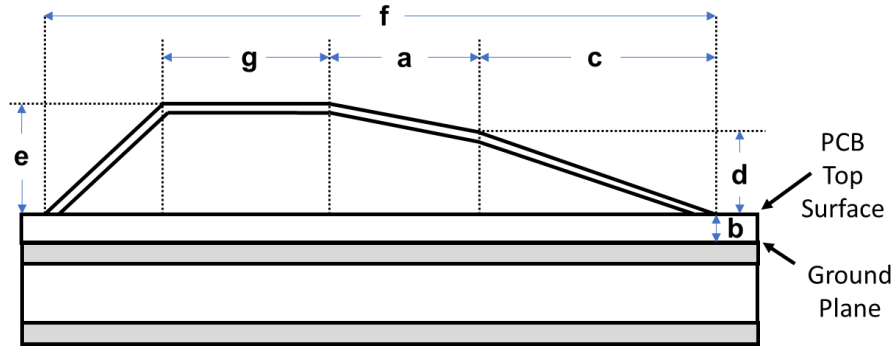
Fig. 3.19   The geometry parameter of the bond wire

Table. 3.1 summarizes the final geometry of the 2nH and 4nH bond-wire inductances. All dimensions are in μm.

Table 3.1   The final geometry of 2 nH and 4 nH wire bond inductances

	a	b	c	d	e	f	g
4nH	1380	100	1380	340	600	4600	690
2nH	720	100	720	340	500	2400	360

To verify the bond-wire inductor design, we design a PCB board on which the designed bond-wire inductor is fabricated. The fabricated bond-wire inductors are shown in Fig. 3.20.
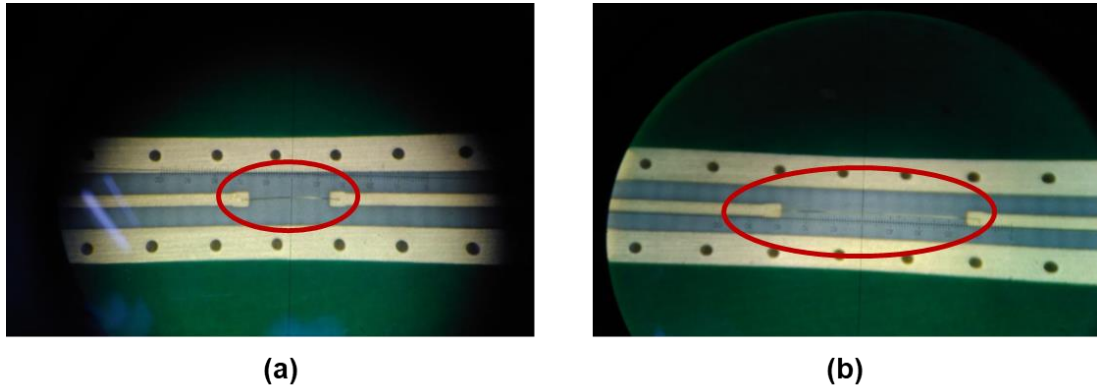
Fig. 3.20   The fabricated bond-wire inductor for (a) 2 nH and (b) 4 nH

The measurement results are illustrated in Fig. 3.21. Based on measurement, the

2nH inductor (Fig. 3.17(a)) is 2.09 nH at 900 MHz. The Q is 59.92. The deviation error

is 4.5%. The 4 nH inductor (Fig. 3.17(b)) is 4.12 nH at 900 MHz. The Q is 77.44. The

deviation error is 3%. The deviation error is within the acceptable range. The Q is much

higher than that of the on-chip spiral inductor.

(a)

(b)
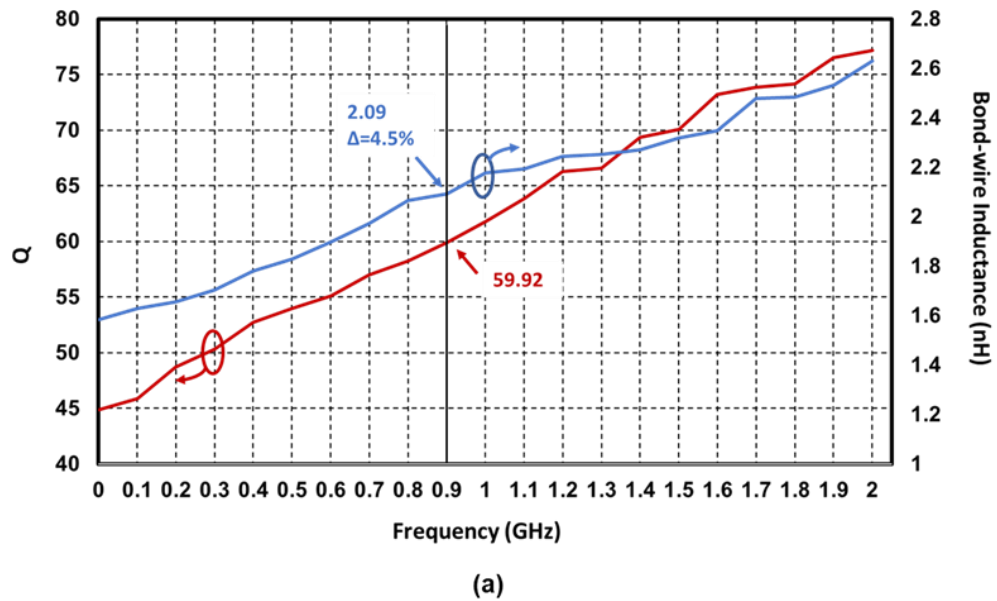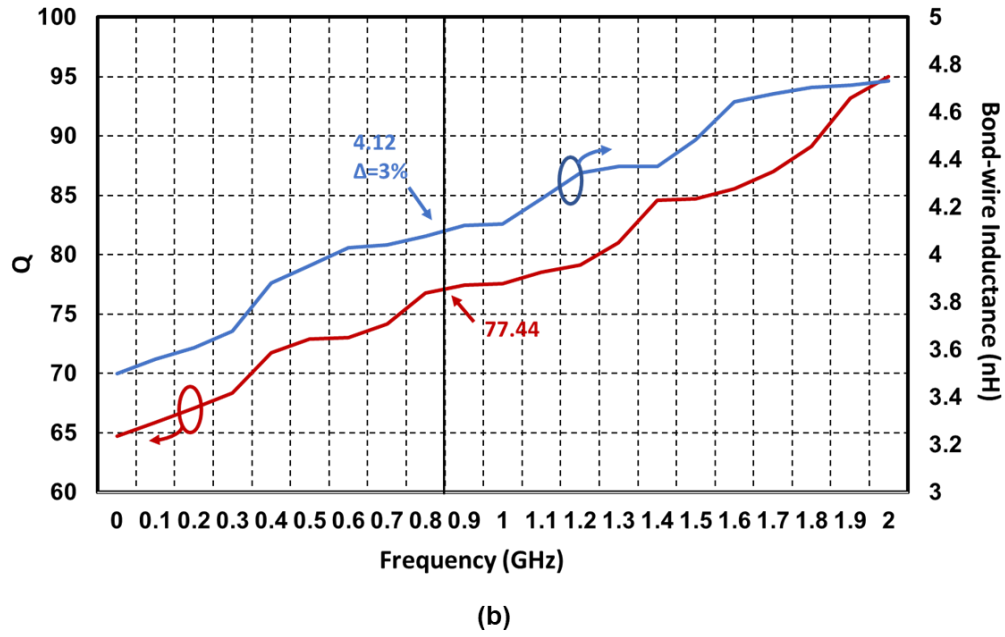
Fig. 3.21   **The bond-wire inductance and Quality factor versus frequency for (a) 2 nH and (b) 4 nH**

3.4.7   Layout of the Class-E PAs

The layout of the prototype is presented in Fig. 3.22. The total area is 1.2 mm x 0.6 mm.
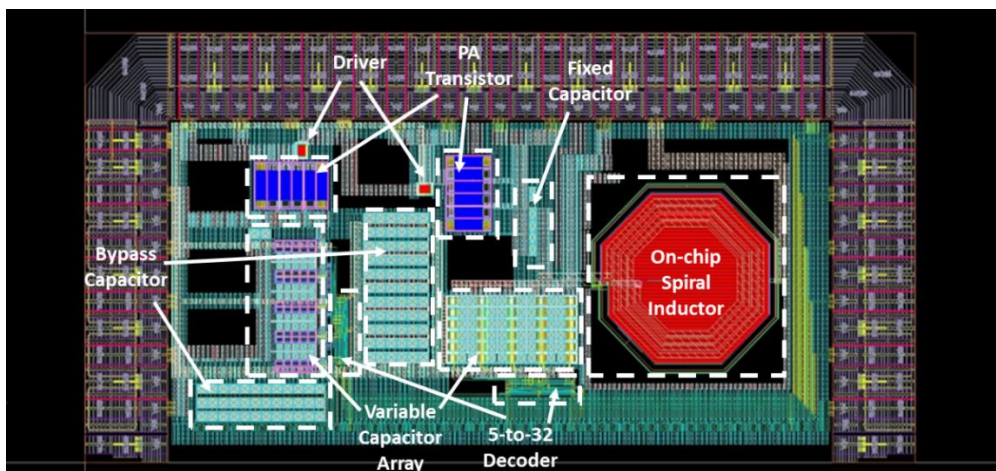
Fig. 3.22   **The layout of the reference PA (with the on-chip spiral inductor) and the proposed PA**

3.5   Conclusions

This chapter has presented the two digitally-controlled Class-E PAs with bond-wire inductors. We varied the components in the OMN to generate the variable-envelope output signal. In the proposed PA, we varied the shunt capacitor to make sure the ZVS condition satisfied, while the shunt capacitor in the reference PA was not changed. In addition, the OMN of the proposed PA obviates the need for the impedance transformation network and enables the use of bond-wires as the inductors. Consequently, the proposed PA has higher a drain efficiency compared with the reference PA. The components value corresponding to each output power level are determined based on the design equations in [11]. Then both the digitally-controlled Class-E PAs have been implemented with TSMC 40nm CMOS.   The design procedure of each building block has been presented.   The 2 nH and 4 nH bond-wire inductors have been designed and verified.   The layout of the prototype IC has been shown. The Simulation results and measurement results will be presented in the next two chapters.

Chapter 4

SIMULATION RESULTS

In this section, we present and compare the simulation results of the proposed Class-E PA and the reference Class-E PA. Both Class-E PAs are simulated with a single-ended 50 Ω resistor, 1.1 V supply, 900 MHz carrier frequency, and with practical device models. The decoder is powered at 2.5 V.

Fig. 4.1(a) shows the drain voltage waveforms of the reference Class-E PA, whereas Fig. 4.1(b) shows the drain voltage waveforms of the proposed Class-E. All the waveforms are obtained with sweeping the AM digital codes. The green lines represent the drain voltage waveforms obtained at the minimum AM signal of 0 V. The blue lines represent the drain voltage waveforms obtained at the medium AM signal of 1.25 V. The red lines represent the drain voltage waveforms obtained at the maximum AM signal of 2.5 V. As compared to the reference Class-E PA in Fig. 4.1(a), the proposed Class-E PA in Fig. 4.1(b) has a lower value of the drain voltage at the instant the switch is on, which can be regarded as an approximate ZVS condition. Thus, it results in smaller current spike at the switch-on moment. These improvements result in a higher efficiency during operation. Besides, the proposed Class-E PA has lower maximum drain voltage of 3.57 V compared to the maximum drain voltage (3.92 V) of the reference Class-E PA. This helps to release the stress of the PA transistor.
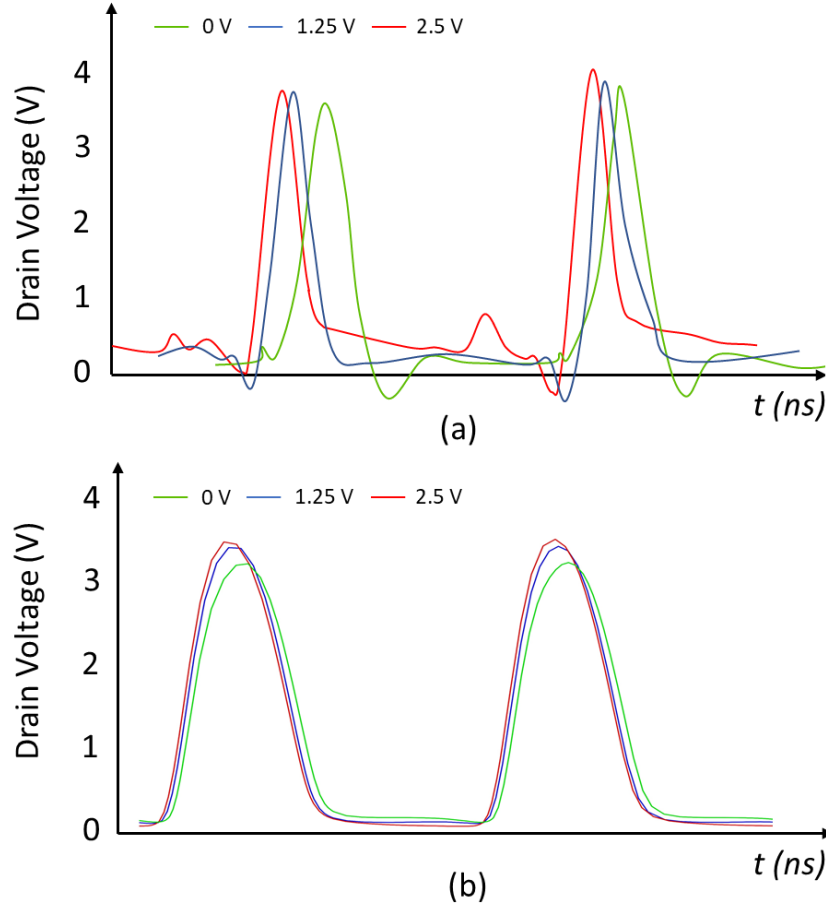
Fig. 4.1   Drain voltage waveforms of (a) the reference PA and (b) the proposed PA.

Fig. 4.2 depicts the plots of the drain efficiency versus the output power for both

Class-E PAs. The red line represents the proposed Class-E PA and the blue line

represent the reference Class-E PA. The proposed PA has a dynamic range of 7.8 dB

from 6.5 dBm to 14.3 dBm. The peak drain efficiency is 51% at 14.3 dBm output power.

The reference PA has a dynamic range of 9.9 dB from 2.3 dBm to 12.2 dBm. The peak

drain efficiency is 36% at 12.2 dBm output power. In general, the results in the red line

obtained from the proposed PA show higher efficiencies at the different output power

levels compared to the results in the blue line obtained from the reference PA, especially

at the relative low output power. The peak drain difference is 13% at the 6.5 dBm output

power. The higher efficiencies achieved by the proposed PA are due to the approximate

ZVS condition and the high-Q off-chip inductor.
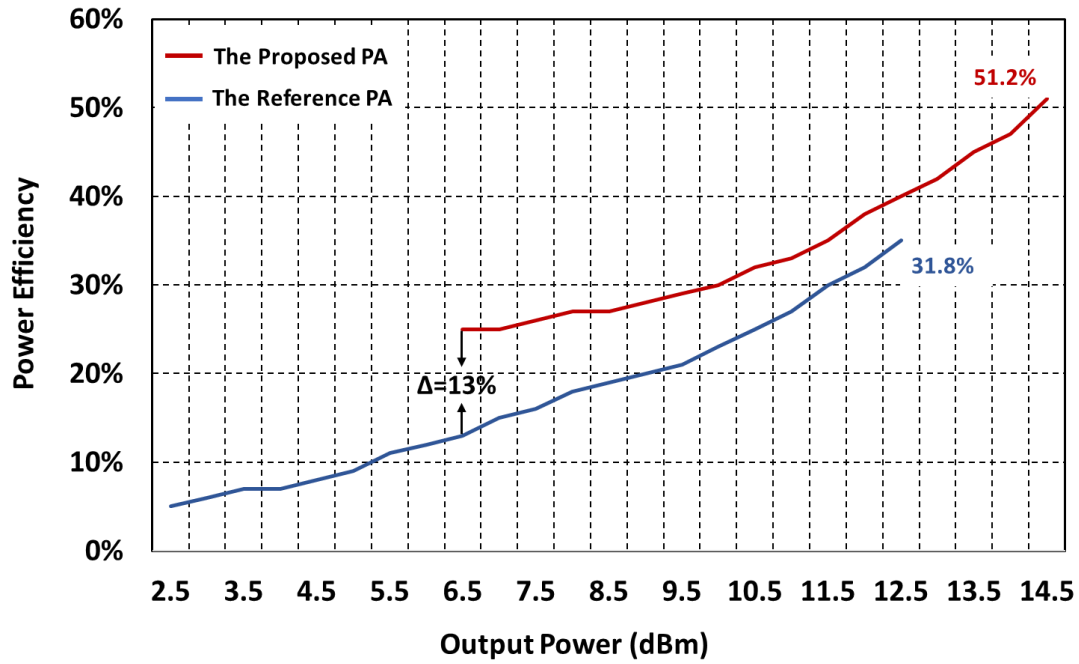
Fig. 4.2   Drain efficiency versus output power

Fig. 4.3 depicts the plots of the harmonic power (with respect to the fundamental

power) versus the normalized fundamental power at the output for both PAs. The plots

are obtained by sweeping the fundamental power. It can be observed that for the

proposed PA, the 2nd-, the 3rd-, and the 4th-harmonic are ≤33 dB, ≤71 dB, and ≤80 dB

lower respectively than the fundamental power. For the reference PA, the 2nd-, the 3rd-,

and the 4th-harmonic are ≤39 dB, ≤79 dB, and ≤87 dB lower respectively than the

fundamental power. The results indicate that the variable capacitor affects the filtering

function, but the filtering is still in the acceptable range.
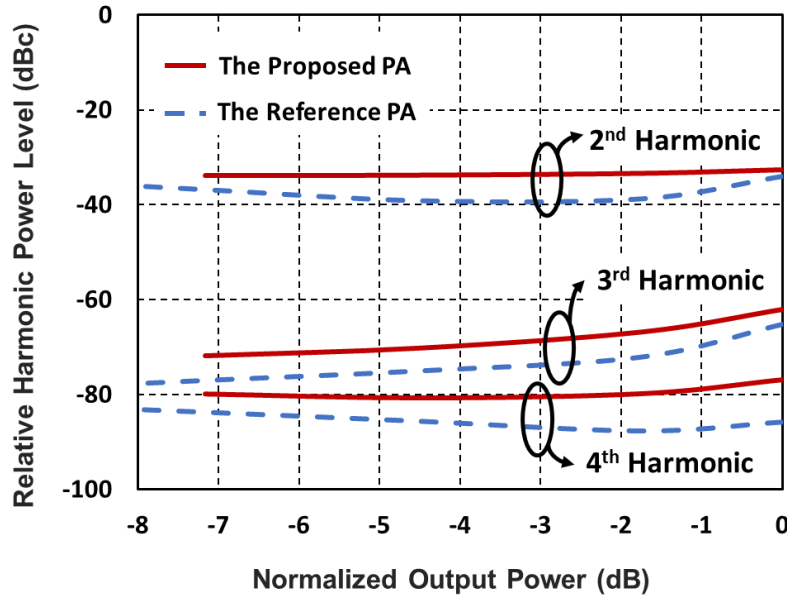
Fig. 4.3   The harmonic power versus the normalized fundamental power

For dynamic simulation, the WBAN standard requires a $\pi/4$ DQPSK modulated signal at a symbol rate of 600 ksps. As shown in Fig. 4.4, first we generate random binary data stream. According to the standard, each symbol has 2 bits and represent one of the eight constellation points for $\pi/4$ DQPSK modulation scheme. After that, we carry out the baseband $\pi/4$ DQPSK modulation. From Fig. 4.5(a), we can observe the ideal $\pi/4$ DQPSK modulation constellation and the spectrum occupies a wide bandwidth. The sharp transitions between ZEROs and ONEs in time domain requires an unnecessarily wide bandwidth in frequency domain. When the bit stream is applied to a band-limited block, it will introduce inter-symbol interference (ISI) and incur distortion. Hence pulse-shaping is required to constraint the signal bandwidth with certain range. In the standard, it has specified that the channel bandwidth is 400 kHz. Raised-cosine filter is usually used for pulse-shaping. It is similar to a sinc pulse and

its spectrum shows like a rectangle. The Raised-cosine filter can be split into two square-root raised cosine (SRRC) filters: one is in the transmitter and the other is in the receiver. The pulse-shaping is done by up-sampling then interpolation. It can be observed from Fig. 4.5(b) that the spectrum of the pulse-shaped baseband modulated signal is shaped with a 400 kHz bandwidth. The constellation of the pulse-shaped signal has a slight deviation from that of the ideal signal. During this process, the bandwidth of the original signal has been shaped and constrained to certain range. The EVM is calculated as –38 dB and the ACPR is –45 dB. After pulse-shaping, the baseband modulated signal in cartesian form is transformed into Polar form: the amplitude information A and the phase information ϕ. We quantize the amplitude information A into 5 bits and get a new amplitude information A'. Then we combine A' with the phase information ϕ to analyze the effect of quantization. As we can see from Fig. 4.5(c), the point representative in the constellation deviates from the ideal location slightly further compared with Fig. 4.5(b). The EVM is calculated as –27 dB. The ACPR is not be affected too much and is –44 dB in this case. In our prototype, the phase information is upconverted to the carrier frequency 900 MHz and the quantized amplitude information is used to control the variable output matching network.
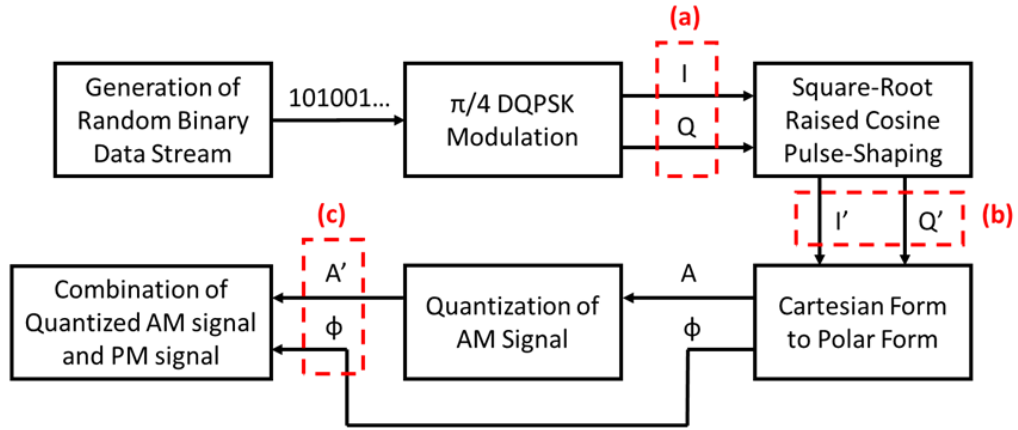
Fig. 4.4   The signal processing flow

(a)

(b)

(c)
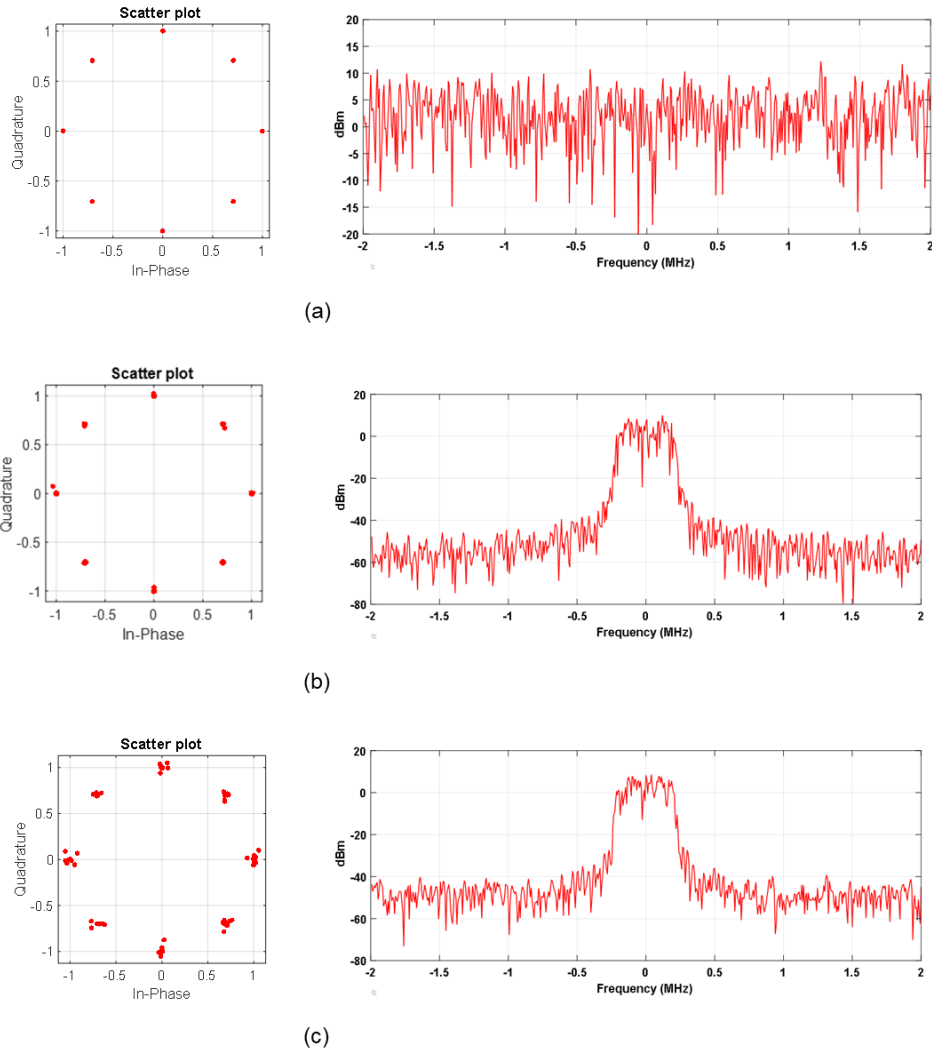
Fig. 4.5   The constellation and the spectrum of (a) ideal π/4 DQPSK modulation signal; (b) pulse-shaped π/4 DQPSK modulation signal; and (c) pulse-shaped π/4 DQPSK modulation signal after quantization

Fig. 4.6 shows the spectral power of the modulated output for both PAs. Fig. 4.6(a) represents the spectral power of the reference PA and Fig 4.6(b) represents the spectral power of the proposed PA. We can see that both the bandwidth of the spectrum is less than 400 kHz and within the spectrum mask. The ACPR for the proposed PA is simulated as –29.7 dB. The ACPR for the reference PA is simulated as –33.2 dB.

(a)

(b)
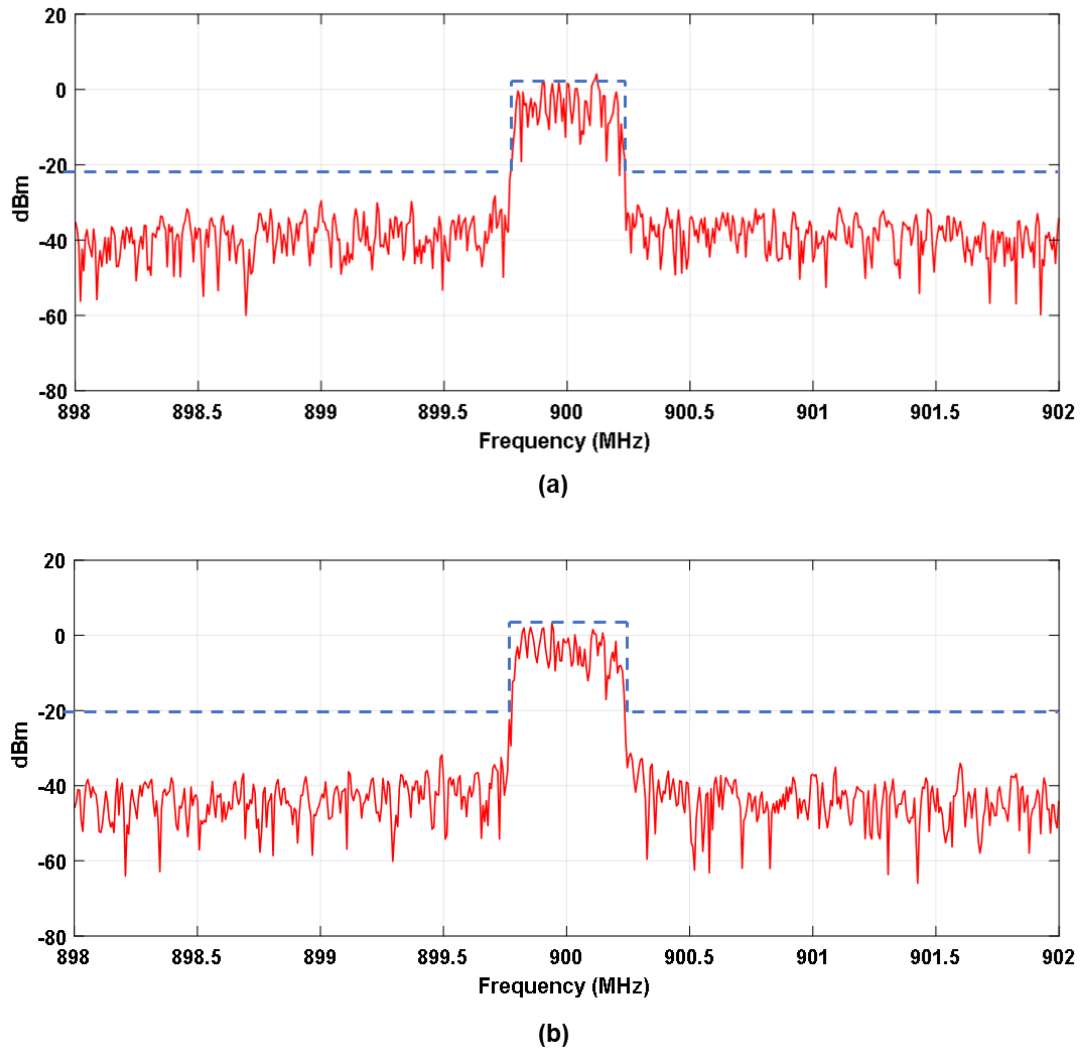
Fig. 4.6   The spectral power of (a) the reference PA and (b) the proposed PA

Fig. 4.7 presents the vector diagrams of the modulated signals analysed with MATLAB. Fig. 4.7(a) presents the reference PA and Fig. 4.7(b) presents the proposed

PA. It features an EVM of –17.45 dB for the reference PA and an EVM of – 18.84 dB for the proposed PA. This shows that the proposed PA has a better system performance than the reference PA.
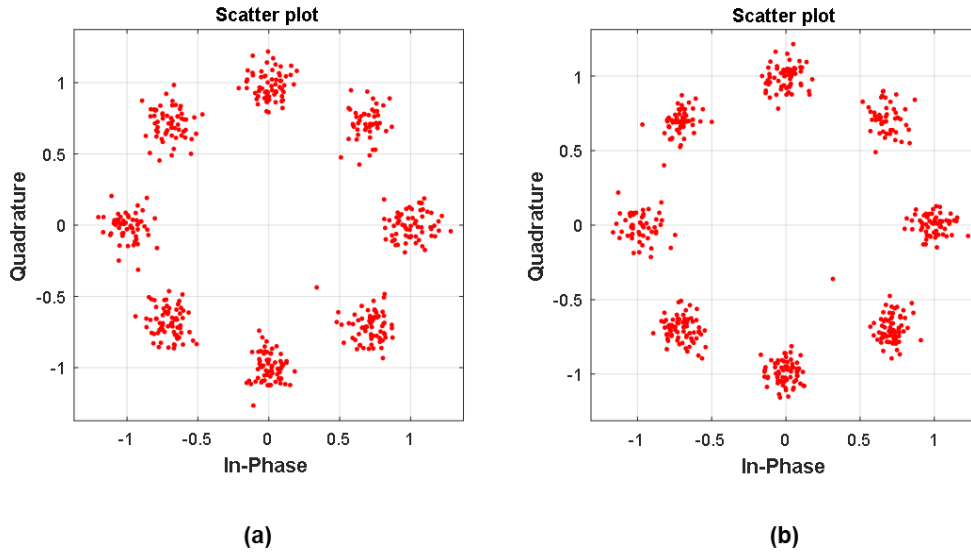
Fig. 4.7   The constellation of $\pi/4$ DQPSK signals from (a) the reference PA and (b) the proposed PA.

Conclusions

Based on the simulation results, we can conclude that the proposed PA is outstanding in the power efficiency when compared to the reference PA, especially at the relatively low output power. This is mainly because of the satisfied ZVS condition and the high-Q bond wire inductor. On the other hand, the filtering of the harmonics is affected by the variable capacitor in the filter. Although the ACPR of the proposed PA is slightly lower than that of the reference PA, it can meet the requirement of the WBAN standard. The EVM of both PAs, indicating the linearity of the PA, are almost equally matched.

Chapter 5

MEASUREMENT RESULTS

The chip microphotograph is presented in Fig. 5.1. The total die area is approximately 600 µm. × 1200 µm. The proposed PA occupies 400 µm. × 150 µm. The reference PA occupies 550 µm. × 400 µm.
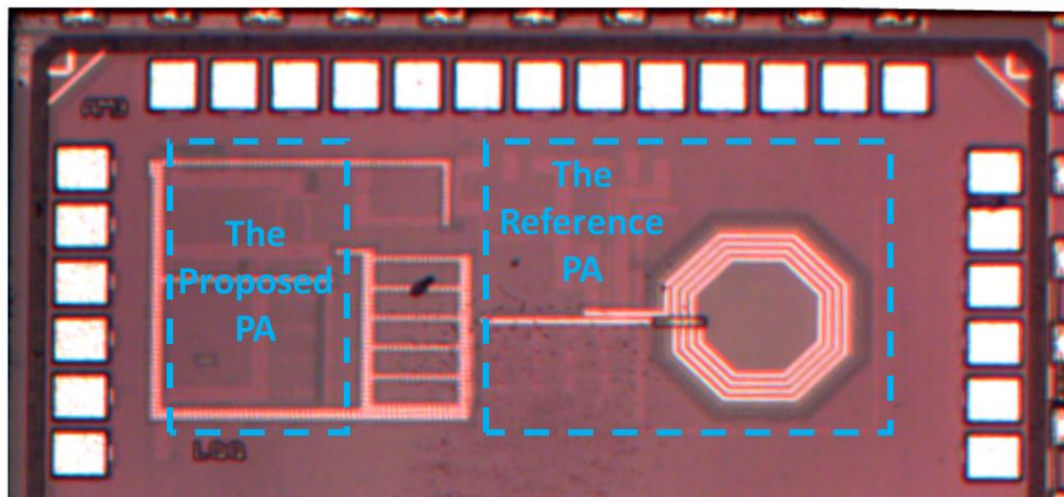
Fig. 5.1   The chip microphotograph

The chip is measured with an on-chip board where the bare silicon IC is mounted to the PCB without a package to it. Hence, as expected, the feature size of the PCB is very small, in the range of 1mil. The board is built of FR4 material. The finalized PCB uses a wire bond to bond IC pads into the PCB pads and realize the required inductor values. The schematic of the PCB is shown in Fig. 5.2.
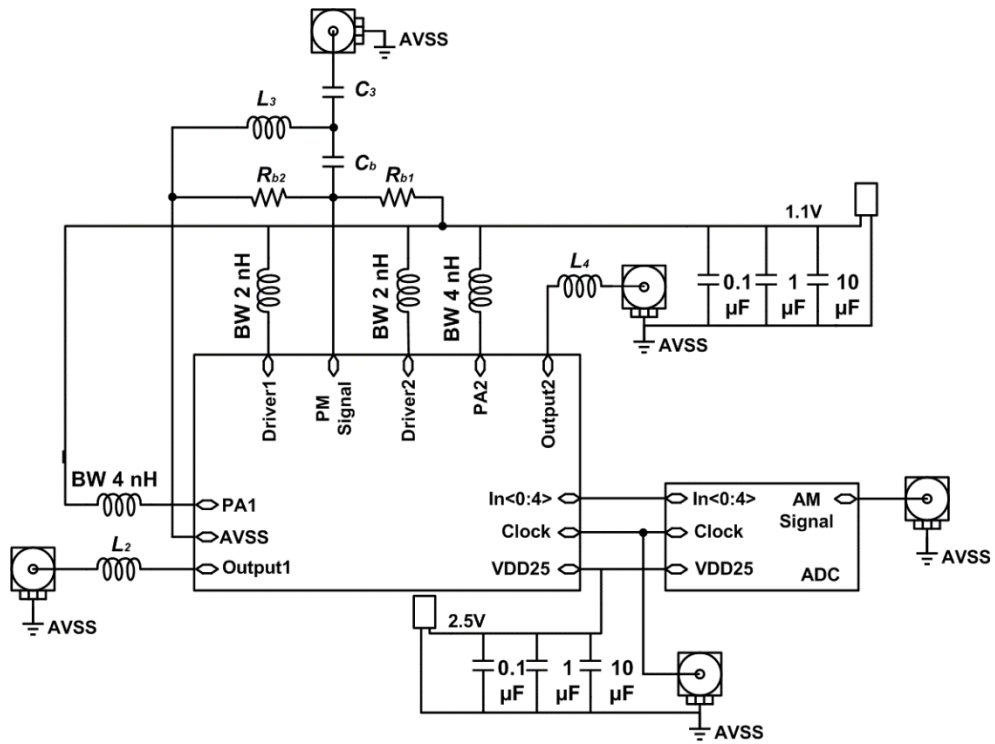
Fig. 5.2   The simplified schematic of the PCB

All measurements are performed on a single-ended 50-Ω load. The PA is provided with 1.1 V core supply and 2.5 V digital I/O supply. Fig. 5.3 shows the final PCB with the on-board chip and components.

Fig. 5.3   The final PCB with the on-board chip and components

Output Power versus AM Input Signal

The variable output power is obtained by controlling the variable OMN with corresponding AM signal. By sweeping the AM signal from the minimum code to the maximum code, we can obtain Fig. 5.4 as shown below. From Fig. 5.4, we can obtain that the peak power delivered by the proposed PA is 5.7 dBm and the minimum power is –1.1 dBm. This means that the dynamic range of the output power is 6.8 dB. By contrast, the reference PA has a dynamic range 10.4 dB from –6.4 dBm to 4 dBm. The output power for both PAs have been lower than the simulations. The dynamic range of the proposed PA has been affected.
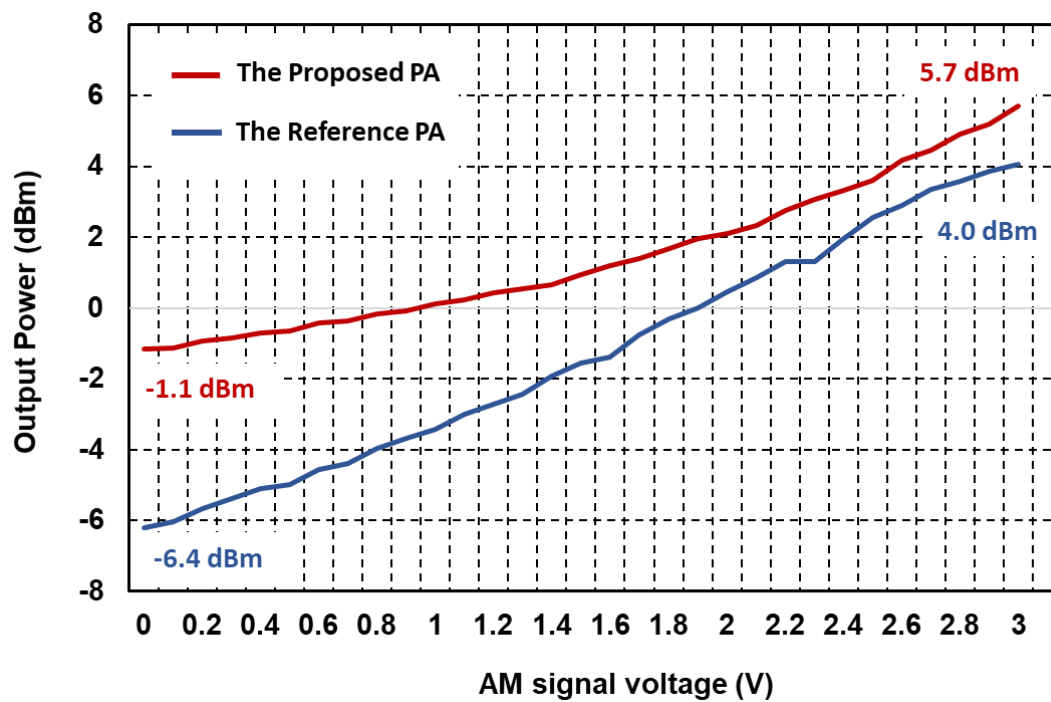
Fig. 5.4   The output power versus AM signal voltage for both PAs

Drain Efficiency versus Output Power

From Fig. 5.5, we can obtain that the maximum drain efficiency is 14.5% at 5.7

dBm output power for the proposed PA, compared to the reference PA which has maximum drain efficiency 10.8% at 4 dBm.
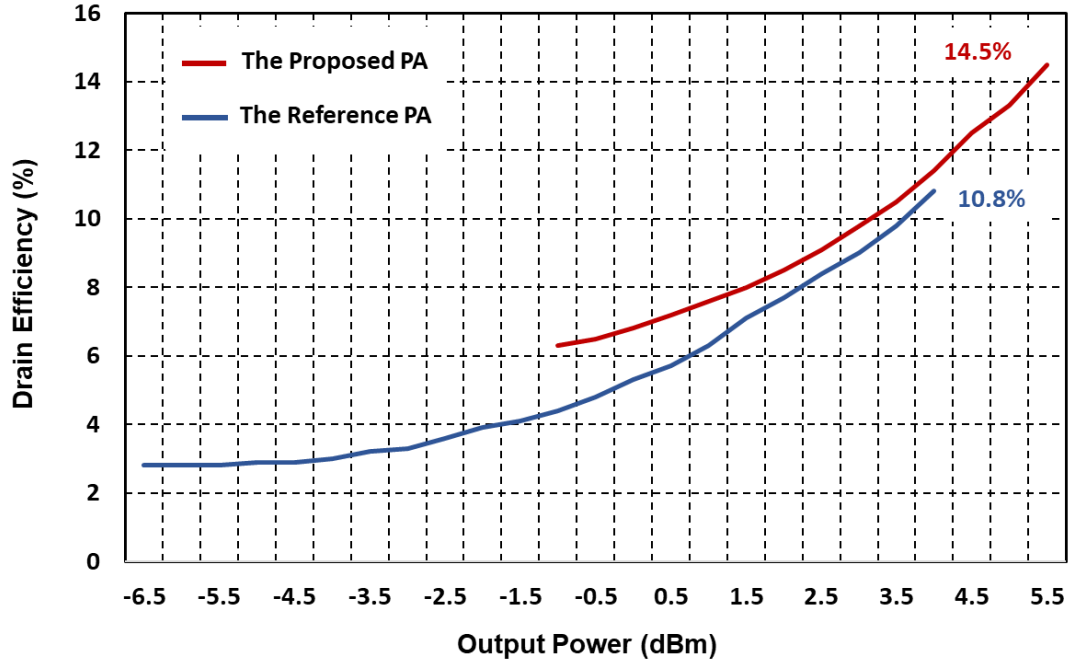
Fig. 5.5   The drain efficiency versus output power for both PAs

Relative Harmonic Power

Fig. 5.6 depicts the plots of the harmonic power (with respect to the fundamental power) versus the normalized fundamental power at the output for both PAs. The plots are obtained by sweeping the fundamental power. It can be observed that for the proposed PA, the 2nd-, the 3rd-, and the 4th-harmonic are ≤ 25 dB, ≤ 29 dB, and ≤ 74 dB lower respectively than the fundamental power. For the reference PA, the 2nd-, the 3rd-, and the 4th-harmonic are ≤ 29 dB, ≤ 59 dB, and ≤ 78 dB lower respectively than the fundamental power.
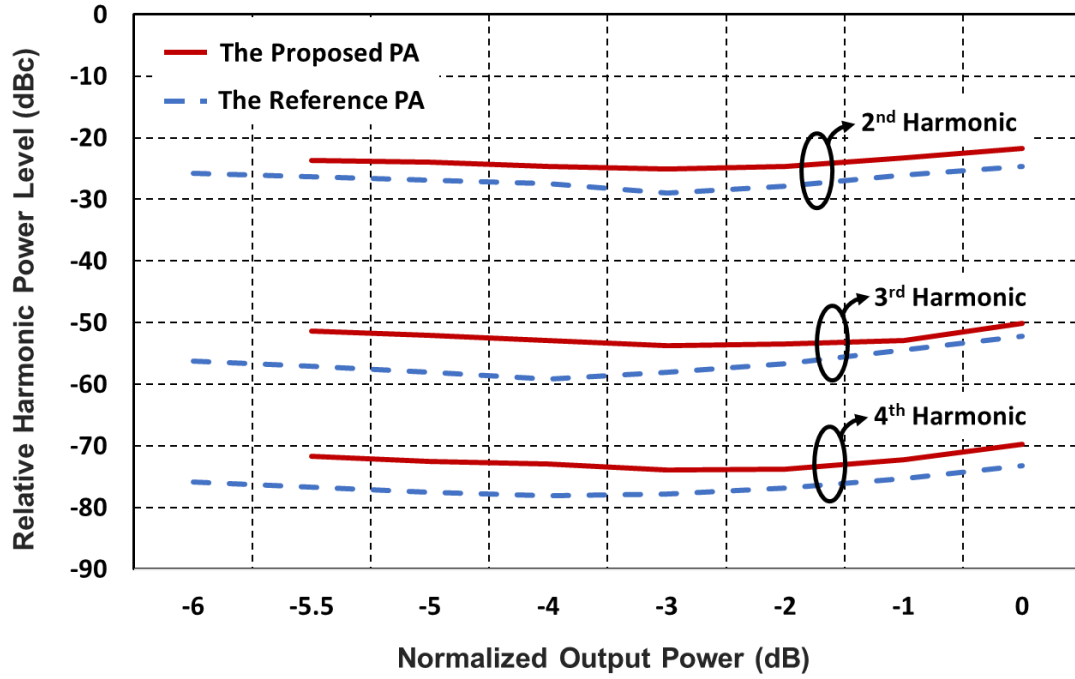
Fig. 5.6   The harmonic power versus the normalized fundamental power

Dynamic Measurement Set-up

The proposed PA has been tested in a Polar measurement setup as shown in Fig. 5.7. The baseband I and Q signal is modulated with pi/4 DQPSK modulation scheme. Then the baseband modulated signal is up-sampled and converted into Polar form. Both amplitude and phase signals are saved in the vector signal generator and applied to the proposed PA. The amplitude signal is sampled at 20 MHz rate and converted to digital signal via 5-bit ADC on board. The phased signal is up-converted to RF signal and applied to the proposed PA. The delay to the PA is 68 ps. The PM and AM signals need to be synchronized as the PM and AM signals run through different paths. The PM signal in Path A runs through the PM modulator and the PA, whereas the AM signal in Path B runs through the 5-bit ADC.   The AM signal Path B needs a trigger delay estimated as the delay to the PA. This can be done with SMU 200A Vector Signal

Generator.
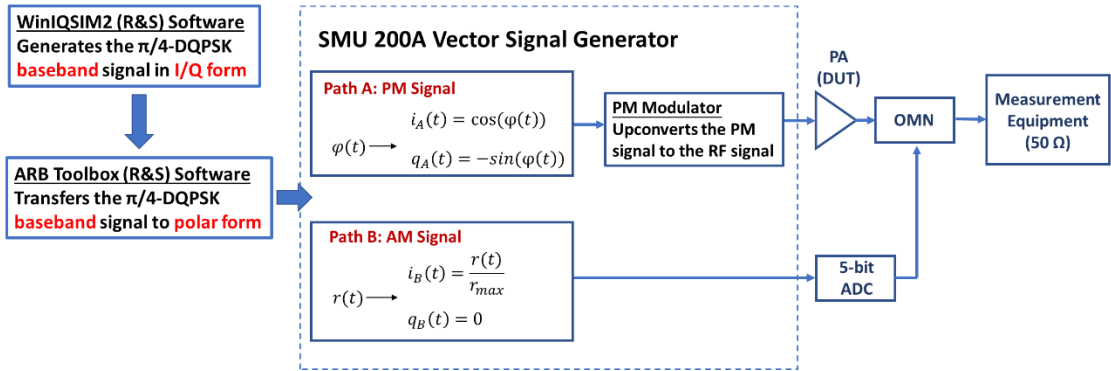
Fig. 5.7   Polar architecture measurement set-up

Spectral Power

Fig. 5.8 shows the spectral power of the modulated output for both PAs. Fig. 5.8(a) represents the spectral power of the reference PA and Fig 5.8(b) represents the spectral power of the proposed PA. We can see that both the bandwidth of the spectrum is larger than 400 kHz and cannot meet the spectrum mask. The ACPR for the proposed PA is measured as –17.56 dB. The ACPR for the reference PA is measured as –18.58 dB.
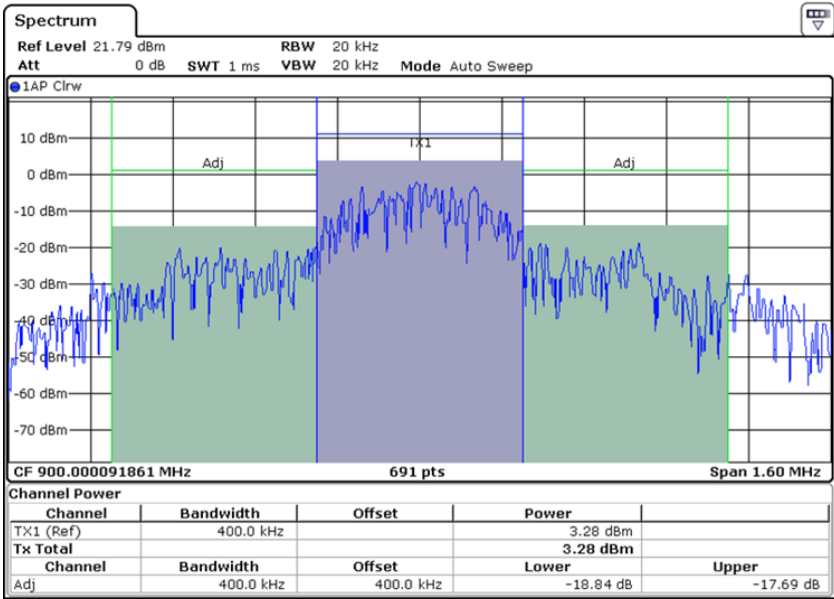
(a)
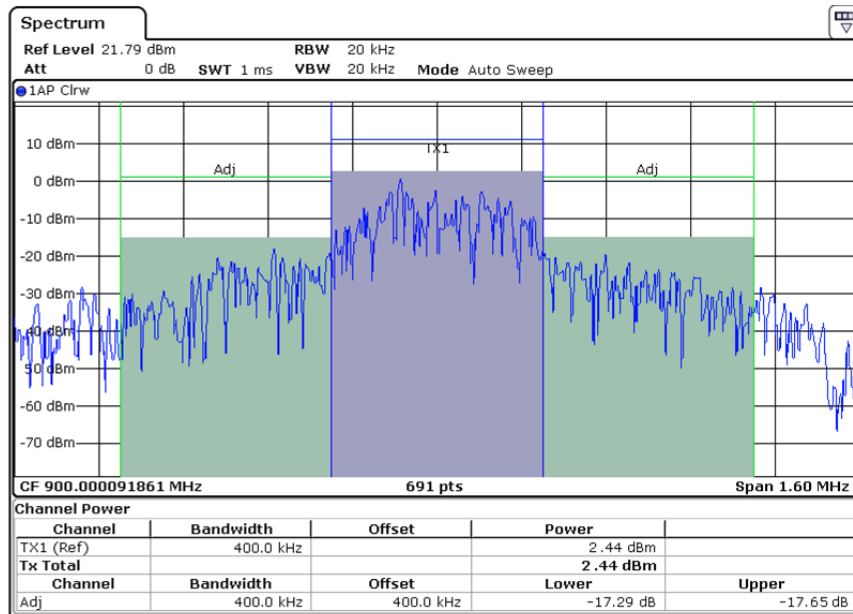
(b)

Fig. 5.8   The spectral power of (a) the reference PA and (b) the proposed PA

EVM

Fig. 5.9 shows the measured vector diagram and it features an EVM of –10.5 dB

for the proposed PA. The reference PA has an EVM of –9.9 dB.

(a)   (b)
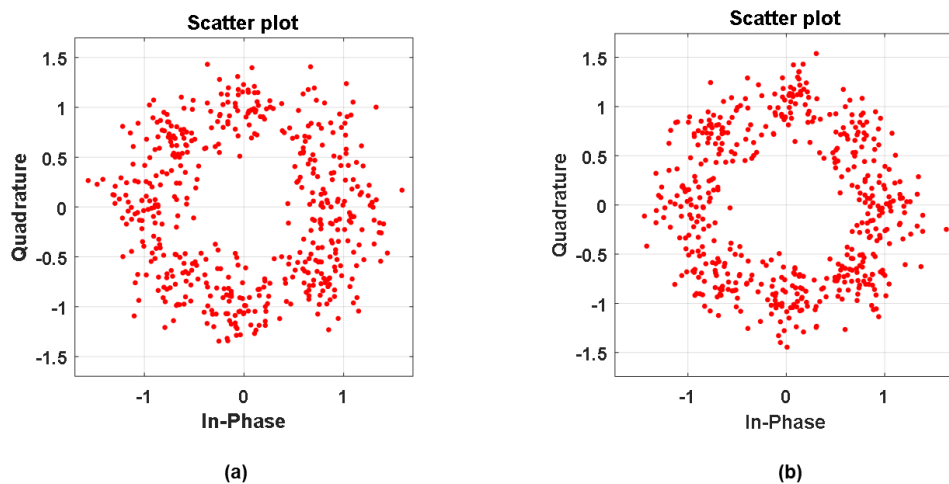
Fig. 5.9   The constellation of π/4 DQPSK signals from (a) the reference PA and (b) the proposed PA.

The measured performance of both PAs, however, are somewhat inadequate to satisfy the (transmitter) requirements specified in the IEEE standard for WBAN. The difference in the power efficiency obtained by simulation and measurement results can be attributed to the following contributors:

a) Bond-wire inaccuracy

In Section 3.4.6, the bond-wire inductors (only) are fabricated separately for verification purposes. These inductors are fabricated using an automatic wire bonder machine (ASM-Eagle Extreme IC Wire Bonding), and the resultant inductor geometry is well-controlled as verified using optical measurement equipment (SmartScope OGP-ZIP250). The fabricated inductors demonstrate that bond-wires can be used as inductors, and that the values required by the proposed PA can be achieved with reasonable accuracy. Nonetheless, the bond-wires that are used by the PA IC are fabricated manually because the pitch between the IC pads (partly due to the limited number of available pads; see (b) below) is too small for the automatic wire bonder machine. The resultant inductor geometry is less accurate compared to that achieved by the machine, and could contribute to the degradation in the measured power efficiency performance by 8%;

b) Limited number of the IC ground pads.

Due to the area constraint (shared IC with another circuit), there are only three IC ground pads that can be allocated to the PA IC used for the measurements. The inductance value between the IC ground and the PCB ground is obtained at ~1 nH,

which ideally should be 0.   This inductance undesirably raises the IC ground to ~0.37 V, and consequently, degrading the measured power efficiency by 12 % from that obtained by simulations.   In future iteration of the PA IC, the number of the IC ground pads should be increased to alleviate this problem;

c) Closely-spaced IC pads, and narrow PCB traces.

As described in (b), due to the area constraint, the IC pads are placed close to each other (narrow pitch), and consequent to this, the mutual inductance between the adjacent bond-wires is larger by 0.4 nH than that obtained by simulations.   The finite DC feed is now effectively increased, thus impeding the PA's ability from achieving the (ideal) ZVS condition, or in other words, decreasing the power efficiency 6%. Further, the end points of the PCB traces, where the bond-wires are soldered onto, are narrow (2 mil) and also closely spaced (2 mil pitch) due to the narrow pitch of the IC pads.   These traces, though designed to be as short as possible, may have some impedance that increases the power loss efficiency by 5%; and

The overall power efficiency loss from the aforesaid contributors is 31 % as obtained from simulations and is approximately close to the 36.5 % (51 % − 14.5 %) difference in the original simulation result and the measurement result.   In summary, the contributors to the difference in the simulation and measurement power efficiency results have been identified and can be rectified in the subsequent IC and PCB iterations.

Chapter 6

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1   Conclusions

In this thesis of the Master of Engineering research project, we have presented the analysis, design, and Integrated Circuit (IC) realization of the proposed Class-E RF PA capable of generating a variable-envelope output signal for digital RF Polar transmitters in the WBAN application, with emphases on low output power and high power efficiency based on TSMC CMOS 40 nm processes technology.   The PA embodying a novel digitally-controlled variable OMN for DLM has achieved three salient features. First, the OMN is directly controlled by the digital Amplitude Modulation (AM) data. It obviates the need for the conventional supply modulator, thereby reducing the area and power dissipation.   Second, the values of the components in the OMN always satisfy the ones required by the ZVS condition, which is ideally a lossless switching, at the PA.   Thus the proposed PA can achieve a high-efficiency operation.   Third, the proposed OMN has a novel network architecture that can choose to employ on-, or off-chip inductors, or both inductor types. This means that high quality-factor bond-wires can be employed to improve the efficiency.

Chapter 2 has provided a comprehensive literature review as background for the work described herein . It commenced with an overview of the WBAN standard

Thereafter, a literature review of the prevalent transmitter architectures has been presented.   Then, the linear PA and non-linear PA have been compared, followed by the detailed review on Class-E PA. Finally, the bond-wire inductor has been also compared with the on-chip spiral inductor.

Chapter 3 has presented the proposed Class-E PA with a novel digitally-controlled variable OMN, compared to a reference state-of-the-art PA with a digitally-controlled variable OMN based on the design in [1]. In the proposed PA, we varied the shunt capacitor to make sure the ZVS condition satisfied, while the shunt capacitor in the reference PA was not changed. Besides, the OMN of the proposed PA obviated the need for the impedance transformation network and enables using the bond-wire as the inductor. Thus, the proposed PA has achieved a higher drain efficiency, compared to the reference PA. The components value corresponding to each output power level have been determined based on the design equations in [11]. Then both the digitally-controlled Class-E PAs have been implemented with TSMC 40nm CMOS.   The design procedure of each building block has been presented.   The 2 nH and 4 nH bond-wire inductors have been designed and verified. The layout of the prototype IC have been shown.

Chapter 4 has presented the simulation results of the proposed Class-E PA and the reference Class-E PA. Both PAs have been designed using the TSMC CMOS 40 nm technology. Simulation results at 900 MHz carrier frequency and 1.1 V supply have shown that the proposed PA has achieved a 51% drain efficiency at 14.4 dBm peak

output power, a 7.8 dB dynamic range, –18.84 dB EVM, and –29.7 dB ACPR. On the other hand, the reference PA had a 36% drain efficiency at 12.2 dBm peak output power, a 9.9 dB dynamic range, –17.45 dB EVM, and –33.2 dB ACPR. Based on the simulations, the proposed PA has obtained a 15% higher drain efficiency while having a comparable performance to that of the reference PA. Both PAs have satisfied the (transmitter) requirements specified in the IEEE standard for WBAN (–15 dB EVM, –26 dB ACPR).

Chapter 5 has presented the IC measurement results of the proposed Class-E PA and the reference Class-E PA. Both PAs have been realized using the TSMC CMOS 40nm technology, and the prototype IC has been bonded directly onto the PCB with the bond-wire inductors for measurments. The experimental measurements have been conducted at 1.1 V supply and 900 MHz carrier frequency. The proposed PA has achieved a 14.5% power drain efficiency at peak output power of 5.7 dBm, –10.5 dB EVM, and –17.6 dB ACPR, while the reference PA had a 10.8% drain efficiency at 4 dBm peak power, –9.9 dB EVM and –18.6 dB ACPR. The benchmarking has shown that the proposed PA featured a higher drain efficiency at higher peak output power, while achieving a similar/comparable performance to that of the reference PA. The measured performance of both PAs, however, were somewhat inadequate to satisfy the (transmitter) requirements specified in the IEEE standard for WBAN. This could be attributed to the loss from the inductance and resistance arising from the closely-spaced IC pads and the consequent narrow (lossy) traces on the PCB used in the measurements. These limitations can be rectified in the subsequent IC and PCB iterations.

As an overall conclusion, the proposed Class-E PA with the novel digitally-controlled variable OMN can generate a variable-envelope signal with DLM. The variable OMN can be controlled directly with the digital AM baseband signal. The values of the components in the OMN always satisfy the ones required by the ZVS condition to ensure high-power-efficiency operation. The novel architecture of the proposed digitally-controlled variable OMN allows to employ the high-Q bondwires as inductors. Based on the aforesaid three salient features, the proposed Class-E PA with the novel digitally-controlled variable can achieve a higher power efficiency (drain efficiency), while achieving a similar/comparable performance to that of the reference PA.

6.2   Recommendations for Future Work

The following directions are recommended for future work:

1. Realizing the bond-wires using the automatic wire-bonder machine to ensure the manufacturing accuracy. As the inductance value of the bond-wire is determined by the wire bending shape, the precise geometry of the bond-wire is critical to obtain the required inductance value. With the automatic bonder machine provided, we can make sure the geometry of the bond-wire satisfied.

2. Separating the chip pads. As the PA deals with high frequency operation, the extra mutual inductance caused by the compact chip pads will distort the transient response of the OMN and affect the power efficiency. Keeping the distance of the chip pads wide helps to reduce the mutual inductance between the bond-wire and

the traces on the PCB. Besides, wider traces with small resistance can be used and it is easy to fabricate the PCB and wire bond the chip onto the PCB with widely-allocated chips pads.

3. Utilizing more pads as the ground pads to reduce the inductance value between the chip ground and the PCB ground. The bond-wire connected the on-chip pads and the pads on the PCB are parallel with each other. Using more ground pads indicates that more bond-wires are connected in parallel thus it can help to reduce the inductance value between the chip ground and the PCB ground.

4. Designing for multi-standard and multi-mode applications. In conventional RF systems that are designed to communicate on multiple wireless standards, a separate radio chip is employed for each different standard. This is inefficient in terms of silicon area, power consumption, and cost. Due to the variable OMN, this PA is reconfigurable for a multimode operation where multiple standards can be addressed with the same hardware.

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[1]   Q. Liu, V. Adrian, B. H. Gwee and J. S. Chang, "A high-efficiency Class-E Polar power-amplifier with a novel digitally-controlled output matching network," 2016 International Symposium on Integrated Circuits (ISIC), Singapore, 2016, pp. 1-4.

[2]   Q. Liu, V. Adrian, B. H. Gwee and J. S. Chang, "A Class-E Amplifier with a Novel Dynamic Load Modulation Matching Network," accepted for presentation in the *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017.

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