Innovative application and driving of enhancement mode gallium nitride power transistors

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**INNOVATIVE APPLICATION AND DRIVING OF
ENHANCEMENT MODE GALLIUM NITRIDE
POWER TRANSISTORS**

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ENGINEERING**

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the degree of Doctor of Philosophy**

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Abstract

Wide-bandgap semiconductors like Gallium Nitride (GaN) are enabling higher efficiency and greater power density in power electronics. The objective of this work is to develop novel gate drive methods and applications for the proliferation of Enhancement mode (E-mode) GaN power transistors.

The challenges of driving enhancement mode GaN devices are identified. Gate drive study is conducted to review the advantages and limitations of various gate drive methods. A 2-stage gate drive is introduced to allow a capacitor-less type gate drive to meet the requirements of the GaN GIT. This is further improved by proposing a 2-stage, 2-phase gate driver to reduce the gate ringing. Simulation is conducted to verify the design and the proposed design demonstrates reduction in gate ringing. A GaN GIT gate driver IC is evaluated against the R-type and RC-type gate driver to demonstrate driving the GaN Gate Injection Transistor (GIT) at high slew rates (~ 150 V/ns) while having built-in active Miller clamp and self-generated negative voltage rail for cross-conduction protection.

This research investigated the application of GaN GIT in Inductive Power Transfer (IPT) for Electric Vehicles (EV). IPT systems provide significant benefits over conventional plug-in chargers. A high frequency inverter using GaN GIT, which have low on-resistance and gate charge, is implemented to reduce switching and conduction loss. The switching characteristics of the GaN GIT are studied and the inverter is designed to ensure low switching losses, while keeping overshoot and slew rates under control. An efficiency centric mode of operation is proposed to improve the efficiency of the system, while ensuring sufficient power transfer. The system efficiency peaks at 95 % at 100 kHz operation and 92 % at 250 kHz operation for a coil gap of 80 mm at 2 kW output power. At a coil gap of 150 mm, the system obtains above 90 % efficiency at 1.3 kW. The inductive power transfer system is compared to a similar system using SiC power transistors and outperforms it by 1 % at 2 kW.

This work identified Point of Load (POL) converters in data centers as another potential application for enhancement mode GaN due to the increasing need for high efficiency and power density. An efficiency study on the buck converter for large step down applications from 48 V to 1 V is conducted and limitations to

this topology are identified. In order to further reduce the solution size and reduce effects of parasitic inductance, a novel 3-dimensional mounting strategy is proposed to integrate the GaN device with the Si gate driver.

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Acronyms

2DEG	2 Dimension Electron Gas
AlGaN	Aluminium Gallium Nitride
ASIC	Application Specific Integrated Circuit
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CMTI	Common Mode Transient Immunity
DCM	Discontinuous Conduction Mode
DEM	Diode Emulation Mode
DMOS	Double-Diffused Metal Oxide Semiconductor
EMI	Electro Magnetic Interference
EPC	Efficient Power Conversion
EV	Electric Vehicles
FBSOA	Forward Biased Safe Operating Area
FPGA	Field Programmable Gate Array
FRD	Fast Recovery Diode
GaN	Gallium Nitride
GIT	Gate Injection Diode
HEMT	High Electron Mobility Transistor
HEV	Hybrid Electric Vehicle
HFET	Heterojunction Field Effect Transistor
ICD	Integrated Circuit Design
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IOT	Internet of Things
IPT	Inductive Power Transfer
JFET	Junction gate Field Effect Transistor
LED	Light Emitting Diode
MISHFET	Metal Insulator Semiconductor Heterojunction Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSHFET	Metal Oxide Semiconductor Heterojunction Field Effect Transistor
OCP	Over Current Protection
PCB	Printed Circuit Board
PD	Photo Diode
PFC	Power Factor Correction
PPF1	Peak Power Frequency 1
PPF2	Peak Power Frequency 2
PQFN	Power Quad Flat No lead
RF	Resonant Frequency
SBD	Schottky Barrier Diode
SCM	Synchronous Conduction Mode
Si	Silicon

SiC	Silicon Carbide
SJ	Super Junction
SMD	Surface Mount Device
SMPS	Switch Mode Power Supply
VMOS	V-groove Metal Oxide Semiconductor
WPT	Wireless Power Transfer

Symbols

C_{DS}	Drain-Source capacitance
C_{GD}	Gate-Drain capacitance
C_{GS}	Gate-Source capacitance
C_{iss}	Input capacitance
E_{crit}	Critical electric field
E_g	Energy of bandgap in eV
E_{off}	Switching energy loss during off transition
E_{on}	Switching energy loss during on transition
E_{total}	Total switching power loss
f_{sw}	Switching frequency
I_{DS}	Drain-Source current
$I_{G,p}$	Peak gate current
$I_{G,av}$	Average gate current
I_{GS}	Gate-Source current
I_{SD}	Reverse conduction current
K	Boltzmann constant
k	coupling coefficient
L_{drift}	drift length
M	Mutual inductance
N_c	Effective electron density
N_D	Total number of electrons in a volume
n_i	intrinsic carrier density
N_v	Effective hole density
$P_{AC \text{ resistance}}$	Transformer/Inductor AC wire loss
$P_{Conduction}$	Power transistor conduction loss
P_{Core}	Transformer/Inductor core loss
$P_{DC \text{ resistance}}$	Transformer/Inductor DC wire loss
P_G	Gate drive loss
P_{off}	Turn-off switching loss
P_{on}	Turn-on switching loss
P_{oss}	Output capacitance loss
P_{SD}	Reverse conduction loss
q	Electric charge of electron
Q_g	Gate charge
$Q_{g,max}$	Gate charge absolute limit
Q_{GD}	Gate-Drain charge
Q_{GS}	Gate-Source charge
Q_{RR}	Reverse recovery charge
R_{ON}	Drain-Source on resistance
$R_{sd,rev}$	Source-Drain resistance during reverse conduction mode
R_{th}	Thermal resistance

T	Temperature in K
t_f	Fall time
t_r	Rise time
t_{SD}	Reverse conduction time
V_{Br}	Breakdown voltage
V_{drv}	Gate drive voltage
V_{DS}	Drain-Source voltage
$V_{GD,th}$	Gate-Drain threshold voltage
V_{GS}	Gate-Source voltage
$V_{GS,f}$	Gate-Source forward voltage
$V_{GS,pl}$	Gate-Source plateau voltage
$V_{GS,th}$	Gate-Source threshold voltage
ϵ_r	Permittivity
λ	Thermal conductivity
μ_n	Electron mobility

Chapter 1

Introduction

1.1 Power transistor background from Si to GaN

The switch is an integral part of power electronics, allowing the user to control the current and voltage to get the desired outputs needed for the application. The history of the power switch is shown in Fig. 1-1.

Figure 1-1 History of power switches

The first implementation of a switch in power electronics was using vacuum tubes to implement an inverter in 1928 [1]. The first semiconductor power switches came in the form of thyristors and Bipolar Junction Transistors (BJT) in the 1950s. BJTs were more favorable in the low and medium power applications due to their faster switching capabilities [2].

The entry of vertical Metal Oxide Semiconductor Field Effect Transistors (MOSFET) in the form of VMOS and DMOS structure in the 1970s displaced the BJT from the low power market. This is due to MOSFET's characteristics of low on-resistance, insulated gate to reduce leakage current, faster switching speed and superior ruggedness and Forward Biased Safe Operating Area (FBSOA) [2]. Vertical MOSFETs device have low on-resistance compared to lateral MOSFETs

Despite the increased efficiency attributing to power MOSFET development, the losses in high voltage devices were significant due to on-state power dissipation [2]. This challenge was overcome by the invention of the Insulated Gate Bipolar Transistor (IGBT) in the 1980s [3]. The device retains the high impedance gate of the MOSFET while having high forward current density and higher breakdown voltage devices are feasible. One disadvantage is that IGBT does not

conduct in reverse [3] and hence require additional anti-parallel diode for inductive load application like Switch Mode Power Supply (SMPS) or inverters [4]. While IGBTs have switching speed advantage over thyristor technology [3], switching speed is slower than MOSFET technology due to tail current [5], which reduce the power density of the solution.

Improvement in MOSFET technology led to the development of Super Junction (SJ) MOSFET in the 1990s [6] and was commercially released by Siemens in 1999. By redesigning the drift region of the SJ MOSFET, it is able to break the silicon limit as shown in Fig.1-2. Unlike IGBT which switches from 10-30 kHz, SJ MOSFETs are able to switch from 100-200 kHz, which makes it popular in application whose trend is moving towards higher power density like SMPS.

Figure 1-2 SJ MOSFET vs. Si limit [7]

Research in wide bandgap materials for power semiconductor devices such as Silicon Carbide (SiC) and GaN will push the boundaries of power electronics performance indices (efficiency, power density, reliability and cost) [8]. The material characteristics and new structures adopted offer new opportunities which can outperform silicon.

1.1.1 GaN vs. SiC vs. Si

The dominant material for power transistors has been Si since the 1950s. The reason is due to decades of capital investment committed to Si based power device. These commitments allowed Si based power transistors to be cheap, reliable and generate new application opportunities [9].

However, as Si approaches its limits, this prompted researchers to explore the feasibility of new materials to replace Si. Table 1-1 illustrates the comparison of the material properties between Si, SiC and GaN.

Table 1-1 Material comparison: Si vs. GaN vs. SiC

Parameter	Units	Si	GaN	SiC
Band Gap, E_g	eV	1.12	3.39	3.26
Critical Field, E_{crit}	MV/cm	0.23	3.3	2.2
Electron Mobility, μ_n	$\text{cm}^2/\text{V.s}$	1400	1500	950
Permittivity, ϵ_r		11.8	9	9.7
Thermal Conductivity, λ	W/cm.K	1.5	1.3	3.8

A normalized comparison is conducted in the radar graph shown in Fig 1-3. From the comparison, GaN outperforms Si and SiC in band gap, critical field, electron mobility and permittivity. SiC outperforms Si and GaN for thermal conductivity.

Figure 1-3 Material comparison: Si vs. GaN vs. SiC

1.2 Motivation

As form factor of mobile devices and computers shrink in size, higher power density chargers and power supplies have to downsize to match the aesthetics. Meanwhile, the proliferation of Internet of Things (IOT) and big data related technologies and products have driven the need for larger data centers to satisfy the need for computation capability.

Data center power consumption in the US is approximately 91 billion kilowatt-hours in 2013 and is expected to increase to 140 billion kilowatt-hours in 2020 [10], creating a need for highly efficient power electronics. These demands drive the focus in power transistor research towards wide bandgap semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) due to the constraints faced by conventional Silicon (Si) MOSFETs.

GaN Heterojunction Field Effect Transistors (HFETs) have been gaining traction due to its material characteristics. GaN HFETs can exist as normally-on devices (depletion mode) or normally-off (Enhancement mode (E-mode) GaN or Cascode GaN). Depletion mode GaN devices can be used in applications such as RF, but for power application, normally-off power devices are required. Due to the difficulty of controlling the switching speed and parasitic inductance of the cascade GaN, this work will focus on E-mode GaN.

Enhancement mode (E-mode) GaN such as GaN GIT [11] had been gaining attention due to their lower gate charge and on-state resistance which translates to lower switching and conduction loss compared to conventional Silicon (Si) power transistors [12]. With lower switching and conducting losses, efficiency of the power electronics can be increased. The lower losses in the semiconductor device allow utilization of smaller and cheaper heat dissipation components [13]. The reliability of the system will improve as temperature related stress is reduced [13]. Finally, the lower gate charge of GaN GIT allows higher frequency operation, resulting in smaller passive filter components and increased power density.

Recent work has showcased GaN power transistor application in various power electronics such as high frequency resonant converters [14], low power integrated DC-DC converters [15] and inverter application for wireless power

transfer [16], photovoltaic applications [13] and motor driver applications [17] [18]. This proves that GaN technology is able to push the pareto optimality boundary for power electronics.

E-mode GaN adopts a High Electron Mobility Transistor (HEMT) structure unlike conventional Si Power transistors, which uses a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure. The different transistor structures create opportunities for novel gate driving methods and power electronics topologies to be researched.

1.3 Objectives

The objective of this work is to explore novel ways to utilize the GaN device and investigate areas of applications where GaN devices can be employed.

Due to the difference in devices structure of E-mode GaN from conventional Si power devices, the first part will focus on developing novel methods of gate driving for E-mode GaN. It will investigate challenges of driving the E-mode GaN and limitations of state-of-the-art gate drive methods. This work aims to achieve a gate drive method which:

1. Fulfils the driving requirements of the GaN GIT
2. Improves the performance of the GaN GIT
3. Resolves issues related to high slew rate power devices.

Subsequently, this work will explore suitable applications for the enhancement mode GaN power devices in effort to energy conservation and commercialization of GaN power devices.

The GaN GIT will be applied in the automotive industry, focusing on inductive power transfer for electric vehicles. The weight of the converter is an important requirement for electric vehicles while power transfer efficiency is critical for inductive power transfer. This work aims to develop and evaluate an IPT system for EV application.

Another prospective application of using E-mode GaN in Data centers is in large step down buck converters for Point-Of-Load applications. This work aims to:

1. Develop an efficiency model of 48 V-to-1 V buck converter to identify pareto optimality curves for E-mode GaN devices.
2. Reduce the converter size by integrating the GaN power device and the Si gate driver.

1.4 Major contribution of the thesis

The contributions of the thesis are:

- A. In the area of E-mode GaN power transistor gate driving
 1. Developed a 2-stage, 2-phase gate drive technique for GaN GIT.
 2. Conducted comprehensive study for GaN GIT comparing various gate drive methods.
 3. Identified critical functions for high slew rate power device operations and verified through evaluation the effectiveness of these techniques.
- B. In the field Inductive Power Transfer
 1. Implementation of Inductive Power Transfer for Electric Vehicle charging using E-mode GaN device.
 2. Developed novel mode of operation to improve overall efficiency of converter.
 3. Optimized gate driver to improved efficiency through reduced switching losses, while ensuring other design parameters are kept within safe operating limits.
 4. This project won best paper for dialogue session D19 (Transportation Power Electronics) in Applied Power Electronics Conference and Exposition 2015.
- C. For Point-of-Load (POL) converters and device integration
 1. Conducted an efficiency modelling of large step down buck converters for 48 V-to-1 V POL converters.

2. Designed integrated gate driver and GaN device and verified performance advantages of integration.

1.5 Organization of the Thesis

This report is organized into 6 chapters as follows:

Chapter 1 provide the background of power transistors and motivation of this work. It also presents the objective of this thesis and its contribution.

Chapter 2 review the state-of-the-art technologies associated with GaN HEMTs and normally off GaN device. This chapter will identify the challenges and considerations associated with driving GaN GIT.

Chapter 3 will review various implementations of capacitor-less and capacitor type gate drivers for E-mode GaN devices. A 2-stage, 2-phase capacitor-less gate drive method is proposed to allow for integration and lesser parasitic inductance. A capacitor-type gate with active Miller clamp and built-in negative voltage is evaluated against 2 other conventional gate drive methods to showcase how performance and reliability can be improved.

Chapter 4 investigates the application opportunities of GaN GIT within IPT application for EVs. This is followed by the design and optimization of the gate drive method for GaN GIT and the development on the efficiency centric IPT system for EVs. Measurement results of the 2 kW system will be presented and analyzed.

Chapter 5 will shift the application focus to Point-of-Load converters for data centers. Various power supply topologies are studied and efficiency simulations were conducted to understand the performance of GaN power device in a large step down buck converter. This is followed by an explanation the opportunities for GaN GIT with Si integration. 3-D integration of GaN device and Si driver is implemented. The results are evaluated to illustrate integration advantages on the performance.

Chapter 6 concludes this report and elaborates on future recommendations.

Chapter 2

GaN Power Devices and Gate Driving Challenges

2.1 GaN HEMT

2.1.1 Introduction to GaN HEMT

GaN based power transistors do not adopt the structures adopted by Si such as MOSFET and BJT. GaN based power transistors adopt the High Electron Mobility Transistor (HEMT) structure, also known as Heterojunction Field Effect Transistor (HFET).

The GaN HEMT is a depletion mode (normally on) device as shown in the Fig.2-1 [19]. The main characteristic of this device is the Aluminum GaN (AlGaN) layer fabricated on top of a GaN layer. This creates a strain at the interface which creates a 2 DEG layer which has highly mobile conducting electrons in high concentration, giving the channel very low resistivity. The electron mobility increases from $1000 \text{ cm}^2/\text{vs}$ at the unstrained GaN to the $1500\text{-}2000 \text{ cm}^2/\text{vs}$ at the 2DEG layer [9].

Figure 2-1 Depletion-mode GaN HFET basic device structure [19]

It is a lateral device fabricated on top of a silicon substrate to allow the device to cost cheaper. Due to thermal and lattice mismatch between GaN and Si, a super lattice buffer layer is grown below the AlGaN/GaN lay for stress relaxation [20]. This structure increases breakdown voltage, making it suitable for high voltage applications.

2.1.2 GaN HEMT for power device application

For power converter application, normally on device are not suitable as a negative voltage needs to be supplied to turn off the device. The absence of this negative voltage during startup will result in a short circuit, therefore damaging the device.

In order to resolve this issue, a normally off device, threshold voltage greater than zero, has to be considered for power converter applications. Various different structures have been suggested to achieve this function [19].

Among the normally off technologies, they can be categorized in 3 types, enhancement mode non-insulated gate, enhancement mode insulated gate and cascode mode GaN.

2.1.2.1 Enhancement mode non-insulated gate

The recessed gate enhancement mode structure as shown in Fig.2-2 [9], is a type of enhancement mode, non-insulated structure [21]. By thinning the AlGa_N layer below the Schottky gate, the voltage generated by the piezoelectric field can be proportionately reduced. When this voltage is reduced to less than the built-in voltage of the Schottky gate metal, the device can be turned off at zero bias.

Figure 2-2 Recessed gate enhancement mode GaN structure [9]

Another non-insulated enhancement mode structure is the pGa_N gate enhancement mode structure as shown in Fig.2-3 [9] [22] [23]. The positive charges in the pGa_N layer have a built in voltage which is higher than the voltage generated by the piezoelectric effect. This depletes the 2DEG layer below the pGa_N layer.

Figure 2-3 pGaN gate enhancement mode structure [9]

2.1.2.2 Enhancement mode insulated gate

Enhancement mode insulated gate device, also known as Metal Oxide Semiconductor Heterojunction Field Effect Transistor (MOSHfet) or Metal Insulator Semiconductor Heterojunction Field Effect Transistor (MISHfet), are HFET devices which have insulation at the gate to reduce gate current consumption and hence driving loss [19].

Hybrid MOS-HFET structure is shown in Fig.2-4 [24], where the recess cuts through the 2 DEG layer. In order turn on the device, the inversion layer must be formed to connect the 2DEG layers on both sides of the recess.

Figure 2-4 Hybrid MOS-HFET enhancement mode structure [24]

2.1.2.3 Cascode mode GaN

The cascode structure is a normally off GaN device implemented on the circuit level, unlike enhancement mode device which is implemented on the process level. The cascode GaN consist of a depletion mode connected in series with a low voltage MOSFET as shown in Fig.2-5 [25] [26].

When the gate-source voltage is lesser than the threshold voltage of the MOSFET, the MOSFET device is turned off. This creates a negative voltage gate-source voltage across the depletion mode GaN which turns off the GaN device. When the MOSFET device is turned on, the gate-source voltage of the MOSFET is pulled down to almost 0 V and the GaN device is turned on.

Figure 2-5 Cascode GaN structure [25]

2.2 GaN GIT

2.2.1 Device structure

The structure of the GaN GIT is shown in Fig.2-6 [23]. The GaN device is fabricated on Si with a super lattice buffer layer between the substrate and the AlGaN/GaN layer for stress relaxation due to thermal and lattice mismatch. This structure also helps with the device achieve higher breakdown voltage [20].

Figure 2-6 Conventional GaN GIT structure [23]

In the GaN GIT, the p-GaN gate is formed over the undoped AlGaN/GaN heterostructure. The p-GaN lifts up the potential at the channel. Therefore, the electrons under the gate are removed by the built in potential of the P-type gate preventing current flow as shown in Fig.2-7 [11].

Figure 2-7 Bandgap of conventional GaN GIT structure [11]

The explanation of the Panasonic GaN power transistor is as shown in Fig.2-8. It will be discussed in 3 different states, which represents different ranges of sweeping the gate source voltage.

$$0 \leq V_{GS} \leq V_{GS,th}$$

At this region, the channel under the gate is fully depleted, when $V_{GS} < V_{GS,th}$ as shown in Fig.2-8a.

$$V_{GS,th} \leq V_{GS} \leq V_{GS,f}$$

From Fig.2-8b, after reaching the threshold voltage, electrons are allowed to flow through the previously depleted region, allowing the device to function like regular FET. This continues up to the forward voltage region.

$$V_{GS} > V_{GS,f}$$

Further increasing the gate source voltage above the forward voltage results in hole injection to the channel from the p-AlGaN as shown in Fig.2-8c. The injection of the electrons from the channel to the gate is well suppressed by the heterobarrier at AlGaN/GaN. The injected holes accumulate the equal number of electrons that flow from the source to keep charge neutrality at the channel. The accumulated electrons are moved by the drain bias with high mobility, while the injected holes stay around the gate because the hole mobility is at least 2 orders of magnitude lower than that of the electron. This conductivity modulation

results in a significant increase of the drain current, resulting in low on-resistance.

Figure 2-8 GaN GIT mechanism [11]

2.2.2 Hybrid Drain embedded GIT (HD-GIT)

A drawback to GaN HFET devices at high voltage is the increasing conduction loss due to current collapse. Current collapse is a phenomenon where accelerated electrons, as a result of high electric fields, getting stuck at passivation interface and defects of the GaN HFET devices [27]. These trapped electrons increase the on-resistance as they obstruct the current flow, increasing the conduction loss and eventually damaging the device.

The latest version of GaN GIT is the Hybrid Drain embedded GIT (HD-GIT). The structure of the device is shown in Fig.2-9 [23], adopts a p-GaN with recessed gate.

Figure 2-9 Hybrid Drain embedded GIT structure [23]

In order to overcome the current collapse issue, a hybrid drain is adopted as shown by the p-GaN region which is electrically connected to the drain. Holes are injected by the p-GaN during turn off by applying high voltage, which release trapped electrons as shown in Fig.2-10 [23].

Figure 2-10 Hybrid drain releasing holes to ease trapped electrons [23]

2.2.3 Reverse conduction mode

For inductive load applications like converters and inverters, a free-wheeling diode is required to conduct energy from source to drain. For IGBTs, a free-wheeling Schottky Barrier Diode (SBD) is required, while MOSFETs have a parasitic body diode.

The GaN GIT does not have a pn-junction between the drain and source, resulting in no body diode. However, the GaN GIT device is still able to conduct from the source to the drain due to the reverse conduction mode mechanism. The forward mode (transistor mode) and reverse conduction mode of the GaN GIT is shown in Fig.2-11 [28].

When drain-source voltage, V_{DS} , is greater than 0 V and the gate-source voltage, V_{GS} , is greater than the threshold voltage, $V_{GS,th}$, at 1.2 V, the device is allowed to conduct, demonstrating the forward characteristics of the device.

Figure 2-11 Forward and reverse characteristics of GaN GIT [29]

In the condition that V_{DS} is between 0 V and $V_{GD,th}$, if V_{GS} is shorted, the GaN device blocks the current flow as shown in Fig.2-12. As V_{DS} decreases to $V_{GD,th}$, current starts to conduct from source to drain. As V_{DS} continues to decrease, more current is able to flow across the device. As shown, the device functions like a diode and it incurs a voltage drop across the drain and source represented by equation 2.1 [19].

$$V_{SD} = V_{GD,th} - V_{GS} + I_{DS}R_{ON} \quad (2.1)$$

Figure 2-12 Reverse conduction mode condition [29]

From the equation, it shows that we can reduce this voltage drop by increasing the V_{GS} . By doing so, we will operate the GaN in reverse direction like a Field Effect Transistor (FET) and incur conduction loss as shown in the $V_{GS} = 5\text{ V}$ curve in Fig.2-11.

As shown, the GaN GIT is able to operate in reverse direction which reduces the need for a free-wheeling diode and hence reduces component cost. Since the GaN GIT's reverse conduction mode does not involve a diode, it does not incur reverse recovery loss (Q_{RR}) in the free-wheeling diode. As shown in Fig.2-13 [29], the reverse recovery charge of the Si Fast Recovery Diode (FRD) results in the large downward current spike, while the absence of the reverse recovery diode has resulted in a negligible drop for GaN GIT.

The advantage of GaN's reverse recovery mode has resulted in the viability of new power electronics topologies which were previously not able due to Q_{RR} such as totem pole PFC [30] [31] .

Figure 2-13 GaN GIT vs. Si FRD Q_{RR} comparison [29]

2.3 Considerations for driving GaN GIT

It is important to remember that the E-mode GaN HEMTs are different from MOSFET power device in terms of:

- Different device structure
- Smaller parasitic capacitances

Therefore, there are additional considerations for GaN power device gate driver. For this work, particular attention will be paid to the GaN GIT which is a non-insulated gate enhancement mode GaN device.

2.3.1 Non-insulated Gate

For non-insulated gate GaN devices like Panasonic's GaN GIT or EPC's p-GaN gate type, the p-doped layer beneath the gate causes a diode like voltage and current characteristics [19]. During turn on, the higher the gate current, the more current it can supply due to channel modulation [11]. This reduces the on-resistance which results in lower conduction loss. However, this increase in gate current will result in higher gate drive loss. Therefore, a compromise between conduction loss and gate drive loss must be made.

For the GaN GIT, the on-resistance is flattens out when gate current is greater than 1mA. Therefore, a steady stream of forward gate current greater than 1mA must be supplied to keep the device during conduction.

In addition, the vulnerability of the gate is not a gate voltage or current limit, but rather a gate charge limitation. The average gate charge must be kept below the rated value to ensure the device is able to maintain its reliability. This will be further investigated in the next chapter.

2.3.2 Reverse conduction loss

The concept of reverse conduction mode has been explained in chapter 2.2.3. It is to note that there will be a voltage drop across the device as shown in (2.1). This voltage increases as gate to source voltage gets more negative [19]. While it is mentioned that a negative voltage increases the margins to prevent false turn on and increases turn off slew rate, it increases the reverse conduction loss

denoted by (2.2). It shows that this loss also increases with switching frequency and dead time.

$$P_{SD} = V_{SD} \times I_{SD} \times t_{SD} \times f_{sw} = (V_{GD,th} - V_{GS} + I_{DS}R_{ON}) \times I_{SD} \times t_{SD} \times f_{sw} \quad (2.2)$$

2.3.3 Design for smaller parasitic inductance

The low gate charge of the GaN device enables high slew rate to achieve lower switching losses and higher operating frequencies. However, it is equally important to design for low parasitic inductance. The parasitic inductances exist within the package (bond wires and lead frame) and the Printed Circuit Board (PCB). The parasitic inductances limit the slew rate and increase the ringing of V_{GS} and V_{DS} .

In order to study the effects of the parasitic inductance, this work will model the problem using a synchronous buck circuit as shown in Fig. 2-14. The choice of using a synchronous buck circuit is that topologies which are best suited for GaN power device are usually variations the half bridge configuration [32]. The impact will be studied by analyzing 2 current loops from Fig.2-14, the gate drive loop in blue and the power loop in red.

Figure 2-14 Power loop and gate drive loop in a half bridge configuration

2.3.3.1 Gate drive loop

A simplified version of the low side gate drive loop shown in Fig.2-15. The gate inductance is ignored as the source inductance is dominant because the drain current also flows through the source. The PCB and package inductance are lumped together to simplify the model. This parasitic source inductance creates a negative feedback by clamping the gate current and is discussed in a few literatures with calculation and analysis [33] [34].

Figure 2-15 Zoomed in low side gate drive loop

With reference to Fig 2-16a, initially, the gate capacitor is supplied with Q_{GS1} amount of charge so that the V_{GS} is charged to the threshold voltage. Prior to that, there is no current flowing through the device. Q_{GS2} amount of charge is supplied to the device, and V_{GS} increases from $V_{GS,th}$ to $V_{GS,pl}$ as I_{DS} increases from 0 A to load current.

As the current starts flowing from the drain and gate to source, a voltage is generated across the parasitic source inductance (L_s). This will reduce the voltage across the driver output and the device source pin, resulting in a lower gate current. This results in slower charging of Q_{GS2} , which is the component of the gate source charge responsible for the I_{DS} slew rate of the power device. From Fig.2-16, the slope during Q_{GS2} transition is gentler than Q_{GS1} transition. In a hard switching situation, the longer the current transient time, the larger the switching power loss. The same phenomenon also applies during turn off when the device is discharging the gate charge.

Figure 2-16 Gate loop effects on the power device transition phase. A) Turn on B) Turn off

To approach this problem from a mathematical perspective, we take Kirchhoff's voltage law around the gate drive loop to obtain (2.3). Next, we find the gate current by using the charge equation to get (2.4). Substituting (2.4) into (2.3), we get (2.5). From (2.4), it is observed that the larger the parasitic source inductance, the larger the time taken. A larger transition time causes larger switching loss and lower efficiency.

$$V_{drv} = V_{Rg} + V_{gs} + V_{Ls} = I_{Rg}R_g + V_{gs} + \frac{L_s I_s}{t_{Qgs2,on}} \quad (2.3)$$

$$I_g = \frac{Q_{gs2}}{t_{Qgs2,on}} \quad (2.4)$$

$$t_{Qgs2} = \frac{Q_{gs2}R_g + L_s I_s}{V_{drv} - V_{gs}} \quad (2.5)$$

2.3.3.2 Power loop

The power loop as shown in Fig 2-14 is the path that the current flows from the DC-link capacitor through the bus voltage across the devices and to the ground. The parasitic inductance includes the package inductance and routing inductance on the board. The parasitic inductances result in overshoot and ringing at the output [9] [33]. The overshoot voltage increases the drain-source voltage during the transition period and hence increases the switching losses.

Therefore, by integrating the driver and the power device in the same package, parasitic inductances of the gate drive loop and power loop can be reduced to improve the switching performance.

2.3.3.3 Surface mount package

To reduce parasitic inductance, many power device manufacturers started adopting Surface Mount Device (SMD) packaging, contrary to the traditional thru-hole packaging like TO-220 and TO-247, which have larger source inductance [35]. In order to further reduce the parasitic inductances, packages such as Power Quad Flat No-leads (PQFN) are can be used [36]. Some manufacturers, like EPC GaN, offer bare die to be directly mounted on the PCB [9].

2.3.3.4 Kelvin source

To further reduce the gate drive loop inductance, a Kelvin source lead connection is introduced to the package. The 3-pin device connection for half bridge circuit is shown in Fig. 2-17a [32] using cascode structured GaN devices. Transistor T_a represents the high side GaN, while T_b is the low side GaN. Due to the source inductance, the gate drive loop inductance increases significantly and this affects device slew rate. In order to reduce the source inductance, a second source pin, also known as Kelvin source is pulled out of the device [37] as shown in Fig. 2-17b. It reduces the source inductance and the current in the gate drive loop allowing for faster slew rate operation [38].

Figure 2-17 Gate loop inductance reduction. a) Design based on conventional package b) Design based on kelvin source package c) Design based on kelvin source package and signal isolation. [32]

For the configuration at Fig.2-17b, the power ground is connected to the signal ground. Due to the high current in the power ground side, this can lead to ground bounce on the signal side. For this reason, there should be isolation between the power ground and signal ground as shown in Fig 2-17c.

2.3.4 Cross conduction prevention

Cross conduction is a challenging issue for all half bridge related topologies. It is a false turn-on mechanism related to half bridge topologies and high slew rate application. It can result in higher switching losses [39] and can damage the device due to shoot-through. This is a greater concern for enhancement-mode GaN device as they have very low threshold voltages and switch at very high slew rates.

2.3.4.1 C_{GD} induced false turn on mechanism

This false turn on mechanism occurs in a half bridge configuration as shown in Fig 2-14. This occurs when both devices are initially turned off during the dead time and suddenly the high side device is turned on. When the high side device is turned on, the drain source voltage of the low side device is increased.

This induces a current across the gate-drain capacitor of the low side power device. This current flows through the gate resistor of the low side device which induces a voltage across the gate-source pin of the power device potentially resulting in false turn on [40].

The false turn on phenomenon is modelled as shown in Fig. 2-18 and is explained in [41] and various other literature [40] [42]. Using KVL around loop 1-3, we get equation (2.6), (2.7) and (2.8) respectively. Solving it, we will obtain (2.9). From the equation obtained, it shows that the induced voltage is directly proportional to the slew rate and the gate resistance. This is a simplified model of the phenomenon and neglects the impact of parasitic inductances of the circuit.

Figure 2-18 CGD induced false turn on mechanism model

$$\frac{dV_{in}}{dt} = \frac{I_3(t) - I_2(t)}{C_{DS}} \quad (2.6)$$

$$I_2(t) \left(\frac{1}{C_{GS}} + \frac{1}{C_{GD}} + \frac{1}{C_{DS}} \right) - I_3(t) \left(\frac{1}{C_{DS}} \right) - I_1(t) \left(\frac{1}{C_{GS}} \right) = 0 \quad (2.7)$$

$$\frac{d}{dt} \left(R_1 (I_1(t) - I_0(t)) \right) + I_1(t) \left(\frac{1}{C_{GS}} \right) + I_2(t) \left(\frac{1}{C_{GS}} \right) \quad (2.8)$$

$$V_g = \frac{dV_{in}}{dt} \times R_1 \times C_{GD} \times \left(1 - e^{\frac{-V_{power supply}}{R_1 \times \frac{dV_{in}}{dt} \times (C_{GS} + C_{GD})}} \right) \quad (2.9)$$

In order to resolve this issue, 2 measures can be adopted to address the issue.

2.3.4.2 Negative voltage turn off buffer

By having a negative voltage turn off, it creates a margin in case there is a voltage spike. This can be achieved using the RC gate drive method [43] [44] [45] or a negative turn-off voltage using a charge pump [46] or DC rail supply [47]. The usage of negative voltage also helps the gate capacitor to discharge faster.

2.3.4.3 Active Miller clamp

The active Miller clamp function in the driver IC works such that it creates a low impedance path to ground when the low side is turned off [48], hence reduce the induced voltage. It has been experimentally shown that reducing the gate impedance reduces the effects of cross conduction [49] [39] and prevent shoot through [48].

Chapter 3

GaN GIT Gate Driving Techniques

Novel ideas and circuits have to be implemented, in order to handle the considerations highlighted in the previous chapter. In this chapter, 2 types of GaN GIT based gate drive circuits will be discussed:

- Capacitor-less type gate drive circuit
- Capacitor type gate drive circuit

3.1 Capacitor-less gate driver

In the previous chapter, the benefits of low parasitic inductance is explained. Multi-chip integration is a good strategy to reduce the package and PCB inductance. In order to do so, one needs to consider a solution where no discrete devices are involved. For this reason, capacitor-less gate drivers are considered. In addition, power MOSFETs typically adopt a capacitor-less gate drive solution like the R-type gate drive method as shown in Fig.3-1.

This section will investigate:

- R-type gate drive and its limitations with GaN GIT
- Other capacitor-less gate drive methods
- Proposed 2-stage, 2-phase capacitor-less gate drive method

3.1.1 Resistor gate driver

This is the most common method for gate driving for power transistors for its simplicity as shown in Fig. 3-1. During turn on, current is channeled through RA1 into the gate of the GaN power transistor and during turn off, current is discharged through RA2 and RA1. The additional path of RA2 and DA1 is to provide a low impedance path to reduce the effects of cross conduction.

Figure 3-1 Driving mechanism of R-type gate drive

3.1.1.1 Design considerations for GaN GIT

In order to ensure reliability of the GaN gate, it is important to keep the gate pulse current ($I_{G,P}$) and gate DC current ($I_{G,av}$) below the absolute maximum ratings (I_{GP} and I_G). For the R-type gate driver, the gate pulse and DC current can be calculated in equation (3.1) and (3.2) respectively. It is to note that for the R-type gate drive method, the current path for turning on the GaN GIT and providing DC gate current is the same path through resistor RA1.

$$I_{G,P} = \frac{(V_{DDA} - V_{pl})}{RA1} \quad (3.1)$$

$$I_{G,av} = \frac{(V_{DDA} - V_{Dr})}{RA1} \quad (3.2)$$

3.1.1.2 $I_{G,P}$ and $I_{G,av}$ limitations for R-type gate drive

This work will be studying the 600 V, 140 m Ω GaN GIT [50] which have absolute ratings of $I_G = 19$ mA and $I_{GP} = 0.6$ A. The equation (3.1) is simulated by varying VCC from 3.6 V to 15 V and RA1 from 25 Ω to 100 Ω to check whether $I_{G,P}$ is in the safe region (<0.6 A). The calculation results are shown in Fig.3-2a, which shows that the maximum value of $I_{G,P}$ is lesser than the I_{GP} limits.

(a)

(b)

Figure 3-2 a) $I_{G,P}$ values of R-type driver based on various R and VCC values b) $I_{G,P}$ values within the I_G limits.

Using equation (3.2), the values of $I_{G,P}$ which exceed the I_G limits are filtered out and shown in Fig.3-2b as they are beyond the safe operating limits of the gate. It is observed that the R-type gate drive is limited to use $VCC < 5$ V and higher

RA1 values are better to keep $I_{G,AV}$ low. However, this reduces $I_{G,P}$ and subsequently slew rates.

3.1.1.3 Slew rate limitations for R-type gate driver

Using the $I_{G,P}$ values found in the previous section and the slew rate using the equation (3.3), the VDS slew rate values that the R-type gate driver is able to achieve are shown in Fig 3-3. The maximum slew rate we can get is 33.6 V/ns using $V_{CC} = 3.9$ V and $RA1 = 25 \Omega$. The choice of using $V_{CC} = 3.9$ V is risky as it is close to the UVLO value of the gate driver. A more practical approach is to use a higher voltage (>4.3 V) and higher resistor ($>45 \Omega$)

$$\frac{dV_{DS}}{dt} = \frac{\Delta V_{DS} \times (V_{DDA} - V_{GS,pl})}{Q_{GD} \times RA1} \quad (3.3)$$

Figure 3-3 Maximum slew rate values that can be achieved for GaN GIT using R-type gat drive method

3.1.2 Other implementations of capacitor-less type gate drivers

A capacitor-less gate-drive circuit was proposed to provide a capacitor-less solution to increase the possibility of integration [50]. This method has lesser reverse conduction loss because there is no negative gate voltage during turn off. In addition, it requires lesser off chip components, allowing for more compact Printed Circuit Board (PCB) design.

In [51], the three-level driving method for GaN power transistor in synchronous Buck converter was implemented. This method put a positive bias voltage on the gate-source of synchronous rectifier GaN device during the dead time. This causes the reverse conduction voltage drop to decreases and hence reduces reverse conduction loss.

3.1.3 2-stage gate driver

Another form of capacitor-less gate driver is the 2-stage gate drive method which was presented previously as a means of driving SiC JFET [47]. The circuit diagram of the 2-stage gate driver is as shown in Fig. 3-4. Firstly, it consists of a dead time circuit to prevent shoot through in the output stage power MOSFETs MP1, MP2 and MN1. This is followed by a one shot circuit to achieve the 2-stage function by supplying 2 sources of current during turn on. The first source is a high current pulse which lasts for a shorter period of time relative to the ON pulse to charge up the gate capacitor to turn on the power transistor fast. The second source is a low current path which serves to supply current into the gate in order to keep the device functioning during conduction. A buffer stage is implemented to drive the power MOSFETs MP1, MP2 and MN1.

Figure 3-4 2-stage driver circuit

The functionality of the GaN GIT is shown in Fig. 3-5. At T1, the input is set to high. There will be propagation delay within the dead time circuit block such that the $V_{GS,MN1}$ will be turned off by T2. The purpose of the dead time circuit is to ensure that MP1 and MP2 do not turn on the same time MN1 is turned off as there is a possibility for shoot-through. A 1ns dead time is implemented and MP1 and MP2 are turned on at T3.

At T3, MP1 and MP2 are turned on. MP1 is designed to be the high current path for fast turn on, while MP2 is designed to be the low current path for conduction current. When $V_{GS,GaN}$ is charged to the threshold voltage, $V_{GS,th}$, the $I_{DS,GaN}$ will

start to increase. $I_{DS,GaN}$ increase to the maximum when the $V_{GS,GaN}$ reaches the $V_{GS,pl}$ and the $V_{DS,GaN}$ starts to drop. The gate capacitor is fully charged at the $V_{GS,f}$. When the device is fully turned on, the GaN GIT devices functions demonstrate a diode characteristic such that the $V_{GS,GaN}$ is clamped to a voltage of approximately 3-4V based on the $I_{GS,GaN}$. The gate current drops after the device is fully charged. MP1 is designed such that its turn on time, $T_4 - T_3$, is larger the designed turn on time of the device (approximately 30ns) so as to ensure that MP1 can fully turn on the device.

Figure 3-5 2-stage driver time chart for GaN GIT

MP1 is turned off at T_4 and only MP2 is supplying current to keep the device in conduction, with a forward gate current in the region of 10mA. Because the gate current supplied is lesser, we start to see a drop in the gate voltage. At T_5 , the input pulse, IN, is turned off and after some propagation delay, MP2 is turned

off at T6. Due to the dead time circuit, MN1 is turned on at T7 and the input capacitance of the GaN GIT is discharged and the device is turned off.

3.1.4 2-stage 2-Phase GaN GIT Gate Driver

3.1.4.1 Gate ringing during high slew rate operation

When designing power electronics, the engineer will design the driver to switch the power transistor at a high slew rate in order to minimize the switching loss. Switching at a high slew rate will also reduce the minimum on time and allowing the converter to switch at high frequencies in order to increase power density. GaN power transistors, which has a lower gate charge compared to Si power transistors, takes a shorter amount of time to turn on with the same amount of current.

GaN GIT has low threshold voltage, and forward voltage. This is advantageous as the driver switching loss can be reduced through lower gate drive switching and conduction loss. However, when switching with large gate current to allow for high slew rates, gate ringing becomes a potential challenge that should be addressed. The gate ringing due to parasitic inductance is model with the gate drive circuit and GaN GIT as shown in Fig. 3-6, gate resistance has been ignored for simplicity.

Figure 3-6 Parasitic for driver circuit

From Fig. 3-6, during T3, the driver provides a large current (approximately 1-2A) to drive the power transistor at a large slew rate. The presence of the parasitic inductance creates 2 effects. Firstly, it clamps the gate current and can affect the slew rate of the device. In order to overcome this, engineers can adopt power transistors with kelvin source or adopt SMD packages which have lower parasitic inductance. Secondly, it can result in voltage ringing at the gate. Taking Kirchhoff voltage law around the loop in Fig. 3-7 to get (3.4), one would note that a positive voltage will be generated across the parasitic gate and source inductance denoted by L_{gate} and L_{source} respectively. This will create a voltage spike and ringing in the gate.

$$V_{drv} = V_{gs} + L_{Gate} \frac{di_{L,gate}}{dt} + L_{Source} \frac{di_{L,Source}}{dt} \quad (3.4)$$

During T4 of Fig. 3-6, MP1 is turned off, causing a sharp drop in the gate current to the power transistor. A negative voltage generated across the parasitic inductances in according to (3.4) leading to a voltage dip and gate voltage ringing.

3.1.4.2 2-stage 2-Phase GaN GIT Gate Driver

In order to reduce the gate ringing as explained in the previous section, this work develops a 2-phase output for the high current stage as shown in Fig. 3-7.

Figure 3-7 Proposed 2-phase 2-stage driver circuit

The proposed solution splits the high current P-MOS, MP1, from the conventional design into 2 channels denoted by MP1A and MP1B. The transistor sizing for MP1A and MP1B is designed using (3.6) based on half the

current requirement from using (3.5). This is to achieve the desired current when MP1A and MP1B are turned on. A phase shift delay block is added to generate 2 signals from the original signal with a small delay between them which will serve as the control signals for MP1A and MP1B. The time chart for the functionality of the proposed circuit is illustrated in Fig.3-8.

$$I_{G,GaN\ GIT} = \frac{Q_{GD,GaN\ GIT}}{V_{DS,GaN\ GIT}} \times \frac{dV_{DS,GaN\ GIT}}{dt} \quad (3.5)$$

$$\frac{W}{L} = \frac{I_{DS}}{\mu C_{ox}((V_{DD}-V_{TH}) \times V_{DS} - 0.5 \times V_{DS}^2)} \quad (3.6)$$

Figure 3-8 2-phase 2-stage driver time chart for GaN GIT

At T3, MP1A and MP2 are turned on. As MP1A is designed to be the first step for the large current path, $I_{GS,GaN}$ increases to charge the C_{iss} . After a small delay of 5ns, at the time T4, MP1B is turned on and the gate current increases to the intended current to allow high slew rate. This method makes the rate of change of the gate current slower than conventional design resulting in lesser gate voltage ringing and voltage spikes. V_{DS} falls when the driver is charging the C_{GD} of the GaN GIT at the $V_{GS,pl}$. Hence, high slew rate for V_{DS} will remain unchanged if MP1B is turn on before V_{GS} reaches $V_{GS,pl}$.

When the device is fully turned on at the $V_{GS,f}$, the $I_{GS,GaN}$ will fall and $V_{GS,GaN}$ is clamped at 3-4V. MP1A is turned off at T5 and $I_{GS,GaN}$ falls as driver impedance increases. The $I_{GS,GaN}$ further falls as MP1B is turned off, leaving only MP2 on to supply a small amount of current for the device to remain in conduction. By reducing the current in steps, it reduces the rate of change of gate current resulting in a smaller voltage dip

3.1.5 Design considerations and limitations

In order to allow for a high slew rate of the GaN transistor, MP1 is designed to have a small R_{on} so that it can source a large current to charge the input capacitance of the GaN GIT. The equation for the gate drive current requirement is shown in (3.5) which are important to use for transistor sizing the MOSFET MP1. During conduction, a small amount of current required to maintain turn on for the GaN GIT, in the region of 10 mA, which is used for transistor sizing of MP2. The transistor sizing for MN1 is to allow for fast turn off of the GaN device and to allow low sink impedance to reduce the effect of C_{GD} induced false turn on. For transistor sizing for MOSFETs can be shown in (3.6).

This explanation does not account for the effects for the gate resistor R1. As R1 increases, the influence of the on-resistance of MP1A and MP1B on the gate current becomes less significant as shown in (3.7). In applications where high slew rates are not required, R1 will be larger than the on-resistance of MP1A and MP1B. This is acceptable as the 2-phase function is aimed at high slew rate and hence high gate current applications, where gate voltage ringing will arise. At slower drain-source voltage slew rate and lower gate current, the gate ringing is

reduced. In addition, the time delay between OUTA and OUTB is small and will not affect the performance of slow slew rate applications.

$$R_{equivalent} = \frac{R_{on,MP1A} \times R_{on,MP1B}}{R_{on,MP1A} + R_{on,MP1B}} + R_1 \quad (3.7)$$

3.1.6 Simulation

This work is simulated on cadence using AMS 0.18 μm process. The setup for the test circuit is shown in Fig. 3-9. For this simulation, resistor load simulation test is adopted as the setup is able to achieve the desired $I_{DS,GaN}$ in a shorter simulation time, hence saving simulation time and resources. The low voltage and high voltage supply is set to 5 V and 400 V respectively. In order to simulate $I_{DS,GaN}$ at 8 A, the load resistor, R_{load} , is set to 50 Ω . The circuit under test is represented by the circuit enclosed in the dotted box in Fig. 3-4 and Fig. 3-7.

Figure 3-9 Resistor load simulation test setup

The first set of simulation is conducted to test the circuit without the presence of parasitic inductances to compare the turn on waveform against the graphs in Fig. 3-5 and Fig. 3-8. The simulation results for the conventional and proposed design are shown in Fig. 3-10 and Fig. 3-11 respectively.

Figure 3-10 Simulation of turn on characteristics of conventional design without parasitic

Figure 3-11 Simulation of turn on characteristics of proposed design without parasitic

Comparing the graphs, the simulated waveforms are similar to the ideal waveforms. When the gate capacitor is fully charged and device is fully turned on, the GaN GIT gate shows some diode characteristics as the voltage gets clamped based on the gate current and the gate current starts to drop. In Fig. 3-10, it is observed that the gate voltage slightly rises before turning on fast. This

is because of the timing mismatch between MP1 and MP2 such that MP2 turns on before MP1.

The next set of simulation is conducted with the inclusion of the gate inductance. Inductance of 2nH is added to the gate, drain and source of the GaN GIT model, which are close to the values of a Surface Mount Device (SMD) package. The simulation graphs for the conventional and proposed design with parasitic inductance are shown in Fig. 3-12 and Fig. 3-13 respectively.

Figure 3-12 Simulation of turn on characteristics of conventional design with parasitic

The presence of parasitic inductance clamps the rate of change in gate current and slows down the slew rate of the drain source voltage. It also introduces ringing at the gate current and voltage. In the simulation results, when the high current path is turned off, the dip in gate voltage is much smaller by adopting the proposed method compared to the conventional method. With the conventional method, the V_{gs} falls to 0.231 V, but with the proposed method it falls to 1.27 V.

Table 3-1 summarizes the results of the 4 simulations by showing the slew rate and the minimum V_{gs} . For practical discussion, engineers should consider the comparison of the conventional and proposed design with parasitic. The differences between the slew rates for the 2 different methods are small. It also shows that the proposed design greatly reduces the ringing at the gate source

voltage. Comparing the compromises to be made, it shows that the proposed method benefits high frequency and high slew rate switching applications.

Figure 3-13 Simulation of turn on characteristics of proposed design with parasitic

Table 3-1 Summary of simulation results

Test	VDS slew rate (V/ns)	VGS,min (V)
Conventional method with parasitic inductance	50.69	0.231
Proposed method with parasitic inductance	45.65	1.27

Simulation is conducted by varying R1 to verify the effects of R1 on the gate voltage when MP1A and MP1B are turned off in the proposed circuit. The simulation waveform is shown in Fig. 3-14. The resistances are varied from 0Ω, 2.5 Ω and 5 Ω and are denoted by the dot, dash-dot and straight lines respectively. MP1A is turned off at time, T1. It is shown that the lower the resistance, the larger the drop in gate voltage. This is because the rate of change of gate current is much larger resulting in a larger V_L .

Figure 3-14 Effects of variation of R1

At time T2, where MP1B is turned off, for a larger resistance, the lower the level of the gate voltage. This is because the lower resistance path has a higher current which charges the gate voltage back up after it drops. The narrow time difference between T1 to T2 does not allow the larger resistance option to charge back to the corresponding gate voltage for that gate current. At T2, the rate of change in gate current is comparable. This results in the larger resistance option falling to a lower voltage. However, subsequent increase in R1 does not result in further drop in R2. This is because the gate voltage barely increases beyond the 5Ω value.

3.2 Capacitor type gate driver

Capacitor type gate drivers are implemented for IGBT devices to generate a negative voltage turn-off using a unipolar supply. A common implementation is the RC-gate driver as shown in Fig.3-15.

This is beneficial for the GaN GIT device:

- The negative voltage can allow fast turn-off characteristics and cross conduction protection.
- Allows the GaN power transistor to be driven at a higher voltage for faster slew rate.

- The RC-gate drive method allows the GaN device to be driven optimally with off-the-shelf MOSFET drivers.

However, this method requires a capacitor in the magnitude of nanofarads, which large to be implemented on a chip and makes it difficult for integration of GaN device with the driver.

3.2.1 RC gate drive method

The functionality of the RC gate drive circuit will be explained using Fig. 3-15. RB2 serves to control the forward gate current of the GaN GIT during turn on conduction and is decided using (3.8). The supply voltage for the gate driver is denoted by VDD. Resistor RB1 is designed to set the slew rate of the GaN GIT and is designed based on (3.9). The resistor sizing for RB1 is smaller than RB2 by at least an order of 1. This is to supply a large current to turn on the device fast. The capacitor CB1 serves to separate the high current route and the low current route and to enable negative voltage turn off. CB1 is designed using (3.10).

Figure 3-15 RC-type gate drive circuit

$$RB2 = \frac{VDD - V_{GS,f}}{I_{GS}} \quad (3.8)$$

$$RB1 = \frac{(VDD - V_{GS,pl}) \times V_{powersupply}}{\frac{dV_{DS}}{dt} \times Q_{gd}} \quad (3.9)$$

$$\frac{Q_{g,forward}}{VDD - V_{GS,f}} < CB1 < \frac{Q_{g,max}}{VDD - V_{GS,f}} \quad (3.10)$$

When the GaN device is turned on at T1, current flows through RB1 and RB2, but a larger amount of current flows through RB1 due to the lower resistance. When the device is fully charged up at T2, the capacitor CB1, which is connected in series with RB1, blocks the current flow. This results in current flowing through RB2 that keeps the device in conduction.

When the device is turned off at T3, the positive end of the capacitor is connected to GND and the negative end is connected to the gate. This results in negative voltage turn off, which allows for faster turn off slew rates and creates a voltage margin in case of false turn-on.

The advantage of this type of circuit is that it allows the off-the-shelf drivers to control the gate current to the GaN device during conduction which reduces the current consumption compared to R-type gate drive method [44]. In [44], a comparison is made between RC and R-type gate drive method. While the R type gate drive circuit is simpler, the gate drive loss is higher by 50 times. Therefore, the designer needs to consider if this gate drive loss is worth the simplicity in design.

It is also able to provide a negative voltage turn off to provide a voltage margin in case of false turn on. Due to the RC circuit, negative voltage will discharge based on the RC constant. This will increase reverse conduction loss. Various literatures have attempted to resolve this issue [45] [43] [52].

3.2.2 Variants of RC-gate drive method

In [53], an additional discharge path was proposed to discharge the negative voltage during turn off to reduce turn-on loss of the GaN device. This method also enabled the reduction of reverse conduction loss.

In [43], an active discharged-type gate drive circuit proposed to decrease the reverse conduction loss of GaN device due to the negative voltage turn-off of the RC gate drive circuit. In [45], the inverter type gate drive method is proposed to solve the same problem as the active discharge method, which is to accelerate the discharge period of the negative voltage in order to reduce reverse conduction loss. The advantage of this method is that it doesn't use a clamp diode, unlike the active discharge method, so it consumes lesser space.

While in [54], an additional circuit was introduced to the RC-type gate drive method to improve the reliability by creating a fixed negative gate voltage to prevent cross conduction. In addition, the gate driver was design for transient performances to be independent from duty cycle. From the evaluation results, the authors were able to driver the devices up to 500 V/ns.

3.2.3 GaN GIT gate driver with active Miller clamp and speed up capacitor discharge function

A single channel GaN GIT gate driver Application Specific Integrated Circuit (ASIC) utilizing a novel gate drive method will be compared to the R-type and RC-type gate drive method shown in Fig. 3-16. Firstly, the functionality of the gate driver IC will be introduced. Next, this chapter examines how the gate driver IC improves the slew rate performance and the cross conduction protection functions. It discusses additional performance and reliability advantages and finally the experimental results.

Figure 3-16 Various gate drive methods a) the R-type b) the RC-type

3.2.3.1 Proposed gate drive strategy

The simplified gate drive circuit for the GaN GIT gate driver IC, AN34092B [55], is shown in Fig. 3-17a below. The gate driver IC has 3 output pins, namely OUT1, OUT2 and OUT3. OUT1's purpose is to charge the GaN power transistor during turn ON phase and discharging the speed-up capacitor C1 during turn off.

OUT2 supplies an adjustable DC current of 2.5 mA – 25 mA during conduction phase and provides a low impedance path using the active Miller clamp function. Integrated within the IC is an adjustable current source which is able to provide a constant current during turn ON, that is important for the conductivity modulation of the GaN GIT.

OUT3 is responsible for the discharge path by pulling the gate to the negative voltage VEE. The turn off slew rate can be controlled using resistor R2. Another integrated function is a charge pump to provide the negative voltage, VEE, during turn OFF, which is adjustable using an external resistor.

Figure 3-17 a) GaN GIT gate driver IC circuit b) Gate driver timing diagram

The gate control waveforms are shown in Fig. 3-17b. During T1, the input signal, V_{INP} , to the driver is pulled low. Outputs are pulled down to VEE; OUT1 discharges the speed-up capacitor C1. At the start of T2, V_{INP} is turned on and there is a 50 ns propagation delay till T3.

At T3, the outputs are pulled high. V_{OUT1} is pulled up to VCC allowing a large amount of current to flow into the gate to turn on the power device with a large slew rate. The user can control the slew rate by tuning resistor R1. Simultaneously, V_{OUT3} is pulled to high impedance, turning off the current sink at OUT3. When the GaN GIT is fully turned on, capacitor C1 will block the high current path at OUT1. OUT2 will supply an adjustable gate current to keep the device in conduction. During T4, V_{INP} will be pulled down. There will be a propagation delay of 50 ns before the output pins are pulled down to VEE.

3.2.3.2 High slew rate gate drive

Power density and efficiency are important metrics in power electronics. High slew rate operation allows reduction of the minimum on-time of the converter resulting in higher power density due to smaller passive components at high frequency operation. In addition, higher slew rates result in an improvement in the switching losses which result in higher efficiency.

The ability to charge and discharge faster means higher slew rates for the power device. A general equation of V_{DS} turn-on and turn-off slew rate is shown in equation (3.11) and (3.12) respectively. The fall and rise in the drain-source

voltage, V_{DS} , occur during the charging and discharging of the gate-drain charge, Q_{GD} , which occur at the plateau voltage, V_{pl} .

The general equation of I_{DS} turn-on and turn-off slew rate is shown in equation (3.13) and (3.14) respectively. The rise and fall in the drain source current, I_{DS} , occurs when the gate driver charges and discharges the gate from the threshold voltage, V_{th} to V_{pl} , which corresponds to the gate charge, Q_{GS2} .

$$\frac{dV_{DS}}{dT_{turn\ on}} = \frac{(V_{DD} - V_{pl}) \times \Delta V_{DS}}{R_{gate} \times Q_{GD}} \quad (3.11)$$

$$\frac{dV_{DS}}{dT_{turn\ off}} = \frac{(V_{pl} - V_{EE}) \times \Delta V_{DS}}{R_{gate} \times Q_{GD}} \quad (3.12)$$

$$\frac{dI_{DS}}{dt_{on}} = \frac{(V_{DD} - \frac{V_{pl} + V_{th}}{2}) \times \Delta I_{DS}}{R_{gate} \times Q_{GS2}} \quad (3.13)$$

$$\frac{dI_{DS}}{dt_{off}} = \frac{(\frac{V_{pl} + V_{th}}{2} - V_{EE}) \times \Delta I_{DS}}{R_{gate} \times Q_{GS2}} \quad (3.14)$$

From the equations (3.11)-(3.14), slew rate improvements can be achieved by controlling gate current and choosing a device with a small Q_{GD} . The high breakdown electric field of GaN material allows the GaN GIT to be fabricated smaller compared to Si power MOSFETs of similar breakdown voltage, which results in smaller parasitic capacitance and correspondingly smaller Q_{GD} . To control the charging and discharging of gate current, one can choose to control the value of the gate resistor or adjust the gate driver source and sink voltage.

3.2.3.2.1 Turn-on: Dual current source paths for gate protection

To protect the GaN GIT's gate from damage, it is important to keep the gate pulse current and gate pulse charge below the absolute limit. However, controlling the turn-on gate current source through a single path like the R-type gate drive method limits the peak gate current, which is responsible for high slew rate performance. On the other hand, the GaN GIT driver IC and RC-type gate drive provide 2 current paths, a high current path during turn-on transients for high slew rate performance and a low current path to keep the GaN GIT in conduction, to not damage the gate.

The high current source path of the GaN GIT driver IC and RC-type gate driver comprises a resistor in series with a capacitor. When the power device is fully

turned on, the capacitor will block current flow, protecting the gate of the GaN GIT. This allows the GaN GIT driver IC and RC-type gate driver to drive the GaN GIT at a higher supply voltage, resulting in a higher gate current and larger turn-on slew rate. This is supported by equation (3.11) and (3.13), which shows that a higher VDD increases slew rate.

3.2.3.2.2 Turn-on: Discharging speed-up capacitor to improve turn-on slew rate

For RC circuit, turn-on slew rate is affected by negative voltage of the speed-up capacitor, CB1 on Fig. 3-16b, prior to turning on as current supplied by the driver needs to discharge CB1. The GaN GIT driver IC resolves this problem with a high speed discharge circuit to discharge C1. Fig. 3-18 shows the schematic of the outputs of the proposed GaN GIT driver IC in Fig. 3-17a.

Figure 3-18 GaN GIT Gate drive IC output schematic

Referring to Fig. 3-18 and the timing diagram in Fig. 3-17b, when transistor PSW is off, transistor DISSW is activated which discharges the capacitor C1. So when transistor PSW is activated during T3, it is able to charge the GaN GIT gate from 0V.

3.2.3.2.3 Turn-off: Negative voltage

The GaN GIT driver IC and RC type gate drive generates a negative voltage turn-off. The RC-type gate driver relies on the connection of the speed-up capacitor, CB1, to create a negative voltage during turn off as explained in the previous section. This negative voltage decays with a RC time constant as it is discharged through RB1 and RB2.

On the other hand, the GaN GIT driver IC has a built in charge pump to generate an adjustable negative rail, VEE, from -3 V to -5 V. According to equation (3.12) and (3.14), negative voltage turn-off allows larger gate discharging current leading to larger turn-off slew rates compared to R-type gate drive circuits which discharge at 0 V.

3.2.3.3 Cross conduction protection

Cross conduction is a false turn-on mechanism which occurs when the high side device is turned on during dead time. When the high side device is turned on, the drain of the low side power transistor is pulled up, inducing a current across the gate-drain capacitor of the low side power device. This current causes a voltage across the gate-source pin of the power device as it flows through the gate resistor. Research showed that the induced voltage is affected by slew rate and gate resistance [41]. For high slew rate power devices, these are practical challenges which need to be addressed. This work aims to reduce V_{GS} spike voltage without sacrificing slew rate performance. There are various countermeasures to reduce the effects of cross conduction.

3.2.3.3.1 Low gate impedance

A common countermeasure using the R-type gate drive for cross conduction protection is to implement a low impedance discharge path through the Schottky barrier diode (DA1) in series with a small resistor (RA2) as shown in Fig.3-16a. During turn off, this forms a very low impedance path which sinks the induced current to GND. In this method, the slew rate is dependent on the cross conduction protection.

Unlike the R-type gate drive which has only one output to sink the gate current, the GaN GIT driver IC has 2 gate sink paths. One path (OUT3) to control the GaN GIT gate discharge current to control the slew rate and another path (OUT2) for active Miller clamp function which implements low gate impedance during the cross conduction period and reduces gate ringing as shown in Fig. 3-19a. Making reference to the timing diagram in Fig. 3-19b, at t_1 , the pull down transistor NSW is turned on and the turn off slew rate is controlled by the resistor R2. The GaN GIT gate voltage is measured and compared to 0V using an operational amplifier as shown in Fig. 3-19a. When the gate voltage falls

below 0V, transistor CLMPSW is activated at t_2 with a typical on-resistance of 0.5Ω to prevent erroneous turn ON. This proposed strategy allows slew rate control which is independent of the active Miller clamp protection function.

Figure 3-19 (a) Schematic and (b) timing diagram of Cross conduction protection function of the GaN GIT driver IC

3.2.3.3.2 Negative voltage

Implementing a negative gate-source voltage during turn off creates a voltage buffer between V_{GS} and V_{th} to prevent the GaN GIT from turning on when cross conduction occurs. The RC-type gate drive creates a negative voltage across the VGS during turn-off due to the change in polarity of the speed up capacitor CB1. On the other hand, the GaN GIT driver IC has built-in negative voltage rail to create this voltage buffer. These 2 methods are able to create a negative voltage rail with a unipolar voltage supply, which saves Bill of Materials (BOM) cost.

3.2.3.3.4 Additional reliability features

3.2.3.3.4.1 Reverse conduction loss

The GaN GIT does not have a pn-junction between the drain and source and therefore no body diode, unlike Si. However, it is able to conduct current due to its reverse conduction mechanism. When reverse conduction occurs, the device will experience a voltage drop across the source and drain as shown in equation (3.15), for $V_{GS} < V_{th}$, and equation (3.16), for $V_{GS} > V_{th}$ [56]. This voltage drop will result in dead time loss as shown in equation (3.16).

$$V_{SD} = V_{GD,th} - V_{GS} + I_{SD}R_{sd,rev} \quad (3.15)$$

$$V_{SD} = I_{SD}R_{sd,rev} \quad (3.16)$$

$$P_{SD} = 2 \times f_{sw} \times \int_0^{Dead\ time} (V_{SD} \times I_{SD}) dt \quad (3.17)$$

From equation (3.15), it is observed that the forward voltage drop across the GaN GIT increases with negative gate voltage. This results in an increase in the reverse conduction loss as shown in equation (3.17). The negative gate voltage during turn-off of the RC-type gate drive and GaN GIT driver circuit can be shown below in Fig.3-20a and 3-20b respectively.

Figure 3-20 VGS during turn off of the (a) RC-type gate drive and (b) GaN GIT gate driver

For the RC-type driver, the negative voltage during the turn-off phase follows equation (3.18) and decays exponentially. V_{n0} is the negative V_{GS} gate voltage the instance the device is turned off. If the intended designed negative gate source voltage during cross conduction for the RC-type and GaN GIT gate driver is the same, for example -5V according to Fig.3-20a, the V_{n0} for the RC-type gate driver is more negative, implying a larger reverse conduction loss.

$$V_{GS(toff)} = V_{n0} e^{\frac{-t_{off}}{\tau_{\omega}}} = (V_{GS,f} - VDD \times \frac{CB1}{(CB1+C_{iss})}) e^{\frac{-t_{off}}{RB2 \times (CB1+C_{iss})}} \quad (3.18)$$

3.2.3.4.2 Forward gate current

Due to the conductivity modulation of the GaN GIT, a small amount of forward gate current needs to be supplied to the gate of the GaN in order to keep it turned on. For the 600 V/10 A GaN GIT (PGA26E19BA), the recommended gate current is 5 mA. Resistor RA1 and RB2 set this gate current for R-type and RC-type gate drive respectively. For bridge configurations circuits, the RA1 and RB2 for the high side GaN GIT are designed to accommodate the minimum bootstrap voltage. A higher bootstrap voltage will result in a larger gate forward current. While a larger gate forward current does not affect the performance as on-resistance for PGA26E19BA is stable beyond 1 mA, it increases the gate drive loss.

For the GaN GIT driver IC as shown in Fig. 3-17b, OUT2 is a constant current source which is adjustable by an external resistor. This allows the user to set a consistent forward gate current for all bootstrap voltages.

3.2.3.5 Experiment results

3.2.3.5.1 Experiment setup

The evaluations are conducted using 600 V, 10 A SMD GaN GIT. R-type and RC-type gate drive are tested using SWEVB005-PGA26E19BA half bridge evaluation board (Fig 3-21a), while the GaN GIT gate driver IC (AN34092B) is tested using SWEVB008-PGA26E19BA half bridge evaluation board (Fig. 3-21b). The purpose is to keep the parasitic inductance of the gate drive loop and power loop similar across the 3 evaluation setups.

Double pulse test was conducted using an inductive load at 400 V bus voltage. It was tested at load currents of 2.5 A, 5 A, 7.5 A and 10 A. Since it is a half bridge circuit, the slew rates for the low side and high side GaN GIT are measured. The gate-source voltage of the low side is probed during high side test to study the cross conduction protection.

Figure 3-21 Experiment setup for (a) R-type and RC-type gate drive method and (b) GaN GIT gate driver IC

The driving methods are tested using a half bridge configuration with settings based on Fig.3-16 and Fig.3-17a as shown below in Table 3-2. The R-type gate driver is designed with the maximum gate charge and current consideration as discussed in section 3.1.1.2. The gate drive voltage is decided to be 5V, which is above the forward voltage of 3.2V and within a region where the gate charge will not be over the limit of 12nC. Using (3.3) and designing with a target slew

rate of 25V/ns, RA1 is calculated at 52.8 Ω , therefore 51 Ω was chosen. To ensure a low impedance path is available for cross conduction protection, RA2 is decided at 1 Ω .

The RC gate drive method is designed using the equations (3.8), (3.9) and (3.10). The presence of CB1 allows the gate driver design to accommodate a higher gate drive voltage without the gate charge concerns of the R-type gate drive method. This is accomplished by controlling the gate current using RB2, which is be calculated using (3.8). 12 V is used as it is common power supply voltage. RB1 is calculated using (3.9), designed for a slew rate of 50 V/ns with a residue voltage in CB1 of 3.2 V. This will give RB1 a value of 56.8 Ω . RB1 was chosen as 51 Ω to provide more gate current as parasitic inductances can slow down the slew rate. The residue voltage in CB1 prior to turn on can slow down the slew rate as it will reduce the gate drive voltage during turn on. (3.10) provides us a range to choose CB1 and the mean value is calculated and chosen to be 1.2 nF.

The calculation for the GaN GIT gate driver IC is very similar to the RC-type gate driver. The gate drive voltage of 12V was chosen for the GaN GIT gate driver IC so that it can be a fair comparison with the RC-type gate drive method. R1 was chosen as 51 Ω illustrate how the speed-up capacitor discharge function can help improve the slew rate. Turn on slew rate is calculated to be 81 V/ns. R2 is chosen as 1 Ω for fast turn off.

Table 3-2 Design parameters and values for experiment

	VDD	V _{Negative}	Component 1	Component 2	Component 3
R-type gate drive	5 V	Nil	RA1 = 51 Ω	RA2 = 1 Ω	DA1 = SBD
RC-type gate drive	12 V	-5 V	RB1 = 51 Ω	RB2 = 2700 Ω	CB1 = 1.2 nF
GaN GIT gate driver IC	12 V	-5 V	R1 = 51 Ω	R2 = 1 Ω	C1 = 120 pF

3.2.3.6 Slew rates results

The V_{DS} turn-on and turn-off slew rate results were taken from 10 % - 90 % and waveforms are shown in Fig. 3-22 and Fig. 3-23. The waveforms are taken at I_{DS}

$=10\text{ A}$ and $V_{DS} = 400\text{ V}$. From Fig 3-22, it is observed that the V_{GS} is charged up slower for the R-type gate drive (Fig. 3-22a) compared to the RC-type (Fig. 3-22b) and GaN GIT gate driver (Fig. 3-22c). This is because the RC-type and GaN GIT gate driver charges the gate up with $V_{DD} = 12\text{ V}$, allowing more charge to be supplied compared to the R-type gate drive which have $V_{DD} = 5\text{ V}$ supply. This results in a faster V_{DS} slew rate.

Figure 3-22 Double pulse waveform for a) R-type, b) RC-type and c) GaN GIT gate driver during turn-off

Figure 3-23 Double pulse waveform for a) R-type, b) RC-type and c) GaN GIT gate driver during turn-on

With reference to Figure 3-23, VGS for the R-type gate drive (Fig. 3-23a) is turned off at 0 V, while the RC-type (Fig. 3-23b) and GaN GIT gate driver (Fig. 3-23c) is turned off with a negative voltage. The negative voltage of the RC-type circuit is decaying to 0 V as the capacitor discharges while the GaN GIT gate driver is held at -5 V until the next turn on cycle.

The results for the low side slew rates are shown in Figure 3-24, which illustrate the turn-on (Fig. 3-24a) and turn-off (Fig. 3-24b) slew rates. From Fig. 3-24a, the GaN GIT has the highest turn-on slew rate (97 V/ns) followed by the RC-type (48 V/ns) and finally the R-type (26 V/ns). The gate drive resistor value, which is critical for turn-on slew rate, is fixed at 51 Ω for all 3 setups. Firstly, the reason is that for R-type gate drive, this resistor choice is set to ensure that the DC gate current is below the critical limit to prevent damage to the gate. Secondly, 51 Ω was selected to set the slew rate for the RC-gate drive method to approximately 50 V/ns. Finally, 51 Ω was selected for the GaN GIT driver to make a fair comparison with the other gate drive methods.

The RC-type and GaN GIT driver are clearly faster than R-type because they are driven at 12 V. GaN GIT driver is faster than the RC-type gate drive because of the discharging speed-up capacitor function and the choice of a smaller speed-up capacitor ($C1=120$ pF vs. $CB1=1.2$ nF). The reason for the larger capacitor for the RC-type gate drive is to increase the RC time constant to slow down the decay of the negative turn-off voltage.

The turn-off slew rate results is depicted in Figure 3-24b. From the graph, it is shown that slew rate for RC-type and R-type are close, while GaN GIT driver IC outperforms them to achieve a maximum slew rate of 110 V/ns. While both RC-type and GaN GIT driver IC discharges the gate with negative voltage, the RC-gate drive method has a larger discharge resistance resulting in a slower turn-off slew rate. The R-type gate drive has a low resistance to GND, but discharges to GND instead of a negative voltage. The GaN GIT driver IC capitalizes on low impedance from gate to VEE and a negative voltage to achieve twice the slew rate.

Figure 3-24 Slew rate measurement results for a) Low side turn-on, b) Low side turn-off

Figure 3-25 Slew rate measurement results for a) High side turn-on, b) High side turn-off

The high side slew rate is shown in Fig. 3-25. Results are very similar to the low side results in Fig.3-24, except that the high side results are slightly faster. This is because of the probe capacitance loading on the VGS and VDS pin during low side test which slow down the slew rate measurement results.

3.2.3.7 Cross conduction protection

The low side V_{GS} spike voltage occurs when high side is turned on is measured and plotted against the slew rates (according to Fig.3-25a) and shown in Fig.3-26. From the results, it shows that the GaN GIT gate driver has the lowest V_{GS} spike voltage, despite higher slew rate operation than the other 2 methods. All 3 methods managed to keep this spike voltage below the threshold voltage of the GaN GIT.

Figure 3-26 Cross conduction test

Chapter 4

Application in Transportation: Inductive Power Transfer for Electric Vehicles (EV)

4.1 Motivation and Literature review

Development of battery technology and advancement of power electronics has allowed EVs to gain popularity in the recent years, with strong boost for greener energy.

From an environmental conservation perspective, EVs demonstrate benefits above conventional Internal Combustion Engines (ICE) vehicles. EVs provides the energy efficient solution to conventional ICE, with energy efficiencies going as high as 62 % compared to 21 % for internal combustion vehicles. Pollution due to EVs is lesser than ICE [57]. Another push for in EVs is the performance benefits. Electric motors have smoother operations and quieter than ICE, while having stronger accelerations, and lesser maintenance [58].

However, there are some challenges facing EVs which are generally battery related issues. Due to limited charge holding capacity of Li-ion batteries, the driving range of EVs is limited compared to ICE vehicles, being able to only travel one-third or half the distance of an ICE vehicle [58]. In addition, the battery charging time is time consuming, with level 1 charging taking 4-8 hours and fast charge consuming 30 minutes compared to 5 minutes for an ICE vehicle [59]. Despite having higher charge carrying capacity compared to other battery materials, Li-ion batteries for EVs are still very big and bulky. They are expensive and may be required to be replaced one or more per car lifetime [59] [60].

Inductive Power Transfer (IPT) is the method of wirelessly transferring power. The system for static wireless charging is as shown in Fig.4-1 [16]. Power drawn from the AC grid is rectified into a DC voltage. Since the application draws more than 75 W, a Power Factor Correction (PFC) stage is necessary to improve the power factor. A high frequency inverter converts the DC voltage into AC

voltage so that it can be transmitted using the magnetic resonant wireless power transfer coil. On the secondary side, the output of the resonant tank is connected to a SiC diode rectifier which rectifies the AC signal into a DC voltage.

IPT for EVs provide a convenience and safety for the user as the user is not directly exposed to conducting parts of the plug-in charger [61] [62]. This system is weather proof and is not easily subjected to vandalism like a plug-in station [60].

Figure 4-1 Static wireless charging

University of Auckland has made notable progress in the development and modelling and design strategies for IPT systems [63] [64] [65] [66] and has developed systems for EV applications [67]. The team at Oak Ridge National Laboratory (ORNL) achieved an efficiency of 90 % at 7 kW [68] while researchers at University of Michigan-Dearborn achieved 95.7 % at 8 kW across 200 mm [69]. Commercialized wireless charging kits have been offered by Qualcomm Halo [70] and WiTricity (Fig.4-2) [59] [71]. Wireless EV charging standard such as SAE J2954 is currently in revision and will be released in 2016.

Currently, there are challenges facing wireless charging. Firstly, it suffers from low efficiency compared to plug-in chargers [60]. Secondly, a wireless charging system is vulnerable to issues of misalignment, which can affect the power transferred by the wireless charging system [60].

Figure 4-2 WiTricity commercialized charger [71]

The next development for IPT is the dynamic IPT, which is wireless power transfer on the go as shown in Fig.4-3. This research has the potential to resolve the battery related problems of EVs. By charging on the move, the vehicle is able to increase its vehicle travel range. In addition, this allows reduction in the size and weight of the batteries in the car by up to 20 % [59]. In addition, by charging and discharging the battery on the go, it is able to improve the battery life. The constraint of this method is the heavy infrastructure investment required.

Figure 4-3 Dynamic wireless charging [72]

Korea Advanced Institute of Science and Technology (KAIST) developed 3 generations of dynamic IPT for golf cart, bus and SUV, which has been running since 2009 [73]. They have been able to transfer 6 kW and 17 kW at 170 mm with greater than 70 % efficiency.

4.2 Concept of IPT

A comparison of conductive and wireless EV charging circuit blocks are shown in Fig.4-4 [74]. For conductive EV charging, an isolated DC/DC converter is used to create galvanic isolation between the charger and the vehicle. Since most of their circuit blocks are similar, IPT can be studied by modelling an isolated full bridge DC/DC converter, which is a common power electronics topology used for high power applications.

Figure 4-4 Conductive vs. Wireless structure for high power EV charging [74]

In the situation of the wireless EV charging, instead of a transformer, a pair of loosely coupled coils is adopted which has a much lower coupling factor, k , compared to a transformer. This reduction in magnetic coupling leads to larger magnetizing current which affects the power transfer and efficiency characteristics of the system [74]. It also creates a load dependency of the output voltage due to non-dissipative inner resistance [74].

In order to improve the power transfer characteristics, capacitors are connected in series with the primary and secondary coils to create a resonant tank such that at the resonant frequency, the reactive power due to the capacitor and inductor cancel themselves out. This reduces the reactive power ratings for the coil and power supply system [59].

4.2.1 Modelling IPT compensation circuit

There are 4 main basic topologies for compensation as shown in Fig.4-5 [75]. There is rich amount of literature studying the voltage, current and transfer characteristics of these circuits [59] [64] [75] [76]. For this work, the author will adopt the Series-Series compensation due to its simplicity.

Figure 4-5 Basic IPT compensation a) Series-Series b) Series-Parallel c) Parallel-Series d) Parallel-Parallel [75]

The IPT compensation circuit can be modelled like a transformer without a core as shown in Fig. 4-6a, which can be simplified to into Fig.4-6b for easy manipulation. By taking Kirchhoff's Voltage Law around the primary and secondary loops respectively, one is able to obtain equation 4.1 and 4.2, while equation 4.3 and 4.4 can be obtained by taking the primary (not including source impedance) and secondary impedance. With some manipulation, the reflected impedance, Z_{ab} , is shown in equation 4.5. These equations are crucial for the calculation of the power transfer and efficiency.

$$VIN = \left(Z_s + \frac{1}{j\omega C_1} + R_1 + j\omega L_1 \right) I_1 - j\omega M I_2 \quad (4.1)$$

$$0 = -j\omega M I_1 + (Z_{Load} + R_2 + \frac{1}{j\omega C_2} + j\omega L_2) I_2 \quad (4.2)$$

$$Z_{11} = \frac{1}{j\omega C_1} + R_1 + j\omega L_1 \quad (4.3)$$

$$Z_{22} = Z_{Load} + R_2 + \frac{1}{j\omega C_2} + j\omega L_2 \quad (4.4)$$

$$Z_{ab} = R_1 + j \left(\omega L_1 - \frac{1}{\omega C_1} \right) + \frac{\omega^2 M^2}{Z_{Load} + R_2 + j \left(\omega L_2 - \frac{1}{\omega C_2} \right)} = Z_{11} + \frac{\omega^2 M^2}{Z_{22}} \quad (4.5)$$

Figure 4-6 IPT modelling (a) full circuit (b) simplified circuit

The resonant frequency, f_0 , of the compensation network can be calculated from equation 4.6. At resonance, the reflected impedance is shown in equation 4.7 which can be noted that that the reactive components cancel each other out.

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}} \quad (4.6)$$

$$Z_{ab} = R_1 + \frac{\omega^2 M^2}{Z_{Load} + R_2} \quad (4.7)$$

4.2.2 Efficiency and power transfer

Using the equations found earlier, the power transfer capability of the compensation network is shown in (4.8). With reference to Fig. 4-6a, the output power can be calculated by multiplying the square of the secondary side current by the output impedance. Many work [77] [78] have provided the calculation for the secondary current with respect to the primary current for series-series compensation. The efficiency of the compensation can be found by dividing the output power from (4.8) by the input power. The input power can be found by multiplying the square of the primary side current by the sum of the source impedance and reflected load, making reference to Fig.4-6b, resulting in (4.9).

$$P_{out} = I_2^2 Z_{Load} = \left(\frac{\omega M I_1}{Z_{22}}\right)^2 Z_{Load} \quad (4.8)$$

$$Efficiency = \frac{P_{out}}{P_{in}} \times 100 = \frac{(\frac{\omega M I_1}{Z_{22}})^2 Z_{Load}}{I_1^2 (Z_s + Z_{ab})} \times 100 = \frac{(\frac{\omega M}{Z_{22}})^2 Z_{Load}}{(Z_s + Z_{ab})} \times 100 \quad (4.9)$$

4.2.3 Coil characteristics

Coil design considerations are to ensure good efficiency, high power transfer [77], while being light weight. The compensation adopts a series-series configuration where the capacitor and inductor on the primary and secondary sides are connected in series. Two sets of resonant coil and capacitors are designed for 2 different operating frequencies of 100 kHz and 250 kHz operation, and their specifications are shown in Table 4-1. Fig. 4-7 shows the experimental setup.

The values of the mutual inductance, M , is obtained through experimental data as shown in Fig. 4-8, based on the 250 kHz compensation network in Table 4-1.

Table 4-1 IPT coil and capacitor specifications

Specifications	100 kHz	250 kHz
Internal radius	75 mm	75 mm
External radius	150 mm	150 mm
Type of wire	210/33AWG	210/33AWG
Number of turns	28	21
Compensation type	Series-Series	Series-Series
Primary and secondary inductance	234 μ H	120 μ H
Primary and secondary capacitance	11 nF	3.29 nF

Figure 4-7 IPT coil setup

Figure 4-8 Experimental results of mutual inductance and coupling against distance for 250 kHz arrangement

4.2.4 Coil efficiency and power transfer simulation

The output power and efficiency equations (4.8) and (4.9), with M values from Fig. 4-8, are simulated in Matlab against frequency by varying distance and load as shown in Figure 4-9 and 4-10 respectively.

In the first simulation as shown in Fig. 4-9, the load is fixed and the distance is varied. Fig. 4-9a and Fig. 4-9b illustrates the output power and efficiency respectively. As the coils are brought closer, the coupling is stronger and mutual inductance to increases. The coil coupling goes from under-coupled to critically-coupled and finally over-coupled.

From Fig. 4-9a, frequency bifurcation phenomenon is observed and the maximum output power moves from the resonant frequency during critical and under-coupled to 2 peaks which are away from the resonant frequency. From Fig 4-9b, there are 3 observations to be drawn. Firstly, peak efficiency falls as the coils are separated further. Secondly, efficiency is peak at the resonant frequency for all types of coupling. Finally, it is observed that for over-coupling, 3 efficiency peaks are observed.

In Fig.4-10, the simulation is conducted by varying loads and fixing the coupling. Fig.4-10a shows the output power, while Fig.4-10b shows the efficiency. More loading increases the coupling as the shown in Fig.4-10a because the quality factor deteriorates. It is observed that as loading increases, the bifurcation phenomenon is observes and the maximum output power occurs at 2 frequencies away from the resonant frequency. Maximum efficiency occurs at the resonant frequency.

The frequency bifurcation phenomenon is explained in [79]. Using the transformer model described earlier in section 4.2.1 and obtaining (4.8), the maximum power can be found by equating the derivative with respect to frequency to zero. Solving the equation will provide three resonant frequencies (3 points of inflection), the native frequency, odd splitting frequency and even splitting frequency. The native frequency is inversely proportionate to the product of the inductance of the coil, making it independent of coupling conditions.

On the other hand, the odd splitting frequency and even splitting frequency is inversely proportionate to the sum of the coil inductance and mutual inductance between the coils. For under coupled conditions, the coupling factor is small, resulting in a small mutual inductance. Therefore, the odd and even splitting frequency is approximately at the native frequency. As coupling increases to an over-coupled condition, the mutual inductance increases and we start to observe the splitting of the peak power.

In the over-coupled condition, at the native resonant frequency, the inductive and capacitive components of the reflected load from the secondary side cancels itself out, resulting in zero reactive power and peak efficiency. The reflected load becomes more capacitive as frequency is decreased and more inductive when frequency is increased. The reactive power increases as frequency moves away from the resonant frequency and efficiency drops.

Real output power also increases quickly as the frequency moves away from the resonant frequency in the over-coupled condition. As the operating frequency approaches the odd and even splitting frequency, the increase in real output power is faster than the increase in reactive power in the compensation network, resulting in the increasing efficiency. However, as the operating frequency moves beyond the odd and even splitting frequency, output power drops and efficiency falls.

Figure 4-9 Simulation results of (a) Output power against frequency for varying distance (b) Efficiency against frequency with varying distance

Figure 4-10 Simulation results of (a) Output power against frequency for varying load (b) Efficiency against frequency with varying load

4.2.5 Coil efficiency and power transfer evaluation

Hardware testing conducted on the coils as shown in Fig.4-11b to verify the simulation results in Fig. 4-11a. The coils are tested at the coil gap of 180 mm at 250 kHz. In the both results, the bifurcation phenomenon is observed in the output power with variation with frequency implying over-coupled conditions.

The graphs of the simulation and evaluation are very similar with small variations.

Figure 4-11 (a) Simulation and (b) evaluation results of normalized output power and efficiency at 250 kHz compensation network

4.3 Switching loss evaluation and gate drive optimization

4.3.1 Power device selection

A common Figure of Merit (FOM) adopted by power semiconductor devices is $R_{on}Q_g$, the product of on-resistance and gate charge. This FOM accounts for the switching and conduction loss such that the lower the FOM, the better the performance. It is a representative of the technology [80]. A comparison of FOM among 3 state-of-the-art transistors using GaN, SiC and Si are compared and shown in Table 4-2.

Table 4-2 FOM comparison between Semiconductor devices

Material	GaN	Si	Si	SiC	SiC
Technology	Gate Injection Transistor	MOSFET	Super Junction MOSFET	MOSFET	MOSFET
Breakdown voltage (V)	600	600	700	650	1200
Rated current (A)	15	6	18	29	40
R_{on} (m Ω)	65	1000	125	120	80
Q_g (nC)	11	33	35	61	106
$R_{on}Q_g$ (n Ω C)	0.715	33	4.38	7.32	8.48

GaN GIT has the lowest FOM due to the high critical field of GaN and the High Electron Mobility Transistor (HEMT) structure. The Si vertical MOSFET performs the worst with the highest FOM. This is followed by SiC MOSFETs which perform an order of magnitude better. It is shown that Si Super Junction MOSFETs being able to outperform SiC MOSFETs for RonQg. This is because the Super Junction technology is able to push beyond the theoretical limits of Si. Current wide bandgap processes are still in its infancy while Si processes are matured. In years to come, one can expect the RonQg of SiC and GaN to further drop.

A comparison of the RonQg of the two SiC MOSFETs of different current and voltage ratings show that the RonQg is similar despite the difference in specifications, proving that RonQg is more technology dependent than specification dependent.

4.3.2 Half bridge circuit loss modelling

The losses in a half bridge circuit constitute conduction loss, switching loss, ringing loss and dead time loss as shown in equation (4.10), using a simplified model which studies the losses like buck type converter. The total conduction loss and switching loss can be shown (4.11) and (4.12), respectively. Reduction in conduction loss is limited by device parameters R_{on} and application requirement I_O . Reduction in switching loss can be achieved by increasing the slew rate to reduce rise and fall time of the GaN GIT.

The ringing loss is obtained from [81] and modified for GaN GIT as shown in (4.12), which does not have Q_{rr} but still has to discharge C_{DS} , which is small compared to Q_{oss} . The turn on ringing loss is affected by the Q_{oss} and turn off losses are affected by slew rates and parasitic source drain inductances that increase the peak voltage. The GaN device will have a voltage drop during dead time that results in dead time loss shown in (4.13). The absence of reverse recovery diode implies that dead time can be reduced, hence reducing dead time loss. Switching, ringing and dead time losses are proportional to frequency.

$$P_{HB\ loss} = P_{cond\ loss} + P_{sw\ loss} + P_{ringing} + P_{dead\ time} \quad (4.10)$$

$$P_{top\ \&\ bot, cond\ loss} = I_{DS}^2 R_{on, top} D + I_{DS}^2 R_{on, bot} (1 - D) \quad (4.11)$$

$$P_{sw,on \& off} = \frac{1}{2} f_{sw} \times V_{DS} \times I_{DS} (t_{r,top} + t_{f,top} + t_{r,bot} + t_{f,bot}) \quad (4.12)$$

$$P_{ringing} = f_{sw} (V_{in} (Q_{DS,top} + \frac{1}{2} Q_{oss,bot}) + \frac{1}{2} (Q_{Vpeak} (V_{peak} - 2V_{in}) + Q_{Vin} V_{in})) \quad (4.13)$$

$$P_{dead\ time} = V_{SD} \times I_{SD} \times t_{SD} \times f_{sw} \quad (4.14)$$

4.3.3 Experimental results and GaN GIT gate driver optimization

For this work, the RC gate drive circuit discussed in chapter 3 was adopted. The reason was that it allowed the GaN GIT to be driven at a higher voltage for higher slew rate operation. The negative voltage turn off allows fast turn off characteristics and cross conduction protection. In addition, it can be adopted with off-the-shelf gate driver ICs.

Double pulse switching characteristic test, using an inductive load circuit shown in Fig. 4-12, is conducted to evaluate the performance of the GaN GIT under EV wireless charging conditions. The GaN GIT device will be evaluated at drain-source voltage at 400 V due to application requirements. The GaN driver voltage is fixed to 12 V due to auxiliary power supply. This experiment will measure the value drain-source voltage/current overshoot, drain-source voltage rise/fall time and switching losses energy while varying load current from 2.5 A-15 A and resistor R1 from 5.1 Ω to 36 Ω . The switching characteristics waveforms are shown in Fig. 4-13 using R1=10 Ω gate resistor at target application voltage and current of 400 V and 10 A.

Figure 4-12 Experimental setup for inductive load circuit for 2 pulse test

Gate drive loop inductance should be small to improve the slew rate of the GaN device. One should consider reduction of the source and drain inductances along the power loop to reduce the V_{DS} ringing. A freewheeling diode with a low

reverse recovery charge improves the slew rate of the device. For realistic results, adopt a freewheeling diode which have a reverse recovery charge equivalent to the GaN GIT's reverse conduction Q_{DS} .

Fig. 4-14 shows the turn-off, turn on and total switching loss energy per cycle respectively. Switching loss energy is reduced as the resistor R1 is reduced because larger gate current reduces rising and fall time. Switching loss energy increases with current. These two observations are in agreement with (4.12).

Figure 4-13 Switching experimental results of 2-pulse test results (a) Turn-off transition for TO-220 GaN GIT (b) Turn-on transition for TO-220 GaN GIT

Figure 4-14 Evaluation results for switching energy per cycle (a) Turn-off switching energy (b) Turn-on switching energy (c) Total switching energy

Another factor for consideration should be the overshoot. Fig. 4-15a and 4-15b shows the turn-off voltage peak and turn-on current peak respectively of the

GaN GIT for varying current levels and varying resistor, R_1 . Overshoot increases as drain-source current increases and as R_1 decreases as higher slew rates cause larger overshoot. The overshoot test shows that the peak does not exceed the absolute value and hence the device is safe.

Figure 4-15 Evaluation results for overshoot (a) Drain source voltage peak vs. absolute rating (b) Drain source current peak vs. absolute rating

Finally, the slew rates of the GaN GIT are plotted in Fig. 4-16. Fig. 4-16a shows the slew rate for the turn off transition. As R_1 is reduced, slew rates increase and the device achieves a maximum slew rate of 67 V/ns. This work utilizes the GaN GIT with TO-220 package which results in low slew rates compared to PQFN packages.

Figure 4-16 Evaluation results for slew rate (a) VDS slew rate during turn-off transition (b) VDS slew rate during turn-on transition

The turn on transition slew rate is illustrated in Fig. 4-16b. Due to the parasitic drain and source inductance of the TO-220 package, a voltage drop is observed in the drain source voltage when drain source current flows through it, affecting the slew rate measurement of V_{DS} at low load (2.5 A and 5 A condition). It is

shown that low resistance results in higher slew rates and slew rates drop as current increases.

Based on the evaluation data, the choice of R_1 should ensure low total switching energy, peak drain-source voltage and current below the limit and having a slew rate less than 50 V/ns. Based on these requirements, 10 Ω was chosen.

4.4 Proposed: Efficiency Centric Mode of Operation

4.4.1 Control objective

For EV charging, the competing technology against IPT is the current norm which is wired plug-in charging, which has the clear advantage of high efficiency [82]. For wireless power transfer to become a feasible alternative, the control objective is to achieve high power transfer efficiency, while being able to deliver sufficient power.

As explained in the previous section, maximum efficiency and maximum power transfer is influenced by the coupling of the coils. In the case of critical or under-coupling, maximum efficiency and maximum power transfer occurs at the resonant frequency, For over-coupled coils, as in the case of this project, maximum efficiency occurs at the resonant frequency and the maximum power transfer occurs at two peaks which are away from the resonant frequency. Hence, it is crucial for the system to identify the coupling characteristics before starting.

4.4.2 Frequency sweep

The system begins an initialization by sweeping the switching frequency across a range of frequencies to understand the coupling characteristics. The diagram of the frequency sweep is shown in Fig. 4-17. With reference to Fig. 4-18 for the explanation of the frequency sweep, the system is first initialized at the starting frequency, freq_start , the state machine is set to 1 and the output power of the inverter is measured. Frequency is swept downwards towards the ending frequency, freq_end and the output power at the inverter is measured at each increment. The measured power is compared to the power measured at the previous increment. At a point of inflection, the state is increased and the frequency of the previous increment is recorded.

Figure 4-17 Frequency sweep diagram for (a) over-coupled condition (b) Under-coupled or critically coupled condition

When the sweep is complete, the system checks the state machine. If the state machine ends at state 4, the system is over-coupled, this means that the bifurcation process occurs as shown in Fig. 4-17a. There would be 3 recorded points of inflection. The first is Peak Power Frequency 1 (PPF1), the second would be the Resonant Frequency (RF) and the third will be Peak Power Frequency 2 (PPF2).

If it ends at state 2, it means that the coil is either critically coupled or under-coupled as shown in Fig. 4-17b. There would only be one point of inflection which is the Resonant Frequency, RF. If the state machine ends at anything

other than the previous 2 conditions, there is an error and the sweep is conducted again.

4.4.3 Sufficient power transfer

The process flow chart is shown in Fig. 4-18 illustrates the mode of operation for sufficient power transfer. Initial starting frequency is at the resonant frequency. The duty cycle of the inverter is increased if more power is needed to reach the target power and reduced if the output power is larger than the target power. There are two levels of tuning, coarse and fine. At a large difference, the systems utilize a coarse increment to improve the response. As error power gets closer, it utilizes the fine tuning to increase the accuracy.

For a critically-coupled or under-coupled system, operation is optimal at resonant frequency RF , where the maximum efficiency and power transfer occurs.

For an over-coupled system, maximum efficiency occurs at RF and Maximum Power Transfer occurs at PPF1 and PPF2. In order to deliver sufficient power at high efficiency, operating frequency will occur between the region of the resonant frequency and Peak Power Frequency 1 as shown in fig. 4-17a. If the inverter is functioning at maximum duty and the power is not sufficient (output power is less than required power), frequency is increased towards Peak Power Frequency 1 (PPF1) to increase output power. If the duty cycle is low, the system will check if it is operating at resonant frequency, and tune itself towards the resonant frequency in order to improve efficiency. If the inverter is already functioning at PPF1, with maximum duty and still unable to deliver enough power, it maintains at that condition as it is at maximum power transfer condition.

The novelty of this operation mode is that the inverter scans the coil configuration at stationary position and operates based on the coupling condition. It adopts an intelligent approach by tuning the operating frequency to balance between output power and efficiency.

Figure 4-18 Process flow chart of frequency sweep

4.5 Measurement Results of IPT system

The experimental setup is as shown in Fig. 4-19. It consists of an inverter, which is connected to the magnetically coupled IPT system. On the secondary side of the coil, the output is rectified and the load is a resistor bank.

The system is evaluated across a distance from 80 mm to 150 mm. Due to the variation of mutual inductance as the distance between the coil varies, the resistor load is varied from 47 Ω at 80 mm to 11.5 Ω at 150 mm so as to ensure the inverter output current is below the current rating of the GaN GIT with consideration of a safety margin. The input to the inverter is supplied at 370 V DC.

Figure 4-19 Experiment setup

The system level efficiency result is shown in Fig. 4-20. At 80 mm, the system is tested to 2.1 kW and achieves a peak efficiency of 95.6 % efficiency at 1.5 kW. As the distance is increased, the peak efficiency of the system falls to 90.4 % at 150 mm with the main contributor of the efficiency variation is due to efficiency loss in the coil and secondary rectifier. The reason for testing until 150 mm at 1.5 kW is to operate the inverter below the current limit of the GaN GIT device.

Figure 4-20 Experimental results: Efficiency vs. distance

Fig. 4-21 and 4-22 shows the efficiency breakdowns of each power conversion stages at 150 mm and 80 mm respectively operating at 100 kHz. The efficiency of the high frequency power inverter remains relatively constant with varying distance, with the inverter operating at about 97-98 % efficiency.

Figure 4-21 Experimental results: Efficiency breakdown at 150 mm

Figure 4-22 Experimental results: Efficiency breakdown at 80 mm

Comparing Fig. 4-21 and 4-22, when the load value is changed from $47\ \Omega$ at 80 mm to $11.5\ \Omega$ at 150 mm as mentioned earlier, the secondary side voltage is decreased and current is increased. It is observed that the coil efficiency drops drastically. The reasons of the efficiency drop is due to weaker coupling as the distance increases and higher secondary current resulting in higher copper loss in the coil.

The rectifier block remains highly efficient at 80mm as the output voltage is very high ($> 300\text{ V}$) due to the larger load resistance, making the losses due to the forward voltage of the diode negligible. However, as the coil gap increases until 150 mm, the lower secondary voltage will make the diode forward voltage drop more significant.

Fig. 4-23 shows the waveforms of the inverter output current (CH1) and voltage (CH2) as well as the IPT output voltage (CH3) and current (CH4) at 80 mm distance. The top half shows the zoom out version of the signals at $20\ \mu\text{s/div}$, while the bottom half displays a close up on the signals at $2\ \mu\text{s/div}$. This setup adopts the 100 kHz compensation network. Using the mode of operation method discussed previously, the operating frequency is tuned towards the resonant frequency of 100 kHz to ensure maximum efficiency.

An efficiency comparison is conducted on the converter with varying frequencies of 100 kHz and 250 kHz at 80 mm coil gap. The system is made to transmit the same amount of target power wirelessly. The results are shown in Fig. 4-24. The efficiency of the converter falls by at 2-3 % as frequency increases from 100 kHz to 250 kHz, with efficiency of 95.13 % falling to 91.7 % at 2 kW.

The efficiency drop is caused by the switching loss due to higher frequency operation. For the inverter, switching losses dominate during low power condition and gradually conduction losses start to dominate as shown by the low efficiency at 250 kHz. The coil will experience higher AC resistance as the frequency is increased 2.5 times. The rectifier will suffer from higher reverse recovery losses with higher frequencies.

Figure 4-23 Experimental results of inverter and coil Channel 1: Inverter output current, Channel 2: Inverter output voltage, Channel 3: IPT output voltage, Channel 4: IPT output current

Figure 4-24 Experimental results: Efficiency vs. input power for varying frequencies

Fig. 4-25 illustrates the efficiency comparison between the GaN based and SiC based system. The SiC based system was made using the similar components as the GaN based system and switching characteristics is optimized to ensure fairness. The GaN based system performs at 1 % higher efficiency compared to the SiC based system. This advantage arises from the GaN inverter which outperforms the SiC inverter by 1 %. The advantage of the GaN based system

comes from the lower on-resistance and gate charge of the GaN GIT compared to the SiC MOSFET which gives it the advantage of lower conduction and switching losses.

Figure 4-25 Experimental results: Efficiency comparison between GaN and SiC

Table 4-3 shows a comparison table between this work and some recently published works. This work demonstrates higher or comparable system level efficiency compared to other works with low switching frequency or smaller coil gap to coil size ratio. A lower switching frequency will result in lower switching loss, but SAE J2954 proposes 85 kHz. This work was developed prior to this knowledge and it would serve as a good example to showcase possibilities of GaN devices to functions beyond this frequency range. A lower coil gap to coil size ratio will result in better coupling and higher efficiency. However, one needs to consider the practicality of a 500-700 mm coil on the car, which can be bulky. Therefore, the authors believe that keeping the coil at a reasonable size should be a design consideration.

Other works have been able to achieve higher output power because of the availability of higher current rating Si and SiC devices in the market. The author believes that as current ratings of GaN devices start to increase, we would start to see more works using GaN HEMTs for EV wireless power transfer. A higher current rating GaN HEMT will have lower R_{on} , which is advantageous for higher power levels where conduction losses dominate.

Table 4-3 Comparison table

	This work		[82]	[83]		[84]		[57]	
Input voltage, VIN (V)	370 V DC		-	-		150 V DC		AC 100 V 60 Hz	
Coil size	300 mm diameter (Circle)		-	500 mm x 500 mm (Square)		700 mm diameter (Circle)		170 mm diameter (Circle)	
Frequency	100 kHz, 250 kHz		23.5 kHz, 48 kHz, 81 kHz	-		42.5 kHz		20-30 kHz	
Coil gap	80 mm	150 mm	-	100 mm	160 mm	100 mm	150 mm	100 mm	150 mm
Output power	2.1 kW @ 100 kHz	1.5 kW @ 100 kHz	3.3 kW	3.0 kW		1.5 kW		670 W	500 W
System peak Efficiency	95.6 % @ 100 kHz 91.7 % @ 250 kHz	90.4 % @ 100 kHz	91.77 % @ 23 kHz 91.54 % @ 49 kHz 88.70 % @ 80.75 kHz	94 %	92 %	86 %	82 %	84 %	81 %

Chapter 5

Application in Data centers: Point-of-Load Converters

5.1 Data center power supply architectures

The proliferation of Internet of Things (IOT) and big data related technologies have driven the need for larger data centers to satisfy the need for computation capability. Data center power consumption in the US is approximately 91 billion kilowatt-hours in 2013 and is expected to increase to 140 billion kilowatt-hours in 2020 [10]; coupled with increasing environmental awareness, legislation and rising oil prices, creates a demand for highly efficient power electronics.

In power electronics, power density is used to measure the compactness of the converter. It is the output power per weight or volume, depending on the application. The packing density of transistors doubles every 15-24 months as predicted by Moore's Law. This reduction of feature size in semiconductor technology has driven the processor and memory technology in the area of performance and miniaturization. These high performance computational devices come with higher power consumption within the server rack. This creates pressure on server power supplies to become more compact to fit into the server rack. Thermal issues and size of passive components makes it challenging to increase power density using Si devices.

These demands drive the focus in power transistor research towards wide bandgap semiconductor materials such as Gallium Nitride (GaN) due to the constraints faced by conventional Silicon (Si) MOSFETs.

The conventional power supply architecture is shown in Fig. 5-1. Reliability is important for data centers as downtime can result in large cost to the companies, especially with increasing transactions conducted online through credit cards and brokerages. An Uninterruptible Power Supply (UPS) is required for protection from any disruption in the grid.

Figure 5-1 Typical data center architecture

The power is rectified and passes through a PFC stage, which is usually implemented using a boost converter, to ensure unity power factor. This is followed by an isolated DC-DC converter which isolates the grid side ground and the load side ground to prevent issues like ground bounce and electrical safety. Finally, the power is stepped down to different voltages using Point of Load (POL) converters. The focus of this work is on the POL converters as it contributes the largest losses [85].

5.1.1 Two stage POL conversion

The conventional approach for implementation of POL converters is the two stages or intermediate bus architecture as shown in Fig. 5-2. The first stage steps the voltage from 48 V down to 12 V, followed by a second stage which steps it down to lower voltages of 12 V, 5 V, 3.3 V, 1.8 V and 1 V based on the different loads it is supplying. It is typical to implement the first stage of the converter as an isolated DC-DC converter as shown in Fig. 5-2a. The separated triangles symbol is used to indicate isolated converters, while the contacted triangles symbol is meant for non-isolated converters.

Figure 5-2 Intermediate Bus Architecture (a) isolated DC-DC in series with non-isolated DC-DC (b) 2 non-isolated DC-DC in series

The rationale for having 2 stages of stepping down is because of the limitations of silicon power transistors. In a non-isolated implementation of a step down converters, a buck converter can be used and will be the considered topology for this work. For large step down applications (48 V to 1 V), the duty cycle is 2.1 %. A rule of thumb is that the ON duty time should be 20 times the sum of the rise time and fall time of the converter. The typical rise and fall time Si

power transistor is in the region of 10 ns, resulting in a sum to be 20 ns. This places the converter on duty time at 400 ns and a maximum period of 20 μ s (Frequency of 50 kHz). The lower frequency will result in larger passive components like inductor and capacitors which will compromise the power density. In addition, a large ON duty cycle will result in a large conduction loss for the power device in synchronous rectification, resulting in lesser efficiency.

By implementing 2 stages of stepping down, we can optimize the second stage to adopt a lower voltage device, which have smaller on-resistance and gate charge due to the smaller die size.

Implementation of the first stage can be done with isolated and non-isolated converter topologies. Isolated topologies provide ground isolation from ground bouncing and decouple the noise associated with the ground. In addition, isolated topologies usually rely on transformers to step down the voltage, which reduces the impact on the minimum duty cycle, hence allowing higher frequency operation.

5.1.2 Single stage POL conversion

The adoption of GaN for POL application seeks to address the issues related to operating frequency, power density and slew rates from the previous section. For the same specification, the smaller size GaN die will reduce the gate charge and on-resistance. The smaller gate charge will increase the slew rate, allowing higher operating frequencies to allow smaller passive components for better power density. The lower on-resistance reduces the conduction losses associated with the buck converter for large stepdown applications. Implementation of the single stage POL is shown in Fig. 5-3, where it can be implemented with isolated DC-DC as shown in [86] or non-isolated DC-DC as shown in [87].

Figure 5-3 Single stage POL a) isolated b) non-isolated

The advantages of a single stage 48 V to 1 V POL converter are discussed in [88]. A single stage POL will firstly be more efficient as it reduces the losses associated with multiple stage conversion, since the losses in each stage in series add up. In addition, since the input current for the 48 V bus would be a quarter of the 12 V bus for the same amount of power, this means that a single stage conversion reduces the conduction losses associated with distribution such as cables and bus bars.

With the improved efficiency, there will be lesser heat loss into the environment; hence thermal management can be simplified. This is critical for data center applications which rely on expensive and energy consuming cooling systems. Power density can be improved by miniaturization of heat sinks and lesser converter stages. This is to allow POL power supplies to keep up with the trend of semiconductor technology which has been shrinking due to Moore's law. With reduction of heat sink size, components and more affordable thermal management, a reduction in a solution cost will make mass adoption feasible.

In [89], 4 different architectures are compared. They are the:

2 stage architecture, with isolation

2 stage architecture, without isolation

1 stage architecture, with isolation

1 stage architecture, without isolation

Using the results from [89], a normalized radar graph in Fig. 5-4 is prepared to compare the 4 topologies. Isolated design provides isolation, which comes with a cost as the isolated designs are the most expensive and complex, using 10-12 layers of PCB. The 1 stage isolated design performs the best in efficiency at 89 %, however, performs poorly for power density and cost.

Figure 5-4 Normalized radar graph comparison of different POL architecture

From the radar graph, taking into consideration of cost, power density and efficiency, the non-isolated designs are most attractive. While they do not provide isolation, this should not be a problem since isolation has already been provided in the previous stage as shown in Fig. 5-1. In this work, the non-isolated converter step-down will be investigated, with a focus on the buck converter. An efficiency model will be developed and studied to understand the loss components in order to decide whether to use a single or multiple stage architecture.

5.2 Efficiency study of 48 V to 1 V buck converter

5.2.1 Motivation

While it is understood that adoption of GaN power devices will push the pareto optimality point of POL converters, there hasn't been many literature to study the improvement in the efficiency boundary. This work aims to identify the bottleneck by studying the loss components existing at various operating points of frequency and load currents. With this information, the engineer can choose a device with the appropriate specification.

In [90], the author developed an efficiency modelling simulator on Matlab to study the efficiency of the E-mode GaN devices in POL converters, with a focus on synchronous buck converters for large step down. The author identified the operating loss components for the buck converter and developed the simulation model for synchronous conduction mode (SCM) and Diode Emulation Mode (DEM). In order to further improve the accuracy of the model, the author

modelled the impact of source inductance, piece-wise linear reverse conduction voltage, AC resistance of inductor winding and equivalent series resistance of passive components. The author verified the efficiency model with evaluation results to show the validity of the model.

This work will adopt the model from [90] to study the feasibility of GaN compared to Si and whether a 48 V to 1 V topology is feasible.

5.2.2 Introduction for synchronous buck converter

The circuit for the synchronous buck converter is shown in Fig. 5-5. Compared to the conventional buck converter, the low side diode is replaced with a low side power device labelled Q2. The reason for switching the diode for a transistor is to reduce the voltage drop across the low side power device to reduce conduction loss. This is particularly important for buck converters in large step down applications as the low side duty will be large, resulting in conduction losses to dominate. This comes at additional complexity in terms of controlling the low side power device and components like low side driver and isolator.

Figure 5-5 Schematic for synchronous buck converter

5.2.2.1 Operation and loss components in SCM

The switching diagram and the associated loss components of the synchronous buck converter are shown in Fig. 5-6. The low side switch is operated in complementary to the high side switch with a dead time between their ON times. This complementary switching strategy is typically known as Synchronous Conduction Mode (SCM). Unlike the conventional buck converter which enters

Discontinuous Conduction Mode (DCM) when inductor current turns negative, in SCM, the low side switch allows the current to flow through the drain-source terminals of the transistor.

Table 5-1 illustrates the equations for respective loss components associated to the synchronous buck converter. The main loss components for the synchronous buck converter come from 3 components, which are the inductor, high side and low side GaN power devices.

For the high side and low side power devices, there are dynamic and static losses. Dynamic losses are related to the switching frequency like switching losses, dead time loss, gate drive loss and output capacitance loss. On the other hand, static losses are loss components not related to the switching frequencies of the converter, like conduction loss. Existing literature [9], [91] explains the losses and the equations of the high side and low side power devices. The third row of Fig. 5-6 shows the various loss components in the synchronous buck converter and when they occur during the switching cycle. The numbers below the loss components directly relates to the various loss components in Table 5-1.

The 3 types of losses associated to inductor losses [92] are DC wiring loss, AC wiring loss and core loss.

The DC wire loss is directly proportional to inductor current and is the resistance of the wire for a DC load current.

As the switching frequency of the converter increases, skin effect kicks in and the conduction area across the conducting wire decreases, this is reflected in the AC wire loss which uses a resistance value which has a relation to frequency. AC wire loss is directly proportional to the inductor ripple current.

The final loss component for the inductor is the core loss, which results from hysteresis, eddy currents and residual losses of the core material. It is usually determined by Steinmetz equations, although recent literature have suggested new models to improve the accuracy of the calculation [93] [94].

Figure 5-6 Switching timing diagram for SCM and loss components of synchronous buck converter [90]

Table 5-1 Equations for the loss components in synchronous buck converter in SCM [90]

Loss component	Loss item	Equation	Remarks
Control (High side)	Gate drive loss	$P_G = Q_G \times V_{DR} \times f_{sw} + I_{GS,leak} \times V_{DR} \times D$	(5.1)
	Turn-on switching loss	$P_{on} = \frac{V_{Bus} \times I_{Lmin} \times f_{sw}}{2} \left[\frac{Q_{GD} \times R_{Gon}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}(R_{Gon} + R_{CSl})}{V_{DR} - \left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.2) [1] in Fig. 5-6
	Turn-off switching loss	$P_{off} = \frac{V_{Bus} \times I_{Lmax} \times f_{sw}}{2} \cdot \left[\frac{Q_{GD} \times R_{Goff}}{V_{pl}} + \frac{Q_{GS2} \times (R_{Goff} + R_{CSl})}{\left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.3) [2] in Fig. 5-6
	Output capacitance loss	$P_{OSS} = f_{sw} \times E_{OSS} = C_{o,er} \times V_{BUS}^2 \times f_{sw}$	(5.4) [3] in Fig. 5-6
	Conduction loss	$P_{conduction} = \left(I_{Load}^2 + \frac{I_{Ripple}^2}{12} \right) \times R_{DS(on)} \times D$	(5.5) [4] in Fig. 5-6
Sync (Low side)	Gate drive loss	$P_G = Q_G \times V_{DR} \times f_{sw} + I_{GS,leak} \times V_{DR} \times (1-D)$	(5.6)
	Turn-on dead time loss	$P_{SD} = V_{SD} \times I_{Lmax} \times t_{SD} \times f_{sw}$	(5.7)

			[9] in Fig. 5-6
	Turn-off dead time loss	$P_{SD} = V_{SD} \times I_{Lmin} \times t_{SD} \times f_{sw}$	(5.8) [8] in Fig. 5-6
	Turn-on switching loss	$P_{on} = \frac{V_{Bus} \times I_{Lmax} \times f_{sw}}{2} \cdot \left[\frac{Q_{GD} \times R_{Gon}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}(R_{Gon} + R_{CSl})}{V_{DR} - \left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.9) [6] in Fig. 5-6
	Turn-off switching loss	$P_{off} = \frac{V_{Bus} \times I_{Lmin} \times f_{sw}}{2} \cdot \left[\frac{Q_{GD} \times R_{Goff}}{V_{pl}} + \frac{Q_{GS2}(R_{Goff} + R_{CSl})}{\left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.10) [5] in Fig. 5-6
	Conduction loss	$P_{conduction} = \left(I_{Load}^2 + \frac{I_{Ripple}^2}{12} \right) \times R_{DS(on)} \times D_{sync}$	(5.11) [7] in Fig. 5-6
Inductor	Resistance loss	$P_{DC\ resistance} = I_{Load}^2 \times DCR \quad (5.12)$ $P_{AC\ resistance} = \frac{I_{Ripple}^2}{12} \times ACR \quad (5.13)$	If $\delta \ll 2r$, $ACR = \frac{1}{2r} \sqrt{\frac{f\mu}{\pi\sigma}}$
	Core loss	$P_{core} = K_1 \times f^x \times (K_2 \times \Delta I)^y \quad (5.14)$	K_1, K_2, x and y are from the manufacturer

5.2.2.2 Operation and loss components in DEM

In SCM mode, the low side device allows current to flow from Drain to Source during OFF period, so the buck converter does not go into Discontinuous Current Mode (DCM). Since low side power device is turned on and current is allowed to flow, it incurs more conduction loss compared to DCM. In addition, the inductor current is allowed to flow, so the high side power device turns on with a load current, compared to Zero Current Switching (ZCS) which DCM experiences. This results in more losses during low load time.

In order to overcome this, engineers can design the converter to adopt a Diode Emulation Mode (DEM) during low load current. The switching strategy and the high side and low side loss components are shown in Fig. 5-7. The inductor current or the drain-source current of the low side device needs to be sensed. The low side device is turned on a short dead time after the high side device is turned off to prevent shoot-through. It is turned off when the inductor current or the drain-source current of the low side device passes the zero crossing. As the low side device is turned off when low side drain source current is zero, it experiences almost zero current turn off. Since the high side device is turned on when the load current is zero, it experiences soft switching in the form of ZCS.

This strategy is useful to reduce power losses to improve the efficiency at low load. The associated power loss components for the power device in DEM are shown in Table 5-2. Comparing the table from Table 5-1 and Table 5-2, it is observed that 3 loss components are removed and 1 loss component is reduced. With DEM, the high side turn-on switching loss and the low side turn-off switching and dead time loss is removed. The low side conduction loss is reduced as the device is turned on only for positive inductor current.

Once the load current is high enough, such that load current is larger than half of the inductor ripple current, the converter will behave similarly to the SCM and the loss components will be the same.

Figure 5-7 Switching timing diagram and loss components of diode emulation mode for a synchronous buck converter [90]

Table 5-2 Equations for the loss components in synchronous buck converter in DEM [90]

Loss component	Loss item	Equation	Remarks
Control (High side)	Gate drive loss	$P_G = Q_G \times V_{DR} \times f_{sw} + I_{GS,leak} \times V_{DR} \times D$	(5.15)
	Turn-off switching loss	$P_{off} = \frac{V_{Bus} \times I_{Lmax} \times f_{sw}}{2} \left[\frac{Q_{GD} \cdot R_{Goff}}{V_{pl}} + \frac{Q_{GS2} \cdot (R_{Goff} + R_{CSl})}{\left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.16) [1] in Fig. 5-7
	Output capacitance loss	$P_{OSS} = f_{sw} \times E_{OSS} = C_{o,er} \times V_{BUS}^2 \times f_{sw}$	(5.17) [2] in Fig. 5-7
	Conduction loss	$P_{conduction} = \left(I_{Load}^2 + \frac{I_{Ripple}^2}{12} \right) \times R_{DS(on)} \times D$	(5.18) [3] in Fig. 5-7
Sync (Low side)	Gate drive loss	$P_G = Q_G \times V_{DR} \times f_{sw} + I_{GS,leak} \times V_{DR} \times (1-D)$	(5.19)
	Turn-on dead time loss	$P_{SD} = V_{SD} \times I_{Lmax} \times t_{SD} \times f_{sw}$	(5.20) [4] in Fig. 5-7

	Turn-on switching loss	$P_{on} = \frac{V_{Bus} \times I_{Lmax} \times f_{sw}}{2} \times \left[\frac{Q_{GD} \cdot R_{Gon}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}(R_{Gon} + R_{CSl})}{V_{DR} - \left(\frac{V_{pl} + V_{th}}{2}\right)} \right]$	(5.21) [5] in Fig. 5-7
	Conduction loss	$P_{conduction} = \left(I_{Load}^2 + \frac{I_{Ripple}^2}{12} \right) \times R_{DS(on)} \times \frac{V_{in} - V_o}{V_o} \times D$	(5.22) [6] in Fig. 5-7
Inductor	Resistance loss	$P_{DC\ resistance} = I_{Load}^2 \times DCR \quad (5.23)$ $P_{AC\ resistance} = \frac{I_{Ripple}^2}{12} \times ACR \quad (5.24)$	If $\delta \ll 2r$, $ACR = \frac{1}{2r} \sqrt{\frac{f\mu}{\pi\sigma}}$
	Core loss	$P_{core} = K_1 \times f^x \times (K_2 \times \Delta I)^y \quad (5.25)$	K_1, K_2, x and y are from the manufacturer

5.2.3 Simulation results and analysis

The intention for this simulation is to study the various loss components for the 48 V to 1 V buck converter. It is important to understand which components are dominant at the various conditions to develop countermeasures. The power device to be used is the EPC2103, which is an 80 V, 28 A device in a half bridge configuration. Both high side and low side devices adopt the same specifications. The inductor of choice will be the SER2915L-153KL from Coilcraft which has a 15 μH inductance, 1.65 m Ω DC resistance and self-resonant frequency of 15 MHz, making it suitable for high current application.

The simulation will be conducted from 100 kHz to 1 MHz and from 0 A to 20 A to study the buck converter at various frequency and loads. It is important to understand the amount of efficiency achieved with at each frequency levels to decide what is the suitable trade-offs between efficiency and power density.

5.2.3.1 48V to 1V GaN based Buck converter

The 3-D graph of the efficiency varying the load and frequency is shown in Fig. 5-8. The efficiency decreases as frequency increases due to dynamic loss components.

Figure 5-8 3-D Efficiency simulation for 48V to 1V buck converter

This efficiency increases initially as load current increases but plateaus as it reaches the load. This is because certain loss components are dominant at low load but as output power increases, the loss components do not increase as fast as the output power. The peak efficiency at full load (20 A) is 87.5 % and it occurs at the lowest frequency of 100 kHz. At 1 MHz, the efficiency at full load falls to 70.0 %.

Fig. 5-9a shows the efficiency against the switching frequency focusing on 4 different load currents. An interesting point to note in this comparison is that variation of efficiency is lowest at high load. This is because at high load, conduction losses dominate and variation in frequency which is directly proportional to dynamic loss components has a smaller effect on the efficiency.

(a)

(b)

Figure 5-9 2-D efficiency variation with (a) frequency (b) load current

Fig. 5-9b illustrates the buck converter efficiency with load current variation, addressing at 5 different switching frequencies. It shows that at 400 kHz the buck converter is still able to achieve more than 80 % efficiency at full load.

In order to justify using a single stage 48 V to 1 V converter using E-mode GaN, the efficiency of the single stage buck should be at least equal to the double stage 48 V to 1 V converter. Referencing [87], the typical efficiency of the double stage power supply is in the region of 83 %. Using Fig 5-9, the switching frequency which corresponds to an efficiency of 83 % is around 290-300 kHz, which justifies the 300 kHz used in [87].

A further investigation into the breakdown of the various loss components is shown in Fig. 5-10. The losses come from mainly 3 components, namely the inductor, high side GaN and low side GaN.

Figure 5-10 Loss components in the buck converter (a) Inductor (b) High side GaN (c) Low side GaN device

From the figure, it is clear the low side GaN is the largest contributor of loss at the full load condition. The high side GaN power loss dominates at high

frequency and low load conditions. The usage of a larger inductor results in small ripple currents. This result in the losses in the inductor being affected by DC related losses like load current, rather than AC related losses like high frequency operation.

A closer analysis into the low side loss components is shown in Fig. 5-11.

Figure 5-11 Low side GaN loss components (a) Conduction loss (b) turn on switching loss (c) turn off switching loss (d) turn on dead time loss (e) turn off dead time loss (f) gate drive loss

The largest contributor of losses at low frequency (100 kHz) comes from the conduction loss at about 1.5 W. The reason for the large conduction losses is because of the long duty cycle of the low side GaN device. A countermeasure is to adopt a power device which has a smaller on-resistance to reduce the conduction loss. Referring back to Table 5-1, there are 2 components to the conduction loss which is the DC load current and the AC ripple current. Since the load current is a design requirement and cannot be reduced to reduce conduction loss, this work targets the ripple current to reduce the other component of the conduction loss. In this design, we designed the inductance to be large such that the ripple current is about 0.6 A at 100 kHz and 60 mA at 1 MHz.

The remaining components like switching loss and dead time loss are low at low frequencies but become severe at higher switching frequency ranges. The dead time loss is low at low frequencies but increases significantly as frequency increases. The dead time loss is related to the amount of dead time, load current and the switching frequency of the converter.

The loss components for the high side devices are shown in Fig. 5-12. For the high side device, losses are mainly dominated by the switching loss and the output capacitance loss. Since it is a hard switching topology, the switching loss for the high side device is a concern to be addressed. The GaN device is used because of its low gate charge to allow faster switching transients to reduce switching loss. The output capacitance loss is directly proportional to the switching frequency and is shared between the low side and high side devices. From Fig. 5-12, as long as the switching frequency is kept low, the losses in the high side device will be small compared to the low side device's conduction loss. From this analysis, the bottlenecks for the efficiency are the conduction loss for the low side device.

(a)

(b)

(c)

(d)

(e)

Figure 5-12 High side GaN loss components (a) Conduction loss (b) Output capacitance loss (c) turn on switching loss (d) turn off switching loss (g) gate drive loss

5.2.3.2 Efficiency results of SCM vs. DEM

From the simulation results, efficiency is poor at low load condition (0-10 % load). Therefore, DEM can be used to increase the efficiency by turning off the low side diode at the zero current crossing point to remove some loss

components. The DEM condition is simulated and compared it with the SCM model previously presented.

Fig. 5-13 shows the efficiency difference between using SCM and DEM in low load conditions. In this simulation, the inductance is fixed at $16\mu\text{H}$ and the ripple current is in the region of 0.6 A at 100 kHz . It shows that DEM improves the low load efficiency by 0.22% from 31.49% to 31.71% . This improvement is very small because the loss components excluded due to DEM is not the dominant loss components.

Figure 5-13 Efficiency improvement using DEM with $16\mu\text{H}$ inductor

Another observation is that efficiency improvement reduces as frequency increases in Fig. 5-14. This is because the inductor ripple current is smaller as switching frequency increases. This results in the converter being in DEM phase for a smaller region of load current.

The efficiency is simulated again using a smaller inductor, SER2915L-152KL, which has an inductance of $1.6\mu\text{H}$. Since the inductance is smaller, the ripple current is larger and hence affects a larger region of the low load current. Efficiency improvements see a peak at 0.46% for 250 kHz operating frequency.

The DEM switching strategy provides efficiency improvements of $0.2\text{--}0.4\%$, which is not very significant, in exchange for additional complexity in terms of zero crossing sensing. Therefore, it is important for the engineer to decide between the trade-offs.

Figure 5-14 Efficiency improvement using DEM with 1.6μH inductor

5.2.3.3 GaN vs. Si based buck converter

To push the pareto optimality boundary of power electronics, engineers have to adopt new technologies which outperform the convention. For POL converters, E-mode GaN is proposed to replace Si MOSFETs. In this simulation, a Si power MOSFET (IRLR2908PbF) of similar specifications (80 V, 30 A) is simulated to study the efficiency of the 48 V to 1 V buck converter.

From Fig.5-15a, which shows the converter efficiency using Si power MOSFET, the efficiency at peak load is 59 % at 100 kHz and falls to 38 % at 1 MHz. The low efficiency implies that Si power MOSFETs are unsuitable for large step down applications using the buck converter. Comparing the loss components from Fig. 5-15(b)-(d), losses come mainly from the power transistors. Analyzing the loss components from the high side and low side power MOSFET in Fig. 5-15(c) and (d) respectively, it is observed that the losses come largely from the low side device in the form of conduction loss.

Fig. 5-16 shows the efficiency behavior of the 48 V to 1 V buck converter using GaN and Si at (a) 100 kHz and (b) 250 kHz respectively. At 100 kHz, the Si based system performs at peak efficiency at 71.4 % at 6 A load, but it falls to 59 % at full load. However, adopting GaN as a power transistor improved the efficiency by almost 30 % to get 88 % efficiency. This is also demonstrated in the 250 kHz system.

(a)

(b)

(c)

(d)

Figure 5-15 3-D simulation for Si based 48V to 1V buck converter (a) Efficiency (b) Inductor loss (c) High side loss (d) Low side loss

The reason for the improvement in efficiency comes from the lower on-resistance of the GaN device, 3.8 mΩ vs. 28 mΩ, because of the high critical electric field. This drastically reduces the conduction loss incurred by the converter. The smaller gate charge and output capacitance also reduces the dynamic losses, which are more significant at the higher frequency ranges.

(a)

(b)

Figure 5-16 Efficiency comparison between GaN and Si (a) 100 kHz (b) 250 kHz

This exercise shows that GaN an enabling technology which allows a single stage large step down buck converter which previously not allowed by Si due to poor efficiencies.

5.2.3.4 Double stage buck converter

The architecture of the 48 V to 1 V buck converter is shown in the Fig 5-17. The first stage steps down the voltage from 48 V to 12 V, while the second stage further reduces it to 1 V. By having 2 stages, the engineer is able to choose components more suitable for that voltage range. For the 48 V to 12 V applications, EPC2103, which was the 80 V, 28 A device used in the earlier simulations was chosen. In the second stage, due to the lower input voltage, one can choose a lower voltage device, as it will have a lower gate charge and on-resistance. For this simulation, the EPC2023 and EPC2100 will be simulated separately to see the performance. The EPC2023 is a single device rated at 30 V, 60 A. The EPC2100 is a half bridge IC has of voltage rating of 30 V and current rating on the high side and low side device at 9.5 A and 38 A respectively.

The first stage buck converter is able to output 240 W since it was designed for 12 V and current capability of the components is greater than 20 A. This means the first stage is able to drive multiple second stages as shown in Fig.0-18.

Figure 5-17 Architecture of double stage 48V to 1V buck converter

Efficiency graphs for both stages are shown in Fig. 5-18. The efficiencies for the first stage with varying frequencies and load currents are shown in Fig 5-18a, for a buck converter to step down from 48 V to 12 V, the efficiency ranges from 98.45 % at 100 kHz to 96.2 % at 1 MHz. Taking a look at the efficiencies on the second stage, we compare the efficiency values of the 12 V to 1 V buck converter using EPC2023 and EPC2100. From Fig. 5-18(b) and (c), their efficiency values are very similar.

Figure 5-18 3-D efficiency curves for (a) First stage buck converter (b) Second stage buck converter using EPC2023 (c) Second stage buck converter using EPC2100

Fig. 5-19 shows the graph of the first and second stage efficiencies at various frequency points. Fig 5-19a shows the first stage buck converter efficiency. The waveforms show that variation in efficiency as frequencies change is small at high loads and deviation becomes visible at low loads.

Since the efficiency difference between using EPC2023 and EPC2100 are so close, only a few frequencies are observed at a fixed intervals away from each other in Fig 5-19b. It shows that EPC2023 performs better at low frequencies compared to EPC2100. This is because at low frequencies, the conduction loss dominates and since the EPC2023 has a low on-resistance, it is able to be more efficient. However, at switching frequencies increase, EPC2100 performs better as it is optimized such that the low side device has low on-resistance for small conduction loss and the high side device has small gate charge for low switching loss. In the graph, EPC2100 outperforms at higher frequencies. For this reason, we will be considering the EPC2100 to operate the second stage at high frequencies to improve the transient response.

Figure 5-19 Efficiency graphs with varying load current at various frequency for (a) first stage
(b) second stage buck converter

Making use of the previous information, the optimal frequency range of operating the double stage converter is investigated. The first stage will be considered for 100-250 kHz operation, while the second stage will be considered for 750 kHz to 1 MHz operation. Multiplying the efficiencies from Fig 5-19, we get the graphs in Fig. 5-20. From the graphs, it shows that the efficiency values are above 80 %. Efficiencies start to fall more significantly when the second stage operates at 1 MHz.

Figure 5-20 Double stage buck converter calculated efficiency a) Zoom out b) Zoom in

In order to select a ball park value for the operating frequency, one needs to consider the efficiency of a comparative method, which is the single stage buck converter, which in the previous section performs at 83 % efficiency. For this reason, this work believes that the double stage POL buck converter should operate at the 250 kHz region for the first stage and at the 750 kHz region at the second stage. Drawing a comparison between these results and the results of single stage 48 V to 1 V converter in the earlier section, the author believes that at the cost of power density, the double stage design allows better transient response and efficiency improvement.

5.2.3.5 Limitations and potential improvements

One of the limitations is thermal impact on the components. The model assumes typical temperatures. However, losses in the components are converted to heat which increases the on-resistance of the power device, increases the DC and AC resistances of the inductor windings and reduce the transconductance of the power device. This can be resolved by adding a thermal component to the calculation of the losses and having an additional function to calculate the temperature based on losses of the component. The efficiency model has to run in iteration such that it stops when the calculated temperature comes sufficiently close to the input temperature value.

Future work can consider on developing a model for the power density of POL converter. This purpose of developing a power density model is to couple the two models together to get the pareto optimality curves for POL buck converter design. This will allow the user to understand the trade-offs they have to make for their power density improvements. It is important to note that such a model will not be a continuous waveform but discrete points on the 3-D plane as component values are sold in discrete values. This would require the user to have a database of components which will vary as circuit values change.

5.3 GaN power device and Si circuit integration

After studying the efficiency behavior for the buck converter under large step down specifications, it is important to address another metrics for power converters, which is power density. Power density is a concern when space and weight is critical such as transportation applications like automotive and aerospace. In the situation of data centers, power density is also important because a reduction in power supply size is needed for the better more power hungry processors and a reduction in weight reduces weight stress on the server rack.

GaN power device enable higher frequency switching which allows for smaller passive components like inductors and capacitor. In addition to reducing the size of passive components, consideration should be made to reduce the size of half bridge stage of the buck converter. This will not only increase the power density,

it can also improve performance. However, thermal management has to be considered as heat issue can result in poorer efficiency and reliability.

5.3.1 Motivation for integration GaN and Si devices

Since the invention of the transistor in 1947, semiconductor technology has seen great leaps in its ability to pack more transistor within an area of Si through the invention of integrated circuits, as solutions moved from multiple discrete components to monolithic solutions. However, even monolithic solutions face its limitations as it only occupies 2 dimensions of area and thermal limitation for power solutions [95]. This prompted the development of multi-chip packages.

Multi-Chip Package (MCP) improves the electrical performance through the usage of shorter interconnects and allowing chip to be placed closer to each other [96] [97]. This improvement in signal propagation can allow engineers to push the operating frequency of GaN based power converters and reduce switching losses through faster voltage and current transitions.

By integrating various functions into a single package, major reductions in the overall size and weight can be achieved, which improves power density. A demonstration of improvement in power density is shown in [98]. By integrating the GaN device with the gate driver, the authors increased the power density by a factor of 3. The power density is further increased by a factor of 6.75 by also integrating the signal and power isolation, demonstrating a power density improvement of 20 times when comparing an implementation using discrete devices and multi-chip solution. In addition, it also increases the packaging efficiency, reduce cost and reduce reliability issues associated with multiple packages.

Due to process limitations, it is difficult to combine different technologies on a wafer. Multi-chip packaging methods allows heterogeneous integration of such technologies to capitalize on the advantages of each technology [99]. In the example of high voltage power devices, the size of a transistor using Si technologies will be either too big or too inefficient to be used. With multi-chip packaging, engineers can combine wide bandgap materials such as GaN and SiC with lower voltage CMOS technology to achieve good performance and form factor.

However, the benefits of MCP do not come without any cost. By integrating the multiple chips together, the complexity of the design increase [100], requiring longer design time and niche design tools. In addition, integrating the dices together will require more sophisticated technology and processes which increases the setup cost, making MCP ICs unfeasible for low quantity and price competitive designs [100]. The yield can be potentially lower when one of the multiple dice within the package becomes defective [101].

An integrated solution also limits the ability for the user to make customization, which was previously available to designers using discrete implementation. This is particularly important for high voltage and high power applications, where the slew rate of the power transistor is controlled to reduced EMI related issues.

While MCP resolves the thermal issues faced using monolithic ICs, there is a limitation to the heat the MCP can dissipate as the power device and controller are still located in the same package, limiting the output power of the solution [100]. Therefore, good thermal management design is required to protect the MCP from getting damaged.

5.3.2 State of the art

There are various different technologies to implement multi-chip integration, each with its own advantages and disadvantages, suited for different applications. The decision on which technology to adopt depends on thermal, cost and complexity.

A simple method of multi-chip packaging is to have multiple dice on a lead frame to be contained within a package [102]. This method is used in controller IC with integrated power FETs where the FETs were previously on the same die as the controller. By separating the FET and the controller, heat from the power transistor can be allowed to dissipate on the lead frame without affecting the controller. This allows higher current applications while using the same package size.

Multi-Chip Modules (MCM) further push the concept of lateral integration within a package by integrating passive components together with the integrated circuit dice [96] [103]. Typically used in high power application, these modules

simplify design for system level designers to utilize a plug and play method to developing their solution.

In order to reduce the volume to increase the packing density, another method is to use an interposer to interface chips together. This method allows top and bottom utilization on the interposer which improves packing density compared to lateral integration from MCM. This method is currently used for integration of processor chips to reduce the length of routing between the IOs [104] and in power applications to interface the power FET with other dice [105] [106].

Further increase in packing density can be achieved using 3-D packaging, which involves stacking of packages [107], dice [108] [109] and wafers [110]. The packing density increases drastically, allowing larger space savings and shorter routings. However, the performance advantage causes a complexity and price trade-off and thermal management becomes very important.

5.4 Proposed 3-D integration of GaN and Si

In this work, we propose to integrate the power device by using 3-D packaging in the form of stacked die as shown in Fig 5-21. This method utilize the flip chip technology to mount the lateral normally off GaN on the Si CMOS gate driver. The GaN device is the EPC2036, which is a 100 V, 1 A GaN device from EPC, while the gate driver is fabricated on 0.18 μm CMOS process from Global Foundries. The PCB is interfaced to the CMOS chip using wire bonding to the board.

Figure 5-21 Proposed 3-D integration of GaN power device and Si gate driver

By adopting the flip chip GaN device to integrate with the CMOS gate driver, gate drive loop is reduced due to shorter interconnects. Space consumption has been reduced by stacking devices vertically instead of placing them laterally in the PCB.

The gate drive circuit to test the E-mode GaN in 3-D integration is shown in figure 5-22. It is a simple gate drive circuit with dead time function to protect the shoot through in the output stage.

The dead time circuit uses a current starved inverter for its delay to reduce the size and process dependence of the delay block. Transistor MN3, MN4, MP3 and MP4 forms an inverter; the discharging current is limited by MN1 and MP1 while the charging current is limited by MN2 and MP2.

Figure 5-22 Gate drive circuit for testing GaN power device

5.4.1 Thermal modelling

Thermal management is important for power related applications as it not only influence the solution's size, it affects the efficiency, functionality and reliability. It is then important to study how well this technology can dissipate heat from the power FET mounted on the Si controller.

The resistance of the 3-D packaging of the GaN and Si dice in Fig 5-21 can be modelled as the diagram shown in Fig. 5-23. There are 2 paths of heat dissipation; the first is from the GaN die through its silicon substrate into the

environment, while the second path is through the Si controller into the PCB and into the ambient.

There are 2 heat source; the GaN power device and the Si CMOS driver. Running the simulation explained in section 5.2 for a 48 V to 1 V application, it is found that the power transistor loss ranges from 79.5 mW at 100 kHz to 223 mW at 1 MHz. On the other hand, the calculated loss for the Si CMOS circuit ranges from 0.84mW at 100 kHz up to 4mW at 1 MHz. Judging that losses due to Si CMOS is at least 1 order of magnitude lower than the GaN die, it is removed to simplify the calculation.

Figure 5-23 Thermal resistance model of 3-D integrated GaN power device and Si driver

The thermal resistance of each component along the heat path has to be calculated using thermal conductivity and the dimensions of these components. The thermal conductivity information can be found in Table 5-3 below. From the table, it can be deduced that the bottle neck could come from materials with poor thermal conductivity such as the dielectric interface and the FR4 material on the PCB, affect the thermal resistances.

Table 5-3 Material and thermal conductivity of 3-D packaging

Item	Material	Thermal conductivity
GaN die	GaN on Silicon	140
Solder bump	SnAg	78
Metal pad	Al	205
Dielectric	SiO2	1.1
CMOS chip	Si	147
Solder pad	SAC	60
PCB	Cu	380
PCB	FR4	0.3

The calculation results of the thermal calculation are shown in Table 5-4. Bottleneck for heat dissipation comes from heat sources using convection, rather than conduction. These are the components where heat is discharge from the surface by means of a motion of a fluid, such as the thermal resistance of the GaN die to ambient and from the PCB to ambient.

Two ways of improving heat transfer using convection is to increase the surface exposed to the fluid in motion and to increase the rate of the fluid in motion. This is shown in table 5-4, where the thermal resistance is lower when heat is dissipated from a larger area such as the PCB when compared to dissipating the heat off the power device. Applying force convection instead of natural improves the thermal management as thermal resistance is significantly lower for forced convection. The equivalent thermal resistance using natural convection is 684.550 K/W, while it is 90.181 K/W for forced convection. This shows the advantages of having forced convection to improve heat dissipation.

Table 5-4 Thermal resistance and junction temperature calculation

Item	Symbol	Thermal resistance	
		Natural convection	Forced convection
Junction through GaN die (K/W)	Rth,j-GoS	5.162	5.162
GaN die to ambient (K/W)	Rth,GoS-a	69444.444	4884.005
Junction to solder bump (K/W)	Rth,j-B	40.830	40.830
Solder bump to metal pad (K/W)	Rth,B-p	0.017	0.017
Metal pad to dielectric (K/W)	Rth,p-D	0.109	0.109
Dielectric to CMOS chip (K/W)	Rth,D-CC	0.041	0.041
CMOS chip to solder pad (K/W)	Rth,CC-sd	0.017	0.017
Solder pad to PCB (K/W)	Rth,sd-PCB	10.965	10.965
PCB to ambient (K/W)	Rth,PCB-a	639.386	39.898

Equivalent thermal resistance (K/W)	$R_{th, equivalent}$	684.550	90.181
Power dissipated (W)		0.182	1.380
Ambient temperature (°C)		25.000	25.000
Junction temperature (°C)		149.588	149.450

It is critical to keep the die temperature below the recommended temperature on the manufacturer. In the case for the EPC, it is recommended to keep the junction temperature below 150°C. Using the thermal resistance calculated and assuming that the ambient temperature is 25°C, the maximum power able to be dissipated in the GaN die using natural convection and forced convection is 0.182 W and 1.38 W respectively. This data can be used to decide the output power depending on the losses on power transistor losses.

5.4.2 Performance simulation

To test the performance difference of the stacked die against the conventional method of lateral arrangement on the PCB, we conduct a double pulse simulation to compare the difference in the slew rate performance. The EPC2036 device will be simulated for slew rates at 48 V and varying currents from 0.25 A to more than 1 A. This is to test the performance of the device at the conditions of the applications.

For the two different packaging methods, characterization of parasitic inductances and resistances need to be conducted. This can be achieved by studying the impedance associated to the parasitic impedance. For the off chip implementation, the LM5113 half bridge gate driver was connected in series to a 1 Ω gate resistor and to the GaN gate. This will result in a pull up resistance of 1.6 Ω and a pull down resistance of 3.1 Ω .

The parasitic inductance of the discrete solution is estimated at 2 nH based on the typical parasitic inductance of on a Power Dual Flat No leads (PDFN) package [111]. For the on-chip implementation, due to the shorter leads, the parasitic resistance is calculated to be 1 Ω . The parasitic inductance is estimated to be 0.1 nH based on the reported parasitic inductance of micro SMD package, which is without wire bonding [112] .

The slew rate results are shown in in Fig. 5-24. The turn on slew rate is shown in Fig. 5-24a, it show that the slew rate does not have any correlation with inductor current. The impact of the parasitic impedances can be severe as it shows that 3-D D packaging can improve the turn-on slew rate by almost 100 %. It is important to note that 40 V/ns is considered fast switching characteristics and die-on-die integration can drastically improve the switching performance.

Fig. 5-24b shows the turn-off slew rate, which demonstrates an upward trend as the inductor current increases. It also shows that both waveforms are close, implying that effects of parasitic inductances have little influence on the slew rates until higher inductor currents ($I_L > 0.8$ A). It is important to note that the turn-off slew rate is much slower compared to turn-on slew rate, making it less sensitive to parasitic components.

Figure 5-24 Simulated slew rate results comparing stacked and lateral placement for a)turn-on and b)turn-off

Chapter 6

Conclusion and Future Recommendations

6.1 Conclusion

In order to resolve the challenge of the non-insulated gate of the GaN GIT, a 2-phase 2-stage gate driver is proposed. Simulations verified that the proposed 2-phase 2-stage driver reduces the gate ringing with minimum compromise on the slew rate. The proposed method requires lesser off chip components and can be developed at the integrated circuit level allowing for compact design and potential for multi-chip integration.

This is followed by work which investigates 3 different gate driving strategies of driving GaN GIT. A GaN GIT dedicated gate driver proposed in this work achieves high slew rate, while still providing protection against cross conduction. Experimental results shows that the proposed GaN GIT gate driver has performance benefits in terms of high slew rates (> 100 V/ns) and protection against the effects of cross conduction.

For the power electronics area, a highly efficient wireless power transfer system for EV charging application is demonstrated capable of transmitting 2 kW of power across 80 mm at 95 % efficiency was developed. Application of GaN HFET is adopted to improve the efficiency of the inverter and a novel guideline is adopted to optimize the gate drive circuit for the GaN HFET. A control algorithm is developed to make it function at the optimal frequency to provide maximum efficiency for the required output power. Experimental results prove the efficiency advantage of adopting GaN HFET in high frequency applications. In comparison against the SiC power transistor based system, GaN HFET based system displays power loss reduction of 20 W.

The second target application for enhancement mode GaN is in the area of POL power supplies for data center application, which it address two important metrics, efficiency and power density.

The efficiency study across a range of frequencies shows that efficiency at 20A output current ranged from 88 % at 100 kHz to 74.15 % at 1 MHz, which is good results for such high frequency, high current application. A comparison between GaN and Si MOSFET shows that GaN outperforms Si by more than 20 % for a 48 V to 1 V POL converter, highlighting how GaN is an enabling technology for POL converters. The efficiency study of a two stage buck converter demonstrates higher transient response using higher switching frequencies while having efficiency improvements by optimizing the power devices.

Finally, in order to reduce power density and improve transient performance, various device integration and packaging methods were studied. This work adopted the die-on-die 3D integration. Thermal study show that forced convection is critical for this form of integration to allow the GaN sustain more power losses. Simulations demonstrate that integration allows the GaN device to double its turn on slew rate from 45 V/ns to 90 V/ns.

6.2 Recommendations

6.2.1 Integrated solution

In the previous chapter, the efficiency study demonstrated the feasibility of developing a large step down converter using GaN. In addition, the stacked die gate driver illustrated the performance and size benefits of integration. Further development of this work can be geared towards a complete integration as shown in Fig. 7-1 below. The goal is to integrate components together within a single package or module to improve power density, while using efficiency brought about by GaN power device to reduce thermal related problems.

Figure 6-1 Integrated controller, isolation, driver and power FET

This integrated solution consists of the gate driver, power FET, isolation and controller. This will require a high voltage process (>50 V), since the input voltage is 48 V. Layout considerations for high voltage applications are important to prevent the chip from breaking down at high voltages.

6.2.2 Power and signal isolation

Power isolation is needed to supply power to the high side driver which has its ground floating with the output pin of the half bridge circuit [113]. This can be implemented using methods such as bootstrap, isolated power supply and inductive isolation.

The most common way to implement power isolation is the bootstrap circuit due to its simplicity and low cost [113]. The bootstrap circuit starts to charge the bootstrap capacitor when the switching node gets pull below the gate driver supply voltage, when the low side conducts. The drawback to this method is that there is a minimum time that the low side should conduct to ensure the capacitor is sufficiently charged up, hence limiting the high side on time and the switching frequency of the converter.

There are existing low voltage isolated power supplies on the market which have isolation up to 1 kV from manufacturers such as Texas Instruments [114] and Murata [115]. The advantage of this method is that the converter's on period is not limited and it is a plug and play solution. The disadvantage is that it is expensive and consumes a large amount of solution area.

Transformers are a good means of power isolation as it is common in the power application. Implementation can be in the form of discrete implementation [113] or integrated coils [116] [117].

In most power electronics applications, signal isolation is require to separate the power ground and the signal ground between the signal input (from the microcontroller or FPGA) to the driver input. The reason for the signal isolation is to transmit a signal to an output stage whose ground is not referenced to the signal ground. An example will be the high side driver in the half bridge circuit.

This is because the power ground usually tend to be noisier compared to signal ground due to the larger current that is conducts and the isolation keeps the

signal ground clean. Another reason is to reduce reduce parasitic loop inductance as discussed.

The level shifter block is commonly used in Integrated Circuit Design to step up or step down voltages especially logic signals. This circuit block uses high voltage process to interfaces 2 low voltage process blocks which are meant to have a different ground or voltage rails. This method is commonly used in older version of half bridge driver ICs like the IR2110.

The optocoupler consist of an input Light Emitting Diode (LED) as a transmitter and an output Photo Diode (PD) as a receiver. It is commonly used in the industry for high power applications due to the high breakdown voltage, high linearity, high bandwidth and low cost [118].

The drawbacks of the optocouplers are slow performance and large pulse width distortions induced [116]. Optocouplers also have lower Common Mode Transient Immunity (CMTI) of 10-25 V/ns compared with coil based isolation like icoupler from Analog devices which is in the region of 50-100 V/ns.

The using of coils to couple signals has the advantage of galvanic isolation, not subjected to negative transients and fast [116]. Implementation can be achieved using discrete isolated pulse transformers, but it can be bulky, expensive and not suitable for integration [116]. Integration of coils within the chip has been achieve by Analog Devices [116] [119] and Panasonic [117] [120], which reduces solution size.

6.2.3 Thermal management

Thermal related problems are the bottle neck to 3-D integration of ICs, especially for power related designs. Considerations need to be made on dissipating the heat from the GaN device, to prevent the GaN device from getting damaged and also to prevent abnormal behavior on the Si controller due to temperature variations.

In order to dissipate the heat effectively, a good thermal conductor needs to interfaces the heat source and transfer the heat to a large surface to be dissipated to the environment. For surface mounted devices on a PCB, thermal vias are used to dissipate heat from the top layer to the bottom layer of the PCB, where a

heat sink is connected. Similar studies can be conducted on the Si die to study the feasibility of vias from the top metal layer through the substrate for heat dissipation. An interposer can be sandwiched between the GaN and Si die as a means to dissipate the heat.

6.2.4 Controller IC

It is critical to study the various control methods and select a suitable control method best suited for large step down buck converter for data center requirements. After choosing a suitable control method, a controller IC should be designed for integration.

It is important to study and implement protection functions which are commonly found in POL converters like Under Voltage Lock Out (UVLO), Over Current Protection (OCP) and Over Voltage Protection (OVP).

Author's Publications

Journal

A. Q. Cai and L. Siek, "A 2-kW, 95% Efficiency Inductive Power Transfer System Using Gallium Nitride Gate Injection Transistors," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 458-468, March 2017.

Conference

A. Cai, A. Pereira, R. Tanzania, Y. K. Tan and L. Siek, "A high frequency, high efficiency GaN HFET based inductive power transfer system," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 3094-3100.

A. Cai, A. C. Herreria, S. B. How and L. Siek, "2-Phase 2-stage capacitor-less gate driver for Gallium Nitride Gate Injection Transistor for reduced gate ringing," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 129-134.

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Book Chapter

A. Q. Cai and L. Siek, "Inductive Power Transfer for Electric Vehicles Using Gallium Nitride Power Transistors," in *Disruptive Wide Bandgap Semiconductor, Related Technologies, and their application*, InTech, ISBN 978-953-51-6108, May 2018. (19 pages).

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