Design of constraint-aware readout circuits for bridge sensor applications

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**Design of Constraint-Aware Readout Circuits for Bridge Sensor
Applications**

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Abstract

The fast development of portable devices, autonomous robot and vehicles have led to growing demand in sensors. This in turn leads to a higher demand in performance-aware sensor electronics. Among various type of sensors, resistive based sensor is one of the popular choices due to its robustness against the environmental effects and flexibility for ease of interface with electronics. For portable devices, the sensor electronics will need to address power or energy-noise parameter while maintaining its dynamic range as high as possible. Thus, the thesis aims to explore different architectural solutions in the context of low energy-noise performance metric as the key design agenda. As such, various design approaches are realized. They are (i) current-to-frequency (IF) converter (ii) voltage-to-frequency (VF) converter and (iii) switched-capacitor (SC) interface.

The IF converter is based on a direct-sensing grounded integrator architecture. With only one operational amplifier (op-amp) clamping the voltage of sensing bridge output nodes, the change in bridge resistance is thus converted into signal current. This current is injected into an integrating capacitor. The ramping voltage of integrator is then converted into frequency through the associated comparator together with the digital logic. With the direct-sensing grounded integrator, the power consumption is reduced and the sensitivity to critical devices pair matching is also lowered. Fabricated using UMC 65nm process technology at 1.2V supply, the measurement results of the converter have achieved the average sensitivity of 41.5Hz/nA with an average output frequency range 2.488MHz. The average frequency uncertainty is 539Hz at the maximum output frequency at an average current consumption of 140 μ A.

With low power consumption and low noise features, the converter has obtained a SNR-energy figure-of-merit (FOM) of 0.71nJ. Thus, the converter has displayed the best figure-of-merit when compared to the recently-reported representative converters.

A VF converter is also proposed. In contrast to the current-to-frequency converter, the VF converter converts the floating output voltage of the Wheatstone Bridge. A simple hybrid transconductor is used to convert the voltage signal into a charging and discharging current. It is based on a combination of a level-shift flipped voltage follower and a folded shunt-feedback source follower. The charging current and the discharging current generated are used to charge and discharge an integrating capacitor. The ramping voltage signal on the integrating capacitor is then translated to frequency domain through a window comparator and digital logic. Implemented in 0.18 μ m CMOS technology at 1V supply, the simulation results have shown that the converter has a sensitivity of 1.936Hz/($\mu\Omega/\Omega$) and a center frequency of 78.2kHz. With this simple architecture, the converter has achieved a SNR-energy FOM of 0.0965nJ, which is at least comparable to the aforementioned IF converter. This demonstrates low noise-energy potential feature of the circuit architecture.

Turning to the resistive Wheatstone bridge that consumes potential high-power consumption, another approach is that of reduction of on-time in the sensing Wheatstone Bridge in conjunction with the proposed low-noise low-energy SC interface. This can be achieved through sampling the Wheatstone Bridge output signal at a short time interval and holding the signal for signal processing. This requires the design of op-amp to operate at high bandwidth

mode during the sampling phase and low-bandwidth low-power mode during the holding phase, thus reducing both of its current consumption and noise. To cater for the above mentioned two operation modes, an op-amp with adaptive bandwidth and adaptive biasing topology is proposed in this work. Implemented with UMC 65nm process technology at 1V supply from the on-chip low dropout regulator, the power of the SC interface together with the Wheatstone bridge, consumes only 6.15nJ per measurement interval. The measured signal-to-noise ratio of the SC interface attains 55.64 dB with a 40 Hz sinusoidal input signal. As a result, it can achieve a 0.19pJ SNR-energy FOM normalized with respect to bridge's resistance variation, which is at least three times better than that of the reported state-of-the-art works. Hence, the SC interface is very suitable for low-noise low-energy sensing system.

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Chapter 1

Introduction

1.1. Motivation

Sensors are becoming more and more popular today due to the development of portable devices, autonomous robot and vehicles. The most popular sensor types are resistive sensors and capacitive sensors. Although capacitive sensors are low power in nature, they are highly susceptible to parasitic capacitances. Resistive sensors are very popular due to its reliability and flexibility to interface with sensor electronic[1]. More importantly, resistive sensors are immune to EMI, hence they are very suitable for Internet-of-Things (IoT) applications.

As the output signals of the sensors are normally in the millivolt range, conversion of the sensor output signal to signal that possess high noise immunity is necessary for signal transmission circuits and systems. To achieve the goal, the sensor's output signal can be converted into either frequency- or time- domain signal prior to signal transmission. Subsequently, the frequency- or time- domain signal can be converted into digital domain through simple direct frequency counting. This conversion can be achieved with counters or microcontroller at ease. These types of sensor interface are often referred to as quasi-digital sensor interface. Examples for sensor interfaces with output signal in frequency and duty cycle form are [2]–[12].

The output signals of the sensor can also be converted directly into digital signal for signal transmission. An instrumentation amplifier is often required to amplify the sensor signal prior to digitize it for transmission.

Examples of this type of sensor interfaces are given in [13]–[18]. In Fig. 1.1, the conceptual diagrams for the two types of sensor interface are shown as follows:

Fig. 1.1 (a) Sensor interface with digital output (b) Sensor interface with output in frequency domain (quasi digital sensor interface)

The design challenges for electronic front-end interface design dedicated to resistive sensor in portable or IoT applications lies in the design of low energy consumption sensor system while maintaining good signal-to-noise ratio (SNR). To maintain good SNR, the front-end interface needs to possess low noise characteristic. For low energy consumption sensor system, the sensor energy consumption is often regarded as the main energy consumption contributor of the system due to the low resistance contributed by the resistive sensors. The commercially available resistive sensor often possesses a resistance of $10\text{k}\Omega$ or less. When configured in Wheatstone Bridge and excited by a 1V supply, the resistive sensor alone will consume at least $100\mu\text{W}$. For comparison of relative power consumption, it is interesting to observe that a low noise VF converter consumes only $80\mu\text{W}$ [11]. Based on the motivation,

this thesis aims to explore the method to reduce resistive-based sensor power consumption and the circuit techniques for the design of low-energy low-noise interface circuits.

1.2. Objectives

The objectives of this project are given as follows:

- (i) To explore different architectural solutions to convert resistive change in sensor to digital or quasi-digital signal for transmission while maintaining good energy-noise performance.
- (ii) To investigate, design, analyze and implement a low power and wide dynamic range current-to-frequency (IF) converter for resistive sensor applications.
- (iii) To investigate, design, analyze and implement a low power and low noise voltage-to-frequency (VF) converter for resistive sensor applications.
- (iv) To investigate, design, analyze and implement a robust low power switched-capacitor (SC) instrumentation amplifier for resistive sensor applications.
- (v) To test the proposed design's prototypes.

1.3. Organization of the Thesis

This thesis is organized in nine Chapters. Followed by the Introduction in Chapter 1, a literature review of the resistive sensors and various configurations of the resistive sensors in Wheatstone Bridge will be conducted in Chapter 2. In Chapter 3, a literature review of the quasi-digital sensor interface will be given. Chapter 4 demonstrates a proposed IF converter for

sensor interface together with its measurement results, and a VF converter together with its simulation results. In Chapter 5, the representative works on switched-capacitor instrumentation amplifier is reviewed. Chapter 6 presents the proposed switched-capacitor amplifier for sensor applications and its measurement results. In Chapter 7, the layout techniques for low noise sensor systems are presented. Finally, in Chapter 8, the conclusions and recommendations of future works are made.

Chapter 2

Review of Resistive Sensors

2.1. *Resistive Sensors*

Resistive sensors are widely utilized in various applications, including pressure sensing, stress sensing, strain sensing, flow rate sensing and temperature sensing. Section 2.1.1 describes the commonly used force sensor. Application method of force sensors such as pressure sensor is described in Section 2.1.2. Different variants of temperature sensor are also introduced in Section 2.1.3.

2.1.1. Force Transducers

Nowadays, human touch sensor becomes one of the key interaction sensors between human and machine to convey the force information. A resistive force sensor is usually needed to transform the physical force magnitude into the electrical signal. The commonly used resistive force sensors are:

- (i) Metal foil strain gauges
- (ii) Semiconductor sensors

2.1.1.1. Metal foil strain gauges

This type of strain gauge is conventionally made by a backing film with metal foil mounted on it. This backing film can be glue to any surface where strain needs to be measured. Fig. 2.1 shows a typical metal foil strain gauge.

Fig. 2.1 A typical metal foil strain gauge[19]–[21]

The gauge factor of the metal foil is given by

$$GF = \frac{\text{relative change in resistance}}{\text{applied strain}} = \frac{\Delta R / R_0}{\Delta L / L} = \frac{\Delta R / R_0}{\varepsilon} \quad (2.1)$$

where R_0 =idle resistance of the strain gauge and ΔR =change in resistance. $\Delta L/L=\varepsilon$ =applied strain. For a block that made of a resistive material, its resistance is given as

$$R = \frac{\rho l}{A} = \frac{\rho l}{wt} \quad (2.2)$$

where ρ =bulk resistivity of the material, l =length of the material, A is the cross-sectional area, w is the width of the material and t is the thickness of material.

Differentiating (2.2) gives

$$\frac{dR}{R} = \frac{d\rho}{\rho} + \frac{dl}{l} - \frac{dw}{w} - \frac{dt}{t} = \frac{d\rho}{\rho} + \varepsilon_l - \varepsilon_w - \varepsilon_t \quad (2.3)$$

where $\varepsilon_l=dl/l$, $\varepsilon_w=dw/w$. and $\varepsilon_t=dt/t$.

When a tensile strain is applied along the length, a compressive strain will result in the orthogonal direction. The ratio of the axial and transverse strain is defined as Poisson ratio, ν . This means that $\epsilon_w/\epsilon_l = \epsilon_t/\epsilon_l = -\nu$, thus we have

$$\frac{dR}{R} = \frac{d\rho}{\rho} + (1 + 2\nu)\epsilon_l \quad (2.4)$$

With (2.4), the gauge factor can be derived as

$$GF = \frac{dR/R}{\epsilon_l} = \frac{d\rho/\rho}{\epsilon_l} + (1 + 2\nu) \quad (2.5)$$

(2.5) shows that there are 2 main effects contributing to the gauge factor. The first term $((d\rho/\rho)/\epsilon_l)$ is the piezoresistive effect whereas the second term $(1+2\nu)$ is the geometric effect. For metal foil strain gauge, the geometric factor usually dominates.

2.1.1.2. Semiconductor sensors

Semiconductor sensors are sensors that utilize the piezoresistive effect of monocrystalline silicon to sense the change in mechanical strain. For this type of sensor, the piezoresistive effect dominates the gauge factor, as contrary to metal foil sensors. While a mechanical strain is applied onto a semiconductor sensor, its electrical resistance will differ. The change in resistive is mainly due to the mobility of holes (electrons) for p (n) type decreases (increases) when stress applied. Semiconductor sensors are gaining more popularity nowadays due to several advantages [1] that they offer as follows:

- (i) High gauge factor, typically 50 to 70 times of a conventional metal coil gauge.

- (ii) High reliability, as the fatigue life are greater than 10^8 at full reverse cycles at $1000\mu\text{m/m}$.
- (iii) Zero hysteresis.
- (iv) Small feature size, thus minimizing power dissipation and self-heating effect.
- (v) Wide strain gauge resistance ranges available.

Some examples of commercial semiconductor strain gauge are [22]–[25].

2.1.2. Pressure Sensors

Pressure sensors are vital in monitoring environment pressure, especially in the field of monitoring gas flow and leakage. Since pressure is defined as force per unit area, the force sensors can be configured as pressure sensors. The pressure sensors can be classified as

- (i) Bonded strain gauge pressure sensor
- (ii) Silicon piezoresistive pressure sensor.

2.1.2.1. Bonded Strain Gauge Pressure Sensor

The bonded strain gauge pressure sensor is fabricated by bonding a strain sensitive resistive element to a diaphragm. This type of pressure sensor can be used to measure very high pressure more than 100,000 psi [26]. However, at low pressure ranges, the strain gauge will start to interfere with diaphragm motion due to a thin diaphragm. Some example of the bonded strain gauge pressure sensor are [27]–[30]. Fig. 2.2 shows the top view and cross-section view of the strain gauge pressure sensor.

Fig. 2.2 Strain gauge pressure sensor's top view and bottom view.

In the bonded strain gauge pressure sensor shown in Fig. 2.2, four metal foils are bonded to a metal diaphragm, forming four variable resistors in the Wheatstone Bridge. The metal foil strain gauge in the above can also be replaced with semiconductor sensor elements. If the pressure at the top P_1 is equal to the pressure at the bottom P_2 , the diaphragm is un-deflected, thus its

output differential voltage is zero. When the air pressure P_1 is larger than the air pressure P_2 , the metal foil at the outer edge will experience compression while the inner metal foil will experience tension force. In this state, the Wheatstone Bridge becomes unbalanced, creating an output differential voltage.

2.1.2.2. Silicon Piezoresistive Pressure Sensor [31]

A silicon piezoresistive pressure sensor can be made by anisotropic etching. This anisotropic etching is often based on $\langle 100 \rangle$ plane with the edges in the $\langle 110 \rangle$ directions, thus forming a square diaphragm. The maximum stress that a square diaphragm experience is at the edge center of the diaphragm. Thus, in order to obtain maximum sensitivity, the sensor elements are placed at the edge center of the diaphragm as shown in Fig. 2.3.

Fig. 2.3 Wheatstone Bridge silicon piezoresistive pressure sensor

2.1.3. Temperature Sensors

Since overheating is one of the main failure mechanisms for machines and electronics, the conversion of temperature information into electrical

parameter becomes an important function in a system. Resistive temperature sensors, which are commonly used in the application, can be categorized into:

- (i) Thermistors
- (ii) Resistor thermometer detectors.

2.1.3.1. Thermistors

A thermistor is a nonlinear resistor with high temperature coefficient. The conventional thermistor used are the negative temperature coefficient (NTC) type of thermistor [32]–[35]. Although a thermistor with positive temperature coefficient (PTC) exists [36]–[38], the usage of it is limited. The thermistor is produced by using ceramic manufacturing technology which involves high pressure forming and high temperature sintering. For NTC thermistors, powdered oxides of Mn, Fe, Ni, Cu, Ti, Zn and Co are used. For PTC, the raw material is usually based on barium titanate. The resistance of a NTC thermistor can be approximated as

$$R_T = R_{T_r} e^{B \left[\frac{1}{T} - \frac{1}{T_r} \right]} \quad (2.6)$$

where T =thermistor temperature in Kelvin, R_T = thermistor resistance at temperature T , R_{T_r} = thermistor resistance at a reference temperature of T_r and B =constants depending on the thermistor's material. The temperature coefficient of the thermistors can be shown as follows:

$$\alpha_T = \frac{1}{R_T} \frac{dR_T}{dT} = -\frac{B}{T^2} \quad (2.7)$$

The coefficient B is ranging from 2580K to 4600K, depending on the material used. A normal thermistor will have a phase transition at 500 degrees

Celsius. As a result, it cannot be used above this temperature. Fig. 2.4 shows the characteristic of NTC thermistors having different temperature coefficients at different temperatures. A Platinum-100 resistance thermometer detector is also shown in this figure to serve as a reference.

Fig. 2.4 Thermistor's R_T/R_{TR} ratio against temperature [32]

2.1.3.2. Resistance thermometer detectors (RTDs)

Resistance thermometer detector [39]–[41] consists of a resistance conductor wound or deposited on an insulating support. The term nominal resistance (R_0) is used to indicate the resistance of the RTD at 0 degree Celsius. The commonly used industrial RTD sensors are usually of $R_0=100$ Ohm and 50 Ohm. Conventional RTD sensors are made by pure metals such as platinum, copper and nickel, stemming from the fact that these materials guarantee good

reproducibility and easy standardization. Fig. 2.5 shows the characteristic of platinum, copper and nickel at different temperatures.

Fig. 2.5 Resistance ratio at various temperatures for Pt, Ni and Cu [42].

2.2. *Wheatstone Bridge Configurations*

Wheatstone bridge was proposed by Charles Wheatstone to measure an unknown resistance. It is often used to measure a small change in resistance with high accuracy. The bridge is comprised of 4 resistors, with one, two or all resistors being the resistive sensors. Without any applied pressure, the bridge resistance is at its nominal value, represented by R_0 . With applied pressure, the resistive sensor will experience a change in its bridge resistance. This change in resistance is represented as ΔR throughout this thesis. The Wheatstone Bridge sensing configuration can consist of four resistive sensors (full bridge), two resistor sensors and two fixed resistors (half bridge), and one resistive sensor with three fixed resistors (quarter bridge). The excitation source to the Wheatstone Bridge can be either voltage source or current source while the output of the Wheatstone Bridge can be either voltage or current which is a function of the change in bridge resistance and the excitation source. Although

there are four possible combinations in the driving source and output mode, only three are usually seen in literature. They are given as

- (i) Voltage Mode Output Voltage Driven (VOVD) Wheatstone Bridge,
- (ii) Voltage Mode Output Current Driven (VOCD) Wheatstone Bridge, and
- (iii) Current Mode Output Voltage Driven (COVD) Wheatstone Bridge.

2.2.1. Voltage Mode Output Voltage Driven Wheatstone Bridge (VOVD) [43]

As depicted in Fig. 2.6, the Wheatstone Bridge is driven by a constant excitation voltage of V_{EX} . Therefore, a change in bridge resistance will be converted to a change in voltage, V_O .

Fig. 2.6 (a) Full bridge VOV, (b) half bridge same direction varying VOV, (c) half bridge opposite direction varying VOV, and (d) quarter bridge VOV sensors [43].

For a full bridge VOVD depicted in Fig. 2.6 (a), the output voltage can be shown as follows:

$$V_o = V_{EX} \left(\frac{\Delta R}{R_0} \right) \quad (2.8)$$

with ΔR = change in bridge resistance and R_0 =Bridge Resistance. For a half bridge same direction varying VOVD depicted in Fig. 2.6 (b), the output voltage is

$$V_o = V_{EX} \left(\frac{\Delta R}{2R_0} \right) \quad (2.9)$$

For the half bridge opposite direction varying VOVD Wheatstone Bridge configuration depicted in Fig. 2.6 (c), the output voltage is

$$V_o = V_{EX} \left(\frac{\Delta R}{2R_0 + \Delta R} \right) \quad (2.10)$$

For the quarter bridge VOVD in Fig. 2.6 (d), the output voltage is

$$V_o = \frac{V_{EX}}{2} \left(\frac{\Delta R}{2R_0 + \Delta R} \right) \quad (2.11)$$

From (2.10) and (2.11), one can see that the output voltages of these 2 configurations comprise a nonlinear term. This can be easily compensated by software in a digital system.

2.2.2. Voltage Mode Output Current Driven Wheatstone Bridge (VOCD)

The Wheatstone Bridge also can be driven by a constant current source, I_{EX} as depicted in Fig. 2.7.

Fig. 2.7 (a) Full bridge VOCD, (b) half bridge same direction varying VOCD, (c) half bridge opposite direction varying VOCD, and (d) quarter bridge VOCD sensors [8].

For full bridge VOCD in Fig. 2.7 (a), the output voltage is

$$V_o = \Delta R (I_{EX}) \quad (2.12)$$

For Fig. 2.7 (b) and (c), the output voltages are similar. They are obtained as

$$V_o = \frac{\Delta R}{2} (I_{EX}) \quad (2.13)$$

For a quarter bridge VOCD, the output voltage becomes

$$V_o = \frac{I_{EX} \Delta R}{R_0 + \frac{\Delta R}{4}} \left(\frac{R_0}{4} \right) \quad (2.14)$$

2.2.3. Current Mode Output Voltage Driven Wheatstone Bridge (COVD)

Instead of converting the change of bridge resistance into the change in output voltage, Wheatstone Bridge can convert the change in bridge resistance into change in output current. This usually requires an operational amplifier which is configured in unity-gain configuration to equalize the output nodes' potential of the Wheatstone Bridge. This output current can be directly injected into an integrating capacitor to convert it into frequency domain. Fig. 2.8 illustrates the current mode sensing Wheatstone Bridge with a constant excitation voltage.

Fig. 2.8 (a) Full bridge COVD, (b) half bridge same direction varying COVD, (c) half bridge opposite direction varying COVD, and (d) quarter bridge COVD sensors.

For Fig. 2.8 (a), the output current, I_{sig} is

$$I_{SIG} = \frac{2\Delta R}{R_0} \left(\frac{V_{EX}}{R_0} \right) \left(\frac{I}{I - \Delta R^2 / R_0^2} \right) \quad (2.15)$$

For Fig. 2.8 (b) and (c), I_{SIG} is obtained as

$$I_{SIG} = \frac{\Delta R}{R_0} \left(\frac{V_{EX}}{R_0} \right) \left(\frac{I}{I - \Delta R^2 / R_0^2} \right) \quad (2.16)$$

Similarly, for Fig. 2.8 (d), I_{SIG} is obtained as

$$I_{SIG} = \frac{\Delta R}{2R_0} \left(\frac{V_{EX}}{R_0} \right) \left(\frac{I}{I + \Delta R / R_0} \right) \quad (2.17)$$

From (2.15) and (2.16) one can see that the output signal will include a small nonlinear term of $1/(1-\Delta R^2/R_0^2)$. However, for a quarter bridge, the nonlinear effect is much larger, that is $1/(1+\Delta R/R_0)$. Nevertheless, this can be compensated by the digital system.

Chapter 3

Review of Quasi Digital Sensor Interfaces

3.1. *Introduction*

Quasi digital sensors interface are the sensor interfaces that convert the sensor signal from either voltage or current domain into frequency- and time-domain. They have received much attention due to their inherent simplicity and good noise immunity. Besides, quasi-digital sensors are also readily integrated with microcontroller having embedded timer or counter [44]. In this Chapter, the main focus will be given to quasi digital sensor interfaces having frequency output. To convert the sensor output voltage to frequency domain, the sensor output voltage will first be converted into current domain and injected into the integrating capacitor of a relaxation oscillator. This relaxation oscillator serves as a current-to-frequency (IF) converter that translates the current signal into frequency domain. For sensor configuration with its output in current domain, the output current can be directly injected into the integrating capacitor of the relaxation oscillator. Fig. 3.1 shows the block diagram of the conventional VF and IF converter.

Fig. 3.1 (a) Block diagram of a VF converter, and (b) block diagram of an IF converter

3.2. *McDonagh's Resistance-to-Frequency Converter [45]*

In the resistance-to-frequency converter proposed by McDonagh, a voltage-to-current converter is firstly used to convert signal voltage into signal current. Following this, a current-to-frequency converter will convert this signal current into frequency. The main objective of this design is to achieve a low temperature coefficient of frequency and able to operate under low voltage headroom. Fig. 3.2 shows the transconductance amplifier (Q_1 - Q_{11} , R_1 and R_2) used to convert the output voltage of the sensor into current domain. The selectable temperature coefficient voltage reference consists of Q_{12} - Q_{20} and R_3 - R_9 . For this circuit, R_g is the resistive sensor. The input pair transistors Q_1 and Q_2 are used to convert input voltage into current linearly over $\pm 30\text{mV}$. This current is then copied through the Wilson current mirrors that consist of Q_4/Q_6 and Q_3/Q_5 . The transistor group $Q_7/Q_8/Q_9$ functions as a subtractor in the process of generating I_o . In this design, the g_m of the input differential pair transistors is compensated by the positive temperature coefficient of Q_{10} , Q_{11}

and R_2 . For the Brokaw voltage reference, Q_{17} is designed to have an emitter area four times larger than Q_{18} to generate a ΔV_{BE} of

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{4I_{C18}}{I_{C17}} \right) \quad (3.1)$$

across R_6 . Since the current is equalized by R_4/Q_{15} and R_5/Q_{16} , we have

$$\Delta V_{BE} = \frac{kT}{q} \ln 4 \approx 36mV \quad (3.2)$$

Thus, the voltage across R_7 becomes

$$V_{R7} = 2 \frac{R_7}{R_6} \frac{kT}{q} \ln(4) \quad (3.3)$$

and this gives

$$V_{B18} = V_{BE18} + \frac{2R_7}{R_6} \frac{kT}{q} \ln 4. \quad (3.4)$$

Fig. 3.2 Differential VI converter with selectable temperature coefficient in Brokaw voltage reference [45].

The temperature coefficient can be tuned by changing the ratio of R_6 and R_7 . The I_o will then be passed to a current-to-frequency converter as shown in Fig. 3.3.

Fig. 3.3 shows the current-to-frequency converter in transistor-level circuit. The current-to-frequency converter used in this design contains a grounded capacitor, C . On the other hand, the transistors $Q_{26}/Q_{28}/Q_{33}$ are used to charge up the capacitor whilst the transistors Q_{29}/Q_{32} are used to discharge the capacitor. A Schmitt trigger is used in this design. It comprises Q_{21} - Q_{25} , R_{10} - R_{18} and Q_{31} . The higher threshold voltage of the Schmitt trigger can be obtained as follows:

$$V_{cH} \geq \frac{(V_{CC} - V_{BE33})R_{11}}{(R_{10} + R_{11})} + V_{BE33} + V_{BE21(off)} - V_{BE22(on)} \quad (3.5)$$

whereas the lower threshold voltage is obtained as

$$V_{cL} \leq \frac{(V_{CC} - V_{CE(sat)31})R_{11}}{R_{10} + R_{11}} + V_{CE(sat)31} + V_{BE21(on)} - V_{BE22(off)} \quad (3.6)$$

Fig. 3.3 Current-to-frequency converter [45].

For the charging current, I_C , it is equal to I_o . For the discharging current it can be shown as

$$I_D = I_o + \frac{I_{CE21}}{\beta_{F21}} \quad (3.7)$$

The oscillating frequency for this current-to-frequency converter is obtained as

$$f_0 = \frac{I_C I_D}{C \Delta V (I_C + I_D)} \quad (3.8)$$

The experimental results have shown that the linearity of the output frequency for the voltage-to-frequency converter is 0.186%. Fig. 3.4 shows the simulated output frequency with different R_7 values. It can be observed that with $R_7=1.09\text{k}\Omega$, this circuit can achieve the best temperature coefficient which turns out to be less than $\pm 192\text{ppm}/^\circ\text{C}$.

Fig. 3.4 Simulated output frequency vs temperature with various R_7 values[45].

3.3. *Ferrari's Resistance-to-Frequency Converter [9]*

Fig. 3.5 shows the circuit architecture of a resistance-to-frequency converter proposed by Vittorio Ferrari. In this circuit, two parameters are measured. They are

- (i) Bridge resistance (a function of temperature), which is converted into duty cycle of the output signal
- (ii) Fractional bridge imbalance, which is converted into output frequency.

This circuit utilizes a full bridge VOCD Wheatstone Bridge architecture. The driving current is generated by an external resistor, clamped by an operational amplifier with an input reference of $V_{DD}/2$.

Fig. 3.5 Ferrari's resistance-to-frequency converter [9].

The biasing current for the bridge, I_B is set to be 8 times of I_{REF} in this design. two high gain differential amplifiers are used. One of the differential amplifier (DA1) is used to amplify the output voltage (V_U) of the Wheatstone Bridge. The other (DA2) is used to amplify the voltage V_B , which contains the information of bridge resistance. To cancel out the offset of the instrumentation amplifier, the polarity of the input is switched periodically. The chopping clock signals (Φ_1 , Φ_2) are self-generated through the SR-latch output, V_{SW} . A biasing current, I_0 is used to generate the center frequency for this resistance-to-frequency converter. The output frequency of this resistance-to-frequency converter taken at V_{SW} and V_{OUT} can be derived as

$$f = f_0 \left(1 + MG_I \frac{R_B}{R_G} \gamma \right) \quad (3.9)$$

where $M=8$, G_1 =gain of differential amplifier=51, $\gamma=[R_2/(R_1+R_2)-R_4/(R_3+R_4)]$.

For the duty cycle, it can be obtained as

$$duty\ cycle = 0.5 \left(1 + \frac{4I_{REF}\Delta R_B MG_2}{V_{DD}} \right) \quad (3.10)$$

where G_2 =gain of DA2 and ΔR_B =variation in bridge resistance.

Fig. 3.6 shows the measured output frequency with input bridge unbalance of $\pm 2.5\%$. The circuit displays a linearity error of less than $\pm 0.5\%$ while consuming 14 mA at 5V. The center frequency is 6.4kHz with a sensitivity of 60.4Hz/1000ppm. From Fig. 3.7, it has shown that the measured output duty cycle sensitivity of 0.276%/(m Ω / Ω) and the linearity error of less than $\pm 0.6\%$.

Fig. 3.6 Measured output frequency vs fractional bridge unbalance

Fig. 3.7 Measured duty cycle vs fractional variation of overall bridge resistance [9].

Fig. 3.8 shows the measured frequency standard deviation at different gate-time over 200 samples. It can be seen that at 20 ms gate time, the frequency standard deviation is about 0.3Hz.

Fig. 3.8 Measured frequency standard deviation vs gate time length [9].

3.4. *Thanachayanont's Resistance-to-Frequency Converter [8]*

Fig. 3.9 shows the conceptual diagram of Thanachayanot's current sensing interface circuit. The differential buffer will firstly convert the change in the resistive sensor into current I_s . The output current relationship with the resistance change can be established as follows:

Fig. 3.9 Thanachayanot's current sensing interface circuit [8].

$$\Delta I = \frac{(V_{DD} - V_{CM})}{R_0} \frac{(\Delta R / R_0)}{(I + \Delta R / R_0)} \quad (3.11)$$

Fig. 3.10 shows the circuit schematic of differential input buffer. The circuit is designed to sense a change of $\pm 1\%$ from a nominal bridge resistance of $2.5\text{k}\Omega$. The differential input stage is realized by a pair of flipped voltage follower (M_{13} - M_{20}) with a common gate voltage of 0.5V . Therefore, the common mode voltage of the resistors becomes

$$V_{CM} = V_{GI} + \sqrt{\frac{2I_I}{\mu_0 C_{ox} (W / L)_I + V_{TH}}} \quad (3.12)$$

where V_G =gate voltage, $\mu_0 C_{ox}$ =MOS transconductance parameter, I_I =drain current, V_{TH} =threshold voltage of the transistor and W/L =aspect ratio of the transistor. The current will be summed or subtracted with the resistive sensor at the source of M_1 and M_2 . To improve the matching of the current mirror, two op-amps are used to equalize the drain voltage of M_3 with M_5 and M_4 with M_6 , respectively. The mirrored current will then be summed at the drain of M_8 with I_{DC} to generate $I_s = I_{DC} + \Delta I$. As shown in Fig. 3.9, this current (I_s) will then be injected into an integrating capacitor, C . When the voltage of the capacitor reaches the threshold voltage of comparator, the output of flip-flop will be high. It turns on the switch at the next clock cycle. The capacitor will be discharged with the current of $I_r - I_s$.

Fig. 3.11 shows that the simulated maximum absolute error is less than 0.23% from an input current range of 200nA. The power dissipation is 270 μ W from a 1.5V supply. The simulated resolution is of 9.67 bit.

Fig. 3.10 Differential input buffer [8].

Fig. 3.11 Simulated number of output digital pulses vs input current [8].

3.5. Azcona's Voltage-to-Frequency Converter [11]

Fig. 3.12 (a) illustrates the schematic of the proposed differential voltage-to-frequency converter. This voltage-to-frequency converter is targeted for rail-to-rail input signals. The input signal will firstly be attenuated by a ratio of $R_1/(R_1+R_2) = 0.5$ as shown in Fig. 3.12 (b). Both the attenuated voltages from each differential input will clamp the potential across R_s to generate I_d . R_s consists of two different types of R_N and R_P which are placed in series to minimize the temperature drift caused by the resistors. The R_s value used is 40k Ω . I_d will be further attenuated by a factor of $K=20/3$ to optimize power consumption. I_d , in conjunction with an offset current I_{off} , will be used to charge up and discharge the integrating capacitor, C through T_3 and T_4 respectively. Cascode current mirror is used to achieve precision current mirroring. The offset current is generated similarly in the voltage-to-frequency converter. It is defined as follows:

$$I_{off} = \alpha \frac{V_{DD} / 2}{KR_{off}} \quad (3.13)$$

with $\alpha=1/6$, $R_{off}=40k\Omega$ and $K=10$. The capacitor value used in this design is 3.125pF. The switching of M_{3C_1} and M_{3C_2} is controlled by the window comparator having the comparison limit of $V_H=2V_{DD}/3$ and $V_L=V_{DD}/3$.

The output frequency is obtained as

$$f_o = \frac{I}{2C(V_H - V_L)} \left(\alpha \frac{V_{in+} - V_{in-}}{KR_s} + I_{off} \right) = \frac{0.9V_{eff}}{V_{DD}} + 0.1MHz \quad (3.14)$$

The experimental results have shown that with a supply of 1.2V, this circuit consumes 80μW. The output frequency has a R^2 nonlinearity of 0.009% and a gain error of 0.27%. The output frequency range of the proposed circuit is from 0.1MHz to 1MHz. Fig. 3.13 shows the measured output frequency of converter versus the input differential voltage at different temperatures. The maximum gain error over the -40 to 120 °C is 3.5%.

Fig. 3.13 Output frequency vs input differential voltage at different temperatures [11].

Chapter 4

Resistance-to-Frequency Converter

4.1. *A Low-Power Current-Mode Resistance-To-Frequency Converter with Wide Frequency Range*

4.1.1. Introduction

A direct current sensing grounded integrator based current-to-frequency converter is proposed in this Chapter. The key advantage is that of simplicity and its straightforward sensing signal conversion. The current-to-frequency converter has been implemented with United Microelectronics Corporation (UMC) 65nm CMOS process technology. The IC measurement results have been obtained and they correlate well with the theoretical results.

4.1.2. Piezoresistive Bridge Sensor Configurations

The proposed transducer is shown in Fig. 4.1. It is implemented using UMC 65nm CMOS technology in which the devices having low (L), regular (R), and high (H) threshold voltages are about 300mV, 500mV and 700mV, respectively. The sizing of each component is listed in Table 4.1. M_{N1} and M_{N2} , and M_{P1} and M_{P2} are having a large area to reduce the noise and mismatch of the transistor. To achieve good input-referred noise performance, M_{N1} and M_{N2} needs to possess high g_m so that the W/L ratio are made high. For M_{P1} and M_{P2} , they are required to possess small g_m , for optimal noise performance. However, due to headroom constraint, the W/L ratios are compromised in the design. For the current mirrors, it is sized to contribute small g_m for good matching. It is noted that the size of each transistor, defined by the ratio of the channel width

and the channel length, is in unit of μm . Using high-gain operational amplifier (op-amp) based topology, the piezoresistive bridge (R_3 – R_4) sensor's middle point potential, V_b , is defined by the potential, V_a , of the resistive divider, which consists of R_1 and R_2 . Therefore, the sensing current, $I_{sens,ac}$, can be expressed as

$$I_{sens,ac} = V_{DD} \left(\frac{I}{R_1 + R_2} \right) \left(\frac{R_1}{R_3} - \frac{R_2}{R_4} \right) \quad (4.1)$$

For a quarter bridge sensor that is having bridge resistance R_0 , we have $R_1=R_2=R_3=R_0$ and $R_4=R_0+\Delta R$. This gives

$$I_{sens,ac} = \frac{V_{DD}}{2R} \left(\frac{\Delta R}{R_0} \right) \left(\frac{I}{1 + \Delta R/R_0} \right). \quad (4.2)$$

Similarly, for a half bridge sensor, we have $R_1=R_2=R_0$, $R_3=R_0-\Delta R$ and $R_4=R_0+\Delta R$. The sensing current becomes

$$I_{sens,ac} = \frac{V_{DD}}{R_0} \left(\frac{\Delta R}{R_0} \right) \left(\frac{I}{1 - (\Delta R/R_0)^2} \right). \quad (4.3)$$

It can be observed that for a quarter bridge sensor, it incurs a high nonlinear term, that is $1/(1+\Delta R/R_0)$ while the piezoresistive half bridge would only incur a nonlinear term of $1/(1-(\Delta R/R_0)^2)$. In this proposed circuit, a bias current, I_{bias} is used to provide a center frequency for the resistance-to-frequency conversion.

Component	V_{TH}	Size	Component	V_{TH}	Size
M_{P1}, M_{P2}	R	80 / 0.5	M_{N6}	H	1 / 1
M_{P3}, M_{P4}	R	20 / 0.5	M_{N7}	R	50 / 0.1
M_{P5}	R	160 / 0.5	M_{B1}, M_{B2}	R	8 / 0.5
M_{P6}	R	200 / 0.1	M_{B3}	R	8 / 0.5
M_{N1}, M_{N2}	R	120 / 0.5	C_C	-	1.48 pF
M_{N3}, M_{N4}	R	80 / 0.5	R_C	-	2 k Ω
M_{N5}	L	10 / 0.1	C_{INT}	-	100 pF

Refer to the converter architecture in Fig. 4.1, it consists of a multi-stage operational amplifier (op-amp) having a flipped voltage follower (FVF) [46], a direct current-sensing grounded integrator, a comparator, a monostable multivibrator and a discharge switch. Regarding the op-amp, the first stage is a telescopic differential gain stage formed by the transistors (M_{N1} - M_{N4} , M_{P1} - M_{P4} ,

M_{B1}) whereas the second stage is an inverting amplifier formed by the transistors (M_{B2} and M_{P5}). A telescopic cascode amplifier topology is employed in this design because it features high dc gain while consuming less power with respect to the folded cascode counterpart. The second stage provides another level of gain boost in order to address the limited output swing of the telescopic cascode amplifier. Miller compensation is achieved by the passive resistor R_C and the passive capacitor C_C . The third FVF stage is formed by the transistors M_{N5} - M_{N6} and M_{B3} . The FVF serves to interface with next integrator stage. Turning to the direct current-sensing grounded integrator, it is composed of the transistor M_{P6} and M_{N7} , the on-chip integrating capacitor C_{INT} and the static biasing current I_{bias} . The very high-drive capability of FVF enables the PMOS transistor M_{P8} to possess a large size such that it directly delivers wide range of sensing current to the C_{INT} . Due to the absence of current mirror(s) in the current-mode conversion process, the linearity as well as precision of the converter will be maintained or not degraded significantly in the context of potential wide output swing encountered in the drain of M_{P6} . Refer to the comparator shown in Fig. 4.2, it is a conventional circuit topology [47] with an added pre-amplifier as the first gain stage in this design. Fig. 4.3 depicts the monostable multivibrator which is employed to control and extend the discharging time of the switch M_{N7} . R_τ and C_τ function as the timing capacitor and timing resistor that determine the discharging time of the switch. Table 4.2 lists each component size in the comparator and multivibrator.

The operation of the resistance-to-frequency converter can be described in the following. The op-amp equalizes the voltage of the resistor bridge and directly couples the sensor current into the grounded integrating capacitor. This

sensor current, $I_{sens,ac}$, combining with the biasing current I_{bias} , forms the summed integrating current, I_{int} . It will then be injected into C_{INT} directly through M_{P6} without going through any current mirror. This reduces the non-idealities introduced by the current mirrors such as channel length modulation and mismatch effect. For the I_{bias} generation, it can be realized in a form of conventional current source or a resistor inserted between the input and the regulated supply. For testing purposes, the latter approach is chosen on the basis of an external resistor. The voltage at the integrating capacitor will be compared with a threshold voltage, V_{ref} , by a comparator. As such, the output frequency for the proposed converter can be obtained as follows:

$$f_{out} = \frac{(I_{sens,ac} + I_{bias})}{C_{INT} V_{ref}} \quad (4.4)$$

In this design, the integrating capacitor, C_{INT} is chosen to be 100pF to reduce the circuit noise, whereas the reference voltage, V_{ref} , is set at 200mV. This yields the theoretical sensitivity of 50Hz/nA.

Fig. 4.2 Comparator with pre-amplifier.

Fig. 4.3 Monostable multivibrator.

Table 4.2 Component sizing for comparator and multivibrator

Comparator	V_{TH}	Size	Multivib.	V_{TH}	Size
M_{P1}, M_{P2}	R	3 / 0.3	M_{P1}	L	0.5 / 0.06
M_{P3}, M_{P4}	L	2 / 0.06	M_{P2}, M_{P3}	L	6 / 0.06
M_{P5}, M_{P6}	L	0.5 / 0.1	M_{P4}	H	6 / 0.06
M_{N1}, M_{N2}	L	1.5 / 0.3	M_{P5}	H	12 / 0.06
M_{N3}, M_{N4}	L	1 / 0.1	M_{P6}	H	24 / 0.06
$M_{N5}, M_{N6}, M_{N7}, M_{N8}$	L	0.5 / 0.1	M_{N1}	L	0.5 / 0.06
M_{B1}	R	8 / 0.5	M_{N2}, M_{N3}	L	2 / 0.06
M_{B2}	R	16 / 0.5	M_{N4}	H	2 / 0.06
—		—	M_{N5}	H	4 / 0.06
—		—	M_{N6}	H	8 / 0.06
—		—	R_{τ}	-	20.1 k Ω
—		—	C_{τ}	-	540 fF

4.1.4. Non-ideal Effects

Non-ideal behaviour of the interface circuit often leads to degradation in the circuit performance. To design an interface with high precision, these non-ideal factors must be studied and taken into consideration. Thus, each critical non-ideal effect on the respective circuit is examined in detail in this section.

These non-ideal effects are:

- (i) Offset of Op-amp
- (ii) Offset of comparator
- (iii) Delay of reset switch and comparator.

4.1.4.1. Offset of Op-amp

The offset for the op-amp can be modeled as V_{OS} at the input of the transistor M_{N2} while the transistor M_{N1} serves as the reference source. The offset effect on the signal current for quarter bridge interface can be derived as

$$I_{sens,ac_nonideal} = I_{sens,ac} - \frac{2V_{OS} [I + \Delta R / (2R)]}{R [I + \Delta R / R]} \quad (4.5)$$

Similarly, for half bridge interface, we obtain as follows:

$$I_{sens,ac_nonideal} = I_{sens,ac} - \frac{2V_{OS}}{R [I - (\Delta R / R)^2]} \quad (4.6)$$

From (4.5) and (4.6), the offset voltage will introduce an offset current. In order to reduce the offset effect of op-amp, a large size of $120\mu\text{m}/0.5\mu\text{m}$ for each transistor in the differential pair in conjunction with the common centroid layout technique [48] is adopted to improve the matching characteristic of the input transistor pair.

4.1.4.2. Offset of Comparator

The offset of comparator can be modeled as $V_{OS,C}$ at its positive terminal.

With this assumption, the output frequency can be re-written in the form of

$$f_{out} = \frac{(I_{sens,ac} + I_{bias})}{C_{INT}(V_{ref} + V_{OS,C})} \quad (4.7)$$

From (4.7), $V_{OS,C}$ will cause a change in sensitivity. In order to reduce the offset sensitivity against process variations, the input transistor pair of pre-amplifier is not sized at minimum channel length value whilst using the common centroid layout to attain good matching.

4.1.4.3. Delay of Reset Switch and Comparator

It is unavoidable that there exists a delay caused by discharging the capacitor and the comparator, the summed delay effect on the output frequency is approximated by Taylor series as

$$f_{out} \approx f_{out,ideal} [1 - f_{out,ideal} (\tau_s + \tau_c)] \quad (4.8)$$

where $f_{out,ideal}$ is the ideal output frequency, τ_s is the delay of reset switch and τ_c is the delay of comparator. It is noted that the size of each transistor, defined by the ratio of the channel width and the channel length, is in unit of μm . From (4.8), this indicates that any delay of the discharging switch will introduce a frequency error of $f_{out,ideal}^2 (\tau_s + \tau_c)$. As a consequence, it will degrade the linearity of the resistance-to-frequency converter. In order to reduce the delay time in discharging the capacitor, a large W/L ratio NMOS switch is employed

to discharge the integrating capacitor sufficiently in 5ns. To study the trade-off between linearity and offset trade-off, 500 runs of Monte Carlo (MC) simulation on the comparator offset variation. This is conducted by setting the channel length for the input pair and the current mirrors of preamplifier to 60nm, 300nm, and 1.5 μ m. Then, the linearity for the current-to-frequency conversion is studied by running the transient simulations at the input current range of 30nA - 60 μ A. The W/L ratio is kept constant for both types of simulations. The MC results are illustrated in Fig. 4.4 whereas the nonlinearity plots are depicted in Fig. 4.5 using the nonlinearity definition [49] as follows:

$$Nonlinearity(\% Full Scale) = \frac{f_{measured} - f_{ideal}}{f_{ideal,max}} \times 100\% \quad (4.9)$$

where $f_{measured}$ = measured output frequency, f_{ideal} = theoretical output frequency by best fit curve and $f_{ideal,max}$ = maximum theoretical output frequency by best fit curve. From Fig. 4.4, although the offset will suffer about 6mV in offset variation with length=300nm, the linearity degradation is minimal. Thus, the optimal length of the input transistor is chosen to be 300nm.

(a)

(b)

(c)

Fig. 4.4 (a) Comparator offset at L=60nm (b) Comparator offset at L=300nm (c) Comparator offset at L=1.5 μm .

Fig. 4.5 Simulated linearity at $L = 60\text{nm}$, 300nm and $1.5\mu\text{m}$

4.1.5. Benchmark with Conventional Current-Mode Converter

The non-ideal effects, which are caused by the current mirrors for sensor current signal transfer in the current-mode converter, are investigated. Fig. 4.6 presents a representative circuit [8] designed under identical 65nm CMOS technology and same supply voltage. The key focus is to study the impact of current mirrors mismatch on precision and linearity. The proposed circuit and the prior-art circuit [8] are designed using the following criteria:

- (i) The sensor used will have the same bridge resistance of $1\text{k}\Omega$ and the maximum fractional bridge imbalance of $\pm 2.5\%$, with the same common mode input voltage of 0.6V .

- (ii) The sensitivity of output frequency with respect to the fractional bridge imbalance are the same at typical case, which is set at $56\text{Hz}/(\mu\Omega/\Omega)$ as an example. It is given that sensitivity is defined as

$$S = \frac{df}{d(\Delta R / R_0)} \quad (4.10)$$

where $df/d(\Delta R/R_0)$ is the slope of output frequency versus the fractional bridge imbalance.

- (iii) The mismatch of the current mirrors will be modeled as $\pm 1.5\%$ different in transistor's width (I_{bias} current source transistor for the proposed converter and M_{B1} , M_{B2} , M_{B5} , M_{P5} , M_{P6} , M_{P10} , and M_{N2} for the conventional current-mode sensor interface). Current mirror mismatch in each op-amp is ignored in this study.

Fig. 4.6 Conventional current-mode bridge sensor interface using topology of [8].

(a)

(b)

Fig. 4.7 (a) Simulated output frequency at worst case with $\pm 1.5\%$ width mismatch. (b) Simulated output frequency and full range non-linearity after trimming.

For fair comparison, I_{bias} of the proposed circuit is implemented using a conventional current source. The simulation results of both circuits are compared in Fig. 4.7. It can be seen that, for $\pm 1.5\%$ of current mirror mismatch, the conventional converter exhibits an offset drift of $\pm 1.2\text{MHz}$ whereas the proposed circuit only exhibits an offset drift of $\pm 20\text{ kHz}$. In order to verify the effect of current mismatch on the linearity, the offset is trimmed by varying the biasing current in M_{B5} . This is regarded as the normal calibration procedure for nulling the offsets in any sensor system. It can be seen that an extra nonlinearity of 0.5% can be induced by the mismatch of current mirrors. With these simulation results, it has validated that the current mirrors involved in sensor current signal transfer will cause higher variation in offset frequency and degrade the linearity of converter.

4.1.6. Experimental Results and Discussions

The converter is realized using UMC 65nm CMOS technology with the chip micrograph presented in Fig. 4.8. The ICs are packaged by QFN 40 packaging and they are tested on printed circuit board with on board regulator. The equipment used for testing is Tektronix TDS5052B oscilloscope, Agilent 34461A multimeter, TP04000 thermostream system and Agilent 54641A oscilloscope. The test setup is shown in Fig. 4.9. Three chips were measured to confirm the consistency of converter's circuit function. At room temperature, the average input offset of the amplifier is measured as 0.9mV . Powered by a single 1.2V supply, the core circuit current consumption is $139.7\mu\text{A}$ on average without the offset frequency biasing current I_{bias} . Turning to the evaluation of offset for the comparator, the peak-to-peak output value of the triangular waveform monitored through the on-chip source-follower buffer tapped at C_{INT} ,

has revealed an average offset of -1mV based on $V_{ref} = 200\text{mV}$. Fig. 4.10 shows the output waveform of chip 1 at 1.2 kHz.

The proposed converter is verified for three types of sensor application. They are (i) current-to-frequency converter, (ii) half bridge sensing interface and (iii) quarter bridge temperature sensing interface. Since the objective is to demonstrate the applications of the proposed circuit in piezo-resistive bridge sensor interface, only 1 chip (chip 1) measured data is given for (ii) and (iii).

Fig. 4.8 Micrograph of the proposed converter.

Fig. 4.9 Test setup of the proposed sensor interface.

Fig. 4.10 Output waveform of chip 1 at 1.2kHz.

4.1.6.1. Current-to-Frequency Converter

In this configuration, the relationship of the integrating current to the output frequency is being measured. For the measurement setup, the discrete resistors in associated with a fixed voltage bias are used to generate the input test current. Fig. 4.11 depicts the output frequency of the circuit versus input

current. Using best fit curve, an average sensitivity of 41.5Hz/nA is measured. The drift of sensitivity from the theoretical value is mainly due to the process variation of the integrating capacitor value and the offsets introduced by the circuit blocks. To compensate the drift in sensitivity, the capacitor trimming circuit can be added to the proposed converter. The average measured output frequency range of the circuit is 2.488MHz, demonstrating wide frequency range characteristic. From the plot in Fig. 4.11, the measured maximum nonlinearity in percentage full scale of the current-to-frequency converter is about 0.6%.

To measure the standard deviation of the frequency, σ_f , the experimental setup is described in the following. A Tektronix TDS5052B oscilloscope to evaluate the chip's output which is in the form of sawtooth waveform. In order to emulate a gate time of 16ms, the average frequency reading of N number of triggers are taken at maximum and minimum frequency, with

$$N = T_{measure} f_{measure} \quad (4.11)$$

where $T_{measure}$ is the gate time and $f_{measure}$ is the average output frequency. The distribution of the 50 samples taken at $I_{int}=60\mu A$ is illustrated in Fig. 4.12. The average standard deviation for three chips' statistical data pertaining to the deviation of output frequency is obtained to be 19.8Hz at $I_{int}=30nA$ and 539Hz at maximum full-scale sensor integration current, $I_{int} = 60\mu A$. It can be seen that the variation of σ_f of the three chips at maximum output frequency is less than 100Hz. This is considerably small in comparison to the average output frequency range of 2.488 MHz. Such a small variation in σ_f is mainly caused by the die-to-die variation and environmental effect. The performance of the circuit

is measured by TP04000 thermostream system from -30°C and 80°C . The system can test the device with 0.1°C accuracy. To ensure the thermal drift of resistors used in this test does not significantly cause the impact on the results, low temperature coefficient ($\leq \pm 50\text{ppm}/^{\circ}\text{C}$) resistors are employed. Fig. 4.13 shows the measured transfer functions among three chips for corner temperatures at -30°C and 80°C , respectively. An average sensitivity drift of -3.32% is obtained at -30°C and of 4.21% at 80°C . The sensitivity drift against temperature variation is mainly caused by the offset in comparator. It can be minimized by increasing the size of input pair through the trade-off between the matching and the delay. Alternatively, other low-offset circuit technique can be employed to reduce the offset at the expense of increased complexity and power consumption.

Fig. 4.11 Measured output frequency at various I_{int} for chip 1, chip 2 and chip 3.

(a)

(b)

(c)

Fig. 4.12 Distribution of measured frequency at $I_{int}=60\mu A$ (a) Chip 1 (b) Chip 2
(c) Chip 3.

Fig. 4.13 Measured output frequency versus I_{int} at $T = -30^\circ\text{C}$ and 80°C for chip 1, chip 2 and chip 3.

4.1.6.2. Half Bridge Sensing Interface

The proposed circuit is interfaced with a half bridge same direction varying sensor which is emulated by the precision resistors and the multi-turn potentiometers. A resistor of $20\text{k}\Omega$ is adopted to set the center frequency to about 1.2MHz . The resistance value of R_1 and R_2 are $4.7\text{k}\Omega$. As shown in Fig. 4.14, in order to have a $1.0278\text{k}\Omega \pm 2.6\%$ resistance for R_3 and R_4 , a fixed resistor of $1\text{k}\Omega$ is deployed for each R_3 and R_4 . In addition, the variable resistors of 50Ω are placed in series with the respective fixed resistor. An optional extra 25Ω fixed resistor is also connected in series with the variable resistor when needed for full range measurement. As shown in Fig. 4.15, the measurement results have shown that with $1.0278\text{k}\Omega$ bridge resistance and a variation of $\pm 2.6\%$ for fractional bridge imbalance, the output frequency can range from 5.5kHz to 2.31MHz in this design, yielding the sensitivity of $44.43\text{Hz}/(\mu\Omega/\Omega)$. The maximum nonlinearity is less than 0.6% full scale.

Fig. 4.14 Test Bridge Setup

Fig. 4.15 Measured output frequency and full range nonlinearity at various fractional bridge imbalance

4.1.6.3. Quarter Bridge Temperature Sensing Interface

The converter is also interfaced with a platinum resistance temperature detector (RTD), with the model number P10K.520.6W.B.010.D manufactured by Innovative Sensor Technology [50]. The sensor bridge is configured in quarter bridge configuration. The purpose of this experiment is to verify the functionality of the converter in the real-world application by interfacing it with a commercial temperature sensor. Referring to Fig. 4.14, R_4 serves as the RTD sensor, and $R_1=R_2=4.7\text{k}\Omega$ in the quarter bridge configuration. To achieve a zero output current for a quarter bridge temperature sensor at room temperature, R_3 is needed to have the same value as that of R_4 at room temperature. From the room temperature measurement result, the RTD sensor's resistance is about $11\text{k}\Omega$. Thus, R_3 value is chosen to be $10.97\text{k}\Omega$. As for the converter, the center frequency is set to be 680 kHz at 25°C . The temperature sensor is placed inside the temperature forcing unit. The measured results are plotted in Fig. 4.16. It is apparent that the curve displays some non-linearity because it comes from the nonlinear characteristic of Quarter Bridge as stated in (4.2). The measurement results are compared with the theoretical results. They indicate good agreement.

Fig. 4.16 Measured and theoretical output frequency at various temperatures

4.1.7. Performance Comparison

Table 4.3 summarizes the measured results of the proposed resistance-to-frequency converter which is based on the average of three chips' results. They are compared with other reported frequency-output based interfaces. It can be seen that the proposed work, with 168μW quiescent power at 1.2V, has achieved one of the lowest power consumption values and supported the integration without external timing capacitor. The nonlinearity is also comparable to other counterparts. The efficiency of energy-noise product among the circuit architectures is evaluated through figure of merits which are defined as follows:

$$FOM_1 = Power \times T_{measured} \times \frac{\sigma_f}{f_{max} - f_{min}} \quad (4.12)$$

$$FOMn_1 = Power \times T_{measured} \times \frac{\sigma_f}{(f_{max} - f_{min}) / [(\Delta R / R_0)_{max} - (\Delta R / R_0)_{min}]} \quad (4.13)$$

$$FOM_2 = Power \times T_{measured} \times \left(\frac{\sigma_f}{f_{max} - f_{min}} \right)^2 \quad (4.14)$$

$$FOMn_2 = Power \times T_{measured} \times \left[\frac{\sigma_f}{(f_{max} - f_{min}) / [(\Delta R / R_0)_{max} - (\Delta R / R_0)_{min}]} \right]^2 \quad (4.15)$$

where $T_{measured}$ = gate time, f_{max} = maximum output frequency, f_{min} = minimum output frequency, σ_f = maximum standard deviation of output frequency, $(\Delta R / R_0)_{max}$ = maximum change in bridge resistance in percentage and $(\Delta R / R_0)_{min}$ = minimum change in bridge resistance in percentage. All of the parameters are measured at typical condition. It is noted that the variation of output frequency is related to the noise. The FOM_1 is similar to the Walden FOM [51] while FOM_2 is similar to the thermal FOM [52]. As the input resistance range may be different among various resistive bridge sensors, the FOM_1 and FOM_2 are normalized with the respective input resistance range so as to provide fair comparison among the interface circuits. Compared to [9], [11], the proposed circuit has achieved the best $FOMn_1$ and $FOMn_2$ due to its low power consumption and wide frequency range. Although the proposed interface circuit has a slightly worse $FOMn_2$ compared to [6] which relies on the JFET devices to achieve low noise. Thus, the circuit [4] may not be favorable for the application on today CMOS based integrated circuits. On the contrary, the proposed work can be fully integrated with the CMOS technology

nodes. Nevertheless, it can be further improved through the addition of low-frequency noise cancellation technique such as auto-zeroing technique, chopper stabilization technique and so forth.

Table 4.3 Comparison of other resistance-to-frequency converters and voltage-to-frequency converters

Param.	[45] TIM 1998	[6] TIM 2000	[7] TCAS II 2006	[9] Sens. Act., A 2007	[8] ETRI 2007	[53] TIM 2011	[11] Sensors J. 2013	This Work	
Tech.	Disc.	Disc.	0.25 μm CMOS	0.7 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	65 nm CMOS	
Supply (V)	3.3	± 6.5	2.5	5	1.5	1.8	1.2	1.2	
Input Range	$\pm 15\text{mV}^*$	5m Ω/Ω	0.1-0.8V	$\pm 0.025\Omega/\Omega$	$\pm 0.01\Omega/\Omega$	0-1.2V	0-1.2V	30n-60μA	
Power (mW)	NA	81.3**	NA	67	0.270	0.375	0.080	0.168	
Sensitivity	NA	0.5 Hz/($\mu\Omega/\Omega$)	520 kHz/V	60.4 Hz/1000ppm	5 $\mu\text{V/V/mmHg}$	861 kHz/V	750 kHz/V	41.5 Hz/nA	
Temp. Range ($^{\circ}\text{C}$)	0 to 50	NA	NA	NA	NA	-20 to 120	-40 to 120	-30 to 80	
Nonlin. (%)	0.186	$\pm 0.2^{\#}$	$\pm 1^{\#}$	$\pm 0.4^{\#}$	0.23	0.4	0.009 ^{##}	$\pm 0.6^{\#}$	0.011^{##}
Timing Capacitor	External	External	Integrated	External	Integrated	Integrated	Integrated	Integrated	
σ_f (Hz)	NA	0.2	NA	0.3	NA	NA	NA	539	
Freq. Range, Δf (Hz)	15-368k	10k $\pm$ 2.5k	52-416k	6.4k $\pm$ 1.51k	NA	0.1-1.1M	0.1M-1M	1.3k-2.489M	
$\sigma_f / \Delta f$ ($\mu\text{Hz/Hz}$)	NA	40.0	NA	99.3	NA	NA	1411 [†]	216	
Conversion time (ms)	NA	10	NA	20	3.3	NA	32.8	16	
FOM ₁ (nJ)	NA	32.5**	NA	133.2	NA	NA	3.7 [†]	0.71[‡]	
FOM ₂ (pJ)	NA	0.325**	NA	82.6	NA	NA	131 [†]	0.95[‡]	
FOM _{n1} (nJ)	NA	32.5**	NA	665	NA	NA	37	3.53[‡]	
FOM _{n2} (pJ)	NA	1.3**	NA	330	NA	NA	522	3.8[‡]	

* Differential input voltage.

** Estimated.

[#] Maximum nonlinearity in % full scale.

^{##} $1-R^2$ nonlinearity.

[†] Estimated based on +5% $\Delta R/R_0$ in half bridge configuration.

[‡] Bias current of 30 μA for center frequency included.

4.2. *A VF Converter Using Hybrid Transconductor for IoT*

4.2.1. **Introduction**

The low power single op-amp IF, which is proposed in section 4.1, is less suitable as compared to traditional VF converter, for it to be used in a sensor network that has multiple sensors having different bridge resistance values. This stems from the fact that the generated integrating current not only proportional to the relative resistance variation, it is also inversely proportional to the bridge resistance. With sensors of different bridge resistance values, the output frequency range can vary widely. For this reason, resistive bridge sensors with voltage output are often used in time-division multiplexed sensor network [14]. Therefore, a VF converter that utilizes a known internal resistance to convert an input voltage into an integrating current prior to converting into frequency is preferable when compared to IF converter. However, a conventional VF converter, which often requires two or more op-amp, tends to have the complicated circuit topology which may increase the power consumption and silicon area. Therefore, in this work, a 0.18 μm CMOS VF converter using hybrid transconductor is proposed. It is noted that the employment of larger technology nodes permits larger device gain arising from higher output resistance. The ease of obtaining high gain factor relaxes the complex circuit topology, leading to the circuit performance with potential low power, small size and low noise. In brief, the architectural simplicity of the proposed circuit serves as one of the key advantages of the work.

4.2.2. Proposed VF Converter Architecture

Fig. 4.17 depicts the proposed circuit architecture of VF converter. It consists of a Wheatstone Bridge, a transconductor, an integrator, a window comparator, a set-reset (SR) latch and a constant current source. The VF converter and Wheatstone Bridge are powered by 1 V regulated supply voltage.

The bridge resistance, R_0 is $1\text{k}\Omega$. A 250Ω resistor, R_{CM} is inserted to provide a dc common mode voltage of 0.6V to cater for the transconductor's dc common-mode input. The output voltage of the Wheatstone Bridge or V_{IN} of the VF converter is obtained as

$$V_{IN} = 0.4 \frac{\Delta R}{R_0} V_{DD} \quad (4.16)$$

A hybrid transconductor is proposed to convert the small output voltage of Wheatstone Bridge into a signal current. The transconductor aims at direct generating the charging current in upper branch and the discharging current in the lower branch without requiring any extra current mirror for sign conversion. This arrangement forms the complementary current push-pull output topology in a natural way. Then, this signal current is being converted through the use of a relaxation oscillator.

The signal current is injected into or drawn from an integrating capacitor (C_{INT}) located in the relaxation oscillator. When the voltage of integrating capacitor reaches the upper threshold voltage (V_H) of window comparator during the charging phase, the Set (S) input to the Set-Reset (SR) latch will be changed to high, causing C_{INT} to be discharged. Similarly, when the voltage of integrating capacitor reaches the lower threshold voltage (V_L)

during the discharging phase, the Reset (R) input to the SR latch will be changed to high, causing C_{INT} to be charged up. With this arrangement, the current information is being converted to frequency domain at the output of SR latch. The SR latch output alternatively turns on the required comparator for half period time to save the power of the system.

Fig. 4.17 Schematic of the VF converter using the hybrid transconductor.

4.2.2.1. Hybrid Transconductor

The transconductor schematic is shown in Fig. 4.18. It is a hybrid combination of a level-shift flipped voltage follower (LSFVF) [54] and a folded shunt-feedback voltage follower (FSFVF) which is modified from the shunt-feedback source follower in [55]. These two follower nodes share similar low output resistance characteristic as that of [54], which is based on negative feedback mechanism to provide a good driving source for resistive load. Refer to FSFVF and consider the case without inserting the folded-cascode gain stage (M_{P5} and I_2) as the interface between the gate of M_{P3} and the drain of M_{N1} , the V_{GS} of shunt-feedback current source transistor M_{P3} will stress the left side of input differential stage (M_{N1} and I_1), particularly significant in low supply

The differential pair M_{N1} and M_{N2} in conjunction with the series-connected resistor, comprising R_{NDIFF} and R_{NPOLY} , serves to translate the input

voltage signal, V_{IN} , into a current signal, I_{SIG} . In this design, the aspect ratio of M_{P1} is the same as that of M_{P2} . The same goes for M_{N1} and M_{N2} . M_{P1} and M_{P2} provide the reference biasing currents of $1.5I_{fc}$, where I_{fc} is the dc current that defines the center frequency of VF converter. This transistor pair is designed to have long channel length and low W/L ratio for good matching. Since the bias current of M_{N1} is equal to that of M_{N2} , $V_{GSN1} \approx V_{GSN2}$. the signal current, I_{SIG} , is given as

$$I_{SIG} = \frac{V_{N1} - V_{N2}}{R_{NDIFF} + R_{NPOLY}} \approx \frac{V_{IN}}{R_{NDIFF} + R_{NPOLY}}. \quad (4.17)$$

where V_{IN} is the input differential voltage. To analyze the error arising from non-zero resistance on N_1 and N_2 pertaining to the I_{SIG} generation, a simplified small-signal analysis is conducted on the small-signal circuit shown in Fig. 4.19. The output resistance of cascode current sources for I_1 , I_2 and I_3 are denoted as r_{oi1} , r_{oi2} and r_{oi3} , respectively, where the subscript i represents the device number. Each has a magnitude equivalent to $g_m r_o^2$. The assumptions for the i_{sig}/v_{in} transfer function are given as follows:

- (i) The current mirror pairs and the input pair have the same transconductance. They are $g_{mp1} = g_{mp2}$, $g_{mn1} = g_{mn2}$ and $g_{mn5} = g_{mn6}$.
- (ii) The current mirror pairs, the input pair and the current source pair (I_2 and I_3) are assumed to have identical output resistance. They are $r_{op1} = r_{op2}$, $r_{op5} = r_{op6}$, $r_{on1} = r_{on2}$ and $r_{oi2} = r_{oi3}$.
- (iii) The gain factor $g_{mx} r_{ox}$ for each transistor gain function is much larger than 1.

The transfer function is obtained as follows:

$$\frac{i_{sig}}{v_{in}} = \frac{I / R_z}{I + \frac{\left(1 + \frac{g_{mp3}}{g_{mn3}}\right) \left[g_{mp5} r_{on1} r_{op5} + r_{oi2} \left(1 + \frac{r_{on1}}{r_{op1}}\right) \right]}{g_{mn1} g_{mp3} g_{mp5} r_{oi2} r_{on1} r_{op5} R_z}} \quad (4.18)$$

Fig. 4.19 Small-signal model of hybrid transconductor.

where the symbols have their usual meanings. Through the first-order binomial expansion on the denominator, the error contributed by the finite loop gain as well as non-zero output resistance is approximated as

$$\varepsilon \approx \frac{I}{g_{mn1} g_{mp3} R_z} \left(1 + \frac{g_{mp3}}{g_{mn3}}\right) \left[\frac{1}{r_{oi2}} + \frac{\left(1 + \frac{r_{on1}}{r_{op1}}\right)}{g_{mp5} r_{on1} r_{op5}} \right] \quad (4.19)$$

Due to the high gain value of cascode gain stage, the error, ε , is negligible. Turning to the temperature compensation, the N+ poly-resistor and

the N+ diffusion resistor, having opposite temperature coefficient with each other, are employed. Therefore, the total resistance can be expressed as

$$R_Z = R_{NDIFF} + R_{NPOLY} + (\alpha_{NDIFF} R_{NDIFF} + \alpha_{NPOLY} R_{NPOLY}) \quad (4.20)$$

The temperature coefficient of N+ diffusion resistor (α_{NDIFF}) is +1.11k ppm/°C whereas the temperature coefficient of N+ poly-resistor (α_{NPOLY}) is -1.28k ppm/°C. To realize an overall resistance of 10kΩ, the N+ diffusion is set to be 5.4kΩ whereas the N+ poly resistor is set to be 4.6kΩ.

In the transconductor, M_{P3} provides the reference current to charge up the integrating capacitor, C_{INT} . On the contrary, M_{N4} is responsible for the discharging action with the reference current. By applying Kirchhoff's current law at the nodes N_1 and N_2 , the charging current flowing through M_{P3} or the discharging current flowing through M_{N4} is as follows:

$$I_{CH} = I_{DCH} = I_{fc} + I_{SIG} \quad (4.21)$$

The coupled signal current associated with the reference I_{fc} will then be mirrored by M_{N5} to discharge or M_{P7} to charge the C_{INT} , respectively. The cascode transistors (M_{N4} , M_{N6} , M_{P4} and M_{P8}) are used to improve the accuracy of current mirrors. The output frequency of VF converter can be derived as

$$f_{OUT} = \frac{I_{DCH} I_{CH}}{C_{INT} (V_H - V_L) (I_{DCH} + I_{CH})} = \frac{I_{fc} + 0.4V_{DD} \frac{\Delta R / R_0}{R_Z}}{2C_{INT} (V_H - V_L)} \quad (4.22)$$

For $C_{INT}=25\text{pF}$, $I_{fc}=1.6\mu\text{A}$ and $V_H - V_L = 400\text{mV}$ in the design, this gives a theoretical center frequency of 80kHz and a sensitivity of 2Hz/(μΩ/Ω).

4.2.2.2. Constant Current Source with PSR Enhanced Circuit

A constant current source circuit is needed to provide a temperature and supply invariant current for center frequency generation. The circuit schematic is depicted in Fig. 4.20, with the exclusion of start-up circuit. To improve the power supply rejection (PSR) of the constant current generator, a feedback circuit, comprising a simple differential stage (M_{N3} , M_{N4} , M_{P4} and M_{P5}) and an output PMOS power transistor (M_{P3}), are employed. R_C , C_{C1} and C_{C2} are the frequency compensation components. The design is made insensitive to temperature variation if the resistor R_B is having similar positive temperature coefficient with that of ΔV_{GS} established between M_{N1} and M_{N2} [11]. It is noted that the M_{N1} and M_{N2} are biased in the subthreshold region to generate a proportional-to-temperature voltage. I_1 , I_2 and I_3 are the currents copies derived from the constant current source circuit with $I_1=4I_2=4I_3=8I_{REF}$.

The window comparator [9] is based on dual operational transconductance amplifier (OTA) types in topology. V_L and V_H are set to be 0.3V and 0.7V, respectively. These voltages can be generated via on-chip low power bandgap references. For the comparator (CMP_2) with lower threshold voltage of V_L , an OTA with the PMOS input transistors is used to cater for input common-mode voltage range. For comparator (CMP_1) with upper threshold voltage of V_H , the NMOS input transistors based OTA is used. To further reduce power consumption, CMP_1 is turned off during the discharging phase. Similarly, CMP_2 is turned off during the charging phase.

Fig. 4.20 Constant current generator with a differential amplifier arranged in feedback for PSR enhancement

4.2.3. Simulation Results and Discussions

The VF converter is implemented and simulated using Globalfoundries 0.18 μm CMOS technology. Refer to the transconductor, the transfer characteristic is illustrated in Fig. 4.21. It has suggested that a transconductance of 0.996mA/V is very close to the target value of 1mA/V. The difference is due to the finite gain error. Including the respective power consumption of biasing circuit for each block, at $V_{IN}=+10\text{mV}$, the power consumption for transconductor, constant current generator and window comparator are 13.4 μW , 2.9 μW and 6.2 μW , respectively. Therefore, the VF converter consumes a total of 22.5 μW at 1V supply, confirming the effectiveness of low-power performance. Fig. 4.22 shows the transient waveforms at the output voltage

(V_{OUT}) and the integrating node (V_{CAP}), which are the voltages at the nodes labelled in Fig. 4.17. The change in output frequency with respect to the fractional bridge imbalance is simulated at temperatures of -40 °C, 25 °C and 90 °C. The results are illustrated in Fig. 4.23. At 25 °C, by best-fit curve, the sensitivity of readout is 1.936Hz/($\mu\Omega/\Omega$) which correlates well with the theoretical value of 2Hz/($\mu\Omega/\Omega$). Meanwhile, the offset frequency of the VF converter is 78.2kHz. The deviation of offset and gain from the ideal is caused by the delay and offset of comparator. For extreme temperatures at -40 °C and 90 °C, the simulated sensitivities are obtained as 1.923Hz/($\mu\Omega/\Omega$) and 1.919Hz/($\mu\Omega/\Omega$), respectively whilst the offset frequencies are obtained as 78.44kHz and 77.94kHz, respectively. There are no significant deviations from the typical case. Consider the nonlinearity of VF converter, it is defined as

$$\%Nonlinearity = \frac{f_{OUT_simulated} - f_{OUT_ideal}}{f_{OUT_ideal_max} - f_{out_ideal_min}} \times 100\% \quad (4.23)$$

where $f_{OUT_simulated}$ = simulated output frequency, $f_{OUT_ideal_max}$ = maximum ideal frequency by best-fit curve and $f_{OUT_ideal_min}$ = minimum ideal frequency by best-fit curve.

Fig. 4.21 Simulated I_{SIG} vs V_{IN} plot of the hybrid transconductor

Fig. 4.22 Output and integrating voltages of the VF converter versus time

The best-fit curve of converter displays the $1-R^2$ value of less than $6 \times 10^{-4} \%$ in the temperature range from -40°C to 90°C . In view of maximum nonlinearity, the VF converter yields 0.11% from the same temperature range. It indicates that the linearity metric is comparable with that of conventional VF converter designs. This is achieved by the impedance reduction via negative feedback of both LSFVF and FSFVF. The distribution of 100 transient noise simulation runs at highest input voltage (+10mV) is also shown in Fig. 4.24.

The results show that that output frequency at maximum input voltage have a standard deviation, σ_f of 31.66Hz and a mean value of 127.02Hz.

Table 4.4 summarizes the performance comparison of the proposed VF converter with other representative reported works. The FOMs are similarly defined by (4.12), (4.13), (4.14) and (4.15). As shown by Fig. 4.25, it has confirmed that the VF converter has achieved best FOM compared to the other representative works.

Fig. 4.23 Output frequency and nonlinearity versus fractional bridge imbalance.

Fig. 4.24 Distribution of output frequency of 100 transient noise runs

Fig. 4.25 $FOMn_1$ and $FOMn_2$ of the proposed works and the other representative works.

Table 4.4 Comparison of other resistance-to-frequency converters and voltage-to-frequency converters

Param.	[45] TIM 1998	[6] TIM 2000	[7] TCAS II 2006	[9] Sens. Act., A 2007	[8] ETRI 2007	[53] TIM 2011	[11] Sensors J. 2013	[56] TIM 2015	This work	
Tech.	Disc.	Disc.	0.25 μm CMOS	0.7 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	65 nm CMOS	0.18 μm CMOS	
Supply (V)	3.3	± 6.5	2.5	5	1.5	1.8	1.2	1.2	1	
Input Range	$\pm 15\text{mV}^*$	$5\text{m}\Omega/\Omega$	0.1-0.8V	$\pm 0.025\Omega/\Omega$	$\pm 0.01\Omega/\Omega$	0-1.2V	0-1.2V	30n-60 μA	$\pm 0.025\Omega/\Omega$	
Power (mW)	NA	81.3**	NA	67	0.270	0.375	0.080	0.168	0.0225	
Sensitivity	NA	0.5 Hz/($\mu\Omega/\Omega$)	520 kHz/V	60.4 Hz/1000ppm	5 $\mu\text{V/V/mmHg}$	861 kHz/V	750 kHz/V	41.5 Hz/nA	1.936 Hz/($\mu\Omega/\Omega$)	
Temp. Range ($^{\circ}\text{C}$)	0 to 50	NA	NA	NA	NA	-20 to 120	-40 to 120	-30 to 80	-40 to 90	
Nonlin. (%)	0.186	$\pm 0.2^{\#}$	$\pm 1^{\#}$	$\pm 0.4^{\#}$	0.23	0.4	0.009 ^{##}	$\pm 0.6^{\#}$ 0.011 ^{##}	$\pm 0.14^{\#}$ 60$\mu^{\#}$	
Timing Capacitor	External	External	Integrated	External	Integrated	Integrated	Integrated	Integrated	Integrated	
σ_f (Hz)	NA	0.2	NA	0.3	NA	NA	NA	539	50.7	
Freq. Range, Δf (Hz)	15-368k	10k $\pm$ 2.5k	52-416k	6.4k $\pm$ 1.51k	NA	0.1-1.1M	0.1M-1M	1.3k-2.489M	78k$\pm$48k	
$\sigma_f / \Delta f$ ($\mu\text{Hz/Hz}$)	NA	40.0	NA	99.3	NA	NA	1411 [†]	216	527.7	
Conversion time (ms)	NA	10	NA	20	3.3	NA	32.8	16	1.3	
FOM ₁ (nJ)	NA	32.5**	NA	133.2	NA	NA	3.7 [†]	0.71 [‡]	0.0965	
FOM ₂ (pJ)	NA	0.325**	NA	82.6	NA	NA	131 [†]	0.95 [‡]	0.051	
FOMn ₁ (nJ)	NA	32.5**	NA	665	NA	NA	37	3.53 [‡]	0.077	
FOMn ₂ (pJ)	NA	1.3**	NA	330	NA	NA	522	3.8 [‡]	0.2	

* Differential input voltage.

^{##} 1- R^2 nonlinearity.

**Estimated.

[†] Estimated based on +5% $\Delta R/R_0$ in half bridge configuration.

[#] Maximum nonlinearity in % full scale.

[‡] Bias current of 30 μA for center frequency included.

Chapter 5

Switched-Capacitor Sensor Interface

5.1. *Introduction*

As Wheatstone Bridge sensors have consumed high current consumption which often lies in the range of 100 μ A to 10 mA, a fast sampling of sensor signal together with time interleaving the sensor signal becomes attractive. Besides, as the output voltage of Wheatstone Bridge sensors are often small, a precision instrumentation amplifier is often needed. Thus, a natural solution to these issues can be resorted to the use of switched-capacitor amplifier because it operates in discrete time-domain and supports a precision gain whilst stable against temperature change. In this section, four representative switched-capacitor sensor interfaces for Wheatstone Bridge sensors will be reviewed.

5.2. *Huang's Telemetry IC for Biomedical Sensors [13]*

In this telemetry IC, an instrumentation amplifier as shown in Fig. 5.1 is employed. To reduce the power consumption of Wheatstone Bridge sensor, a fast sampling phase (Φ_{1a}) is used. The fast sampling phase only lasted for 10 μ s out of a usual sampling phase of 500 μ s. As the fast sampling is independent of the op-amp speed, the design of the op-amp becomes relaxed. This circuit implementation is based on a correlated double sampling integrator, which cancels out the amplifier offset. The correlated double sampling nature of this instrumentation amplifier also suppresses its low frequency noise. A pair of

auxiliary capacitors C_5 is connected between the input and the output of the amplifier to prevent the instrumentation amplifier from running in open loop.

Fig. 5.1 Switched-capacitor instrumentation amplifier used in [13].

The transfer function of the switched-capacitor amplifier is given as follows:

$$\frac{V_O}{V_{IN}} = \frac{C_1}{C_2} \frac{z^{-1/2}}{1 + \frac{C_3}{C_2}(1 - z^{-1})} \quad (5.1)$$

The measurement results have shown that the instrumentation amplifier consumes 29μW from a supply of 3V. The low frequency input-referred noise floor is 3μV/√Hz. The DC offset is 45μV. The common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) are both higher than 70dB. Fig. 5.2 shows the instrumentation amplifier's frequency response. It can

be seen that the instrumentation amplifier has a bandwidth of 32.9Hz. Due to the complexity of circuit, the noise of circuit tends to be high. This is mainly because extra switches and capacitors will introduce extra kT/C noise in the interface.

Fig. 5.2 Frequency response of instrumentation amplifier [13].

5.3. *Claes's Switched-Capacitor Amplifier [14]*

In this design, the instrumentation amplifier's clock is set at 2 kHz for the 16 channels of current driven resistive sensors. Fig. 5.3 shows the instrumentation amplifier reported by Wim Claes for resistive sensor applications. This circuit is a resettable SC amplifier. To reduce the charge injection of the switches, advanced clocks are used for the switches across the

C_2 capacitor pair so that the charge injection are kept constant and independent of input voltage. Extra switches, S_{1B} - S_{6B} and S_{HB} and extra capacitors C_{1B} , C_{2B} and C_{HB} are placed at positive side of op-amp to equalize the impedance seen by the switches. This will help in even distribution of injected charges. A sample-and-hold amplifier is employed to sample the output signal of the switched-capacitor amplifier output.

The measurement results show that the switched-capacitor amplifier consumes $103\mu\text{A}$ whereas the switched-capacitor sample-and-hold circuit consumes $29\mu\text{A}$. The measurement shows that the system in conjunction with the analog-to-digital converter achieves a signal-to-noise ratio of 41.5dB. For this sensor interface, the power consumption of the system is high due to the reason that the sensor is turned on for the whole conversion cycle. Although an extra sample-and-hold circuit can be added to hold the output for the analog-to-digital conversion, it increases the power consumption and noise.

Fig. 5.3 Claes's differential-to-single ended instrumentation amplifier [14].

5.4. *Yen's Instrumentation Amplifier [15]*

Fig. 5.5 shows the schematic of Yen's instrumentation amplifier. In this design, a new offset cancellation scheme is introduced. Three capacitors C_{OS1} , C_{OS2} and C_{OS3} are used to store and cancel the offset voltage of V_{OS1} , V_{OS2} and V_{OS3} . For each switch used in this instrumentation amplifier, two dummy switches with half the length are added to absorb the charge injected during the switching instant. When phase 1 is high, S_1 , S_2 , S_4 , S_5 , S_7 and S_8 are closed and the offset voltage of the op-amps will be stored across the capacitors. The output voltage during this mode is

$$V_o = \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1} \right) (V_+ - V_-) + V_{OS}. \quad (5.2)$$

The offset voltage, V_{OS} can be expressed as

$$V_{OS} = A_1 V_{OS1} + A_2 V_{OS2} + A_3 V_{OS3} \quad (5.3)$$

The gain of amplifiers are

$$A_1 = A_2 = \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1} \right) \quad (5.4)$$

$$A_3 = -2 \left(1 + \frac{R_4}{R_3} \right) \quad (5.5)$$

When phase 2 goes high, the instrumentation amplifier is in offset cancellation mode. During this phase, switches S_3 , S_6 , and S_9 are closed, and the output voltage can be shown as

Fig. 5.4 Schematic of Yen's instrumentation amplifier [15].

$$V_o = \frac{R_4}{R_3} \left(1 + \frac{2R_2}{R_1} \right) (V_+ - V_-) \quad (5.6)$$

The measurement results show that this circuit consumes 61 μ A at a supply of 2.5V. 20kHz clock is used in this instrumentation amplifier. The instrumentation amplifier has a linearity of 0.05% and an average input-referred offset of 0.16mV. The common mode rejection ratio is more than 110dB and the power supply rejection ratio is also more than 102dB. The input-referred noise is 175nV/ $\sqrt{\text{Hz}}$. This gives an input-referred RMS noise of 45 μ V_{RMS} at 20kHz sampling frequency. The requirement of two low-noise operational amplifiers significantly increases power consumption, in particular when driving the resistive loads instead of capacitive loads. Besides, the instrumentation amplifier requires the sensing element to turn on during the whole conversion cycle. To tackle the issue, an extra sample-and-hold amplifier may be added. Unfortunately, this will further increase the power consumption and noise of interface.

5.5. *Nguyen's Switched-Capacitor Sensor Interface [18]*

Fig. 5.5 shows the circuit schematic of Nguyen's inverter based switched-capacitor sensor interface. The operation of the switched-capacitor circuit consists of 3 phases: resetting phase, amplifying phase and holding phase. During the resetting phase ($\Phi_1=0$), the sensor is being powered up by connecting the respective sensor terminal to V_{DD} and ground through S_0 and S_0' respectively. S_3 is being turned on in order to reset the inverter to equalize its input and output voltage to the switching threshold. The transistors, which are realized using high threshold transistor, operate in the subthreshold region. This provides a higher gain and consumes smaller DC current. To enable a fast power up time, a large aspect ratio is used ($25\mu\text{m}/0.5\mu\text{m}$ for NMOS and $45\mu\text{m}/0.5\mu\text{m}$ for PMOS). During the amplifying phase, S_0 and S_0' are flipped, and hence the sensor's supply and ground is flipped. S_3 is opened and C_2 is being switched from the common mode voltage to the output of inverter. The output voltage during this phase is derived as

Fig. 5.5 Nguyen's inverter based switched-capacitor amplifier [18].

$$V_{out} = V_{DD} \frac{\Delta R}{R_0} \frac{C_l}{C_2} \left(1 - \frac{C_l + C_2}{C_2 A_v} \right) \quad (5.7)$$

The measurement results have shown that the sensor will need 37.6 μ s active time for conversion. The average power consumption of the sensor with the interface is 84.5 μ W. A resolution of 7.03 bit is obtained by measuring 100 samples at the saturated output code. As the inverter gain is very low ($\sim$ 40 dB for high threshold device), any process or/and temperature variation will cause significant gain drift on the output. Moreover, the interface is not a gain desensitized design. Gain drift becomes the major disadvantage.

5.6. *Summary of Performance*

The performance of the individual circuit is summarized in Table 5.1. It can be seen that Nguyen's switched-capacitor interface [13] have the lowest power consumption per measurement period, however it has a low SNR compared to the other switched-capacitor implementation. In the scenario that requires high resolution and time multiplexing sensing, Claes's switched-capacitor amplifier [15] is the most suitable solution.

Table 5.1 Performance summary of prior arts

Parameter	JSSC 1998 [13]	JSSC 2002 [14]	TCAS I 2004 [15]	JSSC 2013 [69]	Sens. J. 2014 [18]
CMOS Technology	2 μ m BiCMOS	0.7 μ m CMOS	0.5 μ m CMOS	0.13 μ m CMOS	90 nm CMOS
Supply Voltage (V)	3	3	2.5	1	1
$\Delta R/R_0(\%)$	± 0.0967	–	–	± 10	± 1.28
CMRR at DC (dB)	>70	–	>110	–	–
PSRR (dB)	–	–	102	52	–
Input Referred RMS (μV)	21.2	8.8	45	–	–
SNR(dB)	39.7	67.64 [†]	51.88 [†]	64.44 [*]	44 [*]
Ave. Power (μW)	38	759	465	224.5 [*]	101.3
Meas. Time (ms)	1	0.5	0.05	0.05	0.0376
Energy per measurement interval (nJ)	38	379.5	23.2	11.2	3.81

Chapter 6

A Low Energy-Noise 65nm CMOS Switched-Capacitor Resistive-Bridge Sensor Interface

6.1. *Introduction*

With the goals of devising low energy-noise performance objective, addressing PVT-aware circuit design and providing both gain and offset trimming capability without significantly increasing the power consumption, a switched-capacitor resistive-bridge sensor interface is proposed. The stems from the fact that the switched-capacitor design approach enables the low-frequency noise to be cancelled easily without substantial increased in circuit complexity. The same goes to adding the switched-capacitor based trimming circuits. Besides, through architectural design between the bridge sensor and the interface circuit, it is possible to devise innovative circuit techniques to reduce the power consumption substantially whilst preserving the S/N performance metric. As such, a low energy-noise interface circuit can be implemented.

6.2. *Proposed Sensor Interface*

Fig. 6.1 shows the transducer circuit. The Wheatstone Bridge sensor and the operational amplifier (op-amp) are supplied by a low-dropout (LDO) regulator to improve the immunity against the variation of supply. The change in physical parameter, like pressure as an example, will be translated to the resistive change on each arm of the Wheatstone Bridge sensor. This change in resistance will be converted into the differential voltage in the Wheatstone Bridge. The differential bridge's output voltage is given as

$$V_{IN+} - V_{IN-} = \frac{\Delta R}{R_0} V_{DD} \quad (6.1)$$

From (6.1), it can be seen that the output of sensor is proportional to the supply voltage. Therefore, a LDO regulator is designed to provide a stable supply voltage.

Fig. 6.1 SC correlated double sampling interface with the level shifting capacitor array and the switching op-amp with operation-phase dependent biasing and bandwidth.

Table 6.1: Sizing of Capacitors Pairs in Proposed SC Amplifier

Cap. Pair	Capacitance (pF)	Cap. Pair	Capacitance (pF)
C_{HA}, C_{HB}	6	C_{3A}, C_{3B}	2
C_{1A}, C_{1B}	40	C_{4A}, C_{4B}	2
C_{2A}, C_{2B}	2	—	—

To amplify the sensor signal, a differential-to-single-ended SC amplifier based on [57] is employed. Table 6.1 summarizes the sizes of capacitor pairs used in this design. The amplification portion of SC amplifier consists of the switches $S_{1A}, S_{1B}, S_{2A}, S_{2B}, S_{3A}, S_{3B}, S_{5A}, S_{5B}, S_{6A}, S_{6B}$, the capacitors $C_{HA}, C_{HB}, C_{1A}, C_{1B}, C_{2A}, C_{2B}, C_{3A}, C_{3B}$ and a novel op-amp. The switch pairs are identically designed so that the charge injection and clock feedthrough can be minimized [58]. As the switch pairs S_{3A}/S_{3B} and S_{4A}/S_{4B} are being switched in high impedance nodes, advanced clocks [57] are used for these switch pairs to reduce the charge injection. To reduce the current consumption of sensor, the sensor signal is sampled onto the capacitors C_{HA}, C_{HB}, C_{1A} and C_{1B} in short duration. Fig. 6.2(a) illustrates the clock control signals, input voltage and output voltage of the amplifier, which are simulated using Periodical Steady-State (PSS) analysis. The SC amplifier has a measurement interval of 500 μ s. The duration of which is determined by the non-overlapping clock signals, Φ_1 and Φ_2 , as shown in Fig. 6.2(a). Fig. 6.2(b) shows the zoomed-in view for Φ_1 , Φ_{1A} , Φ_{1S} , Φ_2 and Φ_S . Two pairs of non-overlapping clock signals Φ_1/Φ_2 and their corresponding advanced clock signals Φ_{1A}/Φ_{2A} are made in this design. About 0.5 μ s prior to the main phases Φ_1 and Φ_2 , the Wheatstone Bridge switch

S_{WB} , which is controlled by Φ_S , will be turned on to allow the nodes to be charged up with signals V_{IN+} and V_{IN-} .

During the beginning time of Φ_1 , the sampling switches, S_{1A} and S_{1B} , will be turned on by the clock signal Φ_{1S} for 12.5 μ s to sample the signals V_{IN+} and V_{IN-} onto the respective capacitor pairs, C_{HA}/C_{1A} and C_{HB}/C_{1B} . During this period of time, the op-amp will be switched to high-bandwidth high-power mode by increasing the bias current and activating the low value of compensation capacitance. The detailed design consideration will be discussed in subsection 6.2.1. After the sampling time of 12.5 μ s, the amplifier will be switched to low-power low-bandwidth mode by decreasing the bias current and activating the high value of compensation capacitance. Advanced clocks Φ_{1A} and Φ_{2A} are used to switch C_{3A} and C_{3B} to the corresponding input node of the amplifier. During Φ_1 , C_{2A} and C_{2B} are being shorted to ground. In the end of Φ_1 and Φ_{1A} , the switches that are turned on during these phases (S_{5A} and S_{5B} for Φ_1 ; S_{3A} and S_{3B} for Φ_{1A}) will be turned off. Similarly, during the beginning time of Φ_2 , the bridge output signals V_{IN+} and V_{IN-} , are sampled onto the capacitor pairs, C_{HB}/C_{1B} and C_{HA}/C_{1A} for 12.5 μ s, with the sampling switches turned on by the clock signal Φ_{2S} . In advance to Φ_2 , C_{3A} and C_{3B} will be shorted to ground by S_{4A} and S_{4B} respectively. During Φ_2 , C_{2A} will be switched to the output node of op-amp to function as the feedback capacitor. In the meantime, C_{2B} will be shorted to ground. In the end of Φ_2 and Φ_{2A} , the switches that are turned on during the phases (S_{6A} and S_{6B} for Φ_2 ; S_{4A} and S_{4B} for Φ_{2A}) will be turned off.

To simplify the derivation of the transfer function, C_1 , C_2 , and C_3 represents the respective capacitor pair C_{1A}/C_{1B} , C_{2A}/C_{2B} , and C_{3A}/C_{3B} . With the

assumption of an ideal op-amp, at the end of Φ_2 , the z-transform of the transfer function of this SC circuit can be approximated as

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{C_1}{C_2} (1 + z^{-1/2}) \quad (6.2)$$

If the input signal frequency is very low, the transfer function can be approximated as

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{2C_1}{C_2} \quad (6.3)$$

A five-bit trimming circuit for C_2 pair is also incorporated to allow compensation of sensor sensitivity in variation. To further reduce the power of sensor interface, a SC level-shifting design similar to [59] is adopted. Using the passive capacitors in conjunction with the on-chip regulator as the reference function, the required dc output offset of the SC architecture can be generated. Due to the sharing of common regulator circuit from the sensing system, this eliminates the need of an extra analog ground generation circuit. The generation of the DC output voltage from the capacitive trimming circuit and the regulator will be discussed in section 6.2.2.

(a)

Fig. 6.2(a) Simulated clock control signal, input voltage and output voltage of the proposed SC amplifier for 2 clock cycles. (b) Zoomed-in view of clock signals Φ_I , Φ_{IA} , Φ_{IS} , Φ_2 and Φ_S from 11.245 ms to 11.26 ms.

6.2.1. Dynamically-configured op-amp

Fig. 6.3 shows the proposed two-stage telescopic cascode switching op-amp with dynamically configured biasing circuit and bandwidth-controlled compensation network. A capacitive start-up circuit [60] is adopted to reduce the power of the interface. Compared to traditional switched-op-amp design [61], [62], the proposed circuit is different in the way that the proposed design

allows almost instantaneous sampling action, which is not significantly influenced by the switching transition from low-power mode to the short duration high-power mode. Besides, it gives the driving capability all the time, thus providing ease of interfacing with the following electronic circuit such as A/D converter. More importantly, this work proposed an operation-phase-dependent compensation scheme to reduce the thermal noise during low-bandwidth low-power mode.

In this design, M_{BB} serves as a V_{GS} sensor for body bias of M_{N1} , M_{N2} , M_{N3} , M_{N4} , M_{N5} , M_{N6} , and M_{N7} . The body bias aims to reduce the respective threshold voltage for the transistors M_{N1} , M_{N2} , M_{N3} , M_{N4} , M_{N5} , M_{N6} and M_{N7} . This in turn improves the voltage headroom for M_{P3} and M_{P4} . Under the scenario of worst case corner for process and temperature condition, the V_{GS} sensor dedicated to bulk biasing design can improve the low-frequency gain of amplifier by about 4dB.

Fig. 6.3 Proposed switching op-amp with operation-phase-dependent biasing and bandwidth.

During the sampling of sensor signal, M_S will be turned on to increase the biasing current of op-amp, leading to the increase of bandwidth and slew rate of the amplifier. The compensation capacitor C_{CI} is also switched to the low impedance node ① in order to increase op-amp's bandwidth during the high-bandwidth high-power phase, Φ_S . The low impedance node is established by the transistor M_{BC} in diode connection to generate a V_{gs} value close to that of the transistor M_{N7} at zero input signal. This arrangement allows minimal disturbance caused by the switching action on C_{CI} . After the high-bandwidth high-power phase has ended, M_S will be turned off to reduce the power dissipation and the op-amp enters low-bandwidth low-power phase, Φ_S' . C_{CI} will then be switched to the output node of first stage through the transmission gate TG_{S2} to reduce the thermal noise [63]. Although the switches TG_{S1} and TG_{S2} will introduce extra noise, it is not significant due to the high gain of telescopic amplifier in the first stage design. On the other hand, the switching action will introduce output ripples at the falling edge of control signals Φ_{1S} and Φ_{2S} . Nevertheless, they will not introduce any potential error because the valid output only happens at the end of Φ_1 and Φ_2 . Without this operation-phase dependent compensation network, periodical noise simulation has revealed that the integrated noise power from 1Hz to 1kHz is improved from 246nV² to 170nV². In other words, the noise power will degrade by 45% with respect to current design without the operation-phase dependent compensation. Fig. 6.4 shows the simulated output noise spectral density for these 2 cases.

Fig. 6.4 Simulated output noise power spectral density of the op-amp with and without operation-phase-dependent compensation scheme.

To investigate the bandwidth requirement needed for sampling phases denoted as Φ_{1S} and Φ_{2S} , the voltage difference between Φ_1 to Φ_{2S} is derived for a maximum input frequency of 40Hz. The criterion is based on 9-bit accuracy at the end of Φ_{2S} . V_{Φ_1} , V_{Φ_2} , $V_{\Phi_{1S}}$, and $V_{\Phi_{2S}}$ is defined as the respective output voltage at the end of Φ_1 , Φ_2 , Φ_{1S} , and Φ_{2S} . The change in output voltage between the end of Φ_1 and Φ_{2S} , is denoted as $\Delta V_{\Phi_1 \Rightarrow \Phi_{2S}}$. For simplification, the change in input voltage is assumed to be small and ignored. This is due to low input frequency with respect to the clock frequency. Moreover, the difference between the capacitors' charge during sampling phases and its corresponding holding phases are small and ignored. This leads to $V_{\Phi_{2S}} \approx V_{\Phi_2}$. The z-transform of the transfer function during the end of Φ_1 can be obtained as

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{C_1}{C_2} (-1 + z^{-1/2} + 2z^{-1}) \quad (6.4)$$

Assuming the op-amp with adequate bandwidth, the final voltage change between Φ_I to Φ_{2S} can be approximated as

$$\Delta V_{\Phi_I \Rightarrow \Phi_{2S}}(nT) \approx \frac{C_1}{C_2} \left[V_{in}[nT] + 2V_{in}[(n-0.5)T] - V_{in}[(n-1)T] - 2V_{in}[(n-1.5)T] \right] \quad (6.5)$$

With an input signal frequency of 40Hz, and a maximum input amplitude of $V_{range}/(4C_1/C_2)$, at the end of Φ_{IS} and Φ_{2S} , the input voltage can be obtained as

$$V_{in}[nT] = \frac{V_{range}}{4C_1/C_2} \sin(80\pi nT) \quad (6.6)$$

where V_{range} is the maximum output voltage range. With a clock frequency of 2 kHz, substituting (6.6) into (6.5) and differentiating it with respect to n , we have

$$\frac{d\Delta V_{\Phi_I \Rightarrow \Phi_{2S}}}{dn} = \frac{V_{range} (0.04\pi)}{4} \left[0.0394 \cos \frac{\pi n}{25} - 0.3745 \sin \frac{\pi n}{25} \right] \quad (6.7)$$

By setting $d(\Delta V_{\Phi_I \Rightarrow \Phi_{2S}}[nT])/dn=0$ to find out the maximum point of the equation, the largest change in the output voltage happens when $n=0.83335$. With the n value, the maximum change in the output voltage during Φ_I to Φ_{2S} , which is defined as $\Delta V_{\Phi_I \Rightarrow \Phi_{2S}max}[nT]$, is $0.094V_{range}$.

Since the phase margin of the op-amp is high at the closed-loop gain operation region and the roll-off rate is close to 20dB/decade, it can be approximated as a 1-pole system. For 1-pole system, the op-amp exhibits an output voltage of

$$V(t) = \Delta V_{\Phi_I \Rightarrow \Phi_{2S}}(nT) \left[1 - e^{-2\pi ft} \right] \quad (6.8)$$

where $V(t)$ =voltage at time t , f =bandwidth of the amplifier.

Based on the 9-bit accuracy requirement, we get

$$\Delta V_{\Phi_{I \Rightarrow \Phi_{2S_{\max}}} [nT] - \frac{V_{range}}{2^{9+I}} = \Delta V_{\Phi_{I \Rightarrow \Phi_{2S_{\max}}} [nT] (1 - e^{-2\pi f t}) \quad (6.9)$$

From (6.9), it suggests that the minimum required bandwidth for sampling in a short interval is 58kHz.

Fig. 6.5 shows the stability (STB) simulation results at worst case for the open-loop frequency response of the op-amp in unity-gain configuration, with current probe (iprobe) inserted in the feedback loop. The worst-case unity-gain bandwidth happens at respective corner for slow NMOS and slow PMOS, high resistance, high capacitance and low temperature. In order to further minimize the power consumption, a decompensated op-amp design approach [64] is adopted. The stems from the fact that high gain is always needed to amplify the small sensor signal. For this reason, it is not necessary for the amplifier to be designed for stability at low closed-loop gain at the expense of extra power. Since the sensor has a span variation of $\pm 25\%$, a closed-loop gain of 24.1dB is needed to compensate for +25% variation. Based on this specification, the op-amp is made stable at 24.1 dB to meet the worst-case scenario. Turning to a -25% variation in sensor span, the op-amp needs to provide a closed-loop gain of 28.5dB to attain similar output voltage with that of given sensor span. For a closed-loop gain of 28.5dB, as the op-amp is in the inverting amplifier configuration, the inverse of the feedback factor is 28.8 dB. Refer to Fig. 6.5, the obtained closed-loop bandwidth for the op-amp is 62.7 kHz. This meets the minimum of 58kHz from the prior analysis.

Fig. 6.5 Simulated open-loop gain and phase versus frequency at worst case bandwidth during Φ_S and Φ_S' .

The DC output voltage gain error caused by finite gain is also derived. The derivation is based on following assumptions:

- (i) The circuit is of good symmetry with $C_I = C_{1A} = C_{1B}$, $C_2 = C_{2A} = C_{2B}$, $C_3 = C_{3A} = C_{3B}$ and $C_H = C_{HA} = C_{HB}$, thus the analysis can be simplified to a switched-capacitor amplifier with single-ended input and single-ended output.

- (ii) $C_I=40\text{pF}$, $C_3\approx C_2=1.5\text{pF}$, $C_P\approx C_4$ and $C_H=6\text{pF}$ for worst case closed-loop gain of 28.5 dB that needs to compensate the sensor variation range.
- (iii) $V_{OUT}=V_{OUT}[nT]=V_{OUT}[(n-1)T]$ and $V_{IN}=V_{IN}[nT]=V_{IN}[(n-1)T]=V_{IN}[(n-1/2)T]$ at DC input.
- (iv) With V_{IN_IH} = voltage hold at C_H during Φ_{IH} and V_{IN_2H} = voltage hold at C_H during Φ_{2H} , $V_{IN_IH}=V_{IN_IH}[nT]=V_{IN_IH}[(n-1)T]$ and $V_{IN_2H}=V_{IN_2H}[nT]=V_{IN_2H}[(n-1)T]$ at DC input.
- (v) For simplicity, the sampling phase during Φ_I and Φ_2 are denoted as Φ_{IS} and Φ_{2S} respectively. Similarly, the holding phase are denoted as Φ_{IH} and Φ_{2H} .

Utilizing charge conservation principle, during the transition of Φ_{2H} to Φ_{IS} , we have

$$\begin{aligned} & C_I(V_{IN_2H} + A_H^{-1}V_{OUT}) + C_2V_{OUT}(1 + A_H^{-1}) + C_2V_{OUT} + C_P(A_H^{-1}V_{OUT}) \\ &= C_I(V_{IN} + A_S^{-1}V_{OUT_IS}) + C_2V_{OUT_IS}(1 + A_S^{-1}) + (C_2 + C_P)A_S^{-1}V_{OUT_IS} \end{aligned} \quad (6.10)$$

where C_P = parasitic capacitance seen at the input of the op-amp $\approx C_{4A} = 4\text{pF}$, A_S = open-loop gain of the amplifier at high-bandwidth high-power mode which corresponds to sampling phase, and A_H = open-loop gain of the amplifier at low bandwidth low power mode which corresponds to holding phase and V_{OUT_IS} = output voltage at Φ_{IS} .

During transition from Φ_{IS} to Φ_{IH} , we have

$$C_HV_{IN} + C_I(V_{IN} + A_S^{-1}V_{OUT_IS}) = C_HV_{IH} + C_I(V_{IN_IH} + A_H^{-1}V_{OUT_IH}) \quad (6.11)$$

and

$$\begin{aligned} & C_I(V_{IN} + A_S^{-1}V_{OUT_1S}) + (C_2 + C_P)A_S^{-1}V_{OUT_1S} + C_2V_{OUT_1S}(1 + A_S^{-1}) \\ & = C_I(V_{IN_1H} + A_H^{-1}V_{OUT_1H}) + C_2V_{OUT_1H}(1 + A_H^{-1}) \end{aligned} \quad (6.12)$$

where V_{OUT_1H} is the output voltage during Φ_{1H} .

For transition from Φ_{1H} to Φ_{2S} , we have

$$\begin{aligned} & C_I(V_{IN_1H} + A_H^{-1}V_{OUT_1H}) + (C_2 + C_P)A_H^{-1}V_{OUT_1H} \\ & = C_I(-V_{IN} + A_S^{-1}V_{OUT_2S}) + C_2V_{OUT_2S}(1 + A_S^{-1}) + C_PA_S^{-1}V_{OUT_2S} \end{aligned} \quad (6.13)$$

where V_{OUT_2S} is the output voltage at Φ_{2S} .

For transition from Φ_{2S} to Φ_{2H} , we have

$$C_H(-V_{IN}) + C_I(-V_{IN} + A_S^{-1}V_{OUT_2S}) = C_HV_{IN_2H} + C_I(V_{IN_2H} + A_H^{-1}V_{OUT}) \quad (6.14)$$

and

$$\begin{aligned} & C_I(-V_{IN} + A_S^{-1}V_{OUT_2S}) + C_2V_{OUT_2S}(1 + A_S^{-1}) + C_P(V_{OUT_2S}A_S^{-1}) \\ & = C_I(V_{IN_2H} + A_H^{-1}V_{OUT}) + C_PA_H^{-1}V_{OUT} + C_2V_{OUT}(1 + A_H^{-1}) \end{aligned} \quad (6.15)$$

Solving (6.10) - (6.15), we have

$$V_{OUT} \approx \frac{2C_I}{C_2} \left(1 - KC_I A_S^{-2} - \left(\frac{C_P + C_2}{C_2} + KC_H \right) A_H^{-2} \right) V_{IN} \quad (6.16)$$

where $K = C_I / (C_2(C_H + C_I))$. It can be seen that the open-loop gain under high-bandwidth high-power mode has larger impact because C_H is smaller than C_I .

Assuming $A_L \approx A_H$, for a 0.5 LSB full scale span error caused by finite gain, A_H should be made higher than 44.7dB. Since the proposed circuit has displayed more than 60 dB open-loop gain in corner cases, the gain error is negligible.

6.2.2. DC Output Voltage Generation and Trimming Circuit

To reduce the extra power needed from the analog ground generation circuit, the SC level-shift design approach is employed. It makes use of real ground, regulated supply, SC network and ground-compatible SC op-amp. The shared supply source results in eliminating an extra analog ground generation circuit that consumes power.

To generate the quiescent DC output voltage for zero sensor signal, Fig. 6.6 (a) depicts a basic voltage level-shift trimming network [59] that involves a programmable capacitor C_{4A} with the regulated supply voltage serving as the reference input signal. The programmable capacitor C_{4A} is used to trim the output DC voltage to compensate the sensor's offset. Alternatively, Fig. 6.6 (b) shows the capacitor divider based trimming network. The trimming bits are denoted as B_n , where $n=0, 1, 2, \dots, 8$. The fixed capacitors C_5 and C_6 , the binary-weighted trimming capacitors $(2^9-1)C_{TR}$, and the coupling capacitor C_{4A} form the capacitor divider. In this capacitor trimming network, C_{4A} is fixed at 2pF. The generation of DC common mode output voltage is briefly described as follows: during Φ_1 , the top plates of C_5 and programmable trimming capacitor C_{TRA} will be connected to V_{DD} . They will be shorted to ground during phase Φ_2 .

Fig. 6.6(a) Basic trimming network (b) Capacitor-divider based trimming network.

To trim the common mode DC output, the binary-scaled trimming capacitors can be switched to connect in parallel with C_5 to increase V_{DIV} by setting B_n high, as illustrated by C_{TRA} in . Similarly, to reduce V_{DIV} , the trimming capacitors can be programmed by setting B_n low to connect in parallel with C_6 to reduce V_{DIV} , as illustrated by C_{TRB} in Fig. 6.1. Therefore, during Φ_I , V_{DIV} can be approximated as

$$V_{DIV} \approx \frac{\sum_{n=0}^8 2^n B_n C_{TR} + C_5}{C_5 + C_6 + C_{4A} + \sum_{n=0}^8 2^n C_{TR}} V_{DD} \quad (6.17)$$

where B_n has a value of 1 when logic high is asserted and value of 0 when low is asserted. From (6.17), it is apparent that the introduction of C_5 and C_6 terms allows the flexibility of choosing unit capacitance. Moreover, it can be seen that V_{DIV} varies linearly with the capacitance connected in parallel with C_5 . This is a

desirable characteristic for trimming circuits. In this design, the minimum trimming capacitance, C_{TR} is set to $\frac{1}{4} C_{unit}$ by connecting 4 C_{unit} in series. With $C_{unit}=125\text{fF}$, $C_5=106C_{unit}$, $C_6=78C_{unit}$ and $C_{4A}=16C_{unit}$, the minimum resolution that can be attained is 0.764mV for gain of 40.

To illustrate the difference in layout style from Fig. 6.6 (a) and Fig. 6.6 (b), respectively, they are explained as follows. For Fig. 6.6 (a), with 9-bit trimming at the constraint of feedback capacitor of $C_2=2\text{pF}$ in the design, we have

$$\frac{V_{range}}{2^9} = \frac{C_{TR}}{C_2} \quad (6.18)$$

From (6.18), the minimum required C_{TR} is 3fF. However, the minimum unit capacitance of the 3 metal layers in the standard UMC Metal-Oxide-Metal capacitor is about 2.6fF. With C_{2A} and C_{2B} chosen as 2pF, the minimum LSB capacitor can be realized by connecting 4 unit capacitors of 10fF in series configuration since 10fF is a divisor of 2pF. For matching consideration, C_{1A}/C_{1B} , C_{2A}/C_{2B} and C_{4A}/C_{4B} should use the same unit capacitor size. If C_{1A} and C_{1B} are 40pF, it yields 4000 units for each big capacitor, leading to increased layout complexity using the structure in Fig. 6.6 (a). Turning to capacitor divider based trimming network in Fig. 6.6 (b), it provides the flexibility of choosing the unit capacitance. In this design, the unit capacitance is chosen as 125fF instead of 10fF. As such, the number of unit capacitors are reduced to 320 units, thus reducing the layout complexity and improving the matching characteristic of capacitors due to bigger size in unit capacitance.

6.2.3. Low-Dropout Voltage Regulator with Self-Regulated Voltage Reference

Fig. 6.7 shows the schematic of power supply management unit dedicated to the sensor and SC amplifier circuit. The sensor and op-amp are embedded with a conventional three-stage Nested Miller compensated LDO regulator [65]. This on-chip regulator aims to support fast transient response. To generate a stable reference voltage, a voltage reference based on [66] is designed. Modification is made such that it can drive resistive load arising from the external testing equipment. From [66], the reference voltage generated by the native transistor, M_{N9} and the IO transistor, M_{N10} is given as

$$V_{ref}' = \frac{\eta_8 \eta_9}{\eta_8 + \eta_9} (V_{TH9} - V_{TH8}) + \frac{\eta_8 \eta_9}{\eta_8 + \eta_9} V_T \ln \left(\frac{\mu_8 C_{OX8} W_8 L_9}{\mu_9 C_{OX9} W_9 L_8} \right) \quad (6.19)$$

where η =subthreshold slope, μ =electron mobility, C_{OX} =the oxide capacitance, W =transistor width, L =transistor length, V_{TH} =transistor threshold voltage and V_T =thermal voltage. With proper scaling of M_{N9} and M_{N10} , the voltage V_{REF}' can be made insensitive to temperature. Through the self-cascode current mirror pairs, M_{P7} - M_{P10} , the respective current in M_{N9} and M_{N10} is copied into the M_{N11} and M_{N12} in one-to-one ratio. With the same W/L ratio for the native transistor pair, M_{N9} and M_{N11} , and the IO transistor pair, M_{N10} and M_{N12} , V_{REF}'' is regulated to approximately V_{REF}' through the replica design. By trimming R_3 , the V_{REF} can be scaled to the target of 500mV, yielding the regulator output of 1V when the ratio R_1/R_2 is set to 1.

Fig. 6.7 Low drop-out Regulated with self-regulated voltage reference and start-up circuit.

To further enhance the power supply rejection, the voltage reference is simultaneously powered by the on-chip regulator. Since the supply of voltage reference supply is tied from the output of regulator, a special start-up circuit is realized as shown in Fig. 6.7. When the circuit starts up, V_{CI} is not charged up instantly. The transmission gate is turned on. At this juncture, M_{N6} and M_{N7} are turned on to set the V_{ref} of regulator to approximately 0.6V. Due to R_3 and $R_4 \gg 1/g_{mN7}$, this enables the voltage reference to start up in a proper sequence. When the voltage V_{CI} reaches the threshold voltage of inverter chain, the switch S_1 will be turned off to isolate M_{N6} and M_{N7} from the inverting input of error amplifier. Finally, M_{P6} will be switched off to turn off M_{N6} and M_{N7} .

6.3. *Programmable Trimming Circuit*

In this system, the number of trimming bits needed for the circuits are one set of 9-bits digital signal for DC output trimming, one set of 8-bits digital signal for reference voltage trimming and one set of 5-bits digital signal for gain trimming. With a conventional direct trimming, the number of pin count needed is 22 pins. This is because in conventional direct trimming, the gate of each trimming transistor is routed out to connect to the external switches. This high pin count is unacceptable as the conventional quad-flat-no-lead packaging has around 40 pins only.

To reduce the pin count, a digital programmable trimming circuit is designed and integrated into the system. It only requires three address pins ($ADDR<2:0>$), one write pin (WR), one data pin (DATA) and one register select (SEL) pin. With only five pins, the algorithm used allows the programmable trimming circuit to provide 8 sets of 8-bits digital signal or 64 bits digital signal for trimming purpose. As the trimming bits needed for this circuit are 22 bits, only 4 sets of 8-bits digital signal are generated in the implemented trimming circuit. The architecture for the digital trimming circuit is shown in Fig. 6.8. Each square in Fig. 6.8 represents a register made by a D flip-flop. The D flip-flops' data inputs are all connected to the DATA pin. The clock input for the D flip-flop acts as the enable signal and are controlled through the combination logics with the inputs consisting $ADDR<2:0>$, WR and SEL. There is no reset signal for the D flip-flop to reduce the pin count. As a result, the registers are needed to be programmed and initialized after the circuit has started. As shown in Fig. 6.9, during each write operation for the D flip-flop, the DATA, SEL and $ADDR<2:0>$ will change before the WR signal

goes high. This is to prevent accidental data writing into the D flip-flop. The function of the SEL signal is to determine whether to enable the selector or the trimming bank to write data into. The ADDR<2:0> signals will then determine which register in the selector or the trimming register bank to write into.

Fig. 6.8 Programmable trimming circuit.

Fig. 6.9 Timing diagram for a single write operation of D flip-flop.

The simplified programming procedure for the trimming circuit is as follows:

- (i) SEL goes high to enable selector registers. At the same time, ADDR<2:0> is set to '000' to select the first register and DATA set to high. A '1' will then be written into the first register in the selector bank.
- (ii) The above procedure will be repeated for second to fourth register with the DATA set to 0 to write zeros into the remaining register in the selector.
- (iii) SEL will be set to '0' to select the trimming register bank. As the first register is set to '1', the first set of the trimming register set will be enabled. With ADDR<2:0> set to '000', the first register in the trimming register set is enabled. In the meantime, DATA is set to the desire value in order to be written into the first register in the first trimming set.
- (iv) Procedure (iii) will be repeated for the remaining registers in the first trimming register set by setting ADDR<2:0> to the corresponding value.
- (v) The above procedure will be repeated for the remaining trimming register set.

The trimming process has been done by programming a Terasic DE0 board [67].

6.4. *Experimental Results*

Implemented in UMC-65nm CMOS technology, the readout circuit, together with the trimming circuitry, occupies an effective active area of 0.358mm² as depicted in Fig. 6.10.

(a)

(b)

Fig. 6.10 (a) Chip micrograph of the switched-capacitor sensor interface. (b)

Layout of the switched-capacitor sensor interface.

The equipment employed for testing are Agilent DSO-X 4043A oscilloscope, Agilent 33600A function generator, Stanford Research Systems SR1 audio analyzer, Agilent 34461A multimeter, TP0400 thermostream system,

SMC GZ46-2 pressure gauge and Wiltech AS20W compressor and vacuum pump.

The capacitive divider is characterized, and the voltage change with respect to the change of code is presented in Fig. 6.11. It shows that linear trimming can be achieved with the capacitive divider trimming network. Fig. 6.12 shows the transient response of the sensor interface with a direct injected 40Hz differential sine wave signal, with an amplitude of 9.375mV, generated by Agilent function generator. The signal-to-noise ratio (SNR) is then measured with this direct injected sinewave. Fig. 6.13 shows the analysis result of interface's output signal under Fast-Fourier Transform. The observed harmonics at 50Hz, 150Hz and 250Hz are powerline harmonics which come from the function generator. The measured SNR is 55.64 dB. Hence, the output root-mean-square (rms) noise is obtained as $438\mu V_{RMS}$. The total harmonic distortion at 40Hz input signal is measured as 0.0274%. Thus, the signal-to-noise and distortion ratio is estimated as 55.5dB. The effective number of bit that can be achieved is 8.93-bits at 40Hz.

Fig. 6.11 Measured absolute |Voltage Change| vs Trimming Code.

Fig. 6.12 Transient response of the switched-capacitor interface with a 40Hz input signal.

Fig. 6.13 Measured output spectrum at 2kHz sampling rate.

Besides, the temperature variation of sensor interface is measured. The regulated voltage of the LDO regulator is trimmed to 1V with on-chip digital interface at room temperature before the temperature measurement is carried out. The output thermal characteristic of regulator is shown in Fig. 6.14, with a temperature coefficient of $-216\text{ppm}/^{\circ}\text{C}$. This matches with the untrimmed measurement results reported in [66]. The sensor interface is further tested with a direct DC input to obtain the transfer characteristic depicted in Fig. 6.15. The measured gain drift and DC output drift is $29.2\text{ppm}/^{\circ}\text{C}$ and $-188\text{ppm}/^{\circ}\text{C}$, respectively. The output drift also correlates well with that of the regulator since the DC output voltage of SC amplifier is a scaled version of the regulator output voltage.

Fig. 6.14 LDO regulator's output voltage versus temperature change.

Fig. 6.15 Transfer characteristic of the sensor interface with direct DC input at -40 °C, 25 °C and 90°C.

The performance of the sensor interface is also tested with a replica half-bridge sensor and a commercial sensor, which will be discussed in section 6.4.1 and section 6.4.2. The power supply rejection ratio (PSRR) of LDO regulator is also measured and shown in Fig. 6.16. The PSRR definition is given as follows:

$$PSRR(dB) = 20 \log_{10} \left(\frac{V_{supply_ripple}}{V_{out_ripple}} \right) \quad (6.20)$$

where V_{supply_ripple} is supply ripple generated by a network analyzer and the V_{out_ripple} is the output ripple measured by the network analyzer. The LDO regulator has a DC PSRR of 70dB. The power supply rejection ratio (PSRR) is also measured for the system which comprises the SC amplifier, the LDO regulator and the voltage reference. The PSRR at different frequencies is shown

in Fig. 6.17. The measured PSRR at 12Hz is about 64dB. When the supply is changed by +10% and -10%, the interface output, at $V_{IN}=0$ ($V_{OUT}\approx 500\text{mV}$), is changed by $-100\mu\text{V}$ and $+354\mu\text{V}$. Finally, the CMRR of interface circuit is measured by injecting the common-mode and differential-mode sine wave at different frequencies. The result is shown in Fig. 6.18. A CMRR of 97.5dB is obtained at 12Hz.

Fig. 6.16 PSRR of LDO regulator at various frequencies.

Fig. 6.17 PSRR of sensor interface at various frequencies.

Fig. 6.18 CMRR, inverse of common-mode gain and differential-mode gain of sensor interface at various frequencies.

6.4.1. Half Bridge Sensing Configuration

The sensor interface is measured with a test bridge setup shown in Fig. 6.19. To emulate a half bridge sensor with a bridge resistance of $10\text{k}\Omega \pm 1.875\%$, each of R_3 and R_4 consists of a fixed resistor with a value of $9.76\text{k}\Omega$ and a 25-turns variable resistor of $1\text{k}\Omega$ placed in series. Powered by 1.2V supply, the regulator together with the voltage reference consumes $7.8\mu\text{A}$. The bridge sensor and the interface circuit are supplied by the 1V output of regulator, consuming an average current of $12.3\mu\text{A}$ in one measurement interval. The detailed average power consumption is shown in Table 6.2. To trim for the span variation, the sensor interface is measured at maximum and minimum bridge imbalance. Then, the output span will be trimmed by varying the resistance of R_3 as indicated in the regulator schematic in Fig. 6.7. This in turn changes the gain of overall system. Following the gain calibration, the DC output of the sensor interface will then be trimmed by changing the code of the capacitive divider trimming network for the offset calibration.

The transient response of sensing interface in response to the DC signal of test bridge is shown in Fig. 6.20. With zero differential input signal, the output of interface settles to 499.4mV , with 25mV overshoot and 44mV undershoot in clock transitions. This is very close to the target of 0.5V DC output. The dc transfer function and its corresponding output in nonlinearity are plotted in Fig. 6.21. The sensitivity of output voltage with respect to the bridge imbalance is $199.9\text{mV}/(\%\Omega/\Omega)$. The R^2 value for the best fit curve is 0.999995. The DC nonlinearity of this sensor interface is defined as follows:

$$\text{Nonlinearity}(\%) = \frac{V_{\text{out_measured}} - V_{\text{out_ideal}}}{V_{\text{out_max_ideal}}} \times 100\% \quad (6.21)$$

similar to the definition of [7], the proposed circuit has a good DC nonlinearity of less than 0.15%.

Fig. 6.19 Half-bridge test setup.

Table 6.2 Average Power Consumption of the Analog Sub-circuits in One Clock Cycle

Analog Subcircuits	Power (μW)
Voltage Reference and LDO	9.36
Test Bridge	5.2
Switched-Capacitor Amplifier	7.1
Dropout Voltage Loss	2.46
Total Power	24.12

Fig. 6.20 Transient response of the output voltage of the sensor interface.

6.4.2. Pressure Measurement

To validate the functionality of the sensor interface, a Honeywell full Wheatstone bridge pressure sensor NSCDANN030PGUNV [68] is coupled to the interface to monitor the pressure in a tank. Besides, a compressor plus vacuum pump is used to inject and drain the air from this pressure tank. At the same time, a pressure gauge, GZ46-K2K-01M, manufactured by SMC Pneumatic, is employed to take the pressure readings. The commercial sensor output and the interface output corresponding to a given pressure are measured and shown in Fig. 6.21. The commercial sensor displays a sensitivity of 0.092mV/kPa while the interface indicates a sensitivity of 3.62mV/kPa, yielding a gain of about 40 which is close to the target design.

Fig. 6.21 DC transfer characteristic of the proposed switched-capacitor amplifier.

6.5. *Performance Comparison*

Table 6.3 compares the measured results of proposed SC interface with other reported core interface circuits. For average power consumption of each interface, it includes the analog front-end interface's power and the sensor power, which is calculated based on the assumption of identical $10\text{k}\Omega$ bridge resistance at a constant supply. The performance of the SC amplifiers is evaluated by the FOM_1 and FOM_2 pertaining to the energy-noise efficiency. The FOM_1 is defined as

Fig. 6.22 Measured (a) sensor interface output, and (b) commercial sensor output versus applied pressure.

$$FOM_1 = Power \times T_{Measurement} \times (SNR)^{-1} \quad (6.22)$$

while FOM_2 is defined as

$$FOM_2 = Power \times T_{Measurement} \times (SNR)^{-2} \quad (6.23)$$

where $T_{measurement}$ is the measurement time required and SNR= signal-to-noise ratio in value. FOM_1 is similar to the Walden FOM [51], while FOM_2 is similar

to thermal FOM [52]. Compared with [13], [14], [18], and [15], the proposed circuit shows the best FOM₁ and FOM₂ due to its low power consumption and good resolution. Although [69] is having better FOM₁ and FOM₂ than the proposed work, the input $\Delta R/R_0$ range of the Wheatstone Bridge required is relatively large compared to that of conventional Wheatstone Bridge pressure sensor. Since different sensor interfaces use sensor with different range of resistive change as their input signal parameters, it is apparent that larger range of resistive change is easy to be detected by the sensor interface. To take this issue into account, we propose the normalized FOMn₁ and FOMn₂ on the basis of identical fractional resistance change are proposed. They are given as

$$FOMn_1 = Power \times T_{Measurement} \times \left[\frac{SNR}{(\Delta R / R_0)_{\max} - (\Delta R / R_0)_{\min}} \right]^{-1} \quad (6.24)$$

$$FOMn_2 = Power \times T_{Measurement} \times \left[\frac{SNR}{(\Delta R / R_0)_{\max} - (\Delta R / R_0)_{\min}} \right]^{-2} \quad (6.25)$$

where $(\Delta R/R_0)_{\max}$ is the maximum bridge imbalance of the respective sensor interface and $(\Delta R/R_0)_{\min}$ is the minimum bridge imbalance of the respective sensor interface. Compared to other representative sensor interfaces, the proposed work has achieved the best FOMn₁ and FOMn₂ due to its intrinsic low noise and low energy attributes. The FOMs difference are visualized in Fig. 6.23.

Fig. 6.23 $FOMn_1$ and $FOMn_2$ of the sensor interfaces compared to the other representative works.

Table 6.3 Comparison of the Proposed Work with the Other Discrete-Time
Sensor Interfaces

Parameter	JSSC 1998 [13]	JSSC 2002 [14]	TCAS I 2004 [15]	JSSC 2013 [69]	Sens. J. 2014 [18]	This Work
CMOS Technology	2 μ m BiCMOS	0.7 μ m CMOS	0.5 μ m CMOS	0.13 μ m CMOS	90 nm CMOS	65 nm CMOS
Supply Voltage (V)	3	3	2.5	1	1	1
$\Delta R/R_0$(%)	± 0.0967	–	–	± 10	± 1.28	± 0.938
CMRR at DC (dB)	>70	–	>110	–	–	>97.5
PSRR (dB)	–	–	102	52	–	64
Input Referred RMS (μV)	21.2	8.8	45	–	–	11
SNR(dB)	39.7	67.64 [†]	51.88 [†]	64.44 [*]	44 [*]	55.64
Ave. Power (μW)	38	759	465	224.5 [*]	101.3	12.3
Meas. Time (ms)	1	0.5	0.05	0.05	0.0376	0.5
Energy per measurement interval (nJ)	38	379.5	23.2	11.2	3.81	6.15
FOM₁ (pJ)	393.4	157.4	59.2	6.7	23.8	10.2
FOM₂(fJ)	4072	65	151	4	149	16.8
FOMn₁ (pJ)	0.760	3.149	1.18	1.35	0.609	0.19
FOMn₂ (aJ)	15.22	26.12	60.3	161.5	97.5	5.9

Chapter 7

Layout Consideration and PCB Design

7.1. *Layout*

In integrated circuit design, layout design is a crucial part. The layout of an analog circuit needs to provide good matching for the critical transistors, resistors and capacitors, while ensuring little voltage drop due to wiring resistance and reduced influence from cross talk effect. This section will discuss the common layout techniques pertaining to matching, low noise issue, power line distribution and floor planning.

7.1.1. **Matching**

To understand how to match the passive and active devices, one must have a grasp of the mismatch source. The sources of mismatch for resistors and capacitors [48] are

- (i) Random variation – Microscopic irregularities at the edges of the devices and throughout the devices [70]–[72].
- (ii) Process biases – geometries mismatch due to process such as etching, photolithography and implantation [73].
- (iii) Interconnect parasitics – systematic mismatch introduced due to parasitic resistance and capacitance of the wire routing [74].
- (iv) Etch rate variation – etching rate of the polysilicon resistors and poly-poly capacitor are higher at sides that facing towards larger opening.
- (v) Photolithographic effects – Optical interference occurs when light passing through slits due to regular structure of the integrated circuit or

narrow features during photolithography. Sidewall reflection also contributes to mismatch issue [75].

- (vi) Diffusion interaction – Diffusion interaction between the contact region and the resistor may cause the resistance to vary systematically [76].
- (vii) Hydrogenation – Hydrogen introduced during deposition and etching of metals will affect the value of poly resistors [77].
- (viii) Mechanical stress – The resistance of the poly-resistor and diffusion resistor will change due to mechanical stress induced by packaging due to the piezoresistive nature of the silicon and silicon device stress in CMOS technologies [78].
- (ix) Temperature gradient – Temperature difference across the die will also causes mismatch between different devices [79].
- (x) Thermoelectric effect – The contact potential of metal and silicon junctions are highly temperature dependent. If the end of the resistor segment has different temperatures, a voltage difference will be generated across the resistor.
- (xi) Electrostatic interaction – the value of resistor and capacitor can be influenced by the electrostatic fields. For resistors, electron will occasionally be injected into the interface between the overcoat and the interlevel oxide, thus creating electrostatic field and causing the variation. For capacitors, if the capacitor is charged abruptly, the dielectric might polarize and reducing the electric field intensity, thus reducing the capacitance [80].

The sources for MOSFET mismatch are

- i. Geometries – The threshold mismatch is inversely proportional to the effective active gate area of the MOSFET. With short-channel transistors, the matching will also be poor due to channel length modulation. The orientation of the MOSFET will also influence the matching as the transconductance of MOSFET depends on carrier mobilities. It has different sensitivities to stress of different orientations [81], [82].
- ii. Oxide thickness – MOSFET with thin oxide possess better matching characteristic than MOSFET with thick oxide.
- iii. Diffusion and etch effects – Like poly-resistor, the gate of MOSFET also suffers from etch rate variation due to large opening. This causes variation in gate length, thus causing mismatch. An example for the diffusion effect is that the N-well dopant intersects the channel of the PMOS transistor, causing threshold and transconductance variation.
- iv. Well proximity effect – When the N-well edge is too close to the MOSFET, ions might scatter and dope the adjacent uncovered silicon, thus causing threshold variation [83].
- v. Contact over active gate – Significant threshold variation is found to be induced by placement of contact over active gate area.
- vi. Hydrogenation – Hydrogenation is used to reduce threshold variation, however, if metal geometries impedes the hydrogen redistribution, the matching will suffer from the effect.
- vii. Thermal and stress effect – The threshold and the mobility of the MOSFET are temperature dependent, thus the existence of thermal

mismatch will cause mismatch in MOSFET. Different stress in transistors will cause mismatch in transconductance due to different electron mobilities exhibited by the transistors [84].

7.1.1.1. General matching methods and rules

In this section, the general matching methods and rules are discussed.

They can be summarized into two main categories:

- (i) Common-centroid layout
- (ii) Addition of dummies

Besides, other common layout considerations are also discussed.

7.1.1.1.1. Common-centroid layout[48], [85]

To combat stress gradient and thermal gradient, devices similar in properties such as differential input pair and current mirror are needed to be matched. The most common layout strategy for matching of critical device is the common-centroid layout. With common centroid layout, the centroid of the two matched devices will coincide with each other. Fig. 7.1 (a) shows a common-centroid layout. The centroids of red and blue devices are overlapped with each other, as marked by the magenta cross. This type of one-dimension common-centroid layout is called interdigitation layout. In Fig. 7.1 (b), as the centroids of the blue and red devices, marked by blue and red cross, are not coinciding with each other, it is not regarded as a common-centroid layout. As the centroids are not coinciding with each other, this layout pattern is susceptible to stress and temperature gradient.

Fig. 7.1(a) Common centroid layout (b) Example of incorrect common-centroid layout

For a good common centroid layout, the following rules of thumb are as follows:

- i. Coincidence – The centroid of the matched devices should exactly coincide.
- ii. Symmetry – The array pattern should exhibit symmetry around X and Y axes.
- iii. Dispersion – The unit elements should be uniformly distributed throughout the array.
- iv. Compactness – The array should be very compact and ideally square.
- v. Orientation – The unit elements for the MOSFET should have same orientation.

The common-centroid also applies to 2-dimensional array. 2-dimensional array layout are normally superior to 1-dimensional array because it provides better compactness and dispersion. Fig. 7.2 shows a few examples of 2 devices matching and 3 devices matching in common-centroid layout patterns.

Fig. 7.2 Examples of common-centroid layout patterns.

7.1.1.1.2. Addition of dummy

To ensure uniform etching for poly-resistor, poly-capacitor and MOSFET, dummies are needed to be added. By adding dummy transistor, the opening seen by each unit element are the same. This ensures similar etching rate. All dummies should be connected to ground whenever possible so as to prevent electrostatic charge accumulation, which will in turn alter the matching characteristics of the devices. Fig. 7.3 shows some examples of dummies addition to the resistors, poly-capacitors and transistors, where the dummies are highlighted in grey. If area is of concern, smaller dummies can be used to reduce the etching rate variations. For metal capacitors, dummy capacitors served as electrostatic shield This eliminates non-ideal effect caused by external fringing field.

Fig. 7.3 Examples of dummies addition for (a) resistor matching (b) poly-capacitor matching (c) transistor matching.

For capacitor, instead of using full dummies as etching and electrostatic field shield, dummies of smaller size or metal and polysilicon traces can be used to reduce the impact of etching and fringing field effect. Fig. 7.4 shows the examples of dummies addition by metal traces and dummy capacitors. All of the dummies should be connected to ground which serves as electrostatic shield. Using metal traces as dummies is comparatively better than using dummy capacitors due to smaller area. Besides, by using metal traces as dummies, fringing field shielding between matched capacitors can be done in a compact fashion.

Fig. 7.4 Metal-oxide-metal with (a) metal traces as dummies (b) small size capacitor as dummies, with dummies highlighted in grey.

7.1.1.1.3. Additional common layout rules

Additional common layout rules are listed below:

- i. Use identical unit size for matching – Different in unit size for resistors, capacitors and transistors will lead to poor matching.
- ii. Use large geometry devices – Devices with larger geometry is less susceptible to random fluctuation
- iii. Place matched devices in close proximity and as compact as possible–
 As resistors and transistors are sensitive to temperature and stress gradient, the shorter the distance between matched resistors or transistors the better matching result can be obtained. Although capacitor is much less sensitive with respect to temperature and stress

variation, placing matched capacitors in close proximity will improve matching between capacitors.

- iv. Place devices in areas with low stress gradient and away from power devices – As stated in (iii), matched device should be placed away from die areas with abrupt change in stress, which are typically at the die's corners [86]. Matched device should also be placed away from die areas with abrupt change in temperature gradient.
- v. Avoid routing traces over matched devices – Leads will introduce electrostatic interference, stress and hydrogenation issues. As such leads should not be routed over matched devices.

7.1.1.2. Additional resistor matching rules

- i. Use section resistor instead of serpentine resistor – Sectioned resistors are able to distribute more evenly compared to serpentine resistor.
- ii. Unit elements for each device in matched arrayed resistors should be of even number, and should be connected in square zig-zag fashion – With square zig-zag and even number of unit elements, the thermoelectric effect can be cancelled out.
- iii. Use separate tank for precisely matched resistors – Resistors with separate tank can match better due to elimination of tank modulation effect.
- iv. Use poly-resistor instead of diffusion resistor whenever possible – poly-resistors can be made much narrower than that of diffusion resistors, thus reducing area.

7.1.1.3. Additional capacitor matching rules

- i. Use square geometries for precision matching – As peripheral variation is one of the main sources of mismatch for capacitor, minimizing the peripheral length is important. As square geometry has the smallest periphery-to-area ratio, precision capacitor matching should always base on square geometry.
- ii. Connect upper electrode to higher impedance node – As lower electrode is closer to substrate, it is more susceptible to substrate noise and having higher parasitic capacitance. By connecting lower plate to low impedance, substrate noise coupling effect can be reduced.
- iii. Matched capacitor shielding – Shielding can contain fringing field and prevent electrostatic field from adjacent circuit from interfering with the matched capacitor array.
- iv. Use of cross-couple layout - Due to the square dimension of matched capacitor, matched capacitor devices can be arranged into cross-couple layout to form a compact square.
- v. For varactor, thick-oxide dielectric is better than thin-oxide dielectric – This is due to thick-oxide dielectric capacitors has less dimensional variation in comparison to thin-oxide dielectric capacitor.

7.1.1.4. Additional MOSFET matching rules

- i. For voltage matching, use large W/L while for current matching use small W/L – The offset voltage of a matched op-amp input transistor pair is inversely proportional to its transconductance for a given current. For current matching, it is dependent on threshold voltage. Therefore, larger V_{GS} minimizes impact of current mismatch due to threshold voltage

mismatch. Detailed discussion on influence of transistor sizing on mismatch effect is discussed in [87].

- ii. Thin-oxide devices are preferred over thick-oxide devices – Transistors with thin gate oxide generally have better matching characteristic over transistors with thick gate oxide.
- iii. No contact over active gate area – Placement of contact on active gate area sometimes causes significant threshold mismatch.
- iv. Keep all N-well and deep N-well far away from active gate area – This is to prevent the diffusion or scattering of N-Well dopant from influencing transistors' device characteristic
- v. Connect gate finger of matched transistors with metal traces – For precisely matched transistors, the gate finger should be connected by metal traces instead of polysilicon.

7.1.2. Low Noise Layout Techniques

Without taking into account of the parasitic effect during the layout phase, the signal-to-noise ratio may be greatly degraded by the coupling effect between a noisy source and a high impedance sensitive node. Therefore, in this section, the layout techniques employed to reduce the parasitic induced noise are discussed. They are given as follows:

- (i) Substrate noise reduction techniques
- (ii) Shielding for metal traces
- (iii) Power line distribution and floor planning

7.1.2.1. Substrate noise reduction techniques

In modern integrated circuit, it is unavoidable that the analog blocks and digital or switching blocks are integrated in the same chip. As all current injected into substrate will cause substrate noise, this presents a challenging issue for the mixed-signal integrated circuit. The causes of the substrate noise in mixed-signal ICs are mainly due to digital supply noise and the switching noise coupling from drain and source [88]. During switching instance of digital circuit, there often exists a short interval of on time for both NMOS and PMOS transistors, a large current will be drawn from the power supply to ground. Due to the non-zero resistance and inductance of the wire traces, this often creates voltage spikes and ringing on the supply rail and ground rail. As the substrate is connected to the power supply rail or ground rail, the substrate will also experience voltage spike and ringing. During the switching instance, as there are parasitic capacitances between source/drain and the substrate, the high frequency component of the switching signal will be coupled into substrate, leading to the substrate noise.

To reduce effect of the substrate noise caused by the digital block, a guard ring can be used to provide a low impedance path for the substrate noise. This keeps the substrate inside the guarding reasonably quiet. Highly sensitive blocks should always be surrounded by a guard ring. An example of the guard ring is shown in Fig. 7.5, where the analog block is surrounded by one P-substrate guard ring and one N-well guard ring [89].

Fig. 7.5 An example of guard ring for substrate noise reduction, where white area represents the P-substrate and grey area represents N-well.

An alternative to reduce substrate noise is to place devices in separate body for digital circuit and analog circuit. For PMOS transistors, this can be achieved by simply placing the PMOS transistors in separate N-well. For NMOS transistors, deep N-well can be used to isolate circuit blocks to prevent the switching noise from digital blocks interfering with the analog blocks [90], [91].

7.1.2.2. Shielding for metal traces[92]

Capacitive coupling is normally of concern between the noisy digital metal traces and sensitive analog metal traces. The sensitive analog signal is normally located at the input of circuits that possess high gain or any high impedance node in analog circuit, or nodes with low level signal. Hence, metal traces with sensitive signals should have the shortest length possible to reduce the chance of noise coupling. This can be done by placing the sensitive analog

blocks as close to the bond pad as possible. If situation arises such that it is unavoidable to run the metal traces with sensitive signals over or alongside noisy metal traces, shielding metal traces ought to be inserted between them. The shield should connect to low impedance quiet node, ideally quiet ground. Fig. 7.6 shows an example of sensitive metal trace shielding. Sensitive signal can also be routed through top metal layer in order to increase its distance with the substrate and noisy metal traces, thus reducing the parasitic capacitance with substrate and noisy metal traces.

Fig. 7.6 Shielding of sensitive metal trace with ground.

7.1.2.3. Power line distribution and floor planning

If digital power supply and analog power supply are using the same pad, digital switching noise will be coupled to analog supply unavoidably. This is mainly due to the non-zero resistance and inductance of the metal traces. Fig. 7.7 is used to illustrate this issue. In Fig. 7.7 (a), assuming that the PCB and PAD resistance are both 1Ω , and the power supply line for the digital and analog blocks are shared along the way, during the switching instance 10mA can be drawn by digital supply. This in turn causes a voltage drop of 70mV due to parasitic resistance on analog supply. To reduce this effect, Kelvin (star) connection should be adopted by separating the supply for digital and analog blocks on the pad or when coming out from the pad. Fig. 7.7 illustrate how Kelvin connection at the pad is arranged. During switching instance, a current of 10mA is drawn by the digital supply. As analog supply and digital supply are

separated at the pad, analog supply will only suffer from a voltage drop of 20mV, instead of 70mV.

Fig. 7.7 Power supply routing with (a) shared supply between analog and digital power supply (b) Kelvin (star) connection to reduce impact of digital switching on analog power supply.

For the floor planning, some fundamental issues are taken into consideration.

They are

- i. Stress gradient of die.
- ii. Location of power management devices.
- iii. Location of analog and digital blocks.

For a die, the stress at the corner of die usually is of the highest intensity and experience highest rate of change. Thus, devices that need to be matched are advice to be located at the center of the die. If it is not possible due to

routing, matched device should be placed at the center of the edge. As power devices will usually draw large current, they should be located very close to the pad. The power devices should be located away from the analog block because the heat generated might alter device characteristic of the analog blocks. Digital blocks with frequent switching activities should always be placed far away from the sensitive analog block such as input of analog block. A suggested layout for the floor planning of power management unit, analog blocks and digital blocks are illustrated in Fig. 7.8.

Fig. 7.8 Suggested floor planning, with grey area representing pad ring.

7.2. PCB Design [93], [94]

PCB design is another important step in obtaining good circuit performance. With improper PCB layout, circuit performance may suffer from significant degradation arising from ground bounce, coupling effect and parasitic effect.

To design a low noise PCB, good floor planning is the key. PCB layout similar to Fig. 7.8 can be used. In fact, many PCB wire routing considerations are similar to that of the IC layout, such as shielding of wire and routing differential wire close together. A PCB with at least four layers is preferred for

low noise circuit. Of particular noted, the internal layers should serve as supply layer and ground layer. This enables the parasitic capacitor to form between the ground plane and supply plane. As a result, it serves as a decoupling capacitor to reduce the supply ripple. Multiple parallel decoupling capacitors with large to small values should be inserted between supply and ground in order to decouple the supply and reduce supply ripple [95], [96]. Multiple parallel capacitors are needed due to the fact that the capacitor acts like an inductor once the capacitor passes the self-resonance frequency. Lowest value capacitor should be placed as close as possible to the IC in order to minimize the parasitic resistance and inductance. For trace routing, right angle bend should be avoided due to the radiation it emits [93], [97]. High switching trace should not be placed alongside sensitive metal trace. To minimize the potential cross-talk issues, distance between traces should be at least 2-3 times the width of the traces. Traces should not be routed across a ground plane gap. This will cause a large return loop.

Chapter 8

Conclusions and Future Works

8.1. *Conclusions*

This thesis has presented a current-to-frequency converter, a voltage-to-frequency converter and a switched-capacitor interface circuit for resistive bridge sensor applications. The resistive sensor type and operating principles has been described in this thesis. As the resistive sensor often have an output voltage of about 20 mV, the sensor interface needs to possess low noise characteristic to avoid the degradation of signal-to-noise ratio.

To interface with microcontroller, quasi-digital circuit such as current-to-frequency converters and voltage-to-frequency converters are preferable if a simple interfacing protocol is desired. This is mainly because the frequency of the signal can be converted to digital domain easily through simple counters. A review of the current-to-frequency converter and voltage-to-frequency converter has been conducted. Four representative quasi-digital converters have been investigated and their operating principle are described.

A current-to-frequency converter has been presented in this work. With a stable voltage supply and a voltage reference, the current-to-frequency converter can convert the resistance change of a single resistive sensor or Wheatstone Bridge resistive sensors into frequency. Based on a simple single op-amp transconductor, the sensor interface is able to achieve low power high-resolution conversion, leading to low energy-noise performance. Moreover, the proposed circuit architecture eliminates the use of current mirror. As such, it further reduces the error sources and makes it less susceptible to process

variation. Analysis has been done on the error sources of interface and ways to reduce the impact of the process variation have been discussed.

To further improve on the energy-noise product and to remove the output frequency dependency on the input bridge resistance, a simple voltage-to-frequency converter with a hybrid transconductor was proposed. This transconductor of the converter utilized a simple level shifted flipped voltage follower and a folded shunt feedback follower to convert the input voltage into current. As it does not use multiple op-amp topology to convert voltage into current, the power required is thus reduced. With this proposed work, the simulation results of the voltage-to-frequency converter have shown that it has the capability to achieve very good FOMs with respect to other representative works. Analysis also has been done on the voltage-to-current conversion to provide insight on the small-signal parameters that can influence the precision of the VI converter.

As resistive sensors often consume high current, reducing the on-time of the resistive sensors becomes the utmost concern while designing low energy-noise sensor system. Switched-capacitor interface is particular suitable for this application as it can sample the sensor signal for a short interval. After which, the sensor signal can be turned off whereas the switched-capacitor interface can process the signal during this time period, thus significantly reducing the sensor power consumption. In view of this key merit, a switched-capacitor interface is proposed in this work. This interface has achieved best FOMs when compared to that of counterparts due to the proposed dual-mode circuit operation. This dual-mode circuit operation enables the op-amp to operate in low bandwidth low power mode during the hold period to reduce the op-amp power

consumption. Moreover, this switched-capacitor interface adopts a level shifted design, thus eliminating the need of analog ground circuit without significant increasing the power consumption. Due to the employment of these techniques, the sensor interface is able to achieve the best FOMs in comparison to other representative reported works. Analysis has been conducted on the bandwidth required by the op-amp to achieve the desired resolution. The impact of gain error due to the finite open-loop gain has been studied. It provides an estimation on the open-loop gain required to achieve the required resolution at DC operation.

8.2. *Future works*

Although the quasi-digital interfaces together with the switched-capacitor interface have demonstrated excellent FOMs when compared to their counterparts, further research and implementation can be done to improve their performances.

8.2.1. **Quasi-digital Interfaces**

To improve the performance stability of the IF and VF converters across temperature and process variations, the offset of the input stage should be compensated. At the tradeoff of complexity, this can be achieved through ping-pong structure based auto-zeroing topology [98] as depicted in Fig. 8.1. The maximum residual offset for the input stage after offset cancellation is about $\pm 20\mu\text{V}$ for an input offset of $\pm 10\text{mV}$.

Fig. 8.1 Ping-pong auto-zeroing for input stage offset cancellation.[98]

To cancel the offset of the comparator and reduce the delay caused by discharging the capacitor, the relaxation oscillator shown in Fig. 8.2 is based on [99]. As the capacitors are alternately discharged, there is no dead time arising from the discharging process, thus reducing the overall delay. As seen in Fig. 8.3, compared to the other relaxation oscillator type, this relaxation oscillator only incurs the minimum amount of delay. Thus, the linearity of the system can be improved. To cancel the offset voltage of the comparator, the chopping action can be employed for the comparator. As illustrated from the simulated results shown in Fig. 8.4, the output frequency does not change despite there exists an offset voltage in the comparator.

Fig. 8.2 Improved relaxation oscillator based on [99]

Fig. 8.3 Sketch of output voltage and integrating capacitor voltage for relaxation oscillator with (a) window comparator, (b) single comparator with single C_{INT} , and (c) single comparator with dual C_{INT}

Fig. 8.4 Output waveforms of the relaxation oscillator under various comparator's offset voltages.

Additional future improvement includes:

- i. Devising the methods of converting the quasi-digital to digital codes in order to achieve better signal-to-noise ratio.
- ii. Devising digital temperature compensation for the bridge sensor.

8.2.2. Switched-capacitor Interface

To reduce the start-up time, the inputs of the op-amp during the start-up phase can be shorted to ground during the first Φ_I phase. Fig. 8.5 shows the improved output waveform in the sensor interface output. With the inputs shorted to ground, the switched-capacitor amplifier can reach its steady-state value in 3 cycles instead of 4 cycles.

Fig. 8.5 Simulated output of the switched-capacitor with improved start-up sequence.

Apart from improving the start-up time, a low-power, low temperature coefficient and high accuracy voltage reference dedicated to the switched-capacitor amplifier is also required. This is because the DC output of the amplifier is dependent on the performance of voltage reference. Since the signal-to-noise ratio of the system is also dependent on the analog-to-digital converter (ADC), a low energy-noise SAR ADC is therefore needed to convert the output signal of sensor interface into digital domain. The ADC architectures [100] and [101] fulfill this criteria and can be readily implemented. Low jitter oscillator is vital in a sample system as jittering will cause sampling error [102]. Therefore, a low jitter on-chip oscillator becomes an important topic for SoC sensing system when high resolution is demanded.

Author's Publications

Journal papers

1. **K. C. Koay** and P. K. Chan, "A low-power resistance-to-frequency converter circuit with wide frequency range," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 12, pp. 3173–3182, Dec. 2015.
2. **K. C. Koay** and P. K. Chan, "A low energy-noise 65nm CMOS switched-capacitor resistive-bridge sensor interface," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 64, no. 4, pp. 799–810, Apr. 2017.

Conference paper

1. **K. C. Koay** and P. K. Chan, "A 1V low-power CMOS resistance-to-frequency converter using hybrid transconductor for IoT," in *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2016, pp. 73–76.
2. Y. Li, **K. C. Koay**, and P. K. Chan, "A 65nm CMOS ping-pong auto-zero resistance-to-frequency converter for resistive bridge sensors," in *International Symposium on Integrated Circuits*, 2016, pp. 1–4.

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