Low-voltage aging-tolerant sram designs

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LOW-VOLTAGE AGING-TOLERANT SRAM DESIGNS

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2018

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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ABSTRACT

The sub-threshold or near-threshold operation has been an attractive option for digital integrated circuit design due to the explosive growth of battery operated devices. This approach utilizes ultra-low/low supply voltage to decrease switching energy and suppressing leakage current to achieve low power operation. The effectiveness of power reduction makes it an excellent approach to prolong the battery lifetime and create an alternative opportunity for healthcare monitoring devices, which have limited power budget and low to medium signal processing capability. Static Random Access Memory (SRAM) is known as the critical building block in digital very large-scale integration (VLSI) circuit. It consumes large area overhead with high integration density in the modern System on Chip (SoC). This causes a large amount of leakage power contributed from SRAM array and is recognized as one of the bottlenecks in sub-100nm technologies. Therefore, application-specifically designed SRAMs for low power signal processing SoC have been popular and necessary. A column based split cell-VSS (CS-CVSS) data-aware write-assisted 9T SRAM with enhanced read sensing margin is developed. The CS-CVSS data-aware write assist improve both half-selected static noise margin and write margin while a 3T read port structure is applied for read sensing margin improvement. A 16kb 9T SRAM test chip with the proposed techniques is fabricated in 28-nm fully depleted silicon on insulator (FDSOI) technology and demonstrated $V_{DD,MIN-Write} = 470\text{mV}$ and $V_{DD,MIN-Read} = 250\text{mV}$.

Apart from suffering large leakage power consumption, SRAM reliability is another limiting factor in sub-100nm technology due to temporal variations. Temporal variations such as Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) shift the device threshold voltage (V_{th}) over its functional periods and eventually lead to soft or hard

failures. In particular, BTI has been recognized as the most critical and challenging temporal variation that limits the lifetime of SRAMs much worse than HCI. The critical SRAM operation margins include minimum operating voltage, V_{min} , cell stability and read/write stability. To circumvent the BTI aging in SRAMs, a dynamic reliability management that consists of BTI-Aware Stability Monitor (BTI-SM) assisted with Two-Phase Write Operation (TPWO) is proposed. The BTI-SM monitors the BTI degradation in SRAM cells through a replica row and adjusts the WWL voltage level with the assist of TPWO. The TPWO divides the write wordline (WWL) voltage level into two phases to improve the degraded half-selected cell stability due to BTI degradation without compromising other circuit parameters. Test chip measurement shows that the half-selected cell stability failure is reduced significantly from 57.13% down to 0% with the proposed techniques at a 10% area and 3.42% power overheads in 28-nm FDSOI 16kb SRAM.

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Chapter 1

Introduction and Motivation

1.1 Background

Moore's law is named after Intel co-founder Gordon E. Moore, who described in his 1965 paper that trend of the number of transistors on the integrated circuits that double approximately every two years, and predicted that the trend would continue for at least ten years [19]. Later, David House, an Intel executive at the time, who quoted the chip performance would double every 18 months based on the increase in performance of transistors [20]. History has shown a close relationship between Moore's law to the capabilities of many digital electronic devices such as processors speed, memory capacity, sensors, etc. All of these electronic devices are improving at exponential rates where Moore prediction has proven to be very uncannily accurate especially in the late 20th and 21st centuries, as the semiconductor industry has been using the law as a long-term target guideline for research and development. Figure 1.1 shows the number of transistors in a microprocessor from 1971 to 2011 [1]. The graph described the transistor count is doubling approximately every two years in the history.

Moore's prediction is realized through the steady shrinkage of transistor size. With technology advancement, more transistors can, therefore, be integrated into System on Chips (SoCs)/microprocessors due to the higher packing density. Other benefits achieved along with scaled technologies are higher processing speed and lower cost per transistor which are

essential for today's mass market consumer electronics. However, the exponential trends of scaling caused the minimum sized device and closely matched devices such as Static Random Access Memories (SRAMs) to suffer from Process, Voltage, and Temperature (PVT) variations due to the oxide thickness scaled close to 1-nm and transistor degradation due to aging. Therefore, yield issues have become increasingly important in deep sub-100nm process technologies [21].

SRAMs is a type of on-chip high speed memory, also known as the cache using bistable latching circuitry to store data. It has been widely used in SoCs and microprocessors to improve the performance and throughput. Figure 1.2 shows the size of the on-chip memory in a chip on different technologies. It shows strong evidence that the on-chip memory size is growing significantly with scaled technology. A study also predicted the SRAMs would dominate inside SoC products in the future [22]. This is mainly because of the modern processors have widely adopted on multicore architectures which demands on more on-chip memory.

Figure 1.2: On-die cache memory in a chip on different technologies [2].

1.2 SRAM Design Challenges and Limitations

As battery-powered electronic gadgets have become more common in modern century, extending the battery lifetime is one of the primary design concerns. Unfortunately, the leakage current of transistors increases significantly in advanced technology due to thinner gate oxide and shorter transistor channel length which further deteriorate the battery lifetime. Therefore, energy efficient or low voltage operation is introduced to reduce the total power. Achieving a robust low voltage operation in SRAM is very challenging because of the degraded read and write cell stability, poor bitline sensing, and increased sensitivity to PVT fluctuation in a voltage scaled environment. A study of the read cell stability and leakage current of a conventional 6T SRAM bitcell on different technology nodes is presented in Figure 1.3. It is evident that the read cell stability degrades with scaled technology while the leakage current is increasing. This trend is continuing beyond 32-nm technology node. Therefore, new SRAM bitcell structure with low leakage and improved cell stability is required.

Figure 1.3: Read cell stability and leakage current of 6T SRAM bitcell on different technology nodes [2].

Besides the requirement of new SRAM bitcell structure, the aging reliability issues such as Bias Temperature Instability (BTI) is another limiting factor on the SRAM design. BTI is characterized as the absolute positive shift in transistor threshold voltage $|V_{th}|$ over time. It occurs when the transistor is biased in strong inversion regime, and its lateral electric field (V_{DS}) is small or close to zero. Once the transistor is turned off, the increased $|V_{th}|$ will then recover to its initial value. However, the increased $|V_{th}|$ might not be fully recovered due to fast switching activity in the integrated circuit. Moreover, BTI not only depends on the supply voltage and temperature but also on other technology parameters of the transistor (i.e., the thickness of gate oxide). As a result, BTI degradation worsens with further scaling in technology. Since SRAMs use bistable circuitry to form the storage node, the BTI is unpreventable due to the static dc stress condition even when the SRAM is in the standby mode. This causes degradations on the SRAMs cell stability, read stability and minimum operating voltage (V_{min}) while the write margin improves with operation time.

Overall, the PVT fluctuation is firstly impacted the initially designed SRAM operating margin through changes the transistor characteristics and performance yield. Along with its operation cycles, the degraded SRAM operating margin further deteriorates by the BTI aging. In short, the PVT fluctuation is one time off that alters the transistor performance

while the BTI aging is a lifetime effect. The latter is identified as the worst issue that impacts the SRAM yield. As such, it is important to provide an on-chip BTI-aware circuit to ensure the SRAM functionality/yield over its operation cycle.

1.3 Contributions

This thesis focuses on the design of BTI-aware technique and ultra-low voltage SRAM. The BTI-aware technique used replica row in SRAM to monitor the half-selected cell stability due to BTI degradation and provide proper write wordline (WWL) voltage control based on the feedback loop from the BTI monitor to handle the BTI degradation as to ensure a robust cell operation. This technique can be employed into any SRAMs where reliability or robustness is a primary concern. Moreover, a 9T SRAM bitcell with enhanced read sensing is proposed to operate in ultra-low voltage regime. The following detailed contributions have been achieved:

- The impact of BTI degradation on SRAM cell is studied. The studies included the detailed analysis of read margin, write margin, and half-selected cell stability of SRAM under the BTI degradation.
- A conceptual implementation of the negative bias temperature instability (NBTI)/positive bias temperature instability (PBTI)-aware WWL voltage control circuit is proposed. The control circuits measure the time to data flip of the SRAM cells in the replica bitline and prevent data flip in the half-selected cells by adjusting the WWL level.
- A BTI-aware stability monitor and two-phase write operation for cell stability improvement is developed in 28-nm FDSOI. This proposed work provides an automated on-chip solution for BTI degradation to achieve dynamic reliability management. The test chip measurement results have proven a significant reduction in the half-selected cell failure with the presence of BTI effects in SRAM cell.
- A novel 9T cell structure with column-based split cell-VSS (CS-CVSS) data-aware

write-assisted scheme with enhanced read sensing margin is developed in 28-nm FD-SOI. The proposed data-aware write-assisted scheme controls the CVSS1 and CVSS2 voltage of SRAM bitcell in the selected column during the write operation to improve the write margin and enhances the half-selected static noise margin (HS-SNM) to prevent data loss in the half-selected cell due to unwanted write disturbance. The decoupled read port also shows a much better read sensing margin compare to the conventional 8T cell structure.

1.4 Organization

This thesis is organized as follows. Chapter 1 introduces the background knowledge of the SRAM design limitations and challenges. It also includes the motivations for research into this area and shows the major contributions of this thesis.

Chapter 2 firstly introduces and reviews the common reliability issues and explains in more detail BTI degradation inside a MOSFET device. Based on the BTI degradation in SRAM cell, a study has been conducted on the SRAMs read and write operation. Furthermore, a conceptual implementation of NBTI/PBTI-aware WWL voltage control circuit is proposed to prevent data flip in the half-selected cells by adjusting the WWL level after BTI degradation.

Chapter 3 presents a proposed BTI-aware stability monitor and two-phase write operation for cell stability improvement. The proposed technique is fabricated in 28-nm FDSOI technology. The chapter starts with the review of SRAM circuit solutions on the BTI degradation in the literature. After that, a detailed discussion on the proposed technique on BTI-aware stability monitor and two-phase write operation to achieve dynamic reliability management is in the subsequent subchapter. The test chip measurement results are discussed in the subchapter.

Chapter 4 presents a novel 9T cell structure with CS-CVSS data-aware write-assisted scheme with enhanced read sensing margin. The proposed technique is fabricated in 28-nm FDSOI technology. The chapter begins with a more specific review of various low volt-

age SRAM cells and assist techniques available in the literature. A dedicated subchapter discusses the proposed 9T cell structure, CS-CVSS data-aware write-assisted scheme, and read sensing enhancement based on the 9T cell structure. The test chip measurement results are discussed in the subchapter.

Chapter 5 shows the summary of my research throughout the Ph.D. program. Future works will also be discussed in this chapter.

Chapter 2

NBTI/PBTI-Aware WWL Voltage

Control for Half-Selected Cell Stability

Improvement

2.1 Background

NBTI in PMOS and PBTI in NMOS is a well-recognized primary aging reliability concern in SRAMs especially when it coupled with process variation [23–26]. It is characterized by a positive shift of device threshold voltage in absolute value. Since SRAM cells are constructed with bistable latching circuitry to store data ‘1’ and ‘0’, the NBTI and PBTI are unpreventable due to the static dc stress condition even when the SRAM is in the standby mode which will be discussed in the later chapter. This causes the degradation of the SRAMs cell stability, read stability and V_{min} while the write margin improves with operation time. The SRAM cells will experience data flip once the degradation is large enough to generate the flip. Therefore, SRAM’s operating voltage needs to be raised above V_{min} to compensate for the degraded parameters. However, this is undesirable for ultra-low power applications where the energy consumption is a priority concern. Therefore, a newly proposed circuit technique to address the issues is presented in this chapter. The proposed technique utilizes WWL voltage control to compensate the degraded stability of the half-

selected cells without much affecting other design parameters in a conventional 8T SRAM structure.

2.2 Motivation

Reliability is always the critical design issue in the state-of-the-art CMOS processes to ensure robust operation. The source of reliability issues can be categorized into three classes, namely, process variations, environmental variations, and aging variations. Process variations incur a drift in transistor parameters from their initially designed values along the process steps during chip fabrication. Environmental variations occur when there is a sudden change in operating conditions such as supply voltage and temperature changes when the circuit is in operation. Aging variations may lead to degradation in transistor parametric over time due to the presence of stress in prolonged operation.

Among these three source of variations, aging variations is the most prominent reliability issue for designing robust circuits. This is because the circuit operating margins are changing with respect to time due to the aged transistor. Consequently, it greatly shortens the functional circuit lifetime. According to the predicted data released by the International Technology Roadmap for Semiconductors (ITRS), there are 10-100 failures per million transistors for sub-100nm process technology nodes in 10^9 hours operation [27]. The failure rates continue to grow as device sizes shrinking aggressively to meet the demand for higher packaging density and enhanced performance.

Hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and BTI are the three common aging reliability issues. Figure 2.1(a) presents the occurrence of HCI, BTI, and TDDB effects in an inverter [3]. TDDB effect occurs when the device is operated close to its maximum specified operating voltage. It is worsened with advanced technology nodes because of aggressive scaling in gate oxide thickness. On the other hand, HCI effect occurs when the device switches from one state to the other (low-to-high or high-to-low) and the switching transistor is immediately subjected to BTI effect once switching is completed. This also implies that the impact of BTI on devices or circuits at standby

(a)

NBTI STRESS

(b)

NBTI Recovery

(c)

Figure 2.1: (a) Aging variations (HCI, BTI, and TDDb) in an inverter [3], (b) Illustration of NBTI stress in PMOS device, (c) Illustration of NBTI recovery in PMOS device.

condition.

NBTI in PMOS transistors is recognized as the major threat in modern and future process based on research and industrial data [28–35]. This effect is further exacerbated following the introduction of nitrogen into gate oxide to enhance the k -value [36]. When a PMOS transistor is biased in the strong inversion regime and its lateral electric field (V_{DS}) is small or close to zero, the interface traps are generated through the broken Si-H bond at the dielectric interface layer caused by the holes in the channel as shown in Figure 2.1(b). Consequently, this leads to an increase in the absolute value of PMOS threshold voltage $|V_{th}|$. This is typically known as the stress phase. Once the PMOS is turned off, it immediately enters into a recovery state, known as recovery phase. In the recovery phase, the freed hydrogen will diffuse back to the dielectric interface layer and anneal the broken Si-H bonds (Figure 2.1(c)). Thus, the original PMOS $|V_{th}|$ is recovered.

PBTI in NMOS transistor was not critical in mature technology because the shift in threshold voltage is negligible. However, the PBTI is now a growing threat after the introduction of the high- k metal gate in advanced technology nodes [9, 10, 37, 38]. Note that the effect of NBTI and PBTI degradation is even more aggravated in higher operating temperature. More importantly, the circuit techniques developed to suppress or mitigate NBTI could be the culprit in accelerating degradations due to PBTI effect. Therefore, there is a continuously growing research interest in analyzing, characterizing, and developing circuit solutions such as suppressing or mitigating the deleterious NBTI and PBTI effect [4, 5, 13, 14, 21, 33, 39–41].

In the past, NBTI/PBTI effect was measured by using the device probing approach [40, 42]. However, research and development works on the on-chip digital monitor circuits are increasing over years due to the need for simplistic test process and structures [4, 14, 21, 39, 43–46]. Furthermore, the device probing approach required an extensive measurement setup and is difficult in collecting statistical data under various test conditions [33].

In [4], an on-chip monitor for measuring frequency degradation of digital circuits due to BTI and HCI effect is reported. The reported idea utilized a technique called beat-frequency

detection scheme as shown in Figure 2.2. The technique consists of two free-running ring oscillators and a phase comparator. The reported scheme enabled the ring oscillators to operate under two phases, stress phase to accelerate NBTI degradation while measurement phase to measure the frequency degradation due to NBTI. During the stress phase, the supply voltage of the reference ring oscillator is connected to ground as to prevent device aging while the stress ring oscillator is raised to stress V_{DD} , which is higher than the nominal V_{DD} to accelerate the NBTI degradation. When the circuit is switching from stress to measurement phase, both ring oscillators will be operated in nominal V_{DD} for frequency degradation measurement. In such situation, the ring oscillator, which has been stressed earlier, is running at a lower frequency as compared to the reference ring oscillator due to NBTI degradation induced $|V_{th}|$ shift in PMOS transistor. The comparator will then output the frequency difference of the two ring oscillators, which is known as the beat frequency. A counter with its clock input is connected to the output of reference ring oscillator to measure the beat frequency. Thus, the counter's output N has a close relationship between reference and stress frequency as shown in the equation in Figure 2.2. The difference between N and N' is the counter output measurement before stress and after stress respectively. Therefore, the counter output N is directly proportional to the frequency degradation by using the equation. The complete test-chip architecture is shown in Figure 2.3.

Another compact in-situ sensor for monitoring NBTI effect and oxide degradation is reported in [5]. The reported idea utilized the current relation between the fresh PMOS and aged PMOS. Figure 2.4 shows the circuit schematic of the NBTI sensor. The circuit consists of a 15-stage NAND gate ring oscillator, stress/measure control circuit, a level converter, and devices under test PMOS transistors P1 and P0. As the NBTI effect causes an increase in threshold voltage of PMOS transistors, the current flows from PMOS transistor to ring oscillator decreases and eventually reduces the oscillation frequency. The author claimed that by operating the PMOS transistors P0 and P1 in subthreshold regime, the reported technique could detect a 53% change in oscillation frequency for 10% ΔV_{th} . However, the oscillation frequency sensitivity is increased with temperature. Therefore, the

Figure 2.2: Reported Beat-frequency detection circuit and its principle [4].

Figure 2.3: Reported silicon-odometer test chip architecture [4].

unstressed reference PMOS transistor P0 is used to correct the effects of temperature and process variation. The other identical PMOS transistor P1 is stressed at a negative voltage to accelerate the NBTI effect used for measurement.

Figure 2.4: Reported circuit schematic for NBTI sensor [5].

As discussed earlier, NBTI and PBTI degrades device's parametric with respect to stress time and eventually leads to circuit failure. Hence, it is required to design an aging tolerant circuit that allows either suppressing or mitigating the NBTI and PBTI degradation. In most cases, designers will optimize the device sizing or increased the operating voltage after the BTI degradation to prolong the circuit lifetime. However, all these methods are not suitable for SRAMs. In SRAM design, SRAM cells are designed in minimum sizing to increase the integration level, and thus, oversizing in SRAM cells are not preferable. Moreover, there will be an increase in the V_{min} over time to compensate the degraded SRAM stability due to BTI aging [47], which is highly undesirable in low-power systems where energy efficiency is often the most important design consideration especially in Ultra-Dynamic Voltage Scaling (UDVS) design [48]. In [49,50], the authors utilized a lower WWL voltage to improve the overall SRAM performance due to the process and temperature variations. However, these works did not address the BTI degradation, which degrades the operating margin of the SRAM over time. Therefore, the aging tolerant circuit must be integrated

along in SRAMs design.

2.3 Contributions

SRAM is a widely used embedded memory in SoCs or microprocessor. It usually consumes a large area in SoCs/microprocessor as described in Figure 2.5 [6]. The total relative area of SRAMs in a chip is expected to be increased with CMOS technology scaling. Figure 2.6 shows the predictive SRAM area will exceed 90% in the year 2014 [7,8]. The main reason that SRAMs have become dominant in a chip is that of the consumers demanding higher performance for faster processing speed. Therefore, the large SRAM area in a chip will strongly impact the cost and yield in the future process. Furthermore, the increase of process variation in advanced technology also strongly impacts the SRAM functionality in the low power application as shown in Figure 2.7. Hence, various design considerations such as the cell stability, read and write margins are of primary importance to IC designers. However, since reliability issues such as BTI, HCI, and TDDB further degrade transistors performance, the desired SRAM operating point will shift over its operating time.

Among these reliability issues, BTI is the most critical reliability issue in SRAMs due to the bistable latching circuitry. Therefore, it is also important to design a BTI-tolerant SRAM circuit which improves the SRAM stability and circuit lifetime for ultra-low power applications. In the following chapters, we examine and analyze the various impacts of NBTI and PBTI on 8T SRAM cells and propose an NBTI/PBTI-aware WWL voltage control circuit for half-selected cell stability improvement. All the simulation results in this work are based on 32-nm high-k/metal gate Predictive Transistor Model (PTM) with 256-bit-cells connected on each bitline. The PTM allows transistor's threshold voltage tuning to imitate the threshold voltage degradation due to NBTI and PBTI in NMOS and PMOS transistor respectively. As such, the notations of 'NBTI = PBTI' and 'NBTI & PBTI' in this chapter can be achieved through the PTM. Note that 'NBTI = PBTI' represented the same amount of threshold voltage shift due to NBTI and PBTI degradation on the SRAM cells (i.e., $|V_{thp}| = |V_{thn}|$), while the NMOS and PMOS threshold voltage degradation can

Figure 2.5: Embedded SRAM (caches) on a modern microprocessor [6].

Figure 2.6: SRAM and logic area vs technology scaling in modern SoCs and microprocessors [7, 8].

Figure 2.7: SRAM devices V_{th} variation scaling trend [8].

be different on ‘NBTI & PBTI’ notation.

2.3.1 Impact of NBTI and PBTI in 8T SRAM Cell

NBTI and PBTI are the two primary reliability concerns that alter the transistor characteristics in high-k/metal gate process technology. The aging effect not only increases the probability of circuit failures over its functional time, it also exacerbates when an SRAM is required to support UDVS with high temperature. Figure 2.8 shows an 8T SRAM cell inclusive of NBTI and PBTI with $Q = '1'$ and $QB = '0'$. Note that all the transistors in the cell are designed with minimum width and length ($MP1/MA1 = MN2/MA2$).

Under such storage condition in Figure 2.8, the NBTI and PBTI effect will arise in MP1 and MN2, respectively. In the other storage condition, the NBTI and PBTI aging will occur in MP2 and MN1 instead of MP1 and MN2. As a result, the BTI degradation is unavoidable in every single SRAM cell regardless of the data stored due to its unique cross-coupled inverters structure (MP1-MN1 and MP2-MN2). Therefore, the design parameters such as static noise margin (SNM), write ability, time to data flip, etc. are also varying over time from their initial designed values due to performance degradation in the transistors. The rest of this chapter will analyze and examine the BTI impact on SRAM.

Figure 2.8: Schematic of an 8T SRAM cell with NBTI and PBTI.

2.3.1.1 Static Noise Margin (SNM)

The gains of the cross-coupled inverters (MP1-MN1 and MP2-MN2) can be represented by the static noise voltage source V_n as shown in Figure 2.9. The static noise source is a disturbing dc noise such as offset, device V_{th} mismatch due to process variation, and as well as variations in operating conditions. The SNM is defined as the maximum noise voltage value V_n that the two cross-coupled inverters can tolerate before changing state [51]. In other words, the SNM is used to represent the SRAM cell stability. Therefore, SNM is always designed to ensure it can cover the worst-case operating scenarios such as dynamic disturbances, crosstalk, voltage supply ripple, and thermal noise for a robust SRAM.

For the ease of understanding and illustration, the SNM value is acquired through the maximum possible square formed by the two cross-coupled inverters characteristic curves. This is known as the graphical approach of measuring the SNM as illustrated in Figure 2.10(a) [51–53]. Figure 2.10(b) depicts the SNM of SRAM cell due to NBTI and PBTI degradation. In this case, the SNM is not even anymore, one of the SNM will be larger than the other. Thus, the smallest will determines the new SNM. As a result, the cell stability is degraded. If the SNM value continues to decrease due to NBTI and PBTI, the cell stability will become weaker and it will increase the probability of data loss. Once the SNM value drops below zero, the cell no longer holds the originally stored data as shown in

Figure 2.9: Schematic of static noise voltage source in SRAM cell.

Figure 2.10(c). Note that the Figure 2.10(a), 2.10(b), and 2.10(c) are without considering the process variation. In fact, the SNM value will become even smaller with the presence of the process variations.

2.3.1.2 Read Operation

On the onset of a read operation, read word line (RWL) of the selected row is held high and a virtual ground (VGND) is held at low based on input address. On this biasing condition, the selected pre-charged read bitline (RBL) is conditionally discharged depending on the stored data through the read access transistor (MR1) and dedicated NMOS read buffer (MR2). If a '0' is stored on QB node, the gate of MR2 is low. That means that there is no discharging path for RBL even when the MR1 is turned on. Hence, the RBL is maintained at high. In contrast, the RBL is discharged to low when a '1' is stored on QB node.

Assuming that the read delay of an 8T cell is defined by the time required to discharge RBL to 50% of VDD, it is obvious that the read delay is only affected by the PBTI in MR1 and MR2 in Figure 2.8. However, VGND is held at high and RWL is held at low during non-read operation, which eliminates PBTI in MR1 and MR2. This is true regardless of the value at QB. Since MR1 and MR2 are stressed only when RWL is held at high, VGND is

(a)

(b)

(c)

Figure 2.10: (a) The SNM of a SRAM cell, (b) The Impact of NBTI and PBTI degradation on SNM, (c) NBTI and PBTI degradation caused SNM below zero and eventually leads to data loss.

held at low, and QB is '1', the PBTI impact on MR1 and MR2 becomes negligible. Figure 2.11 shows the impact of NBTI and PBTI degradation on the read delay. It is proven that the read delay is independent of the stability degradation of the storage cell.

Furthermore, in a conventional 6T cell, a read operation can severely degrade the half-selected cells SNM on the selected row. This is known as read disturbance. It occurs when the disturbance current from bitline is flowing through the access transistor to the cell storage node. In this case, the disturbance current pulls the data '0' storage node above ground level and eventually data '1' storage node below V_{DD} level, which significantly degrades the cell SNM. For an 8T cell, however, the read disturbance has been fully eliminated. It is because the read bitline is isolated from the cell storage node. Thus, the SNM of the half-selected cell is equivalent to the two cross-coupled inverters.

Figure 2.11: Simulation of the impact of NBTI and PBTI on Read Delay based on 256-bit cells per bitline.

2.3.1.3 Write Operation

The write operation of an 8T cell is operated similarly to that of a 6T cell. In the write operation, a successful write is completed once the data on a bitline pair is written

into the selected SRAM cell. In Figure 2.8, if WBL and WBLB are loaded with '0' and '1' respectively, Q, whose original data is '1', will be discharged towards '0' through the access transistor MA1. Similarly, QB, which originally has '0', will be charged towards '1' through the access transistor MA2. Once Q is discharged below the trip-point of the inverter consisting of MP2 and MN2, the positive feedback of the cross-coupled inverters will kick-in and eventually pull QB to '1' and Q to '0'. This is known as SRAM write ability, which is often called as Write Margin (WM). It is defined as the highest bitline level to change the stored data.

The higher the WM is, the smaller the write delay and write failure rate also decreases. If WM decreases, write failure will increase, and data may not be written into the cell during the write cycle. Therefore, it is important to analyze the impact of NBTI and PBTI degradation on WM. Figure 2.12 presents the relation between WM and the threshold voltage shift due to NBTI and PBTI stress in MP1 and MN2 without considering the device mismatch. The result shows that both NBTI and PBTI stress improve WM over time. The WM can simply improve three times larger than the initial design value when the amount of NBTI and PBTI degradation induces 60mV threshold voltage shift in MP1 and MN2. This is because of the cross-coupled inverter trip point (MP1 and MN1) is lowered by NBTI while the PBTI stress weakens the transistor MN2 for maintaining data '1'. Therefore, it makes data flip easier. Note that the PBTI on access transistors MA1 and MA2 is negligible because they only experience PBTI stress when the cell is selected during the write cycle.

2.3.1.4 Half-Selected Cell Stability

Although read disturbance has been eliminated in 8T SRAM cell structure, however, write disturbance is still presented in the half-selected cells. The stability of 8T SRAM is mainly dominated by HS-SNM as reported in [54]. At the onset of the write operation, WWL turns on MA1 and MA2 in the entire cells on the selected row. Thus, the half-selected cells would experience the unwanted 6T read-like disturbance since their bitline pairs are pre-charged at V_{DD} . Consequently, the data stored in the half-selected cells can

Figure 2.12: Simulation of the impact of NBTI and PBTI degradation on Write Margin based on 256-bit cells per bitline.

Figure 2.13: Simulation of the impact of NBTI and PBTI degradation on HS-SNM based on 256-bit cells per bitline.

Figure 2.14: Simulation of the impact of NBTI and PBTI degradation on Time To Data Flip in galf-Selected Cells based on 256-bit cells per bitline.

be lost once the disturbance voltage exceeds the HS-SNM, which is the half-selected cell stability.

HS-SNM is the parameter measuring the stability of the half-selected cells. It can be defined as the highest disturbing voltage at the node storing data '0' that can flip the data during the write operation. The BTI stress lowers the trip point of an inverter and raises that of the other inverter, consequently degrading HS-SNM of the cell. Therefore, even if the amount of disturbance from WBL or WBLB is constant, the change in the inverters trip points increases the probability of data flip.

Figure 2.13 demonstrates the relationship between the circuit reliability (i.e., NBTI and PBTI) and the normalized cell stability. As expected, both NBTI and PBTI deteriorate the cell stability. Once the cell stability deteriorates, the half-selected error probability is increased. The SRAM lifetime is reduced correspondingly. Furthermore, the time to data flip in the half-selected cells become faster with BTI stress as illustrated in Figure 2.14. This is due to the degraded cell stability over time and subsequently fastens the data flip time. One typical solution to address the issue is to raise the supply voltage level

for compensating the degraded cell stability at the cost of additional power consumption, which is not acceptable in many power-constrained systems. Consequently, efficient circuit techniques are required to maintain the degraded design parameters with aging without sacrificing other design parameters such as power and performance.

2.3.2 Proposed NBTI/PBTI-Aware WWL Voltage Control Technique for Cell Stability Improvement

In this chapter, we propose an NBTI/PBTI-aware WWL voltage control technique for improving the degraded stability of the half-selected cells due to BTI stress. As explained in Figure 2.13, BTI stress degrades HS-SNM over time. Once the HS-SNM becomes zero or negative, the cell will lose its stored data. A typical way of improving the degraded HS-SNM is to raise the supply voltage. However, this consumes additional power.

Instead of raising supply voltage, the proposed circuit technique lowers the WWL voltage after BTI stress to improve the degraded cell stability (Figure 2.8). When lowering the WWL voltage level, the characteristic of access transistors has been weakened and eventually reduces the disturbance current flowing from the bitline pair (WBLB) to the storage cell (QB). Hence, the HS-SNM is improved accordingly. Figure 2.15 presents the impact of the NBTI and PBTI stress on the HS-SNM at different WWL voltages. As expected, the HS-SNM degrades as BTI stress increases at each WWL level. However, Figure 2.15 also shows evidence that a lower WWL voltage produces larger HS-SNM at a given NBTI and PBTI stress. This is the feature utilized in this work for stability improvement.

SNM is a pessimistic method of estimating SRAM cell stability. In a real situation, the successful operation can be attained even if the SNM is zero or negative. Therefore, dynamic parameters are preferred for accurate estimation. In this work, time to data flip in the half-selected SRAM cells is used as a parameter for stability estimation. Figure 2.16 summarizes the relation between the BTI stress and the time to data flip at various WWL voltage levels. The BTI stress decreases the time to data flip due to the exacerbated cell stability described in Figure 2.15. In addition, a lower WWL voltage level enlarges the data

Figure 2.15: Simulation of the impact of NBTI and PBTI degradation on HS-SNM with WWL voltage control based on 256-bit cells per bitline.

flip time at the same BTI stress, which is also corresponding to the result in Figure 2.15. This indicates that data flipping in the half-selected cells can be prevented by completing SRAM operation within the time to data flip.

Unlike the HS-SNM, lowering WWL level deteriorates the write margin due to the weakened strengths of the access transistors as demonstrated in Figure 2.17. On the other hand, BTI stress in an SRAM cell helps to improve the write margin over time. In this work, the improved write margin is sacrificed for enhancing the cell stability by lowering the WWL level. For example, at the threshold voltage degradation of 40 mV, WWL of 0.25 V shows the same write margin as the design target (Figure 2.17) while it eliminates data flip (Figure 2.16).

Figure 2.18 demonstrates Hspice simulation results of the half-selected SRAM cells under different operating conditions for verifying our proposed idea. Figure 2.18(a) shows that no data flip occurs in the stress-free state due to the initially designed HS-SNM. Once the NBTI and PBTI degradation increases and surpasses a critical threshold level, the stored data will be lost due to the cell stability failure as shown in Figure 2.18(b). However, the data flip can be avoided or delayed by utilizing a lower WWL level. Figure 2.18(c) shows the case of applying 230 mV to WWL for enhancing the time to data flip and improving

Figure 2.16: Simulation of the impact of NBTI and PBTI degradation on time to data flip with WWL voltage control based on 256-bit cells per bitline.

Figure 2.17: Simulation of the impact of NBTI and PBTI degradation on write margin with WWL voltage control based on 256-bit cells per bitline.

HS-SNM.

Comprehensive simulation data is presented in Figure 2.19, illustrating the benefits of the proposed WWL voltage control technique on cell stability, write margin, and time to data flip. The rate of NBTI and PBTI threshold voltage degradation over time is extracted from the measured data in [9, 10]. As expected, BTI stress degrades the half-selected cell stability and hence, fastens the time to data flip (Figure 2.19(a)). On the other hand, the write margin and the write delay are improved accordingly. Note that the stored data will be lost in half-selected cells from the stress time of 10^3 onwards due to the cell stability failure ($\text{HS-SNM} \leq 0$). Figure 2.19(b) shows the effect of the proposed WWL voltage control on the half-selected cell stability. The write margin is maintained at the design target over the stress time through the WWL level control. The result demonstrates that the proposed WWL control scheme significantly improves the cell stability and the time to data flip. Note that the HS-SNM is still positive even at the stress time of 10^5 . However, the write delay increases due to a lower WWL voltage level.

As discussed earlier, lowering WWL voltage level can efficiently deal with the NBTI and PBTI degradation in SRAM cell to maintain a healthy HS-SNM. However, write failures will occur once the write delay exceeds the given write window (ON clock cycle) due to the lowered WWL voltage. Therefore, meticulous considerations of correlation of the write delay, operating frequency, and WWL voltage level are required at the design stage to ensure the write delay falls into the write window. This will ensure that the overall SRAM performance is not compromised by the proposed scheme.

Figure 2.20 shows the error probabilities of half-select and write failure of the SRAM (with 64-bit cells connected to each bitline) based on 10k point Monte Carlo simulation. In the simulation, threshold voltage due to process variation, ΔV_{th} and standard deviation, σ are determined at $\pm 20\%$ and 3σ , respectively. The plot shows that without incorporating our proposed technique, the half-select error probability increases with higher level of BTI degradation. This is because the data in half-selected cells tend to flip easier due to degraded HS-SNM at higher BTI stress as illustrated in Figure 2.20. On the contrary, with the

(a)

(b)

(c)

Figure 2.18: Simulation of the half-selected cells during write operation based on 256-bit cells per bitline (a) fresh state, (b) NBTI = PBTI = 50 mV, and (c) Proposed.

(a)

(b)

Figure 2.19: Simulation of the impact of NBTI and PBTI on HS-SNM, write margin, and write delay based on 256-bit cells per bitline: (a) without proposed scheme and (b) with proposed scheme. The BTI over stress time is employed from [9, 10].

proposed technique, the half-selected error probability is reduced from 50mV onwards and achieving as high as 96% error probability reduction at 100mV degradation. Please note that there is no half-selected error occurred below 50mV degradation. This means that the SRAM cell stability is able to sustain up to 50mV degradation.

Figure 2.20: 10k point Monte Carlo simulation of error probabilities for half-select and write failure with $\pm 20\% \Delta V_{th}$ due to process variation within 3σ region based on 64-bit cells per bitline.

SRAM write failure error is the only constraint with decreased WWL voltage level. As discussed before, the proposed scheme capitalizes on the improvement of write margin due to BTI degradation so that the write margin is either maintained or improved after lowering down the WWL voltage. This is proven in the bar chart of Figure 2.20, which shows the write failure error probability of the SRAM with the proposed technique. The result indicates that the SRAM has a lower write failure error than the initial design value even with a lower WWL voltage. As a result, the SRAM integrated with the proposed scheme presents a very effective method with BTI degradation in SRAM.

2.3.3 Proposed NBTI/PBTI-Aware WWL Voltage Control Circuit

In this section, we present a conceptual implementation of the NBTI/PBTI-aware WWL voltage control circuit (Figure 2.21). The proposed circuit includes a replica bitline, a

read/write circuit, a flip detector, a counter, a decoder, and WWL drivers with level control. The detailed operation of the control circuit is discussed below.

To detect a desirable WWL level, the half-selected condition is applied to the replica bitline by enabling the replica wordline (WWLR) while leaving WBLR and WBLBR floating at V_{DD} . In such a situation, the accessed SRAM cell in the replica bitline undergoes the 6T read-like disturbance. If a data flip occurs at the replica bitline, the flip detector generates a pulse and increments the counter values. The output of the counter is then fed into the decoder to generate the required WWL control signal. Figure 2.22 shows the schematic of the WWL driver with level control. The WWL level is lowered by turning on the NMOS devices connected to GND.

The detailed operation of the entire tracking process is illustrated as follows: During the write operation, both WWLs on the selected row of the SRAM array and the replica cell are raised to a high potential based on the input address (ADDR). In such situation, the replica cell is in half-selected condition as described above. In order to prevent data flip in the SRAM array due to HS-SNM failure, additional time margin is inserted to tackle intra-die variations, and to detect data flip in the near future. This can be implemented by imposing a larger pulse width on WWL. As shown in Figure 2.23, by using a larger WWL pulse width, the proposed control circuit facilitates the detection of data flip in advance and prevents the occurrence of data flip in real operating conditions. Therefore, the replica cells are designed to run on a larger pulse width than that of the SRAM array to introduce more disturbance current.

If the flip detector detects data flip, the counter value will be incremented by one. Thus, the decoder outputs will enable one NMOS device ($LOW < 0 >$) from the WWL driver. The flipped cell data is then rewritten with the initial data for the next testing. This rewrite cycle ensures the replica cell to undergo the BTI worst-case scenario to detect the data flip in advance even with the SRAM cells holding the same worst-case scenario as replica cells. Note that the new effective WWL voltage will be applied to the SRAM array and replica cells on the following write cycles. The rest of the NMOS devices ($LOW < 1 >$)

Figure 2.21: Simplified diagram of the proposed WWL control scheme.

to LOW<3>) will be enabled one after another if any subsequent data flip is detected. In addition, this tracking process can also be repeated periodically to update the required WWL level when the NOP (No Operation) signal is high.

Figure 2.22: WWL driver with voltage control.

Figure 2.23: Margin control for detecting data flip in the near future.

While it is clear that the additional circuitries will incur power and area overheads, the area overhead is marginal (if not negligible) as compared to the whole SRAM array since only one replica bitline and its read/write circuit is used in this design. The flip detector can be constructed simplistically by a few digital logic gates, such as NAND and NOR gates.

On the other hand, the counter, decoder and NMOS level control area are fully depending on the counter count bits. The larger the count bits, the larger the area and the more effective the WWL voltage control can offer against NBTI/PBTI degradation. Therefore, the tradeoff between the area consumption and the effectiveness of WWL voltage control against NBTI/PBTI aging must be meticulously designed.

2.4 Summary

SRAM cell structure consists of two cross-coupled inverters connected as a latch circuitry. Each inverter stored one value which is different from the other inverter. Therefore, NBTI and PBTI degradation in SRAM cell are unavoidable regardless of the stored data even it is in standby mode. In this chapter, analysis based on 32-nm high-k/metal-gate PTM on the impact of NBTI and PBTI degradation on various SRAM parameters such as read stability, write stability, half-selected cells stability, and time to data flip have been presented. Simulation results have shown that BTI stress deteriorates the stability of the half-selected cell over time. To address this stability issue, an NBTI/PBTI-aware WWL voltage control technique without boosted supply voltage and additional power dissipation for half-selected cell stability improvement is proposed. The proposed technique is to lower the WWL level for improving the half-selected cell stability after BTI stress. Simulation results demonstrated significant improvements in the half-selected cell stability and the time to data flip without degrading the write margin. Monte Carlo simulation further clarified that the proposed scheme is a very efficient method to compensate the BTI degradation in SRAM. In addition, a sample implementation of the proposed NBTI/PBTI-aware WWL voltage control technique is also presented. The control circuits measure the time to data flip of the SRAM cells in the replica bitline and prevent data flip in the half-selected cells by adjusting the WWL level. The proposed WWL control scheme is beneficial to many DVFS systems where BTI stress significantly affects the SRAM stability, particularly at ultra-low voltage operation.

Chapter 3

An 8T SRAM with BTI-Aware Stability

Monitor and Two-Phase Write

Operation for Cell Stability

Improvement in 28-nm FDSOI

3.1 Background

With the aggressive scaling of physical geometry size in CMOS technology, random dopant fluctuations and critical dimension variations are not the ones and only challenges in robust SRAM design. Instead, lifetime reliability issues such as BTI, HCI, and TDDDB have emerged as the critical design challenges where the MOSFET device's performance characteristics (i.e., timing/frequency) is deteriorated over the functional operating cycles. This results in functional failure whenever the circuit performance exceeded the design targeted specification. Amongst all the lifetime reliability issues, BTI has been widely recognized as the serious concern that has a significant influence on SRAM cell's metric [22]. Moreover, new degradation concerns like PBTI in NMOS is further exacerbated in high-k metal gate process where it was previously negligible in the poly-gate process [9, 10, 37, 38]. As such, the SRAM becomes more vulnerable to performance degradations

or unrecoverable malfunctions. Furthermore, it is difficult to identify the failure SRAM cell due to BTI after the fabrication process. Therefore, an integrated BTI-aware circuit design where it can monitor and fine-tune the bitcell metric is essential to prevent SRAM functional failure due to BTI.

3.2 Motivation

Embedded SRAM-based memories are commonly found in the application-specific integrated circuit (ASIC) to achieve a faster read or write access [55–58]. It usually occupies a large portion of space in ASIC and forcing the SRAM cell using minimum device size to achieve high density array. However, the design of the cell with minimum device size are subject to having just about a right marginal design parameter: cell hold stability (CHS), HS-SNM, WM, etc. As a result, the SRAM cells are very much prompt to NBTI and PBTI reliability threats that exacerbate the cell targeted design margin over its operating cycles. Furthermore, the design margin gets worsen with the presence of device mismatches. This has posted a critical reliability issue to SRAM to ensure a robust operation where the functional lifetime is an important requirement (i.e., in automotive, surveillance, satellite area) [59–63].

The BTI is characterized by the shift in V_{th} of the MOSFET device. It occurs when the gate of the PMOS device is under negative bias conditions (i.e., $V_{gs} = -V_{DD}$) and positive bias conditions on NMOS device (i.e., $V_{gs} = V_{DD}$) that caused the generation of interface traps. These interface traps are formed at the $Si - SiO_2$ interface due to crystal lattice mismatch. Whenever a correct voltage is applied at the MOSFET device gate, the holes in the channel would have chances to dissociate the weak Si-H bonds and thereby generate the interface traps. As such, the charges are trapped which are immobile to carry the current from drain to source. Therefore, BTI aging manifests as an absolute increase in MOSFET V_{th} . The increase in MOSFET V_{th} lead to device performance changes and could easily cause reliability degradation and potential device failure [64]. The device performance changes in SRAM cell typically degrades the SRAM SNM and thus, degrading cell's read and write

stability which probably results in SRAM functional failure [62, 65]. Furthermore, SRAM cells with minimum device size experienced the largest sensitivity to process variations. Together with the aggressive scaling in gate length of CMOS technology, the process variation in SRAM cells is becoming extremely critical to determine the SRAM functional yield. For instance, the foundries could not identify the marginally passed SRAM cells after fabrication which could fail during its operation lifetime due to BTI degradation. Thus, BTI has become a significant reliability concern and design challenges in deep nanoscale technologies as well as a limiting factor in future device scaling [22, 66].

3.2.1 Negative and Positive Bias Temperature Instability Model

There are two phases in BTI known as stress phase and recovery phase. In stress phase, the MOSFET channel is turned-on and both its source and drain are at equivalent potential. The high energy holes on PMOS and electrons on NMOS under the channel tend to break the weak Si-H bonds at the $Si - SiO_2$ interface and thereby generating the interface traps. These interface traps lead to an increase in the MOSFET V_{th} as long as the stress condition is present. Once the stress is removed, the MOSFET will immediately enter into the recovery phase. In the recovery phase, the MOSFET channel is turned-off and Si-H bonds may be reformed (annealing). Note that not all the Si-H bonds will be reformed. The irreformable Si-H bonds will then cause the permanent increase in MOSFET V_{th} .

Reaction-Diffusion (RD) is one of the popular widely accepted explanations to describe the BTI-induced MOSFET V_{th} shift under DC static stress condition [35, 54, 67–72]. Based on the past various research and experiments, it has proven that the MOSFET V_{th} shift under DC static stress is closely following a power law with respect to the aging stress time [62]:

$$\Delta V_{th}(t) = K_{DC} \times t^n \quad (3.1)$$

where K_{DC} represents the technology dependent parameter (i.e., device geometry, operating voltage, operating temperature, and interface trapped charges, etc.), t is the stress time in seconds and n is the time exponent of degradation. Since MOSFET device operation

condition is fully depending on its gate signal swing, the device will not always encounter DC stress. Therefore, the equation 3.1 can be simplified under alternative stress and given by [62]:

$$\Delta V_{th}(t) = \alpha(s, f) \times K_{DC} \times t^n \quad (3.2)$$

where α is a prefactor of operating frequency and signal probability. In a short summary, equation 3.1 and 3.2 show that BTI has a strong relationship with operating voltage, operating temperature, and operating frequency. Anyone of these parameters will influence the magnitude of change in $\Delta V_{th}(t)$.

3.2.2 State-of-the-Art Techniques and Their Limitations

Design margin reservation is recognized as one of the conventional state-of-the-art techniques to overcome BTI degradation. The circuit designers firstly require considering the device degradation at the beginning of the design phase and reserve sufficient operating margins over its operational lifetime. Typically, the SRAM bitcell area is increased for the purpose of margin reservation. This leads to additional area overhead which is undesirable on designing SRAM array because the area overhead is proportional to SRAM bitcell. Moreover, it is also difficult to determine how much additional margin require in advance since each of the SRAM bitcell is experiencing different signal probability. Besides the margin reservation, on-chip monitoring such as using ring oscillators, current sensors, or PMOS V_{th} sensors was developed to investigate and monitor SRAM cell reliability and performance degradation due to BTI [11, 12, 73]. The idea of on-chip monitoring is to provide BTI degradation information and feedback to the BTI compensation circuits. However, most of the reported works are only involve BTI degradation monitoring circuits only [21, 73, 74]. None of the works reported to-date clearly shown the all in one solution which includes BTI on-chip monitoring together with the compensation circuits. In this section, some state-of-the-art techniques such as BTI on-chip monitoring and BTI circuit solution will be discussed.

3.2.2.1 BTI SRAM Monitoring Circuits

Figure 3.1: Reported SRAM cell in measurement state [11].

In [11], an on-chip monitoring of NBTI degradation in SRAM cells is reported. The reported work is a current sensing based measurement to measure the current flow through the PMOS pull up devices in SRAM cell and compare with a reference current to determine the NBTI degradation. The measurement is done by switching on the access transistor of the cell and forcing two bitlines, BL and BLB to V_{SS} as shown in Figure 3.1. Subsequently, the PMOS pull up devices are used to charge the BL and BLB-Caps. The difference in-term of BL/BLB voltage level to reference could determine the NBTI degradation in the SRAM cell. Note that the entire measurement process is a destructive operation and the original data can no longer be restored after the measurement. Therefore, the author has included an extra register file for temporary storage of the data before initializing the testing on the particular cell. Figure 3.2 and Figure 3.3 show the general structure of SRAM with the proposed DFT block and modified row decoder block and write circuitry from the author. The DFT block is a current measurement unit block for NBTI degradation. The entire measurement process takes two clocks to complete on the selected cells as claimed by the author. The first cycle is the measurement cycle where the pseudo-write operation is performed on the selected cells with both BL and BLB connected to V_{SS} . Thus, the selected cells are entering the stage as described in Figure 3.1. In the second clock cycle, the BL and BLB are disconnected from V_{SS} and left BL and BLB. As such, the PMOS pull up devices are charging the BL and BLB-Caps which later evaluate the NBTI degradation from the

DFT block with the reference current.

Figure 3.2: Reported SRAM structure with DFT block [11].

The advantages of this reported technique can monitor the NBTI degradation inside the operational SRAM cells and without compromising the compactness of the SRAM array. However, the downside is that the stored data is lost every time due to the destructive measurement operation and large power overhead is expected since there is a static discharge path from V_{DD} to V_{SS} during the measurement stage.

A similar approach is reported in [12]. The author reported an NBTI degradation sensing scheme in an SRAM register file as shown in the Figure 3.4. The scheme configures a conventional 6T-SRAM bitcell into V_{th} sensors. This is achievable via implementing two header devices HL and HR, each of them sharing two columns. When a test is asserted, the BL and BLB on the selected cell are connected to V_{SS} . Now, two V_{th} sensors are formed through the PMOS pull up devices, PL and PR from the cell together with HL and HR devices. VL and VR are the two outputs which claimed to be linear functions of the V_{th} of either PL or PR. The change of VL and VR from the initial reading is determined to be the amount of NBTI degradation on the PL or PR. Although this proposed approach can

Figure 3.3: Reported modified row decoder blocks for NBTI testing [11].

Figure 3.4: Reported NBTI degradation sensing scheme in an SRAM. [12].

well characterize the NBTI degradation inside a real operating SRAM, it is also a destructive operation where stored data eventually is lost after the testing. Moreover, no circuit solution such as NBTI compensation circuit is discussed or provided.

3.2.2.2 BTI Circuit Solutions

In [13], the authors reported a new adaptive body (ABB) scheme to compensate NBTI degradation in SRAM cell PMOS pull-up devices. The ABB circuit can tune the transistor threshold voltage by controlling its body-to-source voltage (V_{BS}). A higher transistor's body voltage reduces the threshold voltage whereas a lower body voltage increases the threshold voltage. Consequently, the NBTI degradation in SRAM cells can compensate with the reported circuit. Figure 3.5 shows the reported ABB circuit for NBTI compensation. The circuit was developed by utilizing the equations (4), (5), and (6) under Section II in [13]:

$$|V_{thp}| = |V_{thpo}| + \Delta|V_{thp}|_{BB} \quad \text{and} \quad (3.3)$$

$$\Delta|V_{thp}|_{BB} = \gamma(\sqrt{2\phi_F - V_{SB}} - \sqrt{2\phi_F})$$

$$V_{SB} = \frac{2\sqrt{2\phi_F}}{\gamma} \times \Delta|V_{thp}|_{NBTI} - \frac{1}{\gamma^2} (\Delta|V_{thp}|_{NBTI})^2 \quad (3.4)$$

$$V_{Bp} = V_{DD} - \frac{2\sqrt{2\phi_F}}{\gamma} [|V_{tpstressed}| - |V_{thpo}|] + \frac{1}{\gamma^2} [|V_{tpstressed}| - |V_{thpo}|]^2 \quad (3.5)$$

where $|V_{thpo}|$ is the PMOS device threshold voltage at zero body biased, $|V_{thp}|_{BB}$ is the voltage shift after applying body biased V_{SB} , γ is the body effect coefficient, ϕ_F Fermi potential, $\Delta|V_{thp}|_{NBTI}$ is the difference between estimated threshold voltage, and $|V_{tpstressed}|$ is the threshold voltage changed due to NBTI. The equation 3.5 shows the PMOS body bias voltage to compensate NBTI degradation after substitution of equation 3.4 into 3.3 and rearrange it. An ABB circuit consists of a V_{tp} sensing circuit, two amplifier circuits, and a squaring circuit reported based on equation 3.5 (Figure 3.5). The sensing circuit is used to estimate the PMOS threshold voltage shift under worst-case NBTI effect. The two

amplifiers and squaring circuit are to produce the required threshold voltage used to bias the PMOS body voltage. Therefore, the impact of NBTI degradation in SRAM cells is able to compensate with a proper PMOS body voltage supply by this proposed circuit. The downside of the reported circuit technique that it is too complex to design and multiple V_{DD} are required. Moreover, no test chip results were provided for proof-of-concept in the paper.

Figure 3.5: Reported ABB circuit for NBTI compensation [13].

The following circuit technique reported in [14] is a circuit technique to enhance the NBTI recovery in SRAM cells. The author modified the conventional SRAM cell as shown in Figure 3.6 to allow a faster NBTI recovery. There are two operation modes in this reported SRAM cell, normal operation mode and recovery boost mode where it is controlled by the signal CR. The CR signal can directly be applied to an SRAM row or array for smaller area overhead. When the data in the cell is no longer needed or the cell is in the idle state, the CR signal will then switch from '1' to '0' and eventually placed both PMOS into recovery boost mode. The two extra PMOS transistor in the cell are used to switch between the recovery mode and the normal operation mode within one single cycle. Without these two PMOS transistors, the switching into recovery mode will need multiple clock cycles in order to pull the node '0' and node '1' to V_{DD} which is undesirable for high-speed operation. Furthermore, there is no PBTI exacerbation in the NMOS transistors when the cells

are in recovery boosting mode since both NMOS's drain/source and gate are at V_{DD} level ($V_{gs} = 0$). However, the reported technique is undesirable for large SRAM arrays since the area overhead is large due to two additional PMOS transistors in a cell and it could only be applied to the cell where the data is no longer needed.

Figure 3.6: Reported SRAM modified cell [14].

Figure 3.7: Reported SRAM array with modified cell [14].

3.3 Contributions

As discussed in Chapter 3.2.2, none of the state-of-the-art techniques effectively offers an automated on-chip solution for mitigating or compensating BTI degradation in SRAM. Therefore, it is important to provide an automated on-chip solution for BTI degradation. In the following chapter, we propose an on-chip replica row based BTI-Aware Stability Monitor (BTI-SM) assisted with Two-Phase Write Operation (TPWO). Dynamic reliability management is achieved through automated BTI-aware WWL control.

3.3.1 SRAM Cell Under BTI Degradation

Figure 3.8: Schematic diagram of a decoupled 8T SRAM bitcell [15].

Figure 3.8 depicts the decoupled 8T SRAM cell with dedicated write (6T) and read (2T) ports with differential read bitlines. Note that NBTI and PBTI induce the V_{th} shift on pull-up and pull-down MOSFET devices in the cross-coupled inverters depending on the storage data pattern, Q and QB. It results in BTI degradation, which is an unavoidable reliability issue in SRAM cells. The V_{th} shift eventually causes an undesired change in the SRAM initial design parameters such as the HS-SNM and WM. In the bit-interleaving architecture, half-selected cells during write experience the worst-case cell stability, which is characterized by HS-SNM. More details analysis on the impact of BTI degradation on

Figure 3.9: Simulation of the impact of BTI degradation on HS-SNM with different WWL voltage control.

Figure 3.10: Simulation of the impact of BTI degradation on WM with different WWL voltage control.

SRAM operation and parameters can be found in Chapter 2.3.1.

The simulation results in Figure 3.9 shows the impact of BTI on worst-case HS-SNM with different WWL voltages based on 5k Monte Carlo points on nominal V_{DD} at FS corner. As expected, HS-SNM degrades with the increase in BTI but under-driven (UD) WWL improves it by weakening the drive current on access transistors (MN3 and MN4) and eventually reduces the amount of disturbance current flowing from WBL/WBLB to the storage node. Figure 3.10 depicts the normalized WM vs. BTI. WM improves with the increase in BTI but degrades with UD WWL, which is in an opposite trend to that of HS-SNM. Therefore, careful control of the UD WWL utilizing the amount of improved WM after BTI can maintain HS-SNM and WM to be similar to the initial values. Note that BTI degradation has a negligible impact on the decoupled SRAM read static noise margin (RSNM). As evidenced by the simulation results, the UD WWL approach is hence utilized in our proposed BTI-SM, which is explained in the subsequent chapter.

3.3.2 Proposed BTI-Aware Stability Monitor (BTI-SM) Scheme

Figure 3.11 depicts the proposed BTI degradation aware SRAM architecture. The 16kb SRAM array consists of 4 banks (each 32x128). A Replica Row (RR) (1x128) and a BTI Flip Detector (BTI-FD) are placed at the top of the SRAM array along with a BTI-Aware Controller (BTIC). A RR is employed over a replica column to share the same column circuitry and generate multiple data for accurate HS-SNM monitoring inclusive of PVT variations. The BTIC controls the voltage levels of the WWL drivers driving the SRAM array and RR. Besides, the BTIC also issues ‘Write’ and ‘Read’ signals to RR_WWL and RR_RWL drivers for write and read in RR. Data loading in RR is done through Bank 3 WBL and is controlled by BTIC ‘Write’ signal. BTI-FD consists of read circuits and single flip detectors for each 16 sets of the RR cells. The BTIC is comprised of an SRAM WWL voltage controller and a 16:1 selector to select one of the 16 sets of RR cells. Two replica columns are employed in each bank for two-phase write operation to improve the WM, which will be discussed in the later chapter. Hierarchical write bit line and non-hierarchical

Figure 3.11: Proposed BTI-SM architecture.

Table 3.1: Replica row sets. $W_{PU} = W_{PD} = 80\text{nm}$; $L = 30\text{nm}$								
Set	0	1	2	-	-	13	14	15
W_{PG} (nm)	80	90	100	-	-	210	220	230
Stability failure threshold (SFT)	Highest (low reliable)			-	-	Lowest (high reliable)		

read bit line architectures are used. 8:1 CMUXs, row and column address decoders, control circuit, sense amplifiers and data drivers are not shown for simplicity.

The RR cells are connected to the SRAM array WBL (Bank 3) to mimic the half-selected disturbance condition as bitline loading effect is one of the important factors. Another consideration is that the RR cells must fail in HS-SNM before the SRAM array cells so that the BTI-aware WWL voltage control prevents data loss due to BTI. To cater this, 16 sets (Set 0 to Set 15) of SRAM cells in RR is employed; each set differs in the write access device width by 10nm successively (Table 3.1) with an increasing trend for the half-select disturbance injection. These 16 sets cover a wide range of silicon skew to emulate the effect of BTI on HS-SNM failure better as illustrated in Figure 3.12. A higher write access device width set tends to fail earlier than the average of SRAM cells with the presence of BTI degradation. Therefore, designers can leverage the 16 sets in RR as a stability failure threshold knob to trade-off and achieve a highly reliable SRAM under BTI degradation.

RR and SRAM core (SC) WWL drivers voltage levels are controlled by the PMOS switches gated by digital control codes (VS[6:0]) from the BTIC. The BTIC has five states: 1) Idle 2) Half select noise condition (HSNC) 3) Cell Flip (CF) 4) WWL voltage control (WWLVC) and 5) Cell writeback (CWB). During BTI aging test ($TM = '1'$), the BTIC transits from Idle to HSNC in which half-select disturbance condition is induced for RR with the given voltage level ($RR_WWL = '1'$). Next, the BTIC transits to the CF state where RR cells are read ($RR_RWL = '0'$ and $RR_PRCH = '1'$) using the read circuit. A 'Flip' signal is generated in the BTIC depending on the replica set selection and the single flip detector output. Flip = '1' when a data flip occurs in the RR cells under the half-select disturbance else Flip = '0'. If Flip = '1', the BTIC transits to the WWLVC state and lowers

Figure 3.12: Mechanism of BTI degradation aware SRAM using multiple sets of replica row cells. Multiple sets of replica cells are designed to fail above the average of SRAM core cells. Stability failure threshold (SFT) can be set to trade-off between low and high reliability of data storage in SRAM core cells.

Figure 3.13: Simulation of BTI-SM (TM = '1') showing how closed-loop configuration establishes a desired WWL voltage level for reliable HS-SNM at 1GHz.

the WWL voltage level by one step through the digital code, VS[6:0]. If Flip = '0', BTIC moves back to HSNC. Next BTIC transits to the CWB state where flipped data in RR cells are written back (Write back = '1') with original data (Q = '0'). After this, BTIC again transits to the HSNC state and continues to monitor HS-SNM failure till no data flip is detected. This closed-loop configuration establishes a desirable WWL voltage level for the WWL drivers driving RR and the SRAM array, and maintain reliable CHS after BTI aging. Figure 3.13 depicts a simulation result of the proposed UD WWL control using the WWL voltage levels listed in Table 3.2. Simulation results demonstrate how BTIC is transiting from HSNC → CF → WWLVC → CWB → HSNC - - - establishes a desirable WWL voltage level of 91% V_{DD} , i.e., 910mV ($V_{DD} = 1\text{-V}$) for RR and SRAM array WWL drivers under BTI = 100mV stress for reliable HS-SNM.

Table 3.2: WWL voltage levels vs. digital voltage control code.

VS[6]	VS[5]	VS[4]	VS[3]	VS[2]	VS[1]	VS[0]	WWL Voltage Level
1	1	1	1	1	1	1	100% V_{DD}
1	1	1	1	1	1	0	97% V_{DD}
1	1	1	1	1	0	0	94% V_{DD}
1	1	1	1	0	0	0	91% V_{DD}
1	1	1	0	0	0	0	88% V_{DD}
1	1	0	0	0	0	0	85% V_{DD}
1	0	0	0	0	1	0	82% V_{DD}
0	0	0	0	0	0	0	79% V_{DD}

3.3.3 Proposed Automated Two-Phase Write Operation (TPWO) Scheme

A TPWO scheme with an automatic phase control is proposed to encompass certain extreme write failure cases from UD WWL. Figure 3.14 depicts the implementation of the proposed TPWO for WM improvement without HS-SNM degradation. In the write operation, the scheme divided the WWL voltage level into two phases. In Phase I of the write operation, the WWL level is determined by digital code, VS[6:0], which is set by the BTI-SM explained in the previous chapter. As time elapses, the pre-charged WBL on data storage node '0' of half-selected cells is discharged through the pull-down device. Since the majority of cell disturbances occur in Phase I, Phase II allows the WWL voltage to rise to

Figure 3.14: Proposed automated TPWO scheme.

Figure 3.15: Worst HS-SNM as a function of WWL and WBL with 10k Monte Carlo simulation.

Figure 3.16: Simulation of the half-selected cell with TWPO during write operation.

Figure 3.17: TWPO simulation on Phase I and Phase II during write operation.

V_{DD} , and thereby improves WM. A simulation results with the worst bit cell HS-SNM as a function of both the WWL and WBL voltages with 10k Monte Carlo samples at FS = 27°C and BTI = 100mV is shown in Figure 3.15. The HS-SNM improves with a decrease in the WBL voltage where it has proven the rise of WWL voltage on Phase II is possible without data loss. Figure 3.16 shows an example of a simulated waveform on a half-selected cell with the proposed TPWO scheme. Two replica columns (RC_LWBL0 and RC_LWBL1) are implemented to emulate the worst-case half-selected WBLs discharge to $V_{DD}/2$. Thus, Phase II is activated by setting P2WE = '1' and VS'[6:0] = '111111' when both of the RC_LWBL0 and RC_LWBL1 fall below the threshold of $V_{DD}/2$. This places the WWL at V_{DD} . Note that $V_{DD}/2$, not $V_{DD}/3$ is adopted due to the circuit switching delay to generate P2WE = '1' at $V_{DD}/3$. To reduce the WBL discharging time, we use a WBL dipper that initially discharges WBLs to a lower level ($\sim 80\%$ of V_{DD}). This helps Phase II to start earlier and complete the write operation within a cycle. Figure 3.17 shows the simulated waveforms of the proposed TPWO scheme.

3.3.4 Fabrication and Experimental Results

Figure 3.18: Measurement of WWL voltage level in test chip.

A 16kb SRAM test chip implementing the proposed BTI-SM and TWPO scheme with automatic phase control was fabricated based on 28-nm FDSOI technology. Before starting

Figure 3.19: SRAM cell in stress condition and testing condition together with the test sequence for stress and fast measurement without BTI relaxation.

the measurement, it is important to ensure that the proposed UD WWL voltage and TPWO scheme are functional in the test chip. Figure 3.18 shows the measured 8 WWL voltage levels in the test chip. It also shows at the end how TPWO is able to raise the WWL voltage level to the highest level of 100% V_{DD} in Phase 2. Figure 3.19 shows the SRAM cell in stress and testing condition with the technique of test sequence for stress and fast measurement to prevent BTI relaxation. The test begins by initializing the SRAM and RR cells by writing $Q = '0'$ and $QB = '1'$. As to accelerate BTI aging, $V_{STRESS} = 2\text{-V}$ is applied to the SRAM array and the RR cells in the BTI stress period (t_{stress}). The BTI stress period varies from 0.25hr to 1hr. In the measurement interruption, the SRAM cell voltage is switched from V_{STRESS} to V_{NOM} (1-V). A small amount of waiting period (few clock cycles) is required after the transit from high voltage to a lower voltage for voltage stabilization. Afterward, the TM signal is switching from '0' to '1' to set the WWL voltage level for reliable HS-SNM determined by the BTI-SM as discussed in Chapter 3.3.2. After the measurement, the SRAM switches back to the BTI stress condition. The entire measurement interruption period is $< 3\mu\text{s}$ to prevent any BTI relaxation [11].

Figure 3.20: Measurement of BTI-SM using closed-loop configuration to achieve desirable WWL voltage level control against BTI degradation.

The measured WWL voltage level at each interruption time (also known as BTI stress

Figure 3.21: Measurement on pre- and post-stress of half-selected cell failure w/o proposed BTI-SM.

Figure 3.22: Measurement of the WWL voltage level configuration by BTI-SM due to BTI degradation in SRAM array.

period) is presented in Fig 3.20. As expected, the WWL voltage level decreases with BTI stress time. This shows a strong evidence that BTI-SM is able of monitoring and maintaining a reliable HS SNM after BTI degradation. To further substantiate the effectiveness of the proposed BTI-SM, we measured the pre- and post-stress of half-selected cell failure on 1024 cells, as presented in Figure 3.21. Again, the half-selected cell failure showed a significant reduction from 57.13% to 0% after stress with the proposed BTI-SM at $V_{\text{cell}} = 0.7\text{-V}$. Note that the WWL voltage level has been lowered to 82% of V_{DD} by BTI-SM after 48 hours of stress to achieve a stable HS-SNM (Figure 3.22). A comparison of WWL volt-

age level between conventional and proposed BTI-SM across different Vcell after 48-hour stress is shown in Figure 3.22. It is apparent that lower Vcell had a lower WWL voltage level set by BTI-SM with the same amount of stress time to maintain HS-SNM.

Figure 3.23: BTI-SM area overhead.

Figure 3.23 delineates BTI-SM area overhead. The overhead for the 128×128 SRAM is 10% and for the 256×128 SRAM it is 5%. This shows that the area overhead of BTI-SM is reduced with a larger SRAM array. Thus, it can be concluded the area overhead of the proposed BTI-SM is minimum and negligible. Figure 3.24 shows a die micrograph and the summary of an evaluation of the 128×128 SRAM with BTI degradation aware design technique in 28-nm FDSOI technology.

A comparison table (Table 3.3) summarized the proposed technique to the literature reported technique to further strengthen the advantages of the proposed technique. The reported techniques [13] and [14] only cater for NBTI degradation in PMOS on SRAM cell whereas our proposed technique took care of both NBTI and PBTI degradation. Furthermore, the data in SRAM cell could be lost after the BTI solution in [14]. On the implementation comparison, [13] used analog circuitry to generate the body bias for SRAM cell pull-up device, PMOS. Therefore, it is foreseeable that the reported design in [13] is more complex and not scalable across technology nodes as compared to [14] and proposed technique. Most importantly, no silicon validation was provided by [13] and [14]. As a result, our proposed technique has distinct advantages over the [13] and [14].

Technology	28-nm FDSOI CMOS
Memory Size	16 kbit
Overall Chip Area Breakdown	
SRAM Array & Peripheral Circuitries	31510 μm^2
Proposed BTI-SM & TPWO	3142 μm^2 (10% additional overhead)
Measured Standby Leakage Breakdown @ VDD=1V	
SRAM Array	3.45 μA
Peripheral Circuits	18.23 μA
Proposed BTI-SM & TPWO	0.768 μA (3.42% additional overhead)
Measured Active Power @ VDD=1V ; Freq. = 1GHz	
Read	2.11 mW
Write	1.3 mW
Measured Access Time @ VDD=1V ; Freq. = 1GHz	
Read Access Time	452 ps

Figure 3.24: Chip Microphotograph and test chip summary.

Table 3.3: Comparison between proposed technique to reported techniques.

	[13]	[14]	Proposed Technique
Technology Nodes	65-nm	32-nm (PTM)	28-nm FDSOI
SRAM Cell Structure	6T	8T	8T
BTI Solution	PMOS body bias for NBTI compensation (NBTI Only)	NBTI recovery boosting (NBTI Only)	BTI monitoring scheme with automated WWL control for BTI compensation
SRAM Cell Data	Retain	Lost	Retain
Implementation	Analog(Complex)	Digital(Simple)	Digital(Simple)
Silicon Validation	Only post-simulation results	Only simulation results	Chip experimental results
Scalability	Difficult	YES	YES

3.4 Summary

A 16kb SRAM test chip with on-chip circuit techniques for dynamic reliability management is presented. The proposed BTI-SM scheme monitors the HS-SNM through the RR and establishes a desirable WWL voltage level in the closed-loop configuration to maintain the degraded HS-SNM due to BTI in SRAM cell. To overcome the effect of UD WWL in certain extreme write cases, we also proposed a TWPO where it divided the WWL voltage level into two phases on write cycle to improve WM. TWPO reduces the WWL in Phase I for HS-SNM stability control and raises WWL to V_{DD} level in Phase II for WM improvement without degrading the half-selected cell stability. It is achieved by activating Phase II when the WBL level falls to 50% of V_{DD} where the half-selected noise disturbance has been minimized. The 16kb SRAM test chip was prototyped using 28-nm FDSOI CMOS technology. The hardware implementation demonstrates a significant reduction in half-selected cell failure with the presence of BTI effects in SRAM cell. The proposed technique can be employed by SRAMs where reliability is a major concern.

Chapter 4

A 16kb 28-nm FDSOI Column-based Split Cell-VSS Data-Aware Write-Assisted 9T Ultra-Low Voltage SRAM with Enhanced Read Sensing Margin

4.1 Background

With the massive growth of implantable devices, intelligent wearable devices, wireless sensor nodes, and other electronic gadgets have been significantly increasing in current modern century [75,76]. All of these electronic gadgets are of battery-powered, and hence strongly rely on supply voltage scaling on the SoC to extend or maximize the battery life.

SRAM is the most common type of on-chip memory can be found in modern SoC design. Typically, SRAM implemented with minimum sized devices occupy a large area portion inside SoC [77]. Besides, the total power of SoC is also dominated by SRAM leakage due to the high packing density. This trend continues to increase over the past few years due to the complexity of multicore and multithreaded computing platforms [78]. Moreover,

SRAM V_{min} is recognized as the bottleneck and is often leading to separate supply voltage for the SRAM and logic circuitry [16]. As such, it is important and challenging for SRAM to operate under ultra-low voltage regime. In this chapter, a CS-CVSS data-aware write-assisted 9T ultra-low voltage SRAM with enhanced read sensing margin in 28-nm FDSOI technology is proposed to address the issue.

4.2 Motivation

With the use of advanced technologies, the capabilities of packing more transistors into a single die have been continuously increasing. This allows the modern SoCs to have more on-chip SRAM (cache) to store and share information as to improve the parallel processing speed. However, the total power contribution from SRAM inside SoCs also increases dramatically due to high-density bit cell implementation. Hence, energy efficiency has become the main constraints in battery-operated electronic devices where the device uptime is fully determined by battery lifetime. Equation 4.1 describes the total power of a SoC:

$$P_{Total} = P_{Static} + P_{Dynamic} \quad (4.1)$$

$$P_{Static} = V_{DD} \times I_{Leak} \quad (4.2)$$

$$P_{Dynamic} = \alpha \times V_{DD}^2 \times Freq \times C_L \quad (4.3)$$

where P_{Static} is the static power and $P_{Dynamic}$ refers to switching power. The supply voltage, V_{DD} is the common variable across P_{Static} and $P_{Dynamic}$ from equation 4.2 and 4.3. It indicates clearly that P_{Static} and $P_{Dynamic}$ can be reduced by scaling down the V_{DD} , and thereby reduce the P_{Total} . As such, aggressive supply voltage scaling is widely adopted in current SoC to maximize the battery lifetime. However, it is very challenging to operate SRAM under ultra-low voltage (near- or sub-threshold regime) because of the cell structure, de-

graded cell stability, poor bit line read sensing and exponentially increased sensitivity to PVT fluctuation.

Conventional 6T SRAM fails to operate in such scaled voltage environment. It is mainly because the 6T SRAM bit cell design is targeted to operate robustly at the nominal supply voltage. The cell stability, read, write, and half-selected margin start to erode quickly when not operating in nominal condition [79]. These are the well-known noise margin that is impacting the cell stability. The cell stability will become worse if the ratio cell structure is not designed properly [80].

Read margin is characterized in the read access cycle. At the onset of a read operation, both access devices are turned on by the $WL = '1'$ and the bitline pair is pre-charged at '1'. Based on this biasing condition, the bitline that is connected to the node storing data '0' is discharged through the pull-down device in the cell. Within the discharging window, a voltage dividing effect across the access device and the pull-down device lead to an increased voltage level on data '0' node. The unwanted increase in voltage, also known as disturbance voltage, eventually degrades the read margin as shown in Figure 4.1. Moreover, the read margin would be deteriorated if the operating voltage (V_{DD}) continues to scale. Note that the disturbance voltage can be reduced by sizing up the pull-down device. A model reported in [80] has clearly indicated the proportional relationship between the V_{DD} to read margin.

Write margin is characterized in the write access cycle. At the onset of the write operation, both access devices are turned on by the $WL = '1'$ and the bitline pair is loaded with the write data '0' and '1'. The storage node that is connected to the bitline loaded with write data '0' through the access device will be discharged to change the cell data. In a scaled V_{DD} environment, a desired write trip point, also known as the write margin, without consuming too much energy to drive the pre-charged bitline to voltage '0' in every write cycle is important in ultra-low voltage design to ensure SRAM writability [81]. The write margin in SRAM is defined as the maximum bitline voltage that is able to change the cell data. Typically, the sizing of pull-up devices in SRAM cell determines the write margin

Figure 4.1: Read margin during read operation.

and sizing of pull-down devices determines the read margin. This ended up with a design conflict on SRAM to achieve high read and write margin. Therefore, write margin design is also a critical challenge in scaled V_{DD} environment.

The half-selected margin poses another reliability issue in ultra-low voltage environment. It occurs on the half-selected cells during the read and write operation (conventional 6T SRAM cell structure). On the read and write operation, both access devices on the half-selected cells of the selected row are turned on by the $WL = '1'$ with the bitline pair pre-charged at $'1'$. Based on this biasing condition, the half-selected cells would experience the read-like disturbance due to voltage dividing effect on data $'0'$ node discussed earlier. If the disturbance is large enough and exceeds the cross-coupled inverters threshold voltage, the cell data would be flipped because of the positive feedback effect on the cross-coupled inverters. As such, the half-selected margin is defined as the maximum disturbance voltage on data $'0'$ node that causes the data flip. Although the disturbance is lower with scaled V_{DD} , it is still important to ensure that the SRAM has sufficient half-selected margin in

ultra-low voltage operating environment for robust operation.

Moreover, the 6T SRAM condition becomes worse when coupled to PVT fluctuation and make it difficult to operate in ultra-low voltage environment. As a result, various read and write assist techniques have been reported to tackle the limitations of the conventional 6T SRAM.

4.2.1 State-of-the-Art Techniques and Their limitation

There are various assist techniques reported in the literature to enable ultra-low voltage SRAM. These assist techniques include boosted WL voltage [16, 82–86], under driven WL voltage [16], adjustment of cell-VDD (CVDD) [87–92], dual voltage supply scheme [16, 88, 93, 94], negative bitline (BL) [90], and write-back (WB) schemes after read [17, 89, 95]. In this section, a few representative state-of-the-art assist techniques that enable ultra-low voltage SRAM are discussed.

In [16], a WL-level programming scheme with dynamic-array-supply control assist technique is reported. The reported technique supplied dual-supply, V_{DD} and V_{SM} to the SRAM cell and level-programmable WL drivers (LPWD) to generate an intermediate WL level between the V_{DD} and V_{SM} . The LPWD is constructed by dividing a single PMOS pull-up device into multiple PMOS pull-up devices in a binary manner (px1-px4) as shown in Figure 4.2. The source terminal of each PMOS pull-up device may connect to either V_{DD} or V_{SM} controlled by the programmable signals WID_0 to WID_3. During the write cycle, the WL level on the selected row is formed from the mixture of V_{SM} and V_{DD} . Meanwhile, the selected cell voltage is lowered from V_{SM} to V_{DD} to improve the write margin. During the read cycle, the cell voltage (V_{SM}) is higher than the periphery circuitry (V_{DD}) to prevent read and half-selected margin degradation from scaled V_{DD} . The limitation of this reported work is that it required two different power supply sources for V_{DD} and V_{SM} .

In [17], a self-write-back sense amplifier with capacitance separator was reported to improve the half-selected margin as shown in Figure 4.3. The purpose of capacitance separator was to reduce the overall parasitic capacitance from the core logic circuit to the bitline.

Figure 4.2: Reported level-programmable wordline driver (LPWD) and dynamic array supply control (DASC) [16].

Figure 4.3: Reported self-write-back sense amplifier [17].

As such, the bitline swings faster as compared to the conventional in the read cycle. The sense amplifier bitline (SABL) will start to swing when the bitline is low enough to open the capacitance separator. After that, SABL triggers the self-write-back sense amplifier and latching process is in place to determine the write-back data back to the SABL, bitline, and cell node. The disadvantage is the additional write-back power consumption under the worst-case scenario assuming write back is required for all of the half-selected cells on the selected row, which might not be friendly to be implemented for ultra-low voltage SRAM environment.

In [18], a suppress-coupling-signal negative bitline (SCS-NBL) is reported to improve the write margin as shown in Figure 4.4. A negative-bitline enable signal (ENB_NBL) pulse is generated during the write cycle through the replica bitline. After that, ENB_NBL signal propagated and becomes the coupling signal (NBL_FIRE). A stacked NMOS device is used to suppress the NBL_FIRE signal level below the power rail (V_{DD}) at the higher V_{DD} region. Coupled negative-bias signal (NVSS) is then generated by the falling edge of the NBL_FIRE signal coupled to the C1 capacitor to supply to the write driver. As a result, a negative bitline is generated on the selected column to improve the write margin of the SRAM.

Although many assist techniques have been reported in the literature, none of them enabled the 6T SRAM to operate at voltage levels as low as 0.7V to 0.5V. The most significant technique to realize ultra-low voltage SRAM design is by changing the structure of the conventional 6T SRAM bit cell. Thus, a myriad of SRAM cells with more transistors than the conventional 6T were proposed to achieve ultra-low voltage operation [96]. In [97], Takada K. has proposed a read disturb free asymmetric 7T cell. This bit cell structure enables the SRAM to be free from read disturb, but it makes the storage node to be data dependent floating and the adoption of asymmetric storage structure might not be litho-friendly during fabrication. Read disturb free 8T SRAM cell structure [86, 98–102] with a separate read port for decoupled read and write operation has demonstrated to be promising for operation in ultra-low voltage environment. However, it suffers from poor read bitline

Figure 4.4: Reported SCS-NBL write assist scheme [18].

sensing due to bitline leakage current. Besides 8T, read disturb free 9T and 10T SRAM cell structure [103–110] have also been proposed to achieve ultra-low voltage operation. Even though all of these proposed 7T ~ 10T SRAM cell structures are read disturb free and able to operate in ultra-low voltage, they still suffer from degraded write margin, poor read bitline sensing, and half-selected cell stability issue (HS-SNM).

4.3 Contributions

In this chapter, a 9T SRAM cell (6T write and 3T read ports) with CS-CVSS is proposed to (1) improve the HS-SNM and WM through CS-CVSS data-aware write assist (DAWA) for 6T write port, (2) improve the dynamic half-selected cell stability (Dynamic HS-SNM) of the 6T write port by leveraging write through virtual ground with 8 bitcell load and (3) enhanced read bitline sensing margin by a low leakage 3T read port with read through virtual ground.

4.3.1 Proposed 9T SRAM

Figure 4.5(a) depicts the proposed 9T bitcell. It consists of a 6T write port (PG1,2; PD1,2; PU1,2) and 3T read port (MR1,2,3). The pass gates (PG1, PG2) are controlled by write bitlines, WBL and WBLB. The source of PG1 and PG2 are shorted to form write virtual ground (WR_VGND) and the drain forms storage nodes, Q and QB. The pull-downs (PD1, PD2) have their source biased independently through CS-CVSS lines, CVSS1 and CVSS2. The pull-ups (PU1, PU2) and (PD1, PD2) form two pairs of inverters (INV1, INV2) with switching thresholds (VST1, VST2). The gate node of MR3 is controlled by MR1 and MR2 for leakage suppression and RBL sensing margin enhancement. L- and inverted L-shaped cell layouts (Figure 4.5(b)) are employed for high area efficiency. The architecture of the proposed SRAM macro is shown in Figure 4.6. The macro uses CS-CVSS DAWA comprising of a CVSS-UP voltage (VSSUP) generator and Data-aware CVSS-UP switching circuit. The following chapters will discuss the operation and benefits of the proposed 9T bitcell SRAM macro.

(a)

(b)

Figure 4.5: (a) Proposed 9T SRAM bitcell structure (b) L-shaped and inverted L-shaped cell layout

Figure 4.6: Proposed macro structure of 256 x 64 SRAM.

4.3.2 Column-Based Split Cell-VSS (CS-CVSS) and Data-Aware Write-Assist (DAWA)

The proposed SRAM macro in Figure 4.6 is implemented using a CS-CVSS: CVSS1 and CVSS2. 8:1 column muxing is used to share 8 column bitcells (BCs) WR_VGNDs. During the write operation, the half-selected cells on the selected column will experience half-selected disturbance instead of half-selected cells on the selected row due to the grounded WBLs/WBLBs. Also dynamic half-selected write disturbance is small for 9T cells on the small parasitic capacitance (8 BCs load) on WR_VGND compared to conventional 8T/dual-port-control (DSC) 6T cells [111–114] whose having a large half-selected write disturbance due to a high parasitic capacitance (256 BCs load) on WBL/WBLB (Figure 4.7). Moreover, Data-aware CVSS-UP switching circuit will clamp either CVSS1 or CVSS2 to VSSUP (>0) and other to 0 in the write operation for HS-SNM and write margin improvement which will be discussed later. Table 4.1 depicts the different level of VSSUP clamp voltages generated by the CVSS-UP voltage generator depending on EN, S1 and S0 configurations.

Figure 4.7: Simulation on the HS-SNM comparison between DSC6T, 8T, and proposed 9T with CVSS1/CVSS2.

Figure 4.8 delineates the write '0' operation for the selected column and selected cell

Figure 4.8: Proposed CS-CVSS scheme with DAWA.

Table 4.1: VSSUP configuration based on EN, S1 and S0 signal.

EN	S1	S0	VSSUP(CVSS1/CVSS2)
0	0	0	0
1	0	1	12% V_{DD}
1	1	0	15% V_{DD}
1	1	1	20% V_{DD}

Figure 4.9: Simulation on the proposed 9T SRAM HS-SNM-Q0, HD-SNM-Q1 and write margin (WM) as a function of CVSS1/CVSS2.

in the proposed SRAM macro. Firstly, the WBL and WBLB are loaded with data (WBL = V_{DD} , WBLB = 0V) on the selected column and its selected row WR_VGND is driven to '0'. At the same time, the data-aware CVSS-UP switching circuit configures the CVSS1 and CVSS2 to 0V and VSSUP respectively. By this configuration, VSSUP on CVSS2 weakens PU1 and elevates V_{ST1} of INV1 to improve the WM compared with CVSS is '0' on the selected cell. For half-selected cells, the precharged WR_VGNDs are kept floating. Half-selected cells with Q = '0' experience a voltage bump at Q node due to the disturbance current from floating WR_VGND. The half-selected cell static noise margin (HS-SNM-Q0) is improved in this case based on the VSSUP configuration earlier (CVSS2 = VSSUP) due to reduced strength of PD2 and elevated V_{ST2} of INV2. On the other hand, the half-selected

cell with $Q = '1'$ are free from half-selected disturbance current because of the same voltage level on $Q = WR_VGND = V_{DD}$ with PG2 off. Note that due to $CVSS = VSSUP$, the hold static noise margin (HD-SNM-Q1) is degraded. However, the degraded HD-SNM-Q1 is still far better than the HS-SNM-Q0. The proposed technique is a trade-off between HS-SNM-Q0 to HD-SNM-Q1. To better study and analyze the relation between WM, HS-SNMQ0, and HS-SNMQ1 due to the proposed DAWA scheme, a 10k Monte-Carlo samples simulated with statistical tail bit of the three parameters as a function of CVSS1/CVSS2 at near-threshold voltage, $V_{DD} = 0.5V$ is shown in Figure 4.9. The result indicated write margin and HS-SNM-Q0 is improved significantly with higher CVSS1/CVSS2, whereas HD-SNM-Q1 is degraded. As discussed earlier, HS-SNM-Q1 is still considered healthy (>0) even with $CVSS1/CVSS2 = 20\%V_{DD}$.

DSC6T vs. 9T (Tail bit: Monte-Carlo = 10K samples)

Figure 4.10: Simulation on the dynamic HS-SNM analysis with different bitcell loading.

To further substantiate the proposed 9T cell with 8 BCs load on WR_VGND possess better dynamic cell stability, the transient simulation setup from [115] is employed to ascertain its dynamic HS-SNM-Q0. Figure 4.10 portrays simulated Monte-Carlo, 10k samples tail bits static HS-SNM-Q0 (9T/DSC6T), dynamic HS-SNM-Q0 (9T; 8 BCs load) and dy-

8T vs. 9T (Tail bit: Monte-Carlo = 10K samples)

- HS-SNM-Q0 (SF@27C; WLUD@85% VDD; 8T)
- WM (SF@27C; WLUD@85% VDD; 8T)
- HS-SNM-Q0 (FS@27C; CVSS1/CVSS2=15% VDD; 9T)
- WM (SF@27C; CVSS1/CVSS2=15% VDD; 9T)

Figure 4.11: Simulation on 8T vs. 9T comparison for HS-SNM and write margin (WM) .

namic HS-SNM-Q0 (DSC6T; 256 BCs load). The 9T cell shows improvement of 55-60mV over DSC6T. Figure 4.11 compares the HS-SNM-Q0 and write margin for 8T with WLUD and proposed 9T with CS-CVSS DAWA. It shows that 9T is much more effective compared to 8T.

4.3.3 Proposed 3T Read Port for Enhanced RBL Sensing Margin

Read sensing margin is highly limited by I_{ON} -to- I_{OFF} ratio. This work proposes a novel 3T read port for substantial improvement in I_{ON} -to- I_{OFF} ratio. In the proposed 3T read port of the 9T cell, MR1 and MR2 controls MR3 gate. RWL is connected to MR1 and, MR3 drain and source are connected to RBL and read virtual ground (RD_VGND). When read is enabled (RWL = '1'; RD_VGND = '0'), the precharged RBL is conditionally discharged if QB = '1' as shown in Figure 4.12. If the read is disabled (RWL = '0'; RD_VGND = '0') then the MR3 gate to source voltage is V_{DD} independent of the data Q/QB resulting in a

huge saving in the read port leakage. The proposed 9T cell read port has data-independent leakage in contrast to the 8T cell. Figure 4.13 depicts the proposed 9T enhanced RBL sensing margin compared to the 8T RBL sensing margin in the worst case.

Figure 4.12: Principle of the proposed sensing margin technique.

A more comprehensive simulation of RBL swing (RBL1 (Read '1') - RBL0 (Read '0')) for 8T and 9T as a function of process and temperature with 256 cells per RBL at $V_{DD} = 0.3V$ is shown in Figure 4.14. 9T has enhanced RBL swing in contrast to 8T. Figure 4.15 portrays the simulated RBL swing in $\%V_{DD}$ as a function of the number of cells per RBL with temperatures, $27^{\circ}C$ and $80^{\circ}C$ at $V_{DD} = 0.3V$. At a high temperature of $80^{\circ}C$, 8T has negative RBL swing with 1024 cells per RBL compared to 9T due to significant read port

Figure 4.13: Sensing margin comparison between 8T and 9T.

leakage. Figure 4.16 clearly demonstrates that the proposed read port generates larger RBL swing and a wider sensing timing window than that of the 8T cell.

Figure 4.14: Simulation on the RBL swing of 8T and 9T at different process and temperatures.

Proposed 9T selected cell read '0' current for discharging RBL0 is less due to under-driven MR3 compared to 8T fully-driven footer. To ascertain timing performance, we evaluate read delay as RBL0 falling time from $100\%V_{DD}$ to $50\%V_{DD}$ for both 9T and 8T. Figure 4.17 demonstrates the read delay ratio of 9T over 8T versus V_{DD} with 256 cells per RBL at worst SS process. At near- or sub-threshold voltages, the read delay of 9T is more

Figure 4.15: Simulation of the RBL swing in %VDD for 8T and 9T on different RBL bitcells load.

Figure 4.16: Simulation of the RBL swing for 8T and 9T.

than 1.5x compared to 8T. Note that at $V_{DD} = 0.25\text{V}$; 27°C , the 9T read delay is about 1.7x compared to 8T at 27°C whose RBL swing is negligible to be sensed. Improvement in 9T read delay can be achieved by increasing the coupling capacitor between RWL and the internal gate node (N) of MR3.

Figure 4.17: Simulation of the read delay ratio comparison for 8T and 9T.

4.3.4 Test Chip and Measurement Results

A 16kb SRAM test chip has been fabricated in 28-nm FDSOI technology as shown in Figure 4.18. The test chip consists of the proposed 9T SRAM cells (256×64), RWL and WWL drivers, address decoder, the proposed DAWA and CS-CVSS circuitry, CS-CVSS voltage generator, and global control circuitry. A summary of the overall chip area including each functional block is also indicated in Figure 4.18.

Figure 4.19 illustrates the measured Schmoos plot for write and read, respectively, from the test chip. The Schmoos plot $V_{DD,MIN}$ measurement data was collected by stepping down the V_{DD} (10mV per step) on the SRAM cell and peripheral circuitries until one of the cell-

Technology	28-nm FDSOI CMOS
Memory Size	16 kbit
Total Chip Area	18124 μm^2
Overall Chip Area Breakdown	
SRAM Array	10648 μm^2
RWL & WWL Drivers	4121 μm^2
X & Y Decoders and Global Control Circuits	1009 μm^2
Data-Aware CVSS-UP Circuits & CMUXs	1281 μm^2
CVSS-UP Voltage Generators & IO	1065 μm^2
Measured Chip Performance	
$V_{DD, \text{MIN-READ}}$	250 mV
$V_{DD, \text{MIN-Write}}$	470 mV
E_{Read}	2.75 pJ @ 0.5V
E_{Write}	3.97 pJ @ 0.5V
E_{Total}	6.72 pJ @ 0.5V

Figure 4.18: Test chip micrograph and test chip summary.

s fail. For instance, to characterize the $V_{DD,MIN-Write}$, all the cells are firstly initialized with data '1'. Subsequently, the write operation was performed to write data '0' into all SRAM cells. A read operation was carried out after the write operation to determine the data in the cell. If one of the cell's data not '0', it was characterized as 'FAIL' on current V_{DD} setting. Otherwise, it would be a 'PASS'. The same characterization goes for $V_{DD,MIN-Read}$, i.e., all the cells were preloaded with data '0' and a read operation was performed to read the cell data. If the output data were not '0', it would be indicated as 'FAIL' and otherwise 'PASS'. Figure 4.19(b) depicts the $V_{DD,MIN-Read}$ of the proposed 9T, which can be as low as 250mV. Figure 4.19(a) proved that the proposed 9T achieved lower $V_{DD,MIN-Write}$ than the conventional 8T where the 8T $V_{DD,MIN-Write}$ was capped at 860mV. The proposed 9T cell with CVSS1/CVSS2 of $12\%V_{DD}$ enabled a $V_{DD,MIN-Write}$ at 760mV while CVSS1/CVSS2 of $15\%V_{DD}$ allowed further lowering of $V_{DD,MIN-Write}$ to 660mV. The lowest $V_{DD,MIN-Write}$ of 470mV is achieved by tuning the CVSS1/CVSS2 to $20\%V_{DD}$. As such, the proposed 9T with CS-CVSS scheme enabled the $V_{DD,MIN-Write}$ to be lowered to 470mV at CVSS1/CVSS2 of $20\%V_{DD}$ configuration, which translates to a 390mV improvement as compared to the 8T conventional. Note that the $V_{DD,MIN-Read}$ is lower than $V_{DD,MIN-Write}$. Therefore, no read failure occurred during the measurement of $V_{DD,MIN-Write}$.

Figure 4.20 depicts a measured waveform while reading data '0'. As expected, the read energy is decreasing with V_{DD} . However, the trend is only valid before V_{DD} goes into the subthreshold region. Once the V_{DD} is below the subthreshold region, the read delay increases exponentially. Correspondingly, the increase of read energy per operation cycle is also exponential after V_{DD} is below 400mV. The minimum energy point, 2.4pJ collected from the test chip measurement is, therefore at $V_{DD} = 400\text{mV}$. As discussed earlier, the V_{DD} on the proposed 9T is achieved as low as 250mV with a read access time of 1.57s and maximum operating frequency of 290kHz at the expense of high read energy, 6.1pJ.

Figure 4.21 depicts the measured write power and read power as a function of V_{DD} for the proposed design. Note that the write power is not shown below $V_{DD} = 500\text{mV}$ as

Figure 4.19: Test chip measurement of the Schmoos plot for (a) write operation (b) read operation.

Figure 4.20: Test chip measurement on read energy.

Figure 4.21: Test chip measurement on read and write power at frequency = 10MHz.

$V_{DD,MIN-Write} = 470\text{mV}$ due to the limited strength of the CVSS1/CVSS2 drivers in this design. The $V_{DD,MIN-Write}$ can be further lowered by using much stronger CVSS1/CVSS2 drivers. The total measured energy of read and write is shown in Figure 4.22. In this design, minimum energy considering successful read and write is found to be 6.72pJ at $V_{DD} = 500\text{mV}$. The total energy here is limited by the $V_{DD,MIN-Write}$, which can be improved by implementing a stronger CVSS1/CVSS2 driver.

A performance comparison table of the proposed 9T SRAM with similar reported works is shown in Table 4.2. In order to have a fair comparison, an 8T SRAM and a DSC6T SRAM were designed with the same technology. All the SRAM were constructed with 256×64 bitcells with 50% data '1' and 50% data '0'. Due to the structure of the proposed 9T cell, it is expected that the cell area is slightly larger than the 8T and DSC6T cell. With the reported and proposed write assist scheme on implemented on DSC6T and 9T respectively, it enables a lower operational V_{DD} than 8T and in the meantime improving the HS-SNM at the expense of HD-SNM on half-selected cells to improve the cell stability during the write operation. The cell HS-DNM on the write operation is further improved on the proposed

Figure 4.22: Test chip measurement on read and write energy.

Table 4.2: Test chip performance comparison.

	8T [112]	DSC6T [111]	9T (This Work)
Cell Size (comapred to conventional 6T)	1.25x	1x	1.45x
Write Assist	No	RS-VCSS + NBL - light	CS-CVSS
HS-DNM	Worst (256 BCs load)	Worst (256 BCs load)	Improved (8 BCs load)
Margin Trade-off	N/A	HS-SNM vs HD-SNM	HS-SNM vs HD-SMM
Read Delay	0.7x @ VDD = 0.5V Fail @ VDD = 0.25V	1x @ VDD = 0.5V Fail @ VDD = 0.25V	1.1x @ VDD = 0.5V 1x @ VDD = 0.25V
Read Energy*	1.15x @ VDD = 0.5V Fail @ VDD = 0.25V	1.23x @ VDD = 0.5V Fail @ VDD = 0.25V	1x @ VDD = 0.5V 1x @ VDD = 0.25V
Write Energy	Fail @ VDD = 0.5V	1.1x @ VDD = 0.5V	1x @ VDD = 0.5V
Write Operation	Only CLK ON period	CLK ON & OFF period	Only CLK ON period
*256 × 64 SRAM with data: 50% 1-cells, 50% 0-cells @27°C			

9T over DSC6T due to the bitline implementation structure. As a result, the proposed 9T ($1\times$ @ $V_{DD} = 0.5V$) has a better write energy performance than DSC6T ($1.1\times$ @ $V_{DD} = 0.5V$) whereas 8T failed completely at $V_{DD} = 0.5V$. Note that the DSC6T required a full clock cycle (ON & OFF period) to complete the write operation, which might be one of the limitations to allow a higher operating frequency than that of the proposed 9T. As for read performance, the proposed 9T showed the highest read delay among the 8T and DSC6T. This is because of the 3T read port, which required more time to discharge the bitline as discussed in chapter 4.3.3. The advantage of the 3T read port is that it enables an incredibly low $V_{DD,MIN-Read}$ and read energy. Its read energy is 15% and 23% lower than the 8T and DSC6, respectively. More importantly, both 8T and DSC6 failed to read at 0.25V while the proposed 9T is able to read at such low V_{DD} .

4.4 Summary

A novel 9T cell structure with CS-CVSS data-aware write-assisted scheme with enhanced read sensing margin in 28-nm FDSOI technology is demonstrated to operate in ultra-low voltage. The proposed data-aware write-assisted scheme controlled the CVSS1 and CVSS2 voltage of SRAM bitcell in the selected column during the write operation to improve the write margin and enhanced the half-selected cell stability to prevent data loss in the half-selected cells due to unwanted write disturbance. The measurement results demonstrated a $V_{DD,MIN-Write}$ of 390mV lower than that of 8T SRAM. The proposed 3T read port also demonstrated a much larger sensing window and achieved a $V_{DD,MIN-Read}$ of 250mV in the measurement due to suppressed leakage.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

SRAM is a widely used embedded memory in modern SoCs. It is difficult to achieve low voltage operation in SRAM with the conventional 6T SRAM bitcell especially without any assist schemes due to the degraded cell stability, poor read and write margins, and exponentially increased sensitivity to PVT fluctuation. Moreover, the BTI degradation in SRAM cells is unavoidable even in the standby mode due to the use of bistable latching circuitry. This further deteriorates the cell stability in scaled voltage environment. This thesis focused on the design of an ultra-low voltage and BTI-aware SRAM to address these issues.

To address the half-selected cell stability due to BTI degradation on the write operation, a BTI-aware stability monitor circuit is proposed and fabricated in 28-nm FDSOI technology. The circuit used replica row cells to monitor the worst-case BTI degradation caused data flip in SRAM cell. If any data flip occurred in the replica row on the pre-calibration phase, the circuit will then automatically adjust a suitable lower WWL voltage level (in the pre-defined range) in the subsequent write operation. This lower WWL voltage level will improve the degraded half-selected cell stability to prevent data flip due to BTI degradation. A two-phase write operation assist technique is also proposed to cater the possible worst-case write failure on the tail bitcell due to lowering WWL voltage level.

The two-phase write operation under drive the WWL in phase I to control half-selected cell stability and raise WWL to V_{DD} level in phase II for write margin improvement without degrading the half-selected cell stability. The detailed measurement of the 16kb SRAM macro with the proposed BTI-aware stability monitor circuit proven effective to reduce the half-selected cell failure from 57.13% to 0% after long BTI stress. The proposed monitor circuit consumed additional 3.42% power and 10% area overheads.

A 9T ultra-low voltage SRAM with CS-CVSS data-aware write-assisted scheme and enhanced read sensing margin is proposed and fabricated in 28-nm FDSOI technology. The proposed 9T bitcell decoupled the read and write operation, in which eliminated the read disturbance as compared to conventional 6T SRAM bitcell. CS-CVSS data-aware write-assisted scheme helps to improve the write margin on the selected cell and half-selected cell stability respectively through the CVSS1 and CVSS2 voltage control in the bitcell. The 3T read port in the proposed 9T bitcell provides data-independent leakage and thus, generates larger RBL swing as compared to conventional 8T bitcell, therefore improving the RBL sensing margin. Measurement results on the 16kb SRAM test chip demonstrated a $V_{DD,MIN-Write}$ of 470mV and $V_{DD,MIN-Read}$ of 250mV. The measured energy of 6.72pJ is achieved at 0.5V.

5.2 Future Work

5.2.1 BTI-aware Stability Monitor Circuit in SRAM

BTI aging is predicted to be the dominant reliability issue and limits the SRAM lifetime for current and in the future. This can be foreseen through the rapidly growing on electronics devices in the automotive area where reliability is a high design priority. Furthermore, surveillance devices that can operate in any environments where reliability is also an important factor to ensure the robustness. Therefore, BTI degradation caused the reliability issue in these SoCs where reliability is the design priority is not allowed.

The conventional solution to handle BTI degradation in SRAM cell is still based on

margin reservation where device sizing is the key to preserving the required operational margin for the SRAM lifetime. Note that SRAM cells are typically designed in the way of using minimum transistor size to increase the integration level. Therefore, the conventional approach is not applicable to resolve the BTI degradation. As such, extensive research works have been carried to explore more circuit solution to mitigate or compensate the BTI degradation in SRAM cell. However, none of the reported works produced an all in one circuit solution (BTI monitoring and mitigation circuit) with silicon validation for BTI degradation in SRAM cell. Consequently, the proposed BTI-aware stability monitor circuit design presented in Chapter 3 is applicable and simple to implement into automotive or surveillance SoCs SRAM block to offer the robustness by monitoring and mitigating the BTI degradation in SRAM cell.

The current proposed BTI-aware stability monitor circuit design in Chapter 3 required pre-calibration to determine the right WWL voltage level to prevent data flip in SRAM cell due to BTI degradation when the SRAM is not in operation. To further improve the proposed design, the architecture can be modified to automate the calibration internally without relying on non-operating cycle. This can be achieved by separating the WBL and WBLB of the replica row to the SRAM core cell. Note that the bitline loading effect also plays an important part in the half-selected disturbance. Therefore, careful design the half-selected disturbance in the replica row through WBL and WBLB is required to mimic the actual SRAM cell environment.

Another possible challenge is the implementation of current BTI-aware stability monitor into FinFET technology. The FinFet device layout drawing is purely different to the conventional bulk devices. The device's orientation is an important factor in FinFet where it only allows one orientation. Therefore, transferring layout drawing from conventional bulk into FinFet may incur additional area overhead. Good floor planning ahead is required to maintain or reduces the area overhead of the proposed circuitry.

5.2.2 Ultra-low Voltage SRAM

Ultra-low voltage SRAM is the growing research topic due to their wide application in power- and energy- constrained intelligent wearable devices, Internet of things (IoT) and advance health care SoCs. There have been numbers of new SRAM bitcell structures and assist techniques reported in the literature. Those reported bitcells and assist techniques optimized the SRAM parametric and allow it to operate in ultra-low voltage regime. However, those bitcells and assist techniques have their advantages and disadvantages.

The proposed column-based split cell-VSS and data-aware write-assist technique in Chapter 4 offers a lower $VDD_{MIN-Write}$, write energy and improved half-selected cell stability during the write operation for ultra-low voltage SRAM. Therefore, these write-assist techniques can be widely adopted into any ultra-low SRAM domain such as wearable and portability devices where operational battery time is the priority concern. Furthermore, the proposed 3T read port provides lesser read energy and lower $VDD_{MIN-Read}$ which further enable for ultra-low voltage operation.

The future enhancement of the proposed CS-CVSS and data-aware write-assist technique can focus on further lowering the $VDD_{MIN-Write}$ where currently it is the limiting factor to allow further voltage scaling. This can be achieved by enhancing the driver strength on CVSS1/CVSS2. Other write assist technique such as cell voltage collapse during the write operation can be implemented with the proposed write assist technique in achieving a much lower $VDD_{MIN-Write}$.

APPENDIX A

Author's Publication

A.1 Journal Papers

1. A. Do, **Z. C. Lee**, B. Wang, I. J. Chang, X. Liu and T. T. H. Kim, "0.2 V 8T SRAM With PVT-Aware Bitline Sensing and Column-Based Data Randomization," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 6, pp. 1487-1498, 2016.
2. A. Do, C. Yin, K. Velayudhan, **Z. C. Lee**, K. S. Yeo, and T. T. H. Kim, "0.77 fJ/bit/search Content Addressable Memory Using Small Match Line Swing and Automated Background Checking Scheme for Variation Tolerance," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1487-1498, 2014.
3. **Z. C. Lee**, K. C. Leong, Z. H. Kong, and T. T. H. Kim, "NBTI/PBTI-Aware WWL Voltage Control for Half-Selected Cell Stability Improvement," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 9, pp. 602-606, 2013.
4. T. T. H. Kim, **Z. C. Lee**, and A. Do, "A 32kb 9T Near-threshold SRAM with Enhanced Read Ability at Ultra-low Voltage Operation," submitted to *Solid-State Electronics (SSE)*.

A.2 Conference Papers

1. **Z. C. Lee**, M. Sultan. M. Siddiqui, Z. H. Kong, and T. T. H. Kim “An 8T SRAM with BTI-Aware Stability Monitor and two-phase write operation for cell stability improvement in 28-nm FDSOI,” in *Proc. IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 437-440, 2016.
2. A. Do, **Z. C. Lee**, B. Wang, I. J. Chang, and T. T. H. Kim “0.2 V 8T SRAM with improved bitline sensing using column-based data randomization,” in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 141-144, 2014.
3. **Z. C. Lee**, K. M. Ho, Z. H. Kong, and T. T. H. Kim “NBTI/PBTI-aware wordline voltage control with no boosted supply for stability improvement of half-selected SRAM cells,” in *Proc. IEEE International SoC Design Conference (ISOCC)*, pp. 200-203, 2012.

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