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A New Unified Model for Channel Thermal Noise of Deep Sub-micron RFCMOS

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Abstract — A new unified model for circuit simulation is presented to predict the high frequency channel thermal noise of deep sub-micron MOSFETs in strong inversion region. Based on the new channel thermal noise model, the simulated channel thermal noise spectral densities of the devices fabricated in a 0.13μm RFCMOS technology process are compared to the channel noise directly extracted from RF noise measurements.

Index Terms — Channel thermal noise, high-frequency noise modeling, mobility degradation, MOSFET, noise of deep sub-micron MOSFET, vertical electric field.

I. INTRODUCTION

MOSFETs have become increasingly attractive solution for application in integrated high frequency analog electronics and wireless communication due to its high unity-gain frequency while being cost effective. Nevertheless, a great challenge remains in the design of RF circuits for real products due to the noise that leave very little margins for the RF IC designer [1]. Therefore, an accurate model predicting the noise performance of the CMOS in RF circuits is crucial in order to reduce design cycles.

The main focus in this work is on the channel thermal noise which is the most dominant noise source in short channel MOSFETs. It is often observed that the long channel noise theory is inadequate to predict the channel thermal noise of short channel MOSFETs [2, 3]. Some approaches have been presented to explain the origin of this excess noise by introducing the extra noise generated by velocity saturation effect [4-8], hot carrier effect [4, 5, 7-9] and channel length modulation effect [10].

In this work, a new unified channel thermal noise model, which includes the drain bias and channel length dependent mobility degradation effect, is presented and verified with measured data extracted from noise measurement. The mobility degradation effect is discussed in section II, while the channel thermal noise model is elaborated in section III. The measurement setup is discussed in section IV. Comparisons were made in section V between the model and the measurement data.

II. MOBILITY DEGRADATION EFFECT

The mobility degradation occurs when the carriers are pulled by the vertical electric field towards the Si-SiO₂ (silicon-silicon dioxide) interface, which is rough due to the imperfection of oxide layer. The average vertical electric field can be related to inversion layer charge and depletion charge by [11]

$$E_{eff} = \frac{1}{2}(E_{x,surface} + E_{x,bulk}) = \frac{1}{\epsilon_{Si}}\left(\frac{Q_{inv}}{2} + Q_B\right) \quad (1)$$

where Q_{inv} is the inversion layer charge, and Q_B is the depletion layer charge. The mobility reduction due to vertical field effect is included inside the effective mobility model, which can be approximated by [11]

$$\mu_{eff} = \frac{\mu_0}{\sqrt{1 + \alpha_0 E_{eff}^2}} \quad (2)$$

where μ_0 is the low-field surface mobility, and α_0 is fitting parameter.

Conventionally, one of the assumptions made in the effective mobility model is that the drain bias dependency in the model is negligible, and thus the model can be approximated by [11, 12]

$$\mu_{eff,conventional} = \frac{\mu_0}{1 + \theta_1 V_{GT}} \quad (3)$$

where $V_{GT} = V_{GS} - V_{TH}$, V_{TH} is the threshold voltage, and θ_1 is fitting parameter.

However, as channel length scaled down, the effective vertical electric field will increase and the dependency on the drain bias is no longer negligible. As drain bias increases in the short channel devices, inducing more depletion charge and lowering the barrier to turn on the devices, the inversion layer charge and depletion layer charge increases. The average electric field is enhanced by the drain bias causing the further degradation of the carrier mobility. Thus, the drain bias dependency in the effective mobility model should be taken into account for short channel devices, such as deep sub-micron MOSFETs. The effective mobility model is thus approximated by

$$\mu_{eff,proposed} = \frac{\mu_0}{\sqrt{1 + (\theta_1 V_{GT})^2 + [(1 - 2L'_{total})V_{DS}]^2}} \quad (4)$$

where $L'_{total} = L_{total} \times 10^6$, and L_{total} is the total channel length. The model is valid for $L_{total} \leq 0.50\mu m$. If the total channel length or drawn channel length L_{total} is larger than $0.50\mu m$, the effect of drain bias on the mobility can be neglected and thus the conventional effective mobility model is still valid. The comparison between the channel thermal noise model with the conventional mobility approximation and the channel thermal noise model utilizing the proposed effective mobility equation is presented in section IV.

III. CHANNEL THERMAL NOISE MODEL

In this paper, the calculation of channel thermal noise is based on a two-section channel model, in which the channel of MOSFET is divided into two regions. Region I is the gradual channel region with length of $L_{eff} = L_{total} - \Delta L$, while region II is the velocity saturation region with length of ΔL . The length of velocity saturation region can be calculated by [3, 10]

$$\Delta L = \frac{1}{\alpha} \ln \left[\frac{\alpha(V_{DS} - V_{DSat}) + E_D}{E_c} \right] \quad (5)$$

with

$$E_D = E_c \sqrt{1 + \left[\frac{\alpha(V_{DS} - V_{DSat})}{E_c} \right]^2} \quad (6)$$

and

$$\alpha = \lambda \sqrt{\frac{3}{2} \frac{C_{ox}}{x_j \epsilon_{si} \epsilon_0}} \quad (7)$$

where E_c is the critical electric field where carriers travel at their saturation velocity, C_{ox} is the oxide capacitance per unit area, x_j is the junction depth of source and drain, and λ is the channel length modulation coefficient which is obtained from drain current versus drain voltage curve. For long channel devices, the length of the gradual channel region is close to the total channel length or the drawn length L_{total} . However, the channel length modulation effect becomes more significant due to the continued down-scaling of MOSFET and thus its effect need to be considered in short channel devices.

The channel thermal noise for MOSFETs is derived based on Nyquist theory and DC model of MOSFET [11].

$$S_{i_d} = 4kT \frac{\mu}{L_{total}^2} (-Q_{inv}) \quad (8)$$

with

$$Q_{inv} = -WL_{total}C_{ox}(V_{GS} - V_{TH}) \left[\frac{2}{3} \left(\frac{1+\eta+\eta^2}{1+\eta} \right) \right] \quad (9)$$

and

$$\eta = \begin{cases} 1 - \frac{V_{DS}}{V_{DSat}}, & V_{DS} \leq V_{DSat} \\ 0, & V_{DS} > V_{DSat} \end{cases} \quad (10)$$

where V_{DSat} is the drain saturation voltage, and μ is the constant carrier mobility.

In long channel devices, one of the common assumptions is the carrier in channel moving in a constant mobility. However, this assumption is no longer valid for short channel devices since the mobility degradation due to vertical field becomes significant. Therefore, the effective mobility should be included in the channel thermal noise model. Besides, the velocity degradation due to lateral field is assumed to be negligible since the electric field in the y-direction is much lesser than the critical electric field for most of the sections in the channel. On the other hand, according to [10], there is no current noise generated in the velocity saturation region. Consequently, the channel thermal noise spectral density is only contributed by the fluctuations along the gradual channel region. Hence, the channel thermal noise is calculated with the gradual channel region length L_{eff} instead of the total channel length L_{total} . Thus, the proposed channel thermal noise model is

$$S_{i_d} = 4kT \frac{\mu_{eff}}{L_{eff}^2} (-Q_{inv}) \quad (11)$$

with

$$Q_{inv} = -WL_{eff}C_{ox}(V_{GS} - V_{TH}) \left[\frac{2}{3} \left(\frac{1+\eta+\eta^2}{1+\eta} \right) \right] \quad (12)$$

IV. MEASUREMENTS

In this paper, the device under test (DUT) and OPEN structures were fabricated using Chartered Semiconductor Manufacturing Ltd's $0.13\mu m$ RFCMOS technology process. The devices measured are NMOS transistors, with the number of finger N_F is fixed at $N_F = 4$, while the channel width per finger W' is varying such that $W' = 1\mu m, 2\mu m$ and $5\mu m$. The channel length L is varying also, with $L = 0.13\mu m, 0.25\mu m$ and $0.50\mu m$. On wafer noise measurement was performed using ATN NP5B Microwave Noise Parameter System and HP8510 network analyzer. The frequency of 2GHz to 25GHz is used in this paper, while the gate biases is from 0.4V to 1.2V and drain biases is from 0.6V to 1.2V.

In order to minimize the errors due to interconnect parasitic and pad parasitic, the measurement data obtained were de-embedded [13]. After that, the de-embedded data was processed using the noise correlation matrix method to extract the power spectral density of channel thermal noise S_{i_d} , which will be used for comparison in the next part of paper.

Fig.1 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus drain bias characteristic of the NMOS with channel width $W = 4 \times 5 \mu\text{m}$ and channel length $L = 0.13 \mu\text{m}$, at 5GHz, biased at gate bias of 0.4 V, 0.8 V, and 1.2 V.

Fig.2 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus drain bias characteristic of the NMOS with channel width $W = 4 \times 5 \mu\text{m}$ and channel length $L = 0.50 \mu\text{m}$, at 5GHz, biased at gate bias of 0.4 V, 0.8 V, and 1.2 V.

Fig.3 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus drain bias characteristic of the NMOS with channel width $W = 4 \times 5 \mu\text{m}$ and channel length $L = 0.13 \mu\text{m}$, $0.25 \mu\text{m}$, $0.50 \mu\text{m}$, at 5GHz, biased at gate bias of 1.2 V.

Fig.4 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus drain bias characteristic of the NMOS with channel width $W = 4 \times 1 \mu\text{m}$, $4 \times 2 \mu\text{m}$, and $4 \times 5 \mu\text{m}$, and channel length $L = 0.13 \mu\text{m}$, at 5GHz, biased at gate bias of 1.2 V.

V. RESULTS AND DISCUSSIONS

The effect of the conventional effective mobility model in (3) and the proposed effective mobility model in (4) on the channel thermal noise in (11) across drain biases for different channel lengths and gate biases are illustrated in Figs. 1 to 3. The “proposed model” denotes the model using (11) and including effect of (4), while the “conventional model” indicates the model using (11) and including effect of (3). For longer channel length, the improvement on channel thermal noise prediction due to the proposed model is not significant, as indicated in Fig. 2. As the channel length scaled down, it can be observed that the conventional channel thermal noise model failed to predict the drain bias dependency of channel thermal noise. Only by including the proposed effective mobility

equation in the channel thermal noise model, the model can predict the drain bias dependency more accurately for deep sub-micron device, as shown in Fig. 1. Thus, as shown in Fig. 3, it can be concluded that as channel length shrinks, the improvement on the accuracy of the channel thermal noise model become more prominent by including the proposed mobility reduction due to additional drain bias and channel length dependency.

In order to verify the scalability of the channel thermal noise model, the proposed model is also investigated across different channel length in Fig. 3, across different channel width in Fig. 4, across different frequencies in Fig. 5 and across different gate biases in Fig. 6. From Figs. 3 to 6, it can be concluded that the proposed model is scalable across different channel lengths, channel widths, frequencies, gate biases and drain biases.

Fig.5 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus frequency characteristic of the NMOS with channel width $W = 4 \times 5 \mu\text{m}$ and channel length $L = 0.13 \mu\text{m}$, $0.25 \mu\text{m}$, and $0.50 \mu\text{m}$, at gate bias of 1.2V and drain bias of 1.2V.

Fig.6 Extracted (symbols) and Simulated (lines) spectral density of the channel thermal noise versus gate bias characteristic of the NMOS with channel width $W = 4 \times 5 \mu\text{m}$ and channel length $L = 0.13 \mu\text{m}$, $0.25 \mu\text{m}$, and $0.50 \mu\text{m}$, at 5GHz, biased at drain bias of 1.2V.

VII. CONCLUSION

In this paper, a new unified model of high frequency channel thermal noise in deep sub-micron MOSFETs for strong inversion region is presented. The model includes the drain bias and channel length dependent mobility degradation effect and channel length modulation effect. The proposed model has been verified with data extracted from noise measurements and found to agree well. We found that the effect of drain bias term in the mobility model can improve the accuracy of the channel thermal noise model in shorter channel device. By using this channel thermal noise model with the proposed effective mobility, the deep sub-micron MOSFET noise

performance can be predicted for different channel length, channel width, frequencies, gate biases and drain biases without complex calculation. Thus this model is scalable and can be easily implemented by IC designer in a simulation environment.

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