Integration of TaOx-based resistive-switching element and GaAs diode

Chi, Dong Zhi; Xu, Z.; Tong, X.; Yoon, S. F.; Yeo, Y. C.; Dalapati, G. K.; Chia, Ching Kean

2013

Xu, Z., Tong, X., Yoon, S. F., Yeo, Y. C., Chia, C. K., Dalapati, G. K., et al. (2013). Integration of TaOx-based resistive-switching element and GaAs diode. APL Materials, 1(3), 032121-.

https://hdl.handle.net/10356/79340

https://doi.org/10.1063/1.4820421

Integration of TaOx-based resistive-switching element and GaAs diode

Z. Xu, X. Tong, S. F. Yoon, Y. C. Yeo, C. K. Chia, G. K. Dalapati, and D. Z. Chi

Citation: APL Materials **1**, 032121 (2013); doi: 10.1063/1.4820421
View online: http://dx.doi.org/10.1063/1.4820421
View Table of Contents: http://scitation.aip.org/content/aip/journal/aplmater/1/3?ver=pdfcov
Published by the AIP Publishing

APL MATERIALS **1**, 032121 (2013)

Integration of TaO_x-based resistive-switching element and GaAs diode

Z. Xu,[1,a] X. Tong,[2] S. F. Yoon,[1] Y. C. Yeo,[2] C. K. Chia,[3] G. K. Dalapati,[3] and D. Z. Chi[3]

[1]*School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798*

[2]*Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576*

[3]*Institute of Materials Research Engineering (IMRE), Agency for Science, Technology and Research (A*STAR), 3 Research Link, Singapore 117602*

(Received 15 May 2013; accepted 24 June 2013; published online 24 September 2013)

We report the integration of one selection diode and one resistive-switching memory element (1D1R) structure based on a GaAs diode on germanium-on-insulator on a Si substrate integrated with Cr/TaOx/Al memory element. The 1D1R device showed unipolar resistive-switching with an ON/OFF resistance ratio of over 10^2 within the voltage range 1.1 V–2.0 V. In the low resistance state, a forward-to-reverse current ratio of 60 was obtained at ±1 V. [http://dx.doi.org/10.1063/1.4820421]

The resistive random-access memory (ReRAM) is an emerging non-volatile memory with the potential to overcome the limitations of the Flash memory. The ReRAM has attributes such as a simple structure, high scalability, low power consumption, and CMOS process compatibility.[1] To date, many transition metal-oxides have been reported as resistive-switching material such as HfO_x,[2] TiO_x,[3] NiO_x,[4] and TaO_x.[5–7] TaO_x-based ReRAM has shown highly reliable performance because of its small Gibbs energy of the reduction and oxidation reaction.[5]

To achieve high-density integration, the ReRAM may be integrated in a crossbar architecture or in a three-dimensional architecture. Using the resistive-switching memory element alone in such architectures suffers from the crosstalk problem due to sneak paths through neighbouring cells.[8] One solution is to integrate a selection device such as a diode. The selection diode has to provide a sufficiently high rectifying ratio for the suppression of the leakage current. The poly-Si diode used in phase-change memory has shown a high forward current density and a high rectifying ratio.[9] The major drawback is the very high temperature in the silicon crystallization process.[10] We propose to use the GaAs in the selection diode which has a much lower processing temperature and higher carrier mobility.

In this study, we integrated a Cr/TaO_x/Al ReRAM device with a GaAs diode grown on germanium-on-insulator (GeOI) on a Si substrate. The standalone one resistive-switching memory element (1D1R) device was fabricated by standard photolithography process and its resistive-switching behavior is examined.

Structure preparation: The GaAs diode structure was grown by the solid-source molecular beam epitaxy (MBE) technique on a 2 cm × 2 cm GeOI/Si substrate. The substrate consisted of a 70 nm *p*-type Ge 10° off-cut towards the ⟨111⟩ plane on top of a 100 nm SiO_2 layer on the Si host substrate. Prior to the growth, the GeOI/Si substrate was cleaned by being briefly rinsed in a diluted HF solution (HF:H_2O in a 1:10 ratio) and a diluted H_2O_2 solution (H_2O_2:H_2O in a 1:10 ratio). In the MBE chamber, the substrate was degassed at 350 °C and was heated to 640 °C to desorb the

[a]Author to whom correspondence should be addressed. Electronic mail: n060042@e.ntu.edu.sg

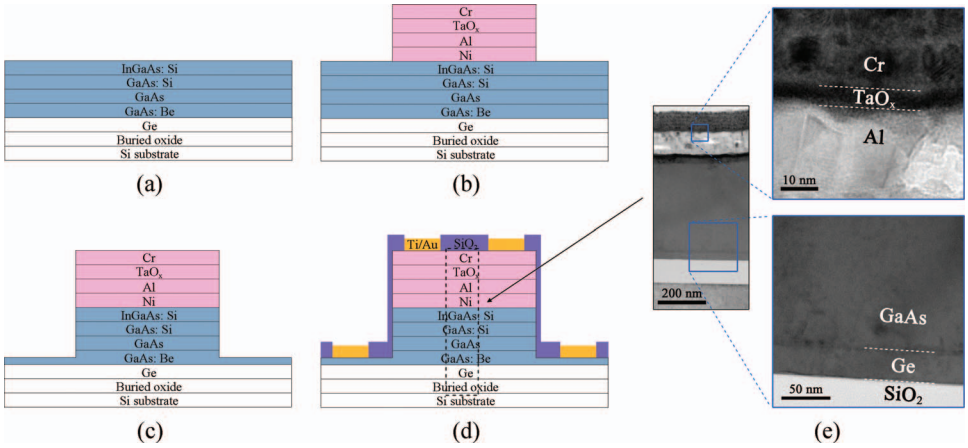

FIG. 1. Illustration of the process flow for 1D1R integration. (a) Growth of the GaAs diode structure on the GeOI/Si substrate. (b) Memory element sputtering and lift-off. (c) GaAs diode etching. (d) Surface passivation and metallization. (e) Cross-sectional TEM images from the device fabricated.

surface oxide and to create double-atomic steps on the Ge surface. The double-atomic steps on the Ge surface help to eliminate the anti-phase domains (APDs) in the subsequent GaAs growth.[11]

A 10-monolayer migration-enhanced epitaxy of GaAs was grown first at approximately 250 °C at an effective rate of 0.1 μm/h as a seeding layer. The subsequent GaAs diode layers were grown at a standard growth temperature of 580 °C at 1 μm/h. The diode consists of a 150 nm *p*-type GaAs layer doped with Be at a concentration of 1×10^{19} cm^{-3}, a 100 nm un-doped GaAs layer, and a 50 nm *n*-type GaAs layer doped with Si at a concentration of 6×10^{18} cm^{-3}. A 15 nm InGaAs layer was grown as a capping layer with the same Si doping concentration, as illustrated in Fig. 1(a).

The surface of the sample was then patterned with a photoresist to define the location of the memory element. The memory element was sputtered onto the sample at room temperature. Prior to the deposition of the 100 nm Al bottom electrode used in the one-resistor (1R) structure,[6] a 10 nm Ni layer was deposited to form an Ohmic contact with the InGaAs layer. The thickness of the TaO_x layer was 8 nm using the Ta_2O_5 sputter target. The Cr top electrode was 100 nm thick.

Device fabrication: The 1D1R device fabrication was performed using the standard photolithography process. The mesa of the 1R cell was formed using a lift-off step after the sputtering [Fig. 1(b)]. The GaAs layers were etched down to the bottom contact layer using a H_2SO_4:H_2O_2:H_2O (1:5:200) solution. The 1R cell was used as the etch mask in the wet etching step [Fig. 1(c)]. The sample surface was passivated with a 400 nm SiO_2 layer. Finally, contact pads consisting of Ti (50 nm)/Au (200 nm) were deposited using electron-beam evaporation, and patterned by lift-off [Fig. 1(d)]. The 1D1R samples were annealed at 330 °C and 360 °C for 1 min to reduce the contact resistance.

The cross-sectional transmission electron microscopy (TEM) images [Fig. 1(e)] show the Cr/TaO_x/Al memory on the GaAs diode stack. A minimal number of APDs are found at the GaAs/Ge interface. These APDs are expected to self-annihilate in pairs within approximately 100 nm[11] in the GaAs layer. Therefore, they should not propagate into the junction region of the diode.

The current-voltage characteristics were measured by an Agilent Semiconductor Parameter Analyzer HP4156B at room temperature. The top electrode of the memory element was grounded, and the voltage of the bottom contact pad connected to the *p*-type GaAs layer was swept. A positive voltage forward biases the diode of the 1D1R structure. In the 1D1R and 1R structures, the as-fabricated memory element was in a high-resistance state (HRS). It was switched to a low-resistance state (LRS) by an initial voltage sweep with a current compliance. During this "forming process," the oxygen vacancies form conducting filament(s) in the TaO_x layer.[6,12] The corresponding voltage that forms the conducting filament(s) is V_{FORM}. After the forming process, the device at the LRS can be reset to a HRS by applying a voltage sweep to the threshold voltage, V_{RESET}, without current compliance. In unipolar resistive-switching, this reset process is dominated by thermally assisted

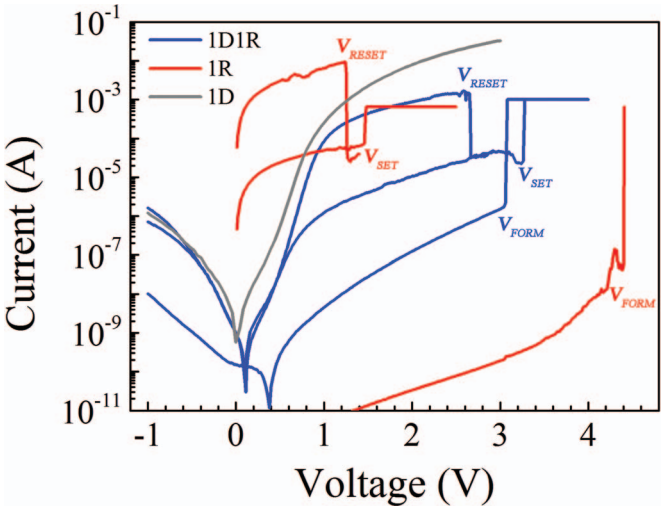

FIG. 2. Current-voltage characteristics for the 1D1R, 1R, and 1D devices (normalizing to a device with a mesa diameter of 90 μm).

local re-oxidation (Joule heating),[12,13] which ruptures the conducting filament(s). After the reset process, the device can be set to a LRS by sweeping to the threshold voltage, V_{SET}, which re-links the ruptured filament(s). During the measurement, the compliance current for the set and forming process was limited to 1 mA.

Figure 2 shows the current-voltage characteristics for the 1D (GaAs diode on GeOI/Si), 1R (Cr/TaO_x/Al on SiO_2/Si), and integrated 1D1R (annealed at 330 °C) devices having the same mesa diameter of 90 μm. The 1D and 1D1R devices had the same diode structure, while the 1R and 1D1R devices had the same memory structure. It should be noted that the 1D and 1D1R devices were fabricated using similar processes while the 1R device was fabricated separately.

GaAs diode on GeOI/Si: The 1D structure showed typical rectifying characteristics. The turn-on voltage was about 0.7 V. The forward-to-reverse current ratio was typically 4.5×10^2 at ± 2 V. The forward current densities were 276 A/cm^2 and 508 A/cm^2 at 2 V and 3 V, respectively. In the reverse bias condition, the leakage current density at -1 V was 0.018 A/cm^2, which is lower than what was reported in an earlier work (1.90 A/cm^2) using a similar layer structure.[14] The improvement resulted from the thicker bottom GaAs layer (150 nm versus 80 nm), which acted as a buffer layer. Therefore, the junction is less affected by imperfections at the GaAs/Ge interface.

Cr/TaO_x/Al memory element and 1D1R integration: The forming voltages for the 1R and 1D1R devices were 4.4 V and 3.08 V, respectively. The higher forming voltage indicates that TaO_x in the 1R structure had a better dielectric quality through sample preparation. For the 1R device, the set and reset voltages were ~1.47 V and ~1.25 V, respectively (the reset current was 5.25 mA). In the LRS, the 1R device had a higher current than the 1D device had in the forward bias region. This indicates that, in the 1D1R integrated structure, the forward current was limited by the diode.

For the 1D1R device, the set and reset voltages were ~3.28 V and ~2.65 V, respectively. These voltages are higher than the set and reset voltages of the 1R alone. This is due to the voltage drop across the resistance from the diode. However, the 1D1R device had a lower reset current of 1.46 mA. When the V_{RESET} is higher, the reset current required is lower since the reset process is dominated by Joule heating ($\sim I_{RESET}{}^2 * R$).[12] In the LRS state, the 1D1R device had a similar leakage current as the 1D device had. This suggests that the diode suppressed the current flow through the memory element. The forward-to-reverse current ratio was ~60 at ± 1 V for the 1D1R device annealed at 330 °C.

The equivalent circuit for the Cr/TaO_x/Al memory element is a resistor in parallel with a parasitic capacitor. The capacitance ($C = (\varepsilon_r \cdot \varepsilon_0 \cdot A)/d$) is approximated to be 176 pF, where ε_r (25) is the dielectric constant of Ta_2O_5, ε_0 (8.854×10^{-12} F/m) is the vacuum permittivity, A is the area of the 1D1R, and d is the thickness of TaO_x layer. Similarly, the capacitance from the intrinsic layer

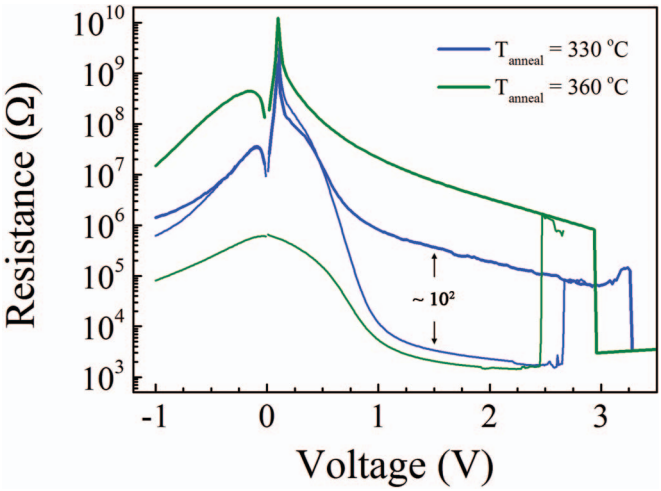

FIG. 3. Resistance-voltage characteristics for 1D1R devices under different post-annealing temperatures.

of the GaAs diode is about 7 pF. During the current-voltage measurement, the voltage was slowly swept from −1 V to V_{SET} in approximately 2 V/s. The transient current ($i = C \cdot dV/dt$) flowing through the parasitic capacitance of TaO_x layer was 0.35 nA which was negligible as compared with the current flowing through the conducting filament(s).

1D1R resistance characteristics: Figure 3 shows the resistance-voltage characteristics for the same 1D1R devices annealed at two different temperatures. For the device annealed at 330 °C, the HRS and LRS resistances were 370 kΩ and 3.3 kΩ at 1.5 V. The HRS/LRS resistance ratio was above 10^2 within the voltage range 1.1 V–2 V. The 1D1R device annealed at 360 °C had HRS and LRS resistances of 7.5 MΩ and 2.1 kΩ at 1.5 V. It showed a higher HRS/LRS resistance ratio of above 3×10^3 within the voltage range 0.9 V–1.7 V.

Under the reverse bias condition, the resistance for the device annealed at 330 °C was almost the same regardless of the switching states. However, for the device annealed at 360 °C, its resistance at the LRS decreased when the diode was in reserve bias. This is undesirable because the leakage current may cause errors in reading the resistance state of the adjacent cell in a crossbar architecture. The higher annealing temperature (360 °C) thus degraded the diode performance.

A 1D1R standalone memory cell consisting of a TaO_x-based resistive-switching memory element and a GaAs diode on GeOI on a Si substrate was fabricated. The resistive-switching capability of the 1D1R structure was demonstrated. High resistance ratio (10^2–10^3) between HRS and LRS was achieved. The forward-to-reverse current ratio was ~60 at ±1 V. The 1D1R operated at a generally low bias condition (V_{SET} ~3.28 V) which is comparable to other reported 1D1R structures.[2,15] In the LRS, the current is limited by the diode. Using a thinner TaO_x layer to reduce the operational voltage is currently under investigation. Optimization of the electrode materials and the annealing temperature are expected to improve the performance.

The authors acknowledge the financial support provided by Agency for Science, Technology and Research (A*STAR) grant under Project No. 0921510089.

[1] D. Mian and Z. Lin, in *Proceedings of the 8th IEEE Conference on Nanotechnology (NANO)* (IEEE, Arlington, Texas 2008), p. 692.
[2] J. J. Huang, T. H. Hou, C. W. Hsu, Y. M. Tseng, W. H. Chang, W. Y. Jang, and C. H. Lin, Jpn. J. Appl. Phys. **51**(4 PART 2), 04DD09 (2012).
[3] K. Tsunoda, Y. Fukizumi, J. R. Jameson, Z. Wang, P. B. Griffin, and Y. Nishi, Appl. Phys. Lett. (USA) **90**(11), 113501 (2007).
[4] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D. S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J. S. Kim, J. S. Choi, and B. H. Park, Appl. Phys. Lett. (USA) **85**(23), 5655 (2004).
[5] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Wawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Lijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi,

R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshima, in *Proceedings of the 2008 IEEE International Electron Devices Meeting, IEDM 2008* (San Francisco, CA, USA, 2008).
[6] W. Wu, X. Tong, R. Zhao, L. P. Shi, H. X. Yang, and Y. C. Yeo, in *Proceedings of the 11th Annual Non-Volatile Memory Technology Symposium, NVMTS 2011* (Shanghai, China, 2011), p. 103.
[7] L. J. Zhang, R. Huang, M. H. Zhu, S. Q. Qin, Y. B. Kuang, D. J. Gao, C. Y. Shi, and Y. Y. Wang, IEEE Electron Device Lett. (USA) **31**(9), 966 (2010).
[8] M. J. Lee, Y. S. Park, D. S. Suh, E. H. Lee, S. Seo, D. C. Kim, R. Jung, B. S. Kang, S. E. Ahn, C. B. Lee, D. H. Seo, Y. K. Cha, I. K. Yoo, J. S. Kim, and B. H. Park, Adv. Mater. **19**(22), 3919 (2007).
[9] Y. Sasago, M. Kinoshita, H. Minemura, Y. Anzai, M. Tai, K. Kurotsuchi, S. Morita, T. Takahashi, T. Takahama, T. Morimoto, T. Mine, A. Shima, and T. Kobayashi, in *Proceedings of the 2011 IEEE Symposium on VLSI Technology* (IEEE, Honolulu, HI, USA, 2011), p. 96.
[10] D. S. Golubovic, A. H. Miranada, N. Akil, R. T. F. Van Schaijk, and M. J. Van Duuren, Microelectron. Eng. (Netherlands) **84**(12), 2921 (2007).
[11] H. Tanoto, S. F. Yoon, W. K. Loke, E. A. Fitzgerald, C. Dohrman, B. Narayanan, M. T. Doan, and C. H. Tung, J. Vac. Sci. Technol. B **24**(1), 152 (2006).
[12] X. Tong, W. Wu, Z. Liu, X. A. Tran, H. Y. Yu, and Y. C. Yeo, in *Proceedings of the International Conference on Solid-State Devices and Materials* (Kyoto, Japan, 2012), p. 614.
[13] R. Waser and M. Aono, Nat. Mater. **6**(11), 833 (2007).
[14] Z. Xu, S. F. Yoon, Y. C. Yeo, C. K. Chia, Y. B. Cheng, and G. K. Dalapati, J. Appl. Phys. **111**(4), 044504 (2012).
[15] M. J. Lee, Y. Park, B. S. Kang, S. E. Ahn, C. B. Lee, K. Kim, W. Xianyu, G. Stefanovich, J. H. Lee, S. J. Chung, Y. H. Kim, C. S. Lee, J. B. Park, and I. K. Yoo, in *Proceedings of the 2007 IEEE International Electron Devices Meeting - IEDM '07* (IEEE, Washington, DC, USA, 2007), p. 771.