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2008

Wang, L. B., See, K. Y., Chang, R. W. Y., & Phang, Z. G. (2008). Comprehensive study of crosstalk isolation for high-speed digital board. 2008 Asia-Pacific Symposium on Electromagnetic Compatibility and 19th International Zurich Symposium on Electromagnetic Compatibility (pp. 867-870) Singapore.

https://hdl.handle.net/10356/79882

https://doi.org/10.1109/APEMC.2008.4560013

Comprehensive Study of Crosstalk Isolation for High-Speed Digital Board

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***Abstract*— A comprehensive crosstalk analysis for different layout configurations has been carried out. Using a full-wave electromagnetic simulation tool, crosstalk reduction techniques based on trace-to-trace separation, guard traces, inter-layer ground plane are studied. With the comprehensive simulated results, useful design guidelines are established so that the designers can select the appropriate layout methodology to achieve the desired level of crosstalk isolation.**

I. INTRODUCTION

Inter-trace electromagnetic coupling or "crosstalk" becomes significant due to ever-increasing speeds of digital systems as well as a tighter budget constraint in the noise margins [1],[2]. Crosstalk occurs between long traces on printed circuit boards (PCBs) and is usually quantified in terms of near-end crosstalk (NEXT) and far-end crosstalk (FEXT). If crosstalk is not properly considered in the PCB layout design stage, it will degrade the performance of the system given the tight noise margin. It has been proposed by many researchers that through the appropriate use of guard traces, it will lead to improvement in crosstalk isolation between adjacent traces provided that they are designed properly [3]. Considerations must be made when implementing guard traces as they will also have significant impact on the signal quality on the data traces around it [4].

This paper looks into the maximum achievable crosstalk isolation for microstrip and stripline configurations by increasing the trace to trace separation distance and the use of guard traces. Finally, the use of a ground planes between traces is also explored for design that requires very high crosstalk isolation.

II. VERIFICATION OF SIMULATION RESULTS

Full-wave simulations were carried out using CST's Microwave Studio [5]. Initially, the crosstalk for a simple microstrip PCB structure, as shown in Fig. 1, was fabricated. The dielectric used is FR4 with a permittivity of 4 and loss tangent of 0.02. The simulated results will be compared with the measured results for verification purposes. For time-domain crosstalk measurement, the model is excited with a voltage source with V_p of 1V and t_r of 0.1ns. The measurement was carried out using Agilent's HP81134A pulse generator and a DSO81204 high-speed oscilloscope with a 12GHz bandwidth [6].

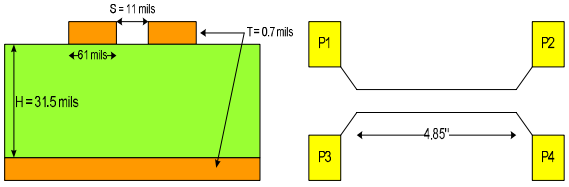

Fig. 1 Microstrip structure for simulation and measurement

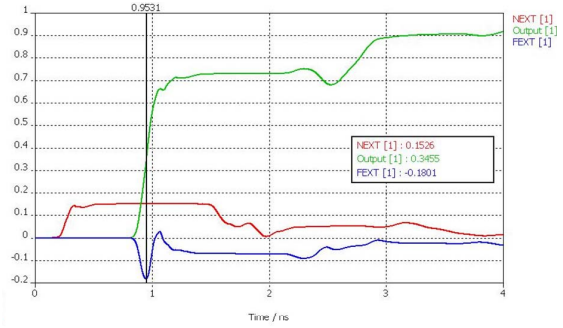

Fig. 2 Simulated time-domain NEXT and FEXT for Fig. 1

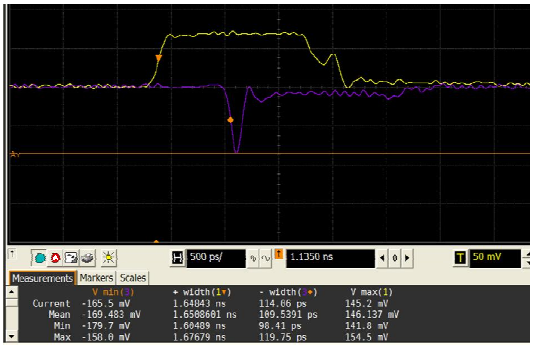

Fig. 3 Measured time-domain FEXT and NEXT for Fig. 1

The simulated and measured results of NEXT and FEXT are shown in Fig. 2 and Fig. 3, respectively. The measured results show that the NEXT is 146.1 mV and the FEXT is 169.5 mV. The simulation results for the NEXT and the FEXT

are 152.6 mV and 180 mV, respectively. The slight difference between the simulation results and the measurement results are expected due to PCB fabrication tolerance. Also, the absence of SMA connectors in the simulated model may also contribute to the difference.

III. CROSSTALK STUDY OF VARIOUS BOARD CONFIGURATIONS

Fig. 4 shows a typical PCB stack-up of a 6-layer board. Layer 1 (L1) and Layer 6 (L6) are in microstrip configuration. Layer 3 (L3) and Layer 4 (L4) are in stripline configuration. Layer 2 (L2) and Layer 5 (L5) are full metal planes.

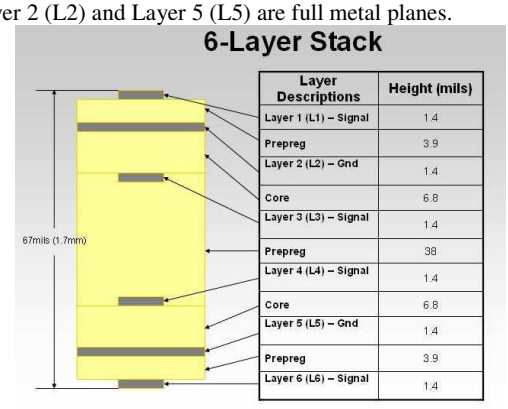

Fig. 4 Stack-up structure of PCB used in the simulation

Table 1 summarizes 7 cases under simulation. Cases 1 and 2 for parallel traces crosstalk studies in microstrip and stripline structures, respectively. Case 3 for traces separated by a ground plane. Cases 4, 5, 6 and 7 explore the application of guard traces with the vias being placed at the ends of the guard trace and vias placed on the guard trace at every 1.7λ, 0.57λ and 0.34λ interval, where λ is the wavelength of the highest frequency of interest, which is 10GHz. The wavelength at 10 GHz is 1.5cm [7].

Table 1

Structure without guard vias

Case	P1	P2	P3	P4	Description
1	L1	L1	L1	L1	S = 1W, 1.5W, 2W, 2.5W and 3W
2	L3	L3	L3	L3	S = 1W, 1.5W, 2W, 2.5W and 3W
3	L1	L1	L3	L3	Traces seperated by 1oz ground plane

Structure with guard vias

Case	P1	P2	P3	P4	Description
4	L1	L1	L1	L1	Ground vias at ends of guard trace
5	L3	L3	L3	L3	Ground vias at ends of guard trace
6	L1	L1	L1	L1	V = 1.7λ, 0.57λ, 0.34λ
7	L3	L3	L3	L3	V = 1.7λ, 0.57λ, 0.34λ

S: Seperation between traces
V: Seperation distance between vias
P1: Aggressor port
P2: Load
P3: NEXT
P4: FEXT

L1: Layer 1
L2: Layer 2 (GND)
L3: Layer 3
L4: Layer 4
L5: Layer 5 (GND)
L6: Layer 6

Parametric studies were carried out to study the effects of coupling on 5" long parallel traces for separation between the traces of 1W to 3W at steps of 0.5W. The trace width, W, was selected to be 6mils and 8mils respectively for microstrip and stripline structures so as to achieve a 50Ω characteristic impedance. For the frequency-domain analysis, the model is excited with a Gaussian pulse covering a bandwidth of 10GHz, whereas for the time-domain analysis, the model is excited with a voltage source having V_p of 1.0V and t_r of 0.1ns.The NEXT and FEXT time-domain simulation results for the parallel 5" microstrip structures with varying separation distances are shown in Figs. 5 and 6, respectively. Similarly, the NEXT and FEXT time-domain simulation results for the 5" stripline structures are shown in Figs. 7 and 8, respectively.

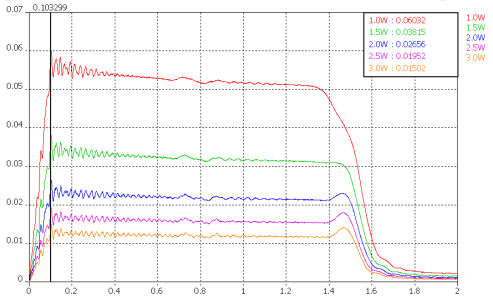

Fig. 5 NEXT of 5 inch microstrip trace

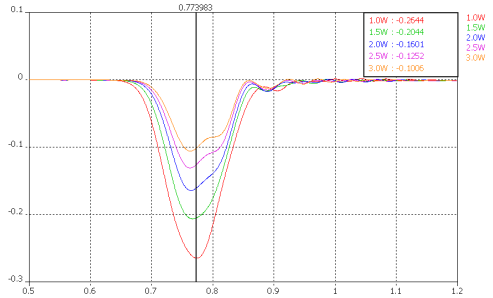

Fig. 6 FEXT of 5 inch microstrip trace

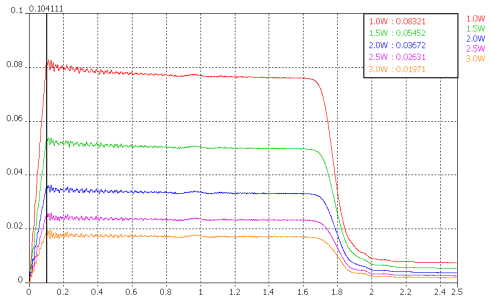

Fig. 7 NEXT of 5 inch stripline trace

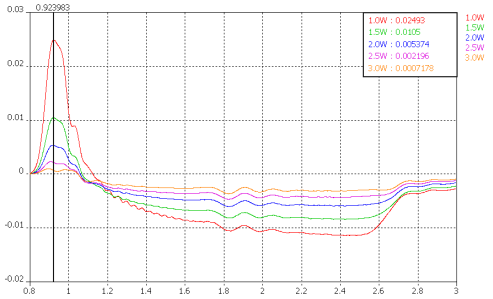

Fig. 8 FEXT of 5 inch stripline trace

The simulations show that most significant reduction in coupling occurs when trace to trace separation is 2W apart. Frequency domain simulation was carried out to analyse the characteristics of traces having different separation distances [8]. The results for case 1 and 2 are shown in Fig. 9 to Fig. 12.

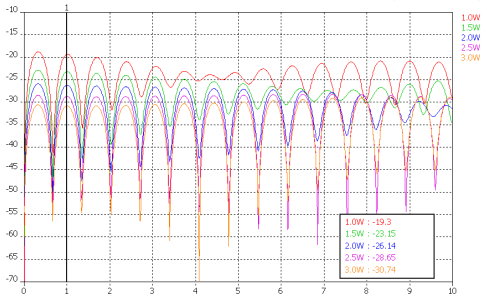

Fig. 9 |S31| dB for 5” microstrip with different trace separation

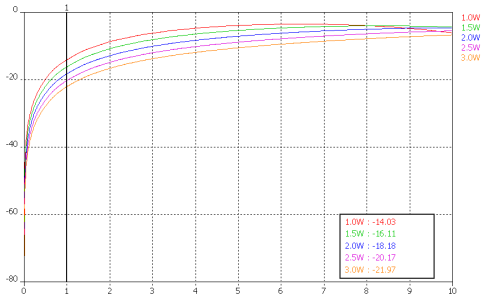

Fig. 10 |S41| dB for 5” microstrip with different trace separation

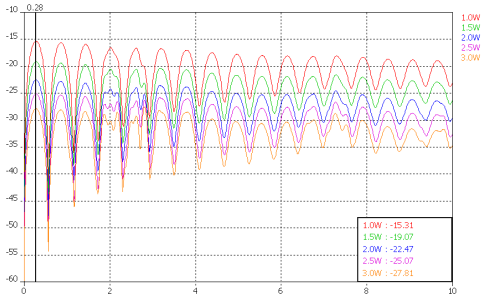

Fig. 11 |S31| dB for 5” stripline with different trace separation

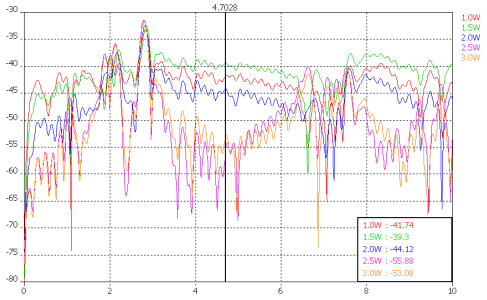

Fig. 12 |S41| dB for 5” stripline with different trace separation

S41 for microstrip structures can be observed to be decreasing with increased in frequency till it finally stabilized 12dB at high frequency. S31 in the stripline configuration is higher than that of the microstrip structure. However, for S41 in the stripline configuration, with the traces having 3W apart, it is possible to achieve isolation of 50dB beyond 3GHz which is 20dB more than that of microstrip structure.

In the next study, 2 microstrip traces routed on different layers separated by a metal plane were modelled to explore the improvement in crosstalk isolation. The traces are designed to be 50Ω using the stack-up for microstrip structures as shown in Fig. 4.

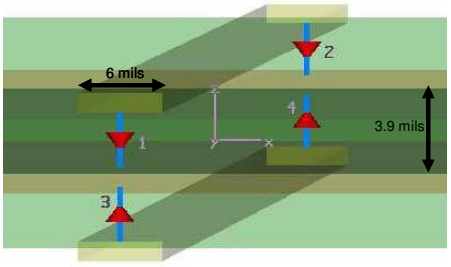

Fig. 13 Layout of model using ground plane to shield signal traces

The structure modelled is shown in Fig. 13. The results in Fig. 14 show that by routing 2 traces on different layers and separated by a metal plane, 85 dB and 90 dB crosstalk isolations for FEXT and NEXT, respectively, can be achieved.

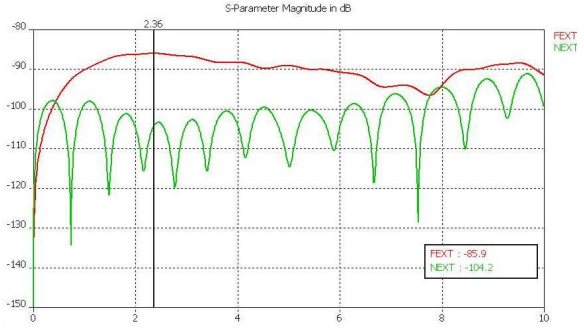

Fig. 14 Magnitude of S31 and S41 for traces separated by ground plane

IV. USING SIMULATION TO STUDY THE EFFECTS OF IMPLEMENTING GUARD TRACES

Asanee et al [4] studied the effects of using guard fences to reduce crosstalk in PCB circuits and also its impact on the signal quality in microstrip structures. For this paper, crosstalk performance of two parallel 5” traces routed in microstrip and stripline configurations [9] having a guard trace in between were studied. Different number of guard vias on the guard trace were simulated and studied in this paper. Fig. 15 to Fig. 18 shows the results of |S31| dB and |S41| dB of the various trace structures where the guard trace is grounded with varying numbers of ground vias.

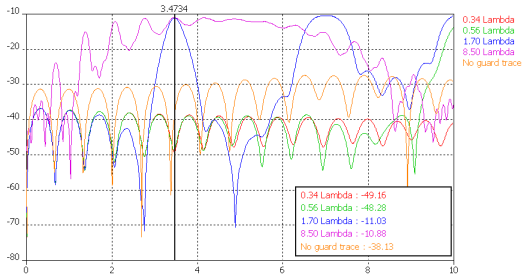

Fig. 15 |S31| dB for 5" microstrip with guard trace

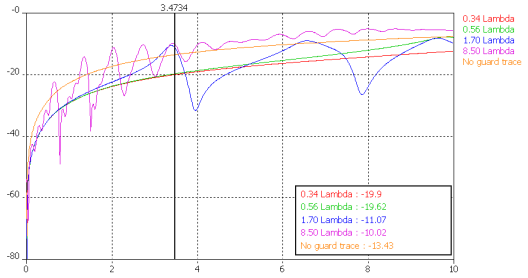

Fig. 16 |S41| dB for 5" microstrip with guard trace

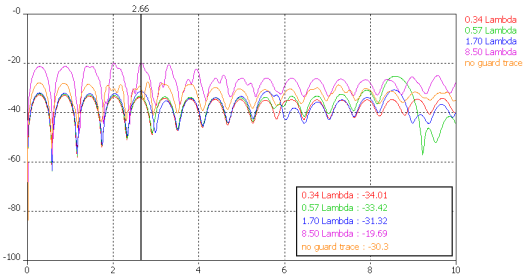

Fig. 17 |S31| dB for 5" stripline with guard trace

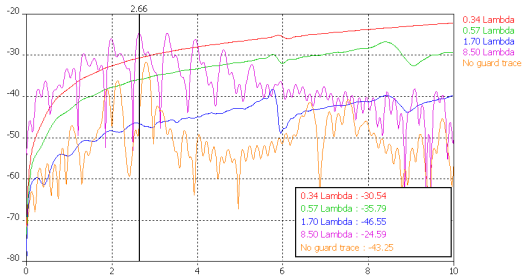

Fig. 18 |S41| dB for 5" stripline with guard trace

The results show that for isolation to be effective on microstrip structures, vias have to be designed 0.57λ apart. For stripline structures, the S31 improves with vias placed closer together. Simulations show that implementation of optimal ground vias for microstrip structures striplines on S31 is also 0.57λ apart. It can be seen that with properly designed guard traces, S31 of microstrip and striplines will improved by additional 7dB and 4dB respectively. It can be observed that if only ends of the guard trace are grounded, the S41 performance is better as compared to the case guard vias placed closer to one another. Overall, simulation shows that the implementation of guard traces on stripline structures is not desirable.

V. Conclusions

The maximum isolation in PCB traces for the various cases are summarized in Table 2.

Table 2

Maximum isolation for various structures

Case	P1	P2	P3	P4	NEXT (dB)	FEXT (dB)
1	L1	L1	L1	L1	30.74	21.97
2	L3	L3	L3	L3	27.81	55.88
3	L1	L1	L3	L3	85.9	104.2
4	L1	L1	L1	L1	10.88	10.02
5	L3	L3	L3	L3	19.69	34.14
6	L1	L1	L1	L1	37.36	24.59
7	L3	L3	L3	L3	32.73	48.32

S: Seperation between traces
N: Number of vias placed per inch of guard trace
P1: Aggressor port
P2: Load
P3: NEXT
P4: FEXT

L1: Layer 1
L2: Layer 2 (GND)
L3: Layer 3
L4: Layer 4
L5: Layer 5 (GND)
L6: Layer 6

Simulation shows that 4 and 3 vias per inch are the optimum criteria for implementing guard traces in microstrip and stripline structures. It is also illustrated that implementation of guard traces can provide at most additional 10dB and 5dB of isolation for microstrip and stripline structures. However, if designers wish to achieve high isolation of at least 80 dB between various traces, it would be recommended to route them on alternate layers shielded by a full ground plane. Through the use of 3D modeling, numerical guides, normalized to the geometry dimensions, are provided for PCB designers.

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