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Equivalent Circuit Model of On-Wafer CMOS Interconnects for RFICs

Xiaomeng Shi, Jian-Guo Ma, *Senior Member, IEEE*, Kiat Seng Yeo, *Member, IEEE*, Manh Anh Do, *Senior Member, IEEE*, and Erping Li

Abstract—This paper investigates the properties of the on-wafer interconnects built in a 0.18- μm CMOS technology for RF applications. A scalable equivalent circuit model is developed. The model parameters are extracted directly from the on-wafer measurements and formulated into empirical expressions. The expressions are in functions of the length and the width of the interconnects. The proposed model can be easily implemented into commercial RF circuit simulators. It provides a novel solution to include the frequency-variant characteristics into a circuit simulation. The silicon-verified accuracy is proved to be up to 25 GHz with an average error less than 2%. Additionally, equivalent circuit model for longer wires can be obtained by cascading smaller subsections together. The scalability of the proposed model is demonstrated.

Index Terms—Empirical formulas, lumped equivalent circuit model, modeling, RF CMOS interconnects, scalable, scattering parameters measurement, skin effect, substrate losses.

I. INTRODUCTION

IN THE RECENT years, wireless devices such as pagers, cellular and cordless phones, global positioning system (GPS) devices and personal communication system (PCS) devices have penetrated in all aspects of our daily lives. Several mobile/wireless communication standards have been widely used covering the frequency range from 0.9 to 5.9 GHz, such as global system for mobile (GSM), code division multiple access (CDMA), Bluetooth, IEEE802.11, etc.. As seen from the market point of view, the cost and ease of system implementation must take priority [1], [2]. Thereby, there is an explosion of interest in the development of radio-frequency system-on-chip (RF-SoC) that integrates RF, analog, and digital circuits together on a single chip. Besides the circuit design, the choice of the implementation technology is also very important and complicated. Compared with other available technologies, such as bipolar CMOS (BiCMOS), GaAs metal-semiconductor field-effect transistor (MESFET), heterojunction bipolar transistor (HBT), etc., CMOS technology is deemed as the most attractive and promising one in the long run [3].

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Due to the combination of the increased circuit complexity and higher operating frequencies of the CMOS RF-SoC, the circuit performance becomes more and more subjected to the interconnect behaviors [4], [5]. The lack of adequate computer aided design (CAD) tools for interconnect modeling is one of the most crucial problems facing the industry. In most available CAD tools, the interconnects are insufficiently modeled as RC components [6], [7]. To improve the accuracy, RLC models have been exploited. Unfortunately, drawbacks still exist in those RLC models. The frequency-variant characteristics, which is substantial at high frequencies, are not included in these RLC models [8]. As improvement, some models employ frequency-variant components to characterize the frequency-variant behaviors [9], [10]. However, up to now the simulations of this kind of components are not supported by commercial circuit simulators. As a consequence, there is an urgent demand of precise, simple and scalable interconnect models which can be implemented into conventional CAD tools. Hence, the circuit design and analysis can be much more facilitated.

Many interconnect modeling methods have been introduced in the literature. These approaches can be mainly classified into two categories. One is electromagnetic (EM) based modeling approach [11]–[13]. It is derived from the numerical solutions of the Maxwell's equations that describe the EM behaviors of the physical structures. The other is measurement based modeling approach [9], [14], which is directly obtained from the measurements of the on-chip test structures. The EM-based approach is known as being capable of predicting the trend of the EM behaviors and flexible with the geometrical dimensions. However, the accuracy of EM based models are limited, since the numerical solution is based on many ideal assumptions. In most cases, the media are assumed to be uniform, isotropic and homogeneous. What is more, the conductors are often assumed to be perfect conductors (PEC) and have zero thickness [15]. Compared with the EM-based modeling approach, the measurement based modeling approach has more silicon-verified accuracy and more computational efficiency [16]. This is the main reason that we adopt it as our methodology. However, the cost for the on-wafer fabrication is very high. Therefore, up to now there are very limited reports on the measurement based modeling approach for RF interconnects.

The objective of the work is to develop accurate scalable interconnect models that are compatible with the commercial CAD tools. In this work, several test structures are designed and fabricated using a 0.18- μm RF CMOS process by Chartered Semiconductor Manufacture Ltd. (CSM). Since S-parameters are the only measurable parameters at RF frequencies

Fig. 1. Cross view of the on-wafer interconnect using CMOS technology.

[17], S-parameter based techniques have been employed. The frequency-variant behaviors of the RF interconnects have been characterized by an elaborately proposed frequency-independent lumped equivalent circuit model. Empirical formulas have been generated for the model parameters. The proposed scalable model is verified with on-chip measurements over a wide frequency range from 50 MHz to 25 GHz, which is adequate for the RF applications. Besides, equivalent circuit model for longer wires can be obtained by cascading shorter subsections together. Thereafter, the paper can also be used for establishment of accurate experimental database for on-wafer RF interconnects.

The remains of this paper are organized as follows. Firstly, we will describe the designed test structures. Secondly, the proposed model construction is introduced. Then the methodology of parameter extraction is presented. After that, the extracted empirical formulas are listed. The verifications and discussions are also given in that section. Finally, the paper is summarized and concluded in Section VI.

II. TEST STRUCTURE DESIGN AND MEASUREMENT

Since the top metal layer has lower sheet resistance and suffers less from the substrate losses, it is commonly allocated for routing critical high frequency paths. Therefore, our test structures are designed and fabricated on the top metal layer employing a CSM 0.18- μm RF CMOS technology. The IC technology cross section view of the test structure is shown in Fig. 1.

The physical dimensions of the test structures are carefully selected. The lengths of the test structures are various from 100 to 800 μm , while the widths are in the range of 1.5–20 μm . The criteria for selecting the minimum width is derived from the foundry design rules, which state that the minimum top-metal width is 1.5 μm . The reason for selecting 20 μm as the maximum width is that the inductor, which is the largest passive device in a circuit, usually has a width less than 20 μm in a typical RF circuit design. The selection of the minimum length for the test structure is based on the concern of the minimum distance that the probes can be placed together. Thereby, the measurement precision is ensured. For typical RF circuit sub-blocks, such as low noise amplifier (LNA), voltage-controlled oscillators (VCO) and mixer, the total die size are around 800 μm by 800 μm . That is the reason why 800 μm is selected as the maximum length in our test structures.

Fig. 2 illustrates the top view of the fabricated test structures. Due to the space limitation of the figure, only six sets of the test structures are shown. The lengths of the shown sets are all 400 μm , while the widths are 1.5, 3, 5, 10, and 20 μm , respectively, from the bottom of the figure. As it is known, three pairs of pads, i.e., ground-signal-ground (GSG) are required for the measurement of each interconnect. From Fig. 2 it is also observed that the ground pads are shared between two adjacent test sets. This so called pad sharing technique is employed here in order to reduce the total size of the die. The test set on the top of Fig. 2 is an open structure designed for de-embedding [8], [18].

Fig. 2. Fabricated interconnect test structures.

Fig. 3. Equivalent network block of interconnect test structure.

It is basically the same layout as the interconnect test structures but without the center conductor. As the test structure can be viewed as a combination of an open structure and the interconnect under interest as shown in Fig. 3, where Y_{p1} , Y_{p2} and Y_{p3} represent the influence of the parallel parasitic contributed by the open structure, the unwanted contributions of the pads can be removed using a Y -parameter-based technique as described in (1) [19]

$$Y_{\text{interconnect}} = Y_{\text{test-structure}} - Y_{\text{open}}. \quad (1)$$

After fabrication, a Cascade Microtech Probe Station and a HP 8510C Vector Network Analyzer are employed for on-wafer measurement. In order to exclude the imperfections of the testing equipment, calibrations are performed before the test structure measurement. As illustrated in Fig. 4, a short-load-open-through (SLOT) calibration technique [20] is used. The S -parameter measurements are then performed on the test structures from 50 MHz to 25 GHz. After that, the de-embedding as described above is carried out. Hence, the probing pads and other parasitic contributions are removed.

Fig. 4. SLOT calibration technique.

Fig. 5. Schematic diagram of one-Π model.

III. MODELING SCHEME

The function of the interconnects is to connect different devices or blocks together. In the low frequency ranges, the interconnects can be characterized by frequency-independent resistors and capacitors. However, this RC model is not applicable at high frequencies, since the interconnect characteristics are much different. Along with the frequency increases, the inductive effect, skin effect, substrate effect and distributed effect begin to impact [21], [22]. All these effects are dependent on the frequency. Consequently, the characteristics of RF interconnects are frequency-variant as well.

Ideally, frequency-variant models should be used in the simulations. However, currently the conventional circuit simulators, such as SPICE do not support simulations of the frequency-variant parameters. Thus, we proposed an equivalent circuit model to characterize these effects with frequency-independent components.

A. Schematic Model Diagram

According to the notion described by Edwards and Steer in [23], when the length of the interconnect is less than $1/20$ of the wave length λ , the signal can be deemed to be reasonably constant along the entire length. Hence, a lumped one-Π model as illustrated in Fig. 5 is adequate. This one-Π model topology is widely used in the modeling of on-chip inductors [24]–[26].

With the increase of the length of the interconnect, the distributed effect begins to impact. When the length is longer than

TABLE I
CRITICAL LENGTH OF VARIOUS FREQUENCY

Frequency (GHz)	0.5	5	15	25
lumped element model (μm)	8695.6	869.6	289.9	173.9
transmission line model (μm)	17391.2	1739.1	579.8	347.8

Fig. 6. Schematic block diagram.

$1/10$ of λ , transmission line model should be used [23]. The criteria for choosing the model topology at various operating frequencies are summarized in Table I.

In Table I, it reveals that for the intended frequency range, i.e., from 500 MHz to 25 GHz, the one-II model is suitable only when the lengths are less than $174 \mu\text{m}$, or else the precision can not be guaranteed. The transmission line model is appropriate only when the lengths are longer than $17391 \mu\text{m}$, otherwise, that model topology is a over-done. As stated in Section II, the lengths of our test structures are various from 100 to $800 \mu\text{m}$. Hence, both of the lumped one-II model and the transmission line model are not proper. Therefore, the choice of the model topology should be carefully concerned. The proposed model should be capable of precisely characterize the high frequency behavior of the interconnects while keeps the model simplicity.

In order to maintain the simplicity, the proposed model is developed based on the one-II model. The problem of the one-II model is that it cannot characterize the distributed effect which is significant at high frequencies. In our work, by strategically cascading two-II lumped blocks together, as illustrated in Fig. 6, the distributed effects can be included. The validity will be demonstrated in Section V. In order to simplify the model construction and parameter extraction, the series blocks of each II are forced to be identical and so are the shunt blocks. This optimization is physically acceptable due to the symmetrical structure of the interconnect.

B. Equivalent Circuit Model

Based on the schematic block model, as shown in Fig. 7, a two-II equivalent circuit model is proposed from a physics point of view.

Traditionally, on-chip interconnect was modeled as coupled RC network [6]. The impact of the magnetic field was generally neglected. However, with the recent significant increase of the operating frequency, the impact of magnetic field and magnetic coupling becomes one of the most emergent issues of the RFIC design [27], [28]. This kind of impact cannot be neglected any more. In our proposed model, the inductance is introduced by L_s , which represents the ideal series inductance.

Typically, the resistance of a line with the length l , width W and thickness t is given by

$$R = \rho \frac{l}{tW} = R_s \frac{l}{W} \quad (2)$$

where ρ is the resistivity of the interconnect material and R_s is the sheet resistance based on dc measurements. In our model, the component R_s represents the ideal series resistance of the interconnects.

However, at high frequencies, say above 5 GHz, the EM fields attenuate substantially when they pass through the conductor. As a result, skin effect starts to emerge [29]. At a sufficient depth, all the fields are negligible and there is no current. Hence, the effective cross section of the conductor shrinks with the increase of the frequency. Skin depth δ is defined in (3). It refers to the depth from the surface of a conductor, where the currents are confined to flow

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \frac{1}{\sqrt{f\pi\mu\sigma}} \quad (3)$$

where μ and σ stand for the permeability and the conductivity of the conductor respectively. ω represents the angular frequency, which is the product of 2π and the operating frequency f .

We now need to modify the conventional calculation of the resistance shown in (2), by replacing the geometrical cross section area with the effective one. Thereby, the resistance formula converts to (4)

$$R = \frac{\rho l}{Wt - (W - 2\delta)(t - 2\delta)}. \quad (4)$$

As the skin depth decreases with the frequency increasing, the resistance of the conductor becomes frequency-variant as while. It increases along with the frequency. On the contrary, the inductance reduces. The reason is that at low frequencies, the magnetic energy is stored inside as well as outside the conductors. However, as frequency increases, the current flow is mostly concentrated near the surface of the conductor. Hence, the magnetic field becomes confined to the region outside the conductor [23]. In RFICS, as the operating frequency approaches multi-gigahertz, the skin effect becomes very significant. Thereafter, it must be included in the simulation. However, as mentioned in the introduction, the frequency-variant components are not supported by conventional circuit simulators. Hence, mimicking the frequency-variant skin effect with frequency-independent components becomes the straight forward solution.

In Fig. 7, the series components R_{sk} and L_{sk} connected in parallel in our proposed model are introduced to characterize the skin effect. As stated above, due to the skin effect, the behavior of the interconnect becomes more resistive than inductive at high frequencies. In this paralleled branch, at low frequencies, the currents mostly pass through L_{sk} . When the operating frequency rises, more currents shift to the path of R_{sk} . With these two frequency-independent components, the frequency-variant skin effect characteristics can be well captured.

Besides the skin effect, at gigahertz frequencies the substrate losses are also substantial. In current CMOS RF technologies,

Fig. 7. Equivalent circuit model.

unneglectable high frequency losses are caused by the low-resistivity substrate [30]–[32]. The substrate affects interconnects in two ways: eddy current losses and displacement current losses. The eddy currents in the substrate are induced by the current flowing through the conductor. The eddy currents, in turn, change the magnetic field and the inductance of the conductor. Particularly, if a high conductivity substrate is used at high frequencies, strong eddy currents will crowd near the surface of the substrate. As a result, the inductance is reduced and significant eddy current losses are caused. This impact of the eddy currents are also frequency-variant. At DC, no eddy currents are induced. The inductance is as the same as that in the free space. As the frequency increases, the eddy currents become stronger and are more crowded to the surface. The changes of the inductance and the eddy current losses become more noticeable. This effect is characterized by L_{sk} and R_{sk} as well, as with frequency increasing, the current flow shifts from L_{sk} to R_{sk} . Hence, the equivalent inductance reduces and the loss increases.

Another part of the substrate losses are derived from the substrate injection of the displacement currents. The displacement currents flow through the capacitance which terminates on the substrate. This results in additional resistive losses. The capacitance to the substrate is frequency-variant as well. It is smaller at higher frequencies, since the electric field lines generally extend further into the substrate before terminating on charge. This effect is modeled by the resistor and capacitors in the shunt block. Together with the understandings of the physical structure, the shunt block is proposed as illustrated in Fig. 7, where C_{ox} represents the oxide layer capacitance, R_{sub} symbolizes the substrate resistance while C_{sub} represents the capacitance of the substrate.

IV. METHODOLOGY OF PARAMETER EXTRACTION

In the stage of parameter extraction, a hybrid Genetic Algorithm is applied. Firstly, the admittance of each sub-block, as shown in Fig. 6, Y_1 and Y_2 , are derived as functions of the circuit components

$$Y_1 = \frac{1}{j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}} \quad (5)$$

$$Y_2 = \frac{1}{\frac{1}{j\omega C_{ox}} + \frac{R_{sub}}{j\omega C_{sub} R_{sub} + 1}}. \quad (6)$$

Then Y -parameters can be presented as functions of the admittance of each sub-block Y_1 and Y_2 , as illustrated in (7)–(10)

$$Y_{11} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1 Y_2)} \quad (7)$$

$$Y_{12} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (8)$$

$$Y_{21} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (9)$$

$$Y_{22} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1 Y_2)}. \quad (10)$$

On the other hand, the measured S -parameters can be converted into Y -parameters, based on the equations from (11) to (14) as follows:

$$Y_{11} = \frac{1}{Z_0} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (11)$$

$$Y_{12} = \frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (12)$$

$$Y_{21} = \frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (13)$$

$$Y_{22} = \frac{1}{Z_0} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (14)$$

where Z_0 is the characteristic impedance of the interconnects under test, which is 50Ω in this work.

Therefore, by combining (7)–(10) and (11)–(14), (15)–(18) can be obtained. By solving (15)–(18), the values of Y_1 and Y_2 can be obtained from the measurement results

$$\frac{1}{Z_0} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1 Y_2)} \quad (15)$$

$$\frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (16)$$

$$\frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (17)$$

$$\frac{1}{Z_0} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1 Y_2)}. \quad (18)$$

TABLE II
COEFFICIENTS OF L_s

Coefficient	Value
a	-7.31643E-12
b	5.51876E-13
c	1.37238E-11
d	-4.13401E-12
e	-7.0167E-14

TABLE III
COEFFICIENTS OF L_{sk}

Coefficient	Value
a	-9.64956E-13
b	1.9307E-14
c	1.655E-11
d	1.99008E-11

Herein, the model parameter becomes an optimization problem. The objective function $F_0(X)$ of this problem as described in (19) can be divided into two parts by the plus sign. The first part is the average error between the derived admittances and those obtained from the measurements. The second part is the variance of the error. The proposed $F_0(X)$

$$F_0(X)|_{X=(X_1, X_2, \dots, X_n)} = \sum_{i=1}^m (f_i(X)^2 + [f_i(X) - F_{\text{mean}}]^2). \quad (19)$$

In (19), the vector $X = (X_1, X_2, \dots, X_n)$ represents the component values to be extracted (L_s, R_s, L_{sk} and R_{sk} of block Y_1 and $C_{\text{ox}}, C_{\text{sub}}$ and R_{sub} of block Y_2). n is the total number of parameters in each block. m is the total number of frequency points under consideration. $f_i(x)$ is the error between the simulated admittance and the ones obtained from the measurement results at each frequency point under interest. The definition of $f_i(x)$ is given in (20). F_{mean} is the mean error within the whole concerned frequency range, which is defined in (21)

$$f_i(X) = \frac{Y_{\text{simulated}(i)} - Y_{\text{measured}(i)}}{Y_{\text{measured}(i)}} \quad (20)$$

$$F_{\text{mean}} = \frac{\sum_{i=1}^m f_i(X)}{m}. \quad (21)$$

A hybrid Genetic Algorithm (GA) is then employed to search for the optimal model parameters. The algorithm is named as a hybrid GA because in the evaluation stage, the *fminsearch* function provided by Matlab is employed. In the hybrid GA, each chromosome is a vector consisting of values of L_s, R_s, L_{sk} and R_{sk} of block Y_1 and $C_{\text{ox}}, C_{\text{sub}}$ and R_{sub} of block Y_2 . The fitness value of each chromosome is evaluated according to the objective junction $F_0(X)$ presented in (19). Chromosomes with smaller fitness values are higher evaluated and have more chance to be selected to reproduce. The generated offsprings are evaluated as well and the reproduction is continued. After 50 generations, the best evaluated chromosome is the final answer. The consisting component values are the most optimized that make the simulation results fit the measurement data best.

TABLE IV
COEFFICIENTS OF R_s

Coefficient	Value
a	0.03644663
b	5.76521E-4
c	0.04092424
d	-0.246694897

TABLE V
COEFFICIENTS OF R_{sk}

Coefficient	Value
a	-0.124733535
b	1.670241E-3
c	2.018170489
d	-2.332177206
e	6.04339E-4

TABLE VI
COEFFICIENTS OF C_{ox}

Coefficient	Value
a	4.58957E-17
b	1.16724E-17
c	2.69628E-18
d	-7.56085E-19
e	1.20727E-18

TABLE VII
COEFFICIENTS OF C_{sub}

Coefficient	Value
a	5.10835E-18
b	1.2102712
c	0.082382533

TABLE VIII
COEFFICIENTS OF R_{sub}

Coefficient	Value
a	1.233421E6
b	-1.146377345
c	-0.25549637

V. RESULTS AND VERIFICATIONS

In this section, the results, further discussions, as well as the verifications of the model accuracy are presented.

A. Results and Discussions

With the extraction methodology described in Section IV, empirical formulas of the circuit parameters are summarized as functions of the design parameters. Therein, with every set of the length and width, the model parameters can be calculated. Then, with (5) and (6) and (15)–(18), S-parameters of the interconnect are also available.

The summarized formulas are presented one by one below. The coefficients of each formula are listed in separate tables.

The formulated expressions for L_s and L_{sk} are defined in (22) and (23). The corresponding coefficients for each expression are shown in Tables II and III

$$L_s = a + bl + c \log W + d(\log W)^2 + e l \log W \quad (22)$$

$$L_{sk} = a + bl + \frac{c}{W} + \frac{d}{W^2}. \quad (23)$$

Fig. 8. Comparisons of simulated and measured magnitude of S_{11} .

Fig. 9. Comparisons of simulated and measured phase of S_{11} .

From (22) and (23), it is observed that both of the L_s and L_{sk} are proportional to the length and inversely proportional to the width of the interconnects. This can be explained with the EM knowledge. When the length of the interconnect increases, the magnetic flux linkage also increases. As the inductors represent the magnetic energy storage capacity, the value of the inductance increases. When the interconnect has a narrower width, the cross section is also smaller. Hence it generates more magnetic flux external to the wire and the inductance increases [33].

The formulas for R_s and R_{sk} are presented in (24) and (25) respectively. The related coefficients are listed in Tables IV and V

$$R_s = a + bl + \frac{c}{W} + \frac{d}{W^2} \quad (24)$$

$$R_{sk} = a + bl + \frac{c}{W} + \frac{d}{W^2} + \frac{el}{W}. \quad (25)$$

Observing (24) and (25), we can find that the two resistance are proportional to the length and inversely proportional to the

Fig. 10. Comparisons of simulated and measured magnitude of S_{21} . Fig. 11. Comparisons of simulated and measured phase of S_{21} .

width. It is congruent with the well-known definition of the resistors.

Equations (26) and (27) are expressions for C_{ox} and C_{sub} . The coefficients are presented in Tables VI and VII

$$C_{ox} = a + bl + cW + dW^2 + eW \quad (26)$$

$$C_{sub} = al^b W^c \quad (27)$$

$$R_{sub} = al^b W^c. \quad (28)$$

In (26) and (27), both of these two capacitances are proportional to the length and the width, which accords with our understanding of the definition of capacitors.

Equation (28) and Table VIII are defined for R_{sub} .

From (28), R_{sub} is inversely proportional to both of the length and the width. The reason is that the interconnect with a larger physical dimension has larger substrate losses. As a result, its equivalent substrate resistance is smaller.

Fig. 12. Comparisons of cascaded and measured magnitude of S_{11} .

Fig. 13. Comparisons of cascaded and measured phase of S_{11} .

B. Verifications

With the aid of Matlab, simulations of the proposed two- Π lumped equivalent circuit model are performed based on the parameter values derived from the empirical formulas. The simulated S -parameters are compared with the corresponding measured ones. The plots are presented in Figs. 8–11. Considering the symmetry of the interconnect test structure, it is known that $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$ [18]. Therefore, only S_{11}

and S_{21} are compared here. The magnitudes and phases are plotted separately.

From these four figures of comparisons, satisfactory agreements between the simulated S -parameters and the measurement results over a whole frequency range have been achieved within a tolerance of 2%. It demonstrates that the proposed two- Π equivalent circuit model and the formulated empirical parameter expressions are capable of accurately characterizing the behaviors of the on-wafer straight-line interconnects over a

Fig. 14. Comparisons of cascaded and measured magnitude of S_{21} . Fig. 15. Comparisons of cascaded and measured phase of S_{21} .

large range of frequencies up to 25 GHz, which is adequate for RF applications.

It is important to note that the given formulas of the model parameters are fit to our specific test chip and process. Moreover, these formulas are only valid within a geometrical range, which is within the coverage of our test structures. For the length, the valid range is from 100 to 800 μm ; While for the width, it is only applicable between 1.5 and 20 μm . However, as stated in Section II, most of the on-chip interconnects used in RFIC's are within this range. Namely, the provided geometrical extent are sufficient for most cases. For those rare cases, in

which the lengths of the interconnects are beyond 800 μm , a cascading methodology can be applied. Firstly, the long wire is split into smaller sections with lengths less than 800 μm . Then, two- Π models are developed for each subsection. After that, those two- Π blocks are cascaded together to form the complete model for the entire wire. We have employed this method to form an 800 μm interconnect with two 400 μm subsections, while form a 400 μm wire with two 200 μm subsections. Referring to Figs. 12–15, the simulated results agree well with the measurement data. These experiments also prove the scalability of our proposed model.

VI. CONCLUSION

In this paper, the methodology of model development for RF on-wafer interconnects is presented. A two- Π lumped equivalent circuit model is proposed. The inductive property, as well as the skin effect and the substrate losses at high frequencies are considered. The distributed effect is also included.

Directly from the S -parameter measurements, the model parameters are extracted and formulated into empirical expressions. The accuracy of the model is verified by the comparisons between the simulated results and the measurement data. The error is less than 2%. Additionally, the scalability of the proposed model has also been demonstrated.

It is highlighted that the proposed model is capable of characterizing the frequency-variant features of RF interconnects with frequency-independent components. It can be easily implemented in any standard simulation environment, such as SPICE. Moreover, given the compact nature of the model, sophisticated EM background is not a requirement for applying the model to circuit simulations. These advantages make it quite convenient for IC designers to use.

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