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A Novel Subthreshold Voltage Reference Featuring 17ppm/°C TC within -40°C to 125°C and 75dB PSRR

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Abstract—Subthreshold voltage references are increasingly prevalent in power-critical applications due to their low-voltage and ultra-low-power attributes. However, the effective temperature range of state-of-the-art subthreshold voltage references remains undesirably narrow for low temperature coefficient (TC) operation and/or their PSRR is low – thereby severely limiting their range of applications. In this paper, we present a novel subthreshold voltage reference embodying a novel paralleled ‘2-Transistor’ structure and a novel auxiliary amplifier. The former serves to facilitate low TC within a wide temperature range, and the latter for high PSRR and low line-sensitivity. The proposed design achieves low TC of 17ppm/°C within a wide effective temperature range of -40°C to 125°C, and high PSRR of 75dB and low line-sensitivity of 0.3%/V with minimum 0.5V supply voltage and 32nW power consumption. Both the TC and PSRR parameters are, at this juncture, the best performance compared to reported subthreshold voltage references, but with a slight power penalty.

I. INTRODUCTION

Low-voltage and ultra-low-power (power-critical) devices such as sensors, mobile devices and portable instruments typically require low-voltage, ultra-low-power and low noise analog/mixed-signal circuits including conditioning circuits, voltage regulators and data converters. The voltage reference therein serves to provide a reference voltage with wide variation-space [1] (a PVT insensitive (Process, Supply Voltage and Temperature) reference voltage) whilst dissipating minimal power [2]. The general requirements include (i) low Temperature Coefficient (e.g. TC<40ppm/°C) within a wide temperature range (e.g. -40°C to 125°C), (ii) high Power Supply Rejection Ratio (e.g. PSRR≥60dB) and (iii) low voltage (e.g. ≤1V) and ultra-low-power operation (e.g. ≤50nW).

To satisfy aforesaid (iii), the subthreshold voltage reference is usually adopted where the gate-to-source voltage (V_{gs}) of the subthreshold-biased CMOS transistor therein is low, typically 0.2-0.3V (for deep submicron processes), and the drain-to-source current (I_{ds}) thereof is also low, typically several nAs.

At this juncture, there are two general subthreshold voltage reference architectures. The former largely adopts a stacked ‘2-Transistor’ structure [3, 4], and their effective temperature range is undesirably narrow. Specifically, the voltage references in [3] and [4] respectively exhibit TC=19ppm/°C for -20°C to 80°C and TC=32ppm/°C for 0°C to 100°C. Their TC would substantially further degrade if the effective temperature range is widened to -40°C to 125°C, the typical ‘industrial grade’ range. The narrow effective temperature range and/or poor TC of the stacked ‘2-Transistor’ structure is largely attributed to the non-ideal drain/source-to-bulk leakage current effect; this mechanism will be investigated in Sec. II.

The latter, on the other hand, adopts diode-connected NMOS structure [5] that is biased by a current source. This structure, for

example designs [5] exhibit a low PSRR of only 45dB. This is largely because the current source therein is sensitive to power supply noise when they are designed for ultra-low-power operation; an amplifier with excessive power consumption is generally not adopted or accepted.

In short, for state-of-the-art reported subthreshold voltage references, their low-voltage and ultra-low-power operation is often achieved with severe compromises to their TC within a limited effective temperature range and/or low PSRR. As these limitations render their application to limited conditions, their applications are commensurably limited. In view of this, it is imperative to design a subthreshold voltage reference that features both low TC within a wide effective temperature range and high PSRR, yet at low-voltage and ultra-low-power operation.

In this paper, we first provide an investigation to ascertain the mechanism of the non-ideal leakage current effect in subthreshold voltage references [3, 4]. By mitigating the effects of the ascertained mechanism, we thereafter present a novel subthreshold voltage reference design that uniquely features the combined attributes of low TC within a wide effective temperature range, high PSRR and low-voltage and ultra-low-power operation – effectively a high variation-space subthreshold voltage reference. Specifically, instead of the stacked ‘2-Transistor’ structure [3, 4], we propose a novel structure embodying a parallel of two NMOS transistors (paralleled ‘2-Transistor’) with different threshold voltages (V_{th}). In this fashion, the non-ideal leakage current effect is largely mitigated, and the proposed subthreshold voltage reference achieves low TC of 17ppm/°C within a widened temperature range of -40°C to 125°C. Further, to obtain high tolerance to supply voltage noise/variations without dissipating excessive power, a novel auxiliary amplifier is proposed. Collectively, the proposed subthreshold voltage reference achieves a high PSRR of 75dB and low line-sensitivity of 0.3%/V, and the auxiliary amplifier dissipates only 6nW – ~20% of the total power consumption of the entire voltage reference. When compared to reported subthreshold voltage references, the proposed design features both lowest TC over widest effective temperature range and higher PSRR, but with a slight power penalty.

II. MECHANISM OF LEAKAGE CURRENT EFFECT

In this section, we will comprehensively analyze, at this juncture unreported, the leakage current effect in the aforesaid subthreshold voltage references [3, 4]. This investigation serves as a preamble to our proposed design.

Fig. 1(a) depicts the voltage reference embodying the ‘stacked 2-Transistor’ structure [3]. In this structure, two NMOS transistors are stacked vertically, and have different threshold voltages (e.g. $N1$ is a native nFET and $N2$ is the IO nFET [3]).

The temperature independence of the voltage reference is based on the assumption of current balance at node V_{REF} where

$$I_{ds1} = I_{ds2} \quad (1)$$

Nevertheless, in practice, this assumption is invalid because of the parasitic diodes depicted in Fig. 1(b) for the same voltage reference. When accounting for the non-ideal leakage current due to these parasitic diodes, the current at node V_{REF} can be re-expressed as:

$$I_{ds1} = I_{ds2} + I_{sb1} + I_{db2} \quad (2)$$

where I_{sb1} is the source-to-bulk leakage current of $N1$, and I_{db2} is the drain-to-bulk leakage current of $N2$.

Figure 1 Schematics of voltage reference of the (a) ideal stacked '2-Transistor' structure, (b) stacked '2-Transistor' structure with leakage current

As I_{sb1} and I_{db2} are highly temperature dependent and they increase exponentially as temperature increases [6], I_{sb1} and I_{db2} become significant, particularly at high temperature. Consequently, the voltage reference that embodying the stacked '2-Transistor' structure becomes highly temperature-sensitive.

In summary, the leakage current effect is serious in the stacked '2-Transistor' structure [3, 4]. In the next section, we will present a novel parallel '2-Transistor' structure that can achieve low TC within a wide temperature range by minimizing the leakage current effect.

III. PROPOSED SUBTHRESHOLD VOLTAGE REFERENCE DESIGN

In this section, we will first describe the proposed voltage reference, and thereafter delineate design considerations to optimize/improve its robustness towards PVT variations.

Fig. 2 depicts the proposed subthreshold voltage reference embodying a novel paralleled '2-Transistor' structure realized by means of a parallel of two NMOS ($N1$ and $N2$), vis-à-vis the stacked '2-Transistor' structure in Fig. 1(a). The functionalities of these transistors are as follows. $N1$ and $N2$ have different threshold voltages – specifically, $N1$ is a regular threshold voltage transistor ($V_{th} \sim 400\text{mV}$ @ $T=25^\circ\text{C}$), and $N2$ is a low threshold voltage transistor ($V_{th} \sim 250\text{mV}$ @ $T=25^\circ\text{C}$). $P1$ and $P2$ are the current sources, and serve to equalize the currents through $N1$ and $N2$. $P0$ and $N0$ serve as an ultra-low-power (6nW) auxiliary amplifier to improve PSRR, R_C and C_C forms the frequency compensation circuit to ensure the stability of the proposed voltage reference.

Since $N1$ and $N2$ are biased in the subthreshold region, V_{gs} and I_{ds} of $N1$ and $N2$ can be respectively expressed as,

$$V_{gs} = V_{th} + mV_T \ln \frac{I_{ds}}{AI_0} \quad (3)$$

where $V_{th} = V_{th0} + \beta T$,

T is the absolute temperature,

V_{th0} is V_{th} at $T = 0\text{K}$,

β is the temperature coefficient of V_{th} , which is a negative constant [7],

m is the subthreshold slope factor, $m=m_1=m_2$ [3],

$V_T (=kT/q)$ is the thermal voltage,

k is the Boltzmann's constant,

q is the electrical charge,

A is the aspect ratio of the transistor,

$I_0 (= \mu_0 T_0^2 C_{ox}(m-1)k^2/q^2)$ is a temperature independent current,

T_0 is an arbitrary temperature, and

μ_0 is the carrier mobility at $T=T_0$.

On the basis of eqns. (3), V_{REF0} in Fig. 2 can be derived as:

$$V_{REF0} = (V_{th0_N1} - V_{th0_N2}) + (\beta_1 - \beta_2)T + \left(\frac{mk}{q} \ln \frac{A_{P1}A_{N2}I_{0_N2}}{A_{P2}A_{N1}I_{0_N1}} \right)T \quad (4)$$

The first term in eqn. (4) is temperature independent. The second term is positively proportional to T as $\beta_1 > \beta_2$ in this design. The third term is designed to be negatively proportional to T , and compensates for the second term by an appropriate selection of A_{P1}/A_{P2} and A_{N1}/A_{N2} ; in the proposed design, A_{P1}/A_{P2} and A_{N1}/A_{N2} are set to 1 and 1.5, respectively.

Figure 2 The proposed subthreshold voltage reference

Design Considerations for Process Variations

Process variations may degrade TC of the proposed voltage reference. On the basis of eqn. (4), the TC trimming circuit in Fig. 2 tunes A_{P2} , thereby optimizing the TC of V_{REF0} .

Further, V_{REF0} in Fig. 2 is also somewhat sensitive to process variations. To eliminate this effect, the V_{REF} trimming circuit in Fig. 2 can achieve a desired output by trimming it with a resistor ladder and a MUX.

Fig. 3 compares the simulation results of trimmed and untrimmed V_{REF} versus temperature under four process corners. On the basis of the simulation results, the trimming circuits reduce the TC variations from 20-32ppm/ $^\circ\text{C}$ to 18-22ppm/ $^\circ\text{C}$, and reduce the V_{REF} variations from 15mV to 4mV.

high PSRR of 75dB is obtained. As expected, the PSRR decreases as the frequency increases in the range from 2kHz to 100kHz because the loop gain dominant pole is at ~ 2 kHz. The PSRR, on the other hand, increases as the frequency increases beyond 100kHz largely because of the loading capacitor (C_L). The high PSRR indicates that the proposed design has excellent tolerance to supply voltage noise, and as delineated earlier, this is attributed to the novel auxiliary amplifier.

Figure 7 PSRR of the proposed voltage reference

Fig. 8 depicts the reference output V_{REF} versus V_{DD} at $T=25^\circ\text{C}$. It can be observed that the minimum V_{DD} of the proposed design is ~ 0.5 V because of the stacked-connection of $P2$, $N2$ and R in Fig. 2. Further, the desirably low line-sensitivity of 0.3%/V is obtained, hence an excellent tolerance to supply voltage variations. As in the case of the high PSRR, the low line-sensitivity is likewise attributed to the novel auxiliary amplifier.

Figure 8 V_{REF} versus V_{DD} @ $T=25^\circ\text{C}$

Table I benchmarks the performance of the proposed subthreshold voltage reference design against state-of-the-art reported designs. The proposed design features the lowest TC over the widest temperature range of all designs. Further, the proposed design is the only design that is rated for industrial temperature grade. Particularly, it is the only subthreshold reference voltage with $\text{TC} \leq 20 \text{ ppm}/^\circ\text{C}$ for $-40^\circ\text{C} \leq T \leq 125^\circ\text{C}$. In terms of PSRR, the proposed design features the highest PSRR, and is ~ 10 dB higher than the nearest competitor. In terms of line-sensitivity, the proposed voltage reference is about the average of the reported designs. In general, as the line-sensitivity is highly affected by the minimum V_{DD} voltage operation, this parameter is, contentiously, a secondary parameter.

TABLE I PERFORMANCE COMPARISONS

	This Work	[3] JSSC 2012	[4] ISCAS 2012	[5] JSSC 2011	[8] JSSC 2007
Technology	65nm	130nm	130nm	180nm	350nm
TC (ppm/$^\circ\text{C}$)[*] (Temp Range ($^\circ\text{C}$))	17 (-40 to 125)	19 (-20 to 80)	32 (0 to 100)	142 (0 to 125)	10 (0 to 80)
PSRR (dB)	75	53	64	45	47
LS (%/V)	0.3	0.03	0.1	0.3	0.4
Minimum V_{DD}	0.5	0.5	0.5	0.45	0.9
Power (nW)	32	0.002	1.5	3.2	36

^{*} Note that TC is specified for different temperature ranges.

In terms of power consumption, the power consumption of the proposed voltage reference is the second highest. Nevertheless, dissipating 32nW for a subthreshold voltage reference is well within that required for ultra-low-power applications, hence sufficiently low and acceptable for a number of applications. The high power consumption is due to resistor therein.

In conclusion, the proposed subthreshold voltage reference features the lowest TC over the widest temperature range (and the only qualified for industrial grade of -40°C to 125°C) and the highest PSRR. On these bases, the proposed subthreshold voltage reference is the most competitive. On the basis of line-sensitivity and power consumption, the proposed voltage reference is average for the former and on the higher side for the latter (nevertheless still applicable for the majority of power-critical applications).

V. CONCLUSIONS

A novel low-voltage (minimum 0.5V) and ultra-low-power (32nW) subthreshold voltage reference, based on a novel paralleled '2-Transistor' structure and the novel auxiliary amplifier, has been presented. When benchmarked against reported designs, it features the lowest TC over the widest temperature range and the highest PSRR. Its line-sensitivity is however average, and its power consumption slightly compromised but still very low power (and applicable to a myriad of power-critical applications).

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