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Total Ionizing Dose (TID) Effects on Finger Transistors in a 65nm CMOS Process

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Abstract — Although Total Ionizing Dose (TID) effects are generally unpronounced in deep-submicron-CMOS, we show the TID-induced leakage current @TID=500Krad is significant in NMOS-finger-transistors of GlobalFoundries 65nm CMOS. Further, Radiation-Hardening-By-Design techniques against said TID effect are recommended.

I. INTRODUCTION

Integrated Circuits (ICs) for space-and-satellite applications are subject to various radiation effects such as Total Ionizing Dose (TID) [1] and Single-Event-Effects (SEEs) [2]. To mitigate said radiation effects, the Radiation-Hardening-By-Design (RHBD) approach [3-6] is increasingly prevalent by leveraging on the commercially-available advanced CMOS processes.

It is generally agreed in the space community that SEE is more pronounced than TID in advanced deep submicron CMOS processes (typically the technology node $\leq 130\text{nm}$). Hence, the SEE mechanisms therein and the pertinent RHBD techniques have been widely reported [5, 6]. Nonetheless, in view of the accumulative effect of TID (as opposed to the intermittent effect of SEEs), it is still highly desirable to achieve minimal TID to extent the lifespan of satellite. Unfortunately at this juncture, the TID effects in deep submicron CMOS processes are not well-understood and unreported, and the reported RHBD techniques [3] for TID are unavailable therein.

In this paper, we investigate the TID effects in GlobalFoundries 65nm bulk CMOS process. The testing and characterization were performed in AeroflexRAD Inc., and the single NMOS transistors (it is known that PMOS has negligible TID effects) and basic digital library cells are tested/characterized up to TID level of 500Krad. Note that these TID levels are largely appropriate for most of space-and-satellite applications including Low Earth Orbit and Medium Earth Orbit. The TID testing standard conforms to MIL-STD-883 TM1019 Condition A.

Our investigation shows that the TID-induced leakage current is significant in multi-finger NMOS transistors at TID=500Krad. This observation is unreported and interesting, and we attribute this effect to the presence of thick-oxide STI (Shallow Trench Isolation) layer at gate edge. This effect is particularly pronounced when NMOS transistors are biased in subthreshold region, and this is increasingly important in view of the increasing demand of subthreshold digital circuits for space-and-satellite applications because of their substantially low power dissipations [7]. We also recommend several RHBD techniques to accommodate for the TID-induced leakage current, including adoption of small transistor size for digital circuits when possible, the NAND-

type library cells against the NOR-type library cells in view of the TID-hardening of the former, and transistor stacking techniques when speed is not a critical parameter.

This paper is organized as follows. Section II investigates the TID effects on single NMOS transistors. Section III investigates the TID on basic digital library cells. Section IV provides some specific recommendations on transistor sizing and layout implementation for both analog and digital circuits. Finally, the conclusions are drawn in Section V.

II. TRANSISTOR CHARACTERIZATION FOR TOTAL IONIZING DOSE (TID) EFFECTS

Fig. 1 (a) depicts a typical transistor layout with a transistor sizing of W/L . The terminals are respectively labeled as S (source), G (gate) and D (drain). There are two primary TID effects: (1) the threshold voltage shift [1, 3] and (2) radiation-induced leakage current [1, 8]. The threshold voltage shift is due to the accumulated charges trapped over time in the gate-oxide [1], eventually affecting the drain current (I_d ; see the bold solid arrow in Fig. 1 (a)). It is well known that the threshold voltage shift has been largely mitigated in deep submicron CMOS processes ($\leq 180\text{nm}$) in view of their gate silicon oxide is thin ($< 5\text{nm}$ [1, 4]). On the other hand, the radiation-induced leakage current is largely due to parasitic ‘edge’ transistors at the gate-diffusion edge-interfaces where the neighboring thick-oxide STI layer may trap charges. The parasitic ‘edge’ transistors undesirably introduce parasitic radiation-induced leakage currents (I_{ri} ; see the two dotted arrows at the two edges in Fig. 1 (a)). Between the PMOS and NMOS transistors, I_{ri} of NMOS transistors is more significant [3, 8].

Fig. 1 Drain current (I_d) and radiation-included leakage current (I_{ri}) in a transistor based on: (a) single diffusion region, and (b) multiple diffusion regions (i.e. with 2 fingers)

Although there are a few RHBD layout practices such as the annular layout and enclosed-source layout [3] reported to mitigate the radiation-induced leakage current, such practices are unfortunately not permitted in the chosen

GlobalFoundries process. Consider the well-established finger layout practice, as depicted in Fig. 1 (b), a large transistor can be folded into two smaller width transistors where their drains (or sources) are shared. This finger layout technique is advantageous to reduce parasitic capacitance, hence resulting in improved speed and low power attributes. However, in the context of TID effects, it undesirably introduces 4 induced-radiation leakage currents (instead of 2 in that in Fig. 1 (a)). In other words, the more fingers used the more possible induced-radiation leakage currents.

In view of the above, we first investigate the TID effects on the GlobalFoundries 65nm low leakage NMOS transistors. Fig. 2 depicts the test board embodying our TID test chip inside the irradiation chamber, and lists the TID test and the process information. For our transistor characterization, the applied TID levels are 0Krad (pre-rad), 10Krad, 20Krad, 30Krad, 50Krad, 100Krad and 500Krad.

Table I tabulates five NMOS transistors that embody respective aspect ratio and number of fingers. The aim of this investigation is twofold. First, the first two transistors (i.e. T1 and T2) are used to investigate the channel length effects. Second, the last three transistors (i.e. T3 to T5) are used to investigate the radiation-included leakage currents with different number of fingers.

Table I
Characterized NMOS Transistors

NMOS ID	Aspect Ratio (W/L)	Number of Fingers (F)	Total Edge Length	Parameter of Interest
T1	2um/0.09um	1	0.18um	Channel length effect
T2	2um/1um	1	2um	
T3	10um/1um	1	2um	Finger effect
T4	10um/1um	4	8um	
T5	10um/1um	10	20um

(a)

TID Testing Information	
TID Test Standard	MIL-STD-883 TM1019 Condition A
TID Range	0 – 500 Krad (Si)
Test Temperature	25° C
Process Information	
Process	GlobalFoundries 65nm CMOS
Process Threshold	Low Leakage Option ($V_T \approx 0.5V$)
Gate Oxide Thickness	$\approx 2.6nm$

(b)

Fig. 2 TID tests: (a) test board inside the chamber, and (b) TID testing and process information

Fig. 3 depicts the characterization of drain current (I_d) versus gate voltage (V_{gs}) for the NMOS transistors T1 and T2. Note that they embody the same channel width ($W=2\mu m$) and different channel lengths ($L=0.09\mu m$ and $1\mu m$, respectively). As expected, the TID effect of threshold voltage shift is not observed in both T1 and T2. On the other hand, the TID radiation-induced leakage current is however not observed, and the vanished leakage current effect is largely attributed to the relatively high substrate doping concentration of the process [9] (the doping concentration of GlobalFoundries 65nm CMOS is $\sim 6 \times 10^{16}/cm^3$).

Fig. 3 I_d versus V_{gs} of T1 ($L=90nm$) and T2 ($L=1\mu m$)

(a)

(b)

(c)

Fig. 4 I_d versus V_{gs} of NMOS with different numbers of finger (a) $F=1$, (b) $F=4$ and (c) $F=10$

Figs. 4 (a), (b) and (c) depict the characterization of I_d versus V_{gs} for the NMOS transistors T3, T4 and T5 respectively; the three NMOS have the same channel width and channel length ($W=10\mu\text{m}$ and $L=1\mu\text{m}$) and different number of fingers ($F=1, 4$ and 10 , respectively). Their total edge lengths (i.e. poly over the edge of diffusion layers) are $2\mu\text{m}$, $8\mu\text{m}$ and $20\mu\text{m}$ respectively. The TID effect is not observed in the three NMOS transistors at $\text{TID} \leq 100\text{Krad}$. Nonetheless, it is interesting to observe that, at $\text{TID}=500\text{Krad}$, the TID radiation-induced leakage current is pronounced in multi-finger NMOS T4 and T5.

Fig. 5 depicts the comparison of I_d versus V_{gs} for T3, T4 and T5 at $\text{TID}=500\text{Krad}$. It is observed that the TID-induced leakage current increases monotonically as the number of fingers increases. Specifically, the TID-induced leakage current increases $18\times$ and $57\times$ for $F=4$ and $F=10$ respectively when compared to that for $F=1$. Viewed differently, each additional $1\mu\text{m}$ edge length contributes $\sim 3\times$ more radiation-included leakage current. This observation is particularly valuable in determining the layout strategy both for analog circuits and digital circuits, and for subthreshold digital circuits that embody a large number of transistors.

Fig. 5 Comparison of I_d of T3, T4 and T5 at 500Krad

III. RADIATION-INDUCED LEAKAGE ENERGY ON DIGITAL CELLS

We further investigate the TID effects for digital library cells based on the RHBD template reported in [10]. The digital library cells are realized using the same GlobalFoundries 65nm CMOS process. With 2-input NAND gates as the basic cells, Fig. 6 depicts the basic test structure that forms a ring oscillator. The enable signal EN triggers the oscillating function. The other library cells (with their inputs connected for each cell) are similarly constructed in the same test structure. In our experiment, we made the ring oscillator self-oscillating and recorded its average energy (per ring operation) at various TID levels, ranging from 0Krad, 20Krad, 50Krad, 100Krad, 200Krad, 300Krad, and 500Krad¹. The other TID testing condition is the same as that mentioned in Fig. 2.

¹ This set of TID dosages was chosen after the feedback of the transistor characterization in Section II.

Fig. 6 The test structure for TID tests

Table II tabulates 3 NAND and 3 NOR library cells with various numbers of fingers for their layout realizations. For brevity, we only indicate the NMOS transistors (as PMOS transistors would unlikely introduce significant radiation-induced leakage currents). Their total edge length that introduces radiation-included leakage current is also provided. For NAND library cells, the NMOS transistor stacking (from the output to the ground) is required. For NOR library cells, all the NMOS transistors can be connected between the output and the ground.

Table II
TID Test: Digital Library Cells

Library Cells	No. of Fingers per NMOS	Total Edge Length	Stacking No.
2-NAND	4	1.44 μm	2
3-NAND	6	3.24 μm	3
4-NAND	6	4.32 μm	4
2-NOR	4	1.44 μm	1
3-NOR	6	3.24 μm	1
4-NOR	8	5.76 μm	1

Consider first the NAND library cells. Fig. 7 depicts the average energy of the 2-input, 3-input and 4-input NAND library cells at various TID dosages. Interestingly, from Fig. 7, we do not observe any insignificant energy changes even when the TID level is high, e.g. $> 100\text{Krad}$; their measured energy variations are within 14%. We attribute the stacking transistor effect [11] that in turn mitigates the leakage currents (including the radiation-induced leakage currents). Put simply, the NAND library cells are structurally more radiation-hardened to mitigate the radiation-induced leakage current. Hence, the finger technique can be safely adopted for their layout realizations.

Fig. 7 NAND library cells: average energy @ various TID levels

Consider now the NOR library cells. Fig. 8 depicts the average energy of the 2-input, 3-input and 4-input NOR library cells at various TID levels. For the 2-input and 3-input NOR library cells, we similarly do not observe much energy variations at various TID levels; their energy variations are within 14%. However, the 4-input NOR library cells dissipate much higher energy at high TID levels. At TID = 500Krad, its average energy increases by 51% attributed to the increased radiation-induced leakage currents. This observation agrees well with the experimented results in Section II earlier. Put simply, we account the relative small total edge length (see Table II) for the small energy variations for the 2-input NOR and 3-input NOR library cells. Conversely, for the 4-input NOR library cells, the total edge length is relatively large, and hence the radiation-induced leakage currents are increasingly more pronounced.

Fig. 8 NOR library cells: average energy @ various TID levels

IV. RECOMMENDATIONS: TRANSISTOR SIZING AND LAYOUT IMPLEMENTATION FOR ANALOG AND DIGITAL CIRCUITS

On the basis of experiment results mentioned in Sections II and III, we make the following discussions and recommendations² for the transistor implementation based on the GlobalFoundries 65nm CMOS process.

For analog circuits, if the TID levels are low (e.g. < 100Krad; this subjects to the specific orbits or applications), it is acceptable to realize large transistors (with either large width or large length or both) and to adopt the finger technique for their ensuing layout realization. However, if the TID level is large, the finger technique should be avoided.

For digital circuits, if the TID levels are low (e.g. < 100Krad; this subjects to the specific orbits or applications), the same recommendation (to analog circuits) can be adopted. If the TID level is large, this leads to a few possible options for various digital cells. Overall, the recommendations include the following. First, small transistors (with small width and length) could be prioritized and considered (at the disadvantage of slower speed). Second, for large transistors,

the finger technique can be adopted for NAND-type library cells (i.e. with transistor stacking) but not for NOR-type library cells (without transistor stacking). Third, if speed is not critical, the duplicated stacking transistors could be considered as a means to reduce leakage currents.

V. CONCLUSIONS

In conclusion, the TID effects on GlobalFoundries 65nm CMOS process are insignificant at low TID levels (≤ 100 Krad). However, at high TID=500Krad, it is interesting to observe that the TID-induced leakage current is increasingly pronounced as the number of fingers increases, and this observation is important for realizing analog and digital circuit (including their operation at the near/sub threshold region) for space-and-satellite applications. Several RHBD techniques to accommodate for the said TID-induced leakage current have also been recommended.

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² The recommendations are based on the assumption that the annular and enclosed-source layout practices are not permitted.