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Study of the electrical and chemical properties of the multistep deposited and two-step (ultraviolet ozone cum rapid thermal) annealed HfO_2 gate stack

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The authors show that the $\text{TiN}/\text{HfO}_2/\text{SiO}_x$ gate stack, formed via multistep deposition cum *two-step* anneal [comprising a room-temperature ultraviolet ozone (RTUVO) anneal and a subsequent rapid thermal anneal (RTA) at 420°C], exhibits more superior electrical characteristics as compared to the gate stacks formed via multistep deposition cum single-step anneal (either RTUVO anneal or 420°C RTA). The former exhibits more than an order of magnitude smaller gate current density, a 14-fold increase in the time-to-breakdown, and reduced positive oxide trapped charge as compared to the latter. The enhanced performance and reliability are attributed to the improved formation of $\text{Hf}-\text{O}$ bonds in HfO_2 , resulting from the efficient incorporation of oxygen atoms facilitated by the thermal activation of the absorbed ozone. The findings provide insights into the improvement mechanism by the two-step anneal method for high- k last integration scheme. © 2015 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4936893>]

I. INTRODUCTION

High- k last integration, by virtue of low-thermal-budget, allows the high- k metal oxide integration into MOSFET without undergoing phase change in conjunction with limited interfacial SiO_x layer (IL) regrowth, thereby achieving sub-1-nm equivalent oxide thickness (EOT) scaling with preserved high- k film quality.^{1,2} However, with reduced IL thickness, the gate stack reliability margin would be compromised since the high- k oxide grown at low temperature is usually loosely packed and inherently defective with high density of oxygen vacancies (V_{O} 's). This gives rise to gap states leading to transient charge trapping (hence threshold voltage instability) and gate leakage current.^{3–5} Attempts to reduce V_{O} density via various annealing methods were reported,^{5–7} but the high temperature involved limits the EOT scaling due to an increase in the IL thickness. Low temperature annealing such as multistep deposition cum room-temperature ultraviolet ozone (RTUVO) anneal, on the other hand, yields only marginal improvement.⁸ The ability to optimize the high- k oxide quality under low thermal-budget is crucial for sub-1-nm EOT scaling. It was recently shown by our group that the multistep deposition cum two-step [comprising a RTUVO and a subsequent RTA repeated each time after a specific number of atomic-layer-deposition (ALD) cycles] annealing method could significantly reduce the gate current density, J_g , and enhances the breakdown (BD) strength of a 0.75-nm EOT HfO_2/TiN gate stack.⁹ However, the underlying mechanism is unclear due to a lack

of understanding on the microscopic changes that have occurred. The improvements cannot be explained with the high- k densification and reduction in precursor-related impurities since a lesser J_g reduction was achieved for the case when the order of the annealing steps was reversed [i.e., RTA-ultraviolet ozone (UVO) sample] and for the case annealed with only RTA.

In this paper, we present a systematic study of the electrical and chemical properties of HfO_2 gate stack, formed via multistep deposition cum two-step annealing method, by using scanning tunneling microscopy (STM), electron energy-loss spectroscopy (EELS), and x-ray photoelectron spectroscopy (XPS). The microscopic data show that the improved performance and reliability of the gate stack is attributed to the enhanced oxygen content (thereby an increase of the $\text{Hf}-\text{O}$ bond density) in the HfO_2 , indicating that oxygen is most efficiently incorporated into the HfO_2 by the UVO-RTA anneal as compared to the other methods.

II. EXPERIMENT

An approximately 1-nm thermal oxide was intentionally formed via rapid thermal oxidation on 150-mm prime grade p-Si (100) substrate. The substrate was split into smaller pieces prior to ALD of 28-Å HfO_2 film at 250°C under 0.2 Torr. Tetrakis (dimethylamino) hafnium was used as the Hf reactant precursor and H_2O was used as the oxidizing agent. The HfO_2 film was grown via multistep ALD cum two-step annealing method.⁹ The ALD was divided into four steps. In each step, a ~ 0.7 -nm HfO_2 film was deposited and then subjected to *ex situ* RTUVO for 1 min followed by

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FIG. 1. (Color online) High-resolution cross-sectional transmission electron micrograph of the (a) as-dep, (b) RTA, (c) RTA (1000 °C), (d) UVO, (e) UVO-RTA, and (f) RTA-UVO samples. Almost all the samples show identical HfO₂ and SiO₂ IL thicknesses except for the RTA (1000 °C), which exhibits a thicker IL.

RTA at 420 °C (unless stated otherwise) in N₂ for 30 s (henceforth denoted as UVO-RTA gate stack). No high temperature annealing was performed so as to mimic the high-*k* last process. During UVO anneal, the ozone (~500–1000 ppm) was produced via interaction between oxygen and UV illumination (254-nm wavelength) generated by a low-pressure Hg vapor grid. For comparison, control samples with (1) as-deposited (as-dep) HfO₂ (i.e., without receiving any anneal), (2) HfO₂ annealed with either UVO (Ref. 8) or RTA (Ref. 6) only after each deposition step, and (3) HfO₂ subjected to a reversed two-step anneal (i.e., RTA precedes UVO anneal in each deposition step) were prepared. The STM study was performed on blanket-deposited samples in ultrahigh vacuum (~10⁻¹⁰ Torr) under controlled temperature. The bias voltage V_s was applied to the p-Si, and the probe (Pt/Ir) was grounded. On some samples, TiN was sputtered and patterned to form MOS capacitors for electrical measurement. All the devices were subjected to a final forming gas anneal at 425 °C for 30 min.

III. RESULTS AND DISCUSSION

High-resolution transmission electron microscopy confirms almost identical HfO₂ film and IL thicknesses for the various gate stacks (Fig. 1), except for a thicker IL in the RTA (1000 °C) sample induced by high temperature annealing. Figure 2(a) shows the high-frequency capacitance versus gate voltage (C - V_g) characteristics (each C - V_g curve is an average of 20 devices) of the TiN/HfO₂/IL gate stacks subjected to various annealing conditions. Relative to the as-dep sample (denoted by open circle), only samples subjected to UVO annealing (i.e., UVO, RTA-UVO, and UVO-RTA samples) show evidently more positive flat band voltage (V_{FB}). V_O 's typically exist as deep positively charged defect levels, V_O^{2+} , and are the dominant state in high-*k* oxide.¹⁰ The positive V_{FB} shift, therefore, clearly indicates a reduced density of the positive oxide trapped charge in the high-*k* resulting from UVO annealing,¹¹ similar to that achieved in O₂ annealing.¹² On the other hand, only a marginal V_{FB} shift is observed for gate stack annealed with only RTA. Compared to the UVO sample, an incremental positive V_{FB} shift for the RTA-UVO sample indicates that the preceding RTA had a subtle effect on the V_O density. In other words, a reduced density of V_O in the sample is attributed mainly to the UVO anneal. Interestingly, however, an additional positive V_{FB} shift, corresponding to a further reduction of the

positive oxide trapped charge, can be observed for the UVO-RTA sample as compared to RTA-UVO sample. This implies further removal of V_O 's by the 420 °C RTA carried out after the UVO anneal. The nearly identical (except for the one annealed at 1000 °C) EOTs of the respective gate stacks (inset) indicate no further increase in the IL thickness after annealed at 420 °C in N₂, consistent with that observed in Ref. 12. Clearly, the multistep deposition and two-step

FIG. 2. (Color online) (a) Quasistatic high-frequency (1 MHz) capacitance-voltage (C - V_g) characteristics of the TiN/HfO₂/IL MOS capacitors subjected to various annealing conditions. The inset shows almost identical EOT for all the samples except for the one annealed at 1000 °C. The gate stack work function is estimated to be 4.7 eV, typical of the TiN/HfO₂ stack. The lesser accumulation capacitance (~1.4 μF/cm² at -1.15 V) is because of the finite capacitance of the lowly doped (~6 × 10¹⁵ cm⁻³) p-Si substrate (Debye length ~500 Å). (b) Average gate current density-voltage (J_g - V_g) characteristics of the various gate stacks measured under room temperature (300 K). More than ten devices were measured for each split.

anneal did not affect the overall gate stack thickness. The larger EOT of the gate stack annealed at 1000 °C is ascribed to an increase in the IL thickness.¹³

The gate current density J_g vs V_g curves are shown in Fig. 2(b). The largest J_g of the 1000 °C RTA sample is due to the crystallization of HfO_2 induced by high temperature anneal.^{14,15} From the current map obtained by STM [Fig. 4(b)(i)], leakage current was shown to preferentially center near grain boundaries (GBs) of the crystallized HfO_2 ,¹⁵ thus making this location an ideal BD spot. Relative to the as-dep sample, the J_g of the 420-°C RTA sample (denoted by filled circle) is about an order of magnitude lower (i.e., $\sim 1.7 \times 10^{-5}$ A/cm² at $V_{\text{FB}} - 1$). It was shown that 400–450 °C anneal could densify a high- k film without inducing crystallization.¹⁶ The improvement in J_g may be attributed to the removal of carbon-related impurities and unreacted precursor ligands from the HfO_2 film by the low temperature anneal,¹⁷ which helped retain the amorphous structure. For the gate stack annealed with only UVO, similar improvement in the J_g was obtained (denoted by open triangle). However, a further reduction in J_g is achieved for the RTA-UVO sample. This implies that the removal of V_{O} 's from the HfO_2 by the UVO anneal could proceed more efficiently after the impurities were driven off by the 420 °C RTA. Further reduction in J_g (by about an order of magnitude relative to the sample annealed with either only UVO or RTA) is achieved when the sequence of the two anneals is reversed, i.e., high- k sublayer deposited in each step was annealed with UVO then followed by 420 °C RTA, consistent with that observed in Ref. 9. It is believed that the subsequent RTA not only drove off the impurities (thus enabling more efficient removal of V_{O} 's), it also provided the thermal activation, which enhanced the rate of structural defect repair.

The time-to-breakdown (T_{BD}) data of the various gate stacks subjected to constant gate (-4.8 V) voltage stressing at 125 °C (Fig. 3) show a trend consistent to our earlier work in Ref. 9. The T_{BD} distributions of the UVO and RTA samples are clustered together, in agreement with the observation on the very similar J_g of these samples depicted in Fig. 2(b). An evidently longer T_{BD} is observed for the two-step annealed samples, with the UVO-RTA sample having ~ 4 and ~ 12 times longer T_{BD} as compared with the RTA-UVO and as-dep counterparts, respectively. From the T_{BD} result in Ref. 9, however, the UVO-RTA sample exhibits only ~ 9 times longer T_{BD} as compared with the as-dep sample. The larger improvement margin in Fig. 3, therefore, is ascribed to the improved IL quality. It is believed that the two-step annealing method not only “repair” the structural defects in high- k , but also a partial of the defects that exist in the IL. The result clearly shows that the BD strength of gate stacks is significantly enhanced by the two-step anneal method. A greater increase in the T_{BD} of the UVO-RTA sample consistently shows that when the RTA is preceded by the UVO anneal, a more efficient removal of oxide traps is achieved.

Figure 4(a) shows the constant-current topography images of the various HfO_2 gate stacks acquired under a fixed positive bias voltage V_s (~ 2.5 V) and tunneling current I_t (~ 15 pA) held constant by an electromechanical feedback

FIG. 3. (Color online) Time-to-breakdown T_{BD} distribution of the various $\text{TiN}/\text{HfO}_2/\text{IL}$ MOS capacitors subjected to constant gate (-4.8 V) voltage stressing at 125 °C. Capacitor area: $50 \times 50 \mu\text{m}^2$. The stress test was not performed on the gate stack annealed at 1000 °C since its breakdown voltage is less than 4.8 V.

circuit. The probability of electrons injected from the STM probe at the tunneling junction was predominantly determined by the vacuum gap that separated the probe from the dielectric surface. As the probe was scanned across the high- k surface, the variations of the high- k structure would affect the electrons' injection probability, thereby resulting in a change in I_t .^{14–16,18} A feedback circuit would sense the change in I_t and then adjusted the vacuum gap to keep I_t constant. Microscopic changes in the vacuum gap, needed to achieve a constant I_t as the probe was scanned across the high- k surface, gave rise to the contrast in the topography image in Fig. 4(a), which corresponds to the convolution data of the high- k morphology and local conductivity induced by the presence of electronic traps. The bright regions correspond to locations where the probe retracts from the high- k surface, either due to microp protrusions and/or local oxide conductance due to electronic traps.¹⁹ The morphology and electronic properties of the high- k stack, however, can be demarcated via reference to the corresponding current maps [Fig. 4(b)] obtained by constant imaging tunneling spectroscopy (CITS) technique.¹⁴ The contrast in the current map denotes the variations of I_t across the high- k gate stack, i.e., bright shades represent high leakage sites due to electronic traps.

The presence of grains in the RTA (1000 °C) sample [Fig. 4(a)(i)], denoted by bright regions with an average size of < 20 -nm, is evident; note that the “leaky” GBs encompassing the less conductive grains in the corresponding current map [Fig. 4(b)(i)].^{14,15,19} These features, however, are clearly absent for the as-dep, UVO, RTA, RTA-UVO, and UVO-RTA samples. The bright shades in the topography images of these samples are dispersed randomly throughout, suggesting that the high- k films are in amorphouslike structure. Moreover, the leakage density in the corresponding current maps is clearly reduced, with the two-step annealed samples showing the lowest leakage density [Figs. 4(b)(v) and 4(b)(vi)], in good agreement with the corresponding lowering of the average I_t of the scanned area [Fig. 5(a)]. It should be

FIG. 4. (Color online) Row (a) depicts the $100 \times 100 \text{ nm}^2$ constant-current STM topographical images of the (i) RTA (1000°C), (ii) as-dep, (iii) UVO, (iv) RTA, (v) RTA-UVO, and (vi) UVO-RTA HfO_2 gate stacks acquired at $V_s = 2.5$ V and $I_t = 15$ pA. The bright regions correspond to locations where the probe retracts from the high- k surface due to microprotrusions and/or local oxide conductance (Ref. 18). Row (b) depicts the corresponding current maps (at $V_s = -3$ V). Bright shades denote regions of higher I_t .

FIG. 5. (Color online) (a) Corresponding average I_t - V_s curves extracted from the $100 \times 100 \text{ nm}^2$ scanned area depicted in Fig. 4(b). Bias voltage V_s was swept from $+5$ to -5 V. All the I_t - V_s curves converge at $V_s \sim +5$ V as a result of the feedback circuit adjust the vacuum gap between the probe and high- k surface to achieve the same I_t at a given V_s . (b) Corresponding statistical spread in the I_t of the current maps [$V_s = -3$ V; traps in the IL (Ref. 18) was probed under substrate injection biasing] depicted in Fig. 4(b). To facilitate comparison, I_t is normalized to the average I_t of the RTA (1000°C) sample.

mentioned that during CITS mode, the vacuum gap between the probe and the high- k surface was already adjusted by the feedback system to achieve the same I_t at a given V_s prior to the local I_t - V_s measurement; therefore, all the I_t - V_s curves converge at $V_s \sim 5$ V. The difference between the STM-measured I_t - V_s and that obtained from the MOS devices [see Fig. 2(b)] is attributed to the presence of vacuum gap between the probe and the high- k surface, which absorbs part of the V_s applied across the gate stacks. Therefore, the I_t measured by STM in Fig. 5(a) does not reflect the actual value and it is expected to be larger. The stress-induced oxide degradation rate and the corresponding electrical uniformity of the respective gate stacks are examined by monitoring the evolution of the I_t statistical distribution (at $V_s = -3$ V) in a given area under repeated STM scanning [Fig. 5(b)]. The gate stack was stressed by extending the voltage-ramp during local I_t - V_s measurement under CITS mode. Electronic trap generation in the IL is probed by the I_t extracted at a negative V_s (i.e., electrons are injected from the Si substrate), whereas the electrical uniformity is monitored by the spread of I_t distribution.¹⁴ To facilitate the comparison, all the I_t are normalized to the average I_t of the RTA(1000°C) sample (arbitrarily selected). A lesser increase in the average negative I_t as well as its spread is evident for the two-step annealed samples compared to the single-step annealed counterparts, pointing to a better immunity against traps generation and a lower degree of I_t nonuniformity. Both the two-step annealed samples exhibit a nearly identical distribution spread. The results in Fig. 5(b) are consistent with the current maps in Fig. 4(b), which clearly shows the impact of the high- k quality on the stress-induced degradation of the underlying IL.

The chemical structures of the various HfO_2/IL gate stacks were examined by EELS measurements. Figure 6(a) shows the background corrected O K edge spectra of the HfO_2 layer for the various samples, which exhibit the characteristic double peaks at the edge onset (one centered at

Fig. 6. (Color online) Background corrected O K edge EELS spectra of (a) 2.5-nm HfO₂ layer, and (b) 1-nm SiO₂ IL for the various gate stacks. The peak intensity corresponds to the amount of local oxygen atoms (i.e., low peak intensity signifies increase oxygen deficiency). Double peaks characteristic can be seen in the O K edge spectra of HfO₂, consistent with the literature (Ref. 22). A growing 537.8 eV peak intensity is observed in the EELS spectra of HfO₂ and SiO₂ IL for the samples annealed in UVO.

~533.5 eV and the other centered at ~537.8 eV), consistent with those reported in the literature.¹⁷ The ratio of the two peaks with comparable heights is nearly identical for most of the samples, except for the sample prepared using the UVO-RTA method, which shows ~40% taller 537.8 eV peak relative to that at the shoulder (centered at 533.5 eV). From the O K edge spectra of SiO₂, only a single peak centered at ~537.8 eV is observed and this peak is attributed to the multiple scattering of the ejected O 1s electron from a given oxygen atom to its six second-nearest neighboring oxygen atoms (first O shell).²⁰ Therefore, the 537.8 eV peak observed in the O K edge spectra of the HfO₂ may be ascribed to the similar mechanism. The peak intensity reflects the amount of local oxygen atoms (i.e., the peak intensity will drop with an increase in oxygen deficiency). Relative to the as-dep sample, the ~537.8 eV peak intensity is significantly enhanced by the UVO-RTA anneal, followed by the UVO anneal and the RTA-UVO anneal. This confirms that the UVO-RTA method is most efficient in incorporating oxygen atoms into the HfO₂ film as compared with the methods. On the other hand, an almost similar trend is also observed for the O K edge spectra of the underlying SiO₂ IL [Fig. 6(b)]. The 537.8 eV peak can be seen growing evidently for the samples annealed in UVO. More interestingly,

the intensity of the peak centered at ~560 eV is enhanced by the two-step anneal. The 560 eV peak was also observed in the SiO₂ EELS results reported in literature and was attributed to the stretched O–O bonds.²¹ This implies that, apart from high-*k*, the quality of the underlying IL was also improved under UVO anneal, thereby contributing to a larger reliability improvement margin relative to the 0.75-nm EOT HfO₂/TiN gate stack,⁹ as evidenced in the TDDDB results (Fig. 3). In addition, a small peak (centered at ~533 eV) with a very low intensity can be seen at the shoulder of the 537.8 eV peak as opposed to the SiO₂ EELS result (which shows no peak at 533.5 eV). This is ascribed to the possible interference signal from the HfO₂ in the IL O K edge spectra.

The inference is also borne out in the XPS measurements using monochromatic Al K α x-ray source ($h\nu = 1486.7$ eV). The O 1s and Hf 4f XPS spectra were referenced to C 1s peak binding energy (BE) at 285 eV. The Hf 4f spectra of the samples are shown in Fig. 7(a). Relative to the as-dep sample, the Hf 4f_{7/2} peak BE of both the RTA and RTA-UVO samples show a slight incremental shift to 17.1 eV in the vicinity of Si (i.e., 17~17.5 eV), indicating the presence

Fig. 7. (Color online) XPS core-level spectra of (a) Hf 4f and (b) Si 2p obtained from the HfO₂/IL gate stacks annealed at various conditions.

of thin Hf silicates (HfSi_xO_y) at the interface region.²² A larger incremental shift to 17.6 eV for the RTA (1000 °C) sample is attributed to the formation of a thicker Hf silicate resulting from the high temperature involved, consistent with the corresponding TEM in Fig. 1(c). For the sample annealed with only UVO, however, a trend similar to the as-dep sample is observed. It is interesting to note that when the UVO anneal precedes the RTA in the two-step annealed sample (i.e., UVO-RTA), a lesser Hf 4f_{7/2} peak BE shift is observed. In addition, the intensity at the valley between Hf 4f_{7/2} and Hf 4f_{5/2} peaks is comparable to that of the as-dep and UVO samples. This suggests no obvious Hf silicate formation, even if the formation occurs, only a thin layer is present at the interface region. In Fig. 7(b), the Si 2p XPS core-level spectra were referenced to the substrate Si 2p peak BE at 99 eV. The ~99 eV peak is attributed to the photoelectrons from the Si-Si bonds in substrate whereas the higher BE peak centered at ~103 eV is attributed to the

photoelectrons from SiO₂ and Hf silicate. Except for the RTA (1000 °C) sample, the rest of the samples exhibit almost identical trend, implying a stable oxidation state of Si. The Hf-O-Si peak centered at ~102.5 eV for the RTA (1000 °C) sample clearly indicates the presence of Hf silicate. Figure 8(a) shows the corresponding O 1s spectra of the various samples. The major peak centered at BE ~530 eV is attributed to the Hf-O bonds in HfO₂ (Ref. 23) whereas the peak centered at BE ~531–532 eV at the shoulder corresponds to the Hf-O-Si bonds in Hf silicate and/or Si-O bonds in SiO₂.^{22–24} The $I_{(\text{Hf-O})}/I_{(\text{Hf-O-Si, Si-O})}$ intensity ratio reflects the relative content of HfO₂ in the respective gate stacks [Fig. 8(b)]. It is observed that the UVO sample shows a higher intensity ratio relative to the as-dep sample. Since the Hf 4f spectra of both samples are identical (i.e., no obvious Hf silicate formation), an increase in the intensity ratio of the former must be necessarily contributed by the higher HfO₂ content rather than a reduced Hf silicate content. A further increase in the ratio is observed in the UVO-RTA sample. This indicates more Hf-O bonds were formed via the incorporation of oxygen (i.e., removal of V_{O} 's) into HfO₂ film when thermal activation was provided by the RTA step.

IV. CONCLUSIONS

A detailed and systematic study of the electronic and chemical properties of the multistep deposited and two-step annealed (comprising a RTUVO anneal and a subsequent RTA at 420 °C) HfO₂/IL gate stack was presented. The improved performance and reliability of the HfO₂/IL gate stack is attributed to the more efficient incorporation of oxygen in the HfO₂ film by the UVO-RTA method, thereby increasing the density of Hf-O bonds, as revealed by the EELS and XPS analyses. In the process, the V_{O} -related electronic traps are removed. The ability of the UVO-RTA method to efficiently incorporate oxygen in the high- k oxide under low thermal budget processing makes it a promising means for enhancing the HKMG performance and reliability in the high- k last integration scheme.

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Fig. 8. (Color online) (a) XPS core-level spectra of O 1s obtained from the HfO₂/IL gate stacks annealed at various conditions. (b) $I_{(\text{Hf-O})}/I_{(\text{Hf-O-Si, Si-O})}$ intensity ratio of the respective samples obtained from their corresponding O 1s spectra in (a). The intensity of ~530 and ~531–532 eV peaks correspond to the relative amount of HfO₂ and Hf silicate/SiO_x content, respectively.

¹E. Simoen, A. Veloso, Y. Higuchi, N. Horiguchi, and C. Claeys, *IEEE Trans. Electron Devices* **60**, 3849 (2013).

²C. L. Hinkle *et al.*, *IEEE Symposia on VLSI Technology* (2010), p. 183.

³E. Cartier, B. P. Linder, V. Narayanan, and V. K. Paruchuri, *IEEE International Electron Devices Meeting* (2006), p. 57.

⁴K. Tse and J. Robertson, *Microelectron. Eng.* **84**, 663 (2007).

⁵T. Naito, C. Tamura, S. Inumiya, R. Hasunuma, and K. Yamabe, *Jpn. J. Appl. Phys.* **46**, 3197 (2007).

⁶T. Nabatame *et al.*, *IEEE Symposia on VLSI Technology* (2003), p. 35.

⁷H. Sim, H. Chang, and H. Hwang, *Jpn. J. Appl. Phys.* **42**, 1596 (2003).

⁸L. Wu *et al.*, *IEEE International Electron Devices Meeting* (2010), p. 273.

⁹K. S. Yew, D. S. Ang, and L. J. Tang, *IEEE Electron Device Lett.* **34**, 295 (2013).

¹⁰K. Xiong, J. Robertson, and S. J. Clark, *Phys. Status Solidi B* **243**, 2071 (2006).

- ¹¹Y. Zhao, K. Kita, K. Kyuno, and A. Toriumi, *Jpn. J. Appl. Phys.* **46**, 4189 (2007).
- ¹²Y.-L. Yang *et al.*, *IEEE Electron Device Lett.* **33**, 1183 (2012).
- ¹³B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, *Appl. Phys. Lett.* **76**, 1926 (2000).
- ¹⁴K. S. Yew, D. S. Ang, L. J. Tang, K. Cui, G. Bersuker, and P. S. Lysaght, *J. Electrochem. Soc.* **158**, H1021 (2011).
- ¹⁵K. S. Yew, D. S. Ang, and G. Bersuker, *IEEE Electron Device Lett.* **33**, 146 (2012).
- ¹⁶J. F. Conley, Y. Ono, and D. J. Tweet, *Appl. Phys. Lett.* **84**, 1913 (2004).
- ¹⁷M. P. Agustin, G. Bersuker, B. Foran, L. A. Boatner, and S. Stemmer, *J. Appl. Phys.* **100**, 024103 (2006).
- ¹⁸Y. C. Ong *et al.*, *Appl. Phys. Lett.* **91**, 102905 (2007).
- ¹⁹Y. C. Ong, D. S. Ang, K. L. Pey, Z. R. Wang, S. J. O'Shea, C. H. Tung, T. Kawanago, K. Kakushima, and H. Iwai, *Appl. Phys. Lett.* **92**, 022904 (2008).
- ²⁰D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, *Nature* **399**, 758 (1999).
- ²¹Z. W. Yuan, S. Csillag, M. A. Tafreshi, and C. Colliex, *Ultramicroscopy* **59**, 149 (1995).
- ²²M. H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D. H. Ko, J. H. Lee, N. I. Lee, and K. Fujihara, *Appl. Phys. Lett.* **81**, 472 (2002).
- ²³T. P. Smirnova, L. V. Yakovkina, V. N. Kitchai, V. V. Kaichev, Yu. V. Shubin, N. B. Morozova, and K. V. Zherikova, *J. Phys. Chem. Solids* **69**, 685 (2008).
- ²⁴G. Aygun and I. Yildiz, *J. Appl. Phys.* **106**, 014312 (2009).