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2015

Kandasamy, K., Vilathgamuwa, M., & Tseng, K. J. (2015). Inter-module state-of-charge balancing and fault-tolerant operation of cascaded H-bridge converter using multi-dimensional modulation for electric vehicle application. IET Power Electronics, 8(10), 1912-1919.

<https://hdl.handle.net/10356/81322>

<https://doi.org/10.1049/iet-pel.2014.0943>

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Inter-Module SOC Balancing and Fault Tolerant Operation of Cascaded H-Bridge Converter Using Multi-dimensional Modulation For Electric Vehicle Application

Abstract— This paper presents a method for module level State-Of-Charge (SOC) balancing and fault tolerant operation of the Cascaded H-bridge (CHB) converter based battery energy storage system for electric vehicle (EV) application. The proposed methods are based on the multi-dimensional PWM (MD-PWM) strategy. It is shown that the proposed methods are conveniently integrated with the PWM generation algorithm. A conceptual design of modular battery pack (or micro-pack) system using lithium-ion cells for the CHB converter is described to show its feasibility for EV application. A brief review on the MD-PWM strategy, and a detailed explanation on the method to integrate the inter-module SOC balancing and fault tolerant control with the PWM generation are presented. Experimental results from the laboratory setup of a five level CHB converter driving an induction motor with a battery system consisting of six 52.8-V 60-Ah (16 lithium-ion cells in series) modules are presented to verify the system operation for fault tolerant control and the proposed SOC balancing method. The results demonstrates the need of SOC balancing, and efficacy of the proposed methods in achieving fault tolerant as well as SOC balanced operation to prolong the system operation.

1 INTRODUCTION

Conventional battery electric vehicles (EV) have a single battery pack with a two-level inverter for motor drive. The battery pack is constructed by interconnecting certain number of electrochemical cells in series (and/or parallel) to achieve required energy and power capacity [1]-[4]. The required power and energy capacity of the battery pack depends on the vehicle size, maximum speed and driving range per charging etc. Among various battery chemistries, lithium-ion technology has been used for EV battery pack construction because of its high power and energy density. Though the lithium-ion cells are of high reliability, the battery packs are susceptible to various faults and combustion hazards [5] - [8]. Any fault in the battery pack or the two-level inverter affects the availability of the vehicle with the conventional design having a single battery pack. A modular battery pack or micro-pack would circumvent this problem and thus could be considered to increase the availability of the vehicle in case of micro-pack fault. The reliability and availability of the vehicle would be increased when the power in each battery micro-packs are controlled independently and also when the system possesses ride through capability under fault conditions. This is achievable using modular power converters. One such system employing cascaded H-bridge (CHB) multilevel converter is discussed in this paper.

Fig. 1 Cascaded H-bridge converter configuration

CHB is one of the important members of the family of multi-level converters [9] including diode clamped converter and capacitor clamped converter, which has its application in medium voltage electric drives [10], STATCOMs [11] etc. CHB has many advantages like modularity, low dv/dt and low voltage Total Harmonic Distortion (THD). However, the main disadvantage of CHB is that it requires isolated DC power supplies and transformer. With the approach of employing battery micro-packs for CHB, this particular disadvantage is circumvented. Many topological variations of CHB have been reported in literature. A three-phase CHB could be either star connected or delta connected. CHB can be classified as symmetrical having equal input DC voltages, and asymmetrical having unequal input DC voltages. The symmetrical star connected CHB based converter with modularized battery system is shown in Fig. 1, in which a generalized N H-bridge units per phase leg is illustrated. For the symmetrical CHB having N number of H-bridges in a phase, the voltage levels L in each phase is given by $L=2N+1$. N is usually called as cascade number. Various modulation techniques like phase shifted multi-carrier PWM (PS-PWM), level shifted multi-carrier PWM (LS-PWM), Space Vector modulation (SVPWM), staircase modulation, selective harmonic elimination (SHE-PWM) etc., are available for CHB multi-level converter [12]-[14]. A generalized modulation strategy called multi-dimensional PWM (MD-PWM) for CHB converter proposed in [15], is employed in this paper to investigate the possibility of module level SOC balancing and fault tolerant operation.

Various fault tolerant operation techniques for CHB converter have been discussed in [16] [17]. Fault in multi-level converters generally refers to the fault in the power electronic switches. In case of CHB, any fault in the power electronic switch requires that particular H-bridge to be bypassed. It requires additional bypass switch for every H-bridge unit. However, in this paper, the bypassing of H-bridge is realized using the zero switching state of the H-bridge. Irrespective of the bypassing technique, all the fault tolerant techniques aim at operating the

CHB to deliver a balanced three-phase current even when some of the H-bridge units are bypassed and not in operation. This has been achieved in two ways. First method is described as ‘without neutral shift’, achieved by disabling one H-bridge unit in the healthy phase legs for every faulty H-bridge, and distributing the load to remaining healthy H-bridge units. Second method is described as ‘with neutral shift’, achieved by adding zero sequence voltage or common mode voltage to the phase voltage reference to generate balanced line-line voltages. The second method is more effective as it does not reduce the capacity of the system, and methods to obtain the zero sequence voltage for PS-PWM have been discussed in [18] [19]. A space vector modulation based fault-tolerant operation of CHB converter utilizing redundant switching state has been proposed in [20]. In this paper, a method for realizing the fault tolerant operation ‘with neutral shift’ using MD-PWM is presented.

The fault tolerant control operates the CHB in such a way that the uneven amount of power are being extracted from the micro-packs, which subsequently results in an imbalance condition among their SOC. The imbalance in SOC of micro-packs is also possible due to change in the battery characteristics over aging, or even battery micro-packs could have been charged to different SOC levels. The entire system has to be stopped even when one of the micro-pack’s SOC reaches the minimum cut-off value. This imbalance in the SOC is undesirable in EV applications, as it affects the driving range of the vehicle. A module level SOC balancing for a grid connected CHB battery energy storage system based on modifying the phase voltage reference with the zero sequence voltage injection and PS-PWM has been demonstrated in [21]. A novel control method for the SOC balancing and micro-pack fault tolerant operation that can be conveniently integrated with the PWM generation algorithm is proposed in this paper. Thus the proposed control methods do not require any extra hardware components. The proposed control method based on MD-PWM and reference phase voltage amplitude is convenient for digital implementation. Preliminary simulation results of the proposed control strategy for SOC balancing in a phase leg of CHB were presented in [22].

A design concept for the battery micro-pack construction for the symmetrical CHB converter in EV application is described in Section 2. The MD-PWM strategy for CHB converter is briefed in Section 3. The proposed inter-module SOC balancing and fault tolerant control using MD-PWM are described in Section 4. The operation of the proposed system and control methods are verified through experimental results from the laboratory hardware prototype and the results are presented in Section 5.

2 BATTERY MICRO-PACK DESIGN CONCEPT

This section describes a method for designing a modularized battery micro-packs using lithium-ion cells for the CHB converter to show its feasibility for the EV application. The basic design parameters of the EV battery

pack are the maximum power required for the maximum acceleration with the given vehicle weight, and the maximum energy capacity of the battery pack required for certain driving range. The voltage of the battery pack should be in accordance with the rated voltage of the drive motor. In order to generate a line-line voltage with peak value of V_p with CHB converter, the required micro-pack voltage is given by,

$$V_{bat} \geq \frac{V_p}{\sqrt{3}N} \quad (1)$$

where N is the number of H-bridge units with battery micro-pack in a given phase leg of the CHB converter. The rated power of the battery pack should be not less than P_{acc} , the power required for the maximum acceleration of the vehicle. To achieve this maximum power with CHB converter and micro-packs, the rated power of each micro-pack should be

$$P_{bat}^{max} \geq \frac{P_{acc}}{3N} \quad (2)$$

With V_{bat} and P_{bat}^{max} , the number of cells and the capacity (Ah) of the lithium ion cell for a battery micro-pack can be manipulated. In this paper, the chosen values for investigation are $V_p = 400$ V and $P_{acc} = 100$ kW. These values are considered for the proposed design of micro-pack, so that it can be compared with the conventional battery pack design of a commercially available electric car: Nissan Leaf battery pack (24 kWh and 360 V) comprising of 192 Lithium-ion cells [4]. The battery pack has the rated power of about 100 kW. The required V_{bat} should be ≥ 115.5 V, 77.7 V, 46 V, and the required P_{bat} should be ≥ 16.67 kW, 11.11 kW, 6.6 kW for the CHB with $N = 2, 3, 5$ respectively. For these V_{bat} and P_{bat} , the rated current of the micro-pack I_{bat} should be ≥ 144 A. Any automotive lithium-ion cell with nominal voltage of 3.7 V and the nominal capacity of 35 Ah with maximum discharging capacity of at-least 5C can be chosen. With such lithium cell, the micro-pack can be constructed with 32, 21, and 13 cells in series for $N=2, 3$, and 5 respectively. The total capacity of such CHB system would be ~24 kWh with each micro-pack being 4.14, 2.72, and 1.68 kWh for $N=2, 3$, and 5 respectively. The parameters of the proposed micro-pack design and that of Nissan leaf battery pack are compiled in Table 1. It can be seen that the micro-packs for CHB could be constructed with almost same number of lithium ion cells, even with reduced capacity compared to the conventional single battery pack system with two-level inverter. It has to be noted that the design of Battery Management System (BMS) and thermal management would become complex with micro-pack system.

Table 1 Parameters of Battery Pack

Parameters	Nissan Leaf	CHB (N=2)	CHB (N=3)	CHB (N=5)
Total number of cells	192	192	189	195
Nominal Capacity of each cell (Ah)	60	35	35	35
Total Energy storage capacity (kWh)	24	24.8	24.5	25.3
Pack Nominal Voltage (V)	360	118.4	77.7	48.1

3 CHB AND MULTI-DIMENSIONAL PWM

Multi-dimensional modulation (MD-PWM) proposed in [15] is a generalized modulation approach for a CHB converter, which can be particularized to operate like PS-PWM or LS-PWM. The MD-PWM technique is based on the geometric representation of the output voltage of each H-bridge in co-ordinate axes as shown in Fig. 2. For the cascade number of two ($N = 2$), the control contour is a straight line bounded by a square, whereas for the cascade number of three ($N = 3$), the control region is a plane bounded by a cube. For cascade number more than three, the control region cannot be represented visually but the concept can be extended.

Fig. 2 Control contour representation for MD-PWM

The phase voltage of an i^{th} phase leg averaged over a period is the sum of average voltage outputs of j H-bridge units and is given by,

$$V_i = \sum_{j=1}^N V_{cell,j} \quad (3)$$

Therefore solution to (3) for any desired value of V_i is a point on the line for $N = 2$, and a point on the plane orthogonal to $[+V_{dc,1} ; +V_{dc,2} ; +V_{dc,3}]$ vector for $N = 3$ as shown in Fig. 2. As such, there can be infinite number of solutions to any desired value of V_i . This is a specific advantage of MD-PWM, since it provides an extra

degree of freedom to choose a $V_{cell,j}^*$ depending on a specific design criterion. For instance, MD-PWM was used to control dc-link voltage in a CHB based synchronous rectifier in [23].

Once $V_{cell,j}^*$ is chosen for a desired phase voltage V_i^* in a switching period (T_{sw}), the next step is to determine the switching time and the switching sequence. The switching period is identical to the carrier wave frequency in SPWM. Each H-bridge can take three switching states $S \in [-I, 0, +I]$ which corresponds to the output voltage of $(-V_{dc}, 0, +V_{dc})$. The switching time is calculated using the equations (4) and (5).

During the time $t_{on,j}$, the j^{th} H-bridge cell is clamped to either state $S = +I$ for positive $V_{cell,j}^*$ or to state $S = -I$ for negative $V_{cell,j}^*$. And during the time $t_{off,j}$, the j^{th} H-bridge cell output is maintained zero which is state $S = 0$.

$$t_{on,j} = \frac{V_{cell,j}^*}{V_{dc,j}} \times T_{sw} \quad (4)$$

$$t_{off,j} = T_{sw} - t_{on,j} \quad (5)$$

Though the MD-PWM is easy to implement and can be extended to CHB of any levels, the complexity of this modulation lies in determining the switching sequence and selection of switching period. The smallest possible switching period traces the reference wave more accurately.

4 MICRO-PACK SOC BALANCING AND FAULT TOLERANT CONTROL USING MD-PWM

Each phase leg in CHB has N H-bridge units with a battery micro-pack. Let SoC_i be the average SOC of N battery micro-packs' SOC's (SoC_{i1} to SoC_{iN}) in phase i , with SoC_{ij} being the SOC of j^{th} micro-pack in phase i for all $i \in (A,B,C)$. And SoC is the average of SoC_A , SoC_B and SoC_C , which represents the SOC of the whole system.

$$SoC_i = \frac{1}{N} \sum_{j=1}^N SoC_{ij} \quad (6)$$

$$SoC = \frac{1}{3} (SoC_A + SoC_B + SoC_C) \quad (7)$$

The deviation of SoC_A , SoC_B and SoC_C from SoC is given by,

$$\Delta_i = SoC - SoC_i \quad (8)$$

The deviation of j^{th} micro-pack SOC in i^{th} phase (SoC_{ij}) from its average SOC (SoC_i) is given by,

$$\delta_{ij} = SoC_i - SoC_{ij} \quad (9)$$

i) Inter-phase SOC balancing

If all the phase legs have equal average SOC (i.e., $\Delta_A = \Delta_B = \Delta_C = 0$), then power extracted during motoring operation and the power delivered during charging operation should be distributed equally among three phases. But when the phase legs have difference in their average SOC values, the power extracted from or delivered to each phase leg should be varied according to their average SOC to achieve a balanced operation. This is achieved by adding or subtracting zero sequence voltage of fundamental frequency to the phase voltage references. The zero sequence voltage modifies the phase voltage generated, and hence affects the power extracted from each phase without affecting the output line-line voltage.

The MD-PWD requires the $V_{cell,ij}^*$ to be manipulated in every switching period. A particular design criterion can be used to manipulate $V_{cell,ij}^*$. In order to extract equal amount of power from each battery micro-packs, $V_{cell,ij}^*$ is calculated using,

$$V_{cell,ij}^* = \left(\frac{V_i^*}{N} \right) \quad (10)$$

where V_i^* is the desired average phase voltage over a switching period. To include the inter-phase SOC balancing control in MD-PWM, the reference for each H-bridge unit in (10) is modified into,

$$V_{cell,ij}^* = \left[\frac{(V_i^* - V_{bal}^*)}{N} \right] \quad (11)$$

where V_{bal}^* is the voltage modifier that represents the required zero sequence voltage at every switching period. It is obtained from the reference phase voltage amplitude V_i^* and the SOC deviation. The required voltage modifier to achieve the inter-phase SOC balancing is given by,

$$V_{bal}^* = G_I [f_A \Delta_A V_A^* + f_B \Delta_B V_B^* (1 - f_A) + f_C \Delta_C V_C^* (1 - f_A)(1 - f_B)] \quad (12)$$

where

$$f_i = \begin{cases} \text{floor} \left[\frac{(\Delta_i + |\Delta_i|)}{2 * \Delta_{max}} \right] & ; \forall i \in (A, B, C) \text{ and } |\Delta_{max}| > 0 \\ 0 & ; \forall i \in (A, B, C) \text{ and } \Delta_{max} = 0 \end{cases}$$

$$\Delta_{max} = \max(\Delta_A, \Delta_B, \Delta_C)$$

The V_{bal}^* follows the voltage reference of the phase leg having higher SOC deviation from the average SOC of three phase legs. Magnitude of the V_{bal}^* is determined based on the SOC deviation and the proportionality constant G_I .

The proportionality constant G_I is the percentage of voltage reference that is required to be subtracted from each of the reference phase amplitudes. The value for G_I is obtained from the input power and SOC relation of each H-bridge unit given in Fig. 3(a). G_I is the representation of difference between the amounts of power delivered by each phase legs in CHB, which needs to be modified for certain time period to nullify their SOC differences. In Fig. 3(a), $P_{L,i}$ is the loss and P_i is the active power of i^{th} phase.

Fig. 3 Control block diagram for SOC balancing

- (a) Inter-phase SOC balancing
- (b) Intra-phase SOC balancing

The closed loop transfer function for Fig. 3(a) is given by,

$$\frac{\Delta_i(s)}{P_L(s)} = \frac{\frac{I}{G_I P_i}}{(1 + s \frac{NQ}{100 G_I P_i})} \quad (13)$$

where Q is the maximum capacity (in Joules) of each battery micro-pack. The value for G_I is manipulated from the time constant of the transfer function given by,

$$T = \frac{NQ}{100 G_I P_i} \quad (14)$$

For $N = 2$; $Q = 19008 \text{ J}$; $P_i = 250 \text{ W}$; if $G_I = 0.5$, then time taken for SOC balancing among three phases would be 12.6 minutes theoretically.

ii) *Intra-phase SOC balancing*

If all the micro-packs in a phase leg have equal SOC (i.e., $\delta_{i1} = \delta_{i2} = \dots = \delta_{iN} = 0$), then power extracted during motoring operation and the power delivered during charging operation should be distributed equally among all the micro-packs in a phase leg. This section explains a novel method that can be integrated with the PWM generation algorithm to achieve SOC balanced operation among the micro-packs within a phase leg. In order to vary the amount of power distribution with respect to SOC of individual battery micro-pack, (11) is modified to,

$$V_{cell,ij}^* = \left[\frac{(V_i^* - V_{bat}^*)}{N} \right] (1 - G_2 \delta_{ij}) \quad (15)$$

The parameter δ_{ij} modifies the $V_{cell,ij}^*$ in every switching period to vary the amount of power distributed among the H-bridge units cascaded in series. The parameter δ_{ij} is determined from the deviation of the j^{th} battery micro-pack's SOC (SoC_{ij}) from the average SOC of all battery micro-packs in i^{th} phase leg. The value of G_2 is obtained in similar way as G_1 in the inter-phase balancing, based on the percentage of power that needs to be varied to nullify the SOC differences among the micro-packs in a phase leg. The control block diagram for intra-phase SOC balancing is shown in Fig. 3(b). From the closed loop transfer function, the proportionality gain G_2 is given by,

$$G_2 = \frac{Q}{100TP_{ij}} \quad (16)$$

For $Q = 19008 \text{ J}$; $P_{ij} = 125 \text{ W}$; if $G_2 = 0.4$, then SOC balancing among the micro-packs in a phase leg would take 6.3 minutes theoretically.

As the parameter δ_{ij} depends on the deviation of SoC_{ij} from SoC_i , δ_{ij} can be positive or negative i.e., δ_{ij} is positive when SoC_{ij} is smaller than SoC_i and δ_{ij} is negative when SoC_{ij} is greater than SoC_i . The minimum value that δ_{ij} can have is -1. But when $\delta_{ij} = -1$, then it is similar to faulty micro-pack and that corresponding H-bridge cell is clamped to zero voltage. This might cause voltage unbalance issues in 3-phase CHB converter, which requires other control techniques and is explained in the following section. The maximum value of δ_{ij} depends on the modulation index and is determined based on the other outer control loop. The upper range of δ_{ij} is determined so that the corresponding H-bridge cell output voltage $V_{cell,ij} \leq V_{dc,ij}$. Hence the range of δ_{ij} can be defined as in (17).

$$-1 \leq G_2 \delta_{ij} \leq \frac{N \times V_{dc,ij} - V_i^*}{V_i^*} \quad (17)$$

To prevent the inverter entering into square wave modulating region, the upper cut-off of the parameter δ should be set to 0.278 so that the maximum modulation index becomes $4/\pi$.

iii) *Ride through operation under faulty condition*

The motivation for investigating modular converters with micro-packs is to achieve the ride through capability under fault conditions, which is not feasible with the conventional single battery pack and the two-level inverter system. Various fault tolerant operation methods was proposed in literature for multilevel and modular converters [18]-[20]. The effective method of operation would be to distribute the load equally among the healthy micro-packs. The authors' motivation in this study is neither on type or place of the fault occurrence nor on the fault detection methods. Instead, a fault tolerant operation realization using MD-PWM is studied in detail. Furthermore, it is assumed that bypassing an H-bridge could be possible using the zero switching state ($S = 0$). The following method is derived assuming that the fault signals are available from any of the real time state of health monitoring systems like the ones proposed in [7] [8]. In-order to achieve ride through capability under faulty condition, the reference voltage for each H-bridge cell given in (15) is modified into

$$V_{cell,ij}^* = \left[\frac{\varepsilon_{ij}(V_i^* - V_{bal}^*)}{\varepsilon_{i1} + \dots + \varepsilon_{ij} + \dots + \varepsilon_{iN}} \right] (1 - G_2 \delta_{ij}) \quad (18)$$

where ε_{ij} is the fault signal for the j^{th} micro-pack in i^{th} phase and is given by 1 for being healthy and 0 for being faulty. This distributes the load among the other healthy units in the same phase in order to generate balanced three-phase output without neutral shift. This method is not efficient, and does not perform well in higher modulation indexes. However with neutral shift, the load can be shared with the healthy units in other phase legs of the CHB. It is well known that the addition of a zero sequence voltage to all three-phase voltage references modifies each phase voltage output without affecting the line-line voltage. For integration with the MD-PWM, the required voltage modifier that represents the required zero sequence voltage for the neutral shift is obtained from the fault signals and the V_i^* . Thus with the proposed method, the fault tolerant control along with the SOC balancing control is conveniently integrated with the PWM generation algorithm.

To achieve ride through capability with efficient load distribution, (18) is modified into,

$$V_{cell,ij}^* = \left[\frac{\varepsilon_{ij}(V_i^* - V_{bal}^* - V_f^*)}{\varepsilon_{i1} + \dots + \varepsilon_{ij} + \dots + \varepsilon_{iN}} \right] (1 - G_2 \delta_{ij}) \quad (19)$$

With the voltage modifier for ride through capability under faulty condition given by,

$$V_f^* = \frac{N \cdot \max(\beta_A, \beta_B, \beta_C)}{3\beta - \max(\beta_A, \beta_B, \beta_C)} [f_A V_A^* + f_B V_B^* (1 - f_A) + f_C V_C^* (1 - f_A)(1 - f_B)] \quad (20)$$

where

$$f_i = \begin{cases} \text{floor} \left[\frac{(\Delta f_i + |\Delta f_i|)}{2 * \Delta f_{max}} \right] & ; \forall i \in (A, B, C) \text{ and } \Delta f_{max} > 0 \\ 0 & ; \forall i \in (A, B, C) \text{ and } \Delta f_{max} = 0 \end{cases}$$

$$\Delta f_{max} = \max(\Delta f_A, \Delta f_B, \Delta f_C)$$

$$\beta_i = \frac{1}{N} \sum_{j=1}^N \varepsilon_{ij}$$

$$\beta = \frac{1}{3} (\beta_A + \beta_B + \beta_C)$$

$$\Delta f_i = \beta - \beta_i$$

The V_f^* follows the voltage reference of the phase leg where the fault occurs and with most number of faulty H-bridge units. Magnitude of the V_f^* is determined based on the number of faulty and healthy H-bridge units. The V_f^* is added to the voltage references of all the three phase legs, which distributes the load demand from the phase leg having more number of faults to the other phase legs. For example, with $N = 2$ and fault occurs in B1 ($\varepsilon_{B1} = 0$), the magnitude of V_f^* is given by $0.67V_B^*$.

5 EXPERIMENTAL INVESTIGATIONS

A laboratory setup has been built to demonstrate the operation of CHB converter with battery micro-packs for the efficacy of the proposed SOC balancing control and fault tolerant control using MD-PWM. The photo of the setup is shown in Fig.4. The setup consists of a three-phase five-level CHB with two H-bridge units per phase made of IGBTs, each supplied with a battery micro-pack. Every battery micro-pack has 16 lithium-ion-phosphate cells of 3.3-V 60-Ah connected in series. A three-phase 1-HP induction motor has been employed as load. The proposed control strategy and the gate signal generation algorithm using the MD-PWM has been implemented in dSPACE DS1104 control board. In this demonstration, the coulomb counting method has been implemented in dSPACE controller for the real-time SOC estimation and is given by,

$$SoC_{ij}(t) = SoC_{ini,ij} - \frac{1}{Q_{bat}} \int V_{bat,ij} i_{bat,ij}(t) dt \quad (21)$$

Q_{bat} is the capacity of the battery in Wh, V_{bat} and i_{bat} are the batter micro-pack voltage and current respectively. The battery current is derived from the line current of the motor, and the switching state ($S_{ij} \in [1, 0, -1]$) of the corresponding H-bridge using,

$$i_{bat,ij}(t) = S_{ij}i_i(t) \quad (22)$$

where $i_i(t)$ is i_A , i_B and i_C . The i_A and i_B are measured and i_C is derived using $i_C = -i_A - i_B$ based on the assumption of balanced load condition. In order to execute the coulomb counting method, the initial SOC ($SoC_{ini,ij}$) of each battery micro-pack is required. And it was entered into the dSPACE controller offline. The parameters of the laboratory setup are listed in Table 2. The lithium cells used for this experiment are of 60 Ah capacities. But to demonstrate the SOC balancing operation in a reasonable time with 1-HP motor load, the capacity of lithium cell is considered as 6 Ah in the SOC calculation. Open loop constant V/Hz control has been implemented for the speed control of the induction motor.

Table 2 Experimental Setup Parameters

Parameter	Value
Cascade Number N	2
Battery micro-pack rating	52.8-V, 60-Ah
Load – Induction Motor	1-HP
Switching period T_{sw}	1 ms
Inter-phase SOC balancing constant G_1	0.4
Intra-phase SOC balancing constant G_2	0.5

Fig. 4 Experimental setup

Under normal operating condition, all the H-bridge units with battery micro-packs would be healthy and fully charged or charged to an identical SOC level. In such cases, equal power has to be maintained across all the H-bridge units. The traces of reference variables and the system parameters under normal operating condition with a step change in the speed reference are shown in Fig. 5. Fig. 5(a) shows the speed reference and the corresponding voltage reference generated by the constant V/Hz control. 5(b) shows the reference signals generated by the proposed control methods. Since all battery modules have equal initial SOC and no fault condition, the V_f^* and V_{bal}^* are zero. Therefore, all the H-bridge units have equal voltage references ($V_{cell,ij}^*$) as shown in Fig. 5(b). The voltages generated by the three-phase five-level inverter, the motor line current, and the

input power from the six battery micro-packs are presented in Fig. 5(c). It can be seen that the power delivered by each micro-pack is identical.

To emulate the fault condition, the unit B1 in phase-B leg is assumed to be faulty and the corresponding fault signal was set to 0. The traces of reference variables and the system parameters under fault condition (without SOC balancing control) with a step change in the speed reference are shown in Fig. 6. Fig. 6(a) shows the speed reference and the corresponding voltage reference generated by the constant V/Hz control. 6(b) shows the reference signals generated by the proposed control methods. V_f^* is the voltage modifier that needs to be added to all the phase voltage references for this fault condition. Since fault has occurred in phase-B, the V_f^* follows V_b^* as explained in Section 4 (iii), and the reference voltage the faulty unit, $V_{cell,B1}^*$ is zero. The other H-bridge units' voltage references ($V_{cell,ij}^*$) are also shown in Fig. 6(b). The voltages generated by the three-phase five-level inverter, the motor line current, and the input power from the six battery micro-packs are presented in Fig. 6(c). It can be seen from the voltage wave forms that the B-phase voltage has only three levels as only one H-bridge is in operation. The balanced motor line current verifies the proposed control scheme for the fault condition. The power extracted from the micro-pack B2 is higher than the other battery micro-packs, which eventually results in an unbalanced SOC condition.

To emulate the condition of unequal SOC, each battery micro-pack was charged to different SOC levels ($SoC_{A1}=21.5\%$, $SoC_{A2}=23\%$, $SoC_{B1}=22\%$, $SoC_{B2}=23.5\%$, $SoC_{C1}=20\%$, and $SoC_{C2}=21\%$). The traces of reference variables and the system parameters under unbalanced SOC condition (with SOC balancing control) with a step change in the speed reference are shown in Fig. 7. Fig. 7(a) shows the speed reference and the corresponding voltage reference generated by the constant V/Hz control. Fig. 7(b) shows the reference signals generated by the proposed SOC balancing control method. Since all battery modules are healthy, the V_f^* is zero. There exists an imbalance between the average SOC of three phases. The inter-phase SOC balancing control makes phase-B to deliver more power than phase-A and phase-C. The V_{bal}^* generated for this unbalanced condition is shown. The intra-phase SOC balancing control considers the individual micro-pack SOC in that particular phase. Corresponding H-bridge voltage references ($V_{cell,ij}^*$) are presented. The voltages generated by the three-phase five-level inverter, the motor line current, and the input power from the six battery micro-packs are presented in Fig. 7(c). It can be seen that the power extracted from the micro-packs are different and is according to their SOC difference from the average SOC of the system. For instance, SoC_{B2} is higher compared to other SOC and hence the power extracted from B2 is higher compared to other micro-packs.

(a)

(b)

(c)

Fig. 5 System operation under normal operating condition
(a) Speed reference and voltage reference from motor control unit
(b) Voltage references generated by the proposed control schemes
(c) Voltages generated by the converter, line currents of the motor, input power from the battery micro-packs

Fig. 6 System operation under fault condition without SOC balancing control
(a) Speed reference and voltage reference from motor control unit
(b) Voltage references generated by the proposed control schemes
(c) Voltages generated by the converter, line currents of the motor, input power from the battery micro-packs

Fig. 7 System operation under unbalanced SOC condition with the SOC balancing control
(a) Speed reference and voltage reference from motor control unit
(b) Voltage references generated by the proposed control schemes
(c) Voltages generated by the converter, line currents of the motor, input power from the battery micro-packs

SOC traces of the battery micro-packs under different operating conditions without any SOC balancing control and with the proposed SOC balancing control are portrayed in Figs. 8(a) and 8(b) respectively. The left plot in Fig. 8(a) is for balanced SOC condition. It can be observed that all the battery micro-packs exhibits equal discharge rate under balanced SOC condition. The middle plot in Fig. 8(a) shows the SOC traces under unbalanced SOC condition with initial SOC's given by $SoC_{A1}=21.5\%$, $SoC_{A2}=23\%$, $SoC_{B1}=22\%$, $SoC_{B2}=23.5\%$, $SoC_{C1}=20\%$, and $SoC_{C2}=21\%$. Without SOC balancing control, the MD-PWM particularized as PS-PWM operates in a way to extract equal amount of power from the battery micro-packs. This would make the micro-pack having lower SOC to reach the minimum cut-off value (15%) quicker, and the system should be stopped at $t = 850$ s from further operation, even though some of the battery micro-packs have the SOC higher than the cut-off value. With the unequal initial SOC conditions, the CHB is operated with the proposed SOC balancing control. The corresponding SOC traces are given in the left plot of Fig. 8(b). There exists an imbalance between the average SOC's of three phases. The inter-phase SOC balancing control makes phase-B to deliver more power than phases A and C. The intra-phase SOC balancing control considers the individual micro-pack SOC in that particular phase. Consequently, the SOC's of micro-packs are balanced in about 22 minutes. With the SOC balancing control, the micro-pack having lower SOC reaches the minimum cut-off value (15%) at $t = 1400$ s. Hence the proposed SOC balancing control prolongs system operation by about 9.1 minutes. Such an operational improvement is very crucial for an electric vehicle, as it has been found that usually personal transportation electric cars have a driving range of about 4.5 hours with average speed in city traffic condition [4].

Without SOC balancing control, the fault tolerant control makes the system to operate in such a way that the power extracted from the phases having healthy micro-packs delivers comparatively more power. It results in the SOC imbalance among the healthy battery micro-packs and is evident from the SOC traces given in the right plot of Fig. 8(a). However, with the SOC balancing control integrated to the fault tolerant control, this imbalance is resolved as shown in the right plot of Fig. 8(b). With the SOC balancing control in loop, unequal amount of power is extracted from each of the healthy micro-packs to maintain the SOC of each micro-pack close to their average SOC. Without SOC balancing control, the SOC of B2 micro-pack reaches 57.5 % at about $t = 510$ s. With the SOC balancing control, the SOC of B2 micro-pack reaches 57.5 % at about $t = 620$ s. This verifies that the proposed SOC balancing schemes aids in prolonging the system operation time.

Fig. 8 SOC traces of battery micro-packs under different operating conditions
(a) without SOC balancing control (left: balanced SOC condition, middle: unbalanced SOC condition, right: fault condition)
(b) with the proposed SOC balancing control (left: unbalanced SOC condition, right: fault condition)

6 CONCLUSION

Modular battery pack system or micro-pack concept has been introduced to increase the availability of an EV in the event of fault. Multi-dimensional modulation (MD-PWM), a generalized modulation technique for the CHB converter has been reviewed. A control strategy for the SOC balancing between the battery micro-packs and realization of fault ride through operation using MD-PWM has been explained. The advantage of the proposed methods is that it can be conveniently integrated with the MD-PWM algorithm. The results obtained from the laboratory setup of a five-level three-phase CHB driving an induction motor with six battery modules of 52.8-V 60-Ah have been presented. The results have verified that the fault tolerant and SOC balancing operation can be achieved with CHB using MD-PWM. This shows that the proposed micro-pack system with CHB would improve the EV performance in the event of fault, which is not possible with the conventional single battery pack and two-level converter designs.

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