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A Low Overhead Quasi-Delay-Insensitive (QDI) Asynchronous Data Path Synthesis Based on Microcell-Interleaving Genetic Algorithm (MIGA)

Rong Zhou, Kwen-Siong Chong, Bah-Hwee Gwee and Joseph S. Chang

Abstract—In this paper, we propose a design approach to mitigate the hardware overhead of the Data Completion Detection circuit (DCD) in Quasi-Delay-Insensitive (QDI) asynchronous-logic circuits. In this proposed design approach, three novelties are highlighted. Firstly, a novel microcell-interleaving approach is proposed to reduce the number of completion detection (CD) circuits whilst retaining the required QDI attribute. Secondly, we analyze the performance of the QDI circuits based on the proposed microcell-interleaving approach graphically in terms of power dissipation, transistor-count and delay; and evaluate/determine the upper and lower boundaries of these performance profiles. Thirdly, we propose a Microcell-Interleaving Genetic Algorithm (MIGA) to stochastically optimize the proposed microcell-interleaving approach on power dissipation, transistor-count, and delay. To validate the proposed design approach, a complete performance profile of ISCAS-85 C499 circuit is investigated on the basis of Differential Cascode Voltage Switch Logic (DCVSL) and Dynamic Strong Indicating (DSI) microcells. We demonstrate the efficiency of the proposed design approach by benchmarking against the competing DCVSL, Null Convention Logic (NCL) and DSI designs on five ISCAS-85 circuits. Specifically, the proposed designs, on average, are $1.77\times$ better in power dissipation, $1.4\times$ better in area, and $1.58\times$ better in a composite metric of $\text{power}\times\text{area}\times\text{delay}$, and reasonably slower for the lowest power dissipation points. We further demonstrate the practicality of the proposed design approach by implementing an 8-tap 16-bit asynchronous QDI Finite Impulse Response (FIR) filter. Finally, we demonstrate the $\sim 10\%$ and $\sim 11\%$ improved efficiency of the proposed MIGA over the Greedy Algorithm and Dynamic Programming respectively.

Index Terms—Asynchronous-logic, DCVSL, NCL, quasi-delay-insensitive (QDI), input-complete, optimization, genetic algorithm

I. INTRODUCTION

Rapid advancement of networking technologies enables numerous emerging applications, including wireless-sensor-networks [1], [2], Internet-of-Things [3], [4], multi-processors [5], etc. For these applications, analog/digital sensing, communication and processing capabilities are integrated collectively, preferably in Systems-on-Chip or Systems-in-Package using advanced nano-scaled fabrication processes. As the minimum-feature size of fabrication processes continues to scale downwards, process-voltage-temperature (PVT) variations therein become increasingly larger. Consequently, designing digital circuits based on the ubiquitous synchronous (sync) approach, whose

synchronization is based on a global clock or its variant, becomes increasingly challenging. The usual methods to accommodate the PVT variations include adopting a conservative clock rate (when the conditions are more benign), timing-tolerant techniques, strict operating conditions, etc. Nevertheless, it can be argued, perhaps somewhat contentiously, that unconditional error-free operation for sync circuits may be compromised because a complete profile of the PVT variations in advanced fabrication processes is intractable.

An alternative design approach for robust operation is the somewhat esoteric asynchronous (async) approach [6]–[15]. There are three practical (and implementable) classes of async circuits: Bundled-Data (BD), Speed-Independent (SI) and Quasi-Delay-Insensitive (QDI) [10]. BD circuits are, to some extent, similar to sync circuits in the sense that their operation relies on a bounded delay assumption for gates and wires. As the bounded delay assumption may be unmatched/insufficient due to the PVT variations, the ensuing circuits are only conditionally robust. SI circuits can tolerate arbitrary microcell delays but assume that all wire delays are negligible, a somewhat unrealistic assumption in advanced nano-scaled fabrication processes and in increasingly complex systems. QDI circuits can tolerate arbitrary gate, wire delays and obey isochronic fork [18] (strong intra-operator fork and inter-operator fork timing assumptions [16]), a condition that can be satisfied in practice. Of these classes of async circuits, it is generally accepted within the async community that the QDI approach probably offers the most practical option [9], [17]–[19] to accommodate PVT variations. This is because it innately detects the computation delays according to different workloads and operating conditions. Nevertheless, the primary drawback of QDI is the increased hardware overhead, for example, due to its dual-rail modality, a near doubling of the hardware compared to single-rail designs. In light of this drawback, there is a substantial on-going research effort to design QDI circuits with reduced hardware overhead. Reported techniques include synthesis based on partial acknowledge [20], adopting a dynamic logic implementation (instead of a static logic implementation to reduce the number of transistors [10]), completion detection (CD) circuits with a high fan-in structure [21], 1-of-4-rail logic (but with more complex circuitry) [10], local input completeness relaxation [22], coping combinational logic delay [23], optimization by relative-timing analysis [24], optimal technology mapping and cell merger [25] etc.

The design styles of QDI pipelines can be generally categorized into integrated pipeline and data-control

decomposition paradigms. The former paradigm (such as pre-charged half-buffer [18]) is a fine-grain pipeline where QDI circuits are optimized at the transistor-level by collectively integrating a functional logic and a controller (including a CD circuit and a latch). This paradigm yields high speed designs but at the cost of high synthesis effort and high IC area overhead. Conversely, the latter paradigm (such as NULL Convention Logic (NCL) [21], Delay-Insensitive Miniterm Synthesis (DIMS) [10], Pre-charge-Static Logic [1], etc.) is a coarse-grain pipeline that considers the functional logic and the controller independently. This paradigm, conceptually similar to a sync pipeline, features design simplicity (in part by leveraging on commercial tools and occupying a smaller IC area) but at the cost of reduced speed largely due to its coarse-grain structure. In this paper, the latter paradigm is of interest, largely due to the smaller IC area and lower power dissipation.

Of the various data-control decomposition QDI methodologies, the NCL_X design methodology [19] reportedly has an efficient design flow, and yields designs with relatively low area overhead (compared to the NCL_D design methodology [26]). Its design flow involves first synthesizing a standard single-rail netlist and thereafter a transformation to an NCL (dual-rail) netlist [19]. To preserve the QDI property, a Data Completion Detection (DCD) circuit embodying local CD circuits is required to detect the outputs of microcells therein. The DCD circuit not only fully acknowledges the output validity/nullity but also avoids gate orphans [21]. From a broad perspective, the DCD circuit has large power dissipation and IC area overheads, and if mitigated, the efficacy of the data-control decomposition QDI realizations would improve, particularly the hardware overhead.

In this paper, we propose a design approach to reduce the aforesaid overhead by means of a novel microcell-interleaving approach and a Microcell-Interleaving Genetic Algorithm (MIGA). Here we define a “microcell” as a dual-rail gate, capable of executing basic operations such as AND/NAND, OR/NOR, etc. Our proposed design approach complements the NCL_X design methodology, and there are several novelties and contributions in this paper. First, our proposed design approach essentially involves interleaving input-complete [21] microcells with non-input-complete microcells to enable hardware to be shared without compromising the QDI property; see later for the definitions of the input-complete and

non-input-complete microcells. This microcell-interleaving approach is beneficial to reduce the number of CD circuits, thereby reducing the overall hardware overhead. Second, unlike the NCL_X design methodology that is targeting for NCL microcells, our proposed design approach is applicable to many implementations of microcells, including non-input-complete microcells (NCL, Differential Cascode Voltage Switch Logic (DCVSL) [10], etc.), (fully and partially) input-complete microcells (DIMS, Dynamic Strong Indicating (DSI) [10], etc.) [20]. This attribute would widen the scope of circuit implementation and its ensuing optimization. Third, we comprehensively analyze the performance limit (upper/lower bounds) of QDI circuits in terms of power dissipation, transistor-count and delay, and derive the optimal point based on the given metrics. Finally, the proposed MIGA, leveraging on the well-established genetic algorithm and its associated fitness functions, enables a fast optimization process to achieve the possible optimal metrics, hence a practical approach to the actual circuit realization.

Based on the DCVSL and DSI microcells as examples, we validate our proposed design approach, including with a full exploration of the performance limit/profile of a QDI circuit. Based on several well-accepted ISCAS-85 benchmark circuits, we also show that our proposed design approach is highly competitive when benchmarked against the competing DCVSL, NCL and DSI (1.77×, 1.4×, 1.58× better in power dissipation, area, a composite metric of power×area×delay respectively, and with a reasonable delay increase). We further demonstrate the practicality of our proposed design approach by means of the implementation of an 8-tap 16-bit async QDI Finite Impulse Response (FIR) filter design. Finally, we show the efficiency of the proposed MIGA by comparing with the Greedy Algorithm and Dynamic Programming.

This paper is organized as follows. Section II describes the proposed microcell-interleaving approach and Section III analyzes its performance profile/limit. Section IV presents the proposed MIGA. Section V presents experimental results of our proposed design approach (including a comparison against the competing methodologies) and finally, conclusions are drawn in Section VI.

II. THE PROPOSED MICROCELL-INTERLEAVING APPROACH

This section first briefly reviews QDI circuits and their

Fig. 1(a) The block diagram of an data-control decomposition pipeline stage i , (b) CD circuits (with OR and C-Muller gates)

properties, followed by a succinct delineation of the proposed microcell-interleaving approach for the QDI circuit realization.

A. Review: QDI Circuits and QDI Properties

As mentioned earlier, QDI circuits should operate perfectly with any gate/microcell/wire delays except for the isochronic forks. This assumption of the isochronic forks leads to practical realizations of digital QDI circuits where all the gates and wires therein are detectable/acknowledgeable [18].

Fig. 1(a) depicts the async data-control decomposition (i^{th} stage) comprising a QDI Handshake Control_{*i*} (consisting of a Register_{*i*}, a Register Completion Detection (RCD_{*i*}) and a C-Muller microcell) and a QDI Data Circuit_{*i*} (consisting of microcells and a DCD_{*i*}); a QDI Handshake Control_{*i+1*} is also presented for ease of illustration. The QDI Handshake Control_{*i*} controls the QDI Data Circuit_{*i*} according to a sequence of pre-defined handshake signals, and the data operation is based on the dual-rail encoding [10] that enables completion detection. When *Input_i* are either all valid or all empty, the RCD_{*i*} will check the input and acknowledge the Handshake Control_{*i-1*} (not shown) of the preceding pipeline. *Ack_i* also acknowledges the input completeness of the Pipeline_{*i*}, where *Input_i* is valid when *Ack_i* = 1 or otherwise empty when *Ack_i* = 0. *Input_i*, via Register_{*i*}, will trigger the QDI Data Circuit_{*i*} for either evaluation or reset. Once the output (*Input_{i+1}*) is stored in the Register_{*i+1*}, the RCD_{*i+1*} will acknowledge Handshake Control_{*i*}. The DCD_{*i*} is to acknowledge the intermediate signals. For completeness, Fig. 1(b) depicts the CD circuit in the DCD_{*i*} and RCD_{*i*}.

Conceptually, the pipeline depicted in Fig. 1(a) is essentially the same as the NCL-X design methodology [21]. The pipeline

will preserve its quasi-delay-insensitivity if the design issue of ‘observability’ is satisfied. The ‘observability’ will avoid ‘gate orphan’ and ‘wire orphan’. The gate/wire orphan refers to that an internal gate/wire is enabled to switch its output but the switching is masked from observable outputs of the entire circuit. The gate-orphan issues can be addressed by the evaluation and reset phase of dual-rail coding; the wire orphan issue can be addressed either by input-complete microcells (where the output will acknowledge the validity/nullity of all the inputs) or by incorporating CD circuits to non-input complete microcells using the assumption of isochronic forks. In Fig. 1(a), the RCD_{*i*}, DCD_{*i*} and the QDI microcells (both input-complete and non-input-complete microcells) collectively address the gate and wire orphan issues.

The efficacy of QDI pipelines strongly depends on the types of the microcells adopted. In general, non-input-complete microcells are widely adopted (over input-complete microcells) in QDI pipelines due to their higher speed, lower power dissipation and smaller IC area. Here we define microcells where their outputs can be all valid/null before all inputs are all valid/null as non-input-complete microcells, whereas the otherwise are input-complete microcells. Despite this, the area and energy overhead of DCD_{*i*} are somewhat large and cannot be ignored especially if the complexity of the functional circuits in QDI Data Circuit_{*i*} is high. In Table I, we characterize and tabulate the power dissipation, transistor-count and delay of 6 basic non-input-complete and input-complete microcells; the former is based on DCVSL and the latter is based on DSI (with transistor-level optimization) [10]. For illustration purpose, the schematics of dual-rail OR/NOR microcells embodying

Fig. 2 (a) The circuit schematic of a DCVSL dual-rail OR/NOR microcell and estimated overhead for CD circuit
(b) the circuit schematic of a DSI dual-rail OR/NOR microcell

Table I
The power, transistor-count and delay characteristics of several dual-rail microcells based on DCVSL and DSI @ 1.2V, 130nm CMOS

	Power, μW @ 100MHz		Transistor-count		Delay, ns	
	DCVSL*	DSI	DCVSL*	DSI	DCVSL*	DSI
2-input OR/NOR	2.2	1.5	23	21	0.14	0.32
2-input AND/NAND	2.2	1.5	23	21	0.15	0.32
2-input XOR/XNOR	2.3	1.6	27	24	0.17	0.33
3-input OA/OAI	2.3	2.9	25	34	0.15	0.93
3-input AO/AOI	2.3	2.9	25	34	0.15	0.94
3-input Carry/ICarry	2.3	2.9	27	38	0.16	0.87
Average	2.3	2.2	25	29	0.15	0.62

* include a local CD circuit

DCVSL and DSI are depicted in Fig. 2(a) and Fig. 2(b) respectively. The readings (in Table I) in DCVSL microcells include a local CD circuit to maintain the QDI attribute. Particularly, the local CD circuit is a 2-input OR microcell and a quarter of a 4-input C-Muller microcell (which is shared by 4 DCVSL microcells to mitigate the power/area overhead). When the DCVSL microcells, embodying a local CD circuit, are compared against the DSI microcells, on average, the latter appear highly uncompetitive in speed (by $\sim 3.1\times$ worse) but comparable in terms of power dissipation (by $\sim 0.04\times$ better) and transistor-count (by $\sim 0.16\times$ worse). Nonetheless, these comparisons allude to possible overhead optimization and we will in turn describe such optimization based on our proposed interleaved microcell approach. Please note that DCVSL and DSI microcells tabulated in table I are necessary for efficacious applications of the proposed approach and algorithm (see later).

B. Delineation of the Proposed Microcell-Interleaving Approach

The fundamental advantage of the proposed microcell-interleaving approach is to reduce the number of local CD circuits and yet maintain the QDI attribute. Fig. 3 depicts a pipeline structure where a DCVSL microcell is interleaved with a DSI microcell; the DSI microcell not only computes its logic operation but also detects the output validity/nullity of its interleaved DCVSL microcell. In this interleaving structure, only a local CD circuit is required to integrate into the DSI microcell (but not to the DCVSL microcell), thereby reducing the overall hardware overhead in the RCD_i and DCD_i . Therefore, the amount of power dissipation and area reduction is largely in line with the number of reduced local CD circuits. For example, the power dissipation overhead due to the local CD circuit (for each DCVSL microcell) is $1.1\mu\text{W}$ @ 100MHz. By using a 3-input OA/OAI DSI microcell (connected to three DCVSL microcells), three local CD circuits can be reduced, namely, $3.3\mu\text{W}$ ($3 \times 1.1\mu\text{W}$) of power dissipation is reduced. Although the DSI microcell dissipates $1.7\mu\text{W}$ ($2.9\mu\text{W} - (2.3\mu\text{W} - 1.1\mu\text{W})$) of power dissipation more than corresponding DCVSL microcell, the overall power dissipation saving is still significantly large at $1.6\mu\text{W}$ ($3.3\mu\text{W} - 1.7\mu\text{W}$). Similarly, the

transistor-count can be minimized by reducing the local CD circuits. With respect to the speed of the optimized circuits, microcell-interleaving circuits are usually featured lower speed attribute when compared to the fully non-input-complete circuits, this is mainly due to the already slow speed attribute of input-complete microcells.

To appreciate our proposed microcell-interleaving approach and the effects of the different interleaving strategies, we consider a circuit depicted in Fig. 4(a)-(d). This circuit has three paths: $Path_1$, $Path_2$ and $Path_3$ where $Path_1$ consists of microcell 1 to 9, $Path_2$ consists of microcell 10 to 15, and $Path_3$ consists of microcell 16 to 20. The rectangle shape comprises only microcells (DCVSL or DSI), while oval shape comprises microcells (DCVSL or DSI) together with a local CD circuit. We assume all the microcells are 2-input microcells. For simplicity, not all the inputs or wires are shown. We assume the objective here is to achieve the lowest power dissipation by using our proposed approach.

In order to minimize the power dissipation (largely due to fewer CD circuits), we intuitively arrange the microcell-interleaving optimization in four stages in Fig. 4(a), Fig. 4(b), Fig. 4(c) and Fig. 4(d) respectively. Fig. 4(a) is the initial circuit where the default microcells are the DCVSL microcells. All the microcells in Fig. 4(a) are oval shape except the primary output microcells. This is because the DCVSL microcells are non-input-complete where local CD circuits are required to be integrated to detect the validity/nullity of internal wires, hence fulfilling by the QDI attribute. The primary output microcells do not require local CD circuits as their primary outputs are checked by the RCD of next register (see the pipeline structure in Fig. 1 (a)). Therefore, a total of 17 CD circuits are required for the circuit in Fig. 4(a). We now apply microcell-interleaving approach to the circuits in Fig. 4(a) with DSI microcells, and integrate appropriate CD circuits to obtain a new circuit configuration as depicted in Fig. 4(b). In this example, the DCVSL microcells $DCVSL_1$, $DCVSL_3$, $DCVSL_5$, $DCVSL_7$, $DCVSL_{10}$, $DCVSL_{12}$, $DCVSL_{14}$, $DCVSL_{16}$, $DCVSL_{18}$ do not require any local CD circuit. While all the output wires of DSI microcells are connected to DCVSL microcells, local CD circuits are integrated into DSI microcells to preserve the

Fig. 3 The proposed async pipeline by adopting microcell-interleaving approach with DCVSL and DSI microcells

QDI attribute. In this case, there are only 8 CD circuits, a reduction of 9 CD circuits as compared to the initial configuration in Fig. 4(a).

For further power dissipation reduction, we eliminate all the CD circuits to achieve a new updated configuration as depicted in Fig. 4(c). In this updated configuration, all the

validity/nullity of the internal wires are checked by the DSI microcells and no CD circuits are required.

Note that even without the CD circuits, the combination of DCVSL and DSI microcells may not be the lowest power dissipation due to redundant wire checking. In Fig. 4(c), we observe that the output wire of $DCVSL_{10}$ is checked twice by the

Fig. 4 Microcell interconnection: (a) initial interconnection, (b) interleaving interconnections, (c) interleaving connection of zero CD circuits, and (d) interleaving connection without redundant wire checking

DSI_{11} and DSI_{18} . In the case, we can easily remove the redundant checking by replacing DSI_{11} with $DCVSL_{11}$, or by replacing DSI_{18} with $DCVSL_{18}$. However, for the latter replacement, the output wire of DSI_{17} is not internally checked, and a CD circuit should be integrated into DSI_{17} ; hence replacing DSI_{11} with $DCVSL_{11}$ is a better choice. The same case can be applied to the output wire of $DCVSL_{16}$, DSI_4 , and DSI_5 ; and DSI_{17} , DSI_5 , DSI_6 can be replaced with $DCVSL_{17}$, $DCVSL_5$, $DCVSL_6$ respectively. The final optimized configuration is depicted in Fig. 4(d), which probably has the lowest power dissipation among different DCVSL and DSI combinations.

This example demonstrates the optimization process of the proposed microcell-interleaving approach. With the increase in complexity of the circuits (number of microcells), the number of combinations between non-input-complete microcells (such as DCVSL, NCL, etc.) and input-complete microcells (such as DSI) will increase exponentially. In this case, it is impossible to manually arrange the locations of different microcells to achieve the lowest power dissipation combination. Hence, we propose an optimization algorithm by employing the genetic algorithm to stochastically search for a combination which yield the best result; the details of the implementation will be explained later, and before that a formal evaluation for the microcell-interleaving approach will be investigated.

III. PERFORMANCE PROFILE ANALYSIS FOR THE PROPOSED MICROCELL-INTERLEAVING APPROACH

In this section, we investigate the complete performance profiles in terms of power dissipation, IC area (largely based on the number of transistors) and delay of QDI circuits. Other attributes, such as the dependency of power and delay profiles, can be explored by the proposed MIGA. In order to study the trend of profiles, we assume the size of circuits (number of microcells) is so large that the impact of a single microcell on the trend is negligible.

A. Power Dissipation

For a QDI circuit, we classify the power analysis on the basis of two categories: individual-microcell analysis and group-microcell analysis.

A1. Individual-microcell Analysis

We first consider the individual-microcell analysis by using the i^{th} non-input-complete microcell $G_{NIC,i}$ and its corresponding input-complete microcell $G_{IC,i}$. The number of primary inputs (a dual-rail input is considered as one primary input) of the microcell is defined as I_i . The power dissipation of $G_{NIC,i}$ and $G_{IC,i}$ are denoted as $P_{NIC,i}$ and $P_{IC,i}$ respectively, and their power difference is ΔP_i . We further assume the power dissipation of one CD circuit for detecting/acknowledging a primary input (of $G_{NIC,i}$) is P_{CD} . Now, we can find an input threshold n_i of the microcell in (1).

$$n_i = \frac{P_{IC,i} - P_{NIC,i}}{P_{CD}} = \frac{\Delta P_i}{P_{CD}} \quad (1)$$

The input threshold integer n_i will be in one of the three domains in (2a) to (2c) in part depending on the number of the primary input I_i .

$$\begin{cases} n_i > I_i \end{cases} \quad (2a)$$

$$\begin{cases} 0 \leq n_i \leq I_i \end{cases} \quad (2b)$$

$$\begin{cases} n_i < 0 \end{cases} \quad (2c)$$

In the domain (2a), ΔP_i is always > 0 , as $G_{NIC,i}$, which integrates with CD circuits, will be more power-efficient than $G_{IC,i}$. Conversely, in the domain (2c), ΔP_i is always < 0 , implying that $G_{IC,i}$ is more power-efficient than $G_{NIC,i}$ (although this scenario is unlikely to be true due to the additional overhead for input-completeness in $G_{NIC,i}$). In the domain (2b), it is of interest to find an optimal combination of microcells as some of the CD circuits can be shared in the actual circuit realization (at the circuit-level), those yet unchecked primary inputs/wires, denoted as $N_{WUC,i}$, will then need to be acknowledged by other CD circuits. If $N_{WUC,i}$ is $<$ input threshold n_i in $G_{NIC,i}$, this scenario indicates that a replacement of their corresponding $G_{IC,i}$ would not be power-efficient. If $N_{WUC,i}$ is $>$ input threshold n_i in $G_{NIC,i}$, this scenario indicates that a replacement of its $G_{IC,i}$ would be power-efficient. In a complex circuit where many microcells are connected and some primary inputs could be shared, the replacement of the microcells and their associated CD circuits will affect the number of yet undetectable primary inputs of other microcells. In other words, it would be possible that a replacement of the i^{th} microcell with $N_{WUC,i} > n_i$ could cause $N_{WUC,k} < n_k$ in k^{th} microcell in a complex circuit.

The analysis of completion detection circuits of individual microcell is performed at the inputs, because it is easier to appreciate the optimization space in this fashion. Nevertheless, from an overall circuit perspective, we perform the analysis on output.

A2. Group-microcell Analysis

We now consider the group-microcell analysis of the overall power dissipation where microcells located in the domain (2b) will be of the main interest. We first pictorially depict in Fig. 5 the power dissipation profile of a QDI circuit embodying many microcells. The abscissa represents the percentage of the number of input-complete microcells over the total number of microcells (including input-complete and non-input-complete microcells), whereas the ordinate represents power dissipation. The shaded region indicates the possible microcell combinations satisfying the QDI attribute. The power $P_{0\%}$ is the power dissipated in the QDI circuit embodying fully non-input-complete microcells, and $P_{100\%}$ is the converse; $P_{0\%} > P_{100\%}$. The lower contour (line $P_{0\%}$ to $P_{j\%}$ to $P_{m\%}$ to $P_{100\%}$) indicates the lower power boundary for their respective percentage of using the input-complete microcells. The upper contour (line $P_{0\%}$ to $P_{100\%}$) indicates the upper power boundary for the same.

The abovementioned power profile is now explained in detail as follows. We first model the power dissipation of the QDI circuit as:

$$P_{j\%}(\alpha) \cong M_{CD,\alpha} \cdot P_{CD} + \sum_{l=1}^{M_{IC}} P_{IC,l}(\alpha) + \sum_{o=1}^{M_{NIC}} P_{NIC,o}(\alpha) \quad (3)$$

where α is the arbitrary point at the $j\%$ (within the lower and upper power dissipation boundaries); $M_{CD,\alpha}$ is the total number of CD circuits used at the point α ; M_{IC} is the total number of input-complete microcells at $j\%$; M_{NIC} is the total number of non-input-complete microcells at $j\%$;

$$j\% = \frac{M_{IC}}{M_{IC} + M_{NIC}} \times 100\% .$$

Within the same percentage of input-complete microcells, e.g. at $j\%$ in Fig. 5, it is possible to have many microcell combinations (with different α points), the minimum point is defined as $P_{j\%}$ as expressed in (4).

$$P_{j\%} = \min[P_{j\%}(0), P_{j\%}(1), P_{j\%}(2), \dots] \quad (4)$$

The minimum point $P_{j\%}$ can be achieved by exhaustively evaluating the different microcell combinations (at different α points). When $j = m$, $P_{m\%}$ is the lowest power point among all the combinations and is the point of interest in our analysis. Considering the lower power boundary, the power dissipation is initially reduced from $P_{0\%}$ to $P_{m\%}$, and the rate of power reduction satisfies:

$$\frac{P_{j\%} - P_{(j-\Delta)\%}}{\Delta\%} \leq \frac{P_{(j+\Delta)\%} - P_{j\%}}{\Delta\%} < 0 \quad \text{where } 0 < j < m \quad (5)$$

This situation is easy to appreciate as the replacement of non-input-complete microcells by the input-complete microcells reduces the number of the CD circuits, and the power reduction per input-complete microcell is more significant initially because each replacement could reduce as many CD circuits as possible. After $m\%$, the overall power dissipation will increase if we continue to replace the non-input-complete microcells with the input-complete microcells, and the rate of power increase can be expressed as follows:

$$\frac{P_{(j+\Delta)\%} - P_{j\%}}{\Delta\%} \geq \frac{P_{j\%} - P_{(j-\Delta)\%}}{\Delta\%} > 0 \quad \text{where } m < j < 100 \quad (6)$$

In this case, the lowest power point $P_{m\%}$ in Fig. 5 will satisfy the condition in (7) as follows:

$$\frac{P_{(m-\Delta)\%} - P_{(m)\%}}{-\Delta\%} < 0 < \frac{P_{(m+\Delta)\%} - P_{(m)\%}}{\Delta\%} \quad (7)$$

Fig. 5 Overall power dissipation profile of all microcell combinations satisfying QDI attribute

For the number of CD circuits, M_{CD} , at the lowest power dissipation point $P_{m\%}$, we derive the following theorem.

Theorem 1: The number of CD circuits M_{CD} of the lowest power dissipation point $P_{m\%}$ satisfies:

$$M_{CD} \leq \sum_{i=1}^{M_{NIC}} \min(I_i, \max(\lfloor n_i \rfloor, 0)) \quad (8)$$

Proof: If $P_{m\%}$ is the lowest power dissipation point, it implies that further power dissipation reduction is impossible through replacing non-input-microcell and CD circuits with its corresponding input-complete microcell. Then, for each non-input-complete microcell, we can obtain that the number of unchecked wires is smaller than or equal to the threshold n_i , namely, $N_{WUC,i} \leq \max(\lfloor n_i \rfloor, 0)$, where $1 \leq i \leq M_{NIC}$. Obviously, the number of unchecked wires $N_{WUC,i}$ is smaller than or equal to the number of primary input, $N_{WUC,i} \leq I_i$, where $1 \leq i \leq M_{NIC}$; hence we can obtain $N_{WUC,i} \leq \min(I_i, \max(\lfloor n_i \rfloor, 0))$ where $1 \leq i \leq M_{NIC}$. Therefore, the number of CD circuits required for ensuring quasi-delay-insensitivity is:

$$M_{CD} = \sum_{i=1}^{M_{NIC}} N_{WUC,i} \leq \sum_{i=1}^{M_{NIC}} \min(I_i, \max(\lfloor n_i \rfloor, 0)) . \quad \blacksquare$$

Furthermore, we consider the 2-input microcells in Table I, for example AND, OR, XOR, we can observe that the n_i for each microcell satisfies $0 < n_i < 1$; hence we can obtain the following corollary, which can be employed to accelerate the convergence of the lowest power dissipation point searching process.

Corollary 1: If $0 < n_i < 1$, where $1 \leq i \leq M_{NIC}$, the lowest power dissipation point $P_{m\%}$ has the attribute: $M_{CD} = 0$.

Proof: According to the Theorem 1, we can obtain $M_{CD} \leq 0$ if $0 < n_i < 1$. Since M_{CD} cannot be negative, so $M_{CD} = 0$. $\blacksquare$

For completeness, we also present the upper power dissipation boundary which connects $P_{0\%}$ and $P_{100\%}$. The upper power dissipation boundary could be an almost straight line or a concave-down line or a concave-up line, depending on the circuit complexity and structure. Initially, since we only consider the region $0 \leq n_i \leq I_i$ for threshold n_i , the replacement of any combination of non-input-complete microcells and CD circuits with the corresponding input-complete microcells will slightly reduce the power dissipation. After some of the non-input-complete microcells have been replaced, which reduce power dissipation marginally, a certain combination that satisfies $N_{WUC,i} < n_i$ will appear. In the next replacement attempt, these combinations will first be replaced and the overall power dissipation will now increase marginally. The amount of increased/decreased power dissipation will determine the contour of the upper power dissipation boundary.

B. Transistor-Count

With respect to the profile of IC area/transistor-count in the proposed microcell-interleaving approach, the analysis is very similar to that of the power dissipation. For clarity, we formulate some key equations as follows.

$$q_i = \frac{TC_{IC,i} - TC_{NIC,i}}{TC_{CD}} \quad (9)$$

where q_i is transistor-count threshold for i th microcell;

$TC_{IC,i}$ is the transistor-count of $G_{IC,i}$;

$TC_{NIC,i}$ is the transistor-count of $G_{NIC,i}$;

TC_{CD} is the transistor-count of a single CD circuit.

The threshold, q_i , also allocates in the three domains as follows.

$$\begin{cases} q_i > I_i & (10a) \\ 0 \leq q_i \leq I_i & (10b) \\ q_i < 0 & (10c) \end{cases}$$

The transistor-count at percentage $r\%$ is modeled as:

$$TC_{r\%}(\beta) \cong M_{CD,\beta} \cdot TC_{CD} + \sum_{s=1}^{M_{IC}} TC_{IC,s}(\beta) + \sum_{t=1}^{M_{NIC}} TC_{NIC,t}(\beta) \quad (11)$$

where β is the arbitrary point at the $r\%$ (within the lower and

upper transistor-count boundaries); $M_{CD,\beta}$ is the total number of CD circuits used at the point β ; M_{IC} is the total number of input-complete microcells at $r\%$; M_{NIC} is the total number of non-input-complete microcells at $r\%$;

$$r\% = \frac{M_{IC}}{M_{IC} + M_{NIC}} \times 100\%.$$

The lowest transistor-count point, $TC_{u\%}$, will satisfy the condition in (12) as follows:

$$\frac{TC_{(u-\Delta)\%} - TC_{(u)\%}}{-\Delta\%} < 0 < \frac{TC_{(u+\Delta)\%} - TC_{(u)\%}}{\Delta\%} \quad (12)$$

According to our analysis, the profile of IC area/transistor-count is (almost) the same as that of power dissipation, because the reduction of power dissipation and transistor-count is largely by reducing the number of CD circuits.

C. Delay

Now we analyze the delay performance profile. For clarity and consistency, we also measure the delay by the percentage of replacement, similar to the power dissipation profile.

The delay profile is depicted in Fig. 6, and it is a region surrounded by the lower delay boundary and upper delay boundary. The lower delay boundary begins from $D_{0\%}$, and passes through $DL_{v\%}$ and $D_{z\%}$, and finally reaches $D_{100\%}$; the line connects the points $(D_{0\%}, DU_{v\%}, D_{y\%}, D_{100\%})$ constitutes the upper delay boundary. The shaded region contains the delay of all combinations satisfying QDI attribute. $D_{0\%}$ is the delay of fully non-input-complete microcells whereas $D_{100\%}$ is the delay of fully input-complete microcells, and $D_{0\%} < D_{100\%}$.

The delay of the QDI circuit in a single pipeline can be computed as the sum of forward and backward delays (local cycle time) in (13), and considered as a reasonable measure of performance for a pipeline stage. However, this measure may be of limited value to complex sequential (multiple pipeline) asynchronous circuits, whose analysis could instead be extended by using reported approaches [27], [28].

$$D_{v\%}(\delta) \cong D_{F,v\%}(\delta) + D_{B,v\%}(\delta) \quad (13)$$

Fig. 6 Overall delay profile of all microcell combinations satisfying QDI attribute

where δ is the arbitrary point at the $v\%$ (within the lower and upper delay boundaries); $D_{F,v\%}$ is the forward delay at point δ of $v\%$; $D_{B,v\%}$ is the backward delay at point δ of $v\%$;

$$v\% = \frac{M_{IC}}{M_{IC} + M_{NIC}} \times 100\%.$$

The forward delay is defined as the delay from Req_i to $Input_{i+1}$, through $Register_i$ and combinational circuit, provided $Input_i$ is ready. The backward delay is defined as the delay from $Input_{i+1}$ to Req_i , through $Register_{i+1}$ and RCD_{i+1} (the pipeline stage see Fig. 1(a)).

$$\text{Hence } DL_{v\%} = \min[D_{v\%}(0), D_{v\%}(1), D_{v\%}(2), \dots] \quad (14)$$

$$DU_{v\%} = \max[D_{v\%}(0), D_{v\%}(1), D_{v\%}(2), \dots] \quad (15)$$

On the lower delay boundary, $D_{z\%}$ is the turning point of delay increasing, in other words, the lower delay boundary satisfy the condition in (16) as follows:

$$\begin{cases} \frac{D_{v\%} - D_{(v-\Delta)\%}}{\Delta\%} = \frac{D_{(v+\Delta)\%} - D_{v\%}}{\Delta\%} = 0 & \text{where } 0 < v < z \\ \frac{D_{(v+\Delta)\%} - D_{v\%}}{\Delta\%} \geq \frac{D_{v\%} - D_{(v-\Delta)\%}}{\Delta\%} > 0 & \text{where } z < v < 100 \end{cases} \quad (16)$$

This situation can be appreciated as the replacement of non-input-complete microcells is initially located at non-critical paths, then critical path.

Similar analysis can be applied to the upper delay boundary, where $D_{y\%}$ is the turning point, and the upper boundary follow:

$$\begin{cases} \frac{D_{v\%} - D_{(v-\Delta)\%}}{\Delta\%} \geq \frac{D_{(v+\Delta)\%} - D_{v\%}}{\Delta\%} > 0 & \text{where } 0 < v < y \\ \frac{D_{v\%} - D_{(v-\Delta)\%}}{\Delta\%} = \frac{D_{(v+\Delta)\%} - D_{v\%}}{\Delta\%} = 0 & \text{where } y < v < 100 \end{cases} \quad (17)$$

The reason is the converse of that for lower delay boundary, in other words, the replacement of non-input-complete microcell is initially located at critical path, then non-critical paths.

IV. THE PROPOSED MICROCELL-INTERLEAVING GENETIC ALGORITHM (MIGA)

The objective of this section is to search for the optimal combination of input-complete and non-input-complete microcells with the objective of achieving lowest power dissipation or the shortest delay, equivalent to point $P_{m\%}$ in Fig. 5 or point $DL_{v\%}$ in Fig. 6 respectively. In general, the lowest power dissipation point, $P_{m\%}$, is near to the smallest number of transistor-count point.

The most obvious way is to search all possible combinations exhaustively. However, as the number of combinations increases exponentially with the number of microcells in one circuit, this renders an exhaustive search virtually impossible for a circuit with a large number of microcells. Specifically, the search space (complexity) is N^M , where N and M are respectively the number of types of library cells and microcells in a given circuit. ($N=2$ in the experiments and $M \approx 400$ in the benchmark circuits herein). The search space in the experiment herein is hence $\sim 2^{400}$. Due to the gargantuan magnitude of the

search space, some search algorithms, such as genetic algorithm [29]-[34] greedy algorithm [35], and dynamic programming [36], should be employed to search for the optimal solution.

The principle of genetic algorithm is to mimic the process of natural selection, where a population of candidate solutions to an optimization problem is evolved toward better solutions by selection, crossover and mutation. The genetic algorithm has the advantage of low possibility of being trapped at local optimal solutions compared to the greedy algorithm, but it is computationally-wise somewhat inefficient. The principle of greedy algorithm is to make the locally optimal choice at each stage with the objective of finding a global optimum. Although the greedy algorithm is computationally more efficient than the genetic algorithm, it suffers from the high possibility of being trapped at a local optimal solution as the decisions made are not changeable. Dynamic programming breaks down the complex problem into a number of sub-problems and thereafter combines the sub-solutions to obtain an optimal solution; it is highly applicable to complex problems with optimal substructure. In view of the disadvantage and requirement of greedy algorithm and dynamic programming, we adopt the genetic algorithm in this paper. We will later present the comparisons on the results (of the proposed approach) generated by genetic algorithm, greedy algorithm and dynamic programming in Section V.

The pseudo-code of the proposed MIGA, which is largely based on the reported genetic algorithms, is depicted in Fig. 7. The input to the MIGA is a synthesized combinational circuit netlist whereas the output is the optimized microcell-interleaving QDI netlist. The **Preprocessing** operation will encode the (input-complete and non-input-complete) microcells of the input combinational circuit netlist into chromosome on the basis of their

The proposed microcell-interleaving genetic algorithm (MIGA)

Input:

Netlist_input: standard single-rail combinational circuit netlist

```

01. Preprocessing:
02. formulate netlist Connection(Gate, Wire);
03. generate Chromosome(Gate);
04. Initial_population_generation:
05.   for  $i=1,2,\dots,number\_of\_population$ 
06.     generate_initial_population(Chromosome(Gate));
07.   end for
08. MIGA_main_loop: for  $i=1,2,\dots,prescribed\_generation$ 
09.   Evaluation: for  $j=1,2,\dots,number\_of\_population$ 
10.     case(optimization_target);
11.       power: fitness_value= calculation_Power();
12.       transistor_count: fitness_value= calculation_TC();
13.       delay: fitness_value= calculation_Delay();
14.     end case
15.     Optimal_chromosome=update_optimal_chromosome();
16.   end for
17. Selection:
18.   select(population);
19. New_population_generation:
20.   for  $j=1,2,\dots,number\_of\_new\_children$ 
21.     crossover();
22.   end for
23.   mutation();
24. end for
25. Mapping: Netlist_optimized=MapChromosomeToNetlist(Optimal_chromosome);

```

Output:

Netlist_optimized: optimal microcell-interleaving dual-rail netlist

Fig.7 Pseudo-code of the proposed Microcell-Interleaving Genetic Algorithm

interconnections. First, the **Initial_population_generation** will randomly generate an initial population (300 in our simulations) of chromosomes. Then, the **Evaluation** process evaluates the fitness value of each chromosome in the population in terms of their power dissipation, transistor-count and delay. With higher fitness value proportional to higher selection probability based on the roulette-wheel selection scheme [27], the **Selection** process selects a group of chromosomes to be the parent chromosomes, the purpose of the **Selection** process in MIGA is to exploit the optimal regions in the search space.

One-point **Crossover** operation [27] applies to two selected parent chromosomes to generate (produce) two offspring chromosomes with a crossover rate of 0.8. The **Crossover** operation is to exchange the information between two fit chromosomes in order to explore/combine the characteristics of different optimal regions in the search space. Bit-flip **Mutation** [27] applies to every gene of the offspring chromosomes with a small probability of 0.01. This is to avoid the MIGA searching process being trapped in the local optimal regions. After a new generation of population is produced, the processes of **Evaluation**, **Selection**, **Crossover**, and **Mutation** will repeat until the termination condition (500 generations in our simulations) is reached. Finally, the **Mapping** decodes the optimal chromosome with the highest fitness value to an output dual-rail QDI netlist.

In view of the pseudo code depicted in Fig. 7, we can obtain the complexity (number of evaluation of fitness function) of the proposed MIGA as the number of generations multiplied by the population (respectively 500 and 300 in our experiments, where the number of microcells is around 400). Hence, we can appreciate the efficiency of the proposed MIGA by obtaining the (near) global optimum in the large searching space of $\sim 2^{400}$ only with the computational complexity of 1.5×10^5 .

We will now elaborate in details on the combinational circuit netlist to chromosome encoding process and the fitness function formulation of the proposed MIGA in the following sections.

A. Genetic Coding of Combinational Circuit Netlist

The general chromosome is represented as:

$$\text{Chromosome} = \langle G_1 G_2 \dots G_M \rangle \quad (18)$$

where M is the number of microcells in given circuit. In the string chromosome, we put all microcells into a string inconsequentially. For example, the combination of the microcells in Fig. 4(a) can be formulated as *Chro_A* as follows: *Chro_A* = $\langle \text{DCVSL}_1 \text{DCVSL}_2 \text{DCVSL}_3 \dots \text{DCVSL}_{20} \rangle$ (19)

We adopt binary coding where a non-input-complete microcell will be represented by a gene value of '0' and an input-complete microcell by a gene value of '1'. As a point of illustration, the configuration of the circuit in Fig. 4(b) is shown below:

$$\text{Chro_A_b} = \langle 01010101001010101010 \rangle \quad (20)$$

With the proposed genetic coding, the circuit characteristics of a combinational circuit netlist can be effectively encoded in the chromosome in order for the proposed MIGA to search for an optimal combination of QDI netlist.

B. Fitness Function Formulation

For each chromosome, the power dissipation fitness function is the reciprocal of the total power dissipation of the CD circuits, input-complete microcells and non-input-complete microcells, expressed as follows:

$$\text{Fitness}(P) = \frac{1}{\sum_{i=1}^{M_{CD}} P_{CD,i} + \sum_{i=1}^{M_{IC}} P_{IC,i} + \sum_{i=1}^{M_{NIC}} P_{NIC,i}} \quad (21)$$

The transistor-count fitness function is the reciprocal of the total transistor-count of the CD circuits, input-complete microcells and non-input-complete microcells, shown as follows:

$$\text{Fitness}(TC) = \frac{1}{\sum_{i=1}^{M_{CD}} TC_{CD,i} + \sum_{i=1}^{M_{IC}} TC_{IC,i} + \sum_{i=1}^{M_{NIC}} TC_{NIC,i}} \quad (22)$$

where $M_{IC} = \sum_{i=1}^M G_i$, $M_{NIC} = \sum_{i=1}^M (1 - G_i)$, $M_{CD} = \sum_{i=1}^M H_i$ and H_i is obtained as follows:

$$H_i = \begin{cases} 0 & \text{if } \exists G_j, G_j \in (G_i \square), \text{ such as } G_j \text{ is an input-complete} \\ & \text{microcell or if } (G_i -) \text{ is conncted to a primary output} \\ 1 & \text{otherwise} \end{cases} \quad (23)$$

where $(G_i \square)$ are the microcells driven by G_i , and $(G_i -)$ is the output wire of microcell G_i .

The delay fitness function is the reciprocal of the sum of forward delay (D_F) and backward delay (D_B), expressed as follows (for fast calculation, we assume the output of a microcell drives the fan-out of 4 inverters):

$$\text{Fitness}(D) = \frac{1}{D_F + D_B} \quad (24)$$

On the basis of the three basic fitness functions in (21), (22), (24), we can further optimize some composite metrics. For example, energy can be optimized through the proposed MIGA with the fitness function in (25):

$$\text{Fitness}(E) = \frac{1}{\left(\sum_{i=1}^{M_{CD}} P_{CD,i} + \sum_{i=1}^{M_{IC}} P_{IC,i} + \sum_{i=1}^{M_{NIC}} P_{NIC,i} \right) \square (D_F + D_B)} \quad (25)$$

Note that higher fitness values in (21), (22), (24) and (25) imply lower power dissipation, smaller transistor-count, smaller delay and lower energy respectively. This allows the proposed MIGA to employ the fitness values to guide (converge) the search process to the fittest region, which is equivalent to the best combination of QDI netlist.

As an example, we use the circuits in Fig. 4(a)-(d) to calculate the fitness values of power dissipation. The fitness values of transistor-count and delay can be calculated accordingly, and omitted here for simplicity. The power dissipation of the CD circuit, input-complete microcell and non-input-complete microcell (based on the average values of 2-input microcells given in Table I) are 1.1, 1.5, and 1.1 respectively. From the circuit in Fig. 4(a), we can obtain $M_{CD} = 17$, $M_{IC} = 0$, $M_{NIC} = 20$; hence the power dissipation fitness,

$Fitness(P_a) = 1/(1.1 \times 17 + 1.5 \times 0 + 1.1 \times 20) \approx 0.025$. Similarly, $Fitness(P_b) \approx 0.029 > Fitness(P_a)$; $Fitness(P_c) \approx 0.035 > Fitness(P_b)$; $Fitness(P_d) \approx 0.037 > Fitness(P_c)$. From the above four fitness values, we can see higher fitness value reflects lower power dissipation.

V. EXPERIMENTAL RESULTS

We first validate the performance profile analysis (described in Section III) by means of implementation an ISCAS-85 benchmark circuit, C499, embodying DCVSL and/or DSI microcells. Thereafter, we compare the proposed design approach against reported design methodologies based on five ISCAS-85 circuits (C432, C499, C880, C1355 and C1908) using different microcells. To demonstrate the practicality of the proposed design approach, we finally design an 8-tap 16-bit Async QDI FIR filter and compare it against the well-established competing DCVSL, NCL counterparts. Finally, we compare the proposed MIGA against the greedy algorithm to demonstrate the efficiency of our algorithm. For completeness, the circuits are implemented in a 130nm CMOS and simulated in Synopsys Nanosim using spice models, and at the nominal VDD = 1.2V. The transistor sizings of all microcells are 560nm/120nm for PMOS and 280nm/120nm for NMOS, except for the weak keepers where 160nm/500nm for

PMOS, 160nm/1000nm for NMOS. The delay of ISCAS-85 benchmark circuits is computed as the combined delay of an evaluation phase ($Req_{i+} \rightarrow Req_{i-}$) and a reset phase ($Req_{i-} \rightarrow Req_{i+}$); the delay of FIR filter is measured per operation (8-tap) by observing the value changes of primary input and primary output. The time duration of the proposed MIGA optimization for each circuit is negligible (within several minutes) on the HP Pro 3130 Microtower PC computer, with an Intel i7 CPU @2.8GHz, and 4GB RAM.

A. The Performance Profile for C499

Figs. 8(a) - (c) respectively depict the performance profiles of power dissipation, transistor-count and delay for C499, ranging from 0% DSI microcells (i.e. all DCVSL microcells) to 100% DSI microcells along the abscissa. In these profiles, the regions are quantified by the lower and upper boundaries.

From Fig. 8(a), C499 embodying all DCVSL microcells (at 0%) dissipates 460 μ W while that embodying all DSI microcells (at 100%) dissipates 284 μ W. Nonetheless, with our proposed approach, C499 can be redesigned to achieve the lowest power dissipation of 262 μ W (at 57%), 43% and 8% lower than that embodying all DCVSL and all DSI microcells respectively.

From Fig. 8(b), C499 embodying all DCVSL microcells (at 0%) requires 6600 transistors while that embodying all DSI microcells (at 100%) requires 4914 transistors. With our

Fig. 8 Performance of benchmark circuit C499 based on our proposed microcell-interleaved approach and genetic algorithm (a) power profile, (b) transistor-count profile, (c) delay profile, and (d) the number of CD circuits in the searching for the lowest power point.

Table II

The power dissipation (P), transistor-count (TC), delay (t) and a composite metric of $P \times TC \times t$ of the lowest power points for various benchmarks @ 1.2V, 130nm CMOS

Circuits	Power, P (μ W) @ 50MHz					Transistor-Count, TC				
	DCVSL	NCL	DSI	Proposed_1	Proposed_2	DCVSL	NCL	DSI	Proposed_1	Proposed_2
ISCAS C432	2.12×	1.91×	1.11×	1.05×	1×(209)	1.51×	1.49×	1.06×	0.99×	1×(4114)
ISCAS C499	1.82×	1.77×	1.13×	1.04×	1×(253)	1.49×	1.59×	1.11×	1.01×	1×(4440)
ISCAS C880	2.22×	1.97×	1.20×	1.12×	1×(359)	1.56×	1.52×	1.13×	1.02×	1×(7072)
ISCAS C1355	2.33×	1.99×	1.28×	1.17×	1×(473)	1.58×	1.53×	1.15×	1.02×	1×(9628)
ISCAS C1908	2.39×	2.07×	1.28×	1.18×	1×(453)	1.60×	1.55×	1.17×	1.02×	1×(9330)
Average	2.17×	1.94×	1.20×	1.11×	1×(349)	1.55×	1.53×	1.12×	1.01×	1×(6917)

Circuits	Delay, t (ns)					Normalized Overall ($P \times TC \times t$)				
	DCVSL	NCL	DSI	Proposed_1	Proposed_2	DCVSL	NCL	DSI	Proposed_1	Proposed_2
ISCAS C432	0.32×	0.46×	1.03×	0.74×	1×(12.66)	1.03×	1.31×	1.20×	0.76×	1×
ISCAS C499	0.48×	0.77×	1.11×	0.91×	1×(8.41)	1.31×	2.16×	1.38×	0.95×	1×
ISCAS C880	0.41×	0.66×	1.17×	0.89×	1×(10.04)	1.42×	1.98×	1.57×	1.01×	1×
ISCAS C1355	0.41×	0.57×	1.15×	0.92×	1×(11.74)	1.51×	1.73×	1.70×	1.10×	1×
ISCAS C1908	0.43×	0.64×	1.19×	0.88×	1×(11.86)	1.65×	2.05×	1.78×	1.06×	1×
Average	0.41×	0.62×	1.13×	0.87×	1×(10.94)	1.39×	1.85×	1.52×	0.98×	1×

proposed approach, C499 can be redesigned to achieve the least transistor-count of 4482 (at 57%), 32% and 9% lesser than that embodying all DCVSL and all DSI microcells respectively.

From Fig. 8(c), it can be seen that the smallest delay of C499 is 4.07ns (at 0%) and the longest delay of C499 is 9.3ns (at 100%). The upper delay boundary increases steeply along the abscissa, and then becomes flat at the turning point of around 20%. The initial steep increase is caused by the replacements of DSI microcells located on critical path(s). Conversely, the lower boundary remains almost flat at low percentage and increases steeply at high percentage, and the turning-up point is around 60%. In the plateau (<60%), almost all the DSI microcells are allocated at non-critical paths, hence a negligible delay penalty.

As echoed from Figs. 8(a) to 8(c), in this C499 example, it would be highly desirable to interleave 57% of DSI microcells (with 43% of DCVSL microcells) to enjoy low power dissipation, small transistor-count and with some delay penalty (see the delay of the lowest power point in delay profile Fig. 8(c)).

Fig. 8(d) depicts the evolving progress of the number of CD circuits in the searching for the lowest power point. With more generations evolved, the number of CD circuits is finally decreased to 0, which is near the global optimal point. The evolving progress is significant (i.e. fast optimization time) for

large and complex circuits.

B. Comparison on ISCAS-85 Benchmark Circuits

We now consider five ISCAS-85 benchmark circuits based on DCVSL, NCL and DSI microcells. For circuits based on our proposed MIGA, we consider two options, Proposed_1 and Proposed_2. The circuits based on the Proposed_1 are interleaved with DCVSL/DSI microcells, and those based on Proposed_2 are interleaved with NCL/DSI microcells. For sake of fair benchmarking in terms of power and energy, the implementation of each circuit (such as DCVSL, NCL, etc.) is simulated at the same input rate and for the same simulation duration. Table II tabulates the performance values having the lowest power dissipation points. For ease of interpretation, these parameters are normalized to the circuits based on the Proposed_2 (with the lowest power dissipation objective), and the actual numerical values are shown in parentheses.

In terms of power dissipation, the circuits of DCVSL, NCL, DSI are respectively, on average, 2.17×, 1.94× and 1.20× worse than those of the Proposed_2. The circuits of the Proposed_1 are better than those of DCVSL, NCL and DSI, but are 1.11× worse than those of the Proposed_2. Put simply, the type of microcells also plays an important role in optimization.

From the transistor-count perspective, the circuits of the Proposed_2 feature the lowest number. The circuits of DCVSL,

Note: No. of CD circuits before optimization: 3505; No. of CD circuits after optimization: 314

Fig. 9 Block diagram of the 8-tap 16-bit Async QDI FIR Filter

NCL, DSI and the Proposed_1 are 1.55 $\times$, 1.53 $\times$, 1.12 $\times$ and 1.01 $\times$ worse than those of the Proposed_2 respectively.

For delay parameter, the circuits of DCVSL, NCL, and the Proposed_1 feature shorter delay than those of the Proposed_2, where their average delays are 0.41 $\times$, 0.62 $\times$ and 0.87 $\times$ better. As expected, the DSI circuits feature the largest delay.

In the composite power $\times$ transistor-count $\times$ delay, on average, the circuits of the Proposed_1 feature the best (0.98 $\times$ marginally better than those of the Proposed_2), and the circuits of DCVSL, NCL, DSI have 1.39 $\times$, 1.85 $\times$ and 1.52 $\times$ worse overall performance than those of the Proposed_2.

In Table II, the circuits of the Proposed_1 and the Proposed_2 are optimized based on the lowest power dissipation. Although not shown, we could apply our proposed design approach to optimize other parameters (including delay and transistor-count). The multiple-objective optimization is also possible by integrating different fitness functions into a composite fitness function, or implementing a decision maker to subjectively conduct the evolution, but it is beyond of the scope of this paper.

C. 8-Tap Async QDI FIR Filter

Fig. 9 depicts the block diagram of the Async QDI FIR Filter – one of the critical building blocks for our targeted wireless sensor network [1]. It contains Read/Write Control State Machine, an 8 $\times$ 16-bit Coefficient ROM, an 8 $\times$ 16-bit Data SRAM, a 16-bit Multiplier, a 32-bit Adder and the corresponding latches and handshake circuits. Initially, all the latches are reset to empty except Latch 4 is reset to valid ‘0’ for data accumulation. When ‘start’ signal is asserted, Read/Write

Control State Machine will generate the write address and write enable signal on *SRAM_Addr* and *R/W* respectively to write in the input *Data_In*. *Write_ack* signal will acknowledge the completion of writing. Thereafter, Read/Write Control State Machine will generate *SRAM_Addr*, *ROM_Addr*, *R/W* signals to read out data and coefficient, and they are held by Latch 2 and Latch 1 respectively, and then fed to the 16-bit Multiplier. The output of the 16-bit Multiplier is held in Latch 3, and then accumulated in the 32-bit Adder.

We apply the proposed MIGA to combinational circuits (such as the 16-bit multiplier, 32-bit adder, and combinational circuits in state machine) in this FIR filter with the objective of minimizing power dissipation. The microcells used are DCVSL and DSI microcells. We further compare it against the competing NCL counterpart based on the NCL_X methodology and conventional DCVSL. We tabulate the result in Table III, which is normalized on proposed FIR filter and its actual numerical values are shown in parentheses. The proposed FIR filter based on our proposed design approach features the lowest power dissipation, smallest transistor-count and smallest $P \times TC \times t$. The layout view of the proposed FIR filter is shown in Fig. 10, and the area is 0.16mm².

D. Comparisons between Greedy Algorithm, Dynamic Programming and the Proposed MIGA

In order to demonstrate the efficiency of the proposed MIGA, we have implemented five ISCAS benchmark circuits based on the greedy algorithm and dynamic programming, and benchmark them against our proposed MIGA. For the implementation of greedy algorithm, we replace the microcells that have the most significant impact on power dissipation reduction in each evaluation. For the implementation of dynamic programming, we consider each microcell as a stage, and combine the solution of each stage to obtain the global solution. The results are now tabulated in Table IV. From Table IV, the proposed MIGA outperforms the greedy algorithm and dynamic programming by ~10% and ~11% respectively. There are two reasons why the greedy algorithm and dynamic programming are potentially worse than the proposed MIGA. First, the proposed MIGA makes use of multiple search paths and global information to explore the multimodal search space. Second, the circuit optimization problem in this paper does not guarantee to possess the property of optimal substructures (an important property for greedy

Table III

The power dissipation (P), transistor-count (TC), delay (t) and a composite metric of $P \times TC \times t$ of the lowest power point for Async QDI FIR Filter @ 1.2V, 130nm CMOS

	Power, P (μ W)	TC	Delay, t (ns)	$P \times TC \times t$
DCVSL	3.98 $\times$	1.36 $\times$	0.36 $\times$	1.96 $\times$
NCL	2.51 $\times$	1.39 $\times$	0.61 $\times$	2.13 $\times$
Proposed	1 $\times$ (1764)	1 $\times$ (47933)	1 $\times$ (254)	1 $\times$

Fig. 10 The layout of the 8-tap 16-bit Async QDI FIR Filter based on the proposed microcell-interleaving design approach

Table IV

The lowest power points (μ W @50MHz) comparisons between the Greedy Algorithm, Dynamic Programming and the proposed MIGA for five ISCAS85 benchmark circuits @ 1.2V, 130nm CMOS; normalized to the proposed MIGA

	C432	C499	C880	C1355	C1908	Average
DSI	1.11 $\times$	1.13 $\times$	1.20 $\times$	1.28 $\times$	1.28 $\times$	1.20 $\times$
Greedy Algorithm	1.10 $\times$	1.12 $\times$	1.06 $\times$	1.12 $\times$	1.10 $\times$	1.10 $\times$
Dynamic Programming	1.09 $\times$	1.10 $\times$	1.13 $\times$	1.12 $\times$	1.11 $\times$	1.11 $\times$
Proposed MIGA	1 $\times$ (209)	1 $\times$ (337)	1 $\times$ (478)	1 $\times$ (473)	1 $\times$ (453)	1 $\times$

algorithm and dynamic programming to work efficiently).

VI. CONCLUSIONS

We have proposed a novel QDI microcell-interleaving approach for timing-robust async circuits with the objective of sharing the local CD circuits, thereby reducing the hardware overhead circuits. We have analyzed the performance profiles of the proposed microcell-interleaving approach graphically in terms of power dissipation, transistor-count (IC area) and delay. We have also proposed a microcell-interleaving genetic algorithm to implement the proposed microcell-interleaving approach, which involved strategic interleaving of non-input-complete microcells with input-complete microcells. Based on ISCAS-85 benchmark circuits, and by means of an async QDI FIR filter design, we have showed the validity, efficiency and practicality of the proposed design approach compared to reported QDI methodologies, we have further showed the efficiency of the proposed MIGA by comparing against the greedy algorithm. Specifically, the proposed designs on average are $1.77\times$ better in power dissipation, $1.4\times$ better in area, and $1.58\times$ better in a composite metric of $\text{power}\times\text{area}\times\text{delay}$, and reasonably slower for the lowest power dissipation points of ISCAS-85 benchmark circuits. When compared against the greedy algorithm and dynamic programming, the proposed MIGA outperformed them by $\sim 10\%$ and $\sim 11\%$ respectively.

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