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**Fully-Additive Printed Electronics:
Transistor Model, Process Variation and Fundamental Circuit Designs**

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Abstract:

Printed Electronics (PE) on flexible substrates (e.g. plastic-film) is an emerging technology that potentially complements silicon-based electronics. To facilitate the design and realization of PE analog and digital circuits for the augmentation of signal processing thereto, we present in this paper, a novel and comprehensive printed transistor model that is simple, accurate and compatible with industry-standard IC (integrated circuit) electronic design automation tools. Unlike reported models, the proposed comprehensive model accommodates and accurately models the effect of the channel length on carrier mobility, leakage current and parasitic capacitances, and is valid for all transistor operating regions, from cut-off to supra-threshold regions. The proposed comprehensive model further embodies process variations (statistical data) and matching based on various layout techniques. These comprehensive modelings are imperative for the practical design and simulation of PE circuits, including manufacturability and implications with respect to the challenges of PE circuits.

On the basis of the proposed comprehensive model, several fundamental analog and digital PE circuits, based on conventional and novel methods, are designed and realized on plastic-films. Their measured parameters agree well with that obtained from simulations (using the model derived herein), depicting the efficacy of the comprehensive model. This model is particularly useful as it provides invaluable insights to PE circuit and system designers.

Key Word:

Printed Electronics, Organic Electronics, Model, Process Variation, Fully-Additive

I. Introduction

Printed Electronics (PE) is an emerging technology with huge market potential - the Organic Electronics Association (OE-A) [1] envisions the market to grow from \$3B today to \$50B within a decade. The PE printing technologies can in general be classified as either ‘*Mixed Subtractive-Additive*’ (where the processing steps involve subtractive steps, such as etching or lift-off [2-3]) or ‘*Fully-Additive*’ (where the processing steps strictly involve deposition only, without etching or lift-off) processes. The primary shortcomings of the Mixed Subtractive-Additive processes are the complexity of the subtractive steps thereof and the associated high costs. Consequently, it can be argued that the Mixed Subtractive-Additive based PE is Un-Green (use of corrosive chemicals), Not-On-Demand (slow throughput and long (duration) processing), and Not-Cheap (expensive/complex equipment and infrastructure, high wastage of chemicals, in part due to etching/lift-off, etc.). In this sense, Mixed Subtractive-Additive based PE somewhat contravenes the aforesaid frequently-touted attributes of PE. On the other hand, Additive processes are advantageous over Mixed Subtractive-Additive processes – they are congruous with the aforesaid frequently-touted attributes of PE.

At this juncture, reported PE circuits and systems [4-13] are realized using the Mixed Subtractive-Additive processes. To the best of our knowledge, PE circuits and systems based on a Fully-Additive process remain unreported except for our recently reported process and circuits [14-16]. Our specific process – screen printing – includes *p*-type transistors whose carrier mobility is ~3x higher than reported Fully-Additive processes (and rivals that of subtractive processes), a full array of passive elements (resistors, capacitors and inductors with $Q > 10$), and at least two layers of metal interconnections. This process has demonstrated fully functional

analog and mixed-signal processing circuits of note [14] – operational amplifiers (op-amps) and digital-to-analog converters.

Irrespective of the printing process, it is interesting to note that a comprehensive model (including not only an accurate transistor model but also process variation and matching accuracies based on various layout techniques) for the design of PE circuits and systems remains unreported. In the view of the IC design community's practices within the IC industry ecosystem, this comprehensive model is imperative for the PE community, more particularly PE electronics designers, to facilitate their designs and simulations of PE circuits and systems.

Furthermore, at this juncture, despite several reported printed transistor models [17-23], an accurate model for printed transistors remains lacking where reported models have three major shortcomings. First, the effect of transistor channel length on the carrier mobility is not modeled. However, this is usually not the case when the transistors are printed using a Fully-Additive printing process, especially for small molecule-based semiconductors such as Pentacene, TIPS-Pentacene, etc., see later. Second, reported models are usually inaccurate in the subthreshold region and/or cut-off region; note that from the circuit design perspective, transistor characteristics in deep-subthreshold region and/or cut-off region are important especially in digital circuit designs as they affect several key parameters including noise margin, leakage current, etc. Third, statistical data (such as process variations), matching accuracy and the effect of layout are unreported. Collectively, these are important as they largely determine the reliability, robustness, manufacturability and yield of PE circuits and systems.

In this paper, we propose, arguably the first-ever, comprehensive model for PE targeted for our Fully-Additive screen printing process, including a novel model for printed transistors, and their process variations (statistical data). The proposed transistor model is based on the

established AIM-SPICE level 15 model [30] but with three imperative augmentations to account for the effect of channel length on carrier mobility, for all operating regions – from the supra-threshold region to the cut-off region, and for the leakage current and parasitic capacitances. The proposed model is verified to be accurate (and useful) by benchmarking it against measurements on individual transistors and on the basis of a number of analog and digital circuits.

To augment the comprehensiveness of our comprehensive model to facilitate practical design of PE circuits and systems, we further investigate the effect of different layout techniques on matching accuracy of printed transistors. We show that by means of appropriate layout, printed transistors can be accurately (in the context of PE) matched – a relatively low mismatch of ~8% can be achieved despite variations of ~30% between individual transistors; for completeness, ~39% variations is reported in another process [3]. This perhaps somewhat contradicts the common perception within the PE community that the matching between printed transistors is poor.

On the basis of the proposed comprehensive model, several fundamental analog and digital circuits are designed, printed and measured. These circuits encompass simple conventional circuits (including an amplifier, inverter and ring oscillator) and improved circuits (including our reported proposed high gain amplifier, inverter with level shifter [31] and ring oscillator with level shifter). By means of simulations (including Monte Carlo simulations of these circuits (based on the comprehensive model herein)) and measurements on printed circuits, the performance of these circuits are benchmarked and their design implications are delineated. The benchmarking shows good agreement between simulations and measurements, thereby depicting the accuracy of the proposed printed transistor model and providing invaluable insights to PE circuits and systems designers.

This paper is organized in the following manner. In Section II, the effect of channel length on carrier mobility is investigated and the novel transistor model for our Fully-Additive printing process is proposed. In Section III, statistical measurement data are presented and an investigation into the effect of layout on transistor matching is discussed. In Section IV, several fundamental analog and digital circuits are designed and printed. The proposed transistor model is verified by comparing simulations based on the proposed model and measurements on printed circuits. The performance of these circuits is discussed and compared, and the implications of printed circuits are delineated. Finally, conclusions are drawn in Section V.

II. Modeling of Printed Transistors

A) Review of our Fully-Additive printing process

In this section, our Fully-Additive printing process [14] is first reviewed, where it is arguably the state-of-the-art Fully-Additive process in terms of transistor carrier mobility, capability to realize complete circuits of note, and its congruity to the frequently-touted advantages of PE.

Fig. 1(a) depicts the cross sectional view of our bottom gate printed transistors and the microphotograph of its cross section is depicted in Fig. 1(b). In the latter, note that because the semiconductor layer is relatively thin ($\sim 100\text{nm}$) compared to the other layers ($\sim 20\mu\text{m}$), it is not visible. The printing steps and materials used for each layer are summarized in Table I. Our Fully-Additive printing process is also able to print passive components, including capacitors, resistors and inductors. The resistivities of the printed transistors range from $3.3\text{k}\Omega/\square$ to $800\text{k}\Omega/\square$ (depending on the resistive inks), the capacitances of the printed capacitors range from $224\text{pF}/\text{cm}^2$ (for single dielectric-layer) to $1.1\text{nF}/\text{cm}^2$ (for quintuple dielectric-layer), and the

inductances of the printed inductors range from $1\mu\text{H}$ to $8\mu\text{H}$ with a relatively high $Q = 10$ at 10MHz .

Fig. 1: (a) Cross sectional view of our Fully-Additive Bottom Gate printed transistor (not to scale), and (b) Microphotograph of the cross section of our printed transistor

Table I: Our Fully-Additive printing process

Layers	Materials	Printing Procedure
Layer 0: Substrate (flexible plastic film)	Polycarbonate	Clean the substrate to remove contaminants
Layer 1: Gate, bottom electrode of capacitors, inductor	Silver	With the First stainless screen mask, print the pattern of Layer 1, and then cure in an oven
Layer 2: Dielectric of transistors and capacitors, isolation between top and bottom interconnections	Dupont 5018 [32]	With the Second stainless screen mask, print the pattern of Layer 2, and then cure in UV light
Layer 3: Resistor	Dupont 5036 [32], Dupont 7082 [32]	With the Third stainless screen mask, print the pattern of Layer 3, and then cure in an oven
Layer 4: Drain, source, top electrode of capacitors, vias, interconnections	Silver	With the Fourth stainless screen mask, print the pattern of Layer 4, and then cure in an oven. Thereafter, immerse into the PFBT (Pentafluorobenzenethiol) solution for 1 hour
Layer 5: Semiconductor	TIPS-Pentacene	Coat Layer 5 using a slot die coater and then cure on a hotplate

B) Modeling of printed transistors

Our proposed transistor model is based on the established AIM-SPICE Level 15 model for hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) with augmentations to account for the effect of channel length on carrier mobility, for both supra-threshold and cut-off regions and for leakage current and parasitic capacitances. The AIM-SPICE Level 15 model is adopted because it is compatible with IC industry standard electronic design automation tools and because the defects of printed transistors (being similar to a-Si: H TFTs) can be sufficiently modeled.

Nevertheless, for our Fully-Additive printed transistors, the AIM-SPICE Level 15 model is inadequate for the following shortcomings. First, the effect of channel length (L) on carrier mobility (μ) of printed transistors is not modeled; note that unlike conventional silicon transistors and a-Si: H TFTs, the carrier mobility of printed transistors is usually channel length dependent. Second, the AIM-SPICE Level 15 model can only adequately model the operation of Fully-Additive printed transistors in the supra-threshold region but not in the linear, sub-threshold and cut-off regions. Third, the AIM-SPICE Level 15 model does not adequately model the leakage current and the parasitic capacitances of the Fully-Additive printed transistors. This is largely because both the leakage current and the parasitic capacitances in a-Si: H TFTs are much lower.

To accommodate these three shortcomings, we make three augmentations to the conventional AIM-SPICE level 15 model and these will now be discussed in turn.

(a) The effect of channel length on carrier mobility

In printing processes where the semiconductors are based on small molecule materials (such as TIPS-Pentacene), the channel is formed by numerous small crystals instead of a single crystal

or a film. In this case, the carrier mobility is largely limited by the number of crystals because the speed of the carrier traveling across the crystal boundaries is much slower than in a single crystal. As the number of crystals is channel length dependent, the carrier mobility of printed transistors is hence also channel length dependent.

On the basis of measurements on numerous printed transistors, μ is empirically derived and can be expressed as:

$$\mu = \frac{\theta + 5^{\frac{L_{norm}}{L}}}{\theta + 5^{\frac{L}{L_{norm}}}} \mu_{norm} \quad (1)$$

where L is the channel length,

μ_{norm} is the carrier mobility when channel length is L_{norm} , and

L_{norm} is the nominal channel length which is 100 μm .

(b) Cut-off region coefficient

To model the transistor for all operating regions from cut-off to supra-threshold regions, a cut-off region coefficient is augmented to the reported AIM-SPICE Level 15 model. For our process, the cut-off region coefficient is empirically derived and can be expressed as:

$$C_{cutoff} = \frac{1 + \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{TH}} \right)^\omega}{1 + [1 + V_m - \varphi(V_{GS} + V_m + V_{TH})] \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{TH}} \right)^\omega} \quad (2)$$

where V_{TH} is the threshold voltage,

V_{DS} is the voltage across the drain and source,

V_{GS} is the voltage across the gate and source,

V_m is the modulation voltage,

ϕ is the voltage modulation parameter, and

ω is the power law modulation parameter.

By accounting for the channel length effect and the cutoff region, the drain-source current of our Fully-Additive printed transistors can be modeled as:

$$I_{DS} = \frac{C_{cutoff} \times \frac{W}{L} C_{ox} \times \mu \times (V_{GS} - V_{TH})^{1+GAMMA}}{(VAA)^{GAMMA} + \frac{W}{L} \times C_{ox} \times \mu \times R \times (V_{GS} - V_{TH})^{1+GAMMA}} \times \frac{V_{DS}(1 + LAMDA \times V_{DS})}{[1 + (V_{DS}/V_{sate})^M]^{1/M}} \quad (3)$$

where W is the channel width,

C_{ox} is the gate dielectric capacitance,

V_{TH} is the threshold voltage,

R is the drain and source resistance,

VAA is characteristic voltage for field effect mobility,

$GAMMA$ is the power law mobility parameter,

$LAMDA$ is the output conductance parameter,

$ALPHASAT$ is the saturation modulation parameter,

M is the knee shape parameter, and

$V_{sate} = ALPHASAT(V_{GS} - V_{TH})$ is the saturation voltage.

(c) Leakage current and parasitic capacitances

In the Fully-Additive printed transistors depicted in Fig. 1, the gate capacitance is largely determined by the overlap between the gate electrode and drain/source electrodes and is largely independent of the operating region of the transistor. Consequently, the parasitic capacitances of

the Fully-Additive printed transistor can be easily modeled as ideal capacitors, C_{GS} and C_{GD} , as depicted in Fig. 2 below.

The leakage current of the printed transistor is largely due to the leakage in the dielectric material. On the basis of measurements, the leakage current is found to be largely proportional to the voltage across the electrodes. Hence, the leakage current can be simply modeled as resistors across the gate and drain/source electrodes, R_{GS} and R_{GD} , depicted in Fig. 2 below.

Fig. 2: Equivalent circuit of Fully-Additive printed transistors

On the basis of measurements, the parasitic elements (capacitors and resistors) can be empirically derived and modeled as follows:

$$C_{GS} = C_{GD} = C_{ox} \times W \times F \quad (4)$$

$$R_{GS} = R_{GD} = \frac{R_{ox}}{W \times (L + F)} \quad (5)$$

where F is the electrode finger width, and

R_{ox} is the gate-electrodes resistance.

Table II summarizes the nominal process parameters of our Fully-Additive printed transistors embodying the three augmentations to the established AIM-SPICE level 15 model.

Table II: Process parameters of our Fully-Additive printed transistors

Parameter	Value	Parameter	Value
μ_{norm}	$0.81\text{cm}^2/\text{Vs}$	KVT	$-0.036\text{V}/^\circ\text{C}$
L_{norm}	$100\mu\text{m}$	$LAMDA$	0.0008V
Φ	0.08	M	1.5474
Θ	45	RD	$9\times 10^4\ \Omega$
Ω	60	RS	$9\times 10^4\ \Omega$
$ALPHASAT$	0.6875	$SIGMA0$	1.97×10^{-16}
$CGDO$	0	$TNOM$	$27\ ^\circ\text{C}$
$CGSO$	0	TOX	$2\times 10^{-5}\text{m}$
$DEF0$	0.6eV	$V0$	0.12V
$DELTA$	2	VAA	10^9V
EL	0.35eV	$VDSL$	12V
EMU	0.06eV	VFB	-92.6V
EPS	4	$VGSL$	12V
$EPSI$	34	$VMIN$	0.3V
$GAMMA$	10^{-10}	V_{TH}	-0.837V
$GMIN$	$10^{23}\text{m}^{-3}\text{eV}^{-1}$	C_{ox}	$223\text{pF}/\text{cm}^2$
IOL	$3\times 10^{-14}\text{A}$	R_{ox}	$6\times 10^6\ \Omega\text{m}^2$
$KASAT$	$0.006\ ^\circ\text{C}^{-1}$	V_m	3V

Using the aforesaid transistor model and the parameters in Table II, Fig. 3 compares the input-output and output characteristics of the Fully-Additive printed transistors obtained from the transistor model and that obtained experimentally. It can be seen that there is good agreement, thereby depicting the accuracy of the proposed transistor model. The accuracy (and usefulness) of this developed model will be further verified in Section IV by comparing simulation results of and measurements on several fundamental PE circuits.

Fig. 3: Model verification of transfer and output characteristics of proposed Fully-Additive printed transistors

III. Process variations and mismatch of printed transistors

In this section, the process variations and the effect of layout on transistor mismatch will be discussed. As delineated earlier, these considerations are imperative for practical PE circuits, including manufacturability.

Process variations

The electrical characteristics of 35 Fully-Additive printed transistors are measured and summarized in Fig. 4. The mean carrier mobility is $0.81 \text{ cm}^2/\text{V}\cdot\text{s}$ with a standard deviation of $0.257 \text{ cm}^2/\text{V}\cdot\text{s}$. The mean threshold voltage is 1.97 V with a standard deviation of 0.89 V .

Fig. 4: Characteristics distribution of our Fully-Additive printed transistors

It is interesting to note that the process variations of our Fully-Additive printed transistors is relatively low in the context of PE, and perhaps somewhat surprising, they are lower than some subtractive processes, for example, [3]. This ‘low variation’ is important in view of the low cost, simplicity, etc., of the Fully-Additive process compared to the expensive, considerably more complex, etc., subtractive process; refer to Section I earlier.

For completeness, the measurements show that the transistors located at the edges of the coating direction tend to have higher carrier mobility. Specifically, the mean carrier mobility of printed transistors located at the edge of coating direction is $0.96 \text{ cm}^2/\text{V}\cdot\text{s}$, equivalent to $\sim 15\%$ higher than that located in the center. However, the process variations of printed transistors located at the edges are significantly higher. From a practical circuit design perspective, it is

hence prudent to layout transistors requiring higher mobility to be placed at the edges. However, if a circuit design requires transistors with reduced variations, we recommend the placement of dummy transistors at the edges – a practice practiced in some silicon-based designs.

Another practical means to reduce variations is to employ larger transistors, a similar practice in silicon-based circuit designs. Specifically, the standard deviation of the carrier mobility of our Fully-Additive printed transistors is 45.41% for transistors with small width (e.g. $W=4,000\mu\text{m}$) and 30.7% for transistors with large width (e.g. $W=40,000\mu\text{m}$).

Layout and mismatch

In this section, transistor matching based on four well-established layout techniques are compared. These techniques include the simple layout, interdigitation, common centroid and the 2D common centroid layouts. Fig. 5 depicts the microphotographs and measured input-output characteristics (with variations Δ/I) of our Fully-Additive printed transistors based on these layout techniques. The aspect ratio of these transistors is $W/L=40000\mu\text{m}/100\mu\text{m}$. For sake of matching and to eliminate aforesaid effects of edge coating, dummy transistors are strategically placed accordingly. In the microphotograph, M_{1a} and M_{1b} respectively denote the first and second half of the first transistor M_1 ; M_{2a} and M_{2b} respectively denote the first and second half of the second transistor M_2 ; and M_0 denotes the dummy transistors.

Fig. 5: Microphotograph and measured input-output characteristics of

(a) Simple layout, (b) Interdigitation, (c) Common centroid, and (d) The 2D common centroid layout

From Fig. 5, the following observations are made:

- (i) Overall, the matching accuracy is relatively good in the context of PE transistors. Specifically, the mismatch between a transistor pair is $\sim 48\%$ for the simple layout (Fig. 5(a)), and in the best case, is markedly improved by 5.5x to $\sim 8.71\%$ for the 2D common centroid layout (Fig. 5(d)).
- (ii) Of these layout techniques, the simple layout features the smallest area but at the cost of the worst matching accuracy while the 2D common centroid layout features the best matching accuracy but at the cost of the largest area. Compared to the simple layout, the interdigitation layout, common centroid layout, and 2D common centroid layout improve the matching accuracy by $\sim 2.2x$ (21.6%), $\sim 2.8x$ (17.05%), and $\sim 5.5x$ (8.71%) respectively, but at the cost of increased area by 55%, 36% and 65% respectively. The area overhead is largely due to the interconnections.

IV. Implications of printed transistor characteristics on analog and digital circuits

The implications of the process variations and employment of various transistor matching techniques will now be delineated by comparing the performance of several fundamental analog and digital circuits designed based on conventional design methods and that based on improved methods for PE. In this section, the simulations are based on the assumption that all the transistors in the circuits follow the characteristics distribution presented in Fig. 4. Of all the 36 parameters listed in Table II, μ_{norm} and V_{TH} are set as variables – in the context of simulations, variables are the parameters are varied in different simulations. To vary μ_{norm} and V_{TH} , a list of 500 samples is randomly (according to their distribution) generated. Parametric simulations are performed to obtain the desired parameters.

Fundamental Analog Circuits – Amplifiers

Figs. 6(a)-(c) depict the schematic of our proposed single-stage [14], conventional single-stage and conventional three-stage differential amplifiers. The microphotograph of the Fully-Additive printed proposed and conventional single-stage differential amplifiers is depicted in Figs. 6(d) and (e) respectively, and the layout of the conventional three-stage amplifier is depicted in Fig. 6(f). The supply voltage of these differential amplifiers is $V_{DD}=60V$. Our proposed single-stage amplifier embodies a novel positive-cum-negative feedback loop which simultaneously improves the gain and output common-mode voltage variation without compromising the gain-bandwidth product and offset voltage. The operation of this amplifier has been delineated in detail in [14]. Of the three amplifiers, the conventional single-stage amplifier features the simplest hardware, while the hardware of the proposed single-stage amplifier and the conventional three-stage amplifier are comparable; the transistor count and area of the three amplifiers are indicated in Fig. 6.

Fig. 6: (a) - (c) Schematics of the proposed single-stage amplifier and conventional single-stage and conventional three-stage differential amplifiers, (d) and (e) Microphotographs of the proposed and conventional single-stage amplifiers, (f) Layout of conventional three-stage amplifier, (g) Time domain input-output waveforms, and (h) Frequency responses [14]

To verify our proposed comprehensive model and to delineate the advantages of our proposed amplifier over the conventional amplifiers, Figs. 6(g)-(h) respectively depict their time

domain input-output waveforms and frequency responses obtained from simulations and from measurements. It is apparent herein that the simulation results agree well with the measurements, thereby verifying the accuracy of the proposed comprehensive model. It is also apparent that the gain of the proposed single-stage amplifier is significantly higher than the conventional single-stage amplifier whilst their gain-bandwidth product is comparable. For completeness, the simulation results for the conventional three-stage amplifier are also depicted. It is apparent that although the printed area and transistor count of the proposed single-stage and conventional three-stage amplifiers are similar, the proposed single-stage amplifier features significantly improved gain ($\sim 30\text{dB}$ vis-à-vis $\sim 13\text{dB}$) and gain-bandwidth product ($\sim 80\text{Hz}$ vis-à-vis $\sim 5\text{Hz}$).

To compare the sensitivity of the proposed single-stage and conventional single-stage amplifiers on process variations and to further verify our proposed comprehensive model, 500 Monte Carlo simulations on several key parameters of the said two amplifiers are performed. These parameters include the gain, gain-bandwidth product, common-mode voltage variation and offset voltage, and are depicted in Fig. 7. For completeness, the measurements of the printed amplifiers (5 circuits for each amplifier, a total 10 circuits) are indicated in the histograms.

Fig. 7: Monte Carlo Simulations: (a) Gain, (b) Gain-bandwidth product, (c) Common-mode voltage variation, and (d) DC offset. Measurements are denoted by ‘o’ and ‘x’ for the proposed single-stage and conventional single-stage amplifiers.

On the basis of the histograms in Fig. 7, the following observations are made:

- (i) From Figs. 7(a), (b) and (d), the respective measured gain, gain-bandwidth product and DC offset of both printed designs are relatively close to the average of the 500 Monte Carlo simulations. In this sense, the proposed model described in Section II is verified.
- (ii) From Fig. 7(a), and as expected, the gain of the proposed single-stage amplifier is significantly higher than the conventional single-stage design – this is due to the positive

feedback path embodied in the proposed amplifier. Specifically, the mean value of the gain and standard deviation for proposed and conventional single-stage amplifiers are 34.1dB and 25.5%, and 7.26dB and 11.2%, respectively.

- (iii) From Fig. 7(b), and as expected, the gain-bandwidth product of the two amplifiers is comparable. Specifically, the mean value of the proposed and conventional single-stage amplifiers is 84Hz and 85Hz respectively. Interestingly, the spread of the gain-bandwidth product of the proposed single-stage amplifier is smaller (better) – its standard deviation is 2.7% vis-à-vis 9.5% for the conventional single-stage amplifier.
- (iv) From Fig. 7(c), and as expected, the output common-mode voltage variation of the proposed single-stage amplifier is significantly smaller than that of the conventional single-stage amplifier. From a practical circuit perspective, this is an important advantage.
- (v) From Fig. 7(d), the DC offset and the spread of the DC offset of the two amplifiers are largely comparable, despite the gain of the proposed single-stage amplifier being significantly higher (see item (ii)).

Fundamental Digital Circuits - Inverters and Ring oscillators

Consider now the implications of the printed transistor characteristics on fundamental digital circuits, represented by inverters and ring oscillators based on the conventional design and a simple improved design embodying a level shifter [31]. Two critical parameters, input-output characteristics and noise margin, are investigated, measured and compared against simulations.

Figs. 8(a)-(d) depict the schematic and microphotograph of the conventional inverter and the inverter with level shifter. Their input-output characteristics obtained from simulations and from measurements are depicted in Figs. 8(e)-(f) respectively. The supply voltage and the bias voltage

are respectively $V_{DD} = 60V$ and $V_{bias} = 90V$. It is apparent that for both designs, the simulation results agree well with measurements, thereby verifying our proposed model. Furthermore, a comparison of the noise margin of the two inverters shows, as expected, that the inverter with level shifter features significantly improved noise margin. Specifically, the noise margin of the conventional inverter and inverter with level shifter is respectively 0.8V and 19.9V. From a circuit perspective, the improved noise margin yields improved robustness of digital circuits, and is an imperative consideration in digital designs, see later. Nevertheless, the penalty is the ~100% increased printed circuit area and ~40% reduced speed.

Fig. 8: (a) and (b) Schematics of the conventional inverter and the inverter with level shifter, (c) and (d) Their microphotographs, and (e) and (f) Input-output characteristics and corresponding noise margin (■).

500 Monte Carlo simulations to ascertain the noise margin of the two different inverters are performed and benchmarked as depicted in Fig. 9. 5 circuits for each inverter are measured. It is apparent that the measured noise margin of both inverters is very close to their respective mean values obtained from Monte Carlo simulations, hence verifying our proposed model. It is also apparent, as expected, that the noise margin of the inverter with level shifter is improved significantly over the conventional inverter. Specifically, the noise margin of the conventional inverter is noise margin high (NMH) =1.4V with a standard deviation of 104.3% and noise margin low (NML) =50.5V with a standard deviation of 11.4%. In comparison, the noise margin of the inverter with level shifter is improved to NMH=27.6V with a standard deviation of 11.2% and NML=24.2V with a standard deviation of 19.2%. From a circuit perspective, the positive noise margins ensure proper operation of the inverter and negative values result in a failure of the operation and signal propagation – improved noise margins consequently result in improved circuit reliability.

Fig. 9: Monte Carlo simulations: (a) Noise margin high and (b) Noise margin low. Measurements are denoted by ‘x’ and ‘o’ for the inverter and the inverter with level shifter respectively.

To illustrate its effect on reliability and speed, the simple conventional ring oscillator and ring oscillator with level shifter are designed, printed and measured. 5 circuits for each ring

oscillators are measured. Their schematics, microphotographs and Monte Carlo simulations on oscillating frequency are depicted in Fig. 10. Similar to the case of inverters, the supply voltage and the bias voltage are respectively $V_{DD} = 60V$ and $V_{bias} = 90V$. On the basis of Monte Carlo simulations, the failure rate of the simple conventional ring oscillator and the ring oscillator with level shifter is $\sim 53\%$ and 0% , respectively. Put simply, because of the significantly improved noise margin of the inverter with level shifter, it is significantly more robust than the simple ring oscillator. However, as mentioned earlier, the penalty is $\sim 40\%$ lower oscillating frequency and the printed area doubled.

Fig. 10: (a)-(d) Schematic and microphotograph of the simple ring oscillator and ring oscillator with level shifter, and (e) Oscillating frequency of simple ring oscillator and ring oscillator with level shifter.

Measurements are denoted by 'x' and 'o' for the simple ring oscillator and ring oscillator with level shifter.

V. Conclusions

A comprehensive model embodying an accurate yet simple model for Fully-Additive screen printed transistors has been proposed. The proposed model is comprehensive, embodying the effect of channel length on carrier mobility, leakage current and parasitic capacitances and is valid for all operating regions of the transistor. The proposed comprehensive model further embodied statistical data and the matching accuracy of printed transistors based on various layout techniques. On the basis of the proposed comprehensive model, several fundamental analog and digital circuits have been designed and realized. The simulated results and measurements on realized PE circuits agreed well, depicting the efficacy of the proposed comprehensive model.

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