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# A 220-285 GHz SPDT Switch in 65-nm CMOS Using Switchable Resonator Concept

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**Abstract**—The paper reports a SPDT switch operating from 220 to 285 GHz in 65-nm bulk CMOS. The switchable resonator concept by using three coupled-lines topology is proposed and adopted in the switch design. Equivalent circuit models are introduced for analyzing the operation mechanism of proposed switch. The fabricated SPDT switch features measured insertion loss of 4.2 dB including RF pad losses, isolation of 19 dB, return loss of better than 10 dB, simulated  $P_{1dB}$  of 9.2 dBm, and zero power consumption. To the best of authors' knowledge, this switch achieves the highest operating frequency and smallest chip size among reported SPDT switches in CMOS and BiCMOS technologies.

**Index Terms**—CMOS, coupled-lines, miniaturization, silicon, SPDT switches, switchable resonator.

## I. INTRODUCTION

ADVANCEMENT of silicon based technologies provide a promising platform for the low-cost and low-power millimeter-wave (mm-wave) and terahertz communication and imaging systems. Many researchers have demonstrated the mm-wave/terahertz transceiver and imager integrated circuits, e.g. a 220-250 GHz transmitter in [1] and a W-band imager in [2]. However, the single-pole double-throw (SPDT) switch, which is an essential building block to enable transceiver time-division duplex (TDD) when operated as a T/R switch or to eliminate imager fluctuations when operated as a Dicke switch, is still implemented using advanced SOI and HBT technologies for operating frequencies beyond 140 GHz [2]-[5]. Those SPDT switches rely on the  $\lambda_g/4$  ( $\lambda_g$  is the guided wavelength at operating frequency) impedance-inverting transmission line (TL) topology, which presents high level of insertion loss and bulky area on silicon substrates. The high insertion loss is one of the design bottlenecks for mm-wave and terahertz SPDT switches in CMOS and BiCMOS technologies. To alleviate these  $\lambda_g/4$  TLs, switchable resonator was adopted in the single-pole single-throw (SPST) switch

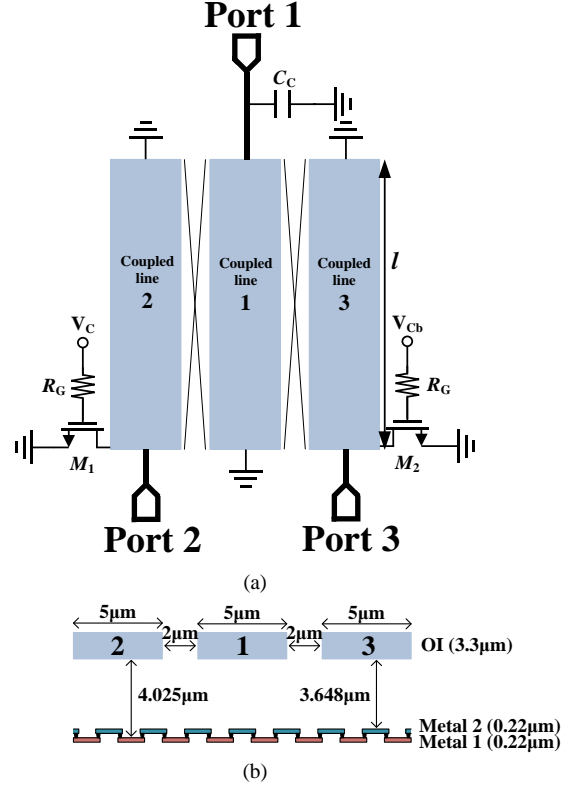


Fig. 1: Proposed SPDT switch using the switchable resonator concept: (a) Configuration; (b) Cross-section view. (Transistors  $M_1$  and  $M_2$ : 17 fingers, single finger  $W = 2\mu\text{m}$ ,  $L = 0.06\mu\text{m}$ ;  $C_c = 19.9\text{ fF}$ ;  $R_G = 8\text{ k}\Omega$ ;  $l = 60\mu\text{m}$ )

designs in [6], where an alternative approach for SPDT switch designs was also presented using the SPST cells and Chebyshev filter synthesis approach.

In the paper, a 220-285 GHz SPDT switch using switchable resonator concept is reported. The resonator is designed with normal RF nFET transistors and three coupled-lines that are closely spaced. The fabricated switch achieves the record highest operating frequency and the smallest chip size among SPDT switches in silicon based technologies.

## II. THEORY AND SWITCH DESIGN

In Fig. 1, the proposed SPDT switch is designed in a commercial 65-nm bulk CMOS. It comprises of three coupled-lines with length  $l$ , two normal RF nFET transistors  $M_1$  and  $M_2$ , one compensating capacitor  $C_c$ , and two biasing resistors  $R_G$  at transistor gate terminals.

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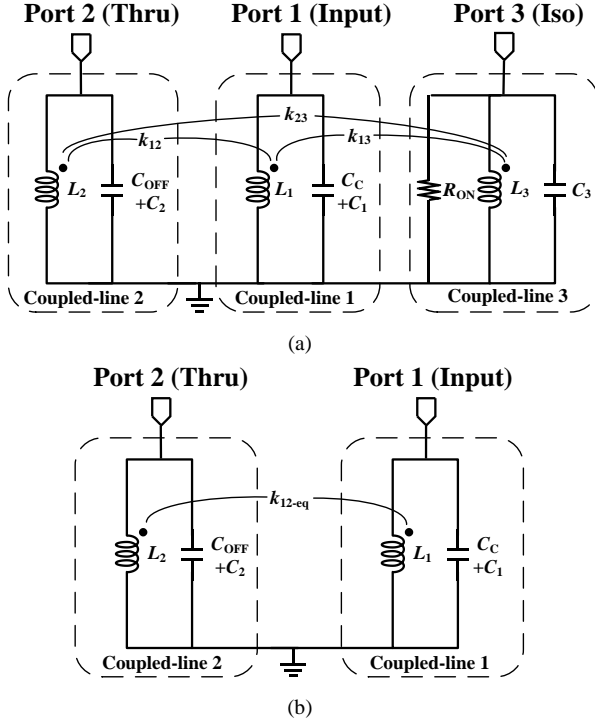


Fig. 2: (a) Equivalent circuit model of the SPDT switch in the operating mode when Port 2 is through port and Port 3 is isolation port; (b) Reduced circuit from (a) by neglecting small  $R_{ON}$ .

In Fig. 2, the basic operating mechanism of proposed SPDT switch is illustrated with equivalent circuit model. In this operating mode, Port 2 is through port and Port 3 is the isolation port, while the opposite operating mode follows the similar operating mechanism. Here, the coupled-lines are modeled as lump elements of self inductors  $L_{1-3}$ , self capacitors  $C_{1-3}$ , and magnetic coupling coefficients  $k_{12, 23, 13}$  as

$$L_1 = L_2 = L_3 = \frac{Z_c \tan(\beta l)}{\omega}, \quad (1)$$

$$C_1 = C_2 = C_3 \approx \frac{\epsilon_0 \epsilon_r w l}{h}, \quad (2)$$

$$k_{ij} = \frac{1}{\sqrt{L_i L_j}} \left[ \frac{\text{Im}(Z_{ij})_{\text{DUT}}}{\omega} \right]_{\text{Low frequency}}, \quad (3)$$

where  $Z_c$  and  $\beta$  are the characteristic impedance and propagation phase constant of the standalone transmission line with length of  $l$  and width of  $w$  at operating frequency  $\omega$ ,  $\epsilon_r$  is the effective dielectric constant of the stacked dielectric materials ( $\epsilon_r = 3.8$  in the used process), and  $h$  is the distance between signal line and metal ground. The coupling coefficients can be extracted using EM simulations of three coupled-lines in Fig. 1(a) as a three-port network and Equation (3). The parasitic resistances of coupled-lines are ignored.

In this operating mode,  $V_C$  is set at 0 V to turn off transistor  $M_1$  whose off-capacitance  $C_{OFF}$  forms a resonating network with the coupled-lines and compensating capacitor. Voltage  $V_{Cb}$  is set at  $V_{DD}$  to turn on transistor  $M_2$  that has small on-resistance to effectively isolate signal from Port 1 to Port 3,

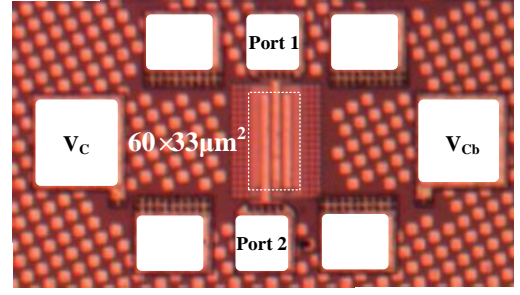


Fig. 3: Die micrograph of fabricated switch.

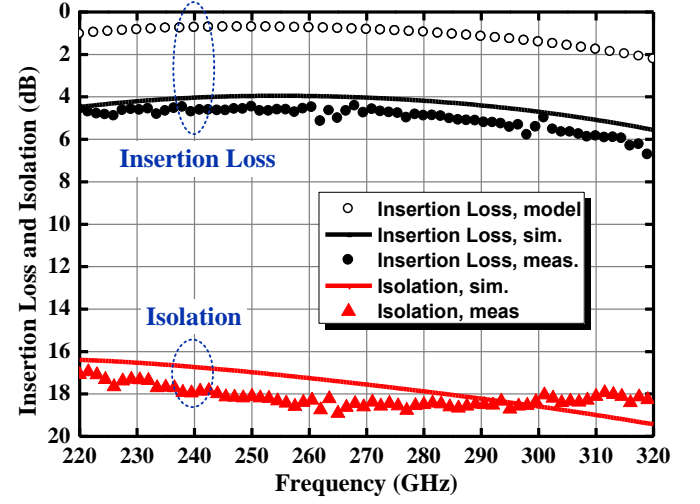


Fig. 4: Insertion loss and isolation from 220 to 320 GHz. (Model in Fig. 2(b);  $L_1 = L_2 = 19$  pH,  $C_{OFF} + C_2 = 17.4$  fF,  $C_C + C_1 = 24$  fF,  $k_{12-eq} = 0.4$ )

which can simply be treated as short-circuit. Thus, the circuit of coupled-line 1 and coupled-line 2 forms a coupled LC resonator as shown in Fig. 2(b), that has a classical bandpass frequency response from Port 1 to Port 2, with the equivalent magnetic coupling coefficient reformulated based on [7] as

$$k_{12-eq} = k_{12} - k_{23}k_{13}, \quad (4)$$

Therefore, the resonator network is switchable based on the control voltages, which effectively performs SPDT switching function. A 220-285 GHz SPDT switch is designed using this topology. Switch transistors are implemented using normal RF nFET with  $R_{ON} \times C_{OFF}$  of 147 fs, while coupled-lines are built using Metal OI as signal lines and stacked Metal 1 and Metal 2 as ground plane with low resistivity. The design parameters are optimized using 3-D full-wave EM simulations by HFSS and circuit co-simulations, which are depicted in Fig. 1(b) and caption of Fig. 1. The fabricated SPDT switch is shown in Fig. 3, where the active area is only  $0.002 \text{ mm}^2$ .

### III. MEASUREMENT

Two-port S-parameter measurements are performed from 220 to 320 GHz using an Agilent 67-GHz PNA-X, a 220-320 GHz VDI's extension module and Cascade WR-3 probes, while Port 3 is internally terminated with an on-chip  $50 \Omega$  resistor. The system is calibrated using an SOLT probe-tip calibration on a Cascade ISS substrate. Therefore, the RF pad

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON OF STATE-OF-THE-ART SPDT SWITCHES OPERATING BEYOND 100 GHz

Ref.	Process $f_T$ (GHz)	Transistor $R_{ON} \times C_{OFF}$ (fs)	Freq. (GHz)	Insertion Loss (dB)	Isolation (dB)	Return Loss (dB)	$P_{1dB}$ (dBm)	DC Power (mW)	Active Area ( $mm^2 / 1000 \times \lambda_0^2$ )	Topology *
[2] TMTT 2010	0.12- $\mu m$ SiGe BiCMOS 200	-	85-105	2.3-3 #	21	>10	-	0	0.0475/4.5	$\lambda_g/4$ TL + SS-SPST
[3] MWCL 2014	0.13- $\mu m$ SiGe HBT 300	83.7	96-163	2.6-3	23.5-29	>10	17 @ 94 GHz	6	0.228/42.5	$\lambda_g/4$ TL + DS-SPST
[4] SiRF 2013	0.12- $\mu m$ SiGe BiCMOS 180	-	110-140	2.5-3.5 #	14.5-17.5	>10	-	-	-	$\lambda_g/4$ TL + SS-SPST
[5] MWCL 2012	45-nm SOI 485	75.6	140-220	3-4.5	20-30	>10	10 †	0	0.1/36	$\lambda_g/4$ TL + DS-SPST
<b>This Work</b>	<b>65-nm CMOS 220</b>	<b>147</b>	<b>220-285</b>	<b>4.2-5</b>	<b>17-19</b>	<b>&gt;10</b>	<b>9.2 †</b>	<b>&lt;4×10<sup>-8</sup></b>	<b>0.002/1.4</b>	<b>Switchable Resonator</b>

\* TL: Transmission line; SS: Single-shunt; DS: Double-shunt # After de-embedding pad loss † Simulation - Not mentioned

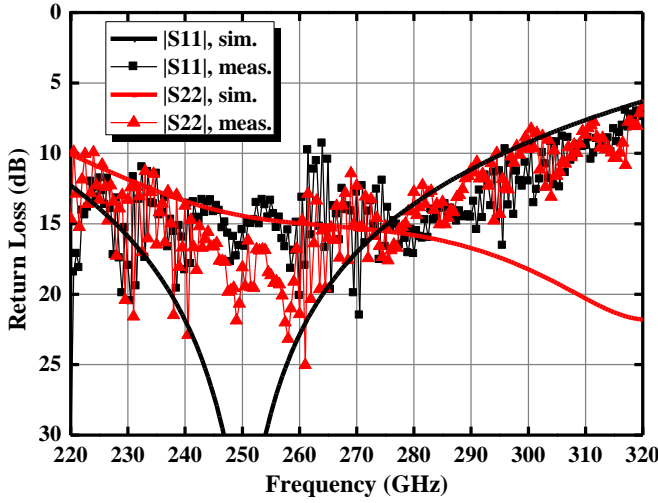


Fig. 5: Return losses from 220 to 320 GHz.

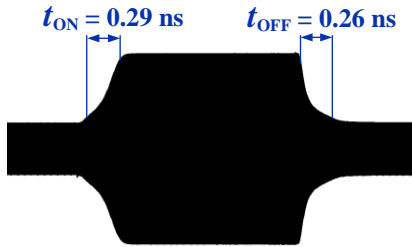


Fig. 6: Simulated switching speed performance.

loss that is 0.5-0.7 dB for each pad at 250 GHz is included in the insertion loss measurements.

Fig. 4 shows that the measured insertion loss and isolation performance are in a good agreement with simulated ones. The measured switch has a minimum insertion loss of 4.2 dB at 250 GHz, including the pad losses of 1.0-1.4 dB. The insertion loss curve is flat with value less than 5 dB from 220 to 285 GHz. The measured isolation curve is also flat with value around 18 dB. The simulated isolation between Port 2 and Port 3 is better than 18 dB. Thus, the switch has ON/OFF ratio of better than 13 dB that satisfies the terahertz imaging

requirements [4].

Fig. 5 shows the return losses that are better than 10 dB from 220 to 300 GHz. The simulated switching ON and OFF times are 0.29 ns and 0.26 ns respectively as shown in Fig. 6, which could support Gb/s modulation and short-pulsed active radar applications. Our measurement setup has maximum output power from extension module of less than -10 dBm that is well below the  $P_{1dB}$  of tested switch. The simulated output  $P_{1dB}$  is 9.2 dBm at 260 GHz.

#### IV. COMPARISON AND SUMMARY

Table I shows the performance comparison of this work with the state of the art. The proposed switch features insertion loss of 4.2 dB and isolation of 19 dB that are comparable to other works. However, it achieves the highest operating frequency and smallest chip size (in terms of both  $mm^2$  and  $\lambda_0^2$  where  $\lambda_0$  is the free space wavelength at center operating frequency) among SPDT switches operating beyond 100 GHz in silicon technologies.

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