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Novel Q-factor Enhancement Technique for On-chip Spiral Inductors and Its Application to CMOS Low-Noise Amplifier Designs

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Abstract

In this paper, a novel Q-factor enhancement technique for on-chip spiral inductors is presented. Symmetric return ground structure in traditional on-chip spiral inductors is modified and shifted towards the side with stronger magnetic field caused by asymmetrical windings of inductors. In full-wave electro-magnetic simulation, it is observed that by applying this technique, inductor with higher Q-factor and larger inductance is obtained with no cost of additional chip area. Using the proposed technique, on-chip inductors are customized for a three-stage cascode low-noise amplifier design. Fabricated in a commercial 65-nm CMOS process, the low-noise amplifier features peak gain of 26.3dB, 21.8mW power consumption, noise figure of 5.3dB, output P_{1dB} of -4dBm, and core size of 0.15mm². In the comparison with prior arts, the proposed design achieves the highest gain and figure-of-merit.

Index Terms

CMOS integrated circuits, low-noise amplifier, millimeter-wave integrated circuits, on-chip inductor, and quality factor.

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I. INTRODUCTION

Recently, millimeter-wave (mm-wave) integrated circuit designs have gradually migrated to silicon platform for applications that require small form-factor, low power consumption and high level of integrations [1, 2]. To implement high performance circuits, it is crucial to design accurate and optimized passive components, especially the on-chip spiral inductors which are widely used in mm-wave circuits. In the literature, techniques for modelling, characterization and design of these on-chip inductors were reported in [3, 4].

In this work, we present a novel Q-factor enhancement technique for on-chip inductors, which are investigated using full-wave electro-magnetic (EM) simulations. Using the proposed inductors, a 60GHz low-noise amplifier (LNA) in 65nm CMOS is designed and achieves the state-of-the-art performance in experiments.

II. Q-FACTOR ENHANCED INDUCTORS

In Fig. 1(a), the 1.5-turns inductor is firstly designed and optimized by using the full-wave EM simulator ANSYS HFSS V.15, for the inductance requirements with the optimized Q-factor by controlling the outer-diameter, trace width, trace spacing, and size of surrounding ground plane [3, 4]. For this inductor, its ground structure is symmetric with respect to XX' axis. Thus, the inductor itself is asymmetrical due to the 1.5-turns nature, and has stronger EM field and return current at its upper side where two windings are presented.

In Fig. 1(b), the ground structure is shifted towards upper side and retains the symmetry of field distribution. In Fig. 2, traditional and proposed inductors are compared with

$$Offset = r_U - r_L. \quad (1)$$

It is observed that after shifting the ground plane by $2\mu\text{m}$, the inductor has Q-factor enhanced by 0.55, and inductance of 1% higher at 60GHz.

III. LNA DESIGN AND IMPLEMENTATION

To utilize the proposed inductor in mm-wave circuits, a 60GHz LNA is designed and implemented based on GlobalFoundries 65-nm 1P9M Lower-Power CMOS technology.

Fig. 3 shows the schematic of the proposed circuit. The LNA is in three-stage cascode topology for the stability consideration, while the matching networks are realized majorly by spiral inductors on the thick metal layer and inter-digital capacitors, and minimized length of transmission lines for interconnections only. The input and output are designed to match to 50Ω . Further, only small inductors ($<150\text{pH}$) are used as they have better Q-factors. The circuit design is completed by HFSS for full chip EM simulation and Cadence for co-simulation. In Fig. 4, the micrograph of fabricated LNA is shown. The circuit has a core chip area of $0.26\text{mm} \times 0.5\text{mm}$.

IV. EXPERIMENTAL RESULTS

The probe-based measurements are performed using Agilent N5247A PNA-X network analyzer and Cascade Elite 300 probe station. The three gate biasing voltages are at 0.83V, 0.8V and 0.81V respectively, while supply voltage VDD is 1.8 V.

In Fig. 5, the simulated and measured power gain are compared, which agree very well with $<1\text{dB}$ discrepancy from 55 to 65GHz. The measured gain has a peak value of 26.3dB at 59.7GHz with 3-dB bandwidth of 56.8 to 62.8GHz. The input and output return losses are better than 10dB from 57 to 64GHz.

In Fig. 6, the noise figure and power performance are illustrated. The measurement of NF is still undergoing. The simulated noise figure is <5.5dB across the 3-dB bandwidth, with minimum value of 5.3dB at 58.7GHz. The measured output P1dB is -4 dBm in average.

The performance summary of the proposed LNA, and a comparison with other state-of-the-art CMOS LNAs in the 60GHz band, are shown in Table I. The LNA described in this paper achieves the highest power gain and the best FoM of 23.7 as defined in [5]

$$\text{FoM}(\text{GHz} \times \text{mW}^{-1}) = \frac{\text{Gain}(\text{abs}) \times f_c (\text{GHz})}{(\text{NF}(\text{abs}) - 1) \times P_{\text{DC}}(\text{mW})}. \quad (2)$$

V. CONCLUSION

A novel Q-factor enhancement technique for on-chip spiral inductors was presented, where the symmetric return ground structure in traditional on-chip spiral inductors was modified and shifted towards the side with stronger magnetic field. In full-wave electro-magnetic simulation, it is observed that by applying this technique, inductor with higher Q-factor and larger inductance can be obtained with no cost of additional chip area. Using the proposed inductors, a 60GHz low-noise amplifier (LNA) in 65nm CMOS was designed and achieved the state-of-the-art performance in experiments.

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Fig. 1. Customized 1.5-turn inductor in commercial 65-nm CMOS: (a) Traditional inductor with symmetric return ground structure; (b) Proposed inductor with asymmetric return ground structure.

Fig. 2. EM simulations of the traditional and proposed inductors.

Fig. 3. Schematic of the 60GHz LNA.

Fig. 4. Micrograph of the chip die.

Fig. 5. S-parameters of the 60GHz LNA.

Fig. 6. Noise figure and power performance of the 60GHz LNA.

Table 1: Performance comparison of state-of-the-art 60-GHz LNAs

Ref.	ISSCC '08 [7]	MWCL '11 [6]	TMTT '13 [5]		This Work
Tech.	CMOS 65- nm	CMOS 65- nm	CMOS 65-nm		CMOS 65- nm
Freq. (GHz)	59.3	61.2	58.5	58	59.8
G_{MAX} (dB)	19.3	18.9	16.5	17.5	26.3
BW (GHz)	7.7	12	4.5	7	6
$ S_{11} $ (dB)	-12	9.3	-20	-15	-10
$ S_{22} $ (dB)	-	13.9	-	-	-12
NF (dB)	6.1	6.06	6.6	5.3	5.3(sim.)
P_{1dB} (dBm)	-2.1	-4.4	-	-	4
P_{DC} (mW)	35	45	27.9	18	21.8
Area (mm ²)	0.21	0.25	0.37	0.51	0.15
FoM (GHz×mW ⁻¹)	5.1	3.9	3.9	10.1	23.7