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Thermal Management of Hotspots with Micro-Jet Based Hybrid Heat Sink for GaN-on-Si Device

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and Kok Fah Choo**

Abstract— The direct-die-attached cooling solution with diamond heat spreader and hybrid Si heat sink has been developed for hotspot cooling of GaN-on-Si device. The hybrid heat sink combines the benefits of micro-channel flow and micro-jet impingement. In the fabricated test chip, the small hotspot is used to represent one unit of transistor. Experimental tests have been implemented on the fabricated test vehicle to investigate the thermal and fluidic performances. Two types of simulation models have been constructed in COMSOL, considering the multi-physics features and temperature dependent material properties. The sub-model in conjunction with the main model is constructed to predict the thermal performance of the GaN-on-Si structure. Various heating powers 10~150W are loaded on 8 tiny hotspots of size 450×300μm (heat flux on each hotspot 0.93~13.89kW/cm²). The spatially averaged heat transfer coefficient of 11.53×10⁴W/m²K has been achieved in the jet-based hybrid heat sink. Consistent results from the experimental and simulation studies have verified the high heat dissipation capability of the designed cooling solution. Several simulations have been conducted to investigate the effects of the structure and dimension on the performances for hotspot thermal management.

Index Terms-- Electronic cooling, Micro-jet impingement, Micro-channel heat sink, Heat dissipation capability, Hotspot, High electron mobility transistor (HEMT).

I . INRODUCTION

The development of the modern electric devices, including shrinking feature sizes, incorporating more functions, and faster circuit speeds, is leading to significant increases in the packaging densities and heat fluxes. Effective thermal management will be the key to ensure that these devices perform well with efficiency and reliability [1]. The problem of heat removal is likely to become more severe

due to the presence of hotspot, which could lead to much higher heat flux than the average over the entire chip and make the temperature distribution highly non-uniform, thus diminishing the device performance and adversely impacting reliability [2]. As the heat dissipation concentrates on tiny gate fingers, the operation of GaN high electron mobility transistor (HEMT) posts huge challenge to thermal management. J.P. Calame [3] performed experimental investigations on the GaN-on-SiC amplifiers, and $4\text{kW}/\text{cm}^2$ heat flux was located on a $1.2\times 5\text{mm}^2$ active area of the $5\times 5\text{mm}^2$ die. Y.J. Lee [4] developed a Cu micro-channel heat sink for GaN-on-Si device, and more than $10\text{kW}/\text{cm}^2$ heat flux was concentrated on eight hotspots (each size $350\times 150\mu\text{m}^2$) of a $7\times 7\text{mm}^2$ Si die. The hotspot removal was also analyzed by V. Sahu [5], and a $500\times 500\mu\text{m}^2$ hotspot area of a $1\times 1\text{cm}^2$ die was considered, and more than $1\text{kW}/\text{cm}^2$ could be dissipated.

Both micro-channel and micro-jet heat sinks can dissipate high heat fluxes anticipated in high power electronic devices [6]. Liquid jet impingement can provide high heat transfer coefficient, when arranged in arrays. Compared with impinging micro-jet, the micro-channel has a lower averaged heat transfer coefficient. However, the coolant can exchange energy with a larger effective surface area with multiple walls within each of the channels. E.G. Colgan [7] presented a Si micro-channel cooler and optimized cooler fin for cooling very high power chip, and $300\text{W}/\text{cm}^2$ uniform heat flux was dissipated. Fabbri and Dhir studied single-phase heat transfer of impinging jet arrays with three different circular array patterns [8]. Laser drilling was used to create 10 arrays with diameters ranging from 69 to $250\mu\text{m}$. The heat transfer coefficients reported were $0.6\sim 6\times 10^4\text{W}/\text{m}^2\text{K}$. Brunswiler [9] created a series of micro-jet arrays with branched hierarchical parallel fluid delivery and return architectures. The peak heat transfer coefficient measured was $8.7\times 10^4\text{W}/\text{m}^2\text{K}$. M.K. Sung [10] combined the micro-channel and jet impingement, and their copper heat sink facilitated the dissipation of $304.9\text{W}/\text{cm}^2$. To reduce the thermal resistances through the key thermal path, the cooling solution directly attached to the chip was proposed [11]. J. P. Calame [3] conducted experimental investigation on the direct-die-attached micro-channel heat sink. A maximum heat flux of $1.5\text{kW}/\text{cm}^2$ was dissipated

on a SiC chip with $3 \times 5 \text{ mm}^2$ resistive zone as heat source. A cooling solution of high thermal conductivity will be required to dissipate the concentrated high heat flux in the chip [12]. The heat spreader tends to be a significant mass in the heat sink [13-15]. CVD diamond, of thermal conductivity five times higher than Cu, can be utilized as the heat spreader for microelectronic cooling [16, 17]. A. Rogacs [18] conducted the numerical simulation to evaluate the thermal effect of the diamond heat spreader for a small heat source.

Fig.1 Schematic image of the cooling structure from top view and bottom view, and layout of the hybrid heat sink.

In this study, the cooling solution directly attached to the Si test chip has been developed and evaluated for hotspot cooling. The hybrid Si heat sink combines the micro-channel flow and micro-jet impingement array. With large concentrated heat fluxes in the test chip, diamond heat spreader is adopted to help to remove the heat to the beneath heat sink. The Si chip, diamond heat spreader and the Si heat sink are assembled together as is shown in Fig.1. The hotspot (resistor) of tiny area is used to represent the gate finger heating area of the GaN transistor. Two types of simulation models, main model of hotspot heating and sub-model of gate finger heating, have been built to investigate the thermal performance. The simulation results show great agreement with the experimental results. The sub-model is used in conjunction with the main model to predict the peak temperature of the transistors under the gate areas. Large heat transfer coefficient of the hybrid heat sink has been obtained, and high

heat dissipation capability can be achieved by the directly attached cooling solution for the GaN-on-Si device. Several further simulations have been conducted to investigate the effects of the structure and dimension on the performances of the cooling structure for hotspot thermal management.

II. EXPERIMENTS

A top view of the typical GaN-on-Si power amplifier (PA) is shown schematically in Fig.2. There are 8 GaN transistors in this configuration, and each transistor is composed of 10 gate fingers of gate width W_G , gate length L_G and gate-to-gate pitch P_G . The HEMT structure, which is magnified in the inset of the Fig.2, consists of source (S), drain (D) and gate (G). During operation, the vast majority of the waste heat in the GaN PA is generated in the portion of each conductive channel that lies directly beneath the gate finger. The Si substrate chip is considered in this study, and 8 GaN transistors cover 8 rectangular active regions on top of the die.

Fig.2 Simplified layout of the GaN-on-Si power amplifier

The experimental tests have been implemented on the Si thermal test chip of $7 \times 7 \text{ mm}^2$ size and $100 \mu\text{m}$ thickness with 8 hotspots evenly located in line, as is illustrated in Fig.2. The size of each hotspot is $450 \times 300 \mu\text{m}^2$, which is a good approximation of an area of 10 gate fingers with $300 \mu\text{m}$ W_G , $0.3 \mu\text{m}$ L_G and $45 \mu\text{m}$ P_G . The space between each hotspot is set to be the same as those of the transistor banks of the GaN-on-Si device, which is $690 \mu\text{m}$. The highly doped N-type resistors are built on the thermal test chip as the hotspot heaters. The resistors are fabricated through a series of

photolithography, etch and implantation processes. The resistivity measurement of the finished wafers shows good consistency within wafer and between wafers. B. L. Lau [19] provided more details on the customized thermal test chip fabrication processes. The diamond heat spreader, which is prepared by Microwave Plasma Chemical Vapor Deposition (MPCVD), is adopted to handle the high concentrated heat flux. For tight bonding with the test chip and the heat sink, the diamond heat spreader is metalized with thin Ti/Pt/Au layer (total thickness around $1\mu\text{m}$). The heat spreader is of the similar size to the test chip and $300\mu\text{m}$ thick. The thermal conductivity of the diamond heat spreader at room temperature is larger than 1800W/mK , and may drop to around 1000W/mK at 200°C . The Si hybrid heat sink is fabricated by bonding two Si plates together, one is with multiple micro-channels (18 channels), and the other is with micro-jet arrays (14×18 nozzles). The micro-channels or micro-jets are etched on the 8-inch wafers with the deep reactive ion etching (DRIE) process. After etching, these two kinds of wafers (one with channels, the other with nozzles) are back-grinded to each designed thickness. Then, one side of each wafer is metalized with AuSn solder, which is of $4\mu\text{m}$ thickness and deposited by evaporation. After the solder layer formation, these wafers are diced into single plate, then chip-level bonding is conducted to bond the micro-channel plate and the micro-jet plate together. The bonding is carried out through thermal compression bonding (TCB) process, in which the 280°C chuck holding time is 2 minutes and the compressive force is 5kgF . The fabricated hybrid Si heat sink is illustrated in Fig.3 and 4.

Fig.3 Cross-section images of (a) the fabricated micro-channel, (b) the fabricated micro-jet, and (c) the bonded hybrid heat sink

Fig.4 X-ray transparent image of the bonded Si heat sink

After the heat sink fabrication, the outside surfaces of the bonded two sets of Si plates are metalized for the die-to-heat spreader-to-heat sink attachment. The chip-level bonding process is conducted in the same TCB process. The bonded interfaces are illustrated in Fig.5.

Fig.5 Cross-section image of the bonded interfaces

Fig.6. Image of the assembled test vehicle

Then, the thermal test chip was wire bonded to the PCB, as is shown in Fig.6. The power input to the heaters on the test chip is controlled by a DC power supplier. The experimental apparatus is illustrated in Fig.7. Water, as the coolant, from a reservoir tank is driven through the flow loop using a micro-gear pump. The inlet water and ambient temperature is around 25°C. This pump forces the water through a 15 μ m filter and a flow meter before entering the micro-channel heat sink. The differential pressure transmitter is attached to the manifold to measure the pressure drop. The test chip temperature at steady state is measured and recorded using the infrared (IR) camera.

Fig.7. Image of (a) experimental test setup and (b) measurement setup using IR camera.

III. SIMULATIONS

Two types of simulation models are constructed using COMSOL Multi-physics, which runs the finite element analysis together with adaptive meshing and error control. The built-in fluid flow and heat transfer interfaces are used in the main model, which couples both solid and fluid part. Due to the symmetries in the system, a quarter of the thermal structure with symmetrical boundary conditions is constructed to investigate the thermal and fluidic performance, as is illustrated in Fig.8. The solution was tested for mesh independency by refining the mesh size. Velocities and temperatures matched within 0.1% for both mesh sizes. The convergence criterion of the solutions is 10^{-6} . The viscous heating feature is considered in the heat transfer interface. The no slip boundary condition is applied for the stationary wall. The main model consists of around 2 million tetrahedral elements. The element size of the fluid part is calibrated for fluid dynamics, while that of the solid part is calibrated for general physics. High heat fluxes are loaded only on the hotspots.

Fig.8 Image of the main model (the fluid part is in blue color) with symmetry boundaries, and the finite element mesh.

As to the GaN transistor, the heat producing regions under the gate fingers are much smaller than the chip, which makes it impractical to perform a single detailed simulation of the entire test chip. A sub-model has been constructed to predict the thermal performance of the actual GaN-on-Si device. One GaN transistor, which is represented by one hotspot in the main model, is considered in the sub-

model, consisting of 10 gate fingers, and each gate finger is of the size of $300 \times 0.3 \mu\text{m}^2$. Once the thermal and fluidic performances are computed in the main model, a sub-model is used to compute the peak temperature of the GaN transistor. For thermal studies, a number of assumptions were made to limit the scope of the investigation. In the sub-model, the active area of one gate is fixed at $300 \times 0.3 \mu\text{m}^2$, and all 10 gate fingers in one unit are built considering the heating influences of the nearby gates. The spatially averaged heat transfer coefficients obtained from the main model will be applied to the sub-model as the convective cooling boundaries. Half structure including one transistor with symmetry boundaries is constructed as is shown in Fig.9. Only the solid parts are considered, and heat transfer coefficient obtained from the main model is applied on the walls of the heat sink channel. The model consists of around 1.4 million tetrahedral elements respectively. The element size is calibrated for general physics.

Fig.9 Image of the sub-model with symmetry boundaries, and the finite element mesh.

IV. RESULTS AND DISCUSSION

The experimental tests are carried out by heating 8 hotspots simultaneously with 10W~150W total power (heat flux on each hotspot: $0.93 \text{ kW/cm}^2 \sim 13.89 \text{ kW/cm}^2$), at the ambient and inlet temperature around 25°C . The flow rate of the water across the hybrid heat sink and the pressure drop between inlet and outlet were recorded in the test, as is illustrated in Fig.10. Based on the estimated low Reynolds

number in the heat sink with the current flow rate, it is considered to be operated in laminar regime. The steady-state simulation is performed on the main model.

Fig.10 Pressure drop as a function of the flow rate in the heat sink from the test and simulation

In the designed hybrid heat sink, to maintain the flow rate of 400mL/min and 600mL/min, the pressure of 30kPa and 60kPa are required respectively. The loading and environment conditions in the multi-physics simulation are set according to the experimental tests, and temperature dependent material properties are considered. The thermal performance in the experimental test and simulation are compared in Fig.11 and 12. The flow rate is set to be 400mL/min in the test.

Fig.11 Maximum hotspot temperature as a function of the heating power from the test and simulation

Fig.12 Comparison of the temperature across the hotspots between test and simulation for different heating power

As is illustrated in Fig.11, excellent agreement has been obtained between experimental results and simulation results. The maximum temperature happens at the hotspot located near the chip center. The designed hybrid heat sink can dissipate around 50W heating power ($4.63\text{kW}/\text{cm}^2$ heat flux on hotspot), 100W ($9.26\text{kW}/\text{cm}^2$) and 120W ($11.11\text{kW}/\text{cm}^2$), while respectively maintaining the maximum hotspot temperature under 85°C , 160°C and 200°C . The maximum heating power loaded in the experiments is 150W ($13.89\text{kW}/\text{cm}^2$ on hotspot), and the hotspot temperature reaches as high as 250°C . The temperature profiles in the longitudinal direction across all hotspots are illustrated in Fig.12. For 50W, 100W and 150W, there is a temperature difference of about 3°C , 7°C and 12°C respectively between the hotspots located near the centre and near the edge of the test chip. The results seen in Fig.11 and 12 show that, the performances can be accurately simulated using the main model. Further investigations have been conducted based on the simulation results, as is shown in Fig.13.

Fig.13 Images of (a) stream line distribution (the color represents temperature), and (b) local heat transfer coefficient distribution in the heat sink under the center hotspot for 150W

When flooded with moving water, the top micro-channel will create the submerged and confined micro-jet condition. The jet impinging will occur with the input driving pressure. For total heating power of 150W, the maximum fluid temperature is around 70°C. The impinging flow has a strong vorticity near the upside impingement plate and that the vorticity weakens away from the impinging plate. The heat transfer coefficient in the heat sink is calculated using the equation $h = Q_w / (T_w - T_{in})$, in which Q_w is the heat flux, T_w is the channel wall temperature and T_{in} is the inlet water temperature. In this study, the spatially averaged heat transfer coefficient at the top impingement wall in the channel is as high as $11.53 \times 10^4 \text{W/m}^2\text{K}$. The local heat transfer coefficient is quite large in the stagnation zone, which can be larger than $100 \times 10^4 \text{W/m}^2\text{K}$, and the cooling performance drops rapidly away from the impingement zone, as is illustrated in Fig.13 (b). The value of the averaged heat transfer coefficient is validated by applying it back into the main model shown in Fig.8 without considering the fluid parts. For sub-model simulation, the convective boundaries are applied inside the channels of the heat sink. The heating power is loaded on the tiny gate finger area, and the steady-state analysis is performed. The results of the sub-model simulation are shown in Fig.14, which gives the temperature distribution across all gate fingers, compared with the representative hotspot of the main model.

Fig.14 Temperature profile in the longitudinal direction across 10 gate fingers and 1 hotspot for different total power

As is illustrated in Fig.14, the maximum temperature of the gate finger is quite higher than that of the hotspot. The heat flux on each gate finger area is extremely high in the sub-model analysis. For total power of 100W, each GaN transistor will dissipate 12.5W power, and the heat flux on each gate will be as high as $1.39\text{MW}/\text{cm}^2$. The designed cooling solution can dissipate 50W and 100W total power, while maintaining the maximum gate temperature under 105°C and 220°C respectively.

V. THERMAL EFFECT ANALYSIS

The designed cooling solution combines three key parts: diamond heat spreader, multiple micro-channels and micro-jet impingement array. The heat flux on tiny hotspots of the test chip is quite high, which is difficult for the liquid-cooled Si heat sink to handle. The diamond heat spreader of high in-plane heat conductivity can enhance the cooling performance by effectively spreading the concentrated heat flux. The effect of the diamond heat spreader is investigated by performing the simulations on the model with and without it. For 100W power heating (heat flux on each hotspot $9.26\text{kW}/\text{cm}^2$), the maximum heat flux on top surface of the Si heat sink for the model with and without diamond heat spreader is $1.03\text{kW}/\text{cm}^2$ and $4.98\text{kW}/\text{cm}^2$ respectively. The diamond heat spreader can enable much smaller and more uniform heat flux for the liquid-cooled heat sink to handle. In this 100W case, with 400mL/min flow rate in the heat sink, the maximum hotspot temperature is around 155.66°C and 252.98°C respectively for the structure with and without diamond heat spreader, suggesting that the diamond heat spreader plays quite a significant role in cooling the tiny hotspot.

The comparison of the performance has been made among the micro-channel heat sink (MCHS), micro-jet heat sink (MJHS) and the hybrid heat sink. The dimensions of the channels in MCHS and the nozzles in MJHS are the same as the hybrid heat sink. The flow rates in these three types of heat sink are all set to be 400mL/min. The increasing heating power has been loaded on the 8 hotspots. The simulation results are illustrated in Fig.15.

Fig.15 Maximum hotspot temperature as a function of the total power for three types of liquid-cooled heat sink

As can be observed in Fig.15, the hybrid heat sink exhibits the best cooling performance among the studied three types. With the same heating power, compared with the MCHS and the MJHS, the hybrid heat sink can reduce the maximum temperature by around 20% and 5% respectively. For these three heat sinks with current flow rate, the pressure drop in the MCHS is the highest (about 42.7kPa), while that in MJHS is 26.0kPa and in hybrid heat sink is 32.5kPa. The hybrid heat sink enables better cooling performance by combining the micro-channel and micro-jet impingement together. In the current design, the micro-channels are of 250 μ m channel width (W_{mc}) and 100 μ m fin thickness (L_{mc}), and the micro-jet array is of 100 μ m nozzle diameter (D_j) and 350 μ m pitch (P_{jx} , P_{jy}). The ratio α , which is defined as $\alpha = W_{mc}/D_j$, is 2.5 in this case. Parametric simulations have been conducted to study the effect of α on the performance of the hybrid heat sink. The results are shown in Fig.16.

The dimensions of the micro-jet array are maintained constant as above. The thermal resistance of the heat sink is calculated based on the maximum heat sink temperature and the total heating power. As is shown in Fig.16, the thermal resistance decreases first, and then increases with the increase of the ratio α , which is resulted by the combined effect of heat convection and conduction. When the value of α is around 2.5, the smallest thermal resistance can be achieved for the hybrid heat sink. With the constant pressure and increasing, the flow rate in the heat sink and the flow velocity in the nozzle will increase., but the heat conduction through the sidewall is weakened due to the reduced fin thickness.

When the value of α is doubled from 1.5 to 3, the flow rate increases by around 24%, and fin thickness decreases from 100 μm to 50 μm . The jet-to-wall distance is an important factor affecting the jet impingement profile in the top channel. Several simulations have been implemented on the jet array structure of different distances, while the other dimensions are kept constant. The results obtained are similar to the reported results about the jet array impingement [20, 21]. The maximum heat transfer occurs at a certain distance for different volume flow rate. In our exact case, for 400mL/min flow rate, the largest heat transfer coefficient is obtained when the jet-to-wall distance is $2.5D_j$, and for 500mL/min, the best distance is $3D_j$.

Fig.16 Effect of the combination ratio α on the performance of the hybrid heat sink with difference pressure

The effect of the micro-jet diameter on the thermal performance of the heat sink is investigated with various driving pressure. The jet array structure with nozzle diameter of 80 μm , 100 μm and 120 μm are considered in this case. The other dimensions of the micro-channels and micro-jets are assumed to be the same as is shown in Fig.3. With the same pressure drop, the volume flow rate in the heat sink of smaller nozzle diameter will be smaller than that in the one of larger diameter. With the same ratio α , the larger diameter will result in smaller fin thickness L_{mc} . It can be observed in Fig.17 that, with the same pressure drop, the thermal performance of the heat sink can be improved by increasing the nozzle diameter. The effect is more sensitive by increasing the diameter from 80 μm to 100 μm , where the thermal resistance can be reduced by 10%~20%. By increasing the nozzle diameter from 100 μm to

120 μm , only slightly improvement can be achieved, which is resulted by the combined effect of the increased heat transfer coefficient and the weakened heat conduction through the fin. As to the same flow rate, higher pressure drop will be required for the array of smaller nozzle diameter, which will result in high flow velocity from the exit of the jet. Although the jet velocity is low for the jet of larger diameter, larger stagnation zone can be achieved for better heat convection. With 400mL/min flow rate in our case, for the jet array of 100 μm diameter the thermal resistance is 5.8% smaller than that for 80 μm , and 7.4% smaller than that for 120 μm . The pressure drop required is much larger for jet of 80 μm , which is around 1 time and 3 times larger than that for 100 μm and 120 μm respectively.

Fig.17 Thermal resistance and the heat transfer coefficient as a function of the pressure drop for the micro-jet array of different nozzle diameters

By decreasing the nozzle pitch, more micro-jets can be involved in the cooling area covered by the hybrid heat sink (5×5mm²). To investigate this influence, the y-direction pitch P_{jy} (along the micro-channel) is decreased from $3.5D_j$ to $2.5D_j$, and then number of the nozzle in each row can be increased from 14 to 18. The micro-jets are still evenly located in 18 columns in x-direction (across the micro-channels). The thermal performance and flow motion in the hybrid heat sink are evaluated with the constant flow rate 400mL/min. To obtain this flow rate, the pressure drop required in array (a) and (b) is 30kPa and 28kPa respectively. Several micro-jets of $P_{jy} = 2.5D_j$ under the center hotspot are illustrated in Fig.18, compared with the micro-jets of $P_{jy} = 3.5D_j$.

Fig.18 Thermal performance and flow motion of the micro-jet array of (a) $P_{jy} = 3.5D_j$, 14×18 , and (b) $P_{jy} = 2.5D_j$, 18×18 .

(The color of the flow stream line represents the fluid temperature.)

With 100W heating power, the maximum hotspot temperature for micro-jet array (a) is 155.6°C, while that for array (b) is 153.4°C. The heat dissipation capability of the heat sink can be slightly improved by using the array of smaller pitch and more nozzles. With the decreased pitch, the flow motion of the jet might be negatively affected by the adjacent jets, which results in 35.3% decrease of the maximum local heat transfer coefficient, but more micro-jets can be located near the main hotspot heating area, which can enable 15.7% increase of the spatially averaged heat transfer coefficient.

V. CONCLUSIONS

The direct-die-attached cooling solution with diamond heat spreader and hybrid Si heat sink has been developed for hotspot cooling. In the fabricated test chip, a hotspot of size $450 \times 300 \mu\text{m}^2$ is used to represent one GaN transistor of 10 gate fingers. High heat flux, from 0.93 kW/cm^2 to 13.89 kW/cm^2 , is concentrated on the heater area in the thermal test chip. The hybrid Si heat sink combines the micro-channel flow and the micro-jet array impingement, and are fabricated with DRIE process and bonded through TCB process. High heat dissipation capability of the direct-die-attached structure for hotspot

cooling has been verified by performing experiments and simulations. The sub-model approach has been used to predict the thermal performance of the GaN-on-Si device. With the flow rate of 400mL/min and the pressure drop of 30kPa, high concentrated heat flux on the Si thermal chip can be dissipated. The spatially averaged heat transfer coefficient of $11.53 \times 10^4 \text{W/m}^2\text{K}$ is yielded, while the maximum local coefficient can be as high as $100 \times 10^4 \text{W/m}^2\text{K}$. The cooling effects of the heat spreader, multiple micro-channels, and micro-jet array are studied separately. The combination of all these key cooling parts can enable better heat removal capability. The dimension effects of ratio α , jet-to-wall distance, nozzle diameter and nozzle pitch have been investigated. The results obtained in this study are expected to aid the design of the cooling solution for electronic devices with hotspots.

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