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Five-Level Multiple-Pole PWM AC-AC Converters with Reduced Components Count

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Abstract—This paper proposes novel multilevel AC/DC/AC converters with reduced number of semiconductor devices to achieve light weight, efficiency and better input current quality. The proposed three-phase front-end bidirectional five-level (5L) rectifier and rear-end 5L-inverter are constructed based on multiple-pole multilevel diode-clamped approach (M²DCC), which consist a total number of 24 diode components clamped. Based on M²DCC concept, the number of switching devices can be further reduced to construct a new unidirectional front-end rectifier (M²SCR). Comparative studies are conducted to analyze the performances of the two proposed front-end rectifiers with supportive mathematical derivations. Experimental prototypes have proven the feasibility of the proposed AC/DC/AC configurations. Results obtained show that low current harmonic distortions of 5% and high power factor of 0.99 are achieved with small input inductors despite of low switching frequency operation at 1 kHz.

Index Terms— Five-level multiple-pole converter, reduce number of semiconductor devices, transformerless drive.

I. INTRODUCTION

Multilevel AC/DC/AC converters (which consists of front-end rectifier and rear-end inverter) for medium-high power motor drives are widely employed in many industrials. This configuration is favorable for many applications such as heat, ventilation and air conditioning (HVAC) systems, pump/blower/traction drives and even permanent-magnet synchronous generator wind turbine with grid-connected. Due to the advantage of decoupling both front-end source and rear-end load through a dc-link, and simple control techniques can be implemented to achieve optimum performance.

The commonly used 3L AC/DC/AC drives can be configured based on a front-end unidirectional (such as Vienna rectifier) or a bidirectional (3L neutral-point-clamped rectifier) rectifier. Both of these 3L rectifier topologies require

high switching frequency in order to mitigate the input current harmonic distortion. However, the output power efficiency is adversely affected. Besides that, the high insulation stress (large dv/dt and di/dt) produced are harmful for dynamic load applications [2].

Higher n-level (such as 5L and above) AC/DC/AC converter topologies offer an alternative solution to address the implications of high switching frequency operation. These higher n-level converters have the natural ability to achieve better efficiency with lower switching and conduction losses while operating at lower switching frequency [1, 3, 4]. Moreover, simple voltage balancing algorithms in [5-7] for 3L AC/DC/AC converters, as well as power factor correction techniques to achieve low input current distortion in [8-11] can be preserved for higher level PWM converters as well.

Nevertheless, the realizing dc-link capacitor voltages is the greatest problem for higher n-level (with more than 3L output stepped voltage) diode-clamped converters. Thus, it results poorer input and output performance.

This unbalanced condition can be solved with the introduction of a multi-winding transformer connected to multi-pulse diode bridge rectifiers or an additional dc/dc balancing circuit in between front-end rectifier and rear-end inverter. Among the two solutions, an additional dc/dc voltage balancing circuit (in Fig. 1) proposed by N. Hatti *et al.* [12] would be more preferable than implementing a bulky and costly multi-winding transformer.

Many classical configuration of high power transformerless five-level AC/DC/AC drive have been experimented for the motor drive applications in [12-15] by the respective authors, but these would still require significant amount of active components. However, the future development of multilevel converters involves in reducing the overall cost and size needed [1, 3].

The 5L AC/DC/AC drives based on proposed multiple-pole multilevel diode-clamped converter (M²DCC) approach presented in this paper (Figs. 1 and 3) reduce drastically the number of power diodes required. Good overall performance is also achieved while operating at low switching frequency.

Two proposed combinations of 5L multiple-pole AC/DC/AC drives are the front-end bidirectional (5L-M²DCR in Fig. 1) and unidirectional (5L-M²SCR in Fig. 3) rectifiers connected to the same rear-end (5L-M²DCI in Fig. 1) inverter. To yield a fair analysis, the performances of both the proposed front-end rectifiers with the 5L-M²DCI are evaluated with the proposed power factor correction technique. The experimental

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Fig. 1. Proposed five-level bidirectional AC/DC/AC drive based on multiple-pole multilevel diode-clamped converter (5L-M²DCC) approach.

Fig. 2. Classical front-end five-level bidirectional rectifier (5L-MDCR).

Fig. 3. Proposed front-end five-level unidirectional rectifier (5L-M²SCR).

results obtained along with the verified theoretical analysis have proven the feasibility of the proposed topologies for any AC/DC/AC drive applications.

II. OPERATING PRINCIPLES OF FIVE-LEVEL AC/DC/AC TOPOLOGIES

This section presents the operating principles of three different 5L AC/DC/AC PWM converters based on the classical MDCC and the proposed M²DCC approaches. The derivation of proposed M²DCR and M²SCR topologies are explained in this section, while the proposed M²DCI topology is detailed in [16].

A. Classical Bidirectional Front-End 5L-MDCR with Rear-End 5L-MDCI Topologies

The classical 5L-MDCC AC/DC/AC converter in [4, 12, 13] is a back-to-back (BTB) configuration based on a front-end bidirectional rectifier (Fig. 2) and a rear-end five-level diode-clamped inverter. A total of sixteen IGBTs and twelve

diodes in each phase-leg are required in this topology to synthesize the five-level input and output voltage waveforms.

The five-level voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration as shown in Fig. 4. It can be observed directly that the phase voltage levels are achieved across the point V_a to the neutral point m .

B. Proposed Bidirectional Front-End 5L-M²DCR with Rear-End 5L-M²DCI Topologies

The proposed 5L-M²DCC AC/DC/AC drive presented in Fig. 1 consists of a front-end bidirectional 5L-M²DCR and a rear-end 5L-M²DCI. This BTB topology requires only eight power diodes in each phase-leg to achieve the same input and output quality as the classical 5L-MDCC. However, when the number of cells in this proposed topology increases, a total number of $6(n-3)$ diode components are reduced.

The five-level voltage stepped waveform of M²DCC topology is achieved with the switching positions based on the multiple poles hierarchy as shown in Fig. 5. The proposed 5L-M²DCC topology is configured with two classical 3L-MDCC

Fig. 4. Circuit diagram of per-phase leg single-pole classical 5L-MDCC topology with switching position.

TABLE I
SWITCHING LOGIC FOR RESPECTIVE IGBT IN 5L-M²DCC TOPOLOGY

Vom \ Switch	Vdc/2 (Sector II)	Vdc/4 (Sector I & III)	0 (Sector I, III, IV & VI)	-Vdc/4 (Sector IV & VI)	-Vdc/2 (Sector V)
Sa1, Ta1	1	0	0	0	0
Sa2, Ta2	1	1	0	0	0
Sa3, Ta3	1	1	1	0	0
Sa4, Ta4	1	1	1	1	0
Sa5, Ta5	0	1	1	1	1
Sa6, Ta6	0	0	1	1	1
Sa7, Ta7	0	0	0	1	1
Sa8, Ta8	0	0	0	0	1

1: on and 0: off

cells (Outer cell – Cell 2 and Inner cell – Cell 1) in each phase-leg, which is constructed based on the multiple-pole concepts. Hence, the five-level input and output voltage stepped waveforms are achieved with proposed multiple-poles configuration according to the corresponding switching state listed in Table I.

C. Proposed Unidirectional Front-End 5L-M²SCR with Rear-End 5L-M²DCI Topology

A bidirectional power flow in the front-end rectifier is not required for certain AC/DC/AC drive applications such as propulsion, compressor or any non-regenerative braking system. Thus, a proposed transformerless front-end unidirectional rectifier is re-constructed in Fig. 3 with the arrangement of the semiconductor devices in the bidirectional M²DCR configuration (Fig. 1). Hence, the unidirectional 5L rectifier in Fig. 3 is named as multiple-pole multilevel switch-clamped rectifier (M²SCR) instead.

Each phase-leg of the proposed unidirectional 5L-M²SCR also requires two cells as shown in Fig. 5 to achieve five-level input voltage stepped waveform. The states selection of the top and bottom diodes of a M²SCR is dependent on 1-Sa1 and 1-Sa2 for the outer cell and similarly for the inner cell. Hence, only two switching devices are required in each cell with four series diodes connected to the terminals of the capacitors in the dc-link. In Fig. 3, the two switching devices (Sa3 and Sa4) of the inner cell are connected directly to the neutral-point-clamped of the four dc-link capacitors, while the other two

Fig. 5. Circuit diagram of per-phase leg multiple-pole 5L-M²DCC topology with switching position.

switching devices (Sa1 and Sa2) of the outer cell are clamped to the output terminals of the inner cell. Due to lesser number of switches needed, higher power efficiency is achieved with lesser switching and conduction losses.

D. General Characteristic of Classical and Proposed 5L AC/DC/AC Converters

The front-end rectifier and rear-end inverter of 5L AC/DC/AC drives are operated independently with same level-shifted PWM (LS-PWM). The LS-PWM requires a reference signal and a set of four 1 kHz triangular carriers to achieve the desired switching signals for the respective semiconductor switches.

The switching function of the LS-PWM technique for the 5L rectifiers and inverters is expressed as:

$$\begin{cases} S_{a1}(t) = T_{a1}(t) = 2m_a \sin \omega t - 1 \\ S_{a2}(t) = T_{a2}(t) = 2m_a \sin \omega t \\ S_{a3}(t) = T_{a3}(t) = 2m_a \sin \omega t + 1 \\ S_{a4}(t) = T_{a4}(t) = 2m_a \sin \omega t + 2 \end{cases} \quad (1)$$

where m_a is the ratio of two times the fundamental component of pole voltage to the dc-link voltage.

Under the condition of steady-state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as:

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1} \left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2} \right) \quad (2)$$

where x represents as phase 'a', 'b' and 'c' and n is the number of voltage level. T_{xi} is the switching states of each switching device depicted in the inverter side.

The voltage transfer ratio of the converters system between the dc bus voltage to the input and output voltage are defined as follows:

$$\begin{cases} M_{x,rectifier}(t) = \frac{V_{dc}(t)}{V_{L-L}(t)} & , M_{x,rectifier}(t) > 1 \\ M_{x,inverter}(t) = \frac{2V_{xm}(t)}{V_{dc}(t)} & , M_{x,inverter}(t) \leq 1 \end{cases} \quad (3)$$

Fig. 6. Incremental input and output voltage stepped waveform of a back-to-back AC/DC/AC drive.

Fig. 7. Ripple current versus modulation ratio of rectifier.

$V_{x,L-L}(t)$ is the line-to-line grid voltage and $V_{xm}(t)$ is the output pole voltage referred to the inverter side.

In general, high modulation index ($M_{x,rectifier}(t) > 1$) of the front-end rectifier is required to mitigate the input current distortion and achieve good voltage tracking due to its boosting effect in nature. Meanwhile the rear-end inverter must be operated at the linear region ($M_{x,inverter}(t) < 1$) to prevent any high order harmonic components incurred in the load.

Thus, low switching frequency can be used for a 5L rectifier to achieve better power conversion efficiency [17, 18]. The ripple current is expressed in the following (4) based on the previous equations (2) and (3)

$$\Delta I_{Lx}(t) \approx \frac{k}{L_x f_s} \left\{ \frac{3V_{x,L-L}(t) - 3\sqrt{3}V_{mn}(t)}{3\sqrt{3}} - \frac{M_{x,rectifier}(t)V_{x,L-L}(t)}{(n-1)} \left(\sum_{i=1}^{n-1} S_{xi,d} - \frac{n-1}{2} \right) \right\} \quad (4)$$

f_s is the switching frequency of the rectifier circuit and $V_{mn}(t)$ is the virtual ground voltage referred from node m to node n in Fig. 1. $S_{xi,d}$ is the switching transition with respect to the respective sector in Fig. 6. k is the duty ratio of switching transition (Fig. 6) and this is expressed as:

$$\begin{cases} 0 \leq [k = 2 \sin \omega t] \leq 1 & 0 \leq \omega t \leq \pi/6 \\ 0 \leq [k = 2(\sin \omega t - 1/2)] \leq 1 & \pi/6 \leq \omega t \leq \pi/2 \end{cases} \quad (5)$$

Fig. 8. Average current stress level for each devices of the respective front-end rectifier topologies.

The critical input inductance value for front-end 5L-M²DCR can be estimated with the duty cycle and the switching states with respect to the sectors shown in Fig. 6. According to (4), the maximum peak value of the input ripple current is determined at $\omega t = 30^\circ$ as shown in Fig. 7. Thus, the critical inductance value is estimated as follows:

$$L_{x,max} \approx \frac{4(0.5V_{xn} - V_{mn}) - V_{dc}}{4\Delta I_{Lx} f_s} \quad (6)$$

V_{xn} is the peak value of the grid phase voltage.

The minimum capacitance value in the dc-link can be estimated in (7) with the change of ampere-second ($\Delta A_{cap,sec}$) and the switching state T_{a1} of the rear-end side. The expression of $\Delta A_{cap,sec}$ is obtained by subtracting the peak value of the grid phase current with the average input current of the converter. Assume all the dc-link capacitors are equal to C . Then,

$$C \approx \frac{4\Delta A_{cap,sec}}{\Delta V_{cap}} = \frac{4T_{a1}(I_a - I_{inv(avg)})}{\epsilon V_{dc} F_s} \quad (7)$$

ϵ is the percentage value of the permissible ripple voltage content and $I_{inv(avg)}$ is the average input current value of the rear-end 5L-inverter. By expanding the expression of (7), the final capacitance value is expressed as:

$$C \approx \frac{4\sqrt{2}I_{rms}(2m-1) \left[\cos \theta - \frac{3}{\pi} \left\{ \left(\frac{1}{2} - \frac{3m}{4} \right) \sin \theta + \left[\left(\frac{\sqrt{3}}{4} + \frac{\pi}{3} \right) m - \frac{\sqrt{3}}{2} \right] \cos \theta \right\} \right]}{\epsilon V_{dc} F_s} \quad (8)$$

where I_{rms} is the root-mean-square value of the grid current and θ is the power factor angle between the grid phase voltage and current.

Fig. 9. Harmonic current distortion characteristics of the respective front-end 5L-rectifiers. (a) Unidirectional 5L-M²SCR and (b) bidirectional 5L-M²DCR.

III. HIGH POWER FACTOR OPERATION OF THREE-PHASE FIVE-LEVEL M²DCR AND M²SCR RECTIFIERS

A. Semiconductors Voltage and Current Stresses

Voltage and current stresses are the dominant factors considered in the converter design, so that the converter can achieve optimum performance with higher reliability. Proper selection of device rating for the proposed front-end rectifiers are determined based on the global stress analysis.

The voltage and current stress expressions for the respective front-end rectifiers are derived with the switching function in equation (1) and based on the following factors: (a) high power factor operation, (b) current and voltage ripple-free, (c) constant switching frequency, (d) balanced dc-link capacitors voltage, and (e) zero voltage dropped across boost inductors (L_x).

The maximum voltage across the power devices of unidirectional 5L-M²SCR and bidirectional 5L-M²DCR are expressed respectively in the following (9) and (10):

$$\begin{cases} V_{Da1} = 3V_{dc}/4 \\ V_{Da4} = V_{Sa1} = 3V_{dc}/8 \\ V_{Da2} = V_{Da3} = V_{Sa2} = V_{dc}/4 \end{cases} \quad (9)$$

$$\begin{cases} V_{Sa1} = 3V_{dc}/4 \\ V_{Sa4} = V_{dc}/2 \\ V_{Sa2} = V_{Sa3} = V_{Da1} = V_{Da2} = V_{dc}/4 \end{cases} \quad (10)$$

Since the maximum voltage stress expressions (9) and (10) are for the power devices in the upper phase-leg, hence the respective complimentary power devices in the lower phase-leg are also determined using the same expressions.

The average current stress is analyzed over one period of the fundamental frequency based on the assumed factors (a) to (e). For simplification, the average current stress is

approximated as follows based on respective switching functions in (1):

$$\begin{aligned} I_{Sa(\text{Outer Cell})}(t) &= I_{Da(\text{Outer Cell})}(t) \\ &= \frac{1}{2\pi} \int_0^{2\pi} I_a \sin(\omega t) S_{a(\text{Outer Cell})} d\omega t \end{aligned} \quad (11)$$

$$\begin{aligned} I_{Sa(\text{Inner Cell})}(t) &= I_{Da(\text{Inner Cell})}(t) \\ &= \frac{1}{2\pi} \int_0^{2\pi} I_a \sin(\omega t) \left[2 - \frac{4V_{am(1)}}{V_{dc}} \sin \omega t \right] S_{a(\text{Inner Cell})} d\omega t \end{aligned}$$

The final average current stress for the respective power devices in the upper phase-leg of the proposed front-end rectifiers are shown in Fig. 8 according to equation (11). It is proved that during the negative cycle of the conduction period, the reverse current through the semiconductor switches in the bidirectional 5L-M²DCR will be cancelled out from the current stress during the positive cycle period. Unlike the case for unidirectional 5L-M²SCR, the current only flows through the diodes during the positive cycle conduction period. Hence, the final net average current stress of 5L-M²DCR in Fig. 8 is found much lower compared to the 5L-M²SCR.

B. Input Current Shaping of 5L-M²DCR and 5L-M²SCR

The performances of the grid current response for the proposed front-end unidirectional and bidirectional rectifiers are shown in Figs. 9(a) and 9(b) respectively. The harmonic current distortions are obtained based on the switching frequency (f_s) and the voltage transfer ratio ($M_{x,\text{rectifier}}$).

Fig. 9 shows that both the proposed front-end rectifiers have high current harmonic distortion when the $M_{x,\text{rectifier}}$ is as low as 1. The current harmonic distortion can be minimized in this case by increasing the switching frequency to 5 kHz and higher.

Fig. 10. Proposed front-end rectifier controller for 5L-AC/DC/AC converter.

TABLE II
NUMBER OF COMPONENTS USED IN THE FRONT-END RECTIFIER TOPOLOGIES

Devices	Topologies				
	Unidirectional Rectifier			Bidirectional Rectifier	
	Classical 5L-MDCR (ref. to Fig. 6 of [1])	Classical 5L-MDCR (ref. to Fig. 7 of [1])	Proposed 5L-M²SCR	Classical 5L-MDCR	Proposed 5L-M²DCR
Diode	24	24	24	18	12
IGBT/MOSFET	18	18	12	24	24
Capacitors	4	4	4	4	4
Complementary Switch	0	9	0	12	12
Isolated Gate Driver	18	18	12	24	24
Cost (USD)	\$7472.72	\$8943.56	\$5698.07	\$6616.08	\$7410.76
Efficiency (%)	77.37	80.44	85.42	80.99	82.30
Weight (kg)	8.01	9.63	6.17	7.14	7.91

TABLE III
MAXIMUM VOLTAGE STRESS LEVEL FOR RESPECTIVE POWER DEVICES UNDER UNBALANCED DC-LINK CAPACITOR VOLTAGES CONDITION

Semiconductor		IGBTs				Diodes			
Topologies		Sa1	Sa2	Sa3	Sa4	Da1	Da2	Da3	Da4
Unidirectional Rectifier	5L-MDCR (ref. to Fig. 6 of [1])	0	$V_{dc}/2$	V_{dc}	V_{dc}	0	$V_{dc}/2$	$V_{dc}/2$	$V_{Da4} < V_{dc}/4$
	5L-MDCR (ref. to Fig. 7 of [1])	$V_{dc}/2$	$V_{dc}/2$	$2V_{dc}$	$2V_{dc}$	0	0	$V_{Da3} < V_{dc}$	$2V_{dc}$
	5L-M²SCR	$V_{Sa1} < V_{dc}/2$	$V_{dc}/2$	$V_{Sa3} < V_{dc}/2$	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{Da4} < V_{dc}/2$
Bidirectional Rectifier	5L-MDCR	$V_{dc}/4$	$V_{dc}/2$	$V_{dc}/2$	$V_{Sa4} < 2V_{dc}$	$V_{dc}/4$	V_{dc}	$2V_{dc}$	$V_{Da4} < 2V_{dc}$
	5L-M²DCR	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{Sa4} < V_{dc}/2$	$V_{Da1} < V_{dc}/2$	$V_{Da2} < V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

However, the grid current distortion does not deviate much with any range of switching frequency utilized when the voltage transfer ratio $M_{x,rectifier}$ is more than 1.3. This can be proved by substituting equations (6) into (4), where the f_s is observed to be cancelled away.

The current harmonic distortion varies non-linearly for the unidirectional 5L-M²SCR in Fig. 9(a), while the results for bidirectional 5L-M²DCR obtained in Fig. 9(b) shows a smoother curve. This is caused by the forward blocking where

the current flows in a single direction from the grid to the dc-link for the 5L-M²SCR.

Even though slight difference is found in the performances, but both proposed front-end rectifiers have met the adopted standard current THD requirements despite of the low switching frequency operation. Hence, these proposed rectifiers can be attractive for high power applications.

Fig. 11. Unity power factor operation with rectifying mode. (a) Voltage and current at the grid side and (b) pole voltage at the rectifier side.

Fig. 12. Unity power factor operation with inverting mode. (a) Voltage and current at the grid side and (b) pole voltage at the rectifier side.

C. Components Count

The number of components count in the front-end rectifiers is listed in Table II. One can observe that the number of the diodes used in the proposed bidirectional rectifier topology is reduced. Hence, it yields a better efficiency due to lower conduction loss. Besides that, the proposed unidirectional rectifier topology also greatly reduces six MOSFET/IGBT devices. Therefore, the required six isolated gate drivers are also eliminated.

The cost, efficiency and weight of the respective converters in the Table II are obtained with the same device ratings for the power semiconductors (Semikron SKM200GB125D) and the diodes (Powerex CN240610) based on a quarter DC-link voltage of a medium voltage 4.4kV drive application. Although the cost and the weight of the proposed bidirectional 5L-M²DCR is slightly higher compared to the classical 5L-MDCR topology, but the efficiency is found to be improved for the proposed bidirectional rectifier.

Moreover, the comparison data in Table II has clearly showed that the proposed unidirectional 5L-M²SCR rectifier topology offers a better cost-to-performance ratio in terms of lowest component cost, highest overall efficiency and lightest weight among the other rectifier topologies. The overall amount of reduction does not only consider the active switches, but also the number of necessary control circuit, as well as the size of the heat sink. The proposed rectifier topologies also greatly reduce the complexity of the control gating signals since lesser isolated power supplies are required.

D. Unbalanced DC-Link Capacitor Voltages

The unbalanced dc-link capacitor voltages may disrupt the smooth operating system and affect the global reliability if the power converter is not adequately designed. This disastrous

Fig. 13. Leading power factor, PF = 0.43. (a) Voltage and current at the grid side and (b) pole voltage at the rectifier side.

Fig. 14. Lagging power factor, PF = 0.43. (a) Voltage and current at the grid side and (b) pole voltage at the rectifier side.

condition will damage the converter by over stressing the limited blocking voltage capability of the semiconductor devices.

Even though this undesirable condition can be resolved typically by disabling the rectifier/inverter operation when any fault condition occurs, but the overall efficiency of the system may be greatly affected. The alternative solution to overcome this issue is to ensure that the power device ratings are properly selected during the design according to the worst case scenarios. Thus, the maximum voltage stress across the respective power devices of the 5L rectifiers are shown in Table III. The obtained results are co-simulated between the PSIM and the MATLAB Simcouple.

It should be noted that the maximum voltage stress across the semiconductor switches in the proposed 5L rectifiers under unbalanced condition are V_{dc} unlike the classical 5L rectifiers will be experiencing $2V_{dc}$ (twice the dc-link voltage). As a result, it is essential to have series-connected switches for the classical 5L rectifiers but these additional switching devices can be avoided for the proposed 5L topologies.

E. Synchronous-Reference-Frame Current Control Scheme

The proposed control algorithm with power factor correction technique is shown in Fig. 10. Two control loops, i.e. Synchronous-Reference-Frame Current Control and Constant Switching Frequency Modulation are implemented to regulate the dc-link voltage and mitigate the current distortions. Due to the simplicity of the control strategy, low cost integrated control circuit can be designed. The balancing control for the dc-dc balancing circuit is presented in [12, 13].

Fig. 15. Experimental waveform of the front-end rectifier performance. (a) Input voltage and current based on front-end 5L-M²SCR configuration, (b) input voltage and current based on front-end 5L-M²DCR configuration, and (c) input current THD of a front-end 5L-M²SCR topology.

Fig. 16. Experimental waveform of the rear-end 5L-M²DCI performance. (a) Output pole voltage, and (b) output line-to-line voltage.

TABLE IV
PARAMETER SETTINGS FOR EXPERIMENTAL AC/DC/AC CONVERTERS

System Parameters	Values
Input Grid Voltage	60 Vrms (50 Hz)
DC-Link Voltage	200 Vdc
Input Inductors (L_x)	5 mH
M_x , inverter	0.8
Switching Frequency	1 kHz

The unity power factor (UPF) controller for the front-end five-level rectifiers (M²DCR or M²SCR) designed in Fig. 10 is based on the synchronous-reference-frame (SRF) current control with the LS-PWM technique. The detailed analysis of the outer-loop dc-link voltage control and inner-loop current control are both presented in [19]. SRF controller provides a good dynamic response to achieve high quality input sinusoidal current with constant unity power factor performance.

The open-loop transfer function of the dc-link voltage control under steady-state condition is written as follows to achieve a stable control system:

$$L(s) = \frac{K_p s + K_I}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{(\sqrt{3} V_p / L_x I_d) - s}{s + (I_{dc} / C_{eq} V_{dc})} \quad (12)$$

K_p and K_I are the PI parameters of the DC voltage control loop selected at 0.4 and 15 respectively. C_{eq} and L_x are the equivalent capacitance of the dc bus and the input (phase 'a', 'b' and 'c') filter inductance with the values of 600 μ F and 5 mH respectively. V_p is the rms value of the grid phase voltage and V_{dc} is the mean value of the dc-link voltage.

As for I_d is the peak value of the reference current which is obtained from the summation of I_{dc} (output of dc voltage control) and feed-forward current (output of K_f). The feed-forward current control loop under steady-state condition is derived based on the power balanced principle, which is expressed in the following:

$$K_f = \frac{V_{dc}}{\sqrt{3} V_p} \quad (13)$$

where V_p is the rms value of the grid phase voltage.

IV. SIMULATION RESULTS

The operation of the proposed bidirectional 5L-M²DCR has been evaluated with the power factor control under various load conditions. Figs. 11 and 12 show the unity power factor operation under two different types of loading effect. However, the proposed unidirectional 5L-M²SCR topology can only achieve unity power factor without any reversal power capability with same performance obtained in Fig. 11.

The reversal power capability with the current shaping in

Fig. 12(a) is achieved by connecting a DC source (i.e. fuel cell, solar, etc.) across the dc-link, in order to validate the bidirectional power flow of the proposed 5L-M²DCR. Since the power factor of the 5L-M²DCR topology can be controlled to achieve leading/lagging performance as shown in Figs. 13 and 14, hence it is known as a four-quadrant multilevel rectifier. With such inherent performances, it is concluded that the 5L-M²DCR can be applicable for reactive power compensator applications with power factor control capability, while the 5L-M²SCR is highly recommended for grid connected rectifier that can be configured either with direct DC load or back-to-back converter that does not require any regenerative power capability.

V. EXPERIMENTAL RESULTS

The AC/DC/AC hardware prototypes are constructed based on the proposed circuit diagrams of Figs. 1 and 3 with the controller loop as shown in Fig. 10. The controller is implemented utilizing the dSPACE RTI1103 controller board. The experimental results are obtained based on chosen system parameters values shown in Table IV.

The input current shaping of the two proposed front-end rectifiers is achieved through the application of proper gating signals based on the LS-PWM. Since the front-end bidirectional 5L-M²DCR consists complementary switches, therefore additional dead time circuits are needed to prevent short circuit. Unlike the 5L-M²DCR, the unidirectional 5L-M²SCR does not have any complementary switches. Hence, the gating signals for 5L-M²SCR are generated with the four logic NAND gates as shown in Fig. 10.

The experimental results obtained in Figs. 15(a) and (b) show the input voltage and current quality of both front-end unidirectional 5L-M²SCR and bidirectional 5L-M²DCR respectively. Both proposed topologies achieve low input current distortions yielding a 0.99 power factor and the general expression of the power factor for bidirectional rectifier is expressed in [20].

$$PF = \frac{\cos \phi}{\sqrt{1 - THD_i^2}} \quad (14)$$

The input pole voltage in Fig. 15(b) is slightly distorted as compared to the Fig. 15(a). This is due to the instantaneous high reverse peak I_{dc} current fed into the close-loop controller. Thus, the current error signal is being affected and caused the input pole voltage to be synthesized from positive voltage step to the negative voltage step as well as vice versa.

Same rear-end 5L-M²DCI topology is implemented for both front-end uni and bidirectional topologies. The experimental results of the output pole voltages and output line-to-line voltages are obtained as shown in the Figs. 16(a) and (b) respectively.

VI. CONCLUSION

A new generation of front-end unidirectional 5L-M²SCR and bidirectional 5L-M²DCR topologies are introduced in this paper to reduce the number of semiconductor devices as compared to the conventional converters. The agreement between the theoretical analysis and the experimental results are validated and also has proven the feasibility of the two proposed AC/DC/AC topologies.

Excellent performance and low input current distortion with high power factor is achieved with low operational switching frequency of 1 kHz without the aid of any bulky LC passive filter. Besides that, the reduction of component counts allows the proposed converters to achieve low voltage/current stress and low switching losses. As a result, the overall converter efficiency is also improved. The size of input reactors is greatly reduced as well because of the incremental voltage stepped waveforms synthesized at low switching frequency. This is at the small cost of having an additional voltage balancing circuitry in the dc-link to balance the capacitor voltages.

However, the dc-link voltage balancing circuit is restricted to certain power applications. For the case of medium voltage drives, the size of the inductors (L1 and L2) in the balancing circuit must be extremely large to meet such required power ratings. Thus, alternative dc-link balancing strategies such as modulation schemes [21, 22] or control algorithms can be implemented to replace the additional balancing circuit. These will provide a more cost effective and energy efficient solution for a higher-level AC/DC/AC drive and can especially be suitable for renewable energy conversion where high efficiency is paramount.

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