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Regular article

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Abstract: Subwavelength modulators play an indispensable role in integrated photonic-electronic circuits. Due to weak light-matter interactions, it is always a challenge to develop a modulator with a nanometer scale footprint, low switching energy, low insertion loss and large modulation depth. In this paper, we propose the design of a vanadium dioxide dual-mode plasmonic waveguide electroabsorption modulator using a metal-insulator-VO₂-insulator-metal (MIVIM) waveguide platform. By varying the index of vanadium dioxide, the modulator can route plasmonic waves through the low-loss dielectric insulator layer during the “on” state and high-loss VO₂ layer during the “off” state, thereby significantly reducing the insertion loss while maintaining a large modulation depth. This ultracompact waveguide modulator, for example, can achieve a large modulation depth of ~10 dB with an active size of only 200×50×220 nm³ (or $\sim\lambda^3/1700$), requiring a drive-voltage of ~4.6 V. This high performance plasmonic modulator could potentially be one of the keys towards fully-integrated plasmonic nanocircuits in the next-generation chip technology.

Keywords: dual-mode; modulator; plasmonics; ultracompact; vanadium dioxide.

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1 Introduction

The continuous scaling down in electronic chips has resulted in the electrical interconnect bottleneck problem [1]. One solution is to replace the electrical interconnect with a silicon photonic waveguide, which is superior in terms of negligible propagation loss, high transmission speed and huge data-carrying capacity [2]. However, photonic-based optoelectronic devices suffer from low response times and high energy consumption due to their sizes. Hence, we look towards plasmonics as a possible device technology to overcome the problems faced by photonic devices. The nature of surface plasmons that allows light to be squeezed far below the diffraction limit has generated interest in the development of miniature chip-scale optoelectronic devices that promise high responsivity and low energy consumption [3]. Progress is seen in the development of plasmonic waveguides [4–6], plasmonic photodetectors [7–9], and plasmonic modulators [10–14].

Plasmonic modulators have numerous performance requirements to meet, such as small device footprint, low switching energy consumption, low insertion loss, high switching speed and large modulation depth [10]. These performance indicators are heavily influenced by both device structure design and the nonlinear coefficient of the active material. Robust structure design could reduce device insertion losses and switching energies. However, the modulation depth – the crucial performance parameter for modulators – is largely determined by the nonlinear coefficient of the active material. For example, silicon, the favored CMOS compatible material, only records a refractive index change, Δn of $\sim 10^{-3}$ [15]. Barium titanate, meanwhile, can show Δn as high as ~ 0.05 [16]. Recently, indium tin oxide (ITO) garnered some research interest due to its ability to show unity-order index change [17, 18].

Here, we discuss a special class of materials which can show similar unity-order index change but occurs throughout the bulk material – the Mott insulator. The Mott insulator is a solid state phase change material which shows a

first order insulator-metal transition (IMT) under certain conditions [19], and it is usually accompanied by a large refractive index change. Vanadium dioxide (VO_2) is one of the Mott insulator candidates, which shows a large refractive index contrast of $n=3.243+0.3466i$ for the insulating phase to $n=1.977+2.53i$ for the metallic phase at the operating wavelength of 1550 nm [20]. The phase transition can be triggered by thermal excitation [21], optical excitation [22], electrical excitation [23], doping [24], or strain engineering [25]. For an electrical excitation scheme, the field required for the phase change to occur is experimentally recorded to be 6.5×10^7 V/m [23]. Independent experiments show that the phase transition is typically picoseconds or faster, making it a potentially ultrafast switching material [26]. Hence, VO_2 has recently attracted research interest in various optical modulator designs [27, 28]. In [27], the authors achieved 6.5 dB modulation with 2 dB insertion loss for a 2 μm long device and 65 nm thin VO_2 films, using a thermal-excitation scheme. In [28], 20 dB modulation is achieved, however with a thick 1 μm waveguide stack.

In this paper, we propose a new type of VO_2 modulator by using a “dual-mode” plasmonic waveguide to realize a low-loss, low energy consumption and highly-compact plasmonic modulator. Taking advantage of the large refractive index contrast between the insulating and metallic phases of VO_2 , the dual-mode plasmonic waveguide modulator has the ability to switch transmission modes between

a low loss hybrid plasmonic mode and a high loss metal-insulator-metal (MIM) mode during the “on” and “off” states, respectively. Thus, the modulator is able to achieve very high modulation depth (~10 dB) with low insertion loss (~1 dB) with this novel modulation scheme.

2 Vanadium dioxide plasmonic slot waveguide modulator

To evaluate the switching performance of VO_2 , we first consider a simple plasmonic slot modulator using VO_2 as its active material. The VO_2 is sandwiched between two copper layers to form a metal-insulator-metal (MIM) waveguide as shown in Figure 1A. We used copper (Cu , $\epsilon=-122+6.2i$) as the plasmonic material in building the waveguide due to its low propagation loss among CMOS compatible metal materials in the near-infrared wavelengths [29]. The front and back ends of the VO_2 slot are interfaced with copper-silicon-copper MIM plasmonic tapered couplers. Silicon taper ($n=3.48$) is used to index-match with the insulating phase of VO_2 to minimize coupling loss. The plasmonic tapered couplers have widths decreasing linearly from 400 nm to the slot width that couple light to and from 400 nm wide silicon waveguides. The whole device is planar and 220 nm thick. Since this device will be used as

Figure 1 (A) Vanadium dioxide plasmonic slot waveguide modulator. (B) Electric-field map of surface plasmons confined in the Cu- VO_2 -Cu slot, as seen from the cross-sectional cutting plane. (C) Variation of insertion loss and modulation depth with slot width. (D) Insertion loss and modulation depth for a 50 nm wide slot waveguide modulator.

an electroabsorption modulator, we denote the VO_2 insulating phase as the “on” state, and the metallic phase as the “off” state due to its increased extinction coefficient.

We simulated this device using C.S.T. Microwave Studio 2012 [30]. Figure 1B shows the electric-field of the surface plasmons being confined strongly inside the $\text{Cu-VO}_2\text{-Cu}$ slot, observed at the cross-sectional cutting plane. Next, Figure 1C shows the variation of the insertion loss and modulation depth with slot widths. At ultra-narrow slot widths (10 nm–40 nm), a tight confinement in the MIM waveguide results in high propagation losses. The loss does not reduce further for slot widths ≥ 50 nm, and hence we choose 50 nm for the slot width to obtain a relative low insertion loss and a reasonable modulation-voltage. Meanwhile, Figure 1D shows the insertion loss (optical attenuation in dB units in the “on” state) and modulation depth (optical attenuation in dB units in the “off” state less the insertion loss) for a 50 nm wide slot waveguide modulator, measured to be around 10 dB/ μm and 50 dB/ μm , respectively. For a 200 nm long waveguide modulator, it would have a 2 dB insertion loss and a 10 dB modulation depth. Optimized couplers have a ~ 0.5 dB loss per facet. At an electric-field threshold of $\sim 6.5 \times 10^7$ V/m [23], the device requires a drive-voltage of ~ 3.3 V arising from the narrow slot width of 50 nm.

Energy consumption of the device is roughly divided into three components: capacitive loss across the VO_2 waveguide, capacitive loss across the plasmonic tapers, and joule heating loss due to leakage currents. If the modulator is assumed to be a simple capacitive device, the 200 nm waveguide modulator would require an energy/bit of $\frac{1}{2}CV^2 = \frac{1}{2} \frac{\epsilon\epsilon_0 A}{d} V^2 = 1.53$ fJ/bit (using ϵ_{VO_2-I} (constant) ~ 36 [31], $\epsilon_0 = 8.85 \times 10^{-12} \text{ Fm}^{-1}$). For the silicon plasmonic tapers, if we assume that they are 200 nm in length and have an average width of 225 nm, the energy/bit loss of each taper is 0.113 fJ/bit (using ϵ_{Si} (constant) ~ 12). Finally,

the joule heating term, given as $\frac{V^2}{RB} = \frac{V^2}{\left(\frac{\rho d}{A}\right)B} = 9.6$ fJ/bit

(using $\rho_{\text{VO}_2-M} \sim 1 \text{ } \Omega\text{m}$ [32], assuming $B=1$ GHz operating bandwidth). The total energy consumption is 11.4 fJ/bit, with the substantial waste coming from the joule heating loss.

Despite the exceptional switching performance of VO_2 , it suffers from high insertion loss due to the plasmonic mode being concentrated in the lossy VO_2 medium. To reduce the loss, one idea is to reroute the surface plasmons from the VO_2 layer to another lossless or low-loss dielectric layer during the “on” state, since we do not

require the surface plasmons to be present in the insulating phase of VO_2 . This idea leads us to the design of a dual-mode plasmonic waveguide modulator, which will be discussed in the next section.

3 Vanadium dioxide dual-mode plasmonic waveguide modulator

3.1 Dual-mode waveguide design

Here, we design a VO_2 waveguide modulator with two transmission modes that can be switched by varying the index of the VO_2 . Figure 2A shows the schematic of the proposed plasmonic waveguide modulator. The device is similar to the plasmonic slot waveguide modulator shown in Figure 1A, except that the VO_2 and silicon plasmonic tapered couplers are now coated with a thin layer of lossless dielectric before being flanked by the metal layers, forming a metal-insulator- VO_2 -insulator-metal (MIVIM) waveguide. During the “off” state, the surface plasmons undergo high extinction in the metallic VO_2 layer, and thus the electric-field distribution is similar to the MIM mode shown in Figure 1B. During the “on” state, we switch the transmission to the low-loss cladding layers to reduce the insertion loss. This is done by raising the refractive index of VO_2 and converting the electric-field distribution to a hybrid plasmonic (MIVIM) mode as shown in Figure 2B [4, 5]. We refer to this design as a “dual-mode waveguide”, the primary mode transmitting through the VO_2 core layer, and the secondary mode through the cladding layers of lossless dielectric. The structure of this waveguide is in-part inspired by recent-fabricated multi-layer nano-plasmonic slot waveguides which are easy to fabricate [33, 34].

The refractive index of the dielectric slot is important in the mode switching mechanism of the dual-mode waveguide, and hence affecting the modulation performance. Due to the large refractive index difference between the insulator (VO_2-I) and metallic (VO_2-M) phases of VO_2 , there are three distinct categories of dielectric slot refractive indices: $n_{\text{slot}} < n_{\text{VO}_2-M}$, $n_{\text{VO}_2-M} < n_{\text{slot}} < n_{\text{VO}_2-I}$ and $n_{\text{VO}_2-I} < n_{\text{slot}}$. The proportion of surface plasmon modes travelling in the dielectric and VO_2 layers would depend on the category in which the dielectric slot refractive index belongs to, and hence determine the surface plasmon mode profile. In general, a higher portion of surface plasmons would travel in a lower index region. Hence, in both the “on” and “off” states, the $n_{\text{slot}} < n_{\text{VO}_2-M}$ modulator operates in

Figure 2 (A) Vanadium dioxide dual-mode plasmonic waveguide modulator. (B) Electric-field map showing strong confinement of surface plasmons in the Cu-SiO₂-VO₂ slots in the “on” state, as observed at cross-sectional cutting plane. (C) Variation of insertion loss with VO₂ and SiO₂ slot widths. (D) Variation of modulation depth with VO₂ and SiO₂ slot widths.

the hybrid plasmonic mode, while the $n_{\text{VO}_2\text{-I}} < n_{\text{slot}}$ modulator operates in the MIM mode. However, in the case of $n_{\text{VO}_2\text{-M}} < n_{\text{slot}} < n_{\text{VO}_2\text{-I}}$, the modulator operates in the hybrid plasmonic mode only in the “on” state. In the “off” state, when the metallic VO₂ index is lower than that of the dielectric slot, the modulator switches to the MIM mode. We specially refer to this property as “modal switching”.

Figure 3 Left axis: insertion loss and modulation depth of the dual-mode plasmonic waveguide modulator as functions of refractive indices of the dielectric slot. Right axis: corresponding modulation depth to insertion loss ratio.

The benefit of the modal switching is clearly seen in Figure 3. On this figure’s left axis, we see two clearly distinct trends, in which the insertion loss increases monolithically with the dielectric refractive index, while the modulation depth increases in the form of a sigmoid curve. This modal switching causes a large appreciation of modulation depth with refractive index in the $n_{\text{VO}_2\text{-M}} < n_{\text{slot}} < n_{\text{VO}_2\text{-I}}$ region. This is very useful to maintain low insertion losses while gaining reasonably high modulation depths. On the right axis of the figure, the modulation depth to insertion loss ratio is plotted. This ratio is considered as a useful figure-of-merit to determine the optimal dielectric slot index for the modulator to operate in, whereby the drop in the insertion loss should over-compensate the drop in the modulation depth. It is observed that this ratio peaks at refractive indices in the $n_{\text{VO}_2\text{-M}} < n_{\text{slot}} < n_{\text{VO}_2\text{-I}}$ region, hence confirming that the best modulation performance occurs through the modal switching.

Table 1 Three dielectric slot materials and their relationships with the two phases of VO₂.

VO ₂ insulator phase (VO ₂ -I), $n=3.243+0.3466i$		
VO ₂ metallic phase (VO ₂ -M), $n=1.977+2.53i$		
SiO ₂ , $n=1.44$	TiO ₂ , $n=2.7$	Ge, $n=4.27$
$n_{\text{SiO}_2} < n_{\text{VO}_2\text{-M}}$	$n_{\text{VO}_2\text{-M}} < n_{\text{TiO}_2} < n_{\text{VO}_2\text{-I}}$	$n_{\text{VO}_2\text{-I}} < n_{\text{Ge}}$

3.2 Layer geometry

While it was mentioned above that the refractive indices of the dielectric slot and VO_2 determine the proportion of traveling surface plasmon modes, here the slot widths would determine the “carrying capacity” of the slot layers. That is, on top of distribution according to the refractive index, the surface plasmon modes also distribute according to the dimensions. For example, in

a $\text{Cu-SiO}_2\text{-VO}_2\text{-SiO}_2\text{-Cu}$ waveguide stack, variation of the widths of the SiO_2 and VO_2 layers will affect the insertion loss as well as the modulation depth. Figure 2C shows that in general, the insertion loss increases with increasing VO_2 slot widths and decreasing SiO_2 slot widths. Similar trends could be seen for the modulation depth as well in Figure 2D. The choice of dielectric and VO_2 slot widths should therefore consider the tradeoff between low insertion losses, high modulation depths and low

Figure 4 Insertion loss and modulation depth for the dual-mode plasmonic waveguide modulator with the dielectric slot filled with (A) SiO_2 , (B) TiO_2 and (C) Ge material. (D), (E) and (F) are corresponding lateral electric-field profiles (normalized to refractive index) for the “on” and “off” states for SiO_2 , TiO_2 and Ge-filled slots, respectively.

drive-voltages to obtain an optimal device performance. For the subsequent discussions we will use a VO_2 slot width of 50 nm and a dielectric slot width of 10 nm as our reference dimensions.

3.3 Case studies

Here we examine three different dielectric slot materials (SiO_2 , TiO_2 and Ge), characterized by their relationships with the two phases of VO_2 as tabulated in Table 1. Figure 4 shows the simulation results for the three different dielectric slot materials. For the case of SiO_2 in Figure 4A, the insertion loss is 2 dB/ μm , and modulation depth is 13 dB/ μm . For TiO_2 in Figure 4B, the insertion loss is 5 dB/ μm , and the modulation depth is 45 dB/ μm . For Ge in Figure 4C, the modulation depth is the highest at 57 dB/ μm , but comes with a larger insertion loss of 8 dB/ μm . Optimized coupling losses from the plasmonic tapered couplers are determined to be ~ 0.5 dB per facet on average.

Figures 4D, E and F are the index-normalized lateral electric-field profiles of the dual-mode waveguide for SiO_2 , TiO_2 and Ge, respectively. For SiO_2 , in both “on” and “off” cases, the modulator operates in the hybrid plasmonic mode, hence explaining the low insertion loss and low modulation depth. For Ge, in both cases the modulator operates in the MIM mode, hence the high insertion loss and modulation depth. However, for TiO_2 , the modal switching occurring between the “on” and “off” states are remarkably seen in Figure 4E. In the “on” state, the modulator operates in the hybrid plasmonic mode, confining the surface plasmons in the dielectric slot. In the “off” state, the modulator operates in the MIM mode and as a result a great portion of the surface plasmons is transmitted in the VO_2 layer.

Table 2 shows the modulation depth to insertion loss ratio of various insulating slot materials of 200 nm length VO_2 dual-mode plasmonic waveguide modulators. The “no slot” column refers to the simple plasmonic slot waveguide modulator in section 2. From the ratio figures, it is evident that TiO_2 shows the largest ratio of modulation depth and insertion loss. This analysis validates TiO_2 to be the optimal dielectric material choice among the three reported materials.

The additional 10 nm dielectric slot layers slightly increases the waveguide width to 70 nm. Using an electrical excitation scheme with a field threshold of $\sim 6.5 \times 10^7$ V/m, we work out the drive-voltage to be ~ 4.6 V. The capacitive loss of the waveguide is 2.12 fJ/bit, and 0.220 fJ/bit for each silicon plasmonic taper. Leakage

Table 2 Modulation depth to insertion loss ratio of various VO_2 dual-mode plasmonic waveguide modulators (200 nm length).

	Dielectric slot material			
	No slot	SiO_2	TiO_2	Ge
Insertion loss	2 dB	0.4 dB	1 dB	1.6 dB
Modulation depth	10 dB	2.6 dB	9 dB	11.4 dB
Ratio	5	6.5	9.0	7.1

currents which contribute to joule heating loss will be negligible. Therefore, the total energy consumption is very much reduced to 2.6 fJ/bit.

Finally, we compare our results with a recent work using similar modal-switching concept for a hybrid VO_2 plasmonic switch, but employed a metal-insulator- VO_2 (MIV) structure [35]. While the MIV structure efficiently reduced the insertion loss of the device during the “on” state, it suffered from low modulation depth because the surface plasmons are not efficiently confined in the VO_2 layer during the “off” state. The MIV design in [35] reported a highest modulation depth of only 6.1 dB/ μm .

4 Conclusion

We have proposed an ultracompact, high modulation depth, low insertion loss, and low energy consumption plasmonic modulator by employing VO_2 in a plasmonic dual-mode waveguide. The dual-mode configuration has the ability to route surface plasmons through low-loss or lossless dielectric layers in the “on” state, and rerouting them through the lossy VO_2 medium in the “off” state, thereby significantly reducing insertion loss while maintaining a high modulation depth. The designed modulator could be as short as ~ 200 nm ($\sim \lambda/8$) in length, and have low insertion loss (~ 1 dB) and high modulation depth (~ 10 dB). The device’s drive-voltage is ~ 4.6 V, with energy/bit as low as 2.6 fJ/bit. This high performance modulator contributes a step closer to realizing fully-integrated nanophotonic-nanoelectronic nanocircuits in next-generation chip technology.

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