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2014

Liu, X., Zhou, J., Yang, Y., Wang, B., Lan, J., Wang, C., et al. (2014). A 457 nW Near-Threshold Cognitive Multi-Functional ECG Processor for Long-Term Cardiac Monitoring. IEEE Journal of Solid-State Circuits, 49(11), 2422-2434.

<https://hdl.handle.net/10356/81729>

<https://doi.org/10.1109/JSSC.2014.2338870>

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A 457-nW Near-Threshold Cognitive Multi-Functional ECG Processor for Long-Term Cardiac Monitoring

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Abstract— A low-power multi-functional Electrocardiogram (ECG) signal processor is presented in this paper. To enable long-term monitoring, several architecture-level power saving techniques are proposed, including global cognitive clocking, pseudo-downsampling wavelet transform, adaptive storing, and denoising-based run-length compression. An ultra-low-voltage ADC is designed for low-power signal digitization with adaptive clocking. Through these architecture-level techniques, the total power consumption can be significantly reduced by 63% as compared to the conventional design. Several circuit-level design techniques are also developed, including ultra-low-voltage operation and near-threshold level shifting, to further reduce the power consumption by 33%. In addition, a low-complexity cardiac analysis scheme is proposed to realize comprehensive on-chip cardiac analysis. Implemented in 0.18 μm CMOS process, the proposed cognitive ECG processor consumes only 457 nW at 0.5 V for real-time ECG recording and diagnosis.

Index Terms— ECG, ultra low power, cognitive, multi-functional, near-threshold

I. Introduction

Electrocardiogram (ECG) is a common medical investigation, which is widely used in

healthcare applications for monitoring and diagnosis, from heart attacks to electrolyte imbalances [1]. Long-term ECG monitoring is highly desired to detect, characterize and document cardiac arrhythmias in clinical practice. To mitigate the workload of medical professionals and reduce the power consumed for raw ECG data transmission, it is highly recommended that the ECG recording system has comprehensive on-chip cardiac analysis capabilities. During the past few years, the intelligent ECG sensor design has got more and more attention because it contains an on-chip signal processor which can perform signal filtering, data analysis, and wireless baseband processing, etc. There are two key design challenges in the on-chip ECG processor design. The first challenge is that the power consumption should be extremely low in order to maximize its battery lifetime, because of the limited power source and system size. The second challenge is that the on-chip ECG processor should be able to perform comprehensive cardiac analysis functions, given such limited power budget.

Several state-of-art ECG processor designs have been proposed [2–8]. Some designs have an embedded RISC core [2, 3], so that they can achieve high reconfigurability to realize diverse functions by running different software. However, their power consumption is relatively high due to the nature of software execution. In [4–8], application-specific ECG processors without the RISC core have been reported. This type of ECG processors has lower power consumption, while their reconfigurability is limited as they usually provide limited functions, such as *QRS* detection and heart-beat-rate (HBR) calculation. The advanced ECG monitoring for diagnosis and clinical treatment requires much more comprehensive functions. These functions include the clean ECG reconstruction after filtering the noise and interference for visual diagnosis, the important cardiac features extraction related to *P* wave, *T* wave, and the corresponding intervals calculation [9, 10], etc. In our previous work [11], an application-specific ECG processor was proposed to realize multiple functions, including *QRS* detection, HBR calculation, noise suppression and baseline drift removal, and the clean ECG reconstruction. However, its power and area consumptions are

relatively large due to the increased complexity of processing algorithms.

In this paper, we present a real-time multi-functional ECG processor for long-term monitoring, which archives ultra-low power consumption and realizes comprehensive cardiac analysis functions [12]. Various power-saving techniques are proposed from different levels of design hierarchy. In the architecture level, a global cognitive clocking scheme is proposed for the entire system, by which the system operation clock can dynamically switch between different frequencies according to different temporal resolution requirements. Correspondingly, an ultra-low-voltage analog-to-digital converter (ADC) is developed with adaptive clocking. As the conventional design uses large number of storage units which consume large power and silicon area, several novel architecture-level techniques are developed to reduce the number of storage units and their access frequency, and to maintain the performance. Such techniques include pseudo-downsampling wavelet transform and inverse wavelet transform (PDWT and PDIWT), adaptive storing, and denoising-based run-length compression (DBRLC). To realize comprehensive on-chip cardiac analysis with low power, a low-complexity cardiac analysis scheme is proposed. It can realize $P/QRS/T$ detection, morphology identification, as well as $P-R/R-T/R-P$ intervals calculation. This on-chip analysis scheme is designed to be reconfigurable so that the analysis of different ECG segments can be realized, and thus most of the hardware resource can be reused to minimize the overhead.

In addition to the architecture-level techniques, several circuit-level design techniques are proposed to further reduce the power consumption while achieving reliable performance. Ultra-low-voltage operation techniques are used for the ECG processor, by which the operating voltage can be scaled down to the near-threshold region. Correspondingly, a novel near-threshold level shifter design is proposed to transfer the signal between the core operating at the near-threshold voltage and the I/O pads operating at super-threshold voltage. A glitch-free clock switch is also implemented to enable the reliable cognitive clocking. With all aforementioned

techniques, the proposed ECG processor achieves extremely low power consumption, making it well suited for power-constrained long-term cardiac monitoring.

II. ECG Processor System

Fig. 1 illustrates the overall system architecture of the proposed ECG processor, which includes an ultra-low-voltage ADC block and a digital signal processing engine (DSPE). In our system, the 50/60 Hz power line interference and low-frequency baseline wandering/motion artifact are filtered out in off-chip analog front-end before ADC. The DSPE module performs quadratic spline wavelet transform (WT) for ECG decomposition [4, 11]. The high-frequency noise and interference are suppressed by the signal processing on WT decomposition outputs, and the clean ECG signal is reconstructed by the inverse WT (IWT) [11]. According to the characteristic of the ECG signal, the sampling rate is chosen in the range of 250 Hz – 1 kHz for different temporal resolution requirements [4], [9], [13], [14], [15]. In our design, to enable visual diagnosis using reconstructed clean ECG waveform, 500 Hz is chosen for QRS segment, and 250 Hz is chosen for the rest segments, to achieve an optimal trade-off between good temporal resolution and low system complexity, and thus 4 scales of WT is sufficient for the required signal processing. A cardiac signal analysis (CSA) module performs the on-chip analysis using decomposition high pass filter (DHPF) outputs. It can detect *P* wave, *QRS* complex and *T* wave, identify ECG waveform morphology, and *P-R*, *R-T*, *R-P* intervals calculation. A cognitive clock management module is designed to track the characteristic of ECG waveform and generate dynamic operation clocks for different modules. In the following sections, key power-saving design techniques are described in details.

III. Architecture-Level Design Techniques

A. Global Cognitive Clocking Scheme

Fig. 2 presents the morphology of the ECG waveform. The most significant characteristics are *QRS* complex, *P* wave, and *T* wave. Among them, *QRS* complex contains more components with higher frequencies, whereas *P* and *T* waves are dominated by components with lower frequencies.

Theoretically, the bandwidth of *QRS* complex is around 8 – 27 Hz, and the bandwidth of *P* and *T* waves is around 4 – 13.5 Hz [9, 10]. In the conventional ECG signal processing, the constant sampling rate which satisfies the Nyquist sampling theorem for *QRS* complex is adopted for the entire ECG waveform, as shown in Fig. 3(a). However, it can be observed that the duty cycle of *QRS* segment is comparatively low (typically ~25%), and all the rest are low frequency segments (~75%). Therefore, it is unnecessary and power-wasting to apply the same high sampling rate for *P/T* segments as that for *QRS* segment.

Based on this observation, it is reasonable to apply a high sampling rate only for the *QRS* segment, while applying a low sampling rate for the rest of the waveform, as shown in Fig. 3(b). By doing so, the total amount of sampled data can be reduced greatly, compared with the method using constantly high sampling rate. Meanwhile, the quality of the obtained ECG waveform is still satisfying because the Nyquist sampling rate for each segment (*QRS*, *P/T*) is maintained, and sufficiently high resolution is achieved for visual diagnosis. In this design, we apply 500 Hz and 250 Hz for *QRS* segment and *P/T* segments respectively. In Fig. 3(c), considering that the typical duty cycle of *QRS* segment is around 25%, the total amount of data that needs to be processed can be reduced to around 62.5% compared to that using the conventional clocking, resulting in significant reduction of the overall power consumption. Fig. 4 presents the block diagram of the global cognitive clocking scheme. The upper part presents the main signal processing modules of the ECG processor. The operation clocks of different modules are generated by a clock generator, including an ADC internal clock f_{smp} , an ADC sampling clock f_{ADC} , and a DSPE clock f_{DSPE} . The frequencies of all these clocks can be adjusted cognitively according to the characteristic of the input signals. The DHPF output in Scale 2 (DHPF_S2) is compared with a threshold T_f to decide whether a high frequency f_H or a low frequency f_L should be adopted. If DHPF_S2 is higher than T_f , it indicates that the *QRS* segment occurs. Then higher frequencies are used for f_{smp} , f_{ADC} , and f_{DSPE} . After a pre-defined period, all the clocks switch back to the lower frequencies for processing *P/T*

segments.

The threshold T_f is calculated adaptively from DHPF_S2' which is the output obtained after processing DHPF_S2 with the noise suppression module to track the trend of the input signal. We define the n^{th} instant threshold as $\hat{T}_f(n) = \alpha \times \text{DHPF_S2}'$, where DHPF_S2' is the DHPF_S2 output after noise suppression. α is a weighting factor and its value set by experience determines the instant threshold based on the current value of DHPF_S2'. Assuming that the $(n-1)^{\text{th}}$ threshold is $T_f(n-1)$, the value of $T_f(n)$ is updated by a recursive algorithm

$$T_f(n) = \lambda T_f(n-1) + (1 - \lambda) \times \hat{T}_f(n) \quad (1)$$

where λ is a forgetting factor and its value is set by experience within the range of $0 < \lambda < 1$, as shown in Fig. 4. For ASIC implementation, we can choose the values like 0.875, 0.9375, or 0.96875, so that the multiplication circuit can be easily replaced by a shift-and-add circuit to reduce the complexity.

It is noted that due to the dynamic change of the operation clock frequency f_{DSPE} , there is a timing change in the processor outputs compared to the original waveform. To solve this issue, a retiming output buffer is designed by using another clock signal f_{OUT} , as shown in Fig. 4. f_{OUT} is a delayed version of f_{DSPE} , where the delay d_{OUT} is equivalent to the processing delay of DSPE module. The ECG processor outputs are stored in this output buffer with f_{DSPE} firstly, and then read out with f_{OUT} . In this way, the processor outputs with correct timing information can be obtained.

Some signal acquisition hardware with adaptive sampling rate or adaptive resolution has been proposed. In [16], an analog decision module is designed to sense the rate of the input signal change by using a switched-capacitor (SC) differentiator. This SC structure consumes relatively large area especially when it is used to process low-frequency signal such as ECG. In our design, however, as WT outputs are readily available for ECG signal processing in the system, there is no significant area and power overhead caused by another dedicated module to generate control signals for clock selection. According to the synthesis results, the area overhead of the proposed

global cognitive clocking is only around 2% of the overall chip size. Moreover, the SC differentiator may amplify high-frequency noise and interference. In contrast, the effect of both high- and low-frequency noise and interference is greatly reduced in our design, because the bandwidth of DHPF_S2 output is at the median of the ECG signal. It is also important to note that DSPE dominates the power consumption in our system, so that the cognitive clocking is applied to not only ADC but also DSPE module to achieve significant power reduction of the overall system.

The reasons why DHPF_S2 is chosen for the frequency control are as follow. Firstly, the 2nd scale of WT is at the median of WT decomposition, and thus its output has less high-/low-frequency noise and interference. The frequency control using DHPF_S2 output is more robust and reliable, compared to the control using DHPF output of other scales. Secondly, the control using DHPF_S2 minimizes the processing delay in the feedback loop. This processing delay mainly comes from the WT and comparison modules. If this processing delay is not small enough, distortion will occur at the beginning of fast sampling stage. Since the WT decomposition is performed on the input ECG signal sequentially from low scale to high scale, the processing delay when using DHPF_S2 is smaller than the delay when using higher scales. Therefore, DHPF_S2 is selected for frequency control to archive fast tracking and minimal distortion.

B. Ultra-Low-Voltage ADC with Adaptive Clocking

A non-binary redundant SAR ADC is designed to sample the signal using the proposed cognitive clocking scheme, as shown in Fig. 5. The operation voltage can be scaled down to 0.5 V, while maintaining the effective number of bits (ENOB) greater than 8.1 bits. The ADC clocks f_{ADC} and f_{samp} can switch between high frequencies (6 kHz and 500 Hz) and low frequencies (3 kHz and 250 Hz) using a glitch-free clock switch in the cognitive clock manager. A bootstrapped switch with gate signal swing from 0 to 2 VDD is used to reduce switching delay and improve linearity of the sampling circuit for ultra-low-voltage operation. Single-ended structure and top-plate sampling technique are employed to minimize power consumption. Non-binary redundant

algorithm is also adopted to correct the decision errors made in the initial conversion steps, which allows slower settling for better power efficiency at the expense of additional redundant bits [17]. Splitting the capacitor array into a pair of subtraction and addition capacitor arrays maximize energy saving during switching events. A time-domain comparator consisting of voltage controlled delay lines and a binary phase detector [18] is used to eliminate static power consumption and enable ultra-low-voltage operation.

C. Pseudo- Downsampling WT & IWT and Adaptive Storing

WT is widely used for singular point detection [9, 19], and it is simple for hardware implementation [4]. WT can be implemented by a cascade of finite impulse response (FIR) filters. There are 4 types of WT filters, i.e., decomposition high pass filter (DHPF), decomposition low pass filter (DLPF), reconstruction high pass filter (RHPF), and reconstruction low pass filter (RLPF). We denote $l_{D,j}(i)$, $h_{D,j}(i)$, $l_{R,j}(i)$, and $h_{R,j}(i)$ as the coefficients of the j^{th} scale DLPF, DHPF, RLPF and RHPF, respectively. Figs. 6 (a) and (b) illustrate two implementations of WT, i.e., downsampling WT (DWT) and non-downsampling WT (NDWT). In DWT, the WT output of each scale is down-sampled twice before being fed to the next scale, but it makes the signal representation time-variant and reduces the temporal resolution of the wavelet coefficients with the scale increasing, as explained in [10]. Therefore, in our design, NDWT is adopted for ECG signal decomposition, reconstruction and cardiac signal analysis [10, 11]. For $j=1$, the coefficients of $l_{D,1}(i)$, $h_{D,1}(i)$, $l_{R,1}(i)$, and $h_{R,1}(i)$ are given by $\{0.125, 0.875, 0.875, 0.125\}$, $\{2, -2\}$, $\{0.125, 0.875, 0.875, 0.125\}$, $\{-0.0078125, -0.054685, -0.171875, 0.171875, 0.054685, 0.0078125\}$, respectively [11, 20]. For $j > 1$, $l_{D,j}(i)$, $h_{D,j}(i)$, $l_{R,j}(i)$, and $h_{R,j}(i)$ are obtained by inserting $2^{j-1}-1$ zeros between each non-zero coefficients [11]. For example, Fig. 6 (c) shows the hardware implementation of DLPF, where $y_j(i)$ is the i^{th} DLPF outputs of j^{th} scale. It can be observed that the NDWT has a “sparse” structure, because there are huge numbers of filtering taps but only few of them are used for multiplication and addition operations, especially for higher scale with $2^{j-1}-1$

increasing. The FIR filtering stages are normally implemented by shift registers, and thus the hardware area and the power consumption will be significantly increased when the number of filtering tapes increases. In [11], static random-access memory (SRAM) is utilized to realize the data delay and FIR filtering for such “sparse” filter structure, which can reduce the frequency of data shifting and hardware overhead. However, huge number of storage units and their access are still required for the intermediate data storage. For example, since all the DLPF outputs need to be used for the next scales filtering in Fig. 6 (c), $2^{j-1}-1$ storage units or shift registers need to be used between any two non-zero filter coefficients.

In this paper, we propose a novel WT processing scheme, named pseudo-downsampling WT & IWT (PDWT & PDIWT). We denote $y_j(i)$ as the i^{th} value of WT output. Similar as DWT, we will store WT outputs in every $2^{j-1}-1$ samples, i.e., $y_j(k \times 2^{j-1})$, where $k=0,1,2,\dots$. The average increment $\Delta y_j(k)$ between WT outputs $y_j(k \times 2^{j-1})$ and $y_j((k+1) \times 2^{j-1})$ is calculated and stored.

$$\Delta y_j(k) = [y_j((k+1) \times 2^{j-1}) - y_j(k \times 2^{j-1})] / 2^{j-1}. \quad (2)$$

For $y_j(k \times 2^{j-1} + n)$ between $y_j(k \times 2^{j-1})$ and $y_j((k+1) \times 2^{j-1})$, the value can be approximated by

$$\hat{y}_j(k \times 2^{j-1} + n) = y_j(k \times 2^{j-1}) + n \times \Delta y_j(k) \quad (3)$$

where $n=1, 2, \dots, 2^{j-1}-1$. By doing so, we only need to store $y_j(k \times 2^{j-1})$ and $\Delta y_j(k)$, resulting in significant storage units reduction. However, there can be distortions on the WT outputs when this method is used, because we only approximate the WT outputs between $y_j(k \times 2^{j-1})$ and $y_j((k+1) \times 2^{j-1})$, instead of actual values. To alleviate this distortion, a compensation scheme is proposed. We compare the actual value $y_j(k \times 2^{j-1} + n)$ with the estimated value $\hat{y}_j(k \times 2^{j-1} + n)$. If the difference exceeds a pre-defined threshold T_d , then it is considered as a significant wavelet output, and the actual value of $y_j(k \times 2^{j-1} + n)$ is saved in the storage units. Otherwise, the actual value does not need to be saved, and (3) will be used to approximate it. For example, assume DHPF_S4 output is like Fig. 7(a), and then $y_4(2)$ and $y_4(6)$ are the significant WT

outputs. Therefore, only $y_4(0)$, $y_4(2)$, $y_4(6)$, $y_4(8)$ and $\Delta y_4(0)$ are needed to be saved, as shown in Fig. 7(b). The hardware implementation of PDWT & PDIWT is shown in Fig. 7(c). Before the signal processing of the next scale, the corresponding reverse procedure will be performed to interpolate the original data. By doing so, the significant wavelet coefficients can be maintained, and thus the distortions on PDWT can be minimized with some additional storage units. Furthermore, this method can also eliminate the issue of time variance in DWT.

It is worth to emphasize that for the lower scales WT, because the value of $2^{j-1}-1$ is smaller, the required number of storage units is also small. Therefore the proposed PDWT may not be necessary. For higher scales, on the other hand, the value of $2^{j-1}-1$ becomes large with j increasing, and thus the proposed PDWT is more desired. Fortunately, since the WT outputs of higher scales corresponds to signal components with lower frequency, the number of significant wavelet outputs tends to be small, and thus the required additional storage units is comparatively low.

D. Run-Length Compression with Threshold-Based Noise Suppression

Between ECG decomposition using PDWT and ECG reconstruction using PDIWT, there is huge number of synchronization delays for each scale, especially for the lower scales. It is because that the DHPF outputs of lower scales need to wait till the DHPF outputs of higher scales get ready, then they can be aligned to each other and fed into the WT reconstruction module [11], as shown in Fig. 8 (a). These huge numbers of storage unit result in large power and area consumption.

In our ECG signal processing system, the adaptive threshold based noise suppression scheme is proposed. The basic idea of this scheme is to force the DHPF output which is smaller than a threshold to zero. Therefore, after noise suppression, the DHPF outputs of low scales will be dominated by zeros and only small portion contains continuous non-zero values. Inspired from this fact, we propose the run-length data compression scheme cooperating with adaptive threshold-based noise suppression in Figs. 8 (b) and (c). The non-zero data will be stored in the storage units. Once continuous zeros are detected, a flag of writing 0 will be written into storage

units. Following that, a counter starts to count the number of zeros. Only when the next non-zero data is detected, the counted number of zeros is written into storage units, followed by the next non-zero data. At the input port of RHPF, once the flag of writing 0 is red out, the continuous “0” will be fed into RHPF according to the detected number of continuous 0. By this method, we naturally combine data compression with the threshold-based noise suppression to further reduce the required number of storage units of synchronization delays without signal distortion. This technique leads to great power and area reduction of the overall system.

IV. Low-Complexity Multi-Functional Cardiac Signal Analysis Scheme

In our ECG processor design, we propose a low-complexity multi-functional CSA scheme as shown in Fig. 9, which can perform $P/QRS/T$ detection, $P/QRS/T$ wave morphology identification, as well as $P-R/R-T/T-P$ interval calculation. The morphologies that can be detected include positive (+), negative (−), biphasic (+/− or −/+), only upwards (OU), and only downwards (OD). Benefiting from the fact that P wave, QRS complex, and T wave occur sequentially, and the analysis procedures are similar, we propose a sequential analysis scheme to minimize the operation clock frequency, and maximally reuse the hardware resource to reduce the required silicon area.

There are 2 levels of states transition. The 1st level state transition controls the searching behavior switching between P , QRS , and T segments. DHPF_S2 is used as the control signal to control the states transition. As shown in Fig. 9, the initial state is “ P Search”, and the state switches between “ P search”, “ QRS Search”, and “ T Search” under certain conditions. During state “ QRS Search”, high operation frequency is used, while the low operation frequency is used elsewhere.

The 2nd level state transition controls the detailed signal analysis flow. If the current 1st level state is “ P Search”, then the 2nd level state transition will detect the P wave and identify its morphology. According to [10], the morphologies of P wave includes positive (+), negative (−),

and biphasic (+/-, -/+). The basic idea is to examine the shape of the input DHPF_S4 waveform. The key points will be identified, such as positive peak, zero-crossing point, and negative peak. By checking the occurrence and sequence of these key points, the *P* wave and its morphology can be identified. This processing flow can be easily modified for *QRS* complex and *T* wave search as well.

From Fig. 9, it can be observed that the state transitions under each search segment can be represented by 9 states at most, and the transaction behaviors in different segments are similar. So we only need to set different parameter configurations for different search segment as shown in Fig. 9, and reuse the hardware resource for the 2nd level state transitions. Pipeline structure is also designed so that the required highest operation frequency is same as the input sampling rate.

For 2nd level state transition, we always use DHPF_S4 as signal inputs for all three search segments. Table I provides the ECG signal spectrum analysis based on WT decomposition of several ECG processing schemes. It can be observed that the major energy of the interesting characteristics always falls in 4th scale in our design. For *P/T* waves search, DHPF_S4 corresponds to 4 – 13.5 Hz because of 250 Hz sampling rate; whereas for *QRS* complex search, DHPF_S4 corresponds to 8 – 27 Hz because of 500 Hz sampling rate. This aligns with the analyses from other works in [4, 9, 10]. Therefore, although we always use DHPF_S4 in different search segments, the corresponding bandwidths are different, and we always choose the suitable signal bandwidth.

V. Circuit-Level Design Techniques of Proposed ECG Processor

A. Near-Threshold Operation

To further reduce the system power consumption, near-threshold circuit operation techniques are adopted to the overall system. The voltage of the digital logic and ADC is scaled down to 0.5 V which is close to the threshold voltage in the 0.18 μm CMOS technology. The I/O pads work at the standard 1.8 V/3.3 V. To enable near-threshold operation, the digital standard cell library is

reconstructed from a commercial library, by selecting the cells with relatively small delay and variation at ultra-low-voltages through extensive simulations. Following that, the reconstructed library is characterized at 0.5 V to obtain timing information for synthesis and back-end design. It is noted that since the total number of storage units is significantly reduced, we use the flipflop instead of SRAM to implement the storage units. By this way, the near-threshold operation can be applied to overall system without the need for ultra-low-voltage SRAM design.

B. Near-Threshold Level Shifter

To enable the near-threshold operation, a new level shifter is proposed to interface between the near-threshold and super-threshold regions. As shown in Fig. 10, the proposed level shifter is composed of two stages for fast level shifting at ultra-low supply voltages. Compared to the two-stage sub-threshold level shifter from [21], this structure provides shorter average delay with more symmetric rise and fall delay. For high-to-low transition, M_{N1} is switched off before M_{N2} is switched on due to the delay of the input inverter. The current flowing through both pull-down paths (M_{N1} & M_{P1} , M_{N2} & M_{P2}) are close to zero, causing low transconductance and long fall delay. For low-to-high transition, the M_{N2} is switched off after the M_{N1} is switched on. The overlapped on-time of M_{N1} and M_{N2} leads to high transconductance and short rise delay. A simple way to reduce the fall delay is to balance the arrival time of the non-inverted and inverted inputs by delaying the non-inverted input V_{IN} . However, this will increase the rise delay by reducing the overlapped on-time of M_{N1} and M_{N2} . In the proposed level shifter, a delay balancer composed of an inverter and a pull-down NMOS transistor M_{N6} is used to achieve short average delay with symmetric rise and fall delay. For high-to-low transition, M_{N1} is switched off before M_{N2} is switched on, but M_{N6} remains on until the second inverter flips. This increases the transconductance in the cross-coupled PMOS transistors during switching and reduces the fall delay. The overlapped on-time of M_{N2} and M_{N6} during fall transition may increase the short current slightly. However, the switching energy remains similar as the fall delay is reduced.

In addition to the asymmetric rise and fall delay, we propose a reconfigurable structure to improve delay for higher supply voltages. When operating in the near-threshold region, M_{P5} is disabled so that M_{N5} is in use to weaken the strong pull-up path for ultra low voltage level shifting. On the other hand, M_{P5} is enabled to bypass M_{N5} to achieve faster level shifting when operating in the super-threshold region. In addition, the proposed design utilizes the inverse narrow width effect (INWE) [22] to improve the switching speed and energy efficiency by employing minimum-width fingers to construct the pull-down transistors M_{N1} – M_{N4} and M_{N6} .

C. Glitch-Free Clock Switch

The dynamic switching of the clocks in the cognitive clock manager is conducted by the glitch-free clock switches as shown in Fig. 11. It has only one input control SEL, which is asynchronous to the input clocks, i.e., CLK1 and CLK2. To make the switching glitch-free, two-flipflop synchronizer is used to synchronize SEL to the clocks and make sure that one clock is switched off before the other is switched on.

VI. Chip Implementation & Experiment Results

The proposed ECG processor has been fabricated using a 0.18 μm CMOS process. The 0.18 μm process has relatively low leakage and process variation as compared to the more advanced CMOS process. This fact is especially beneficial for the near-threshold operation, such as our case. The chip micrograph and measured performance summary are provided in Fig. 12 and Table II, respectively. The supply voltage of the overall system is 0.5 V. The measured power consumption of ADC and DSPE are 22.7 nW and 435 nW, respectively.

Measurement results from a logic analyzer are shown in Fig. 13. The input ECG signal is distorted by noise and interference. It can be observed that the clean ECG with dynamic clock f_{OUT} is reconstructed after noise/interference suppression. $P/QRS/T$ identification (Indicator_ P , Indicator_ QRS , and Indicator_ T) and morphology detection can be correctly performed. The reconstructed ECG using f_{DSPE} is also presented, and we can observe some distortion due to the

dynamic change of clock frequency. It is the reason why the re-timing output buffer with f_{OUT} is used to correct the timing and remove distortion of the ECG processor outputs.

The performance of the proposed ADC is shown in Fig. 14. Fig. 14 (a) shows the measured ADC input, sampling clock f_{samp} , and ADC output from oscilloscope and logic analyzer, respectively, with 0.5 V supply voltage. We can observe that f_{samp} switches dynamically between 250 Hz and 500 Hz during P segment and QRS segment, respectively. In Fig. 14 (b), the ADC output spectrum at 500 S/s sampling rate is presented. The frequency of sinusoidal input is 20 Hz, which falls in the bandwidth of QRS complex. It can be observed that the signal-to-noise and distortion ratio (SNDR) is 50.5dB, which is equivalent to 8.1 ENOB.

The average delays of the proposed level shifter are shown in Fig. 15. The delay of the level shifters from [21] is also shown for comparison. Our proposed level shifter has much smaller transition delays when converting ultra-low voltages to the nominal voltage (1.8 V). The advantage is especially significant for the near-threshold voltages. In this design, our proposed level shifter can operate with small transition delay till 0.48 V.

Fig. 16 provides the power reduction breakdown figure of the proposed DSPE, to indicate the effectiveness of the proposed architecture-level and circuit-level power-saving techniques. For the comparison purpose, the baseline design is utilized as reference which can realize the same functions as our proposed design. The baseline design adopts NDWT, but none of the proposed techniques including cognitive clocking, PDWT, adaptive storing, DBRLC, and near-threshold operation. In Fig. 16, the power consumption values with various power-saving techniques are normalized against that of the baseline design. The corresponding power consumption values are also presented. By using global cognitive clocking scheme, the system power consumption can be reduced from 1 to 0.62. Furthermore, the adoption of PDWT / PDIWT, adaptive storing, and DBRLC reduce the system power consumption to 0.37 by reducing the number of required storage units. Combined with the near-threshold circuit design technique, a total power reduction of 96%

can be achieved. For the proposed ultra-low voltage ADC design, its power consumption is only around 5% of that for the ADC operating at nominal supply voltage (i.e., 1.8 V for 0.18 μm process) in simulation.

In Fig. 17, we present the performance comparison of our cardiac analysis scheme with some existing algorithms, in terms of the detection accuracy of *P* wave, *QRS* complex, and *T* wave. The ECG data from MIT-BIH database [14] is used, and the key performance indicator Sensitivity (Se) is adopted [4], defined by $Se = TP / (TP + FN)$, where TP and FN are the number of correct detection and the number of missing detection, respectively. The sensitivities of *P* wave, *QRS* complex and *T* wave of our design are 98.23%, 99.29%, and 98.71%, respectively. The proposed PDWT introduces distortion on the WT outputs as explained in Section III, which also affects the ECG detection performance. However, as explained in [23], the detection probability values greater than or equal to 95% for Se are desirable. Therefore, the performance of our proposed ECG processor is satisfying considering the low complexity and low power consumption that we can achieve. Our future research will focus on improving detection performance while maintaining ultra-low power consumption.

Table III provides the comparison between our proposed ECG processor design and other state-of-art designs. Our proposed ECG processor outperforms other designs in terms of power consumption, which is only 457 nW. At the same time, more comprehensive cardiac analysis functions can be realized by our design. As a result, our proposed ECG processor is more suitable for wearable and implantable long-term monitoring where the power budget is extremely critical.

VII. Conclusions

In this paper, we have presented an ultra-low power multi-functional ECG signal processor for long-term ECG monitoring system. To minimize power consumption, several architecture-level power-saving techniques are proposed. The novel global cognitive clocking scheme is proposed to dynamically adjust the operation clock frequencies of the entire system including ADC and DSPE,

according to the characteristic of the input signal. PDWT/ PDIWT, adaptive storing, and DBRLC are proposed to reduce the number of storage units and their access frequency. A low-complexity multi-functional CSA scheme is proposed to simplify the signal processing flow and hardware implementation, while archiving satisfying performance on comprehensive cardiac signal analysis. Several circuit-level design techniques are also proposed to further reduce the power consumption and achieve reliable performance, including ultra-low-voltage operation, wide-range level shifting, and glitch-free clock switching. This proposed ECG processor has been fabricated in 0.18 μm CMOS process. Benefiting from the aforementioned techniques, the total power consumption can be reduced by 96%, as compared to the conventional design. The proposed ECG processor is measured at 0.5 V, and consumes only 457 nW with higher than 98% detection performance, making it highly suitable for wearable sensor applications of long-term multi-functional ECG monitoring and diagnosis.

Reference:

- [1] Braunwald E., Heart Disease: A Textbook of Cardiovascular Medicine, Fifth Edition, p. 108, Philadelphia, W.B. Saunders Co., 1997.
- [2] S. -Y. Hsu, Y. Ho, Y. Tseng, T. -Y. Lin, P.-Y. Chang, J. -W Lee, J.-H. Hsiao, S. -M. Chuang, T. -Z. Yang, P. -C. Liu, T. -F. Yang, R. -J. Chen, C. Su, and C. -Y. Lee, "A sub-100 μ W multi-functional cardiac signal processor for mobile healthcare applications," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2012, pp. 156-157.
- [3] H. Kim, R. F. Yazicioglu, T. Torfs, P. Merken, H. -J. Yoo, and C. V. Hoof, "A low power ECG signal processor for ambulatory arrhythmia monitoring system," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2010, pp. 19-20.
- [4] C. I. Jeong, P. -I. Mak, C. -P. Lam, C. dong, M. -I. Vai, P. -U. Mak, S. -H. Pun, F. Wan, and R. P. Martins, "A 0.83- μ W QRS detection processor using quadratic spline wavelet transform for wireless ECG acquisition in 0.35- μ m CMOS," *IEEE Trans. Biomed Circuits Syst.*, vol. 6, pp. 586-595, 2012.
- [5] M. W. Phyu, Y. J. Zheng, B. Zhao, X. Liu, and Y. S. Wang, "A real-time ECG QRS detection ASIC based on wavelet multiscale analysis," in *IEEE Asian Solid-State Circuits Conference*, Nov. 2009, pp.293-296.
- [6] T. T. Hoang, J. P. Son, Y. R. Kang, C. R. Kim, H. Y. Chung, and S. W. Kim, "A low complexity, low power, programmable QRS detector based on wavelet transform for implantable pacemaker IC," in *Proc. IEEE International SOC Conference*, pp.160-163, 2006.
- [7] H. -M. Wang, Y. -L. Lai, M. C. Hou, S. -H. Liu, B. S. Yen, Y. -C. Huang, L. -C. Chou, S. -Y., Hsu, S. -C. Huang, and M. -Y. Jan, "A ± 6 ms -accuracy, 0.68 mm² and 2.21 μ W QRS detection ASIC," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2010, pp. 1372–1375.

- [8] R. A. Abdallah, and N. R. Shanbhag, “An energy-efficient ECG processor in 45-nm CMOS using statistical error compensation,” *IEEE J. Solid-State Circuits*, vol.48, pp. 2882-2893, Nov. 2013.
- [9] C. Li, C. Zhang, and C. Tai, “Detection of ECG characteristic points using wavelet transforms,” *IEEE Trans. Biomed. Eng.*, vol. 42, pp. 21-28, Jan. 1995.
- [10] J. P. Martínez, R. Almeida, S. Olmos, A. P. Rocha, and P. Laguna, “A wavelet-based ECG delineator: evaluation on standard databases”, *IEEE Trans. Biomed. Eng.*, vol. 51, pp. 570-581, Apr. 2004.
- [11] X. Liu, Y. J. Zheng, M. W. Phyu, B. Zhao, M. Je, and X. J. Yuan, “Multiple functional ECG signal processing for wearable applications of long-term cardiac monitoring,” *IEEE Trans. Biomed. Eng.*, vol. 58, no. 2, pp. 380–389, Jan. 2011.
- [12] X. Liu, J. Zhou, Y. Yang, B. Wang, J. Lan, C. Wang, J. Luo, W. L. Goh, T. T. –H. Kim, and M. Je, “A 457-nW Cognitive Multi-Functional ECG Processor,” *IEEE Asian Solid-State Circuits Conference*, 2013, pp. 141-144.
- [13] R. M. Rangayyan, *Biomedical Signal Analysis – A Case-Study Approach*, John Wiley & Sons, INC., 2001.
- [14] MIT-BIH Arrhythmia Database [Online]. Available:
<http://www.physionet.org/physiobank/database/mitdb>
- [15] J. L. Willems et al., “A reference data base for multilead electrocardiographic computer measurement programs,” *J. Amer. Coll. Cardiol.*, vol. 10, no. 6, pp. 1313–1321, 1987.
- [16] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. V. Hoof, “A 30 μ W analog signal processor ASIC for portable biopotential signal monitoring,” *IEEE J. Solid-State Circuits*, vol. 46, pp. 209-223, Jan. 2011.

- [17] J. H. Cheong, K. L. Chan, P. B. Khannur, K. T. Tiew, and M. Je, "A 400-nW 19.5-fJ/conversion-step 8-ENOB 80-kS/s SAR ADC in 0.18 μ m – CMOS" *IEEE Tran. on Circuits & System II*, vol. 58, no.7, pp. 407-411, July 2011.
- [18] S. K. Lee, S. -J. Park, H. -J. Park, and J. -Y. Sim, "A 21 fJ/Conversion-Step 100 kS/s 10-bit ADC with low-noise time-domain comparator for low-power sensor interface" *IEEE J. Solid-State Circuits*, vol.46, no.3, pp. 651-659, March 2011.
- [19] P. Chaovalit, A. Gangopadhyay, G. Karabatis, and Z. Chen, "Discrete wavelet transform-based time series analysis and mining," *ACM Comput. Surv.*, vol. 43, pp. 1–37, 2011.
- [20] S. Mallat and S. Zhong, "Characterization of signals from mutiscale edges," *IEEE Trans. Pattern Anal. Machine Intell.*, vol. 14, pp. 710-732, Jul. 1992.
- [21] S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An Energy-Efficient Subthreshold Level Converter in 130-nm CMOS," *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.57, no.4, pp. 290-294, April 2010.
- [22]J. Zhou, S. Jayapal, J. Stuyt, J. Huisken, H. Groot, "The impact of inverse narrow width effect on sub-threshold device sizing", *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2011.
- [23] AAMI, "References testing and reporting performance results of cardiac rhythm and ST segment measurement algorithms," Tech. Rep., 1998, Recommended Practice/Amer. Nat. Standard.

Figure caption:

Figure 1. System architecture of the cognitive ECG processor.

Figure 2. Morphology and significant characteristics of the ECG waveform.

Figure 3. Concept of the global cognitive clocking scheme: (a) conventional clocking, (b) cognitive clocking, (c) comparison between the conventional and cognitive clocking schemes in the ECG processing.

Figure 4. Block diagram of the global cognitive clocking scheme.

Figure 5. Ultra-low voltage ADC with adaptive clocking.

Figure 6. Hardware implementation of WT: (a). downsampling WT; (b). non-downsampling WT; (c). j^{th} scale DLPF.

Figure 7. PDWT/PDIWT and adaptive storing: (a) example of DLPF_S4 outputs, (b) data saved in storage units, (c) block diagram of PDWT/PDIWT and adaptive storing.

Figure 8. Run-length compression with threshold-based noise suppression: (a) WT decomposition and reconstruction, (b) compressed data in storage units, (c) processing flow using DBRLC.

Figure 9. Low-complexity multi-functional cardiac signal analysis scheme.

Figure 10. Schematic of the near-threshold level shifter.

Figure 11. Schematic of the glitch-free clock switch.

Figure 12. Chip micrograph.

Figure 13. Measurement results of the cognitive ECG processor.

Figure 14. Performance of the ultra-low-voltage adaptive ADC: (a) waveforms of ADC input and output, (b) ADC output spectrum.

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Figure 16. Power reduction breakdown using proposed techniques.

Figure 17. Performance comparison between different cardiac analysis schemes.

Table I. 3dB bandwidth of different WT scales

Table II. Measured performance summary

Table III. Comparison with the existing ECG processors

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Figure 17. Performance comparison between different cardiac analysis schemes.

TABLE I. 3dB BANDWIDTH OF DIFFERENT WT SCALES

	[4]	[9]	[10]	<i>This work</i>	
<i>f</i> (Hz)	300	250	250	250	500
WT S1	75 – 150	62.5 – 125	62.5 – 125	62.5-125	125-250
WT S2	21.6 – 70.2	18 – 58.5	18 – 58.5	18-58.5	62.5-125
WT S3	9.6 – 32.4	8 – 27 (QRS)	8 – 27 (QRS)	8-27	18-58.5
WT S4	4.8 – 16.2	4 – 13.5 (P/T)	4 – 13.5 (P/T)	4-13.5	8-27
QRS	S3	S1 – S4	S1 – S4	--	S4
P/T	--	S4	S4	S4	--

TABLE II. MEASURED PERFORMANCE SUMMARY

Chip Summary		
Process		CMOS 0.18 μm
Logic count (NAND2 equivalent)		115 k
Operation Frequency		3 kHz/6 kHz (ADC) 250 Hz/500 Hz (DSPE)
Supply Voltage		0.5 V (ADC & DSPE)
ADC	ENOB	8.10 bits
	Power	22.7 nW (@ 3 kHz/6 kHz)
DSPE	Input Signal	250/500 Sample/s, 9 bits
	Power	435 nW (@ 250 Hz/500 Hz)

TABLE III. COMPARISON WITH THE EXISTING ECG PROCESSORS

	This Work	[2]	[3]	[4]	[5]	[11]
Process (nm)	180	90	180	350	180	180
Sampling Rate (Hz)	3k/6k (ADC) 250/500 (DSPE)	125 – 1k	250-1k	300	1k	1k
Voltage (V)	0.5	0.5/1.0	1.8	1.8	1.8	1
Functions*	1-5	1 – 4, 6	1 – 3, 6	2	2	1 – 3
Power (μW)	0.022 (ADC) 0.435 (DSPE)	22.6/ 46.5	6	0.83	176	29

*Functions: (1) Noise/interference suppression; (2) *QRS* detection;
 (3) Clean ECG reconstruction; (4) *P/T* detection;
 (5) *P/QRS/T* morphology detection; (6) Encryption