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Kim, Tony Tae-Hyoung; Le Ba, Ngoc

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Design of a Temperature-Aware Low Voltage SRAM with Self-Adjustable Sensing Margin Enhancement for High Temperature Applications up to 300°C

Tony Tae-Hyoung Kim, *Senior Member IEEE*, and Ngoc Le Ba, *Student Member, IEEE*

School of Electrical and Electronic Engineering, Nanyang Technological University

Address: 50 Nanyang Avenue, Singapore, Singapore 639798

Primary Contact: Tony Tae-Hyoung Kim

School of Electrical and Electronic Engineering, Nanyang Technological University

Address: 50 Nanyang Avenue, Singapore, Singapore 639798

Phone: (65) 6790-4001, fax: (65) 6793-3318, email: thkim@ntu.edu.sg

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Abstract

This paper presents an 8-Kbit low power SRAM for high temperature (up to 300°C) applications. For reliable low voltage operation, we employed a decoupled 8T SRAM cell structure. To minimize the performance variations caused by the wide operating temperature range, supply voltage is selected in the near-threshold region. A temperature-aware bitline sensing margin enhancement technique is proposed to mitigate the impact of significantly increased bitline leakage on bitline swing and sensing window. A temperature-tracking control circuit generates bias voltage for optimal pull-up current for realizing the proposed

enhancement technique. Test chips were fabricated in a commercial 5 V, 1.0- μm SOI technology. Test chip measurement demonstrates successful operation down to 2 V at 300°C. The average energy of 0.94 pJ was achieved at 2 V and 300°C.

I. INTRODUCTION

The development of ruggedized electronics such as automotive, aerospace and Logging-While-Drilling (LWD) systems has demanded more robust integrated circuit solutions with reliable operation at high temperatures ($> 200^\circ\text{C}$) [1]-[4]. One of the most challenging issues in circuit design for high temperature operation is leakage, which increases exponentially with temperature. Silicon-on-Insulator (SOI) technology has been preferred for high temperature applications due to the feature of lower leakage compared with bulk CMOS technology [4]. The SOI technology significantly reduces the junction area and accordingly the leakage. Even though the leakage is improved dramatically by the SOI technology, it still becomes substantial at the temperature of 300°C, which is the target of this research work. In addition, special process technologies such as Silicon Carbide (SiC) CMOS and interconnect material of Tungsten have also been employed to enhance the reliability of the devices and interconnections at high temperature [6].

Several analog and digital circuits operating at the temperature up to 300°C have been demonstrated [2],[4],[6],[7]. Davis *et al.* implemented a 14-bit $\Sigma\Delta$ modulator in standard CMOS, which is capable of 14-bit resolution at 225°C [2]. A 300°C instrumentation amplifier was published in [7]. Chen *et al.* presented a Silicon Carbide CMOS driver circuit with the operating temperature of 300°C [6]. However, there have been very few memory solutions offering reliable operation up to 300°C except EEPROMs. Gogl *et al.* presented an EEPROM with the operating temperature up to 250°C with the aid of SIMOX technology

[1],[5]. In [4], Grella *et al.* experimentally demonstrated that EEPROMs can operate up to 400°C even though the threshold voltage window and the storage time are degraded dramatically. Recently, nano-electro-mechanical (NEM) devices using electromechanical contacts have been explored for high temperature data storage due to the ideally zero leakage current [8]-[10]. However, NEM devices have limitations in mechanical lifetime and physical dimension compared with CMOS devices. Therefore, they have not been widely accepted as a memory solution for high temperature applications.

One of the most popular memory solutions for providing computational capability is SRAM [11]-[24]. In this work, we present an 8-Kbit low power and low voltage SRAM for high temperature applications up to 300°C in 1.0- μm SOI process technology. A temperature-aware bitline sensing margin enhancement technique is proposed to augment the bitline sensing margin at a given operating condition. In addition, to minimize the performance variations caused by the wide operating temperature change, we adopted near-threshold operation where the overall variation in device current is minimized due to the complementary effect of temperature on mobility and threshold voltage. A part of this paper has been presented in [31]. In this paper, we present more comprehensive analysis at high temperature and the detailed operation of the proposed technique with additional measurement results. The rest of the paper consists of as follows. Section II discusses SRAM design challenges for high temperature operation. In section III, we present the proposed sensing margin improvement technique for low power and low voltage operation. Test chip implementation and measurement results are explained in section IV, followed by conclusions in section V.

II. DESIGN CHALLENGES IN LOW POWER SRAMS FOR HIGH TEMPERATURE APPLICATIONS

Leakage is the most critical factor limiting the implementation of reliable circuits and systems for high temperature ($> 150^{\circ}\text{C}$). A proper process technology has to be chosen considering the impact of high temperature on leakage. Device leakage is proportional to intrinsic carrier concentration (n_i or n_i^2) at high temperature while off-current is more dominant at lower temperature. The intrinsic carrier concentration is proportional to temperature due to the decreased bandgap. Therefore, devices with higher bandgap are preferred for high temperature applications to suppress the amount of leakage at the cost of additional process steps [1],[5],[6]. In addition, SOI technology has been widely accepted for high temperature operation [4]. In the SOI technology, the device junction area associated with silicon substrate can be minimized, consequently reducing leakage dramatically.

However, circuit techniques tackling performance variations coming from a wide temperature range are equally important as the device fabrication technologies. This is particularly true in SRAMs where leakage current plays a key role in overall performance [25]-[35]. One of the most critical operations affected by high temperature is bitline sensing since non-negligible bitline leakage exacerbates sensing margin [32]-[34]. Fig. 1 illustrates a simplified bitline structure using conventional 8T SRAM cells. The 8T SRAM cells are adopted to provide enough cell stability at low supply voltage. The 8T SRAM cell consists of a 6T SRAM cell and a dedicated read port for decoupling the cell nodes from the read bitline (RBL) during read operation. Since the cell disturbance from RBL is removed, the 8T SRAM cell shows improvement in stability and performance. However, the bitline sensing is still remained as a challenging task especially at high temperature where the amount of bitline leakage is significant compared to the cell read current. A read operation starts by asserting a read wordline (RWL), and this discharges RBL conditionally according to the accessed cell data. The worst case scenario for reading data '0' has the slowest RBL discharging speed of data '0'. This occurs when the rest cells sharing RBL store data '1', which produces

minimum bitline leakage (Fig. 1(a)). Similarly, the worst case scenario for reading data '1' shows the fastest RBL discharging speed of data '1'. This arises when the data in the rest cells is '0', producing maximum leakage (Fig. 1(b)). The difference in the RBL discharging speed forms RBL voltage at a given time and is detected by a sense amplifier.

However, at high temperature, the difference in the RBL discharging speed diminishes due to the exponentially increased bitline leakage. Therefore, the bitline sensing margin is also rapidly degraded. In addition, the time period for RBL sensing is exacerbated since the RBL discharging speed of data '1' becomes similar to that of data '0'. This is particularly problematic in single ended bitlines where sense amplifiers have to detect a threshold level for generating data '1' and '0'. An extremely careful sense amplifier activation and deactivation control is required for successful sensing.

Fig. 2 shows the impact of temperature and process variations on RBL under the worst case data patterns described in Fig. 1. As expected, the RBL discharging speed for data '1' increases substantially by raising temperature (Fig. 2(a)), deteriorating the sensing margin. Fig. 2(b) shows RBL waveforms over various corners at 300°C. Even though the RBL discharging speed for data '1' is high, the RBL still generates positive sensing margins in the simulated conditions. However, in the SNFP corner (Fig. 2(c)), the RBL discharging speed for data '0' at 27°C is slower than that of data '1' at 300°C, leading to negative a sensing margin and a read failure. Fig. 2(b) also shows the requirement of the accurate sense amplifier control since the RBL sensing operation has to be executed within a narrow time period. Consequently, securing acceptable sensing margins is tremendously challenging under the process variations and the wide operating temperature range as shown in Fig. 2(d). Therefore, temperature-aware design techniques for improved RBL sensing are highly demanded. Various circuit techniques have been proposed to improve the bitline sensing margin [28]-[30],[32]-[35]. Lo et al. introduced a P-P-N based 10T SRAM cell for improving

read stability and accordingly sensing margin by implementing a cross-coupled P-P-N inverter pair [28]. An L-shaped 7T SRAM and zigzag 8T SRAM were proposed for read bitline swing expansion and differential sensing [29], [30]. Verma et al. employed sense amplifier redundancy to improve the sensing capability of sense amplifiers [32]. This is only applicable when bitline sensing margin is high enough to be captured by the sense amplifiers with redundancy. If the bitline sensing margin is extremely small or negative, this scheme cannot be adopted. Kim et al. presented data-independent bitline leakage to improve the bitline sensing margin [33]. The main drawback of this scheme is requiring 10-T SRAM cells, which generates large area overhead. In [34], a differential sensing scheme was presented to augment sensing margin. However, it also used four additional devices, which is not acceptable in many high density SRAMs. Bitline equalization is proposed to achieve positive sensing margin regardless of the bitline length at the cost of additional two devices per SRAM cell [35]. To address the above challenges, in this work, we propose a circuit technique to enhance the RBL swing and the sensing timing window at a wide operating temperature range. The following section explains the details of the proposed circuit technique.

III. PROPOSED TEMPERATURE-AWARE SRAM DESIGN

SRAM operations are highly affected by a wide operating temperature range causing large amount of variations in leakage. Thus, temperature-aware design methodologies have to be mandatorily considered for robust SRAM operation. In this section, we present design techniques for implementing the proposed temperature-aware low voltage SRAM covering from optimal supply voltage selection for minimum variations to design techniques for bitline sensing margin enhancement.

A. Optimal Supply Voltage Selection

Low power consumption is achieved by scaling supply voltage. However, scaled supply voltage enlarges variations in device parameters. In addition, temperature changes have different effects on device leakage current and driving current. When a device is turned on, raising temperature reduces the driving current while it increases the leakage current exponentially. Therefore, supply voltage should be carefully chosen for reliable low power and low voltage SRAM operation with a wide operating temperature range. Fig. 3 shows the effect of temperature on the I-V characteristics of the devices used in the design. As expected, the current drivability is degraded in both NMOS and PMOS when the supply voltage (V_{DD}) is greater than 2.5 V. However, when V_{DD} is below 2.5 V, higher temperature shows higher current drivability, which is primarily explained by sub-threshold current. Note that the current drivability at 300°C is greater than that at 27°C by seven and five orders of magnitude in PMOS and NMOS, respectively (Fig. 3). Consequently, a minimum variation point is formed at the near-threshold region as shown in Fig. 3(b) and (d) where the positive temperature coefficient and the negative temperature coefficient compromise each other.

Fig. 4(a) explains the impact of temperature on digital circuits at various supply levels. Similar to the device IV characteristics, the delay of a digital logic circuit increases as V_{DD} is lowered and the temperature rises at high V_{DD} . However, at low V_{DD} , the ring oscillator operates in the sub- or near-threshold region, and the delay decreases dramatically by raising the temperature. Note that leakage current and sub-threshold current are exponentially proportional to the temperature. To minimize the impact of the wide operating temperature range (27°C ~ 300°C) on SRAM operation, we select a V_{DD} level producing minimum performance variation (μ/σ). Fig. 4(b) shows the effect of process variations on the minimum performance variation (σ/μ) point. The minimum σ/μ fluctuates over process corners. However, the effect of the process corners on the supply voltage for minimum performance variation is insignificant. In most corners except FF, the minimum σ/μ point is formed at

2.5V. In the FF corner, the minimum σ/μ is found at $V_{DD} = 2.0$ V. Consequently, V_{DD} of 2.5 V is considered as the minimum σ/μ point and the target V_{DD} range is set between 2V and 3V.

B. Cell Design

The conventional 8T SRAM cell structure is employed in this work due to the significantly improved cell stability compared with the 6T SRAM cell. Fig. 5 shows the schematic, the layout, and the butterfly curves of the designed 8T SRAM cell. The commercial SOI technology used in this work imposes two additional design constraints for reliable high temperature operation. First, VIAs and CONTACTs cannot be stacked. For example, to connect Metal2 to Poly, VIA1 (for connecting Metal2 to Metal1) and CONTACT (for connecting Metal1 to Poly) have to be placed at different locations. Second, each device must have a body contact. Note that all the devices (M1 ~ M8) have a body contact indicated by black boxes. These extra rules increase the cell layout size inevitably. Forward-body-bias (FBB) [13], [36] is adopted in the write access devices and read access device to boost the current drivability without any area penalty (Fig. 5(a)). The design SRAM cell occupies $56\mu\text{m} \times 10\mu\text{m}$ in the $1.0\mu\text{m}$ SOI technology (Fig. 5(b)). The butterfly curves in Fig. 5(c) illustrates the stability of the SRAM cell under process variation and temperature variation. Simulation shows the SNM of 961 mV at $V_{DD} = 2.5$ V.

C. Static Read Bitline (S-RBL)

A larger bitline voltage swing and a wider sensing timing window are desirable for reliable bitline sensing under variations. However, as explained in section II, this is extremely difficult to be achieved at high temperature. To tackle this issue, we propose circuit techniques facilitating both enhanced bitline swing and a widened sensing timing window.

Fig. 6 illustrates the principle of the proposed static read bitline (*S-RBL*) compared with that of the conventional RBL during read operation. In the conventional RBL (Fig. 6 (a)), RBL for both data ‘1’ and ‘0’ have only pull-down paths, discharging RBL with different speeds. The differences in the time constants (τ) for data ‘1’ and ‘0’ will determine the RBL swing and the sensing timing window, which will lead to failures (Fig. 2). However, in the proposed static RBL, we inject a pull-up path (R_{ref}) to prevent RBL from fully discharged to GND. The added pull-up path forms the RBL voltage at a level where the strength of R_{ref} and that of the pull-down network ($R_{cell} // R_{leak}$) are balanced. The theoretical RBL levels for data ‘1’ and ‘0’ are given in Fig. 6 (b). The difference between the RBL for data ‘1’ and that for data ‘0’ can be maximized by properly controlling the value of R_{ref} at given R_{cell} and R_{leak} .

The circuit implementation of the proposed *S-RBL* is illustrated in Fig. 7. The bitline structure is the same as the conventional 8T SRAM bitline structures. Compared with the conventional bitline structures, precharging operation is removed in the proposed *S-RBL* scheme since the RBL level is determined by static operation, not by dynamic operation. During read operation, a read wordline (RWL<i>)</i> is enabled and the RBL enhancing devices (M1, M2, M3, and M4) are turned on to provide the pull-up reference current (I_{ref}). The pull-up reference current (I_{ref}), the pull-down RBL leakage current (I_{lkg}), and the pull-down cell current (I_{read0} and I_{read1}) form the RBL levels for data ‘1’ and ‘0’. The worst case RBL level for data ‘1’ occurs with $I_{lkg-max}$ while that for data ‘0’ with $I_{lkg-min}$ as shown in Fig. 7. Fig. 8 presents a sample simulation result highlighting the feature of the proposed static RBL. It can be seen that the proposed *S-RBL* prevents RBL from being fully discharged to GND (Fig. 8(Left)). It provides larger RBL swing and a wider sensing window (Fig. 8(Right)). In contrast, extremely careful sensing control is required in the conventional bitline structure since the RBL is discharged to GND regardless of the read data and the RBL swing is smaller than that of *S-RBL*. Thus, sensing operation should be conducted within a tiny timing window,

causing the sense amplifier control circuit complex.

D. S-RBL Controller for Maximizing RBL Sensing Margin

To maximize the RBL sensing margin, the strength of the reference current (I_{ref}) need to be properly controlled. If the strength of I_{ref} is too high, the RBL levels will be formed at higher levels, reducing the sensing margin for data ‘0’ (Fig. 9(center)). In addition, the RBL swing ($V(\text{RBL of data ‘1’}) - V(\text{RBL of data ‘0’})$) is also deteriorated. Similarly, if the strength of I_{ref} is too low, the RBL levels are shifted to a lower level, decreasing the sensing margin for data ‘1’ (Fig. 9(right)). In this section, we introduce an S-RBL control circuit for adjusting the strength of I_{ref} so that the sensing margins for data ‘1’ and data ‘0’ are balanced.

The proposed S-RBL controller is illustrated in Fig. 10(a). It consists of two replica bitlines with hardwired data patterns (one for reading data ‘0’ and the other for reading data ‘1’), sense amplifiers (SAs), two counters, V_{ref} ladders, I_{ref} generating devices (MU1, MU2, ML1, and ML2), and basic logic gates. The upper loop tracks the maximum I_{ref} for sensing data ‘0’ and the lower loop traces the minimum I_{ref} for sensing data ‘1’. Fig 10(b) shows the simplified schematic of the hardwired replica bitlines. In each replica bitline, the worst case data pattern is implemented to calculate the worst case Bias0 and Bias1. The detailed operation of the controller is explained below. To detect the maximum I_{ref} for sensing data ‘0’, the down counter is initialized by RSTB with the minimum code, accordingly generating lowest voltage at Bias0. Once the replica bitline is enabled by EN_REF and a clock is applied, RBL0 is sensed by the sense amplifier (SA). Assuming the strength of I_{ref0} is too high, SA and the clock (CLK_REF) will increment the up-counter output and accordingly the Bias0 level. This operation loop will be repeated until RBL0 is sensed as data ‘0’ as shown in Fig. 10(b). After that, the clock and the incrementing operation of the up-counter are gated by the SA output. Similar operations are executed in the lower loop. In the lower loop, a down-

counter is utilized and it is initialized with the maximum code to generate minimum I_{refl} from highest Bias1 level. RBL1 is initially sensed as data ‘0’ due to the insufficient I_{ref} . This will decrement the down-counter output and the Bias1 level until RBL1 is high enough to be detected as data ‘1’. After detecting the Bias0 level for the maximum I_{ref0} and the Bias1 level for the minimum I_{refl} , the optimal bias voltage (Bias_Out) is obtained by taking the average of the two bias levels. This is simply implemented by connecting two V_{ref} latter outputs as shown in Fig. 10 (a). The generated Bias_Out is used in the main SRAM array to generate the optimal I_{ref} (Fig. 6) for the proposed sensing margin enhancement. Fig. 11 illustrates the above operation of the proposed control circuit.

The proposed RBL sensing margin enhancement technique is applicable to other state-of-the-art SRAM cells [12], [16], [25]-[34] without hurting their memory operations. For example, the 10T SRAM cells with low bitline leakage [12], [33], [34] can employ the proposed technique for further enhancing the RBL swing. The RBLs in those SRAMs are similar to the conventional 8T SRAM used in this work except the reduced leakage through the additional devices in the read ports. Therefore, the employment of the proposed technique will also implement static RBLs in those SRAMs, too. However, the area overhead of the 10T SRAM cells is too large to be practically adopted. The L7T and Z8T SRAM cells [29], [30] have different bitline structures compared to the conventional 8T SRAM cell. Due to the dynamic virtual ground control in the read ports, they implement static RBLs, which provides a better sensing window. However, the voltage level for data ‘0’ is highly affected by the temperature-dependent bitline leakage, significantly degrading the RBL swing at high temperature. In this case, we can provide well-controlled pull-down current for positioning the RBL swing around the sense amplifier’s trip point, which can be easily implemented by the proposed technique after minor modification (*i.e.* pull-down current instead of pull-up current). Consequently, the proposed sensing margin enhancement technique can further

improve the sensing margin of many state-of-the-art SRAMs without hurting the existing operation of the SRAMs. In addition, the proposed technique automatically set the amount of the optimal I_{ref} including the process variations of SRAM cells and sense amplifiers.

E. PVT Variation Tolerance of S-RBL

The effects of temperature and supply voltage on the bias voltages (Bias0 and Bias1) are presented in Fig. 12 and Fig. 13. As the temperature rises, both Bias0 and Bias1 rise slightly due to the different sensitivities of the PMOS and NMOS driving current to temperature (Fig. 12). It can be inferred that the current drivability of the PMOS devices (MU1, MU2, ML1, and ML2) in Fig. 10(a) increases faster than that of NMOS devices in Fig. 10(b). If the temperature coefficient of the PMOS devices is identical to that of the NMOS devices, Bias0 and Bias1 will not be affected by the temperature change. When the final optimal bias voltage, Bias_Out, is located between Bias0 and Bias1, successful RBL sensing could be achieved regardless of the operating temperature. In this work, the average of Bias0 and Bias1 is used to maximize the sensing margin for both data ‘1’ and ‘0’.

Fig. 13 summarizes the effect of supply voltage on Bias0 and Bias1. As supply voltage increases, Bias0 and Bias1 changes accordingly tracking the minimum I_{ref} and the maximum I_{ref} for improving the RBL sensing margin. Note that Bias1 at 300°C is 5 V with VDD = 5 V. This indicates that the leakage through the I_{ref} generating devices with Bias1 = 5 V is equal or larger than the minimum leakage current required at this condition. Therefore, the RBL level could be detected as data ‘1’ even with Bias1 = 5 V. In this case, the final Bias_Out is primarily determined by Bias0 generating the maximum required I_{ref} . Bias1 and Bias0 at higher temperature (300°C in Fig. 13) are always higher than those at lower temperature (80°C in Fig. 13) regardless of the VDD levels. This also corresponds to the result in Fig. 12.

Fig. 14 shows the impact of process variations on the RBL levels and the corresponding

Bias_Out. Even though process variations change the required I_{ref} , the proposed control circuit tracks the optimal I_{ref} points desirably under process variations and maintains the RBL levels for data ‘1’ and data ‘0’ without noteworthy fluctuations. However, Bias_Out varies more than RBL since the variations in the device parameters such as on-current and off-current have to be compensated by Bias-Out.

Mismatch between the replica bitlines and the SRAM affects the RBL swing of the proposed scheme. Fig. 15 illustrates the impact of the mismatch on the RBL swing. It is assumed that the replica bitlines are under the typical (TT) corner while varying the corners for the SRAM array. No significant degradation is observed when both NMOS and PMOS devices are degraded or improved in the same direction. However, large degradation occurs in the FNFP and SNFP corners. Particularly, the SNFP corner produces the RBL swing of 150 mV, which is too small to be sensed by single-ended sense amplifiers. In this case, the I_{ref} in the SRAM array is much stronger than that in the replica bitlines, pulling up the RBL levels upward. In addition, the cell current in the SRAM array is also worse than that in the replica bitlines, which further raise the RBL levels. In Fig. 15, the threshold voltage variation of ± 200 mV is assumed in the corners. However, this condition is very unlikely to happen when considering the amount of threshold voltage variations utilized in Fig. 15.

Fig. 16 demonstrates simulated RBL waveforms with the proposed scheme. The same conditions used in Fig. 2 are used for fair comparison. As expected, the RBL levels for data ‘1’ are maintained close to VDD (= 2 V) by supplying optimized I_{ref} . Even though the data levels for data ‘0’ have small offset voltage, they are insignificant in sensing due to the enhanced RBL swing. The proposed S-RBL also provides a wider sensing window. Since the RBL for data ‘1’ is not discharged to GND, S-RBL sensing margin will not be deteriorated during sensing. Therefore, the timing of sense amplifier deactivation can be relaxed. Note that, in the conventional bitline structures, RBL sensing should be executed within a small

sensing window where sense amplifier control is extremely challenging (Fig. 8).

IV. TEST CHIP IMPLEMENTATION AND MEASUREMENT

To validate and demonstrate the benefits of the proposed RBL sensing margin enhancement technique, an SRAM test chip with the array density of 8kb has been designed and fabricated in a commercial 1.0 μm SOI technology, including 3 tungsten interconnection layers for high temperature applications. Fig. 17 illustrates the overall architecture of the fabricated SRAM test chip. It consists of a memory controller, address decoding blocks, an SRAM array, read/write circuitry, and the proposed RBL controller. The SRAM array is configured with 128 rows and 64 columns. The multiplexers (Mux.) select 8 bits out of 64 bits for the 8 sense amplifiers. Similarly, the demultiplexers (Demux.) choose 8 bits out of 64 bits for the 8 write drivers. The output of the optimal bias generator (Bias_Out) for RBL sensing margin enhancement is connected to the pull-up current generation devices for RBL swing enhancement. The RBL controller including two replica bitlines can be positioned not only at the edges of the array but also at the center of the array for more realistic process variation tracking. Fig. 18 shows the die photo of the SRAM test chip. The proposed controller occupies 5% of the total area (5 mm $\times$ 2.5 mm). Note that increasing the density of the SRAM array will decrease the area overhead since the complexity of the proposed circuitry is independent of the SRAM array size.

Fig. 19 demonstrates the leakage of the test chip at various temperatures and supply voltage levels. As expected, the leakage increases exponentially with temperature rise. The leakage at VDD = 2.0 V is 5.5 nA at the room temperature. It becomes 82.4 μA at VDD = 5.0 V. At high temperature (*i.e.* 300 $^{\circ}\text{C}$), the leakage increases exponentially, generating 16.9 μA at 2.0 V and 270 μA at 5.0 V. The average power of the SRAM test chip is presented in Fig. 20 (applying 50% read and 50% write). At room temperature, the SRAM consumes 0.58 mW

at $V_{DD} = 2.0$ V and 12.2 mW at $V_{DD} = 5.0$ V. At 300°C , the average power becomes 0.94 mW at $V_{DD} = 2.0$ V and 35.5 mW at $V_{DD} = 5$ V. The clock frequency of 1 MHz is used in this power measurement. Fig. 21 shows the read access time measurement results. As expected, the access time increases by lowering V_{DD} . However, the slope of the access time varies according to the operating temperature. This is particularly substantial at low V_{DD} where the device current is highly sensitive to temperature. The measurement shows the minimum variation point at $V_{DD} = 2.5$ V when sweeping V_{DD} by a step of 0.5 V. From Fig. 20, it can be inferred that the actual minimum variation point will be formed at a point at $V_{DD} \cong 2.3$ V. This result corresponds to the simulation result in Fig. 3. The variation in the access time of $V_{DD} = 2.5$ V is 28ns while that of 2 V and 5V is 84ns and 35ns, correspondingly. At $V_{DD} = 2$ V, the access time is 340ns at room temperature and 256ns at 300°C . At $V_{DD} = 5$ V, it becomes 33ns at room temperature and 68ns at 300°C , showing the opposite trend of $V_{DD} = 2$ V. The measured energy is presented in Fig. 22. At The energy consumption of 0.58 nJ is achieved at 2.0 V and room temperature. It becomes 0.94 nJ at 2.0 V and 300°C . At the minimum variation point ($V_{DD} = 2.5$ V), the energy of 0.68 nJ is obtained and it becomes 16.2 nJ at 300°C . No minimum energy point was found in the near- or sub-threshold region since the SRAM fails to operate earlier. Fig. 23 shows sample measured waveforms at $V_{DD} = 2.5$ V. Table I summarizes the SRAM test chip results.

V. CONCLUSIONS

This paper has presented design techniques for low voltage SRAMs requiring high temperature operation up to 300°C . For robust low voltage operation under the required wide range of temperature ($25^{\circ}\text{C} \sim 300^{\circ}\text{C}$), a minimum performance variation point is chosen as a target design point. In addition, we proposed circuit techniques for enhancing bitline sensing margin at low voltage and high temperature. The proposed static read bitline (S-RBL)

improves not only the RBL swing but also the sensing timing window. A PVT-tracking controller is implemented to generate bias voltage (Bias_Out) for optimizing the pull-up reference current (I_{ref}). A SRAM test chip was fabricated in a commercial 1.0 μm SOI process technology. Tungsten metal interconnections are provided by the technology for device reliability at high temperature. The test chip was successfully demonstrated to operate at 300°C with $V_{DD} = 2\text{ V}$ ($V_{DD_NOM} = 5\text{ V}$).

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(a)

(b)

(c)

(d)

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(a)

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TABLE I
SUMMARY OF THE TEST CHIP.

Technology	1 μ m SOI
Supply Voltage	2 ~ 5 V
Array Density	8 kb
# of Cells per BL	128 cells
SRAM Cell Type	8T
Chip Size	4.9 mm $\times$ 1.9 mm
Cell Size	56 μ m $\times$ 10 μ m
Power (CLK=1MHz)	0.94 mW @ 2.0 V, 300°C
Leakage	16.9 μ A @ 2.0 V, 300°C
Energy	0.94nJ @ 2.0 V, 300°C

Figure Captions

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