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Five-Level Multiple-Pole Multilevel Diode-Clamped Inverter Scheme for Reactive Power Compensation

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Abstract—This paper proposes a space vector modulation based dc-link capacitor voltage balancing technique for a five-level multiple-pole multilevel diode-clamped (M2DCI) inverter. The new five-level inverter contains lesser number of clamping diodes compared to the conventional five-level diode-clamped inverter (DCI) topology and does not require any extra balancing circuits to maintain balanced voltages across the four dc-link capacitors. The effect of load power factor and modulation indices on voltage balancing strategy has been studied, and the stability region for five-level M2DCI is determined based on investigation done in the Matlab/Simulink® and PSIM environment during balanced, unbalanced and distorted load conditions. The proposed reduced device topology with SVM technique, which self balances the dc-link capacitors can be very attractive for reactive power control in a grid connected environment.

Index Terms—Active balancing circuit, five-level NPC inverter, multilevel inverter, neutral point potential, SVM.

I. INTRODUCTION

Diode-clamped multilevel inverter (DCI) for more than three-level (3-L) operation is less attractive due to dc-link capacitor voltage unbalancing issues and increased losses. In an n-level DCI, $(n-1) \times (n-2)$ clamping diodes connected in series per-leg will generate high reverse recovery current during commutation which increases the conduction losses and even affect the switching losses of other devices [1, 2]. A converter topology with minimum number of series connected devices which share the total voltage equally between the semiconductors and new multilevel modulation schemes, which utilizes more number of levels, redundant voltage vectors and zero common mode voltage vectors available in higher level DCI can be used together to solve the above mentioned issues in higher level DCI [3, 4].

The space vector modulation (SVM) based multilevel algorithms have the potential to achieve dc-link capacitor voltage balancing, common-mode voltage elimination,

reduction in switching frequency and THD over carrier-based PWM schemes [3, 5]. The SVM involves the following steps for generating the PWM signals: initially, the three nearest vectors surrounding the reference space vector is obtained, then their duty ratios are calculated and are switched in a sequence over one sampling time to generate a stepped waveform which best matches the three phase reference voltages.

The main challenge in operating with five-level (5-L) DCI is to retain the voltage across the dc-link capacitors to '1/4' times the total dc-link voltage during steady-state and transient operations. A transformer with isolated secondary windings connected to individual capacitors through diode-bridge rectifiers can eliminate voltage drift phenomena but will makes the system heavier and inefficient. An active balancing circuit proposed by Newton *et al* in [6, 7] gives balanced capacitor voltages during motoring and regenerative modes, however increases the system cost especially at high power levels.

The work presented in this paper proposes a SVM based voltage balancing strategy for a new 5-L multiple-pole multilevel diode-clamped inverter (M2DCI) topology to eliminate the voltage drift phenomena. The 5-L M2DCI topology proposed in [8] is derived from 3-L DCI topology and uses lesser number of clamping diodes compared to the classic 5-L DCI. The voltage balancing strategy is developed from the switching function model of 5-L M2DCI and involves reduced number of calculations at each sampling period compared to the sector based method presented in [9]. The stability region for M2DCI with the balancing technique is obtained from simulation studies done in Matlab/Simulink and PSIM environment during balanced, unbalanced and distorted load conditions. The proposed reduced device topology together with SVM based capacitor balancing scheme can fit in reactive power applications by reducing the system size, weight and losses.

5-L M2DCI

Figure. 1 (a) Proposed SVM based capacitor voltage balancing of 5-L M2DCI (b) Classical 5-L DCI configuration showing phase A.

II. PROPOSED SVM BASED VOLTAGE BALANCING SCHEME FOR FIVE-LEVEL M2DCI

Clamping diodes in classical 5-L DCI shares unequal voltage stress during each switching state and to distribute the voltage stress equally, 12 diodes per-leg are required. While in 3-L DCI, all semiconductor devices share equal voltages in each switching states. The M2DCI proposed by authors in [8] generates 5-L output waveform by cascading multiple-poles of 3-L DCI by using lesser number of clamping diodes compared to the classic 5-L DCI. And level-shifted triangular waves are used to generate the stepped output waveforms. Fig.1 (a) shows the schematic of the proposed SVM based capacitor voltage balancing of 5-L M2DCI. The 5-L M2DCI generates per-phase multilevel structure by combining two-poles of 3-L DCI. The redundant switching states are not shown in space vector representation to reduce the complexity. The space vector modulator block generates the

TABLE I
SWITCHING STATES AND POLE VOLTAGE OF A 5-LEVEL M2DCI
(X=A,B,C)

Level	Switching states				Pole Voltage
L_X	S_{X1}	S_{X2}	S_{X3}	S_{X4}	(V_{X2})
4	ON	ON	ON	ON	$E_{dc}/2$
3	OFF	ON	ON	ON	$E_{dc}/4$
2	OFF	OFF	ON	ON	0
1	OFF	OFF	OFF	ON	$-E_{dc}/4$
0	OFF	OFF	OFF	OFF	$-E_{dc}/2$

switching signals for the 5-L M2DCI correspond to the reference modulating signal parameters 'm' and 'theta'. The SVM based voltage balancing algorithm also requires dc-link capacitor voltages, load currents and dc-link voltage to maintain balanced voltage across the dc-link capacitors and to generate the required three-phase output voltage at the inverter terminals. Fig.1 (b) shows the per-phase

TABLE II

SPECIFICATION OF THE 5-LEVEL INVERTER SYSTEM

DC-Link voltage, E_{dc}	340V
DC-Link capacitor, C_j , $j=1,2,3,4$	2200 μ F $\pm$ 20% tolerance and ESR=100m Ω
Sampling Frequency, f_s	4kHz
Load current Amplitude, $I_{L, peak}$	5A
Frequency	50Hz

configuration of classical 5-L DCI. The switching states and the corresponding pole voltages of 5-L M2DCI are given in Table I. The maximum voltage stress on clamping diodes in 5-L M2DCI is $\frac{1}{4}E_{dc}$, whereas in conventional 5-L DCMI it was $\frac{3}{4}E_{dc}$. Hence the new topology will reduce the number of clamping diodes as well as voltage stress across clamping diodes compared to classic 5-L DCI shown in Fig.1 (b). The following section describes the capacitor voltage unbalancing issue in 5-L M2DCI and shows how a SVM based voltage balancing algorithm is developed to eliminate this voltage drift phenomena.

A. DC-Link Capacitor Voltage Unbalancing

For the valid switching states from Table I, the dc-link capacitor currents i_{Cj} can be written in terms of load current and switching states as

$$i_{Cj} = S_{Aj}i_A + S_{Bj}i_B + S_{Cj}i_C - i_{in} \quad \text{for } j = 1, 2, 3, 4. \quad (1)$$

Where i_{in} is the current supplied by the dc-source.

If all the capacitors are assumed to have equal magnitude, the current through the mid-point between dc-link capacitors are responsible for capacitor voltage change as given in (2).

$$\Delta V_j = V_{Cj+1} - V_{Cj} = \frac{1}{C} \int i_{j+1} dt. \quad \text{for } j = 1, 2, 3. \quad (2)$$

And the mid-point currents generated during each valid switching state are given in (3)

$$i_j = (S_{Aj} - S_{A,j-1})i_A + (S_{Bj} - S_{B,j-1})i_B + (S_{Cj} - S_{C,j-1})i_C \quad (3) \\ \text{for } j = 2, 3, 4.$$

Hence from (2), by controlling the average value of mid-point currents over one sampling time, the voltage unbalancing can be minimized.

B. SVM based Voltage Balancing Control

The total energy of the capacitors in 5-L M2DCI is

$$E = \frac{1}{2} \sum_{j=1}^4 C_j V_{Cj}^2 \quad (4)$$

When all the capacitor voltages are equal to the desired dc magnitude, (4) gives a minimum value. And a cost function given in (5) is used to select the combination of best redundant switching vectors over one sampling time which gives minimum value for (4) [10].

Figure. 2 Voltage balance limits for SVM-based capacitor voltage balancing strategy of 5-L M2DCI.

$$G(t) = C \sum_{j=1}^4 \Delta V_{Cj} i_{cj} = 0 \quad (5)$$

Let V_s represents the reference voltage space vector to be generated at the inverter terminals. V_1, V_2, V_3 are the nearest three voltage vectors and d_1, d_2, d_3 are their respective duty ratios obtained from [11]. Then the average mid-point currents $\bar{i}_j$ are calculated by (6)

$$\bar{i}_j = i_{j,V_1} \times d_1 + i_{j,V_2} \times d_2 + i_{j,V_3} \times d_3 \quad \text{for } j = 2, 3, 4. \quad (6)$$

$i_{j,V_1}, i_{j,V_2}, i_{j,V_3}$ are the mid-point currents calculated from (3) while switching one redundant vector from each vector group V_1, V_2, V_3 respectively. Then, by representing capacitor currents in terms of mid-point currents and averaging the cost function over one sampling time assuming constant capacitor voltages, (5) becomes

$$\sum_{j=1}^3 \Delta V_{Cj}(k) \left(\sum_{x=j+1}^4 \bar{i}_x \right) \geq 0 \quad (7)$$

Here $\Delta V_{Cj}(k) = V_{Cj} - (E_{dc}/4)$ is the voltage error of j^{th} capacitor C_j at the beginning of the sampling interval T_s , and $\bar{i}_x$ is the average value of mid-point current over that period. The switching set which maximizes (7) is selected for generating gate signal for the converter, and is arranged in sequence such that minimum number of switch transition takes place in one sampling period.

III. PERFORMANCE EVALUATION OF VOLTAGE CONTROL STRATEGY

To evaluate the performance of the proposed SVM based voltage control strategy of 5-L M2DCI, a constant DC source is connected at the dc side of the inverter and three-phase RL load is connected at the ac side of the inverter. The whole system is co-simulated between Matlab/Simulink® and PSIM environment. The system parameters are given in Table II. To

Figure 3. M2DCI waveforms with balanced load operating at PF=1 and $m=0.5$ (Stable operating point "A").

Figure 4. M2DCI waveforms with balanced load operating at PF=1 and $m=0.65$ (unstable operating point "B").

Figure 5. M2DCI waveforms with balanced load operating at PF=0.35 and $m=0.9$ (Stable operating point "C").

- (a) Line voltage, V_{AB} .
- (b) Line currents i_{ABC} .
- (c) dc-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$.

obtain the limits of the proposed voltage balancing strategy for the M2DCI, simulation is done at various load power factor angles and modulation indexes. The stability region obtained is shown in fig.2. The voltage balancing control fails to provide equal voltage sharing of dc capacitors when the converter operating point is above the solid line in fig.2. To verify this, the simulation results for balanced, unbalanced and distorted load conditions are presented in subsequent sections.

A. Balanced Load Condition

The M2DCI waveforms corresponding to operating points 'A', 'B' and 'C' as marked in fig.2 at balanced load condition

Figure 6. M2DCI waveforms with unbalanced load operating at PF=0.35 and $m=0.9$ (Stable operating point "C").

Figure 7. M2DCI waveforms with distorted load (20% of 3rd harmonic) operating at PF=0.35 and $m=0.9$ (Stable operating point "C").

Figure 8. M2DCI waveforms with distorted load (20% of 3rd and 10% of 5th harmonics) operating at PF=0.35 and $m=0.9$ (Stable operating point "C").

- (a) Line voltage, V_{AB} .
- (b) Line currents i_{ABC} .
- (c) dc-link capacitor voltages V_{Cj} for $j=1, 2, 3, 4$.

are shown in figs.3, 4 and 5 respectively. At unity power factor (PF=1), when load is assumed as linear and balanced, the control algorithm will provide a balanced voltage across dc-link capacitors for modulation index of $m=0.5$ (point "A" on fig.2) as shown in fig.3. The line voltage waveform shown in fig.3.(a) has five distinct levels 170, 85, 0, -85 and -170V. Three-phase output currents are shown in fig.3.(b). It can be seen from fig.3.(c) that the dc-link capacitor voltages reach a steady-state value around 85V with balancing control.

When modulation index has increased above $m=0.53$, the capacitor voltages are uncontrollable and hence line voltages are distorted. The inverter waveforms corresponding to

unstable operating point “B” on fig.2 ($m=0.65$ and $PF=1$) are shown in fig.4. Since the inverter operating point lies in the unstable region, the top and bottom capacitors will charge continuously to reach 170V and the two middle capacitors will discharge towards 0V as shown in fig.4.(c).

As the load power factor angle has increased to 69.51° ($PF=0.35$) with $m=0.9$ (point “C” on fig.2), the dc-link capacitors converges to a voltage of $E_{dc}/4$ which is equal to 85V [fig.5.(c)] ensuring that, when the converter operates at stable operating points, the balancing algorithm eliminates the voltage drift phenomena in M2DCI. Fig.5 shows the inverter waveforms at operating point $m=0.9$ and $PF=0.35$. The capacitors are balanced and converter output voltage V_{AB} gives 9 levels.

B. Unbalanced Load Condition

The operating points mentioned in the balanced load conditions are simulated with unbalanced load currents (12% unbalance) of amplitudes $\hat{I}_A = 5.6A$, $\hat{I}_B = 5A$ and $\hat{I}_C = 4.4A$ to verify the effectiveness of proposed SVM based capacitor voltage balancing control. And it was observed that, the stability region remains constant even for unbalanced load condition. The inverter waveforms corresponding to operating point “C” on fig.2 ($PF=0.35$ and $m=0.9$) are shown in fig.6. Fig.6.(a) shows, the line voltage waveforms when 340V is applied at the dc-link, while the load current waveforms and individual capacitor voltages are shown in figs.6.(b) and (c) respectively. The capacitors are balanced and the line voltage waveform V_{AB} has 9 levels.

C. Effect of Harmonics

Non-linear loads connected at inverter terminals generate harmonics in output currents. Hence to study the performance of proposed SVM-based balancing strategy, three phase current sources are connected at the ac side of the inverter to generate distorted load currents. Fig.7 shows the M2DCI waveforms with 20% third order harmonic current injection. The fundamental component amplitude is 5A. Fig.8 depicts the converter waveforms with 20% of third order harmonic and 10% of fifth order harmonic current injection. In both cases, the dc-link capacitor voltages are balanced and give a steady state voltage of 85V and converter output voltage V_{AB} gives 9 levels. .

IV. CONCLUSION

This paper proposes a space vector modulation based voltage balancing strategy for a 5-L M2DCI without using any extra hardware. The switching signal model of five-level M2DCI is derived to predict the dc-link capacitor currents by sensing the load currents which reduces the number of calculations per sampling period to implement the proposed voltage control technique when compared to conventional sector based SVM techniques. A comprehensive set of simulation results are also presented to verify the proposed technique operating at balanced, unbalanced and distorted load conditions. It is found that to achieve capacitor balancing, modulation index is restricted to about 60% of its maximum value when loads of high power factor i.e $PF \geq 0.8$ is

connected at the inverter terminals. Hence the proposed reduced device topology with SVM technique, which self balances the dc-link capacitors can be very attractive for reactive power control in a grid connected environment. The proposed converter with significant reduction in clamping diodes/phase and elimination of balancing circuit will improve the performance of the system by reducing the converter losses, size, weight, cost and THD.

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